APPLICATION NOTE – REFERENCE DESIGN

MODEL NAME：3.7inch e-Paper

2 bit B/W/DG/LG

1 About This Application Note

This document describes a reference design system that integrates E Ink's black, white, dark gray and light gray 3.69" display (3.7inch e-Paper). It includes an application circuit, timing information and pin assignments for the ePaper display module.

2 Overview

This display is a 280x480 ePaper display with integrated timing control and power management circuitry. Each pixel on the display has the capability of showing black, white, dark gray and light gray. The 3.7inch e-Paper is ideal for applications such as signage for retail pricing.

3 Device Interface

This chapter describes the interface and pin assignments of the3.7inch e-Paper panel.

Table 1 Pin descriptions for 3.7inch e-Paper

Pin Assignment			
Pin #	**Type**	**Single**	**Description**
1		NC	No connection and do not connect with other NC pins
2	O	GDR	N-Channel MOSFET Gate Drive Control
3	O	RESE	Current Sense Input for the Control Loop
4		NC	No connection and do not connect with other NC pins
5	P	VSH2	Positive source driver voltage for Red
6	O	TSCL	I2C Interface to digital temperature sensor Clock pin
7	I/O	TSDA	I2C Interface to digital temperature sensor Date pin
8	I	BS	Bus selection pin; L: 4-wire IF. **H: 3-wire IF. (Default)**
9	O	BUSY_N	Busy state output pin
10	I	RST_N	Reset
11	I	DC	Data /Command control pin
12	I	CSB	Chip Select input pin
13	I	SCL	serial clock pin (SPI)
14	I/O	SDA	serial data pin (SPI)
15	P	VDDIO	Supply voltage
16	P	VCI	Supply voltage
17	P	VSS	Ground
18	P	VDD	Core logic power pin
19		VPP	OTP Program power
20	P	VSH1	Positive Source driving voltage
21	P	VGH	Positive Gate driving voltage
22	P	VSL	Negative Source driving voltage
23	P	VGL	Negative Gate driving voltage
24	P	VCOM	VCOM driving voltage

I: Input Pin; O: Output Pin; I/O: Input/Out Pin; P: Power Pin

3.1 3-Wire SPI and 4-Wire SPI setting

Please follow below table for SPI HW setting that you want use

BS	Interface	CSB	DC	SCL	SDA
High	**3-wire SPI**	High	Low	High	High
Low	**4-wire SPI**	High	High	High	High

3.2 SPI Interface Timing

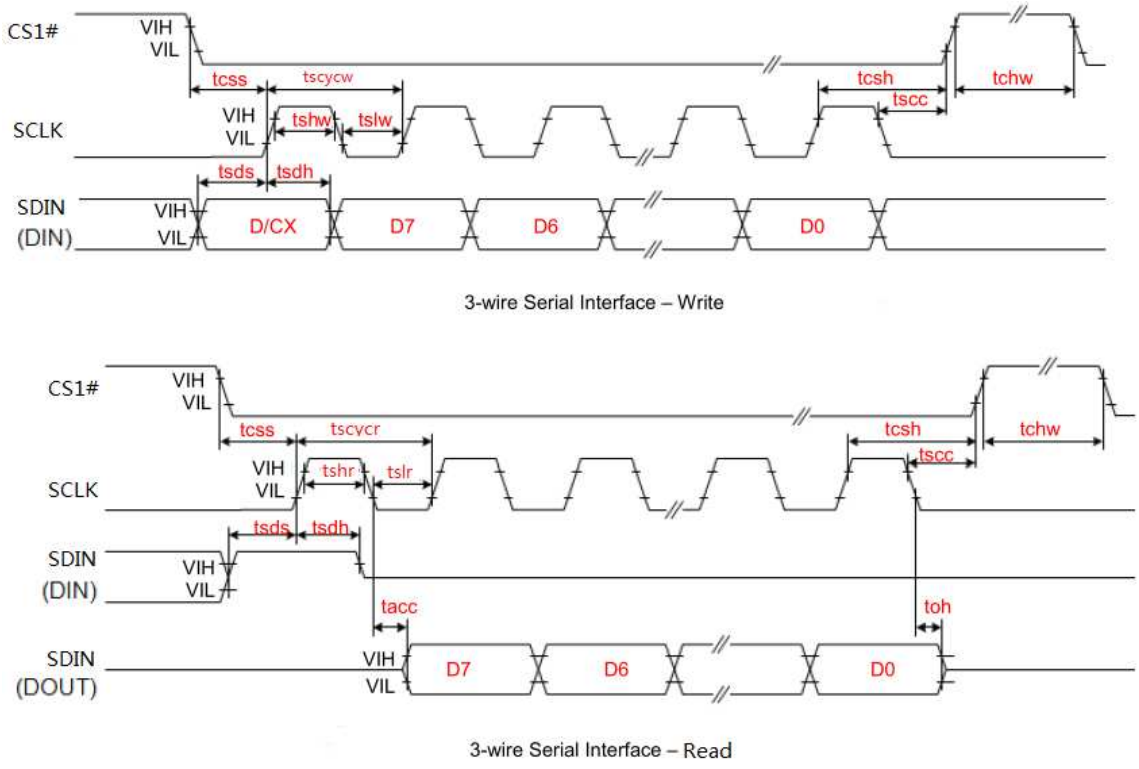


Figure 1 3-wire SPI Timing Diagram

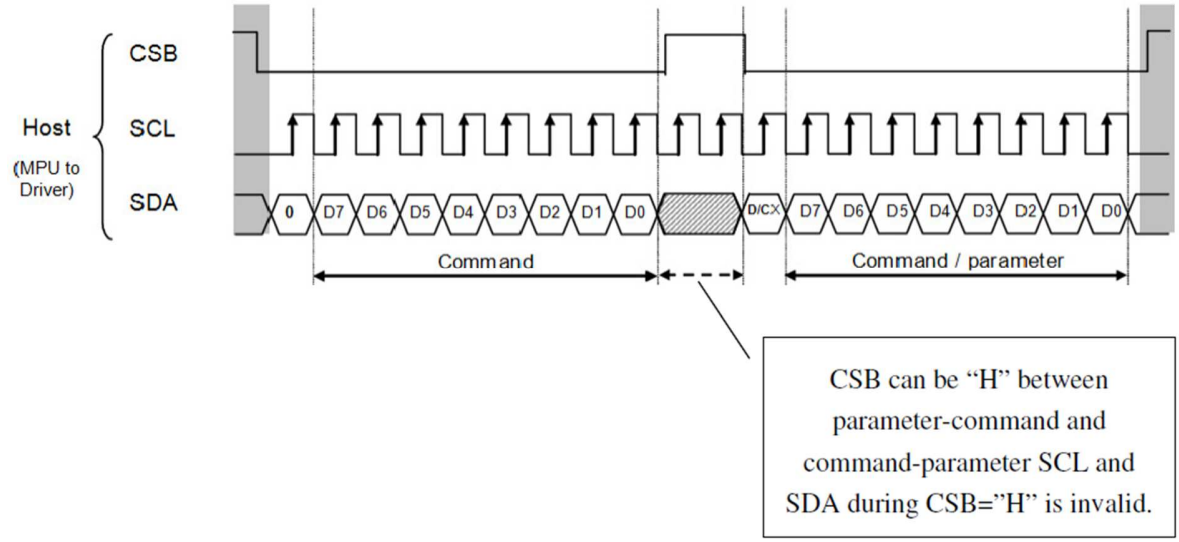


Figure 2 Host Communications Timing Diagram

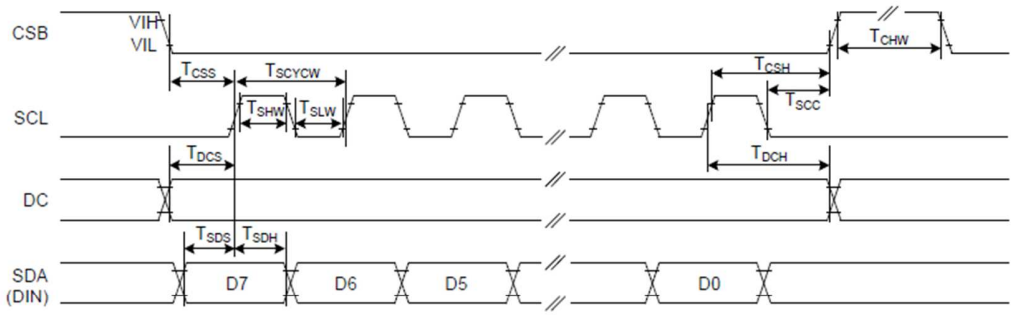


Figure: 4-wire Serial Interface Characteristics (Write mode)

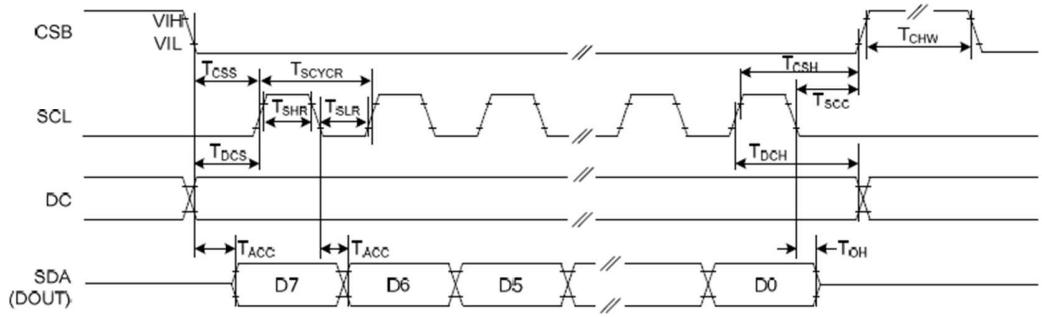


Figure: 4-wire Serial Interface Characteristics (Read mode)

Figure 3 4-wire SPI Timing Diagram

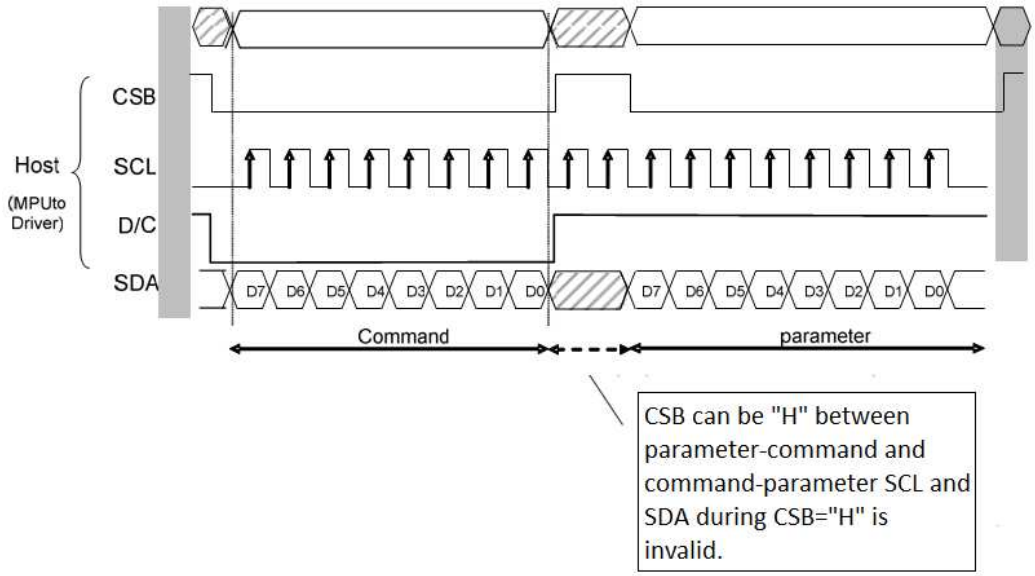
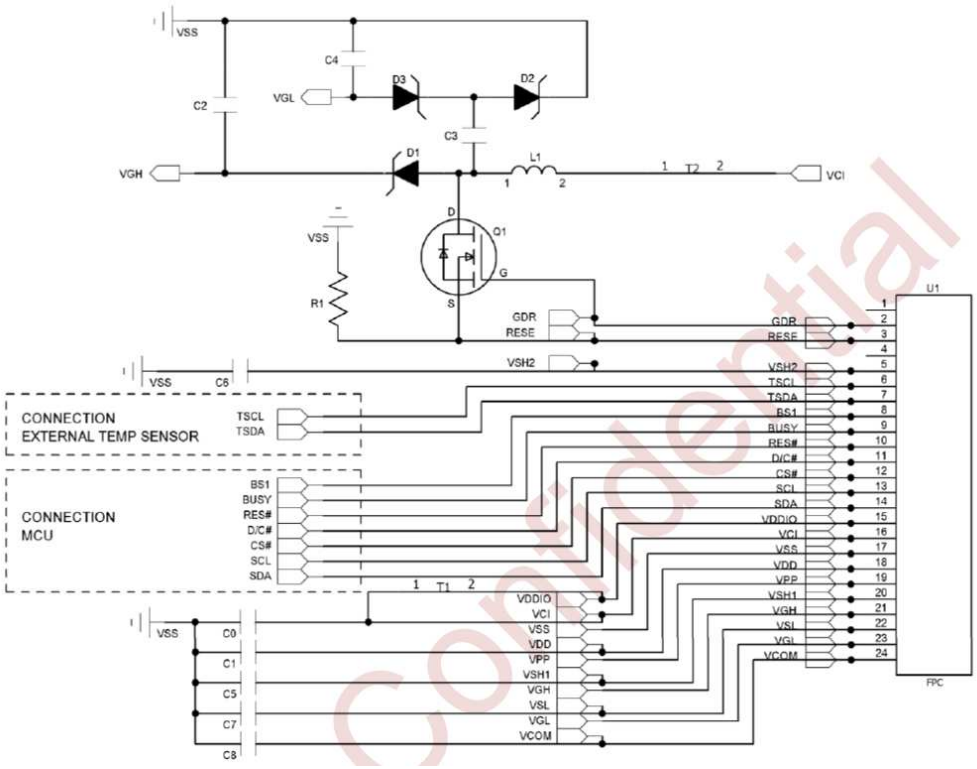


Figure 4 Host Communications Timing Diagram

Symbol	Signal		Min	Typ	Max	Unit
SERIAL COMMUNICATION						
tCSS	CSB	Chip select setup time	60			ns
tCSH		Chip select hold time	65			ns
tSCC		Chip select setup time	20			ns
tCHW		Chip select setup time	40			ns
tSCYCW	SCL	Serial clock cycle (Write)	100			ns
tSHW		SCL “H” pulse width (Write)	35			ns
tSLW		SCL “L” pulse width (Write)	35			ns
tSCYCR		Serial clock cycle (Read)	150			ns
tSHR		SCL “H” pulse width (Read)	60			ns
tSLR		SCL “L” pulse width (Read)	60			ns
tSDS	SDA (DIN) (DOUT)	Data setup time	30			ns
tSDH		Data hold time	30			ns
tACC		Access time			10	ns
tOH		Output disable time	15			ns

Table 2 Timing Table

4 Reference circuit



Part Name	Value	Reference Part/ Requirement
C0-C1	1uF	0603; X5R/X7R; Voltage Rating 6V
C2-C7	4.7uF	0805; X5R/X7R; Voltage Rating 25V
C8	1uF	X7R; Voltage Rating 25V
R1	2.2 Ohm	0805; 1%

Figure 5 3.7inch e-Paper Reference Circuit

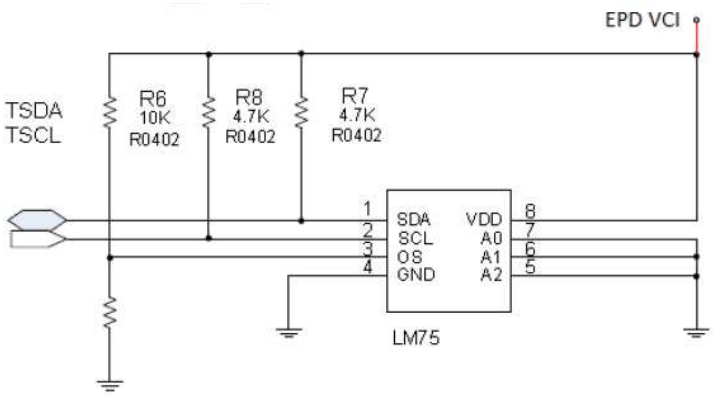


Figure 6 Temperature Sensor Circuit (optional)

5 Software Programming Guide

This chapter describes image update flow of 3.7inch e-Paper. Defining the pin connection between MCU and the display is needed. The definition is customized in the file ”pindefine.c” User only need to assign the MCU pins to connect the pins defined in this file. The definition is shown in figure 7. When the pin define setting is done, the display is automatically controlled by the function. The next two sections will describe the simulation of SPI transmission protocol and image update flow.

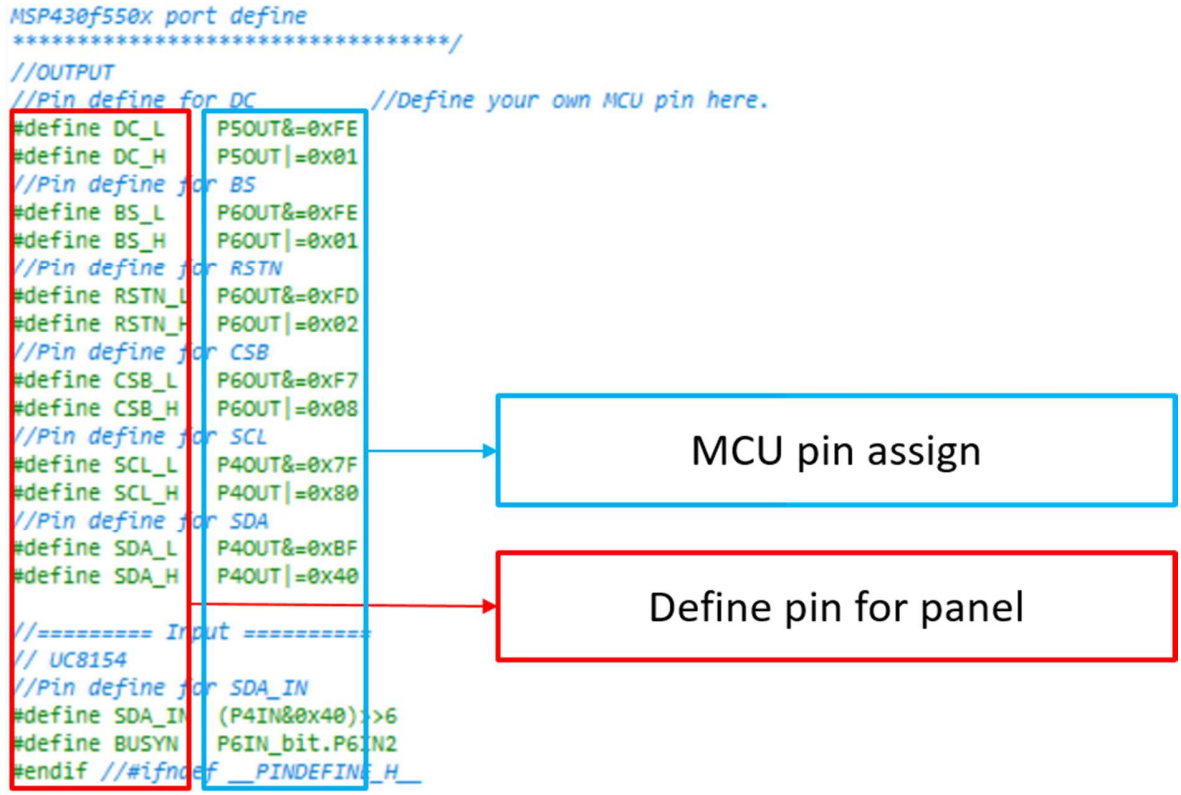


Figure 7 Program of ”pindefine.c” file.

5.1 EPD Software Reset

EPD software reset is include in the function ” **void EPD_Init(void)**”. The setting process is illustrated in figure 10. The last step “**check_busy”** is important for the programming sequence. The main idea is to check the device is powered up. Two functions are defined in table 5.

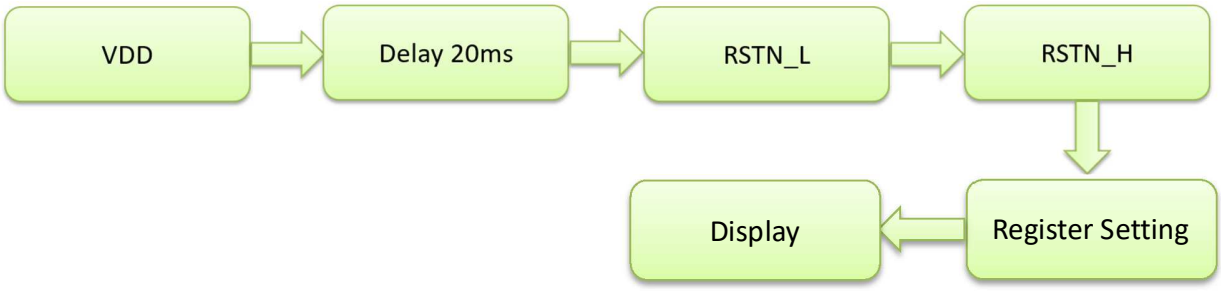


Figure 10 EPD Software Reset process.

5.2 Display

There are 2 image display functions, which are listed in table 6 with frame buffer settings (Ram BW and Ram Red). The display process is shown in figure 12. Frame buffer settings will be introduced next chapter.

Table 5 check_busy Function Table

Function	Description
void check_busy_high(void)	Check high peak finish.
void check_busy_low(void)	Check low peak finish.

Table 5 check_busy Function Table

Function	Description	RAM BW	Ram Red
void EPD_Display_White(void)	Display white image	0xFF	0xFF
void EPD_Display_Black(void)	Display black image	0x00	0x00
void EPD_Display_LG(void)	Display LG image	0x00	0xFF
void EPD_Display_DG(void)	Display DG image	0xFF	0x00

Table 6 Display Function Table

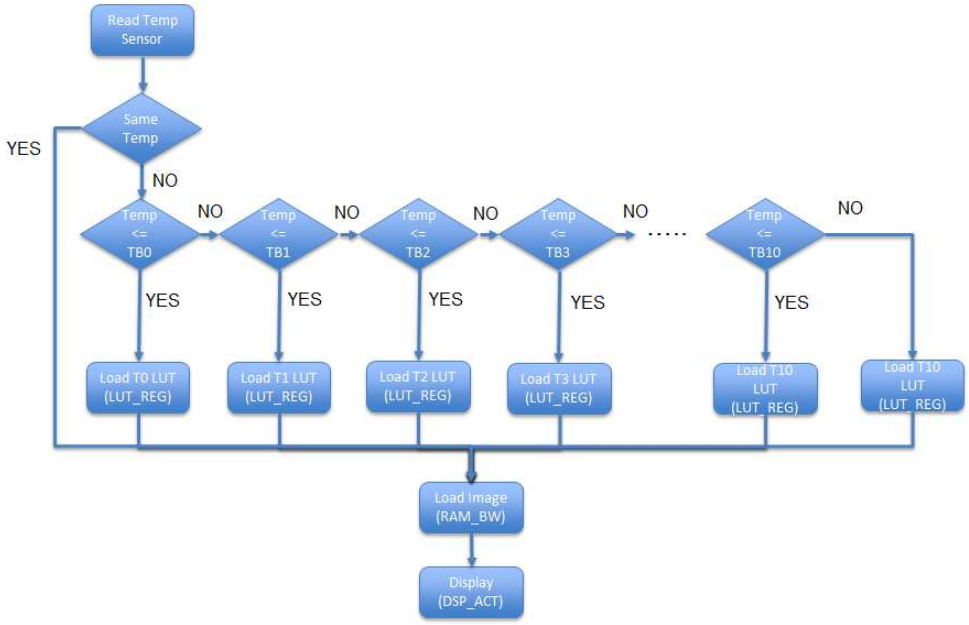


Figure 12 Display process

	Temperature Range
TB0	**0<Temperature <= 5**
TB1	**5<Temperature <=10**
TB2	**10<Temperature <=15**
TB3	**15<Temperature <=20**
TB4	**20<Temperature <=25**
TB5	**25<Temperature <=30**
TB6	**30<Temperature <=35**
TB7	**35<Temperature <=40**
TB8	**40<Temperature <=45**
TB9	**45<Temperature <=50**
TB10	**50<Temperature <=55**

Table 7 Temperature Range Table

6 Registers Table

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B[7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		

B[7] = 1,
VSH2 voltage setting from 2.4V to 8.8V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AFh	5.7
8Fh	2.5	B0h	5.8
90h	2.6	B1h	5.9
91h	2.7	B2h	6
92h	2.8	B3h	6.1
93h	2.9	B4h	6.2
94h	3	B5h	6.3
95h	3.1	B6h	6.4
96h	3.2	B7h	6.5
97h	3.3	B8h	6.6
98h	3.4	B9h	6.7
99h	3.5	BAh	6.8
9Ah	3.6	BBh	6.9
9Bh	3.7	BCh	7
9Ch	3.8	BDh	7.1
9Dh	3.9	BEh	7.2
9Eh	4	BFh	7.3
9Fh	4.1	C0h	7.4
A0h	4.2	C1h	7.5
A1h	4.3	C2h	7.6
A2h	4.4	C3h	7.7
A3h	4.5	C4h	7.8
A4h	4.6	C5h	7.9
A5h	4.7	C6h	8
A6h	4.8	C7h	8.1
A7h	4.9	C8h	8.2
A8h	5	C9h	8.3
A9h	5.1	CAh	8.4
AAh	5.2	CBh	8.5
ABh	5.3	CCh	8.6
ACh	5.4	CDh	8.7
ADh	5.5	CEh	8.8
AEh	5.6	Other	NA

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 9V to 17V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
23h	9	3Ch	14
24h	9.2	3Dh	14.2
25h	9.4	3Eh	14.4
26h	9.6	3Fh	14.6
27h	9.8	40h	14.8
28h	10	41h	15
29h	10.2	42h	15.2
2Ah	10.4	43h	15.4
2Bh	10.6	44h	15.6
2Ch	10.8	45h	15.8
2Dh	11	46h	16
2Eh	11.2	47h	16.2
2Fh	11.4	48h	16.4
30h	11.6	49h	16.6
31h	11.8	4Ah	16.8
32h	12	4Bh	17
33h	12.2	Other	NA
34h	12.4		
35h	12.6		
36h	12.8		
37h	13		
38h	13.2		
39h	13.4		
3Ah	13.6		
3Bh	13.8		

C[7] = 0,
VSL setting from -9V to -17V

C[7:0]	VSL
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA

Remark: VSH1> VSH2

0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate driving voltage A[4:0] = 00h [POR] VGH setting from 12V to 20V
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		

A[4:0]	VGH	A[4:0]	VGH
00h	20	10h	16.5
07h	12	11h	17
08h	12.5	12h	17.5
09h	13	13h	18
0Ah	13.5	14h	18.5
0Bh	14	15h	19
0Ch	14.5	16h	19.5
0Dh	15	17h	20
0Eh	15.5	Other	NA
0Fh	16		

0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] A[7:4] Red RAM option
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

0000	Normal
0100	Bypass RAM content as 0
1000	Inverse RAM content

A[3:0] BW RAM option

0000	Normal
0100	Bypass RAM content as 0
1000	Inverse RAM content

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR)
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Operating sequence	Parameter (in Hex)
Enable clock signal	80
Disable clock signal	01
Enable clock signal Enable Analog	C0
Disable Analog Disable clock signal	03
Enable clock signal Load LUT with DISPLAY Mode 1 Disable clock signal	91
Enable clock signal Load LUT with DISPLAY Mode 2 Disable clock signal	99
Enable clock signal Load temperature value from I2C Single Master Interface Load LUT with DISPLAY Mode 1 Disable clock signal	B1
Enable clock signal Load temperature value from I2C Single Master Interface Load LUT with DISPLAY Mode 2 Disable clock signal	B9
Enable clock signal Enable Analog Display with DISPLAY Mode 1 Disable Analog Disable OSC	C7
Enable clock signal Enable Analog Display with DISPLAY Mode 2 Disable Analog Disable OSC	CF
Enable clock signal Enable Analog Load temperature value from I2C Single Master Interface Load temperature value from I2C Single Master Interface DISPLAY with DISPLAY Mode 1 Disable Analog Disable OSC	F7
Enable clock signal Enable Analog Load temperature value from I2C Single Master Interface Load temperature value from I2C Single Master Interface DISPLAY with DISPLAY Mode 2 Disable Analog Disable OSC	FF

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	24	0	0	1	0	0	1	0	0	Write RAM (Black White) / RAM 0x24	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For White pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0

0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [105 bytes], which contains the content of VS [nX-LUT], TP #[nX], RP#[n].
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		:	:	:	:	:	:	:	:		
0	1		.	..	.	.	.	.	.	.		

Revision History

Version	Date	Page	Description	Author
0.1	2020/06/15		Initial	Hans Yeh