Product Specification

Model NO.: 7.5inch HD e-Paper

Product VER:A1

Version	Content	Date	Producer
A0	New release		
A1	Increasing the Brand of components		

CONTENTS

1. General Description

This is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 7.5" active area contains 528×880 pixels, and has 1-bit B/W full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC. SRAM.LUT, VCOM and border are supplied with each panel.

2. Features

- 528×880 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Low voltage detect for supply voltage
- High voltage ready detect for driving voltage
- Internal temperature sensor
- 10-byte OTP space for module identification
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/built-in temperature sensor

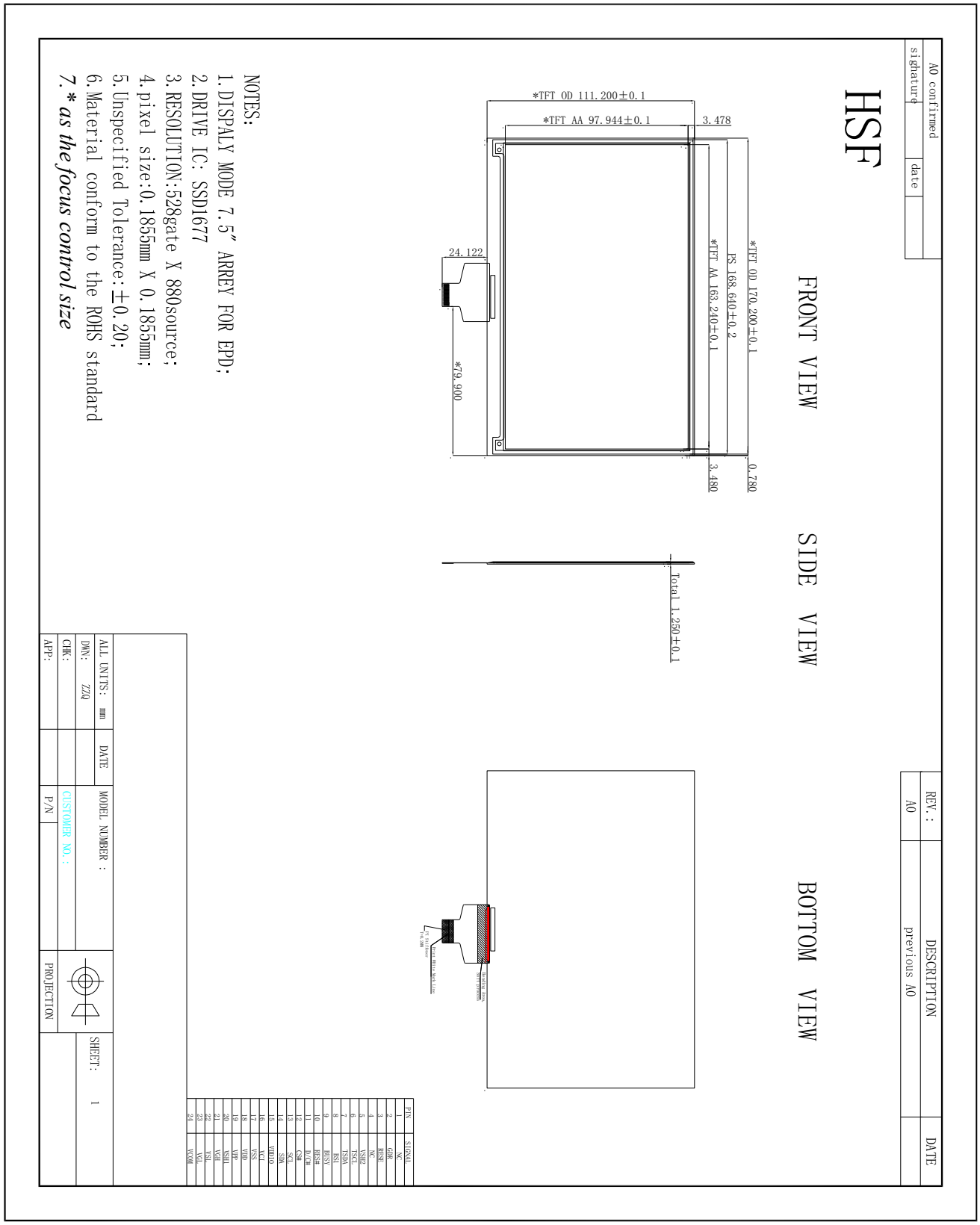
3. Application

Electronic Shelf Label System

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	7.5	Inch	
Display Resolution	528(H)×880(V)	Pixel	Dpi:137
Active Area	163.24(H)×97.94(V)	mm	
Pixel Pitch	0.1855×0.1855	mm	
Pixel Configuration	Rectangle		
Outline Dimension	170.2(H)×111.2 (V) ×1.25(D)	mm	
Weight	31±0.2	g	

5. Mechanical Drawing of EPD module



6. Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins e	Keep Open
5	VSH2	Positive Source driving voltage	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS1	Bus selection pin	Note 6-5
9	BUSY	Busy state output pin	Note 6-4
10	RES #	Reset	Note 6-3
11	D/C #	Data /Command control pin	Note 6-2
12	CS #	Chip Select input pin	Note 6-1
13	SCL	serial clock pin (SPI)	
14	SDA	serial data pin (SPI)	
15	VDDIO	Power for interface logic pins	
16	VCI	Power Supply pin for the chip	
17	VSS	Ground	
18	VDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VSH1	Positive Source driving voltage	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH	
22	VSL	Negative Source driving voltage	
23	VGL	Power Supply pin for Negative Gate driving voltage, VCOM and VSL	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CS# is pulled LOW.

Note 6-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 6-4: This pin (BUSY) is Busy state output pin. When Busy is High the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin High when the driver IC is working such as:

- Outputting display waveform; or

- Communicating with digital temperature sensor

Note 6-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected.

7. MCU Interface

7.1 MCU interface selection

Display can support 4-wire or 3-wire serial peripheral MCU interface, which is pin selectable by BS1 pin. The interface pin assignment for different MCU interfaces is shown in Table 7-1.

Note
(1) L is connected to VSS
(2) H is connected to VDDIO

Table 7-1: Interface pin assignment for different MCU interfaces

	Pin Name						
MCU Interface	**BS1**	**RES#**	**CS#**	**D/C#**	**SCL**	**SDI**	**SDO**
4-wire serial peripheral interface (SPI)	L	Required	Required	Required	SCL	SDI	SDO
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	Required	Required	L	SCL	SDI	SDO

7.2 MCU Serial Peripheral Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data input SDI, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 7-2 and the write procedure in 4-wire SPI is shown in Figure 7-1..

Table 7-2 : Control pins status of 4-wire SPI

Function	**SCL pin**	**SDI pin**	**D/C# pin**	**CS# pin**
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:
(1) L is connected to VSS and H is connected to VDDIO
(2) ↑ stands for rising edge of signal
(3) SDI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

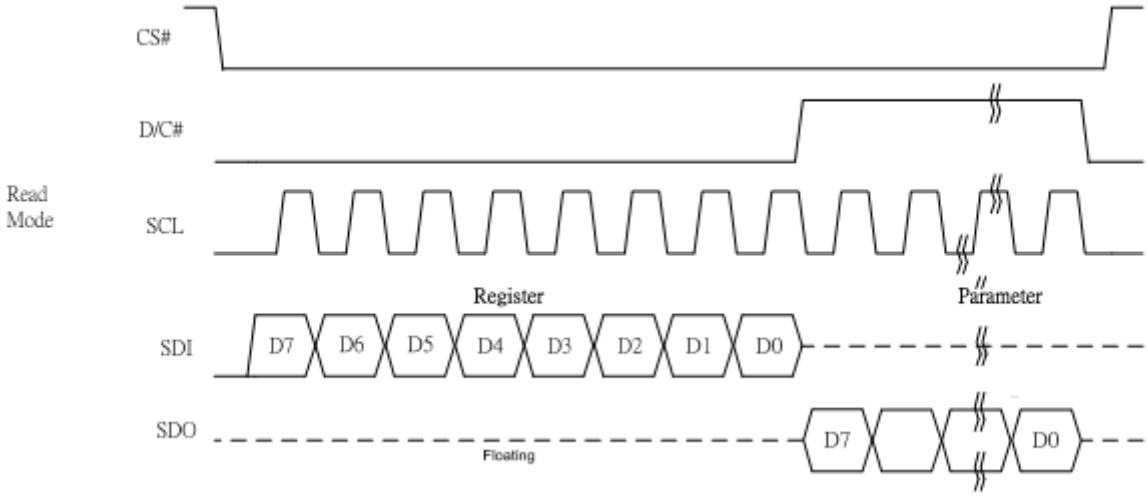


Figure 7-1: Read procedure in 4-wire SPI mode

In the read operation, after CS# is pulled low, the first byte sent is command byte, D/C# is pulled low. After command byte sent, the following byte(s) read are data byte(s), so D/C# bit is then pulled high. An 8-bit data will be shifted out on every clock falling edge. The serial data output SDO bit shifting sequence is D7, D6, to D0 bit. Figure 6-2 shows the read procedure in 4-wire SPI.

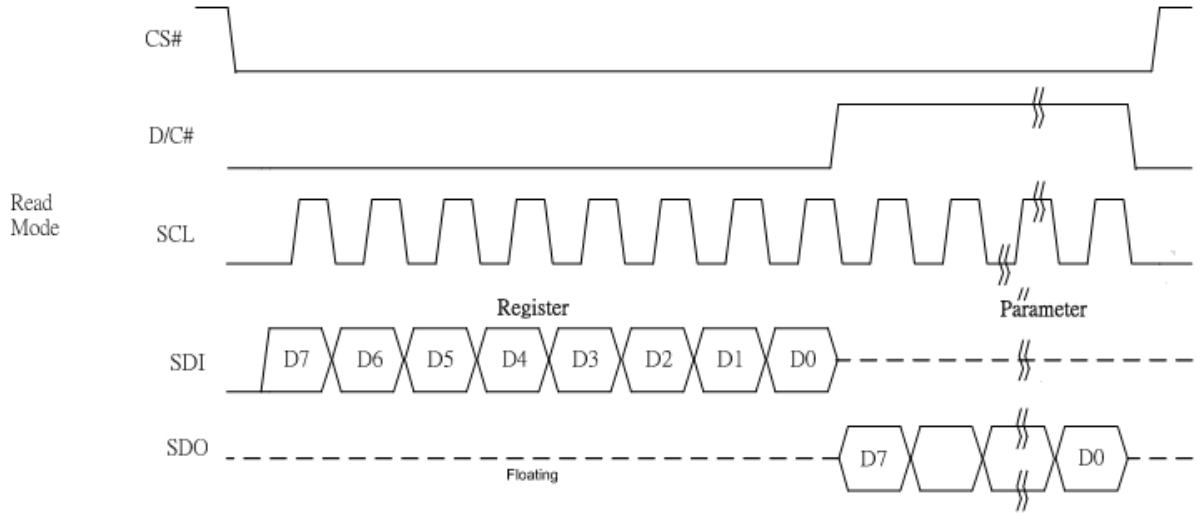


Figure 7-2: Read procedure in 4-wire SPI mode

7.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data input SDI, and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 7-3.

In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 7-3 shows the write procedure in 3-wire SPI

Table 7-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDI pin	D/C# pin	CS# pin

Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:
(1) L is connected to V_{SS} and H is connected to V_{DDIO}
(2) ↑ stands for rising edge of signal

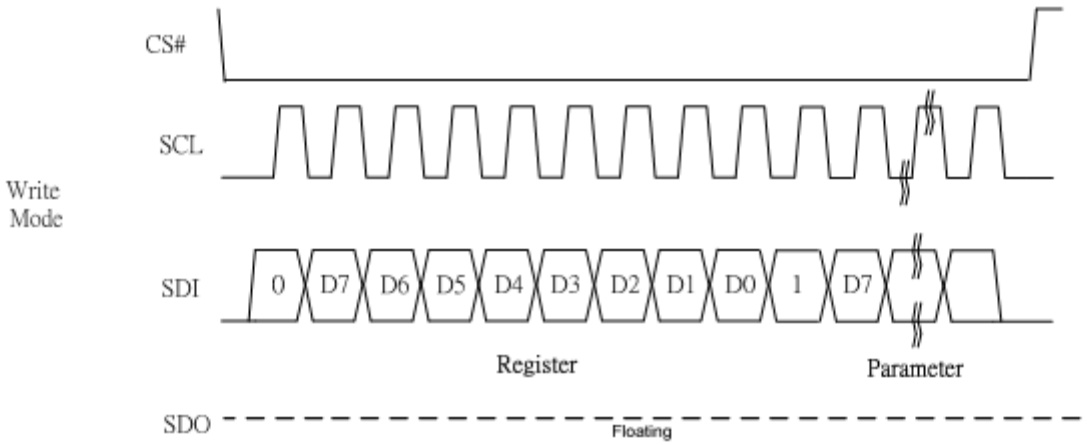


Figure 7-3: Write procedure in 3-wire SPI mode

In the read operation, serial data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command byte, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1. After D/C# bit sending from MCU, an 8-bit data will be shifted out on every clock falling edge. The serial data output SDO bit shifting sequence is D7, D6, to D0 bit. Figure 7-4 shows the read procedure in 3-wire SPI.

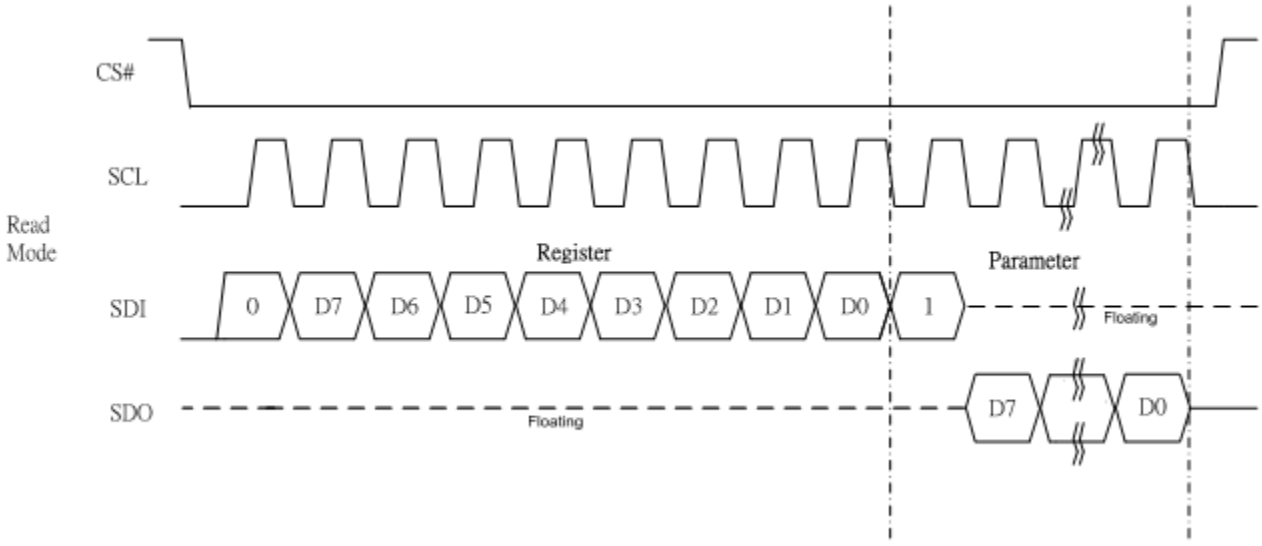


Figure 7-4: Read procedure in 3-wire SPI mode

8. COMMAND TABLE

<table>
<tr><td colspan="12">Command Table</td></tr>
<tr><td>R/W#</td><td>D/C#</td><td>Hex</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Command</td><td>Description</td></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="4">Driver Output control</td><td rowspan="4">Gate setting
A[9:0]= 2A7h [POR], 680 MUX
MUX Gate lines setting as (A[9:0] + 1).

B[2:0] = 000 [POR].
Gate scanning sequence and direction

B[2]: GD
Selects the 1st output Gate
GD=0 [POR],
G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, …
GD=1,
G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, …

B[1]: SM
Change scanning order of gate driver.
SM=0 [POR],
G0, G1, G2, G3…679 (left and right gate interlaced)
SM=1,
G0, G2, G4 …G678, G1, G3, …G679

B[0]: TB
TB = 0 [POR], scan from G0 to G679
TB = 1, scan from G679 to G0.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A9</td><td>A8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td></td><td>0</td><td>0</td><td>0</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Gate Driving voltage Control</td><td>Set Gate driving voltage
A[4:0] = 00h [POR]
VGH setting from 12V to 20V
<table><tr><th>A[4:0]</th><th>VGH</th><th>A[4:0]</th><th>VGH</th></tr><tr><td>00h</td><td>20</td><td>10h</td><td>16.5</td></tr><tr><td>07h</td><td>12</td><td>11h</td><td>17</td></tr><tr><td>08h</td><td>12.5</td><td>12h</td><td>17.5</td></tr><tr><td>09h</td><td>13</td><td>13h</td><td>18</td></tr><tr><td>0Ah</td><td>13.5</td><td>14h</td><td>18.5</td></tr><tr><td>0Bh</td><td>14</td><td>15h</td><td>19</td></tr><tr><td>0Ch</td><td>14.5</td><td>16h</td><td>19.5</td></tr><tr><td>0Dh</td><td>15</td><td>17h</td><td>20</td></tr><tr><td>0Eh</td><td>15.5</td><td>Other</td><td>NA</td></tr><tr><td>0Fh</td><td>16</td><td></td><td></td></tr></table></td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
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<tr><td>0</td><td>0</td><td>04</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="4">Source Driving voltage Control</td><td rowspan="4">Set Source driving voltage
A[7:0] = 41h [POR], VSH1 at 15V
B[7:0] = A8h [POR], VSH2 at 5V.
C[7:0] = 32h [POR], VSL at -15V

B[7] = 1,
VSH2 voltage setting from 2.4V to 8.8V
<table><tr><th>A/B[7:0]</th><th>VSH1/VSH2</th><th>A/B[7:0]</th><th>VSH1/VSH2</th></tr><tr><td>8Eh</td><td>2.4</td><td>AFh</td><td>5.7</td></tr><tr><td>8Fh</td><td>2.5</td><td>B0h</td><td>5.8</td></tr><tr><td>90h</td><td>2.6</td><td>B1h</td><td>5.9</td></tr><tr><td>91h</td><td>2.7</td><td>B2h</td><td>6</td></tr></table>
A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 9V to 17V
<table><tr><th>A/B[7:0]</th><th>VSH1/VSH2</th><th>A/B[7:0]</th><th>VSH1/VSH2</th></tr><tr><td>23h</td><td>9</td><td>3Ch</td><td>14</td></tr><tr><td>24h</td><td>9.2</td><td>3Dh</td><td>14.2</td></tr><tr><td>25h</td><td>9.4</td><td>3Eh</td><td>14.4</td></tr><tr><td>26h</td><td>9.6</td><td>3Fh</td><td>14.6</td></tr></table>
C[7] = 0,
VSL setting from -9V to -17V
<table><tr><th>C[7:0]</th><th>VSL</th></tr><tr><td>1Ah</td><td>-9</td></tr><tr><td>1Ch</td><td>-9.5</td></tr><tr><td>1Eh</td><td>-10</td></tr><tr><td>20h</td><td>-10.5</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A2</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>C7</td><td>C6</td><td>C5</td><td>C4</td><td>C3</td><td>C2</td><td>C1</td><td>C0</td></tr>
</table>

92h	2.8	B3h	6.1
93h	2.9	B4h	6.2
94h	3	B5h	6.3
95h	3.1	B6h	6.4
96h	3.2	B7h	6.5
97h	3.3	B8h	6.6
98h	3.4	B9h	6.7
99h	3.5	BAh	6.8
9Ah	3.6	BBh	6.9
9Bh	3.7	BCh	7
9Ch	3.8	BDh	7.1
9Dh	3.9	BEh	7.2
9Eh	4	BFh	7.3
9Fh	4.1	C0h	7.4
A0h	4.2	C1h	7.5
A1h	4.3	C2h	7.6
A2h	4.4	C3h	7.7
A3h	4.5	C4h	7.8
A4h	4.6	C5h	7.9
A5h	4.7	C6h	8
A6h	4.8	C7h	8.1
A7h	4.9	C8h	8.2
A8h	5	C9h	8.3
A9h	5.1	CAh	8.4
AAh	5.2	CBh	8.5
ABh	5.3	CCh	8.6
ACh	5.4	CDh	8.7
ADh	5.5	CEh	8.8
AEh	5.6	Other	NA

27h	9.8	40h	14.8
28h	10	41h	15
29h	10.2	42h	15.2
2Ah	10.4	43h	15.4
2Bh	10.6	44h	15.6
2Ch	10.8	45h	15.8
2Dh	11	46h	16
2Eh	11.2	47h	16.2
2Fh	11.4	48h	16.4
30h	11.6	49h	16.6
31h	11.8	4Ah	16.8
32h	12	4Bh	17
33h	12.2	Other	NA
34h	12.4		
35h	12.6		
36h	12.8		
37h	13		
38h	13.2		
39h	13.4		
3Ah	13.6		
3Bh	13.8		

22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA

Remark:
VSH1> VSH2

0	0	0F	0	0	0	0	1	1	1	1	Gate scan start position	Set the scanning start position of the gate driver. The valid range is from 0 to 679. A[9:0] = 000h [POR] When TB=0: SCN [9:0] = A[9:0] When TB=1: SCN [9:0] = 679 - A[9:0]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	A9	A8		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control: A[1:0] : Description 00 Normal Mode [POR] 01 Enter Deep Sleep Mode 1 11 Enter Deep Sleep Mode 2 After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver
0	0		0	0	0	0	0	A2	A1	A0		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR]
0	1		0	0	0	0	0	A2	A1	A0		

												A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection A[6:0] = 00h [POR] The command required CLKEN=1 and ANALOGEN=1. Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	0	15	0	0	0	1	0	1	0	1	VCI Detection	VCI Detection A[2:0] = 100 [POR] , Detect level at 2.3V A[2:0] : VCI level Detect A[2:0] / VCI level 011 / 2.2V 100 / 2.3V 101 / 2.4V 110 / 2.5V 111 / 2.6V Other / NA The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. After this command initiated, VCI detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	1		0	0	0	0	0	A2	A1	A0		
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperatrure sensor A[7:0] = 80h Internal temperature sensor
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	1A	0	0	0	0	0	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[11:0] = 7FFh[POR]
0	1		A11	A10	A9	A8	A7	A6	A5	A4		
0	1		A3	A2	A1	A0	0	0	0	0		
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register.
1	1		A11	A10	A9	A8	A7	A6	A5	A4		

1	1		A3	A2	A1	A0	0	0	0	0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to External temperature sensor)	Write Command to External temperature sensor. A[7:0] = 00h [POR], B[7:0] = 00h [POR], C[7:0] = 00h [POR], A[7:6]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		

A[7:6]	Select no of byte to be sent
00	Address + pointer
01	Address + pointer + 1st arameter
10	Address + pointer + 1st parameter +2nd pointer
11	Address

A[5:0] – Pointer Setting
B[7:0] – 1st parameter
C[7:0] – 2nd parameter
The command required CLKEN=1.
Refer to Register 0x22 for detail.
After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.

0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.

0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] A[7:4] Red RAM option
0	1		A7	A6	A5	A4	A3	A2	A1	A0		

0000	Normal
0100	Bypass RAM content as 0
1000	Inverse RAM content

A[3:0] BW RAM option

0000	Normal
0100	Bypass RAM content as 0
1000	Inverse RAM content

0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR)
0	1		A7	A6	A5	A4	A3	A2	A1	A0		

	Parameter (in Hex)
Enable Clock Signal, Then Enable ANALOG Then DISPLAY with DISPLAY Mode 1 Then Disable ANALOG Then Disable OSC	C7
Enable Clock Signal, Then Enable ANALOG Then DISPLAY with DISPLAY Mode 2 Then Disable ANALOG Then Disable OSC	CF
Enable Clock Signal, Then Load LUT with DISPLAY Mode 1	90
Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 1	B0
Enable Clock Signal, Then Load LUT with	98

DISPLAY Mode 2	
Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 2	B8
Enable Clock Signal, Then Load LUT with DISPLAY Mode 1 To Disable Clock Signal	91
Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 1 To Disable Clock Signal	B1
Enable Clock Signal, Then Load LUT with DISPLAY Mode 2 To Disable Clock Signal	99
Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 2 To Disable Clock Signal	B9
Enable ANALOG Then DISPLAY with DISPLAY Mode 1 Then Disable ANALOG Then Disable OSC	47
Enable ANALOG Then DISPLAY with DISPLAY Mode 2 Then Disable ANALOG Then Disable OSC	4F
To Enable Clock Signal (CLKEN=1)	80
To Enable Clock Signal, then Enable ANALOG (CLKEN=1, ANALOGEN=1)	C0
Enable ANALOG Then DISPLAY with DISPLAY Mode 1	44
Enable ANALOG Then DISPLAY with DISPLAY Mode 2	4C
To DISPLAY with DISPLAY Mode 1	04
To DISPLAY with DISPLAY Mode 2	0C
To Disable ANALOG, then Disable Clock Signal (CLKEN=0, ANALOGEN=0)	03
o Disable Clock Signal (CLKEN=0)	01

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	24	0	0	1	0	0	1	0	0	Write RAM (BW)	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM(BW) = 1

												For Black pixel: Content of Write RAM(BW) = 0
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED)	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM [According to parameter of Register 41h to select reading RAM(BW) / RAM(RED)], until another command is written. Address pointers will advance accordingly. The 1st byte of data read is dummy data.
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[6]=1, Normal Mode A[6]=0, Reserve A[3:0] = 09h, duration = 10s. VCOM sense duration = Setting + 1 Seconds
0	1		0	A6	0	0	A3	A2	A1	A0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2B	0	0	1	0	1	0	1	1	Write Register for VCOM Control	This command is used to reduce glitch when ACVCOM toggle. Two data bytes D04h and D63h should be set for this command.
0	1		0	0	0	0	0	1	0	0		
0	1		0	1	1	0	0	0	1	1		
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		

A[7:0]	VCOM	A[7:0]	VCOM
08h	-0.2	58h	-2.2
0Ch	-0.3	5Ch	-2.3
10h	-0.4	60h	-2.4
14h	-0.5	64h	-2.5
18h	-0.6	68h	-2.6
1Ch	-0.7	6Ch	-2.7
20h	-0.8	70h	-2.8
24h	-0.9	74h	-2.9
28h	-1	78h	-3
2Ch	-1.1	7Ch	-3.1
30h	-1.2	80h	-3.2
34h	-1.3	84	-3.3
38h	-1.4	88	-3.4
3Ch	-1.5	8C	-3.5

												40h	-1.6	90	-3.6
												44h	-1.7	94	-3.7
												48h	-1.8	98	-3.8
												4Ch	-1.9	9C	-3.9
												50h	-2	A0	-4
												54h	-2.1		
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read forDisplay Option	Read Register for Display Option: A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte G) [5 bytes] H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte H to Byte K) [4 bytes]			
1	1		A7	A6	A5	A4	A3	A2	A1	A0					
1	1		B7	B6	B5	B4	B3	B2	B1	B0					
1	1		C7	C6	C5	C4	C3	C2	C1	C0					
1	1		D7	D6	D5	D4	D3	D2	D1	D0					
1	1		E7	E6	E5	E4	E3	E2	E1	E0					
1	1		F7	F6	F5	F4	F3	F2	F1	F0					
1	1		G7	G6	G5	G4	G3	G2	G1	G0					
1	1		H7	H6	H5	H4	H3	H2	H1	H0					
1	1		I7	I6	I5	I4	I3	I2	I1	I0					
1	1		J7	J6	J5	J4	J3	J2	J1	J0					
1	1		K7	K6	K5	K4	K3	K2	K1	K0					

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command for OTP content validation. BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status Read	CRC Status Read A[15:0] is the CRC readout Value
1	1		A15	A14	A13	A12	A11	A10	A9	A8		
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	37	0	0	1	1	0	1	1	1	Write Register for Display Option	Write Register for Display Option B[7:0] Display Mode for WS[7:0] C[7:0] Display Mode for WS[15:8] D[7:0] Display Mode for WS[23:16] E[7:0] Display Mode for WS[31:24] F[3:0] Display Mode for WS[35:32] 0: Display Mode 1 1: Display Mode2 F[6]: PingPong for Display Mode 2 F[7]: PingPong for Display Mode 1 1: Ping-Pong 0: Default G[7:0]~J[7:0] module ID /waveform version. Remarks: A[7:0]~J[7:0] can be stored in OTP
0	1		0	0	0	0	0	0	0	0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		
0	1		D7	D6	D5	D4	D3	D2	D1	D0		
0	1		E7	E6	E5	E4	E3	E2	E1	E0		
0	1		F7	F6	F5	F4	F3	F2	F1	F0		
0	1		G7	G6	G5	G4	G3	G2	G1	G0		
0	1		H7	H6	H5	H4	H3	H2	H1	H0		
0	1		I7	I6	I5	I4	I3	I2	I1	I0		
0	1		J7	J6	J5	J4	J3	J2	J1	J0		
0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]]~J[7:0]: UserID [10 bytes] Remarks: A[7:0]~J[7:0] can be stored in OTP
0	1	A7	A6	A5	A4	A3	A2	A1	A0	A7		
0	1	B7	B6	B5	B4	B3	B2	B1	B0	B7		
0	1	C7	C6	C5	C4	C3	C2	C1	C0	C7		
0	1	D7	D6	D5	D4	D3	D2	D1	D0	D7		
0	1	E7	E6	E5	E4	E3	E2	E1	E0	E7		
0	1	F7	F6	F5	F4	F3	F2	F1	F0	F7		

0	1	G7	G6	G5	G4	G3	G2	G1	G0	G7		
0	1	H7	H6	H5	H4	H3	H2	H1	H0	H7		
0	1	I7	I6	I5	I4	I3	I2	I1	I0	I7		
0	1	J7	J6	J5	J4	J3	J2	J1	J0	J7		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	39	0	0	1	1	1	0	0	1	OTP program mode	OTP program mode A[1:0] = 00: Normal Mode [POR] A[1:0] = 11: Internal generated OTP programming voltage Remark: User is required to EXACTLY follow the reference code sequences
0	1		0	0	0	0	0	0	A1	A0		
0	0	3A	0	0	1	1	1	0	1	0	Reserved	Reserved
0	0	3B	0	0	1	1	1	0	1	1	Reserved	Reserved
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HIZ. A [7:6] :Select VBD option
0	1		A7	A6	A5	A4	A3	A2	A1	A0		

A[7:6]	Select VBD as
00	GS Transition, Defined in A[1:0]
01	Fix Level, Defined in A[5:4]
10	VCOM
11[POR]	HiZ

A [5:4] Fix Level Setting for VBD

A[5:4]	VBD level
00[POR]	VSS
01	VSH1
10	VSL
11	VSH2

A [1:0] GS Transition setting for VBD

A[1:0]	VBD Transition
00[POR]	LUT0
01	LUT1
10	LUT2
11	LUT3

0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0: Read RAM corresponding to 24h 1: Read RAM corresponding to 26h
0	1		0	0	0	0	0	0	0	A0		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit for RAM A[9:0]: XSA[9:0], XStart, POR = 000h B[5:0]: XEA[9:0], XEnd, POR = 3BFh
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		-	-	-	-	-	-	A9	A8		
0	1		0	0	B5	B4	B3	B2	B1	B0		
0	1		-	-	-	-	-	-	B9	B8		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	45	0	1	0	0	0	1	0	1	Set RAM Y-address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit for RAM A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 2A7h
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		-	-	-	-	-	-	A9	A8		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		-	-	-	-	-	-	B9	B8		
0	0	46	0	1	0	0	0	1	1	0	Auto Write RED RAM for Regular Pattern	Auto Write RED RAM for Regular Pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate
0	1		A7	A6	A5	A4	A3	A2	A1	A0		

<table>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>
<table>
<tr><td>A[6:4]</td><td>Height</td><td>A[6:4]</td><td>Height</td></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>256</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>512</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>960</td></tr>
</table>
A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source
<table>
<tr><td>A[2:0]</td><td>Width</td><td>A[2:0]</td><td>Width</td></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>256</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>512</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>680</td></tr>
</table>
BUSY pad will output high during operation.
</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>47</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Auto Write B/W RAM for Regular Pattern</td><td>Auto Write B/W RAM for Regular Pattern
A[7:0] = 00h [POR]
Auto Write B/W RAM for Regular Pattern
A[7:0] = 00h [POR]
<table>
<tr><td>A[6:4]</td><td>Height</td><td>A[6:4]</td><td>Height</td></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>256</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>512</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>960</td></tr>
</table>
A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source
<table>
<tr><td>A[2:0]</td><td>Width</td><td>A[2:0]</td><td>Width</td></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>256</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>512</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>680</td></tr>
</table>
uring operation, BUSY pad will output high.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
</table>

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[9:0]: 000h [POR].
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	A9	A8		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[9:0]: 000h [POR].
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	A9	A8		
0	0	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However, it can be used to terminate Frame Memory Write or Read Commands.

9.Reference Circuit

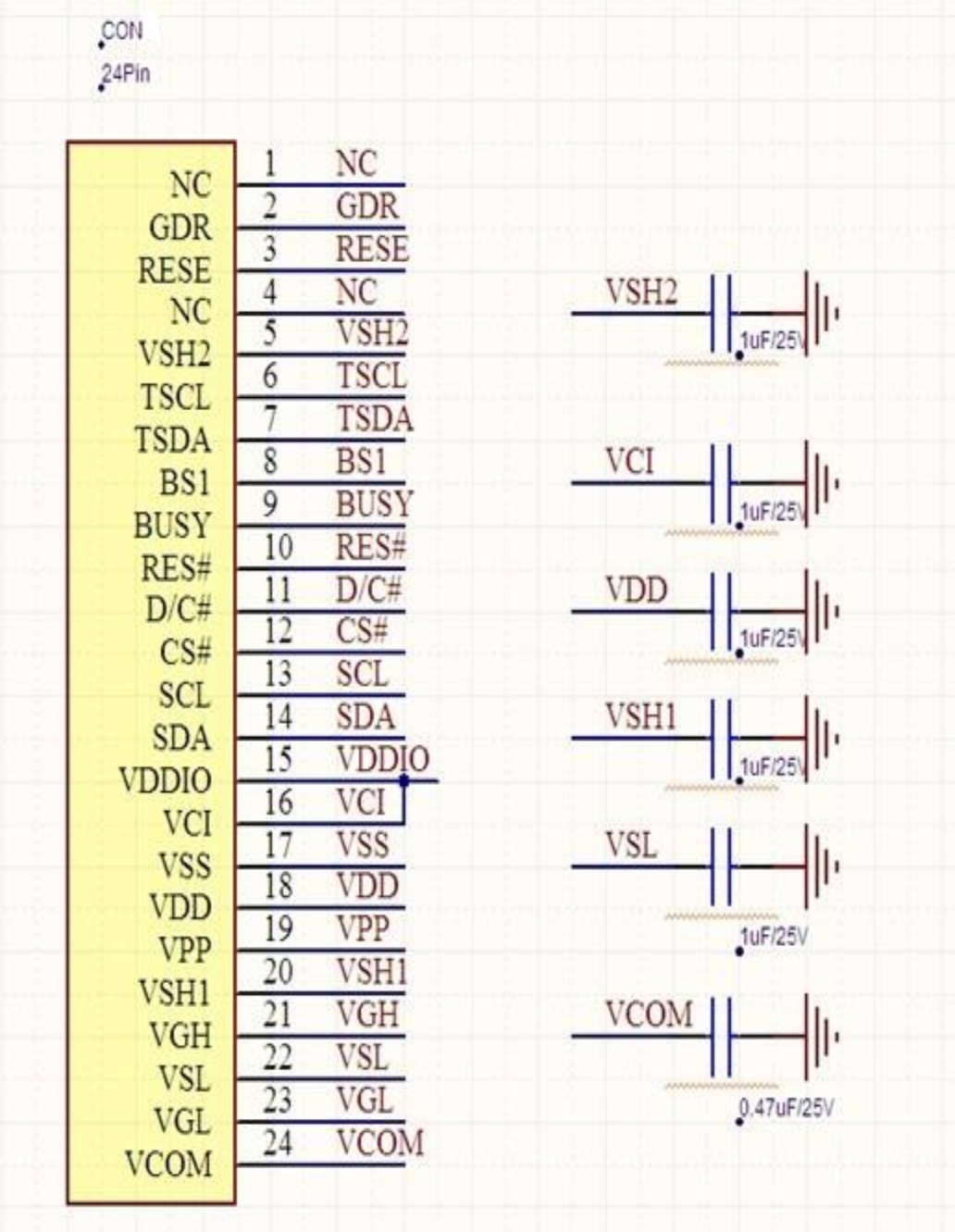


Figure. 9-1

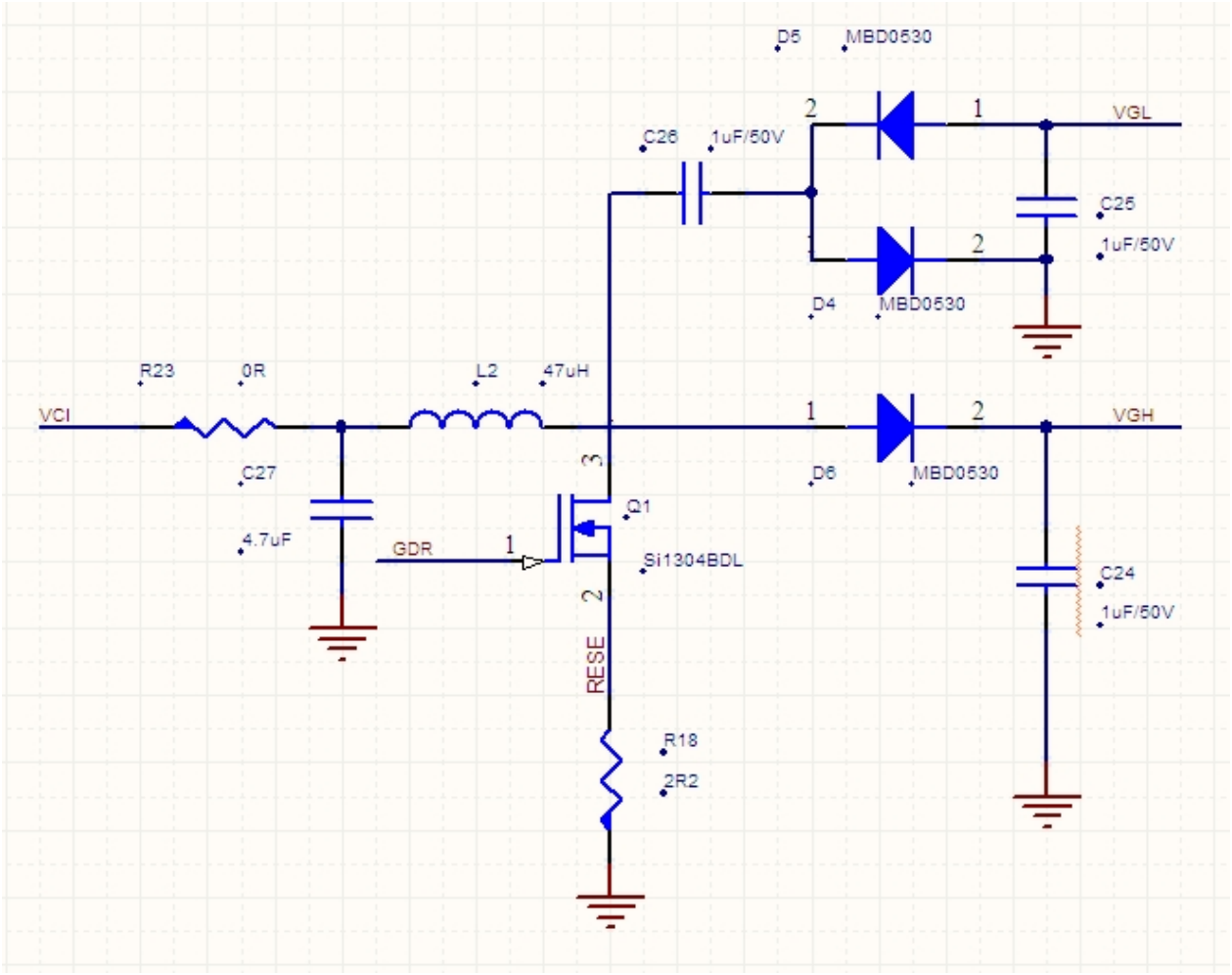


Figure. 9-2

Part Name	Value/Type	Reference Part
D4-D6	Diode	OnSemi:MBR0530
L2	47uH	Sumida:CDRH2D18/LDNP-470NC
Q1	NMOS	Vishay:Si1304BDL
R18	2.2Ohm	Vishay:CRCW08052R20FKEA
CON 24Pin	0.5mm ZIF socket	Hirose:FH34S-24S-0.5SH(50)

10. ABSOLUTE MAXIMUM RATING

Table 11-1: Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CI}	Logic supply voltage	-0.5 to +6.0	V
T_{OPR}	Operation temperature range	0 to 50	°C
T_{STG}	Storage temperature range	-25 to 60	°C

11. DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.3V, T_{OPR}=25℃.

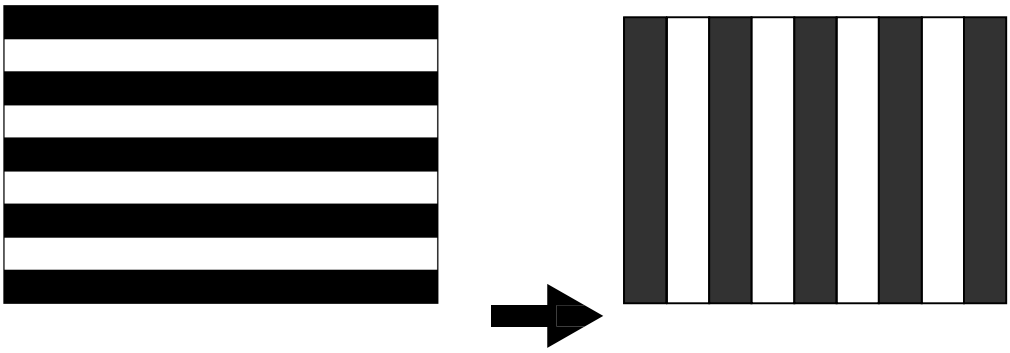
Table 12-1: DC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCI	VCI operation voltage	-	VCI	2.2	3.3	3.7	V
VIH	High level input voltage	-	SDA, SCL, CS#, D/C#, RES#, BS1	0.8VDDIO	-	-	V
VIL	Low level input voltage	-		-	-	0.2VDDIO	V
VOH	High level output voltage	IOH = -100uA	BUSY,	0.9VDDIO	-	-	V
VOL	Low level output voltage	IOL = 100uA		-	-	0.1VDDIO	V
Iupdate	Module operating current	-	-	-		18	mA
Isleep	Deep sleep mode	VCI=3.3V	-	-		2	uA

- The Typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 11-1)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by XingTai.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 11-1

The Typical power consumption



12. Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VCI=2.2V to 3.7V, T_{OPR}=25℃

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CSB has to be low before the first rising edge of SCLK	20			ns
tCSHLD	Time CSB has to remain low after the last falling edge of SCLK	20			ns
tCSHIGH	Time CSB has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CSB has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CSB has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CSB has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

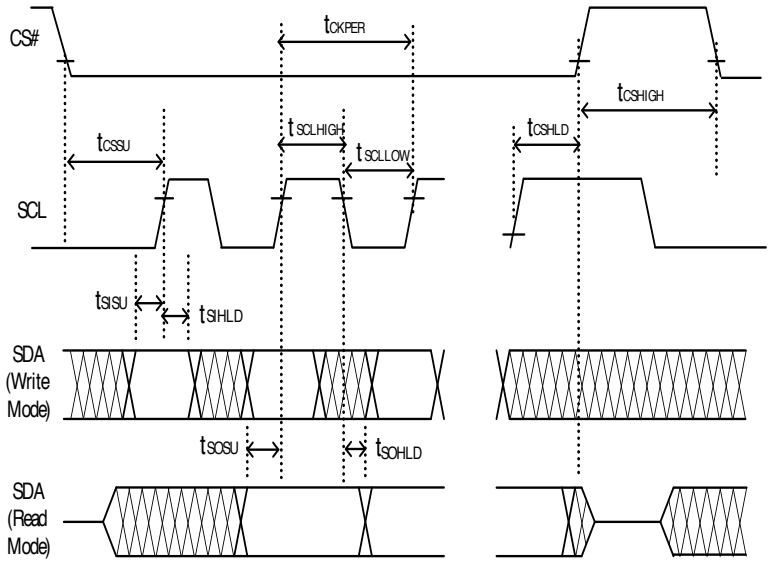


Figure 13-1: Serial peripheral interface characteristics

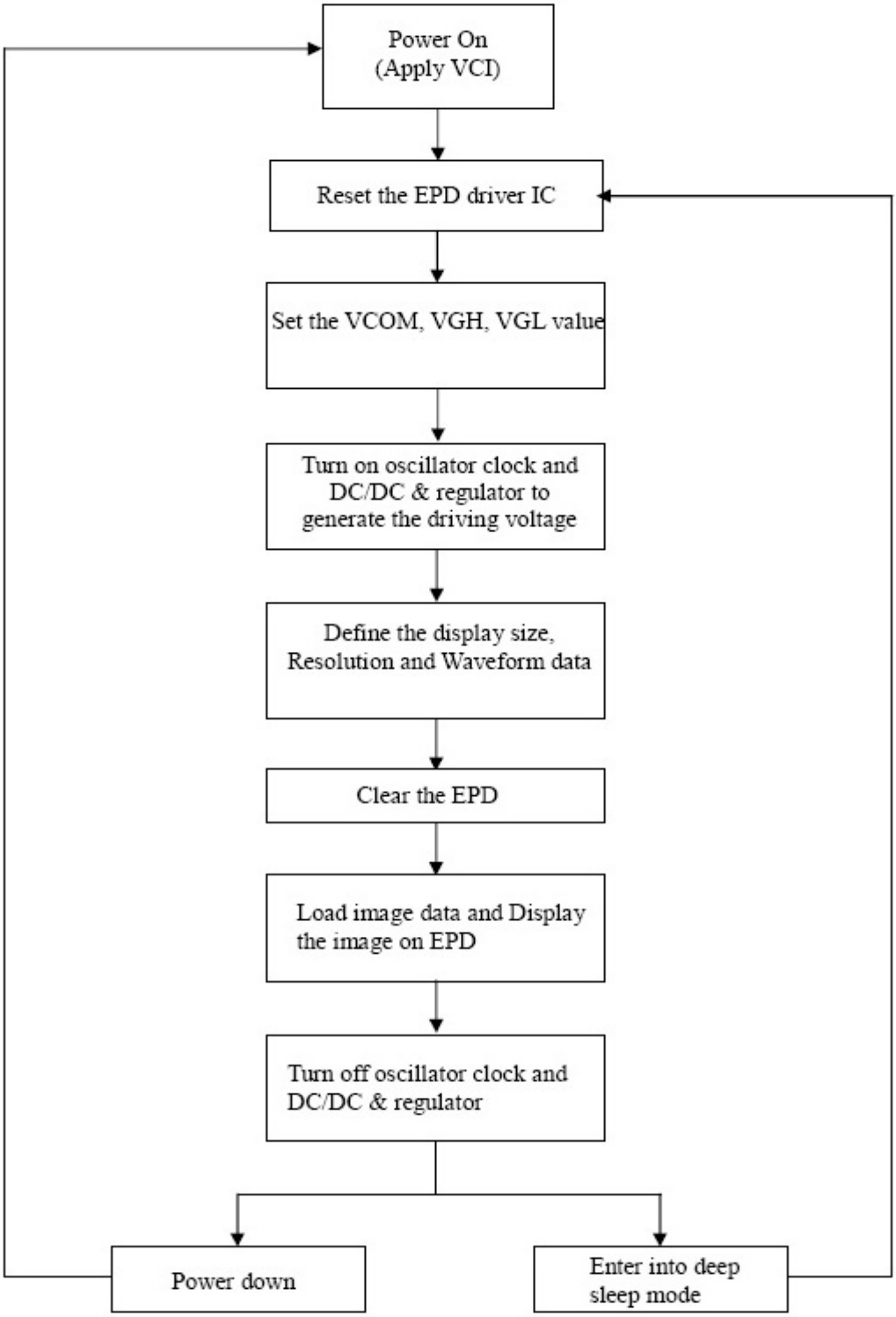
13. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25□		75	mAs	-
Deep sleep mode	-	25□		2	uA	-

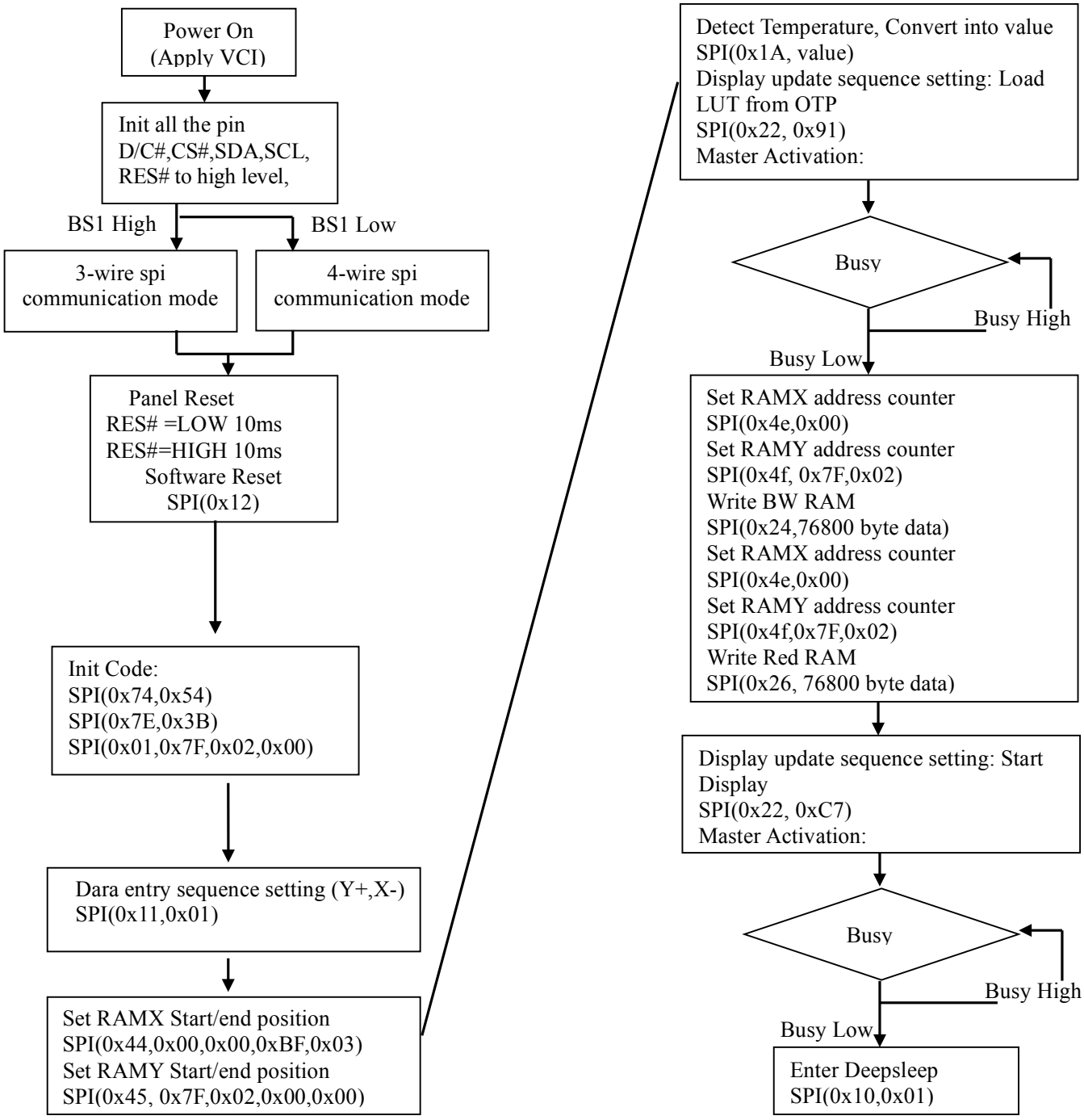
Mas=update average current × update time

14. Typical Operating Sequence

14.1 Normal Operation Flow



14.2 Reference Program Code



15. Optical characteristics

15.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25□

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 15-1
Gn	2Grey Level	-	-	DS+(WS-DS)×n(m-1)	-	L*	-
CR	Contrast Ratio	indoor	-	10	-	-	-
Panel's life	-	0℃～50℃		5years or 1000000 times	-	-	Note 15-2

WS: White state, DS : Dark state

m: 2

Note 15-1: Luminance meter : Eye - One Pro Spectrophotometer

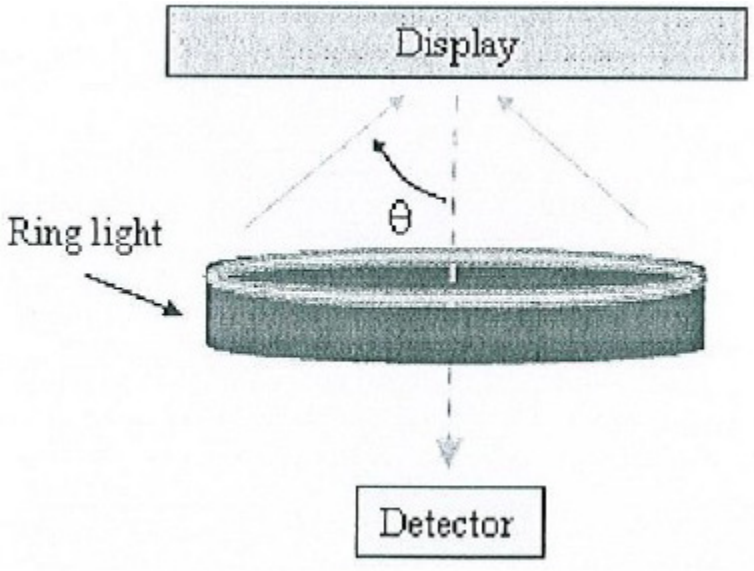
Note 15-2: We guarantee display quality from 0□～30□ generally,If operation ambient temperature from 0□～50□, will Offer special waveform by Xingtai.

15.2Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)() :

R1: white reflectance Rd: dark reflectance

CR = R1/Rd

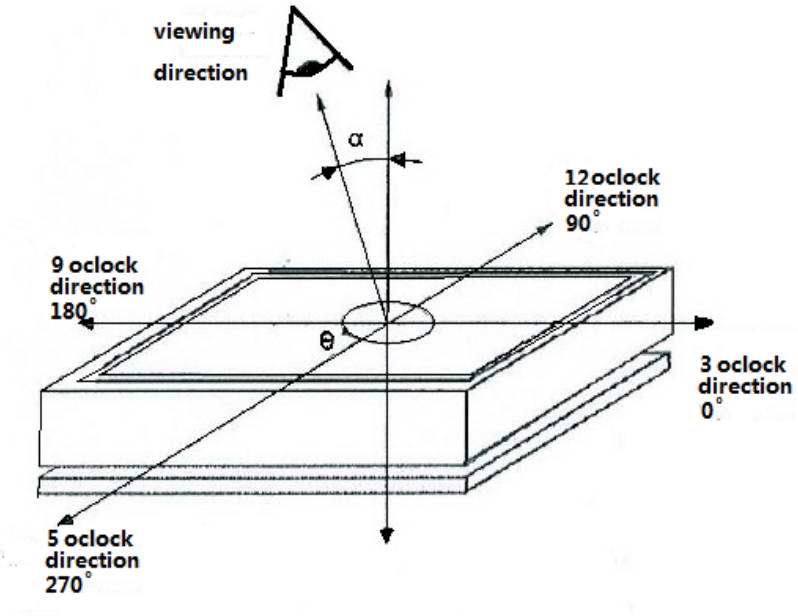


15.3 Reflection Ratio

The reflection ratio is expressed as :

R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1) . $L_{\text{white board}}$ is the luminance of a standard white board . Both are measured with equivalent illumination source . The viewing angle shall be no more than 2 degrees .



16. HANDLING,SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.

(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Product specification	The data sheet contains final product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification
ROHS

REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

7. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T=40□, RH=35%RH, For 240Hr	IEC 60 068-2-2Bb	
2	Low-Temperature Operation	T = 0□ for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T=60□ RH=35%RH For 240Hr Test in white pattern	IEC 60 068-2-2Bb	
4	Low-Temperature Storage	T = -25□ for 240 hrs Test in white pattern	IEC 60 068-2-2Ab	
5	High Temperature, High-Humidity Operation	T=40□, RH=80%RH, For 168Hr	IEC 60 068-2-3CA	
6	High Temperature, High-Humidity Storage	T=50□, RH=80%RH, For 240Hr Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	-25□(30min)~60□(30min), 50 Cycle Test in white pattern	IEC 60 068-2-14NB	
8	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
9	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges,6face One drop for each.	Full packed for shipment	
10	UV exposure Resistance	765 W/㎡for 168hrs,40□	IEC 60068-2-5 Sa	
11	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF	IEC61000-4-2	

Actual EMC level to be measured on customer application.

Note1: The protective film must be removed before temperature test.

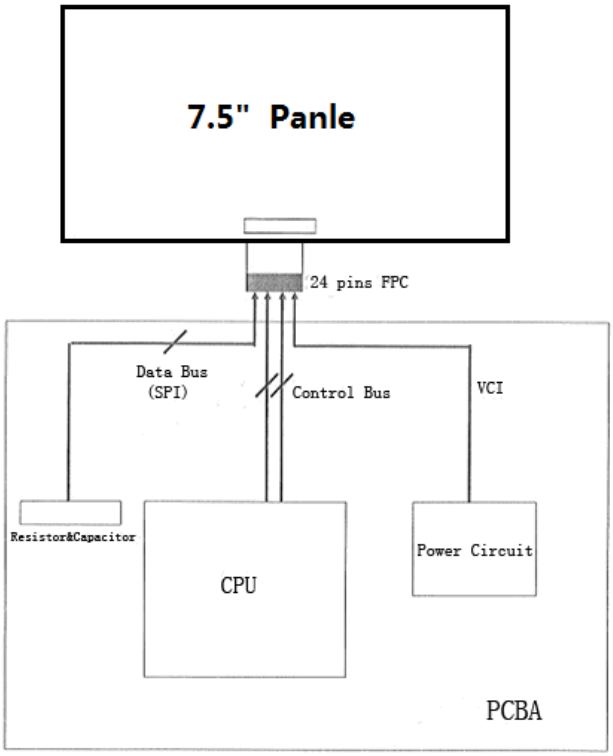
Note2 : Stay white pattern for storage and non-operation test.

Note3 : Operation is black/white/red pattern , hold time is 150S.

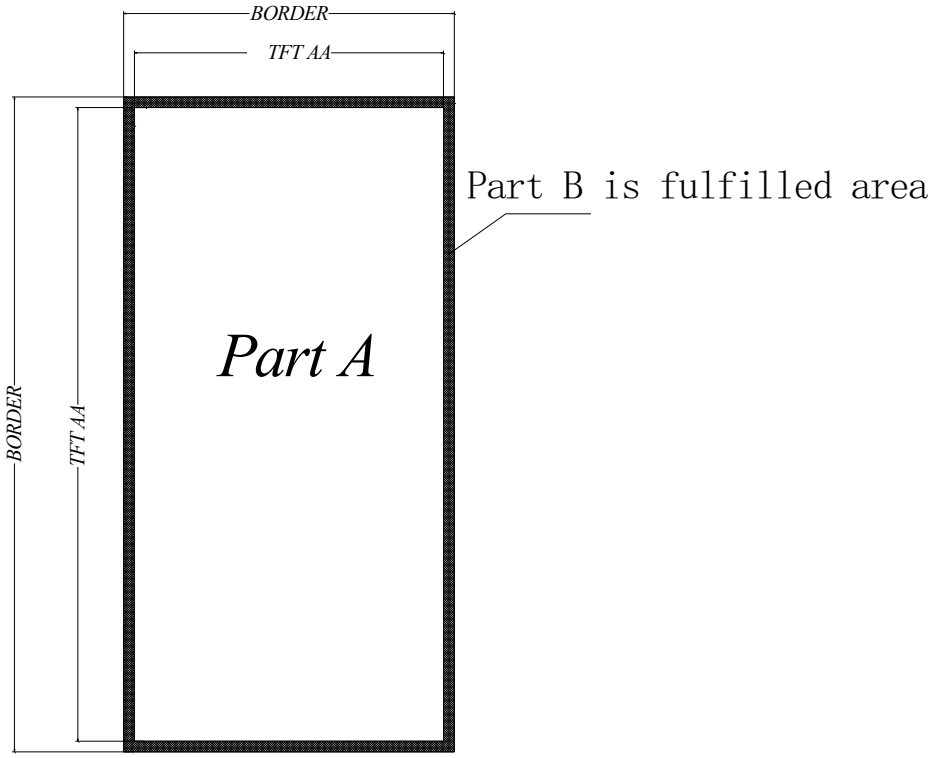
Note4 : The function,appearence,opticals should meet the requirements of the test before and after the test.

Note5 : Keep testing after 2 hours placing at 20℃-25℃.

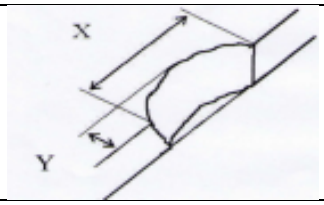
18. Block Diagram

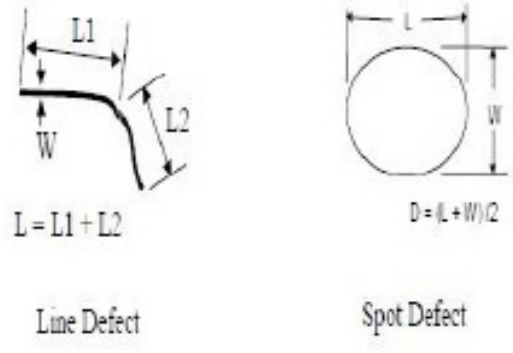


19. PartA/PartB specification



20. Point and line standard

Shipment Inspection Standard						
Equipment：Electrical test fixture, Point gauge						
Outline dimension	170.2(H) × 111.2(V) ×1.25(D)	Unit：㎜	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19℃～25℃	55%±5%RH	800～1300Lux	300 ㎜	35Sec	
Defet type	Inspection method	Standard		Part-A		Part-B
Spot	Electric Display	D≤0.4 ㎜		Ignore		Ignore
		0.4 ㎜＜D≤0.6 ㎜		N≤4		Ignore
		0.6 ㎜＜D≤0.8 ㎜		N≤1		Ignore
		D＞0.8 ㎜		Not Allow		Ignore
Display unwork	Electric Display	Not Allow		Not Allow		Ignore
Display error	Electric Display	Not Allow		Not Allow		Ignore
Scratch or line defect(include dirt)	Visual/Film card	L≤2 ㎜，W≤0.2 ㎜		Ignore		Ignore
		2.0mm＜L≤9.0mm，0.2＜W≤0.6mm,		N≤2		Ignore
		L＞9.0 ㎜，W＞0.6 ㎜		Not Allow		Ignore
PS Bubble	Visual/Film card	D≤0.4mm		Ignore		Ignore
		0.4mm≤D≤0.6mm		N≤4		Ignore
		D＞0.6 mm		Not Allow		Ignore
Side Fragment	Visual/Film card	X≤8mm，Y≤1mm, Do not affect the electrode circuit, Ignore				
						
Remark	1.Cannot be defect & failure cause by appearance defect；					
	2.Cannot be larger size cause by appearance defect；					
	L=long W=wide D=point size N=Defects NO					



Line Defect Spot Defect

L=long W=wide D=point size