SPI display expansion board for STM32 Nucleo

Introduction

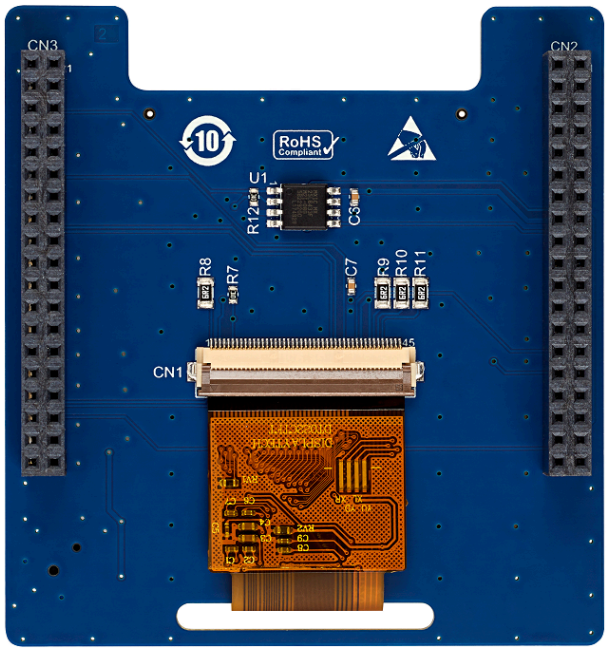
The X-NUCLEO-GFX01M1 expansion board adds graphic user interface (GUI) capability to STM32 Nucleo boards.

It features a 2.2” SPI QVGA TFT display as well as a 64-Mbit SPI NOR Flash memory for storing graphic images, texts and texture. The expansion board also offers a joystick for GUI navigation.

X-NUCLEO-GFX01M1 uses the ST morpho connector. It is compatible with the NUCLEO-F030R8, NUCLEO-F070RB, NUCLEO-F072RB, NUCLEO-F091RC, NUCLEO-F401RE, NUCLEO-F410RB, NUCLEO-F411RE, NUCLEO-F446RE, NUCLEO-G071RB, NUCLEO-L053R8, NUCLEO-L073RZ, NUCLEO-L412RB-P, NUCLEO-L433RC-P, NUCLEO-L452RE, NUCLEO-L452RE-P and NUCLEO-L476RG Nucleo boards.

Figure 1. X-NUCLEO-GFX01M1 top view

Figure 2. X-NUCLEO-GFX01M1 bottom view



Pictures are not contractual.

1 Features

- 2.2” SPI QVGA TFT LCD
- 64-Mbit SPI NOR Flash memory
- Joystick for easy menu navigation
- Compatible with selected STM32 Nucleo boards using the ST morpho interface

2 Ordering information

To order the X-NUCLEO-GFX01M1 module, refer to Table 1.

Table 1. Ordering information

Order code	Board reference	Target STM32
X-NUCLEO-GFX01M1	MB1642	Not applicable

The STM32 Nucleo boards feature STM32 32-bit microcontrollers based on the Arm® Cortex®-M processor.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2.1 Product marking

The sticker located on the top or bottom side of the PCB board shows the information about product identification such as board reference, revision and serial number.

The first identification line has the following format: “MBxxxx-Variant-yzz”, where “MBxxxx” is the board reference, “Variant” (optional) identifies the mounting variant when several exist, "y" is the PCB revision and "zz" is the assembly revision: for example B01.

The second identification line is the board serial number used for traceability.

Evaluation tools marked as “ES” or “E” are not yet qualified and therefore not ready to be used as reference design or in production. Any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering sample tools as reference designs or in production.

“E” or “ES” marking examples of location:

- On the targeted STM32 that is soldered on the board (For an illustration of STM32 marking, refer to the STM32 datasheet “Package information” paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck or silk-screen printed on the board.

3 Development environment

3.1 Demonstration software

The demonstration software supporting the X-NUCLEO-GFX01M1 expansion board is available from the X-CUBE-DISPLAY STM32Cube Expansion Package and must be programmed into the corresponding Nucleo board. The latest versions of the demonstration source code and associated documentation can be downloaded from *www.st.com*.

4 Quick start

Before the first use, make sure that no damage occurred to the board during shipment:

- All socketed components must be firmly secured in their sockets
- Nothing should be loose in the board plastic bag or in the box

To start using the X-NUCLEO-GFX01M1 expansion board, follow the steps below:

1. Plug the board on a compatible STM32 Nucleo development board
2. Download the evaluation firmware and full set of documentation from www.st.com/x-cube-display and program the target device
3. Evaluate the graphic possibilities of STM32 devices combined with the TouchGFX Engine graphic library in X-CUBE-TOUCHGFX or develop your own application

5 Hardware layout and configuration

Figure 3 and Figure 4 help users to locate the different features on the X-NUCLEO-GFX01M1 board. The mechanical dimensions of the X-NUCLEO-GFX01M1 product are shown in Figure 5.

Figure 3. X-NUCLEO-GFX01M1 PCB layout: top side

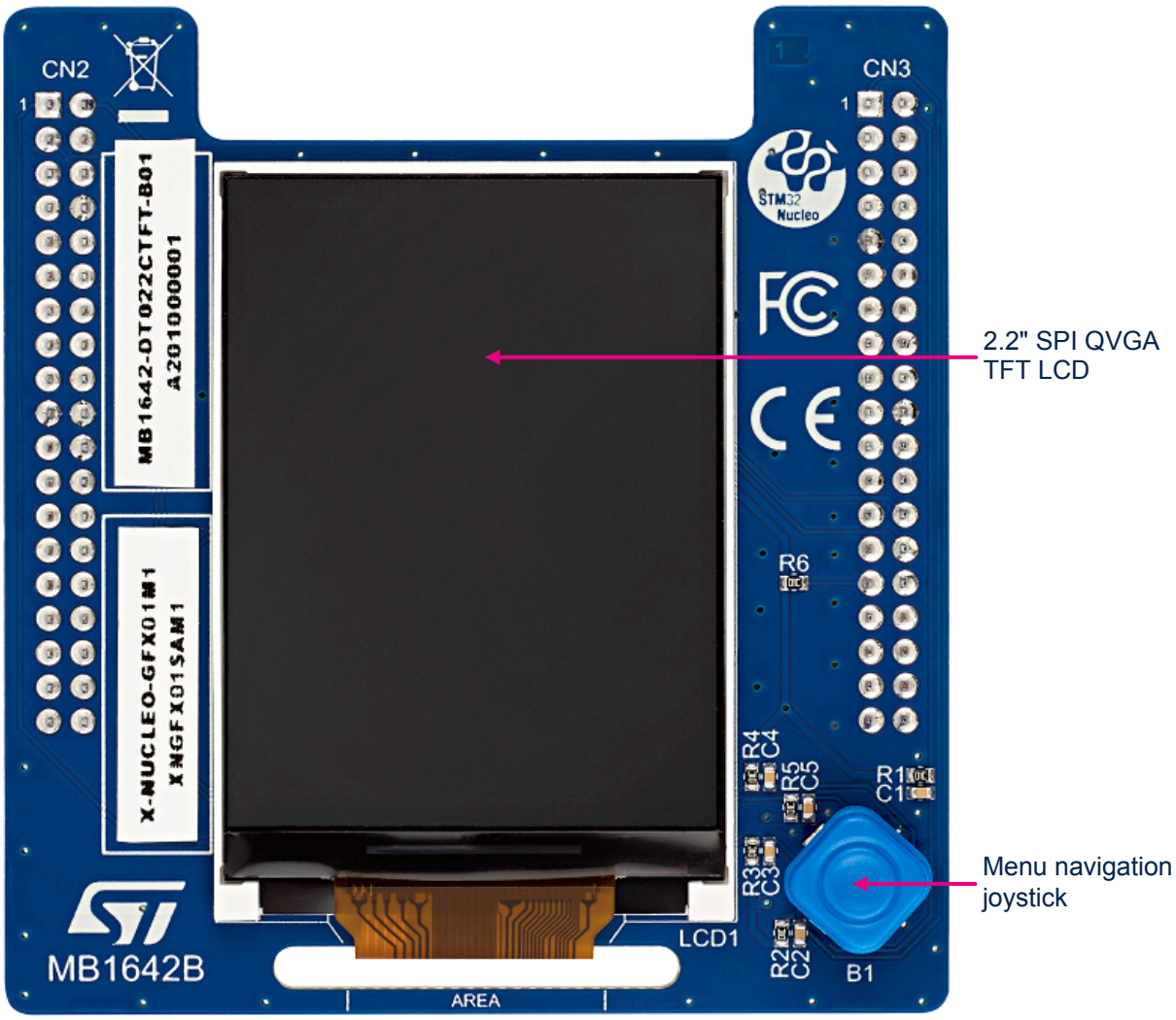


Figure 4. **X-NUCLEO-GFX01M1 PCB layout: bottom side**

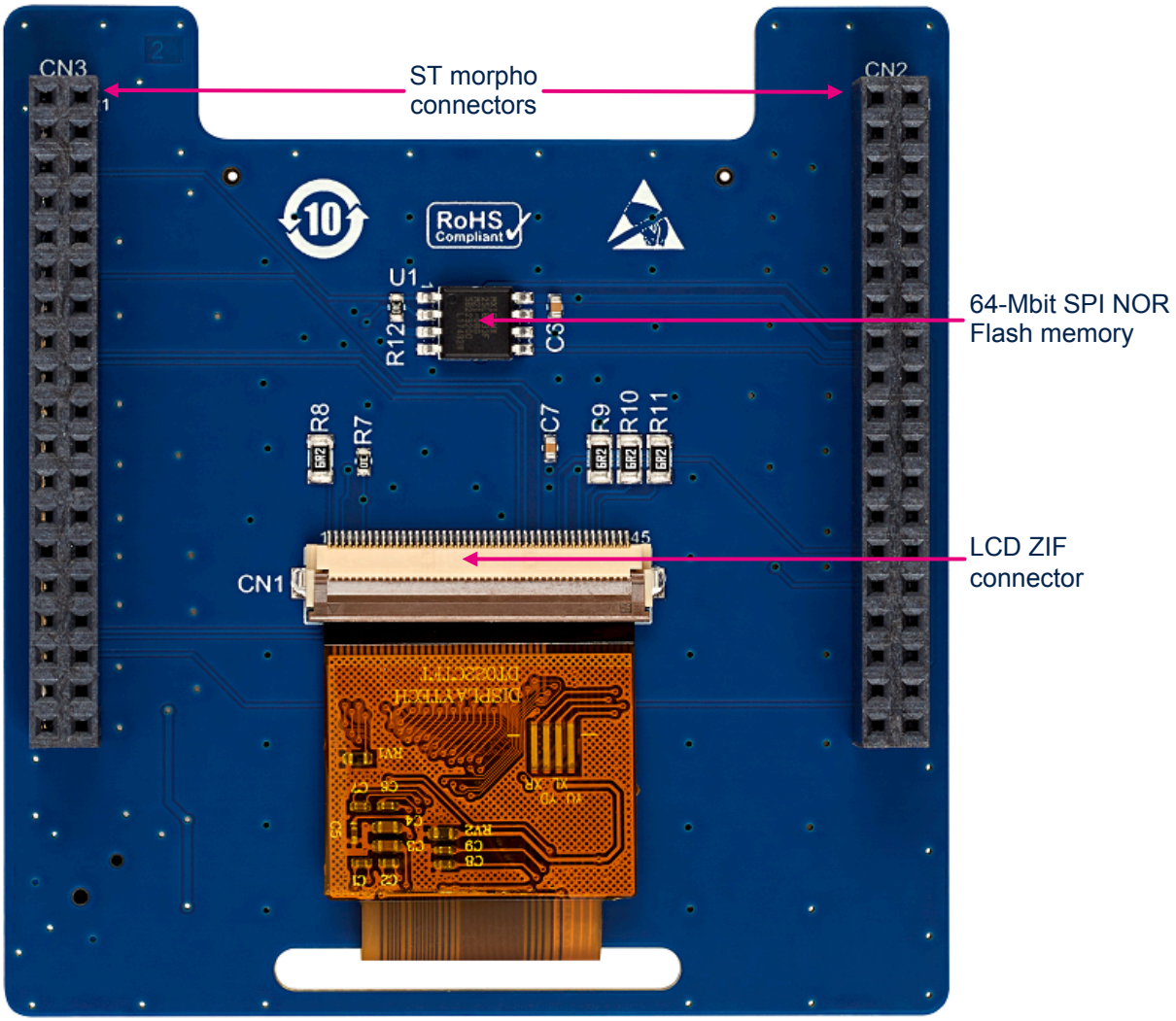
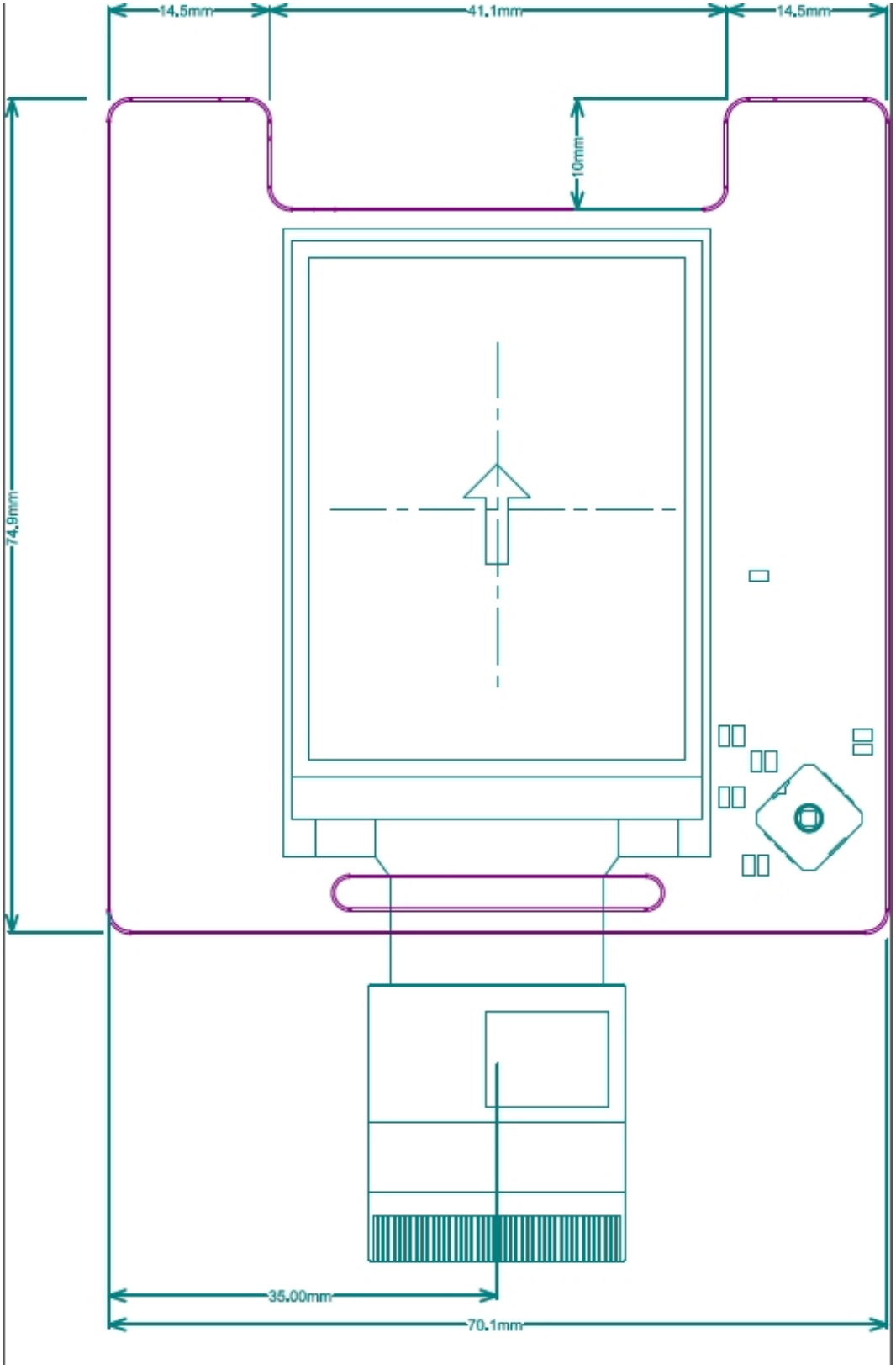


Figure 5. **X-NUCLEO-GFX01M1 mechanical drawing**



5.1 Power supply

The X-NUCLEO-GFX01M1 is directly powered by a 3.3 V power supply provided by the Nucleo development board through pin 16 of the CN2 connector.

5.2 SPI QVGA TFT LCD (LCD1)

5.2.1 Description

The SPI QVGA TFT LCD is connected to a first SPI interface (SPIA) of the STM32 device.

5.2.2 Operating voltage

The LCD is designed to operate only with a 3.3 V compatible SPI and GPIO interface.

5.2.3 I/O interface

Table 2. I/O configuration of the LCD

Pin number	Pin name	Signal name	STM32 GPIO	Function
1	LED_K4	-	-	Display backlight LED4 cathode
2	IM0	GND	-	System interface selection: 4-line 8-bit data SPI mode
3	IM1	3V3	-	
4	IM2	3V3	-	
5	IM3	3V3	-	
6	RESET	DISP_NRESET_PA1	PA1(1) (2)	Reset active low
7 - 28	-	-	-	Not connected
29	SDO	SPIA_MISO_PA6_PB14	PA6(1) PB14(2)	SPI master in/slave out
30	SDI	SPIA_MOSI_PA7_PB15	PA7(1) PB15(2)	SPI master out/slave in
31	RD	-	-	Not connected
32	RS/SCL	SPIA_SCK_PA5_PB13	PA5(1) PB13(2)	SPI serial clock
33	WR	SPIA_DCX_PB3_PB3	PB3(1) (2)	SPI write enable
34	CS	SPIA_NCS_PB5_PB5	PB5(1) (2)	SPI chip select active high
35	FMARK	DISP_TE_PA0	PA0(1) (2)	Tearing effect output pin to synchronize MCU on frame writing
36	VCC	3V3	-	3.3V power supply
37	GND	GND	-	Ground
38	LED_A	3V3	-	Display backlight LED common anode
39	LED_K1	-	-	Display backlight LED1 cathode
40	LED_K2	-	-	Display backlight LED2 cathode
41	LED_K3	-	-	Display backlight LED3 cathode
42 - 45	-	-	-	Not connected

1. *STM32 GPIO for NUCLEO-F030R8, NUCLEO-F070RB, NUCLEO-F072RB, NUCLEO-F091RC, NUCLEO-F401RE, NUCLEO-F410RB, NUCLEO-F411RE, NUCLEO-F446RE, NUCLEO-G071RB, NUCLEO-L053R8, NUCLEO-L073RZ, NUCLEO-L452RE and NUCLEO-L476RG.*
2. *STM32 GPIO for NUCLEO-L412RB-P, NUCLEO-L433RC-P and NUCLEO-L452RE-P.*

5.3 SPI NOR Flash memory (U1)

5.3.1 Description

The 64-Mbit SPI NOR Flash memory is connected to a second SPI interface (SPIB) of the STM32 device and can be used to store graphic objects. The use of a second SPI ensures optimum data transfer between the Flash memory and the LCD display.

5.3.2 Operating voltage

The NOR Flash memory is designed to operate only with a 3.3 V SPI interface.

5.3.3 I/O interface

Table 3. I/O configuration of the NOR Flash memory

Pin number	Pin name	Signal name	STM32 GPIO	Function
1	CS#	SPIB_NCS_PB9_PB7	PB9(1) PB7(2)	SPI chip select active high
2	SO	SPIB_MISO_PC2_PA6	PC2(1) PA6(2)	SPI master in/slave out
3	WP#	-	-	Write protection feature disabled
4	GND	GND	-	Ground
5	SI	SPIB_MOSI_PC3_PA12	PC3(1) PA12(2)	SPI master out/slave in
6	SCLK	SPIB_SCK_PB13_PA5	PB13(1) PA5(2)	SPI chip select active low
7	HOLD#	-	-	Pause feature disabled
8	VCC	3V3	-	3.3V power supply

1. *STM32 GPIO for NUCLEO-F030R8, NUCLEO-F070RB, NUCLEO-F072RB, NUCLEO-F091RC, NUCLEO-F401RE, NUCLEO-F410RB, NUCLEO-F411RE, NUCLEO-F446RE, NUCLEO-G071RB, NUCLEO-L053R8, NUCLEO-L073RZ, NUCLEO-L452RE and NUCLEO-L476RG.*
2. *STM32 GPIO for NUCLEO-L412RB-P, NUCLEO-L433RC-P and NUCLEO-L452RE-P.*

5.4 Joystick (B1)

5.4.1 Description

The joystick (B1) allows the navigation within the menu displayed on the LCD.

5.4.2 I/O interface

Table 4. I/O configuration of the joystick

Pin number	Pin name	Signal name	STM32 GPIO	Function
1	LEFT	KEY_LEFT_PC9	PC9	Joystick left direction (active low)
2	CENTER	KEY_CENTER_PC8	PC8	Joystick center (active low)
3	DOWN	KEY_DOWN_PC10	PC10	Joystick down direction (active low)
4	UP	KEY_UP_PC12	PC12	Joystick up direction (active low)
5	COMMON	GND	-	Common connected to ground
6	RIGHT	KEY_RIGHT_PC11	PC11	Joystick right direction (active low)

5.5 ST morpho connectors (CN2 and CN3)

5.5.1 Description

The ST morpho connectors allow the X-NUCLEO-GFX01M1 connection to a standard Nucleo-64 development board.

5.5.2 I/O interface

Figure 6. **Pinout of the ST morpho connectors**

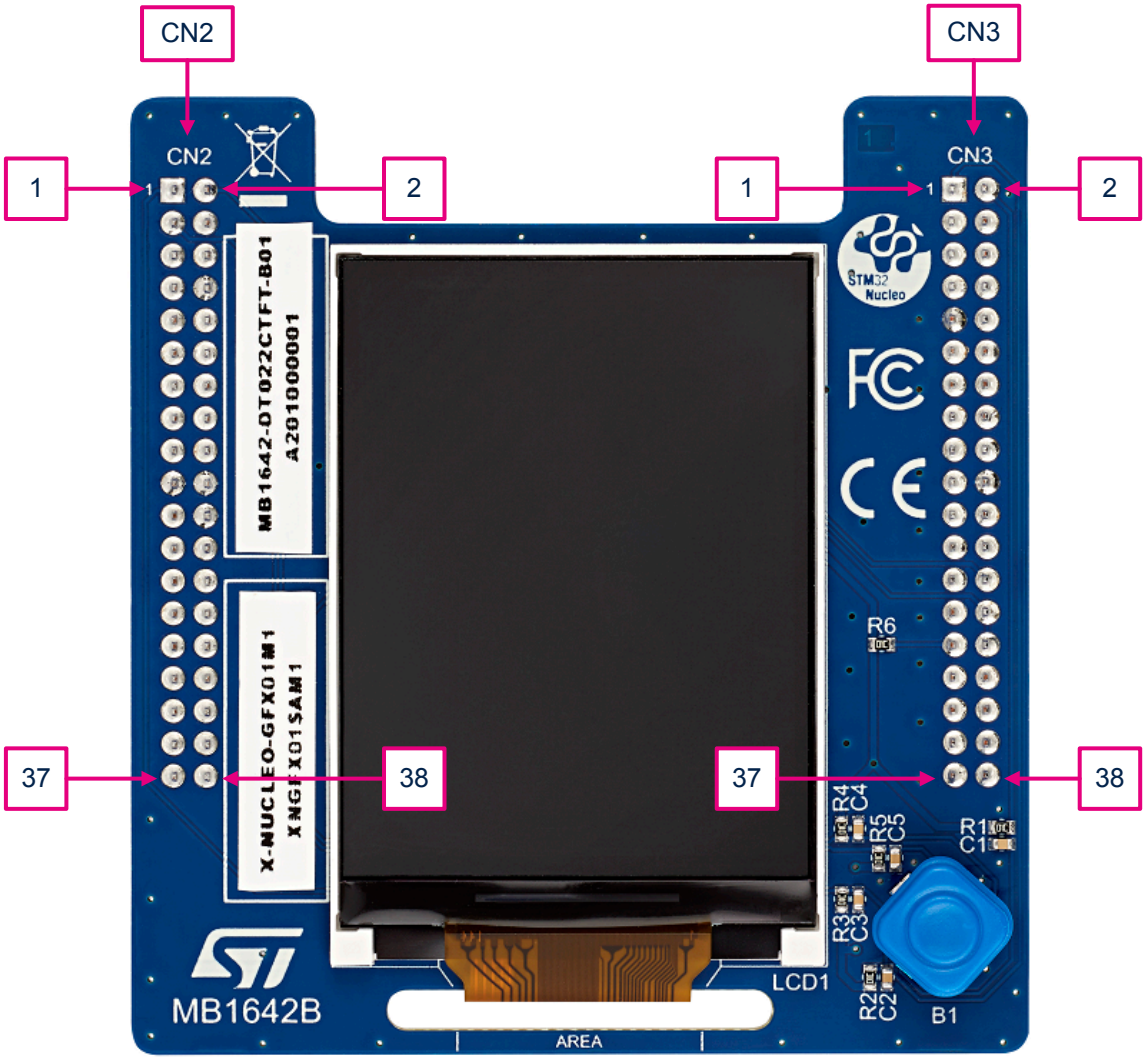


Table 5. I/O configuration of ST morpho connector CN2

Pin number	Pin name	Signal name	STM32 GPIO	Function
1	DOWN	KEY_DOWN_PC10	PC10(1) (2)	Joystick down direction (active low)
2	RIGHT	KEY_RIGHT_PC11	PC11(1) (2)	Joystick right direction (active low)
3	UP	KEY_UP_PC12	PC12(1) (2)	Joystick up direction (active low)
4 - 7	-	-	-	Not connected
8	-	-	-	Ground
9 - 15	-	-	-	Not connected
16	-	3V3	-	3.3V power supply
17 – 18	-	-	-	Not connected
19	GND	-	-	Ground
20	GND	-	-	Ground
21	-	-	-	Not connected
22	GND	-	-	Ground
23 – 27	-	-	-	Not connected
28	FMARK	DISP_TE_PA0	PA0(1) (2)	Display tearing effect output pin to synchronize MCU on frame writing
29	-	-	-	Not connected
30	RESET	DISP_NRESET_PA1	PA1(1) (2)	Reset active low
31 – 34	-	-	-	Not connected
35	SO	SPIB_MISO_PC2_PA6	PC2(1)	Flash memory SPI master in/slave out
36	-	-	-	Not connected
37	SI	SPIB_MOSI_PC3_PA12	PC3(1)	Flash memory SPI master out/slave in
38	-	-	-	Not connected

1. *STM32 GPIO for NUCLEO-F030R8, NUCLEO-F070RB, NUCLEO-F072RB, NUCLEO-F091RC, NUCLEO-F401RE, NUCLEO-F410RB, NUCLEO-F411RE, NUCLEO-F446RE, NUCLEO-G071RB, NUCLEO-L053R8, NUCLEO-L073RZ, NUCLEO-L452RE and NUCLEO-L476RG.*
2. *STM32 GPIO for NUCLEO-L412RB-P, NUCLEO-L433RC-P and NUCLEO-L452RE-P.*

Table 6. I/O configuration of ST morpho connector CN3

Pin number	Pin name	Signal name	STM32 GPIO	Function
1	LEFT	KEY_LEFT_PC9	PC9(1) (2)	Joystick left direction (active low)
2	CENTER	KEY_CENTER_PC8	PC8(1) (2)	Joystick center (active low)
3 – 4	-	-	-	Not connected
5	CS#	SPIB_NCS_PB9_PB7	PB9(1) PB7(2)	Flash memory SPI chip select active high
6 - 8	-	-	-	Not connected
9	GND	-	-	Ground
10	-	-	-	Not connected
11	RS/SCL	SPIA_SCK_PA5_PB13	PA5(1) PB13(2)	Display SPI serial clock
12	-	-	-	Not connected
13	SDO	SPIA_MISO_PA6_PB14	PA6(1) PB14(2)	Display SPI master in/slave out
14	-	-	-	Not connected
15	SDI	SPIA_MOSI_PA7_PB15	PA7(1) PB15(2)	Display SPI master out/slave in
16-19	-	-	-	Not connected
20	GND	-	-	Ground
21 – 25	-	-	-	Not connected
26	SO	SPIB_MISO_PC2_PA6	PA6(2)	Flash memory SPI master in/slave out
27	-	-	-	Not connected
28	SCLK	SPIB_SCK_PB13_PA5	PA5(2)	Flash memory SPI chip select active low
29	CS	SPIA_NCS_PB5_PB5	PB5(1) (2)	Display SPI chip select active high
30	SCLK	SPIB_SCK_PB13_PA5	PB13(1)	Flash memory SPI chip select active low
31	WR	SPIA_DCX_PB3_PB3	PB3(1) (2)	Display SPI write enable
32	-	-	-	Not connected
33	SI	SPIB_MOSI_PC3_PA12	PA12(2)	Flash memory SPI master out/slave in
34 - 38	-	-	-	Not connected

1. *STM32 GPIO for NUCLEO-F030R8, NUCLEO-F070RB, NUCLEO-F072RB, NUCLEO-F091RC, NUCLEO-F401RE, NUCLEO-F410RB, NUCLEO-F411RE, NUCLEO-F446RE, NUCLEO-G071RB, NUCLEO-L053R8, NUCLEO-L073RZ, NUCLEO-L452RE and NUCLEO-L476RG.*
2. *STM32 GPIO for NUCLEO-L412RB-P, NUCLEO-L433RC-P and NUCLEO-L452RE-P.*

6 Federal Communications Commission (FCC) and ISED Canada Compliance Statements

6.1 FCC Compliance Statement

Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

Part 15.105

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Responsible party (in the USA)

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Telephone: +1 972-466-7845

6.2 ISED Compliance Statement

This device complies with FCC and ISED Canada RF radiation exposure limits set forth for general population for mobile application (uncontrolled exposure). This device must not be collocated or operating in conjunction with any other antenna or transmitter.

Compliance Statement

Notice: This device complies with ISED Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

ISED Canada ICES-003 Compliance Label: CAN ICES-3 (A) / NMB-3 (A).

Déclaration de conformité

Avis: Le présent appareil est conforme aux CNR d'ISDE Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Étiquette de conformité à la NMB-003 d'ISDE Canada: CAN ICES-3 (A) / NMB-3 (A).

7 CE conformity

7.1 Warning

EN 55032 / CISPR32 (2012) Class A product

Warning: this device is compliant with Class A of EN55032 / CISPR32. In a residential environment, this equipment may cause radio interference.

Avertissement : cet équipement est conforme à la Classe A de la EN55032 / CISPR 32. Dans un environnement résidentiel, cet équipement peut créer des interférences radio.

Revision history

Table 7. **Document revision history**

Date	Version	Changes
26-Aug-2020	1	Initial release.

Contents

List of tables

List of figures