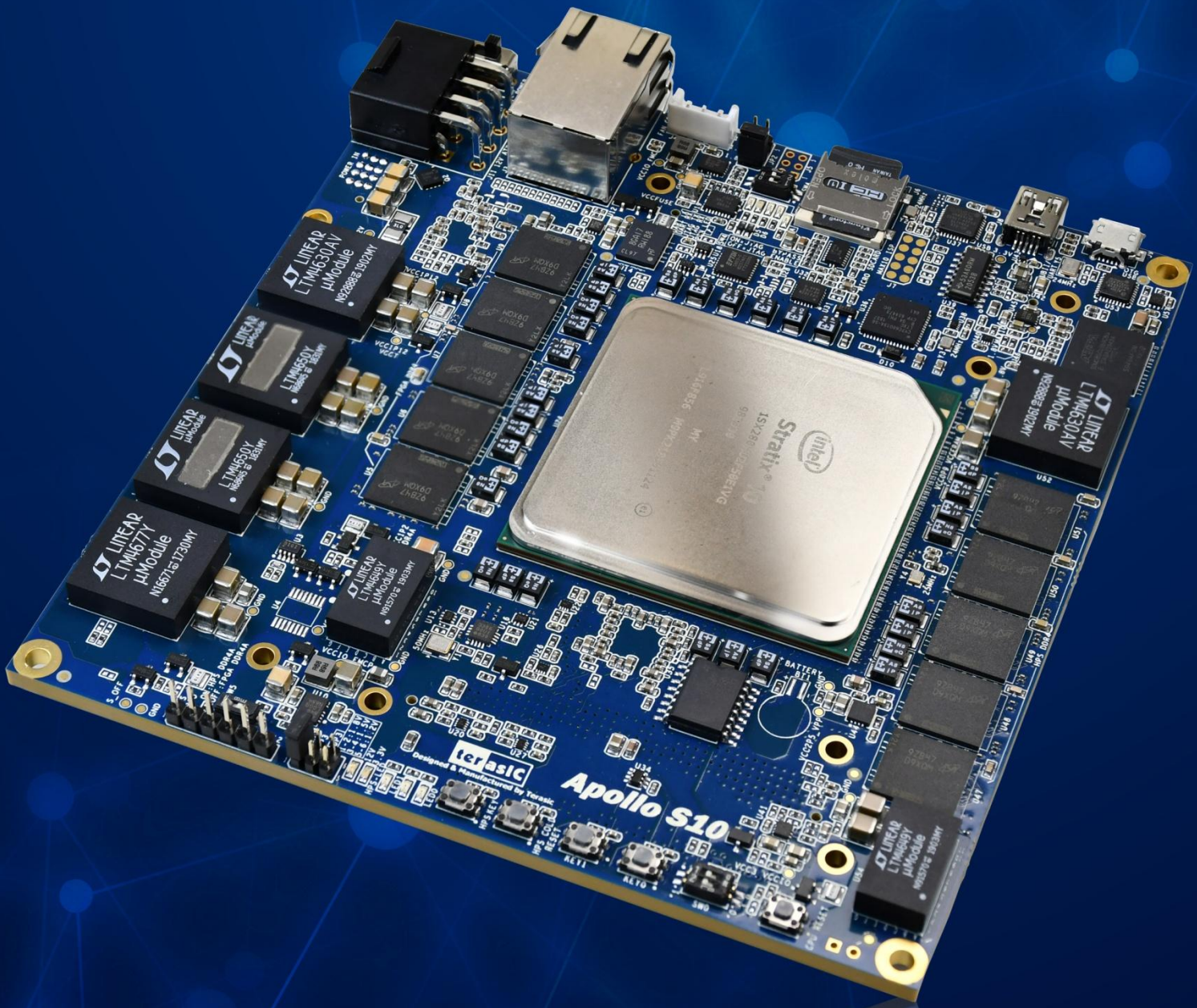
Apollo S10 SoM Board

USER MANUAL



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Contents

Chapter 1

Overview

This chapter provides an overview of the Apollo S10 SoM Board and installation guide.

1.1 General Description

Designed for modular and scalable high-performance FPGA Prototyping and HPC solutions, Apollo S10 SoM packs unbeatable performance and energy efficiency in a tiny form factor and provides up to 90X performance increase over CPUs for critical workloads such as simulation acceleration, molecular dynamics, machine learning.

Apollo S10 SoM takes advantage of the latest Intel® Stratix® 10 SoC with 2800K logic elements to obtain speed and power breakthrough (with up to 70% lower power). Combining a number of high-end hardware interfaces such as high-capacity and high-bandwidth DDR4 SDRAM (up to 64GB), on-board USB-Blaster II, and FMC/FMC+ connectors for I/O expansion, the board delivers more than 2X the performance of previous generation development kits.

Apollo S10 SoM is also extensible. Apollo Carrier board is designed to assist our clients' development of Apollo S10 SoM. The carrier board features two ultra low-latency, straight connections 40Gbps QSFP+ module and Thunderbolt™ 3 for our clients' to evaluate the I/O planned for their systems, and build their custom systems around it.

Figure 1-1 Apollo S10 board with heat sink and fan

1.2 Board Layout

The figures below depict the layout of the board and indicate the location of the connectors and key components.

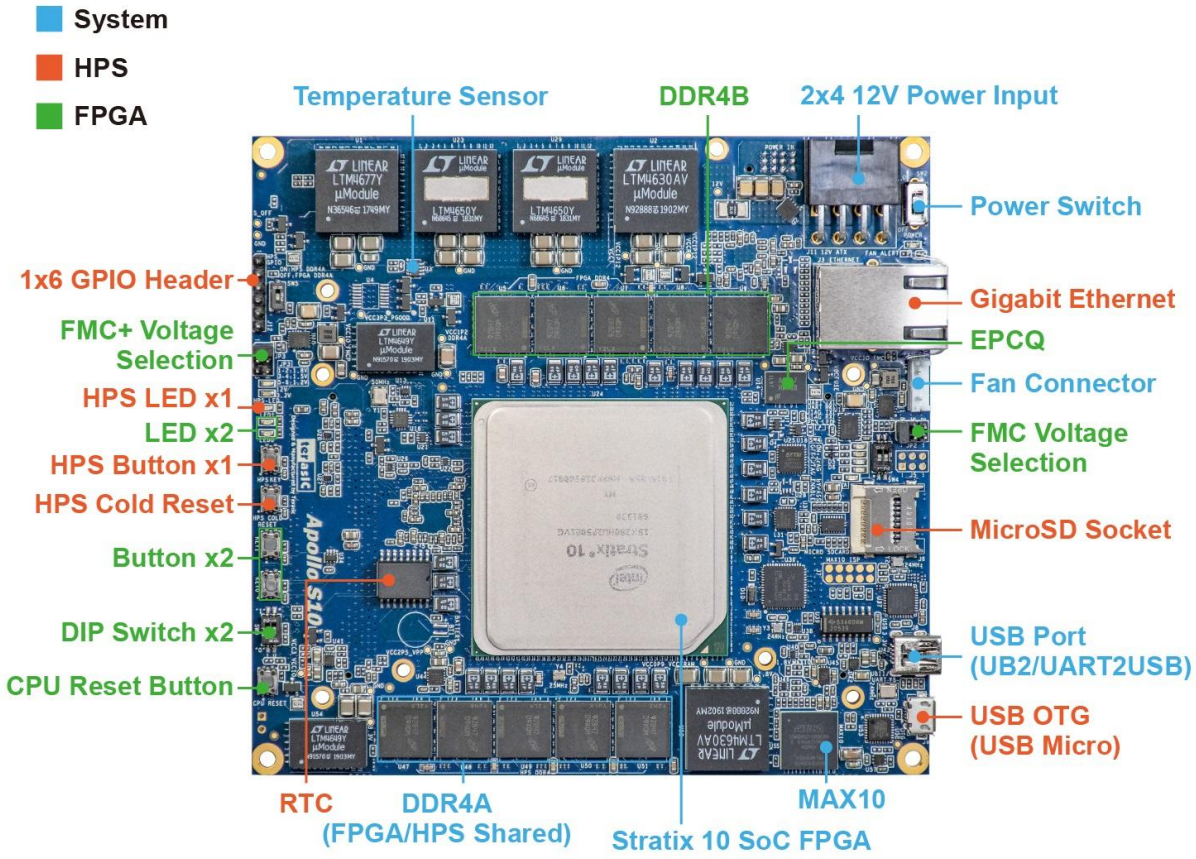


Figure 1-2 Apollo S10 board top

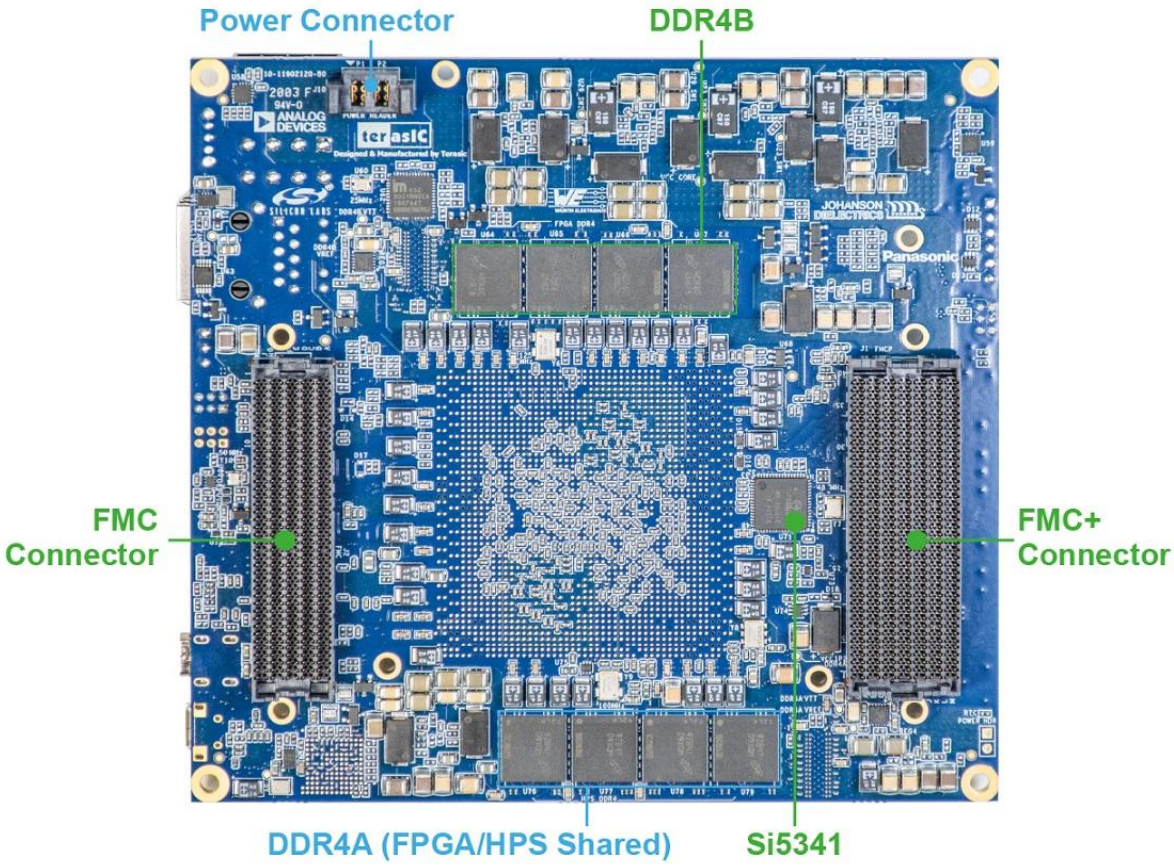


Figure 1-3 Apollo S10 board bottom

1.3 Key Features

The following hardware is implemented on the Apollo S10 board:

■ FPGA Device

- Intel Stratix ® 10 SoC FPGA : 1SX280HU2F50E1VG
  - 2,800K logic elements (LEs)
  - 229 Mbits embedded memory(M20K)
  - 96 transceivers (up to 28.3Gbps)
  - 11,520 18-bit x 19-bit multipliers
  - 5,760 Variable-precision DSP blocks

FPGA Configuration

- On-Board USB Blaster II for FPGA programming and Debug
- AS Mode configuration from QSPI Flash

FPGA Fabric

- 1024Mbit QSPI Flash (EPCQL1024 Compliant)
- 2 on-board independent DDR4 banks
  - Each 32GB x72bit DDR4-2133MT/s
  - One bank is shared with FPGA and HPS
- FMC (Vita57.1) connector with 10 transceivers
  - FMC 1.8V/1.5V/1.2V Voltage Selection
- FMC+(Vita57.4) connector with 24 transceivers
  - FMC+ 1.8V/1.5V/1.2V Voltage Selection
- Two 50Mhz Single-ended Clock Source
- Clock Generator Si5341
- LED x2, Button x2, DIP Switch x2, CPU Reset

HPS(Hard Processor System) Fabric

- Quad-core 64 bit ARM Cortex-A53 MPCore* processor
- MicroSD Socket
- Gigabit Ethernet with RJ45
- USB OTG with Micro USB Connector
- UART to USB with Mini USB Connector
- LED x1, Button x1, Cold Reset Button
- 1x6 GPIO Header
- RTC

Dashboard System

- Input Power Monitor
- FPGA and Board Temperature Monitorl
- Fan Control and Monitor
- Auto Fan Speed
- Auto Shutdown

- **Power Source**
  - 12V from 2x4 PCIe connector
  - 12V from Samtec connector (reserved for carrier board)

1.3. Block Diagram

Figure 1-4 shows the block diagram of the Apollo S10 board. To provide maximum flexibility for the users, all key components are connected to the Stratix ®10 SX FPGA device. Thus, users can configure the FPGA to implement any system design.

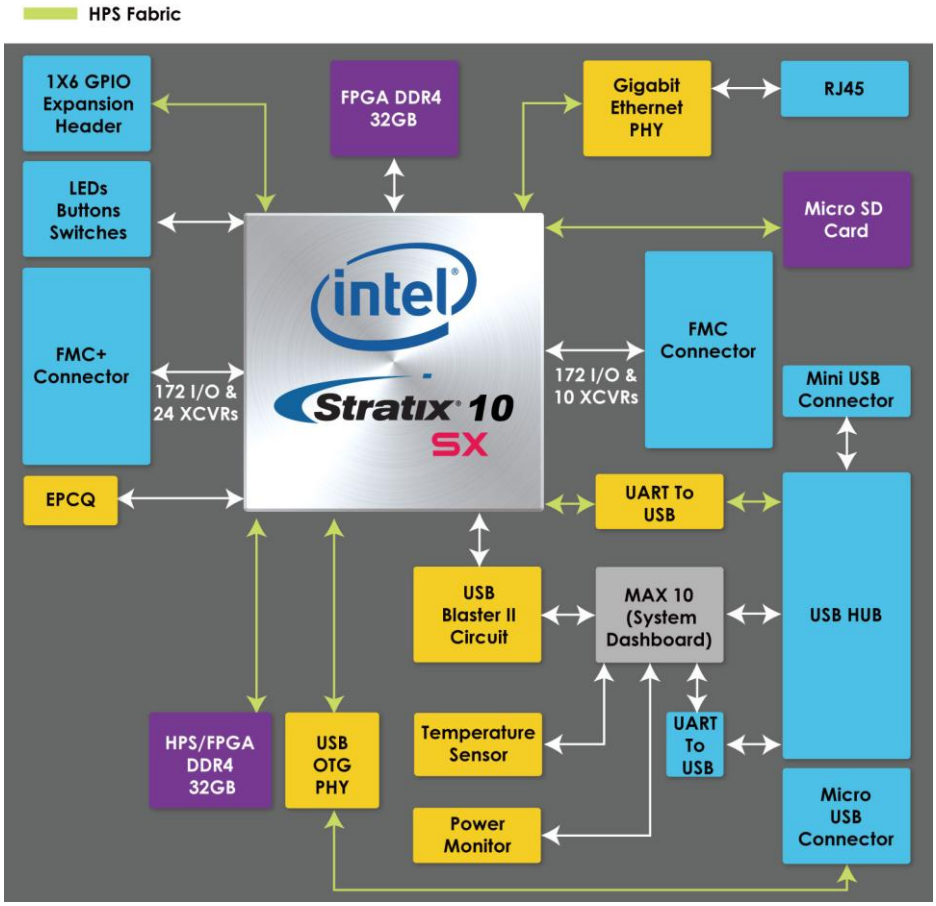


Figure 1-4 Block diagram of the Apollo S10 board

1.4. Mechanical Specifications

Figure 1-5 and **Figure 1-6** are the top and bottom Mechanical Layout of Apollo S10 board. The unit of the Mechanical Layout is millimeter (mm).

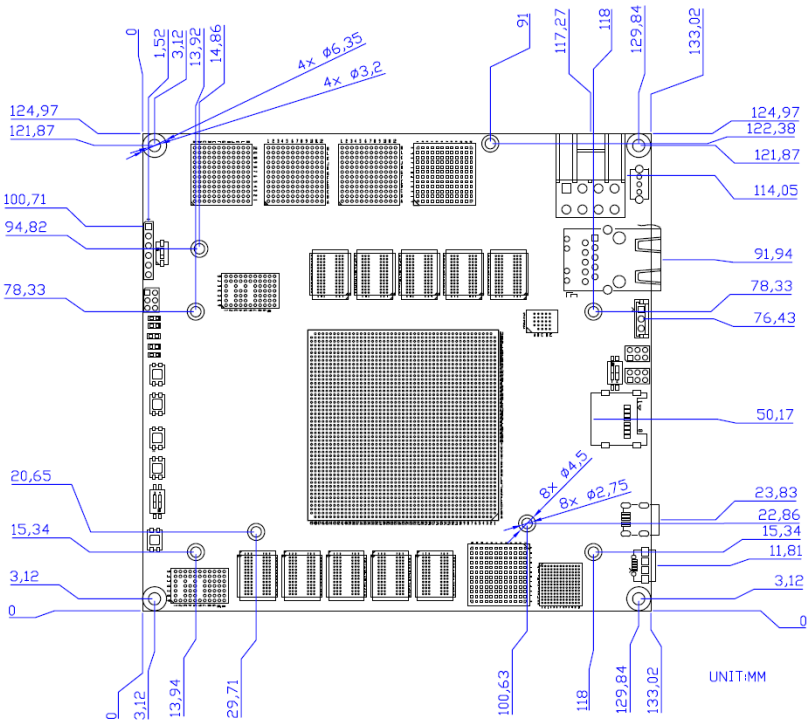


Figure 1-5 Top side mechanical layout

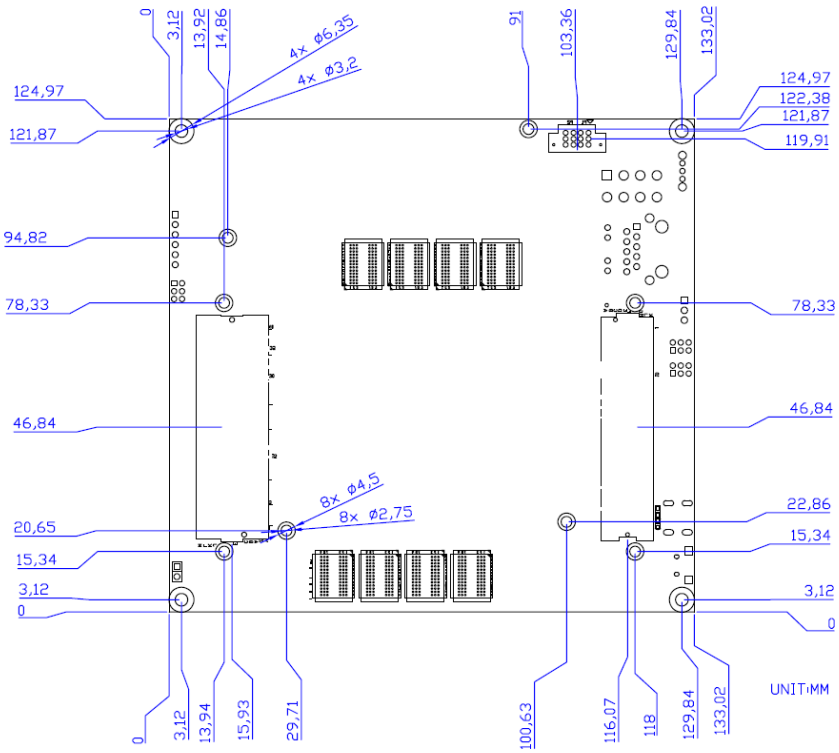


Figure 1-6 Bottom side mechanical layout

1.5. The Purpose of Screw Set

The screw set (See **Figure 1-7**) in the Apollo s10 SoM kit content is mainly provided for connecting to Terasic or user owned **carrier board** (See **Figure 1-8**). If the user wants to use screw set to the connection between Apollo S10 SoM and FMC / FMC + daughter card is not 100% applicable. We still recommend users to use the screw set provided by the daughter card to connect the Apollo S10 SoM.

For how to use screw set to connect module to carrier board, please refer to User manual of the Apollo Carrier board (*Apollo_Carrier_Board_User_Manual_revB.pdf*) in chapter 3 : Board Assembly.

Figure 1-7 Screw set provided in the kit content

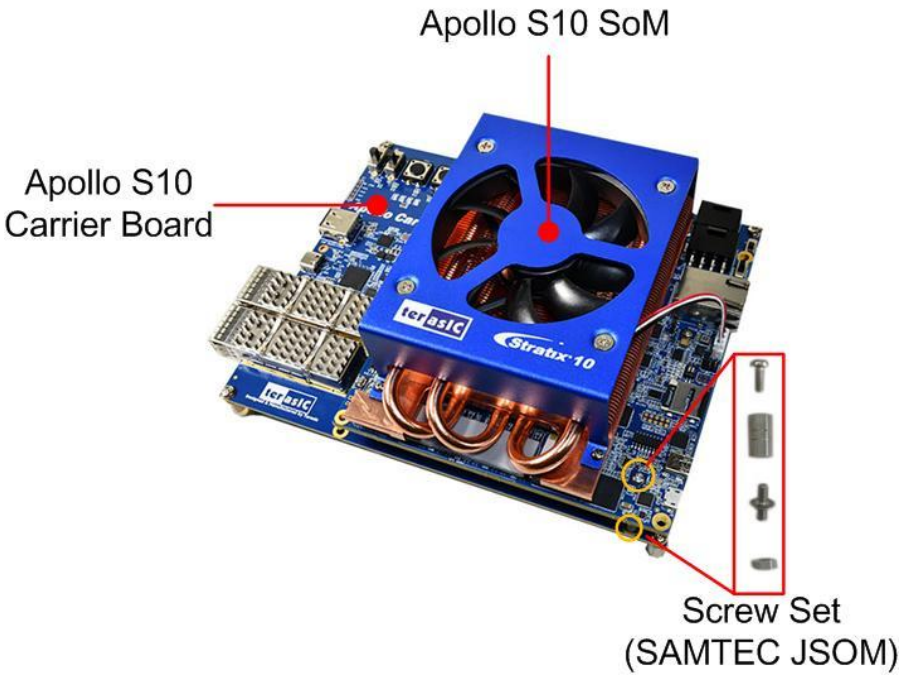


Figure 1-8 Screw set for connecting carried and module board

1.6. Power Requirement

■ **Stand-alone mode**

When the Apollo S10 board is used in stand-alone mode, users can use the 12V ATX power provided in the kit to connect to the 8-pin 12V ATX power connector (See **Figure 1-9** and **Figure 1-10**) of the Apollo S10.

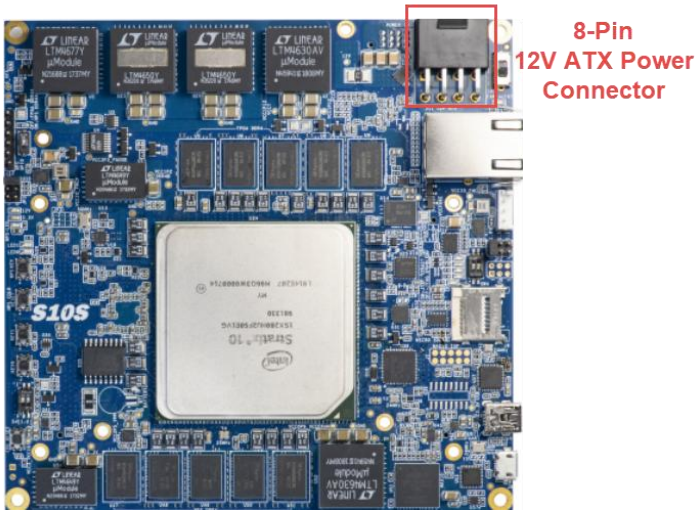


Figure 1-9 8-Pin 12V ATX Power Connector

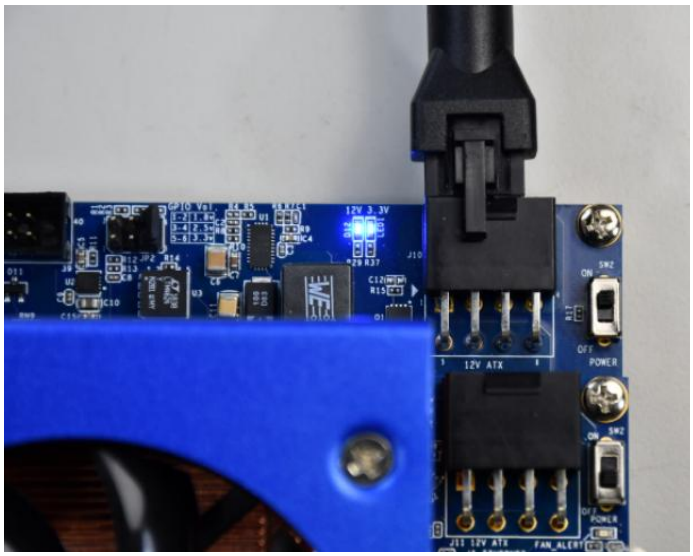


Figure 1-10 Connect 12V ATX Power Connector to Apollo S10

■ Connect to the based board

If user wants use the Apollo S10 board as the module board and connect it to the carrier board. The carrier board needs to provide at least **12V 15A** power to the J10 power connector (See **Figure 1-11**) of the Apollo S10 board. Please note that the 12V and 3.3V of the FMC and FMC + connector are provided by the Apollo S10 board, the carrier board does not need to provide these powers. For part number of the connector connected to J10, please refer to **Table 1-1** in the section 1.6.

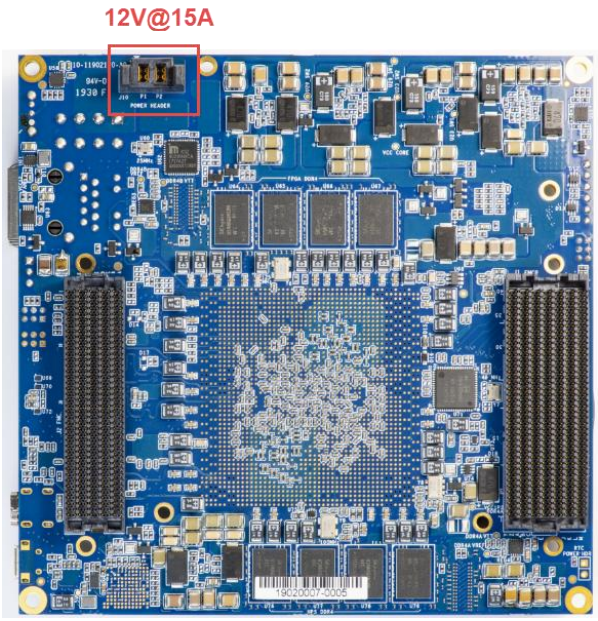


Figure 1-11 Power connector for connecting based board

1.7. Connectivity

The Apollo S10 board provides FMC and FMC + connector as expansion interface. Users can use Apollo S10 as stand alone, connect FMC daughter card (See **Figure 1-12**).

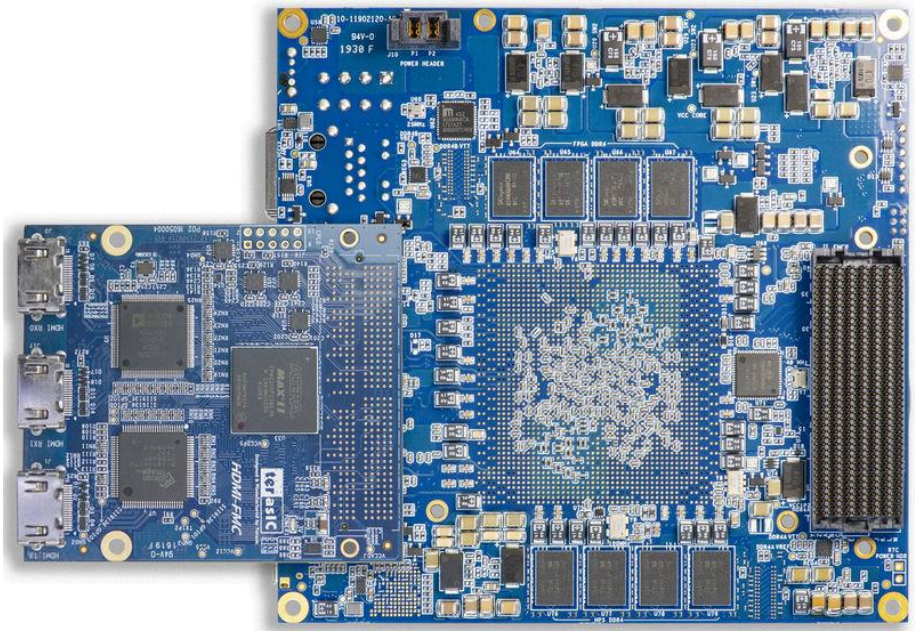


Figure 1-12 Apollo S10 board connects to the FMC daughter card

Users can also use Apollo-S10 as an FPGA module board and connect to other carrier boards to form a system (See **Figure 1-13**).

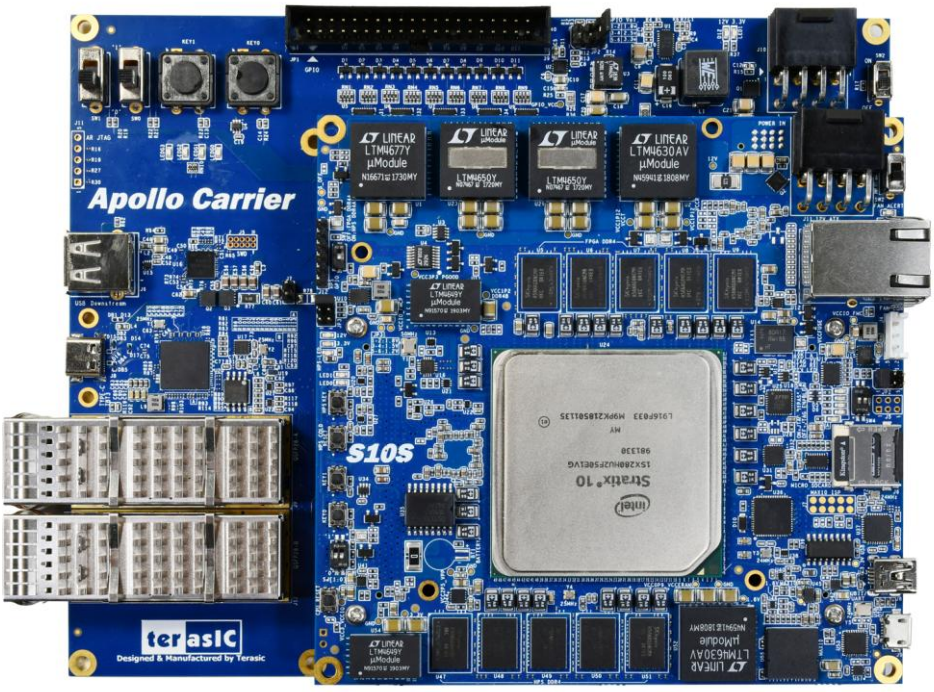


Figure 1-13 Apollo S10 board connects to the based board

If user wants to make their owned carrier board to connect with the Apollo S10 board, there are three connectors are needed to be used, they are FMC +, FMC and Power connector (See **Figure 1-14**). The following table lists the manufacturer and manufacturer part numbers of the three connectors that can match with the connectors of the Apollo S10 board.

Table 1-1 Part Number of the connector on the Apollo S10 board

Connector	Apollo S10 Board's Part Number	Carrier Board's Part Number
FMC	**J2** Samtec : ASP-134486-01	Samtec : ASP-134488-01
FMC+	**J1** Samtec : ASP-184329-01	Samtec : ASP-184330-01
Power Connector	**J10** Samtec : UPS-02-07.0-02-L-V	Samtec : UPT-02-03.0-01-L-V

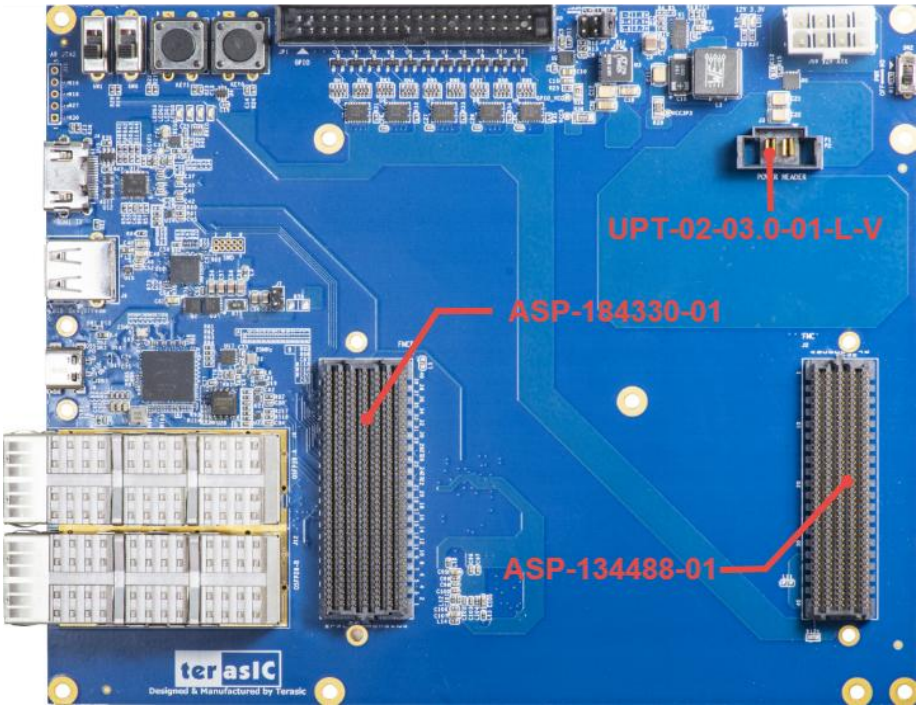


Figure 1-14 Part Number of the connector for based board

Chapter 2

Board Component

This chapter introduces all the important components on the Apollo S10.

2.1 Configuration Interface

This section describes the configuration mode for Stratix 10 SX FPGAs available on the Apollo S10. The peripheral circuits and usage scenarios for each mode will be listed.

As shown in **Figure 2-1**, the mode select pin of the FPGA on the Apollo-S10 board has been set to **Active Serial (AS) mode** using resistors. Thus, the Apollo S10 board supports the following configuration modes:

- JTAG Mode (Configure the FPGA using the on-board USB-Blaster II).
- Active Serial (AS) mode

Users can use these modes to configure the FPGA or HPS (Hardware Process System) fabric in the Stratix 10 SX FPGA and make the FPGA to run the user's logic or boot the HPS to run the OS.

Below we will introduce more detailed information of AS mode, as well as other configuration information.

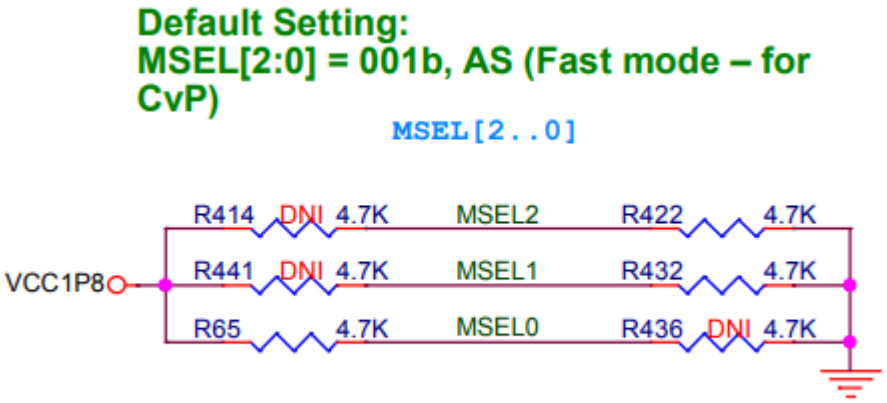


Figure 2-1 The MSEL pin setting

■ Active Serial (Fast) mode

In AS mode, the FPGA's configuration file is stored in the QSPI flash. The Secure Device Manager (SDM) in Stratix 10 FPGA is responsible for the entire AS mode process and interface. The SDM will load the initial configuration firmware from the QSPI flash to configure the FPGA including FPGA I / O and core configuration. HPS part of the boot can also be completed in this mode. **Figure 2-2** shows the architecture of the AS mode of the Apollo S10 board.

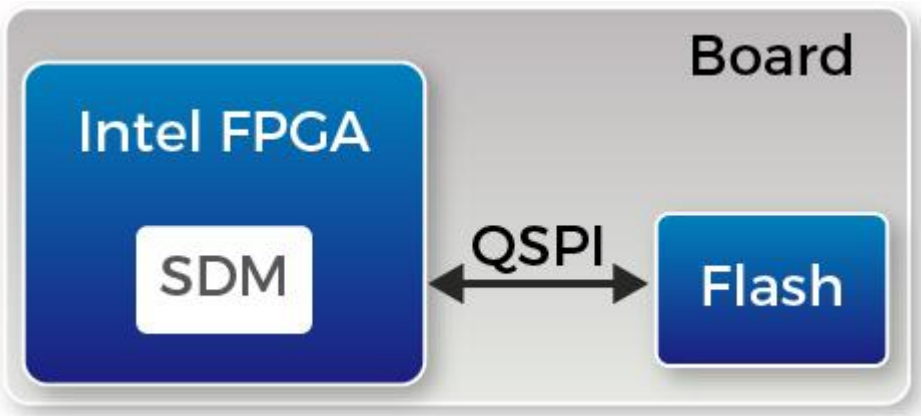


Figure 2-2 AS mode for the Apollo S10 board

For more information on the configuration of Stratix 10 FPGAs, please refer to the file: Intel Stratix 10 Configuration User Guide

■ SoC FPGA boot

The boot process for Stratix 10 SoC FPGAs can be divided into two different methods:

- FPGA Configuration First Mode
- HPS Boot First Mode

The difference between the two methods is the initial difference between HPS and FPGA fabric after powering on. More details can be found in the user documentation: Intel Stratix 10 SoC FPGA Boot User Guide.

The factory setting of the SoC boot of the Apollo S10 board is the **FPGA Configuration First Mode**. The architecture is shown in the **Figure 2-3**. Two storage mediums are used. The system needs QSPI flash on Apollo S10 as SDM flash for booting.

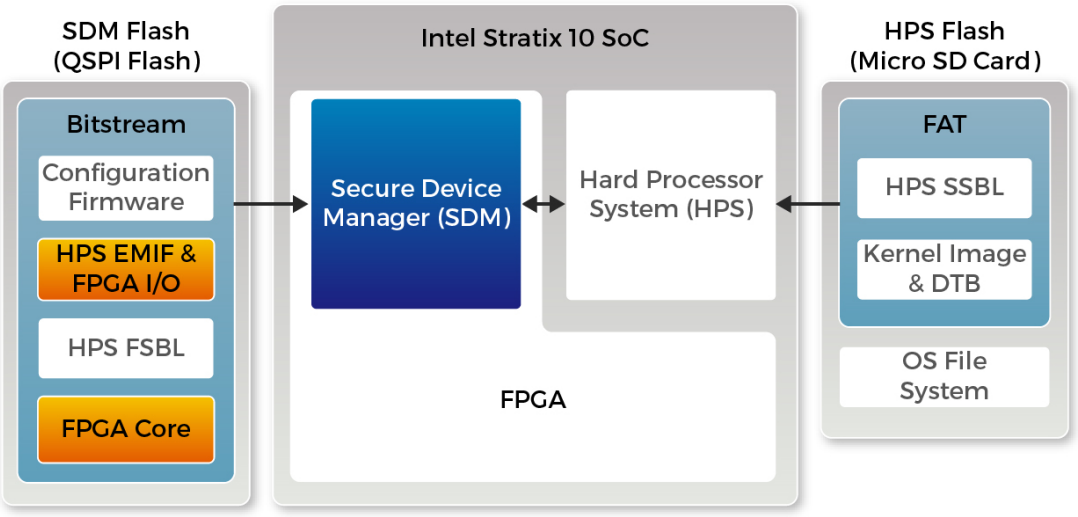


Figure 2-3 FPGA Configuration First Dual SDM and HPS Flash

The QSPI flash memory has the following boot data for the first part of the SoC FPGA configuration:

- Configuration firmware for the SDM
- FPGA I/O and HPS external memory interface (EMIF) I/O configuration data
- FPGA core configuration data
- HPS First-Stage Boot Loader(FSBL) code and FSBL hardware handoff binary data

Meanwhile, Terasic provides the micro SD card with built-in image data as HPS flash, which is used for HPS boot in the later part. The micro SD card stores the following data:

- Second-Stage Boot Loader(SSBL)
- Kernel Image and Device Tree Blob(DTB)
- Operating System

The factory SoC boot process of Apollo S10 is summarized as follows:

When the Apollo S10 board is powered on, the SDM will read the configuration firmware and complete SDM initial form the QSPI flash according to the MSEL pin setting. Then, the SDM will configure the FPGA I/O and core (full configuration).

After the FPGA is first configured, SDM continues to load the FSBL(First-Stage Boot Loader) from the QSPI flash and transfer it to the HPS on-chip RAM, and releases the HPS reset to let the HPS start using the FSBL hardware handoff file to setup the clocks, HPS dedicated I/Os, and peripherals.

The FSBL then loads the SSBL(Second-Stage Boot Loader) from the Micro SD Card into HPS SDRAM and passes the control to the SSBL. The SSBL enables more advanced peripherals and loads OS into SDRAM.

Finally, the OS boots and applications are scheduled for runtime launch.

■ JTAG Programming

The JTAG interface of the Apollo S10 is mainly implemented by the USB blaster II circuit on the board. For programming by on-board USB-Blaster II, the following procedures show how to download a configuration bit stream into the Stratix 10 SX FPGA:

- Make sure that power is provided to the FPGA board
- Connect your PC to the FPGA board using a micro-USB cable and make sure the USB-Blaster II driver is installed on the PC.
- Launch Quartus Prime programmer and make sure the USB-Blaster II is detected.
- In Quartus Prime Programmer, add the configuration bit stream file (.so

f), check the associated “Program/Configure” item, and click “Start” to start FPGA programming.

■ Quartus Prime 19.1 Patch

If user using the Intel® Quartus® Prime Pro Edition software version 19.1 with on board USB blaster II circuit on the Apollo S10 board, a USB device enumeration error may occur when using the USB blaster II circuit to the computer hosting the Intel® Quartus® Prime Pro Edition software. To workaround this problem, please download and install patch 0.03 from the links below.
You must install the Intel® Quartus® Prime Pro Edition software version 19.1 software before installing this patch:

- Download the version 19.1 patch 0.03 for Linux (.run)
- Download the version 19.1 patch 0.03 for Window (.run)
- Download the Readme for the version 19.1 patch 0.03 (.txt)

2.2 Setup and Status Components

This section will introduce the use of the switch for setup on the Apollo S10 board, as well as a description of the various status LEDs.

■ Status LED

The FPGA development board includes board-specific status LEDs to indicate board status. Please refer to **Table 2-1** for the description of the LED indicators. **Figure 2-4** shows the location of all these status LED.

Table 2-1 Status LED

Board Reference	LED Name	Description
D1	FAN_ALERT	Illuminates when the fan is abnormal, such as when the fan speed is different from expected
D2	12-V Power	Illuminates when 12-V power is active.
D3	3.3-V Power	Illuminates when 3.3-V power is active.
TXD	UART_TXLED	T Illuminates when the UART interface is transmitting data
RXD	UART_RXLED	T Illuminates when the UART interface is receiving data

D7	JTAG_TX	Illuminates when the USB Blaster II circuit is transmitting data
D8	JTAG_RX	Illuminates when the USB Blaster II circuit is receiving data
D9	FPGA_PDN_LED	When the FPGA temperature or the board temperature exceeds 95 degrees or the power consumption exceeds 180W, all the power of the FPGA will be cut off, and the D9 will be flashing.

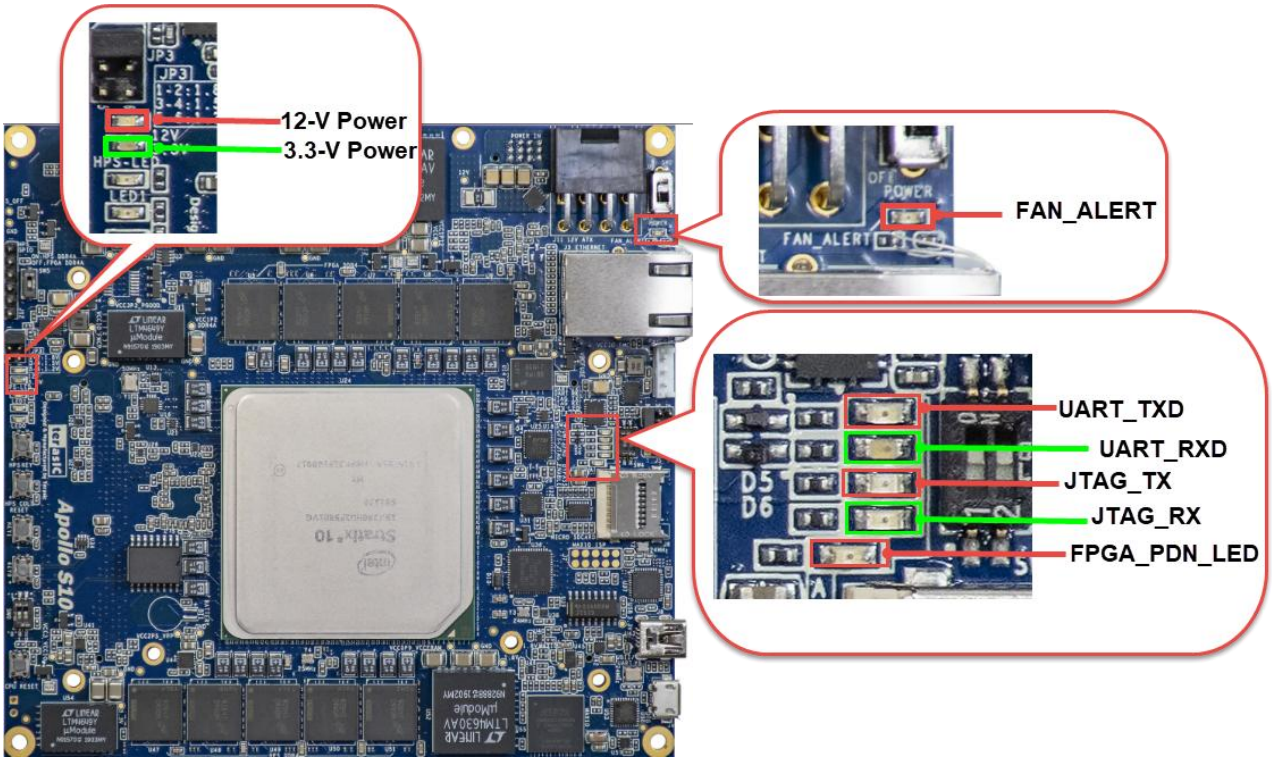


Figure 2-4 Position of the status LED

■ JTAG Interface Switch

The JTAG interface switch **SW4** is to set whether the JTAG interface of the FMC and FMC + connector is connected to the JTAG chain in the Apollo S10 board. Both the FMC+ and FMC connectors will not be included in the JTAG chain if the switches are set to ON position (See **Figure 2-5**).**Table 2-2** lists the setting of the SW4.

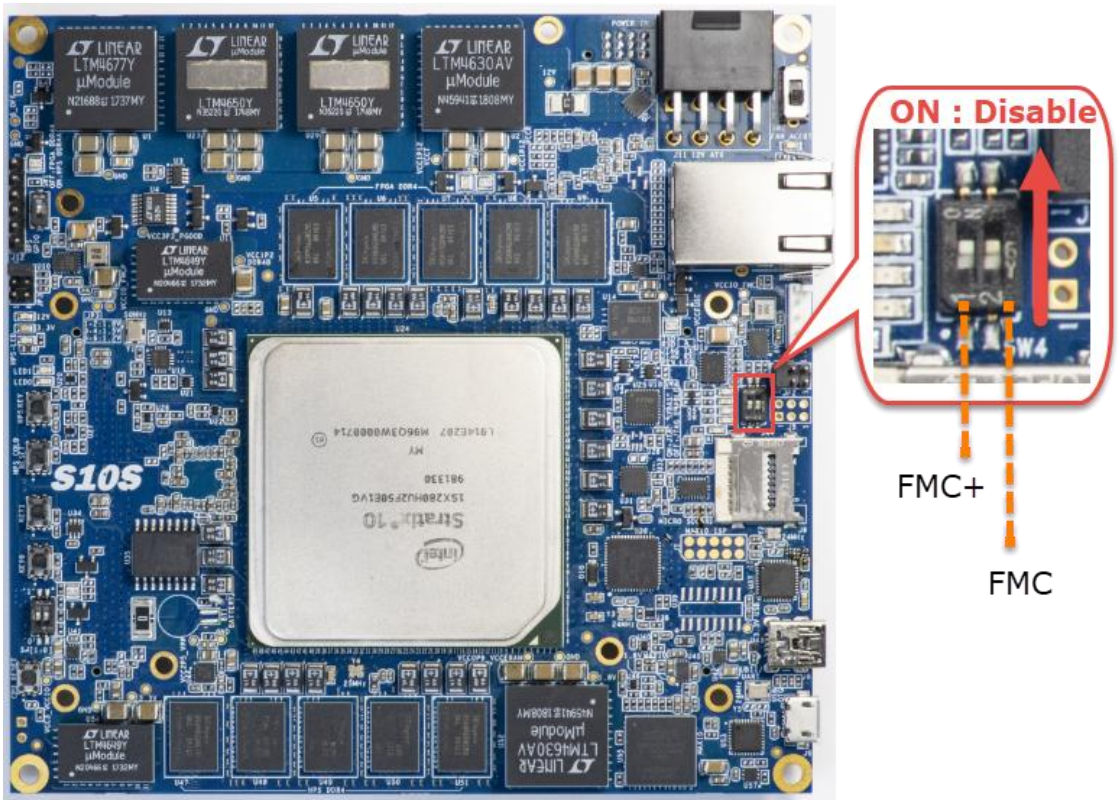


Figure 2-5 Position of slide switches SW4

Table 2-2 SW4 setting

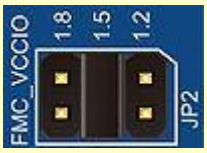
Board Reference	Signal Name	Description	Default
SW4.1	FMCP_JTAG_BYPASS_n	**ON** : **Disable** the JTAG interface of the FMC+ connector into the JTAG chain **OFF**: **Enable** the JTAG interface of the FMC+ connector into the JTAG chain	ON
SW4.2	FMC_JTAG_BYPASS_n	**ON** : **Disable** the JTAG interface of the FMC connector into the JTAG chain **OFF**: **Enable** the JTAG interface of the FMC connector into the JTAG chain	ON

■ FMC_VCCIO and FMCP_VCCIO Select Header

The FMC and FMC + connector I / O standard on the Apollo S10 can be set to three voltages: 1.8V, 1.5V and 1.2V. Users can set the desired voltage of FMC and FMC + by setting JP2 and JP3 respectively. The JP2 and JP3 can change the VCCIO voltage of FPGA I/O on FMC and FMC+ connector. **Figure 2-6** shows the position of the JP2 and JP3. **Table 2-3** list the FMC_VCCIO Headers (JP2) setting for FMC connector. **Table 2-4** shows the setting of the JP3 for FMC+ connector.

Figure 2-6 FMC and FMC+ I/O standard setting headers

Table 2-3 JP2 Setting for FMC I/O standard

JP2 Setting	FMC I/O Standard
	1.2V
	1.5V
	1.8V (Default Setting)

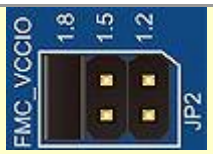
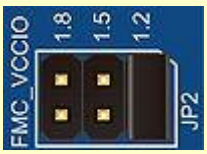
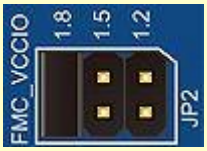
	

Table 2-4 JP3 Setting for FMC+ I/O standard

JP3 Setting	FMC I/O Standard
	1.2V
	1.5V
	1.8V (Default Setting)

2.3 General User I/O

This section describes the user I/O interface of the FPGA and HPS fabric. Please note that the HPS and FPGA portions of the device each have their own pins. Pins are not freely shared between the HPS and the FPGA fabric.

■ User Defined Push-buttons

The FPGA board includes two FPGA fabric and one HPS fabric user defined push-buttons that allow users to interact with the Stratix 10 SX device. Each push-button provides a high logic level or a low logic level when it is not pressed or pressed, respectively. **Table 2-5** lists the board references, signal names and their corresponding Stratix 10 SX device pin numbers for the push-buttons of the FPGA fabric. **Table 2-6** list the information of the push-button for the HPS fabric.

Table 2-5 Push-button (FPGA fabric) Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Stratix 10 SX Pin Number
PB0	BUTTON0	High Logic Level when the button is not pressed	3.0-V LVTTL	PIN_AE36
PB1	BUTTON1		3.0-V LVTTL	PIN_AG34
PB3	CPU_RESET_n		3.0-V LVTTL	PIN_AC35

Table 2-6 Push-button (HPS fabric) Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Stratix 10 SX Pin Number
PB6	HPS_KEY	High Logic Level when the button is not pressed	1.8-V	PIN_C28

■ User-Defined Dip Switch

There are two positions dip switch (SW0) on the FPGA fabric to provide additional FPGA input control. When a position of dip switch is in the DOWN position or the UPPER position, it provides a low logic level or a high logic level to the Stratix 10 SX FPGA, respectively.

Table 2-7 lists the signal names and their corresponding Stratix 10 SX device pin numbers.

Table 2-7 Dip Switch Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Stratix 10 SX Pin Number
SW0	SW0	High logic level when SW in the UPPER position.	3.0-V LVTTL	PIN_AG35
SW1	SW1		3.0-V LVTTL	PIN_AH33

■ User-Defined LEDs

The FPGA board consists of 2 FPGA fabric and 1 HPS fabric user-controllable LEDs to allow status and debugging signals to be driven to the LEDs from the designs loaded into the Stratix 10 SX device. Each LED is driven directly by the Stratix 10 SX FPGA. The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin names on the FPGA that are connected to the LEDs is given in **Table 2-8**. **Table 2-9** list the information of the LED for the HPS fabric.

Table 2-8 User LEDs (FPGA fabric) Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Stratix 10 SX Pin Number
LED0	LED0	Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	3.0-V LVTTL	PIN_AH32
LED1	LED1		3.0-V LVTTL	PIN_AC33

Table 2-9 User LEDs (HPS fabric) Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Stratix 10 SX Pin Number
HPS_LED	HPS_LED	Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	1.8-V	PIN_G30

2.4 Micro SD Card Socket

The board supports Micro SD card interface with x4 data lines. It serves for an external storage for the HPS fabric. Figure 2-7 shows signals connected between the HPS and Micro SD card socket. **Table 2-10** lists the pin assignment of Micro SD card socket to the HPS.

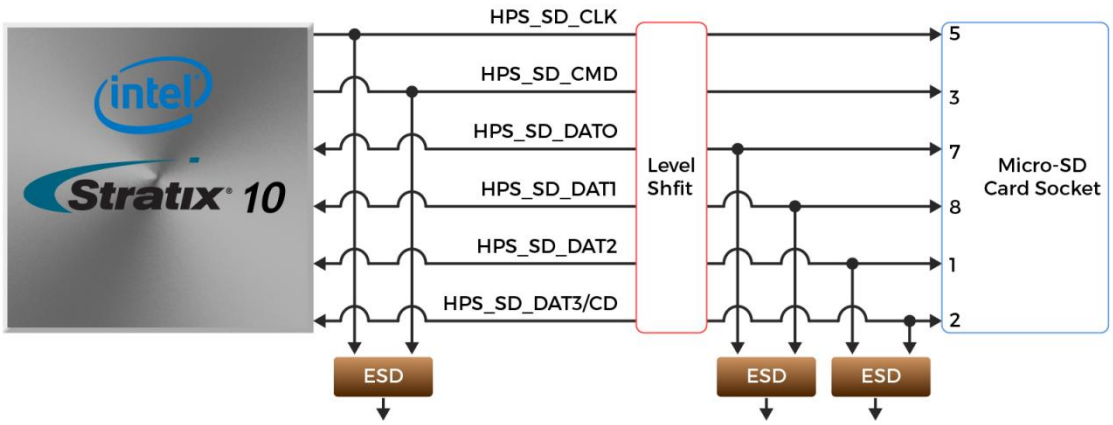


Figure 2-7 Pin-out of Micro SD Card socket

Table 2-10 Micro SD Card Socket Header Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Stratix 10 SX Pin Number
HPS_SD_CLK	HPS SD Clock	1.8-V	PIN_A31
HPS_SD_CMD	HPS SD Command Line	1.8-V	PIN_J30
HPS_SD_DATA[0]	HPS SD Data[0]	1.8-V	PIN_P30
HPS_SD_DATA[1]	HPS SD Data[1]	1.8-V	PIN_H30
HPS_SD_DATA[2]	HPS SD Data[2]	1.8-V	PIN_D31
HPS_SD_DATA[3]	HPS SD Data[3]	1.8-Vs	PIN_H32

2.5 FMC Connector

The FPGA Mezzanine Card (FMC) interface provides a mechanism to extend the peripheral-set of an FPGA host board by means of add-on daughter cards, which can address today's high-speed signaling requirements as well as low-speed device interface support. The FMC interfaces support JTAG, clock outputs and inputs, high-speed serial I/O (transceivers), and single-ended or differential signaling.

There is one FMC connector on the Apollo S10 board, it is a High Pin Count (HPC) size of connector, The HPC connector on Apollo S10 board can provides 160 user-define, single-ended signals (Not include clock, I2C and some control signals) and 10 serial transceiver pairs. **Figure 2-8** is the FPGA I/O connected to the FMC connector on the Apollo S10 board.

Below we will introduce according to the individual functions of FMC connector.

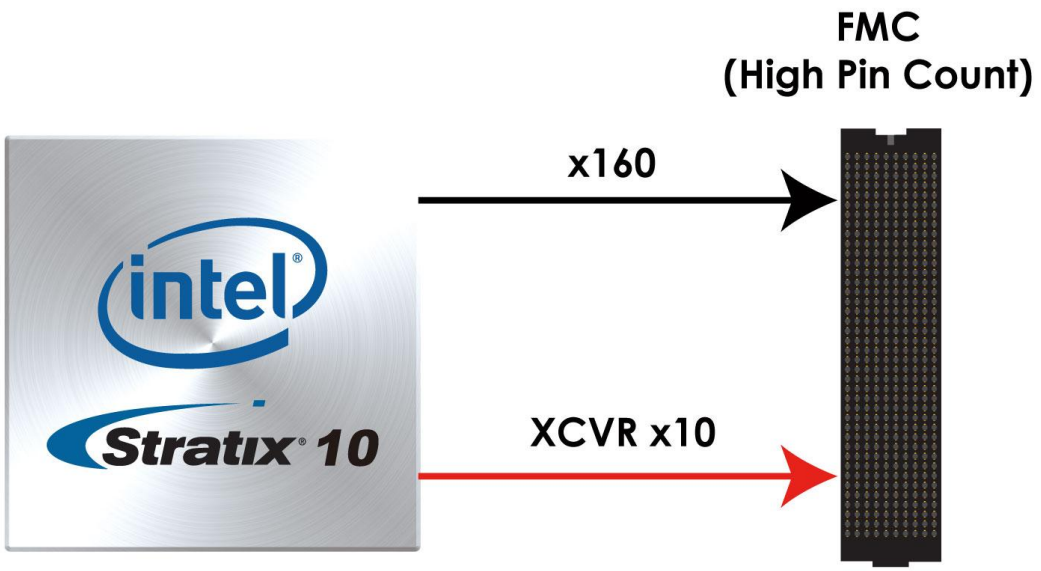


Figure 2-8 FMC connector on Apollo S10 board

- **Clock Interface**

Table 2-11 shows the FPGA dedicated clock input pin placement on the FMC connector.

Table 2-11 FMC clock interface distribution

Signal Name	FMC Clock in/out pin name	FPGA Clock Input Pin Placement	FPGA Pin Assignment
FMC_CLK_M2C_p0	CLK0_M2C_P	CLK_3L_1P	C22
FMC_CLK_M2C_n0	CLK0_M2C_N	CLK_3L_1N	C21
FMC_CLK_M2C_p1	CLK1_M2C_P	CLK_3K_1P	J16
FMC_CLK_M2C_n1	CLK1_M2C_N	CLK_3K_1N	H16
FMC_HA_p0	HA00_P_CC	CLK_3J_0P	P14
FMC_HA_n0	HA00_P_CC	CLK_3J_0N	N13
FMC_HA_p1	HA01_P_CC	CLK_3J_1P	J13
FMC_HA_n1	HA01_N_CC	CLK_3J_1N	K13
FMC_HB_p0	HB00_P_CC	CLK_3K_0P	E16
FMC_HB_n0	HB00_P_CC	CLK_3K_0N	F16

FMC_LA_p0	LA00_P_CC	CLK_3L_0P	J20
FMC_LA_p0	LA00_N_CC	CLK_3L_0N	J19

■ Power Supply

The Apollo S10 board provides 12V, 3.3V and VCCIO_FMC power through FMC ports. **Table 2-12** indicates the maximum power consumption for the FMC connector.

CAUTION: Before powering on the Apollo S10 board with a daughter card, please check to see if there is a short circuit between the power pins and FPGA I/O.

Table 2-12 Power Supply of the FMC

Supplied Voltage	Max. Current Limit
12V	1A
3.3V	3A
VCCIO_FMC	4A

■ Adjustable I/O Standards

The FPGA I/O standards of the FMC ports can be adjusted by configuring the header position. Each port can be individually adjusted to 1.2V, 1.5V or 1.8V via jumper **JP2** on the Apollo S10 board. For detailed setting, please refer to Section 2.2: **FMC_VCCIO and FMCP_VCCIO Select Header**.

■ JTAG Chain on FMC

The JTAG chain on the Apollo S10 board supports JTAG interface extension to the FMC connector so that the JTAG device on the user's FMC daughter card can be joined with JTAG chain on the Apollo S10 board. Users can enable this feature through the switch (**SW4.2**) on the Apollo S10 board. In the board's default setting, the JTAG interface of the FMC connector is bypassed to keep the Apollo S10 board JTAG chain to maintain close loop. For detailed setting, please refer to Section 2.2: **JTAG Interface Switch.**

■ Transceiver Channels Speed

There are 10 transceivers connected to the Stratix 10 FPGA on the FMC connector, two of which belong to the GX channels, and the maximum transmission speed is 17.4 Gbps. The other 8 belong to GXT channels, and the maximum transmission speed can reach 25Gbps. For details, please to see "*Intel ® Stratix® 10 L- and H-Tile Transceiver PHY User Guide*" for section "*1.3. L-Tile / H-Tile Building Blocks*". **Table 2-13** lists the distribution and speed of the two channels of the FMC connector.

Table 2-13 GX and GXT channels on the FMC connector

Transceiver channel Type	Net Name	Speed
GX Channels	FMC_DP_M2C_p2/ FMC_DP_C2M_p2 , FMC_DP_M2C_p5/ FMC_DP_C2M_p5 ,	17.4 Gbps
GXT Channels	FMC_DP_M2C_p0/ FMC_DP_C2M_p0 , FMC_DP_M2C_p1/ FMC_DP_C2M_p1 , FMC_DP_M2C_p3/ FMC_DP_C2M_p3 , FMC_DP_M2C_p4/ FMC_DP_C2M_p4 FMC_DP_M2C_p6/ FMC_DP_C2M_p6 FMC_DP_M2C_p7/ FMC_DP_C2M_p7 FMC_DP_M2C_p8/ FMC_DP_C2M_p8 FMC_DP_M2C_p9/ FMC_DP_C2M_p9	25 Gbps

■ Component Information of the FMC Connector

For information on the FMC part number used on the Apollo S10 board and the male connector connected to it, refer to **Table 1-1** in the section 1.6.

■ FPGA Pin Assignments for FMC Connector

Figure 2-9 shows the pin out table of the FMC connector on the Apollo S10 and **Table 2-14** lists the FMC connector pin assignments, signal names and functions.

	K	J	H	G	F	E	D	C	B	A
1	FMC_VREFB	GND	FMC_VREFA	GND	M2C_PG	GND	C2M_PG	GND	NC	GND
2	GND	CLK3_BIDIR_P	NC	CLK_M2C_P1	GND	HA_P1	GND	DP_C2M_P0	GND	DP_M2C_P1
3	GND	CLK3_BIDIR_N	GND	CLK_M2C_N1	GND	HA_N1	GND	DP_C2M_N0	GND	DP_M2C_N1
4	CLK2_BIDIR_P	GND	CLK_M2C_P0	GND	HA_P0	GND	GBTCLK_M2C_P0	GND	DP_M2C_P9	GND
5	CLK2_BIDIR_N	GND	CLK_M2C_N0	GND	HA_N0	GND	GBTCLK_M2C_N0	GND	DP_M2C_N9	GND
6	GND	HA_P3	GND	LA_P0	GND	HA_P5	GND	DP_M2C_P0	GND	DP_M2C_P2
7	HA_P2	HA_N3	LA_P2	LA_N0	HA_P4	HA_N5	GND	DP_M2C_N0	GND	DP_M2C_N2
8	HA_N2	GND	LA_N2	GND	HA_N4	GND	LA_P1	GND	DP_M2C_P8	GND
9	GND	HA_P7	GND	LA_P3	GND	HA_P9	LA_N1	GND	DP_M2C_N8	GND
10	HA_P6	HA_N7	LA_P4	LA_N3	HA_P8	HA_N9	GND	LA_P6	GND	DP_M2C_P3
11	HA_N6	GND	LA_N4	GND	HA_N8	GND	LA_P5	LA_N6	GND	DP_M2C_N3
12	GND	HA_P11	GND	LA_P8	GND	HA_P13	LA_N5	GND	DP_M2C_P7	GND
13	HA_P10	HA_N11	LA_P7	LA_N8	HA_P12	HA_N13	GND	GND	DP_M2C_N7	GND
14	HA_N10	GND	LA_N7	GND	HA_N12	GND	LA_P9	LA_P10	GND	DP_M2C_P4
15	GND	HA_P14	GND	LA_P12	GND	HA_P16	LA_N9	LA_N10	GND	DP_M2C_N4
16	HA_P17	HA_N14	LA_P11	LA_N12	HA_P15	HA_N16	GND	GND	DP_M2C_P6	GND
17	HA_N17	GND	LA_N11	GND	HA_N15	GND	LA_P13	GND	DP_M2C_N6	GND
18	GND	HA_P18	GND	LA_P16	GND	HA_P20	LA_N13	LA_P14	GND	DP_M2C_P5
19	HA_P21	HA_N18	LA_P15	LA_N16	HA_P19	HA_N20	GND	LA_N14	GND	DP_M2C_N5
20	HA_N21	GND	LA_N15	GND	HA_N19	GND	LA_P17	GND	GBTCLK_M2C_P1	GND
21	GND	HA_P22	GND	LA_P20	GND	HB_P3	LA_N17	GND	GBTCLK_M2C_N1	GND
22	HA_P23	HA_N22	LA_P19	LA_N20	HB_P2	HB_N3	GND	LA_P18	GND	DP_C2M_P1
23	HA_N23	GND	LA_N19	GND	HB_N2	GND	LA_P23	LA_N18	GND	DP_C2M_N1
24	GND	HB_P1	GND	LA_P22	GND	HB_P5	LA_N23	GND	DP_C2M_P9	GND
25	HB_P0	HB_N1	LA_P21	LA_N22	HB_P4	HB_N5	GND	GND	DP_C2M_N9	GND
26	HB_N0	GND	LA_N21	GND	HB_N4	GND	LA_P26	LA_P27	GND	DP_C2M_P2
27	GND	HB_P7	GND	LA_P25	GND	HB_P9	LA_N26	LA_N27	GND	DP_C2M_N2
28	HB_P6	HB_N7	LA_P24	LA_N25	HB_P8	HB_N9	GND	GND	DP_C2M_P8	GND
29	HB_N6	GND	LA_N24	GND	HB_N8	GND	JTAG_TCK	GND	DP_C2M_N8	GND
30	GND	HB_P11	GND	LA_P29	GND	HB_P13	JTAG_TDI	SCL	GND	DP_C2M_P3
31	HB_P10	HB_N11	LA_P28	LA_N29	HB_P12	HB_N13	JTAG_TDO	SDA	GND	DP_C2M_N3
32	HB_N10	GND	LA_N28	GND	HB_N12	GND	VCC3P3	GND	DP_C2M_P7	GND
33	GND	HB_P15	GND	LA_P31	GND	HB_P19	JTAG_TMS	GND	DP_C2M_N7	GND
34	HB_P14	HB_N15	LA_P30	LA_N31	HB_P16	HB_N19	JTAG_TRST	GA0	GND	DP_C2M_P4
35	HB_N14	GND	LA_N30	GND	HB_N16	GND	GA1	VCC12	GND	DP_C2M_N4
36	GND	HB_P18	GND	LA_P33	GND	HB_P21	VCC3P3	GND	DP_C2M_P6	GND
37	HB_P17	HB_N18	LA_P32	LA_N33	HB_P20	HB_N21	GND	VCC12	DP_C2M_N6	GND
38	HB_N17	GND	LA_N32	GND	HB_N20	GND	VCC3P3	GND	GND	DP_C2M_P5
39	GND	NC	GND	VCCIO_FMC	GND	VCCIO_FMC	GND	VCC3P3	GND	DP_C2M_N5
40	NC	GND	VCCIO_FMC	GND	VCCIO_FMC	GND	VCC3P3	GND	NC	GND

Figure 2-9 FMC pin out table

Table 2-14 FMC Connector Pin Assignments, Signal Names and Functions

Signal Name	FPGA Pin Number	Description	I/O Standard
FMC_CLK2_BIDIR_p	PIN_AW18	FMC data bus	FMC_VCCIO*(1)
FMC_CLK2_BIDIR_n	PIN_AV17	FMC data bus	FMC_VCCIO*(1)
FMC_CLK3_BIDIR_p	PIN_C1	FMC data bus	FMC_VCCIO*(1)
FMC_CLK3_BIDIR_n	PIN_D1	FMC data bus	FMC_VCCIO*(1)
FMC_CLK_M2C_p[0]	PIN_K5 *(2)	Clock from mezzanine module to carrier card positive 0	FMC_VCCIO*(1)
FMC_CLK_M2C_n[0]	PIN_L5*(2)	Clock from mezzanine module to carrier card negative 0	FMC_VCCIO*(1)
FMC_CLK_M2C_p[1]	PIN_AW14*(2)	Clock from mezzanine	FMC_VCCIO*(1)

		module to carrier card positive 1	
FMC_CLK_M2C_n[1]	PIN_AW15*(2)	Clock from mezzanine module to carrier card negative 1	FMC_VCCIO*(1)
FMC_HA_p[0]	PIN_K12*(3)	FMC HA bank data p0	FMC_VCCIO*(1)
FMC_HA_p[1]	PIN_M12*(2)	FMC HA bank data p1	FMC_VCCIO*(1)
FMC_HA_p[2]	PIN_D10	FMC HA bank data p2	FMC_VCCIO*(1)
FMC_HA_p[3]	PIN_E12	FMC HA bank data p3	FMC_VCCIO*(1)
FMC_HA_p[4]	PIN_H13	FMC HA bank data p4	FMC_VCCIO*(1)
FMC_HA_p[5]	PIN_J11	FMC HA bank data p5	FMC_VCCIO*(1)
FMC_HA_p[6]	PIN_N13	FMC HA bank data p6	FMC_VCCIO*(1)
FMC_HA_p[7]	PIN_L13	FMC HA bank data p7	FMC_VCCIO*(1)
FMC_HA_p[8]	PIN_J14	FMC HA bank data p8	FMC_VCCIO*(1)
FMC_HA_p[9]	PIN_F13	FMC HA bank data p9	FMC_VCCIO*(1)
FMC_HA_p[10]	PIN_D13	FMC HA bank data p10	FMC_VCCIO*(1)
FMC_HA_p[11]	PIN_G14	FMC HA bank data p11	FMC_VCCIO*(1)
FMC_HA_p[12]	PIN_A10	FMC HA bank data p12	FMC_VCCIO*(1)
FMC_HA_p[13]	PIN_G12	FMC HA bank data p13	FMC_VCCIO*(1)
FMC_HA_p[14]	PIN_A12	FMC HA bank data p14	FMC_VCCIO*(1)
FMC_HA_p[15]	PIN_A7	FMC HA bank data p15	FMC_VCCIO*(1)
FMC_HA_p[16]	PIN_A9	FMC HA bank data p16	FMC_VCCIO*(1)
FMC_HA_p[17]	PIN_C12*(3)	FMC HA bank data p17	FMC_VCCIO*(1)
FMC_HA_p[18]	PIN_B11	FMC HA bank data p18	FMC_VCCIO*(1)
FMC_HA_p[19]	PIN_M7	FMC HA bank data p19	FMC_VCCIO*(1)
FMC_HA_p[20]	PIN_F10	FMC HA bank data p20	FMC_VCCIO*(1)
FMC_HA_p[21]	PIN_C9	FMC HA bank data p21	FMC_VCCIO*(1)
FMC_HA_p[22]	PIN_C8	FMC HA bank data p22	FMC_VCCIO*(1)
FMC_HA_p[23]	PIN_G11	FMC HA bank data p23	FMC_VCCIO*(1)

FMC_HA_n[0]	PIN_L12*(3)	FMC HA bank data n0	FMC_VCCIO*(1)
FMC_HA_n[1]	PIN_N12*(2)	FMC HA bank data n1	FMC_VCCIO*(1)
FMC_HA_n[2]	PIN_E10	FMC HA bank data n2	FMC_VCCIO*(1)
FMC_HA_n[3]	PIN_F12	FMC HA bank data n3	FMC_VCCIO*(1)
FMC_HA_n[4]	PIN_J13	FMC HA bank data n4	FMC_VCCIO*(1)
FMC_HA_n[5]	PIN_K11	FMC HA bank data n5	FMC_VCCIO*(1)
FMC_HA_n[6]	PIN_P13	FMC HA bank data n6	FMC_VCCIO*(1)
FMC_HA_n[7]	PIN_L14	FMC HA bank data n7	FMC_VCCIO*(1)
FMC_HA_n[8]	PIN_K13	FMC HA bank data n8	FMC_VCCIO*(1)
FMC_HA_n[9]	PIN_F14	FMC HA bank data n9	FMC_VCCIO*(1)
FMC_HA_n[10]	PIN_E13	FMC HA bank data n10	FMC_VCCIO*(1)
FMC_HA_n[11]	PIN_H14	FMC HA bank data n11	FMC_VCCIO*(1)
FMC_HA_n[12]	PIN_B10	FMC HA bank data n12	FMC_VCCIO*(1)
FMC_HA_n[13]	PIN_H12	FMC HA bank data n13	FMC_VCCIO*(1)
FMC_HA_n[14]	PIN_B12	FMC HA bank data n14	FMC_VCCIO*(1)
FMC_HA_n[15]	PIN_A8	FMC HA bank data n15	FMC_VCCIO*(1)
FMC_HA_n[16]	PIN_B9	FMC HA bank data n16	FMC_VCCIO*(1)
FMC_HA_n[17]	PIN_C13*(3)	FMC HA bank data n17	FMC_VCCIO*(1)
FMC_HA_n[18]	PIN_C11	FMC HA bank data n18	FMC_VCCIO*(1)
FMC_HA_n[19]	PIN_N7	FMC HA bank data n19	FMC_VCCIO*(1)
FMC_HA_n[20]	PIN_G10	FMC HA bank data n20	FMC_VCCIO*(1)
FMC_HA_n[21]	PIN_D9	FMC HA bank data n21	FMC_VCCIO*(1)
FMC_HA_n[22]	PIN_D8	FMC HA bank data n22	FMC_VCCIO*(1)
FMC_HA_n[23]	PIN_H11	FMC HA bank data n23	FMC_VCCIO*(1)
FMC_HB_p[0]	PIN_E1	FMC HB bank data p0	FMC_VCCIO*(1)
FMC_HB_p[1]	PIN_G4	FMC HB bank data p1	FMC_VCCIO*(1)
FMC_HB_p[2]	PIN_N8*(3)	FMC HB bank data p2	FMC_VCCIO*(1)
FMC_HB_p[3]	PIN_J4	FMC HB bank data p3	FMC_VCCIO*(1)

FMC_HB_p[4]	PIN_H2	FMC HB bank data p4	FMC_VCCIO*(1)
FMC_HB_p[5]	PIN_G5	FMC HB bank data p5	FMC_VCCIO*(1)
FMC_HB_p[6]	PIN_D3*(3)	FMC HB bank data p6	FMC_VCCIO*(1)
FMC_HB_p[7]	PIN_A2	FMC HB bank data p7	FMC_VCCIO*(1)
FMC_HB_p[8]	PIN_B1	FMC HB bank data p8	FMC_VCCIO*(1)
FMC_HB_p[9]	PIN_AT13	FMC HB bank data p9	FMC_VCCIO*(1)
FMC_HB_p[10]	PIN_AM17	FMC HB bank data p10	FMC_VCCIO*(1)
FMC_HB_p[11]	PIN_AJ16	FMC HB bank data p11	FMC_VCCIO*(1)
FMC_HB_p[12]	PIN_AW13	FMC HB bank data p12	FMC_VCCIO*(1)
FMC_HB_p[13]	PIN_AV14	FMC HB bank data p13	FMC_VCCIO*(1)
FMC_HB_p[14]	PIN_AP14	FMC HB bank data p14	FMC_VCCIO*(1)
FMC_HB_p[15]	PIN_AK16	FMC HB bank data p15	FMC_VCCIO*(1)
FMC_HB_p[16]	PIN_AU16*(3)	FMC HB bank data p16	FMC_VCCIO*(1)
FMC_HB_p[17]	PIN_AT17	FMC HB bank data p17	FMC_VCCIO*(1)
FMC_HB_p[18]	PIN_AM15	FMC HB bank data p18	FMC_VCCIO*(1)
FMC_HB_p[19]	PIN_AR15*(3)	FMC HB bank data p19	FMC_VCCIO*(1)
FMC_HB_p[20]	PIN_AP16	FMC HB bank data p20	FMC_VCCIO*(1)
FMC_HB_p[21]	PIN_AV18	FMC HB bank data p21	FMC_VCCIO*(1)
FMC_HB_n[0]	PIN_E2	FMC HB bank data n0	FMC_VCCIO*(1)
FMC_HB_n[1]	PIN_H4	FMC HB bank data n1	FMC_VCCIO*(1)
FMC_HB_n[2]	PIN_P8*(3)	FMC HB bank data n2	FMC_VCCIO*(1)
FMC_HB_n[3]	PIN_J5	FMC HB bank data n3	FMC_VCCIO*(1)
FMC_HB_n[4]	PIN_H3	FMC HB bank data n4	FMC_VCCIO*(1)
FMC_HB_n[5]	PIN_H6	FMC HB bank data n5	FMC_VCCIO*(1)
FMC_HB_n[6]	PIN_E3*(3)	FMC HB bank data n6	FMC_VCCIO*(1)
FMC_HB_n[7]	PIN_B2	FMC HB bank data n7	FMC_VCCIO*(1)
FMC_HB_n[8]	PIN_C2	FMC HB bank data n8	FMC_VCCIO*(1)
FMC_HB_n[9]	PIN_AT14	FMC HB bank data n9	FMC_VCCIO*(1)

FMC_HB_n[10]	PIN_AL17	FMC HB bank data n10	FMC_VCCIO*(1)
FMC_HB_n[11]	PIN_AH16	FMC HB bank data n11	FMC_VCCIO*(1)
FMC_HB_n[12]	PIN_AV13	FMC HB bank data n12	FMC_VCCIO*(1)
FMC_HB_n[13]	PIN_AU14	FMC HB bank data n13	FMC_VCCIO*(1)
FMC_HB_n[14]	PIN_AP15	FMC HB bank data n14	FMC_VCCIO*(1)
FMC_HB_n[15]	PIN_AK17	FMC HB bank data n15	FMC_VCCIO*(1)
FMC_HB_n[16]	PIN_AU17*(3)	FMC HB bank data n16	FMC_VCCIO*(1)
FMC_HB_n[17]	PIN_AT18	FMC HB bank data n17	FMC_VCCIO*(1)
FMC_HB_n[18]	PIN_AM16	FMC HB bank data n18	FMC_VCCIO*(1)
FMC_HB_n[19]	PIN_AR16*(3)	FMC HB bank data n19	FMC_VCCIO*(1)
FMC_HB_n[20]	PIN_AN16	FMC HB bank data n20	FMC_VCCIO*(1)
FMC_HB_n[21]	PIN_AV19	FMC HB bank data n21	FMC_VCCIO*(1)
FMC_LA_p[0]	PIN_A3*(2)	FMC LA bank data p0	FMC_VCCIO*(1)
FMC_LA_p[1]	PIN_B4*(3)	FMC LA bank data p1	FMC_VCCIO*(1)
FMC_LA_p[2]	PIN_T9	FMC LA bank data p2	FMC_VCCIO*(1)
FMC_LA_p[3]	PIN_M10	FMC LA bank data p3	FMC_VCCIO*(1)
FMC_LA_p[4]	PIN_U9	FMC LA bank data p4	FMC_VCCIO*(1)
FMC_LA_p[5]	PIN_J10	FMC LA bank data p5	FMC_VCCIO*(1)
FMC_LA_p[6]	PIN_H8	FMC LA bank data p6	FMC_VCCIO*(1)
FMC_LA_p[7]	PIN_L9	FMC LA bank data p7	FMC_VCCIO*(1)
FMC_LA_p[8]	PIN_M9	FMC LA bank data p8	FMC_VCCIO*(1)
FMC_LA_p[9]	PIN_G6	FMC LA bank data p9	FMC_VCCIO*(1)
FMC_LA_p[10]	PIN_E8	FMC LA bank data p10	FMC_VCCIO*(1)
FMC_LA_p[11]	PIN_B6	FMC LA bank data p11	FMC_VCCIO*(1)
FMC_LA_p[12]	PIN_A5	FMC LA bank data p12	FMC_VCCIO*(1)
FMC_LA_p[13]	PIN_D5	FMC LA bank data p13	FMC_VCCIO*(1)
FMC_LA_p[14]	PIN_B7	FMC LA bank data p14	FMC_VCCIO*(1)
FMC_LA_p[15]	PIN_E6	FMC LA bank data p15	FMC_VCCIO*(1)

FMC_LA_p[16]	PIN_E5	FMC LA bank data p16	FMC_VCCIO*(1)
FMC_LA_p[17]	PIN_F9*(3)	FMC LA bank data p17	FMC_VCCIO*(1)
FMC_LA_p[18]	PIN_K8*(2)	FMC LA bank data p18	FMC_VCCIO*(1)
FMC_LA_p[19]	PIN_R8	FMC LA bank data p19	FMC_VCCIO*(1)
FMC_LA_p[20]	PIN_F7	FMC LA bank data p20	FMC_VCCIO*(1)
FMC_LA_p[21]	PIN_C4	FMC LA bank data p21	FMC_VCCIO*(1)
FMC_LA_p[22]	PIN_U11	FMC LA bank data p22	FMC_VCCIO*(1)
FMC_LA_p[23]	PIN_V11	FMC LA bank data p23	FMC_VCCIO*(1)
FMC_LA_p[24]	PIN_R11	FMC LA bank data p24	FMC_VCCIO*(1)
FMC_LA_p[25]	PIN_F2	FMC LA bank data p25	FMC_VCCIO*(1)
FMC_LA_p[26]	PIN_R7	FMC LA bank data p26	FMC_VCCIO*(1)
FMC_LA_p[27]	PIN_T12	FMC LA bank data p27	FMC_VCCIO*(1)
FMC_LA_p[28]	PIN_J6	FMC LA bank data p28	FMC_VCCIO*(1)
FMC_LA_p[29]	PIN_G1	FMC LA bank data p29	FMC_VCCIO*(1)
FMC_LA_p[30]	PIN_K7	FMC LA bank data p30	FMC_VCCIO*(1)
FMC_LA_p[31]	PIN_P10	FMC LA bank data p31	FMC_VCCIO*(1)
FMC_LA_p[32]	PIN_M6	FMC LA bank data p32	FMC_VCCIO*(1)
FMC_LA_p[33]	PIN_N11	FMC LA bank data p33	FMC_VCCIO*(1)
FMC_LA_n[0]	PIN_A4*(2)	FMC LA bank data n0	FMC_VCCIO*(1)
FMC_LA_n[1]	PIN_C3*(3)	FMC LA bank data n1	FMC_VCCIO*(1)
FMC_LA_n[2]	PIN_T10	FMC LA bank data n2	FMC_VCCIO*(1)
FMC_LA_n[3]	PIN_M11	FMC LA bank data n3	FMC_VCCIO*(1)
FMC_LA_n[4]	PIN_U10	FMC LA bank data n4	FMC_VCCIO*(1)
FMC_LA_n[5]	PIN_K10	FMC LA bank data n5	FMC_VCCIO*(1)
FMC_LA_n[6]	PIN_J8	FMC LA bank data n6	FMC_VCCIO*(1)
FMC_LA_n[7]	PIN_L10	FMC LA bank data n7	FMC_VCCIO*(1)
FMC_LA_n[8]	PIN_N9	FMC LA bank data n8	FMC_VCCIO*(1)
FMC_LA_n[9]	PIN_H7	FMC LA bank data n9	FMC_VCCIO*(1)

FMC_LA_n[10]	PIN_F8	FMC LA bank data n10	FMC_VCCIO*(1)
FMC_LA_n[11]	PIN_C6	FMC LA bank data n11	FMC_VCCIO*(1)
FMC_LA_n[12]	PIN_B5	FMC LA bank data n12	FMC_VCCIO*(1)
FMC_LA_n[13]	PIN_D6	FMC LA bank data n13	FMC_VCCIO*(1)
FMC_LA_n[14]	PIN_C7	FMC LA bank data n14	FMC_VCCIO*(1)
FMC_LA_n[15]	PIN_E7	FMC LA bank data n15	FMC_VCCIO*(1)
FMC_LA_n[16]	PIN_F5	FMC LA bank data n16	FMC_VCCIO*(1)
FMC_LA_n[17]	PIN_G9*(3)	FMC LA bank data n17	FMC_VCCIO*(1)
FMC_LA_n[18]	PIN_L8*(2)	FMC LA bank data n18	FMC_VCCIO*(1)
FMC_LA_n[19]	PIN_P9	FMC LA bank data n19	FMC_VCCIO*(1)
FMC_LA_n[20]	PIN_G7	FMC LA bank data n20	FMC_VCCIO*(1)
FMC_LA_n[21]	PIN_D4	FMC LA bank data n21	FMC_VCCIO*(1)
FMC_LA_n[22]	PIN_U12	FMC LA bank data n22	FMC_VCCIO*(1)
FMC_LA_n[23]	PIN_V12	FMC LA bank data n23	FMC_VCCIO*(1)
FMC_LA_n[24]	PIN_R12	FMC LA bank data n24	FMC_VCCIO*(1)
FMC_LA_n[25]	PIN_G2	FMC LA bank data n25	FMC_VCCIO*(1)
FMC_LA_n[26]	PIN_T8	FMC LA bank data n26	FMC_VCCIO*(1)
FMC_LA_n[27]	PIN_T13	FMC LA bank data n27	FMC_VCCIO*(1)
FMC_LA_n[28]	PIN_K6	FMC LA bank data n28	FMC_VCCIO*(1)
FMC_LA_n[29]	PIN_H1	FMC LA bank data n29	FMC_VCCIO*(1)
FMC_LA_n[30]	PIN_L7	FMC LA bank data n30	FMC_VCCIO*(1)
FMC_LA_n[31]	PIN_R10	FMC LA bank data n31	FMC_VCCIO*(1)
FMC_LA_n[32]	PIN_N6	FMC LA bank data n32	FMC_VCCIO*(1)
FMC_LA_n[33]	PIN_P11	FMC LA bank data n33	FMC_VCCIO*(1)
FMC_GBTCLK_M2C_p[0]	PIN_P31	LVDS input from the installed FMC card to dedicated reference clock inputs	LVDS
FMC_GBTCLK_M2C_p[1]	PIN_K31	LVDS input from the	LVDS

		installed FMC card to dedicated reference clock inputs	
FMC_REFCLK_p	PIN_T31	FPGA transceiver Reference Clock (From on board PLL)	LVDS
FMC_DP_C2M_p[0]	PIN_M39	Transmit pair p0 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_C2M_p[1]	PIN_L37	Transmit pair p1 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_C2M_p[2]	PIN_K39	Transmit pair p2 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_C2M_p[3]	PIN_J37	Transmit pair p3 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_C2M_p[4]	PIN_H39	Transmit pair p4 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_C2M_p[5]	PIN_G37	Transmit pair p5 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_C2M_p[6]	PIN_F39	Transmit pair p6 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_C2M_p[7]	PIN_E37	Transmit pair p7 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_C2M_p[8]	PIN_D39	Transmit pair p8 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_C2M_p[9]	PIN_C37	Transmit pair p9 of the FPGA	HSSI

		transceiver	DIFFERENTIAL I/O
FMC_DP_M2C_p[0]	PIN_P35	Receiver pair p0 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_M2C_p[1]	PIN_R33	Receiver pair p1 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_M2C_p[2]	PIN_M35	Receiver pair p2 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_M2C_p[3]	PIN_N33	Receiver pair p3 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_M2C_p[4]	PIN_K35	Receiver pair p4 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_M2C_p[5]	PIN_L33	Receiver pair p5 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_M2C_p[6]	PIN_H35	Receiver pair p6 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_M2C_p[7]	PIN_J33	Receiver pair p7 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_M2C_p[8]	PIN_F35	Receiver pair p8 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_DP_M2C_p[9]	PIN_G33	Receiver pair p9 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMC_GA[0]	PIN_E11	FMC geographical address 0	3.3 V*(2)

FMC_GA[1]	PIN_AL18	FMC geographical address 1	3.3 V*(2)
FMC_SCL	PIN_J9	Management serial clock line	3.3 V*(2)
FMC_SDA	PIN_F4	Management serial data line	3.3 V*(2)

- *(1): The FMC_VCCIO value depends on the setting of JP2, which can adjust the FMC_VCCIO to **1.2V, 1.5V or 1.8V**. Please refer to section 2.2 : "*FMC_VCCIO and FMCP_VCCIO Select Header*" for details.
- *(2): There are level shift ICs that convert FMC_VCCIO to 3.3V between the FPGA pins and the FMC pins.

2.6 FMC+ Connector

In addition to an FMC connector on the Apollo S10 board, there is also an FMC + connector for expanding FPGA I/Os (See Figure). FMC+ is the latest Standard in the popular VITA FMC family. The main difference between FMC + and FMC specifications is that the number of FMC + transceiver can provide up to 24 pairs (High Serial Pin Count version, HSPC).

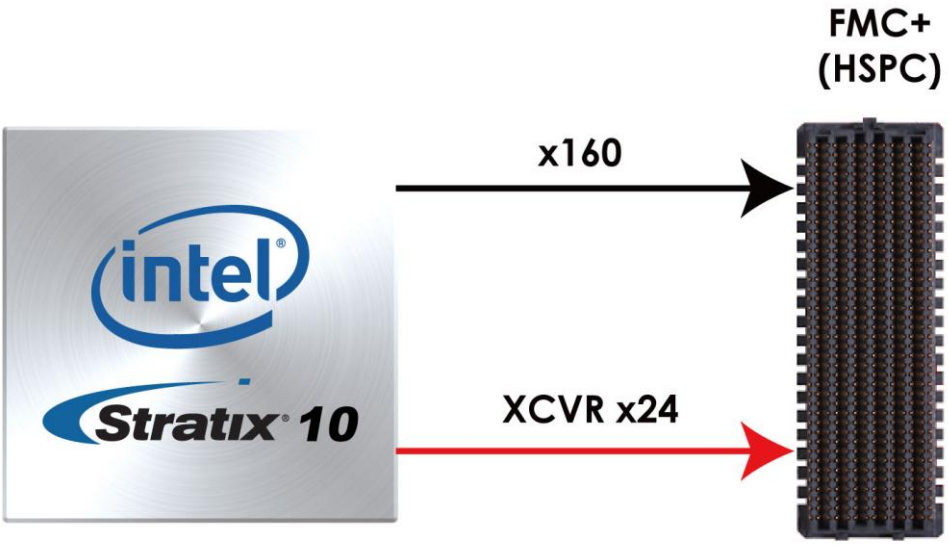


Figure 2-10 FMC+ connector on Apollo S10 board

As the number of transceivers increases, the connector size of the FMC+ becomes a

14x40 array, compared to the 10x40 array of the FMC.

Below we will introduce according to the individual functions of FMC+ connector.

■ Compare the FMC and FMC+

Table 2-15 lists the number of I/O, power, transceiver, clock and other interfaces provided by FMC and FMC + connector on the Apollo-S10 board.

Table 2-15 FMC and FMC+ compare list on the Apollo S10 board

Parameter	FMC (J2)	FMC+(J1)
Number of DIFF/SE I/O	80 DIFF/160 SE	80 DIFF/160 SE
M2C Clocks (DIFF)	2	2
SYNC M2C+C2M (DIFF)	-	1+1
REFCLK M2C+C2M (DIFF)	-	1+1
Gigabit Transceivers	10	24
Gigabit reference clocks	2	6
Miscellaneous	JTAG, SYNC, Power Good, Geographic Address	JTAG, SYNC, Power Good, Geographic Address
Power supplies	VADJ(4 pins), 3V3(4 pins), 12V (2 pins), 3V3 Aux (1 pin)	VADJ(4 pins), 3V3(4 pins), 12V (2 pins), 3V3 Aux (1 pin)

■ Clock Interface

Table 2-16 shows the FPGA dedicated clock input pin placement on the FMC+ connector.

Table 2-16 FMCP clock input interface distribution

Signal Name	FMC Clock in/out pin name	FPGA Clock Input Pin Placement	FPGA Pin Assignment
FMCP_CLK_M2C_p0	CLK0_M2C_P	CLK_2C_1P	BH36
FMCP_CLK_M2C_n0	CLK0_M2C_N	CLK_2C_1N	BH37
FMCP_CLK_M2C_p1	CLK1_M2C_P	CLK_2B_0P	AW36

FMCP_CLK_M2C_n1	CLK1_M2C_N	CLK_2B_0N	AV36
FMCP_HA_p0	HA00_P_CC	CLK_2A_0P	BE31
FMCP_HA_n0	HA00_P_CC	CLK_2A_0N	BD31
FMCP_HA_p1	HA01_P_CC	CLK_2A_1P	AW30
FMCP_HA_n1	HA01_N_CC	CLK_2A_1N	AV36
FMCP_HB_p0	HB00_P_CC	CLK_2F_1P	AN27
FMCP_HB_n0	HB00_P_CC	CLK_2F_1N	AN28
FMCP_LA_p0	LA00_P_CC	CLK_2C_0P	AW38
FMCP_LA_p0	LA00_N_CC	CLK_2C_0N	AW39
FMCP_REFCLK_M2C_p	REFCLK_M2C_P	CLK_2B_1P	BH33
FMCP_REFCLK_M2C_n	REFCLK_M2C_N	CLK_2B_1N	BG33

■ Power Supply

The Apollo S10 board provides 12V, 3.3V and VCCIO_FMCP power through FMC+ port.**Table 2-17** indicates the maximum power consumption for the FMC+ connector.

CAUTION: Before powering on the Apollo S10 board with a daughter card, please check to see if there is a short circuit between the power pins and FPGA I/O.

Table 2-17 Power Supply of the FMC

Supplied Voltage	Max. Current Limit
12V	1A
3.3V	3A
VCCIO_FMCP	4A

■ Adjustable I/O Standards

The FPGA I/O standards of the FMC+ ports can be adjusted by configuring the header position. Each port can be individually adjusted to 1.2V, 1.5V or 1.8V via jumper **JP3** on the Apollo S10 board. For detailed setting, please refer to Section 2.2: **FMC_VCCIO and FMCP_VCCIO Select Header**.

■ JTAG Chain on FMC

The JTAG chain on the Apollo S10 board supports JTAG interface extension to the FMC+ connector so that the JTAG device on the user's FMC+ daughter card can be joined with JTAG chain on the Apollo S10 board. Users can enable this feature through the switch (**SW4.1**) on the Apollo S10 board. In the board's default setting, the JTAG interface of the FMC connector is bypassed to keep the Apollo S10 board JTAG chain to maintain close loop. For detailed setting, please refer to Section 2.2: **JTAG Interface Switch.**

■ Transceiver Channels Speed

There are **24** transceivers connected to the Stratix 10 FPGA on the FMCP connector, **5** of which belong to the GX channels, and the maximum transmission speed is 17.4 Gbps. The other 19 belong to GXT channels, and the maximum transmission speed can reach 25Gbps. For details, please to see "*Intel ® Stratix® 10 L- and H-Tile Transceiver PHY User Guide*" for section "*1.3. L-Tile / H-Tile Building Blocks*". **Table 2-18** lists the distribution and speed of the two channels of the FMCP connector.

Table 2-18 GX and GXT channels on the FMCP connector

Transceiver channel Type	Net Name	Speed
GX Channels	FMCP_DP_M2C_p2/ FMCP_DP_C2M_p2 , FMCP_DP_M2C_p5/ FMCP_DP_C2M_p5 , FMCP_DP_M2C_p8/ FMCP_DP_C2M_p8 , FMCP_DP_M2C_p11/ FMCP_DP_C2M_p11 , FMCP_DP_M2C_p14/ FMCP_DP_C2M_p14	17.4 Gbps
GXT Channels	FMC_DP_M2C_p0/ FMC_DP_C2M_p0 , FMC_DP_M2C_p1/ FMC_DP_C2M_p1 , FMC_DP_M2C_p3/ FMC_DP_C2M_p3 , FMC_DP_M2C_p4/ FMC_DP_C2M_p4, FMC_DP_M2C_p6/ FMC_DP_C2M_p6, FMC_DP_M2C_p7/ FMC_DP_C2M_p7, FMC_DP_M2C_p9/ FMC_DP_C2M_p9, FMC_DP_M2C_p10/ FMC_DP_C2M_p10 , FMC_DP_M2C_p12/ FMC_DP_C2M_p12 , FMC_DP_M2C_p13/ FMC_DP_C2M_p13 ,	25 Gbps

	FMC_DP_M2C_p15/ FMC_DP_C2M_p15, FMC_DP_M2C_p16/ FMC_DP_C2M_p16, FMC_DP_M2C_p17/ FMC_DP_C2M_p17, FMC_DP_M2C_p18/ FMC_DP_C2M_p18, FMC_DP_M2C_p19/ FMC_DP_C2M_p19, FMC_DP_M2C_p20/ FMC_DP_C2M_p20 , FMC_DP_M2C_p21/ FMC_DP_C2M_p21 , FMC_DP_M2C_p22/ FMC_DP_C2M_p22 , FMC_DP_M2C_p23/ FMC_DP_C2M_p23	

■ FPGA Pin Assignments for FMCP Connector

Figure 2-11 shows the pin out table of the FMC connector on the Apollo S10 and **Table 2-19** lists the FMC connector pin assignments, signal names and function.

	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	FMC_VREFB	GND	FMC_VREFA	GND	M2C_PG	GND	C2M_PG	GND	GND	GND	FMCP_PRSNT_M2C_L	GND
2	DP_M2C_P23	GND	GND	CLK3_BIDIR_P	FMCP_PRSNT_M2C_L	CLK_M2C_P1	GND	HA_P1	GND	DP_C2M_P0	GND	DP_M2C_P1	GND	DP_C2M_P23
3	DP_M2C_P23	GND	GND	CLK3_BIDIR_N	GND	CLK_M2C_N1	GND	HA_N1	GND	DP_C2M_N0	GND	DP_M2C_N1	GND	DP_C2M_N23
4	GND	GBTCLK_M2C_P4	CLK2_BIDIR_P	GND	CLK_M2C_P0	GND	HA_P0	GND	GBTCLK_M2C_P0	GND	DP_M2C_P9	GND	DP_C2M_P22	GND
5	GND	GBTCLK_M2C_N4	CLK2_BIDIR_N	GND	CLK_M2C_N0	GND	HA_N0	GND	GBTCLK_M2C_N0	GND	DP_M2C_N9	GND	DP_C2M_N22	GND
6	DP_M2C_P22	GND	GND	HA_P3	GND	LA_P0	GND	HA_P5	GND	DP_M2C_P0	GND	DP_M2C_P2	GND	DP_C2M_P21
7	DP_M2C_P22	GND	HA_P2	HA_N3	LA_P2	LA_N0	HA_P4	HA_N5	GND	DP_M2C_N0	GND	DP_M2C_N2	GND	DP_C2M_N21
8	GND	GBTCLK_M2C_P3	HA_N2	GND	LA_N2	GND	HA_N4	GND	LA_P1	GND	DP_M2C_P8	GND	DP_C2M_P20	GND
9	GND	GBTCLK_M2C_N3	GND	HA_P7	GND	LA_P3	GND	HA_P9	LA_N1	GND	DP_M2C_N8	GND	DP_C2M_N20	GND
10	DP_M2C_P21	GND	HA_P6	HA_N7	LA_P4	LA_N3	HA_P8	HA_N9	GND	LA_P6	GND	DP_M2C_P3	GND	DP_M2C_P10
11	DP_M2C_P21	GND	HA_N6	GND	LA_N4	GND	HA_N8	GND	LA_P5	LA_N6	GND	DP_M2C_N3	GND	DP_M2C_N10
12	GND	GBTCLK_M2C_P2	GND	HA_P11	GND	LA_P8	GND	HA_P13	LA_N5	GND	DP_M2C_P7	GND	DP_M2C_P11	GND
13	GND	GBTCLK_M2C_N2	HA_P10	HA_N11	LA_P7	LA_N8	HA_P12	HA_N13	GND	GND	DP_M2C_N7	GND	DP_M2C_N11	GND
14	DP_M2C_P20	GND	HA_N10	GND	LA_N7	GND	HA_N12	GND	LA_P9	LA_P10	GND	DP_M2C_P4	GND	DP12_M2C_P
15	DP_M2C_N20	GND	GND	HA_P14	GND	LA_P12	GND	HA_P16	LA_N9	LA_N10	GND	DP_M2C_N4	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA_P17	HA_N14	LA_P11	LA_N12	HA_P15	HA_N16	GND	GND	DP_M2C_P6	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA_N17	GND	LA_N11	GND	HA_N15	GND	LA_P13	GND	DP_M2C_N6	GND	DP13_M2C_N	GND
18	DP_C2M_P14	GND	GND	HA_P18	GND	LA_P16	GND	HA_P20	LA_N13	LA_P14	GND	DP_M2C_P5	GND	DP14_M2C_P
19	DP_C2M_N14	GND	HA_P21	HA_N18	LA_P15	LA_N16	HA_P19	HA_N20	GND	LA_N14	GND	DP_M2C_N5	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA_N21	GND	LA_N15	GND	HA_N19	GND	LA_P17	GND	GBTCLK_M2C_P1	GND	NC	GND
21	GND	REFCLK_C2M_N	GND	HA_P22	GND	LA_P20	GND	HB_P3	LA_N17	GND	GBTCLK_M2C_N1	GND	NC	GND
22	DP_C2M_P15	GND	HA_P23	HA_N22	LA_P19	LA_N20	HB_P2	HB_N3	GND	LA_P18	GND	DP_C2M_P1	GND	DP15_M2C_P
23	DP_C2M_N15	GND	HA_N23	GND	LA_N19	GND	HB_N2	GND	LA_P23	LA_N18	GND	DP_C2M_N1	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB_P1	GND	LA_P22	GND	HB_P5	LA_N23	GND	DP_C2M_P9	GND	DP_C2M_P10	GND
25	GND	REFCLK_M2C_N	HB_P0	HB_N1	LA_P21	LA_N22	HB_P4	HB_N5	GND	GND	DP_C2M_N9	GND	DP_C2M_N10	GND
26	DP_C2M_P16	GND	HB_N0	GND	LA_N21	GND	HB_N4	GND	LA_P26	LA_P27	GND	DP_C2M_P2	GND	DP_C2M_P11
27	DP_C2M_N16	GND	GND	HB_P7	GND	LA_P25	GND	HB_P9	LA_N26	LA_N27	GND	DP_C2M_N2	GND	DP_C2M_N11
28	GND	SYNC_M2C_P	HB_P6	HB_N7	LA_P24	LA_N25	HB_P8	HB_N9	GND	GND	DP_C2M_P8	GND	DP_C2M_P12	GND
29	GND	SYNC_M2C_N	HB_N6	GND	LA_N24	GND	HB_N8	GND	JTAG_TCK	GND	DP_C2M_N8	GND	DP_C2M_N12	GND
30	DP_C2M_P17	GND	GND	HB_P11	GND	LA_P29	GND	HB_P13	JTAG_TDI	SCL	GND	DP_C2M_P3	GND	DP_C2M_P13
31	DP_C2M_N17	GND	HB_P10	HB_N11	LA_P28	LA_N29	HB_P12	HB_N13	JTAG_TDO	SDA	GND	DP_C2M_N3	GND	DP_C2M_N13
32	GND	GND	HB_N10	GND	LA_N28	GND	HB_N12	GND	VCC3P3	GND	DP_C2M_P7	GND	DP_M2C_P16	GND
33	GND	GND	GND	HB_P15	GND	LA_P31	GND	HB_P19	JTAG_TMS	GND	DP_C2M_N7	GND	DP_M2C_N16	GND
34	DP_C2M_P18	GND	HB_P14	HB_N15	LA_P30	LA_N31	HB_P16	HB_N19	JTAG_TRST	GA0	GND	DP_C2M_P4	GND	DP_M2C_P17
35	DP_C2M_N18	GND	HB_N14	GND	LA_N30	GND	HB_N16	GND	GA1	VCC12	GND	DP_C2M_N4	GND	DP_M2C_N17
36	GND	12P0V	GND	HB_P18	GND	LA_P33	GND	HB_P21	VCC3P3	GND	DP_C2M_P6	GND	DP_M2C_P18	GND
37	GND	12P0V	HB_P17	HB_N18	LA_P32	LA_N33	HB_P20	HB_N21	GND	VCC12	DP_C2M_N6	GND	DP_M2C_N18	GND
38	DP_C2M_P19	GND	HB_N17	GND	LA_N32	GND	HB_N20	GND	VCC3P3	GND	GND	DP_C2M_P5	GND	DP_M2C_P19
39	DP_C2M_N19	GND	GND	NC	GND	VCCIO_FMC	GND	VCCIO_FMC	GND	VCC3P3	GND	DP_C2M_N5	GND	DP_M2C_N19
40	GND	12P0V	NC	GND	VCCIO_FMC	GND	VCCIO_FMC	GND	VCC3P3	GND	RES0	GND	3P3V	GND

Figure 2-11 FMC+ pin out table

Table 2-19 FMCP Connector Pin Assignments, Signal Names and Functions

Signal Name	FPGA Pin Number	Description	I/O Standard
FMCP_CLK2_BIDIR_p	PIN_AW33	FMCP data bus	FMCP_VCCIO*(1)
FMCP_CLK2_BIDIR_n	PIN_AY33	FMCP data bus	FMCP_VCCIO*(1)
FMCP_CLK3_BIDIR_p	PIN_AW34	FMCP data bus	FMCP_VCCIO*(1)
FMCP_CLK3_BIDIR_n	PIN_AW35	FMCP data bus	FMCP_VCCIO*(1)
FMCP_CLK_M2C_p[0]	PIN_ BH36 *(2)	Clock from mezzanine module to carrier card positive 0	FMCP_VCCIO*(1)
FMCP_CLK_M2C_n[0]	PIN_BH37 *(2)	Clock from mezzanine module to carrier card negative 0	FMCP_VCCIO*(1)
FMCP_CLK_M2C_p[1]	PIN_ AW36 *(2)	Clock from mezzanine module to carrier card positive 1	FMCP_VCCIO*(1)
FMCP_CLK_M2C_n[1]	PIN_AV36 *(2)	Clock from mezzanine module to carrier card negative 1	FMCP_VCCIO*(1)
FMCP_HA_p[0]	PIN_BE31	FMCP HA bank data p0	FMCP_VCCIO*(1)
FMCP_HA_p[1]	PIN_AW30	FMCP HA bank data p1	FMCP_VCCIO*(1)
FMCP_HA_p[2]	PIN_BC30	FMCP HA bank data p2	FMCP_VCCIO*(1)
FMCP_HA_p[3]	PIN_AW28	FMCP HA bank data p3	FMCP_VCCIO*(1)
FMCP_HA_p[4]	PIN_AT29	FMCP HA bank data p4	FMCP_VCCIO*(1)
FMCP_HA_p[5]	PIN_AU29	FMCP HA bank data p5	FMCP_VCCIO*(1)
FMCP_HA_p[6]	PIN_BD29	FMCP HA bank data p6	FMCP_VCCIO*(1)
FMCP_HA_p[7]	PIN_BC31	FMCP HA bank data p7	FMCP_VCCIO*(1)
FMCP_HA_p[8]	PIN_AU30	FMCP HA bank data p8	FMCP_VCCIO*(1)
FMCP_HA_p[9]	PIN_BA29	FMCP HA bank data p9	FMCP_VCCIO*(1)

FMCP_HA_p[10]	PIN_BE32	FMCP HA bank data p10	FMCP_VCCIO*(1)
FMCP_HA_p[11]	PIN_BG29	FMCP HA bank data p11	FMCP_VCCIO*(1)
FMCP_HA_p[12]	PIN_AY31	FMCP HA bank data p12	FMCP_VCCIO*(1)
FMCP_HA_p[13]	PIN_AY29	FMCP HA bank data p13	FMCP_VCCIO*(1)
FMCP_HA_p[14]	PIN_BF31	FMCP HA bank data p14	FMCP_VCCIO*(1)
FMCP_HA_p[15]	PIN_BA32	FMCP HA bank data p15	FMCP_VCCIO*(1)
FMCP_HA_p[16]	PIN_BA31	FMCP HA bank data p16	FMCP_VCCIO*(1)
FMCP_HA_p[17]	PIN_BH32	FMCP HA bank data p17	FMCP_VCCIO*(1)
FMCP_HA_p[18]	PIN_BH31	FMCP HA bank data p18	FMCP_VCCIO*(1)
FMCP_HA_p[19]	PIN_BF29	FMCP HA bank data p19	FMCP_VCCIO*(1)
FMCP_HA_p[20]	PIN_BB30	FMCP HA bank data p20	FMCP_VCCIO*(1)
FMCP_HA_p[21]	PIN_BG30	FMCP HA bank data p21	FMCP_VCCIO*(1)
FMCP_HA_p[22]	PIN_BJ30	FMCP HA bank data p22	FMCP_VCCIO*(1)
FMCP_HA_p[23]	PIN_BJ28	FMCP HA bank data p23	FMCP_VCCIO*(1)
FMCP_HA_n[0]	PIN_BD31	FMCP HA bank data n0	FMCP_VCCIO*(1)
FMCP_HA_n[1]	PIN_AW31	FMCP HA bank data n1	FMCP_VCCIO*(1)
FMCP_HA_n[2]	PIN_BD30	FMCP HA bank data n2	FMCP_VCCIO*(1)
FMCP_HA_n[3]	PIN_AV28	FMCP HA bank data n3	FMCP_VCCIO*(1)
FMCP_HA_n[4]	PIN_AT30	FMCP HA bank data n4	FMCP_VCCIO*(1)
FMCP_HA_n[5]	PIN_AU28	FMCP HA bank data n5	FMCP_VCCIO*(1)
FMCP_HA_n[6]	PIN_BE29	FMCP HA bank data n6	FMCP_VCCIO*(1)
FMCP_HA_n[7]	PIN_BC32	FMCP HA bank data n7	FMCP_VCCIO*(1)
FMCP_HA_n[8]	PIN_AV30	FMCP HA bank data n8	FMCP_VCCIO*(1)
FMCP_HA_n[9]	PIN_BB28	FMCP HA bank data n9	FMCP_VCCIO*(1)
FMCP_HA_n[10]	PIN_BF32	FMCP HA bank data n10	FMCP_VCCIO*(1)
FMCP_HA_n[11]	PIN_BG28	FMCP HA bank data n11	FMCP_VCCIO*(1)
FMCP_HA_n[12]	PIN_AY32	FMCP HA bank data n12	FMCP_VCCIO*(1)
FMCP_HA_n[13]	PIN_AW29	FMCP HA bank data n13	FMCP_VCCIO*(1)

FMCP_HA_n[14]	PIN_BF30	FMCP HA bank data n14	FMCP_VCCIO*(1)
FMCP_HA_n[15]	PIN_BB32	FMCP HA bank data n15	FMCP_VCCIO*(1)
FMCP_HA_n[16]	PIN_BA30	FMCP HA bank data n16	FMCP_VCCIO*(1)
FMCP_HA_n[17]	PIN_BG32	FMCP HA bank data n17	FMCP_VCCIO*(1)
FMCP_HA_n[18]	PIN_BJ31	FMCP HA bank data n18	FMCP_VCCIO*(1)
FMCP_HA_n[19]	PIN_BE28	FMCP HA bank data n19	FMCP_VCCIO*(1)
FMCP_HA_n[20]	PIN_BB29	FMCP HA bank data n20	FMCP_VCCIO*(1)
FMCP_HA_n[21]	PIN_BH30	FMCP HA bank data n21	FMCP_VCCIO*(1)
FMCP_HA_n[22]	PIN_BJ29	FMCP HA bank data n22	FMCP_VCCIO*(1)
FMCP_HA_n[23]	PIN_BH28	FMCP HA bank data n23	FMCP_VCCIO*(1)
FMCP_HB_p[0]	PIN_AN27	FMCP HB bank data p0	FMCP_VCCIO*(1)
FMCP_HB_p[1]	PIN_AP30	FMCP HB bank data p1	FMCP_VCCIO*(1)
FMCP_HB_p[2]	PIN_AP25	FMCP HB bank data p2	FMCP_VCCIO*(1)
FMCP_HB_p[3]	PIN_AP26	FMCP HB bank data p3	FMCP_VCCIO*(1)
FMCP_HB_p[4]	PIN_AP28	FMCP HB bank data p4	FMCP_VCCIO*(1)
FMCP_HB_p[5]	PIN_AV27	FMCP HB bank data p5	FMCP_VCCIO*(1)
FMCP_HB_p[6]	PIN_AR26	FMCP HB bank data p6	FMCP_VCCIO*(1)
FMCP_HB_p[7]	PIN_AT27	FMCP HB bank data p7	FMCP_VCCIO*(1)
FMCP_HB_p[8]	PIN_AY28	FMCP HB bank data p8	FMCP_VCCIO*(1)
FMCP_HB_p[9]	PIN_AR28	FMCP HB bank data p9	FMCP_VCCIO*(1)
FMCP_HB_p[10]	PIN_BC28	FMCP HB bank data p10	FMCP_VCCIO*(1)
FMCP_HB_p[11]	PIN_AV25	FMCP HB bank data p11	FMCP_VCCIO*(1)
FMCP_HB_p[12]	PIN_BC27	FMCP HB bank data p12	FMCP_VCCIO*(1)
FMCP_HB_p[13]	PIN_AW26	FMCP HB bank data p13	FMCP_VCCIO*(1)
FMCP_HB_p[14]	PIN_BG27	FMCP HB bank data p14	FMCP_VCCIO*(1)
FMCP_HB_p[15]	PIN_BE27	FMCP HB bank data p15	FMCP_VCCIO*(1)
FMCP_HB_p[16]	PIN_BE26	FMCP HB bank data p16	FMCP_VCCIO*(1)
FMCP_HB_p[17]	PIN_BJ25	FMCP HB bank data p17	FMCP_VCCIO*(1)

FMCP_HB_p[18]	PIN_BH26	FMCP HB bank data p18	FMCP_VCCIO*(1)
FMCP_HB_p[19]	PIN_BA25	FMCP HB bank data p19	FMCP_VCCIO*(1)
FMCP_HB_p[20]	PIN_BJ26	FMCP HB bank data p20	FMCP_VCCIO*(1)
FMCP_HB_p[21]	PIN_BC26	FMCP HB bank data p21	FMCP_VCCIO*(1)
FMCP_HB_n[0]	PIN_AN28	FMCP HB bank data n0	FMCP_VCCIO*(1)
FMCP_HB_n[1]	PIN_AP31	FMCP HB bank data n1	FMCP_VCCIO*(1)
FMCP_HB_n[2]	PIN_AN25	FMCP HB bank data n2	FMCP_VCCIO*(1)
FMCP_HB_n[3]	PIN_AN26	FMCP HB bank data n3	FMCP_VCCIO*(1)
FMCP_HB_n[4]	PIN_AP29	FMCP HB bank data n4	FMCP_VCCIO*(1)
FMCP_HB_n[5]	PIN_AV26	FMCP HB bank data n5	FMCP_VCCIO*(1)
FMCP_HB_n[6]	PIN_AT26	FMCP HB bank data n6	FMCP_VCCIO*(1)
FMCP_HB_n[7]	PIN_AU27	FMCP HB bank data n7	FMCP_VCCIO*(1)
FMCP_HB_n[8]	PIN_AY27	FMCP HB bank data n8	FMCP_VCCIO*(1)
FMCP_HB_n[9]	PIN_AR27	FMCP HB bank data n9	FMCP_VCCIO*(1)
FMCP_HB_n[10]	PIN_BD28	FMCP HB bank data n10	FMCP_VCCIO*(1)
FMCP_HB_n[11]	PIN_AW25	FMCP HB bank data n11	FMCP_VCCIO*(1)
FMCP_HB_n[12]	PIN_BB27	FMCP HB bank data n12	FMCP_VCCIO*(1)
FMCP_HB_n[13]	PIN_AY26	FMCP HB bank data n13	FMCP_VCCIO*(1)
FMCP_HB_n[14]	PIN_BF27	FMCP HB bank data n14	FMCP_VCCIO*(1)
FMCP_HB_n[15]	PIN_BF26	FMCP HB bank data n15	FMCP_VCCIO*(1)
FMCP_HB_n[16]	PIN_BD26	FMCP HB bank data n16	FMCP_VCCIO*(1)
FMCP_HB_n[17]	PIN_BH25	FMCP HB bank data n17	FMCP_VCCIO*(1)
FMCP_HB_n[18]	PIN_BG25	FMCP HB bank data n18	FMCP_VCCIO*(1)
FMCP_HB_n[19]	PIN_BB25	FMCP HB bank data n19	FMCP_VCCIO*(1)
FMCP_HB_n[20]	PIN_BH27	FMCP HB bank data n20	FMCP_VCCIO*(1)
FMCP_HB_n[21]	PIN_BC25	FMCP HB bank data n21	FMCP_VCCIO*(1)
FMCP_LA_p[0]	PIN_AW38	FMCP LA bank data p0	FMCP_VCCIO*(1)
FMCP_LA_p[1]	PIN_AP35	FMCP LA bank data p1	FMCP_VCCIO*(1)

FMCP_LA_p[2]	PIN_AN33	FMCP LA bank data p2	FMCP_VCCIO*(1)
FMCP_LA_p[3]	PIN_AP36	FMCP LA bank data p3	FMCP_VCCIO*(1)
FMCP_LA_p[4]	PIN_AT37	FMCP LA bank data p4	FMCP_VCCIO*(1)
FMCP_LA_p[5]	PIN_BB37	FMCP LA bank data p5	FMCP_VCCIO*(1)
FMCP_LA_p[6]	PIN_AT38	FMCP LA bank data p6	FMCP_VCCIO*(1)
FMCP_LA_p[7]	PIN_BB39	FMCP LA bank data p7	FMCP_VCCIO*(1)
FMCP_LA_p[8]	PIN_AP34	FMCP LA bank data p8	FMCP_VCCIO*(1)
FMCP_LA_p[9]	PIN_BA40	FMCP LA bank data p9	FMCP_VCCIO*(1)
FMCP_LA_p[10]	PIN_AW40	FMCP LA bank data p10	FMCP_VCCIO*(1)
FMCP_LA_p[11]	PIN_BD39	FMCP LA bank data p11	FMCP_VCCIO*(1)
FMCP_LA_p[12]	PIN_AU38	FMCP LA bank data p12	FMCP_VCCIO*(1)
FMCP_LA_p[13]	PIN_AV37	FMCP LA bank data p13	FMCP_VCCIO*(1)
FMCP_LA_p[14]	PIN_BB38	FMCP LA bank data p14	FMCP_VCCIO*(1)
FMCP_LA_p[15]	PIN_AY37	FMCP LA bank data p15	FMCP_VCCIO*(1)
FMCP_LA_p[16]	PIN_BC40	FMCP LA bank data p16	FMCP_VCCIO*(1)
FMCP_LA_p[17]	PIN_AY38	FMCP LA bank data p17	FMCP_VCCIO*(1)
FMCP_LA_p[18]	PIN_BE40	FMCP LA bank data p18	FMCP_VCCIO*(1)
FMCP_LA_p[19]	PIN_BE39	FMCP LA bank data p19	FMCP_VCCIO*(1)
FMCP_LA_p[20]	PIN_BF40	FMCP LA bank data p20	FMCP_VCCIO*(1)
FMCP_LA_p[21]	PIN_BG37	FMCP LA bank data p21	FMCP_VCCIO*(1)
FMCP_LA_p[22]	PIN_BF37	FMCP LA bank data p22	FMCP_VCCIO*(1)
FMCP_LA_p[23]	PIN_BD33	FMCP LA bank data p23	FMCP_VCCIO*(1)
FMCP_LA_p[24]	PIN_BF36	FMCP LA bank data p24	FMCP_VCCIO*(1)
FMCP_LA_p[25]	PIN_BE36	FMCP LA bank data p25	FMCP_VCCIO*(1)
FMCP_LA_p[26]	PIN_BD34	FMCP LA bank data p26	FMCP_VCCIO*(1)
FMCP_LA_p[27]	PIN_BB33	FMCP LA bank data p27	FMCP_VCCIO*(1)
FMCP_LA_p[28]	PIN_BG34	FMCP LA bank data p28	FMCP_VCCIO*(1)
FMCP_LA_p[29]	PIN_BC36	FMCP LA bank data p29	FMCP_VCCIO*(1)

FMCP_LA_p[30]	PIN_BJ35	FMCP LA bank data p30	FMCP_VCCIO*(1)
FMCP_LA_p[31]	PIN_BH35	FMCP LA bank data p31	FMCP_VCCIO*(1)
FMCP_LA_p[32]	PIN_BJ33	FMCP LA bank data p32	FMCP_VCCIO*(1)
FMCP_LA_p[33]	PIN_BE33	FMCP LA bank data p33	FMCP_VCCIO*(1)
FMCP_LA_n[0]	PIN_AW39	FMCP LA bank data n0	FMCP_VCCIO*(1)
FMCP_LA_n[1]	PIN_AR34	FMCP LA bank data n1	FMCP_VCCIO*(1)
FMCP_LA_n[2]	PIN_AP33	FMCP LA bank data n2	FMCP_VCCIO*(1)
FMCP_LA_n[3]	PIN_AR36	FMCP LA bank data n3	FMCP_VCCIO*(1)
FMCP_LA_n[4]	PIN_AT36	FMCP LA bank data n4	FMCP_VCCIO*(1)
FMCP_LA_n[5]	PIN_BC37	FMCP LA bank data n5	FMCP_VCCIO*(1)
FMCP_LA_n[6]	PIN_AR37	FMCP LA bank data n6	FMCP_VCCIO*(1)
FMCP_LA_n[7]	PIN_BA39	FMCP LA bank data n7	FMCP_VCCIO*(1)
FMCP_LA_n[8]	PIN_AR33	FMCP LA bank data n8	FMCP_VCCIO*(1)
FMCP_LA_n[9]	PIN_AY40	FMCP LA bank data n9	FMCP_VCCIO*(1)
FMCP_LA_n[10]	PIN_AV40	FMCP LA bank data n10	FMCP_VCCIO*(1)
FMCP_LA_n[11]	PIN_BD38	FMCP LA bank data n11	FMCP_VCCIO*(1)
FMCP_LA_n[12]	PIN_AU37	FMCP LA bank data n12	FMCP_VCCIO*(1)
FMCP_LA_n[13]	PIN_AV38	FMCP LA bank data n13	FMCP_VCCIO*(1)
FMCP_LA_n[14]	PIN_BC38	FMCP LA bank data n14	FMCP_VCCIO*(1)
FMCP_LA_n[15]	PIN_BA37	FMCP LA bank data n15	FMCP_VCCIO*(1)
FMCP_LA_n[16]	PIN_BB40	FMCP LA bank data n16	FMCP_VCCIO*(1)
FMCP_LA_n[17]	PIN_AY39	FMCP LA bank data n17	FMCP_VCCIO*(1)
FMCP_LA_n[18]	PIN_BD40	FMCP LA bank data n18	FMCP_VCCIO*(1)
FMCP_LA_n[19]	PIN_BE38	FMCP LA bank data n19	FMCP_VCCIO*(1)
FMCP_LA_n[20]	PIN_BF39	FMCP LA bank data n20	FMCP_VCCIO*(1)
FMCP_LA_n[21]	PIN_BG38	FMCP LA bank data n21	FMCP_VCCIO*(1)
FMCP_LA_n[22]	PIN_BE37	FMCP LA bank data n22	FMCP_VCCIO*(1)
FMCP_LA_n[23]	PIN_BC33	FMCP LA bank data n23	FMCP_VCCIO*(1)

FMCP_LA_n[24]	PIN_BF35	FMCP LA bank data n24	FMCP_VCCIO*(1)
FMCP_LA_n[25]	PIN_BD36	FMCP LA bank data n25	FMCP_VCCIO*(1)
FMCP_LA_n[26]	PIN_BD35	FMCP LA bank data n26	FMCP_VCCIO*(1)
FMCP_LA_n[27]	PIN_BB34	FMCP LA bank data n27	FMCP_VCCIO*(1)
FMCP_LA_n[28]	PIN_BF34	FMCP LA bank data n28	FMCP_VCCIO*(1)
FMCP_LA_n[29]	PIN_BC35	FMCP LA bank data n29	FMCP_VCCIO*(1)
FMCP_LA_n[30]	PIN_BJ36	FMCP LA bank data n30	FMCP_VCCIO*(1)
FMCP_LA_n[31]	PIN_BG35	FMCP LA bank data n31	FMCP_VCCIO*(1)
FMCP_LA_n[32]	PIN_BJ34	FMCP LA bank data n32	FMCP_VCCIO*(1)
FMCP_LA_n[33]	PIN_BE34	FMCP LA bank data n33	FMCP_VCCIO*(1)
FMCP_GBTCLK_M2C_p[0]	PIN_AM41	LVDS input from the installed FMCP card to dedicated reference clock input pin	LVDS
FMCP_GBTCLK_M2C_p[1]	PIN_AT41	LVDS input from the installed FMCP card to dedicated reference clock input pin	LVDS
FMCP_GBTCLK_M2C_p[2]	PIN_AH41	LVDS input from the installed FMCP card to dedicated reference clock input pin	LVDS
FMCP_GBTCLK_M2C_p[3]	PIN_AM38	LVDS input from the installed FMCP card to dedicated reference clock input pin	LVDS
FMCP_GBTCLK_M2C_p[4]	PIN_T41	LVDS input from the installed FMCP card to dedicated reference clock input pin	LVDS
FMCP_REFCLK0_p	PIN_AP41	FPGA transceiver Reference Clock (From on	LVDS

		board PLL)	
FMCP_REFCLK1_p	PIN_AK38	FPGA transceiver Reference Clock (From on board PLL)	LVDS
FMCP_REFCLK2_p	PIN_P41	FPGA transceiver Reference Clock (From on board PLL)	LVDS
FMCP_DP_C2M_p[0]	PIN_BJ46	Transmit pair p0 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[1]	PIN_BF45	Transmit pair p1 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[2]	PIN_BG47	Transmit pair p2 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[3]	PIN_BE47	Transmit pair p3 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[4]	PIN_BF49	Transmit pair p4 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[5]	PIN_BC47	Transmit pair p5 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[6]	PIN_BD49	Transmit pair p6 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[7]	PIN_BA47	Transmit pair p7 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[8]	PIN_BB49	Transmit pair p8 of the FPGA transceiver	HSSI DIFFERENTIAL

			I/O
FMCP_DP_C2M_p[9]	PIN_AW47	Transmit pair p9 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[10]	PIN_AY49	Transmit pair p10 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[11]	PIN_AU47	Transmit pair p11 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[12]	PIN_AV49	Transmit pair p12 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[13]	PIN_AR47	Transmit pair p13 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[14]	PIN_AT49	Transmit pair p14 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[15]	PIN_AP49	Transmit pair p15 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[16]	PIN_AK49	Transmit pair p16 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[17]	PIN_AL47	Transmit pair p17 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[18]	PIN_AJ47	Transmit pair p18 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[19]	PIN_AF49	Transmit pair p19 of the FPGA transceiver	HSSI DIFFERENTIAL

			I/O
FMCP_DP_C2M_p[20]	PIN_F49	Transmit pair p20 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[21]	PIN_G47	Transmit pair p21 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[22]	PIN_E47	Transmit pair p22 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_C2M_p[23]	PIN_C47	Transmit pair p23 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[0]	PIN_BH41	Receiver pair p0 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[1]	PIN_BJ43	Receiver pair p1 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[2]	PIN_BG43	Receiver pair p2 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[3]	PIN_BE43	Receiver pair p3 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[4]	PIN_BC43	Receiver pair p4 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[5]	PIN_BD45	Receiver pair p5 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[6]	PIN_BA43	Receiver pair p6 of the FPGA transceiver	HSSI DIFFERENTIAL

			I/O
FMCP_DP_M2C_p[7]	PIN_BB45	Receiver pair p7 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[8]	PIN_AW43	Receiver pair p8 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[9]	PIN_AY45	Receiver pair p9 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[10]	PIN_AU43	Receiver pair p10 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[11]	PIN_AV45	Receiver pair p11 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[12]	PIN_AR43	Receiver pair p12 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[13]	PIN_AT45	Receiver pair p13 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[14]	PIN_AP45	Receiver pair p14 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[15]	PIN_AN43	Receiver pair p15 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[16]	PIN_AL43	Receiver pair p16 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[17]	PIN_AH45	Receiver pair p17 of the FPGA transceiver	HSSI DIFFERENTIAL

			I/O
FMCP_DP_M2C_p[18]	PIN_AF45	Receiver pair p18 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[19]	PIN_AG43	Receiver pair p19 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[20]	PIN_G43	Receiver pair p20 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[21]	PIN_D45	Receiver pair p21 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[22]	PIN_C43	Receiver pair p22 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_DP_M2C_p[23]	PIN_A43	Receiver pair p23 of the FPGA transceiver	HSSI DIFFERENTIAL I/O
FMCP_REFCLK_C2M_p	PIN_BB35	Reference clock from carrier card mezzanine module to positive	LVDS
FMCP_REFCLK_M2C_p	PIN_BH33	Reference clock from mezzanine module to carrier card positive	LVDS
FMCP_GA[0]	PIN_AU35	FMCP geographical address 0	3.3 V*(2)
FMCP_GA[1]	PIN_AV35	FMCP geographical address 1	3.3 V*(2)
FMCP_SCL	PIN_AU34	Management serial clock line	3.3 V*(2)
FMCP_SDA	PIN_AU33	Management serial data line	3.3 V*(2)

FMCP_RES[0]	PIN_AJ34	Reserved	3.3 V
FMCP_RES[1]	PIN_AD34	Reserved	3.3 V
FMCP_SYNC_C2M_p	PIN_AU32	Synchronize signal from carrier card to mezzanine module positive	LVDS
FMCP_SYNC_M2C_p	PIN_AV33	Synchronize signal from mezzanine module to carrier card positive	LVDS

- *(1): The FMCP_VCCIO value depends on the setting of JP2, which can adjust the FMCP_VCCIO to **1.2V, 1.5V or 1.8V**. Please refer to section 2.2 : "*FMCP_VCCIO and FMCP_VCCIO Select Header*" for details.
- *(2): There are level shift ICs that convert FMCP_VCCIO to 3.3V between the FPGA pins and the FMC pins.

2.7 Clock Circuit

The development board includes one 50 MHz TCXO and two programmable clock generators. **Figure 2-12** shows the default frequencies of on-board all external clocks going to the Stratix 10 SX FPGA.

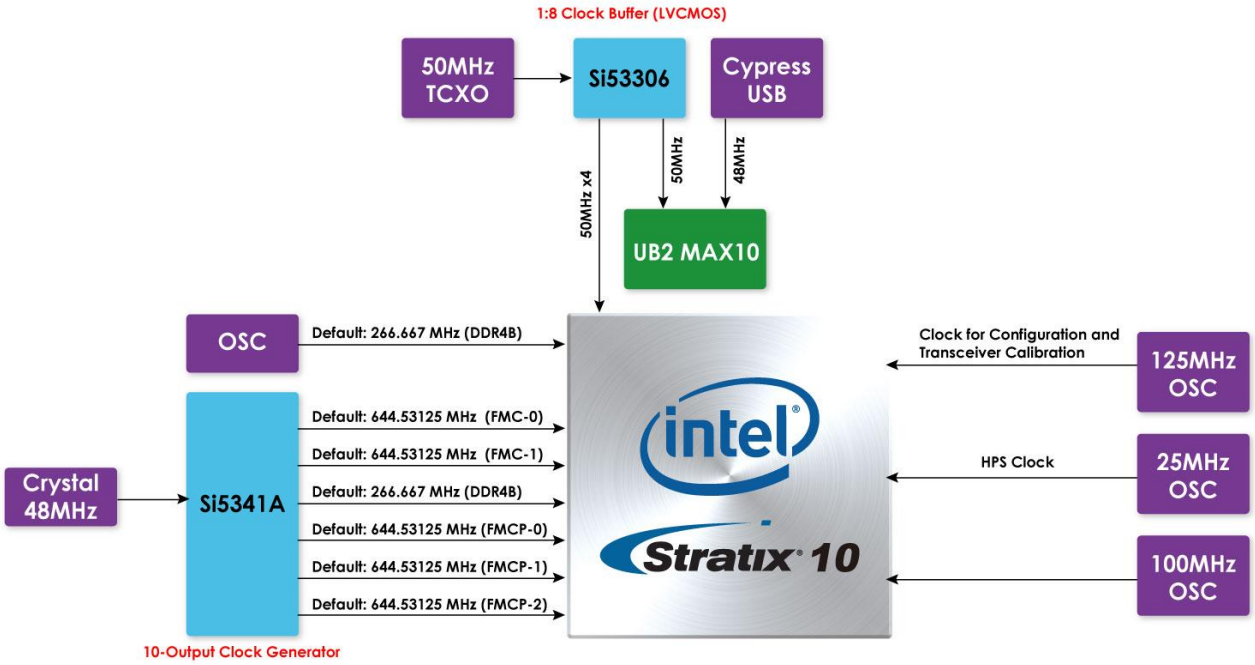


Figure 2-12 Clock circuit of the FPGA Board

A clock buffer is used to duplicate the 50 MHz TCXO output clock, so there are two 50MHz clocks fed into different two FPGA banks. The two programming clock generators with low-jitter clock outputs are used to provide special and high- quality clock signals for high-speed transceivers and high bandwidth memory. Through I2C serial interface, the clock generator controllers in the Stratix 10 SX FPGA can be used to program these two Si5341As to generate FMC and FMC+ connector reference clock and high bandwidth memory reference clocks respectively. One oscillator provides a 125 MHz clock used as configuration clock or used as the clock for transceiver calibration.

In addition, the reference clock (DDR4A_REFCLK_p) for DDR4A can be selected by a dual frequency OSC to the FPGA. For details, please refer to the "DDR4A Reference Clock Switch" part in the section 2.2.

Table 2-20 Clock source and clock pin to the FPGA

Source	Schematic Signal Name	Default Frequency	I/O Standard	Arria 10 GX Pin Number	Application
U16	CLK_50_B2F	50.0 MHz	VCCIO_FMC	PIN_BA27	User application

Si53306	CLK_50_B2L		1.8V	PIN_J25	User application
	CLK_50_B3C		1.8V	PIN_BF21	User application
	CLK_50_B3I		1.8V	PIN_M24	User application
Y6 OSC	OSC_CLK_1	125MHz	1.8V	PIN_BA22	Clock for configuration and transceiver calibration
Y9 OSC	CLK_100_B3I	100Mhz	VCCIO_FMC	PIN_L24	User application
Y8 Dual Frequency OSC	DDR4A_REFCLK_p	266.267Mhz	LVDS	PIN_M35	DDR4 reference clock for A port
U71 Si5341A	FMC_REFCLK0_p	644.53125 MHz	LVDS	PIN_AK12	FMC connector reference clock 0
	FMC_REFCLK1_p	644.53125 MHz	LVDS	PIN_P9	FMC connector reference clock 1
	FMCP_REFCLK0_p	644.53125 MHz	LVDS	PIN_AP41	FMCP connector reference clock 0
	FMCP_REFCLK1_p	644.53125 MHz	LVDS	PIN_AK38	FMCP connector reference clock 1
	FMCP_REFCLK2_p	644.53125 MHz	LVDS	PIN_P41	FMCP connector reference clock 2
	LVDS_REFCLK_p	50 MHz	LVDS	PIN_U24	User application
	DDR4B_REFCLK_p	266.267Mhz	LVDS	PIN_AT17	DDR4 reference clock for B port

2.8 USB to UART for HPS

The Apollo-S10 board provides a UART interface for users to communicate and transfer data with HPS through the host. This interface is mainly implemented through a USB to serial UART chip (FT232R). It can convert commands and data from the host via USB protocol to the UART interface and send it to HPS. Please note that due to space constraints, The Apollo S10 uses a USB hub to allow USB to UART interface (for HPS and FPGA fabric), USB blaster II circuit and MAX10 system controller to share a Mini USB connector to connect to the host.

For More information about the USB UART chip is available on the manufacturer's website, or in the directory \Datasheets\UART_TO_USB of Apollo S10 system CD. **Figure 2-13** shows the connections between the HPS, FT232R chip, and the USB Mini-B connector. **Table 2-21** lists the pin assignment of UART interface connected to the HPS.

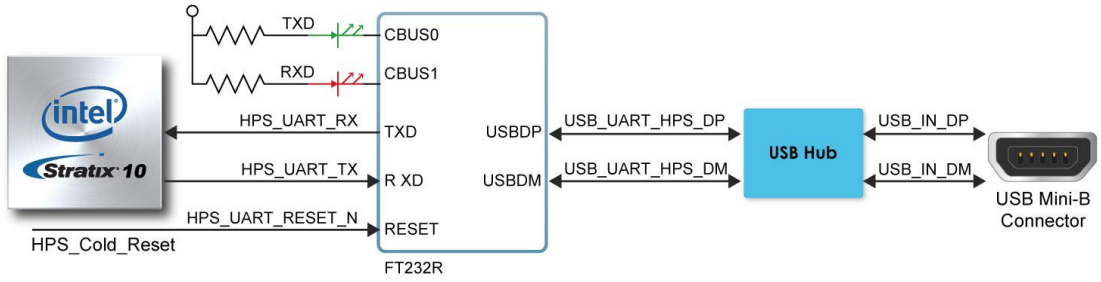


Figure 2-13 Connections between the HPS of Apollo S10 and FT232R Chip

Table 2-21 Pin Assignment of UART Interface

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_UART_RX	PIN_K29	HPS UART Receiver	1.8V
HPS_UART_TX	PIN_F32	HPS UART Transmitter	1.8V

2.9 DDR4 SDRAM

The development board supports four independent banks of DDR4 SDRAM (**DDR4A**, and **DDR4B**). Each DDR4 bank can support 32GB DDR4-2133. The I/O bank where DDR4A is located can implement Intel Stratix 10 EMIF IP with the Intel Stratix 10 Hard Processor Subsystem (HPS). If no HPS EMIF is used in a system, the DDR4A bank can be used for the EMIF of the FPGA fabric. The DDR4A and DDR4B bank can run at the fastest clock frequency of 1066MHz clock for a maximum theoretical bandwidth up to 136.4 Gbps. **Figure 2-14** shows the connections between the DDR4 SDRAM bank and Stratix 10 SX FPGA.

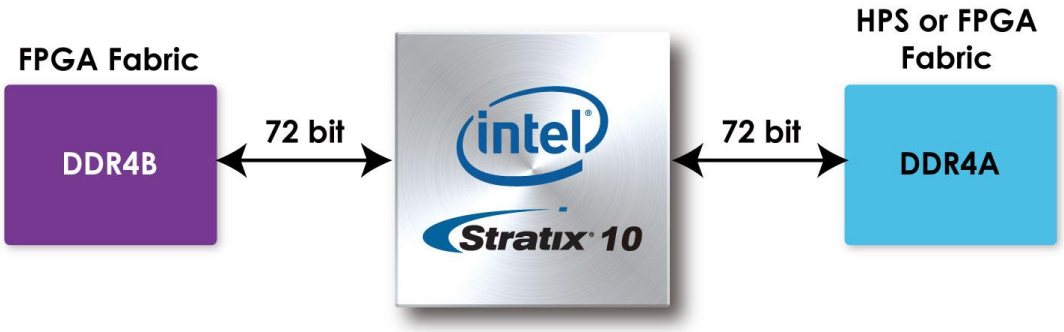


Figure 2-14 Connection between the DDR4 and Stratix 10 SX FPGA

The pin assignments for DDR4 SDRAM Bank A and Bank B are listed in **Table 2-22** and **Table 2-23** respectively.

Table 2-22 DDR4A Bank Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Stratix 10 Pin Number
DDR4A_DQ0	Data [0]	1.2-V POD	PIN_B35
DDR4A_DQ1	Data [1]	1.2-V POD	PIN_A37
DDR4A_DQ2	Data [2]	1.2-V POD	PIN_D36
DDR4A_DQ3	Data [3]	1.2-V POD	PIN_B38
DDR4A_DQ4	Data [4]	1.2-V POD	PIN_C35
DDR4A_DQ5	Data [5]	1.2-V POD	PIN_C38
DDR4A_DQ6	Data [6]	1.2-V POD	PIN_C37
DDR4A_DQ7	Data [7]	1.2-V POD	PIN_B37
DDR4A_DQ8	Data [8]	1.2-V POD	PIN_D38
DDR4A_DQ9	Data [9]	1.2-V POD	PIN_F37
DDR4A_DQ10	Data [10]	1.2-V POD	PIN_E39
DDR4A_DQ11	Data [11]	1.2-V POD	PIN_D35
DDR4A_DQ12	Data [12]	1.2-V POD	PIN_E38
DDR4A_DQ13	Data [13]	1.2-V POD	PIN_D34
DDR4A_DQ14	Data [14]	1.2-V POD	PIN_E37
DDR4A_DQ15	Data [15]	1.2-V POD	PIN_H37
DDR4A_DQ16	Data [16]	1.2-V POD	PIN_G35
DDR4A_DQ17	Data [17]	1.2-V POD	PIN_J35

DDR4A_DQ18	Data [18]	1.2-V POD	PIN_E34
DDR4A_DQ19	Data [19]	1.2-V POD	PIN_H33
DDR4A_DQ20	Data [20]	1.2-V POD	PIN_H35
DDR4A_DQ21	Data [21]	1.2-V POD	PIN_H36
DDR4A_DQ22	Data [22]	1.2-V POD	PIN_F35
DDR4A_DQ23	Data [23]	1.2-V POD	PIN_J36
DDR4A_DQ24	Data [24]	1.2-V POD	PIN_K32
DDR4A_DQ25	Data [25]	1.2-V POD	PIN_N31
DDR4A_DQ26	Data [26]	1.2-V POD	PIN_M33
DDR4A_DQ27	Data [27]	1.2-V POD	PIN_N32
DDR4A_DQ28	Data [28]	1.2-V POD	PIN_K33
DDR4A_DQ29	Data [29]	1.2-V POD	PIN_N33
DDR4A_DQ30	Data [30]	1.2-V POD	PIN_K34
DDR4A_DQ31	Data [31]	1.2-V POD	PIN_M34
DDR4A_DQ32	Data [32]	1.2-V POD	PIN_N27
DDR4A_DQ33	Data [33]	1.2-V POD	PIN_P25
DDR4A_DQ34	Data [34]	1.2-V POD	PIN_L25
DDR4A_DQ35	Data [35]	1.2-V POD	PIN_R26
DDR4A_DQ36	Data [36]	1.2-V POD	PIN_U25
DDR4A_DQ37	Data [37]	1.2-V POD	PIN_P26
DDR4A_DQ38	Data [38]	1.2-V POD	PIN_M25
DDR4A_DQ39	Data [39]	1.2-V POD	PIN_T25
DDR4A_DQ40	Data [40]	1.2-V POD	PIN_U28
DDR4A_DQ41	Data [41]	1.2-V POD	PIN_V26
DDR4A_DQ42	Data [42]	1.2-V POD	PIN_U27
DDR4A_DQ43	Data [43]	1.2-V POD	PIN_V25
DDR4A_DQ44	Data [44]	1.2-V POD	PIN_T30
DDR4A_DQ45	Data [45]	1.2-V POD	PIN_U29
DDR4A_DQ46	Data [46]	1.2-V POD	PIN_T29
DDR4A_DQ47	Data [47]	1.2-V POD	PIN_U30
DDR4A_DQ48	Data [48]	1.2-V POD	PIN_F25
DDR4A_DQ49	Data [49]	1.2-V POD	PIN_H27
DDR4A_DQ50	Data [50]	1.2-V POD	PIN_H25
DDR4A_DQ51	Data [51]	1.2-V POD	PIN_K27
DDR4A_DQ52	Data [52]	1.2-V POD	PIN_G25

DDR4A_DQ53	Data [53]	1.2-V POD	PIN_M27
DDR4A_DQ54	Data [54]	1.2-V POD	PIN_L27
DDR4A_DQ55	Data [55]	1.2-V POD	PIN_H26
DDR4A_DQ56	Data [56]	1.2-V POD	PIN_D26
DDR4A_DQ57	Data [57]	1.2-V POD	PIN_B25
DDR4A_DQ58	Data [58]	1.2-V POD	PIN_F27
DDR4A_DQ59	Data [59]	1.2-V POD	PIN_B27
DDR4A_DQ60	Data [60]	1.2-V POD	PIN_G27
DDR4A_DQ61	Data [61]	1.2-V POD	PIN_C27
DDR4A_DQ62	Data [62]	1.2-V POD	PIN_C26
DDR4A_DQ63	Data [63]	1.2-V POD	PIN_D25
DDR4A_DQ64	Data [64]	1.2-V POD	PIN_R31
DDR4A_DQ65	Data [65]	1.2-V POD	PIN_P33
DDR4A_DQ66	Data [66]	1.2-V POD	PIN_U32
DDR4A_DQ67	Data [67]	1.2-V POD	PIN_R34
DDR4A_DQ68	Data [68]	1.2-V POD	PIN_T31
DDR4A_DQ69	Data [69]	1.2-V POD	PIN_T34
DDR4A_DQ70	Data [70]	1.2-V POD	PIN_V32
DDR4A_DQ71	Data [71]	1.2-V POD	PIN_U33
DDR4A_DQS0	Data Strobe p[0]	DIFFERENTIAL 1.2-V POD	PIN_A36
DDR4A_DQS_n0	Data Strobe n[0]	DIFFERENTIAL 1.2-V POD	PIN_A35
DDR4A_DQS1	Data Strobe p[1]	DIFFERENTIAL 1.2-V POD	PIN_E36
DDR4A_DQS_n1	Data Strobe n[1]	DIFFERENTIAL 1.2-V POD	PIN_F36
DDR4A_DQS2	Data Strobe p[2]	DIFFERENTIAL 1.2-V POD	PIN_G33
DDR4A_DQS_n2	Data Strobe n[2]	DIFFERENTIAL 1.2-V POD	PIN_G34
DDR4A_DQS3	Data Strobe p[3]	DIFFERENTIAL 1.2-V POD	PIN_L32
DDR4A_DQS_n3	Data Strobe n[3]	DIFFERENTIAL 1.2-V POD	PIN_L31

DDR4A_DQS4	Data Strobe p[4]	DIFFERENTIAL 1.2-V POD	PIN_T26
DDR4A_DQS_n4	Data Strobe n[4]	DIFFERENTIAL 1.2-V POD	PIN_R27
DDR4A_DQS5	Data Strobe p[5]	DIFFERENTIAL 1.2-V POD	PIN_V28
DDR4A_DQS_n5	Data Strobe n[5]	DIFFERENTIAL 1.2-V POD	PIN_V27
DDR4A_DQS6	Data Strobe p[6]	DIFFERENTIAL 1.2-V POD	PIN_J26
DDR4A_DQS_n6	Data Strobe n[6]	DIFFERENTIAL 1.2-V POD	PIN_K26
DDR4A_DQS7	Data Strobe p[7]	DIFFERENTIAL 1.2-V POD	PIN_E26
DDR4A_DQS_n7	Data Strobe n[7]	DIFFERENTIAL 1.2-V POD	PIN_F26
DDR4A_DQS8	Data Strobe p[8]	DIFFERENTIAL 1.2-V POD	PIN_R32
DDR4A_DQS_n8	Data Strobe n[8]	DIFFERENTIAL 1.2-V POD	PIN_T32
DDR4A_DBI_n0	Data Bus Inversion [0]	1.2-V POD	PIN_C36
DDR4A_DBI_n1	Data Bus Inversion [1]	1.2-V POD	PIN_D39
DDR4A_DBI_n2	Data Bus Inversion [2]	1.2-V POD	PIN_F34
DDR4A_DBI_n3	Data Bus Inversion [3]	1.2-V POD	PIN_J34
DDR4A_DBI_n4	Data Bus Inversion [4]	1.2-V POD	PIN_N25
DDR4A_DBI_n5	Data Bus Inversion [5]	1.2-V POD	PIN_V30
DDR4A_DBI_n6	Data Bus Inversion [6]	1.2-V POD	PIN_L26
DDR4A_DBI_n7	Data Bus Inversion [7]	1.2-V POD	PIN_E27

DDR4A_DBI_n8	Data Bus Inversion [8]	1.2-V POD	PIN_U34
DDR4A_A0	Address [0]	SSTL-12	PIN_K38
DDR4A_A1	Address [1]	SSTL-12	PIN_L37
DDR4A_A2	Address [2]	SSTL-12	PIN_M37
DDR4A_A3	Address [3]	SSTL-12	PIN_M38
DDR4A_A4	Address [4]	SSTL-12	PIN_J39
DDR4A_A5	Address [5]	SSTL-12	PIN_J38
DDR4A_A6	Address [6]	SSTL-12	PIN_K39
DDR4A_A7	Address [7]	SSTL-12	PIN_L39
DDR4A_A8	Address [8]	SSTL-12	PIN_P37
DDR4A_A9	Address [9]	SSTL-12	PIN_R37
DDR4A_A10	Address [10]	SSTL-12	PIN_N37
DDR4A_A11	Address [11]	SSTL-12	PIN_P38
DDR4A_A12	Address [12]	SSTL-12	PIN_P35
DDR4A_A13	Address [13]	SSTL-12	PIN_K36
DDR4A_A14	Address [14]/ WE_n	SSTL-12	PIN_K37
DDR4A_A15	Address [15]/ CAS_n	SSTL-12	PIN_N36
DDR4A_A16	Address [16]/ RAS_n	SSTL-12	PIN_P36
DDR4A_A17	Address [17]/ NC	SSTL-12	PIN_L35
DDR4A_BA0	Bank Select [0]	SSTL-12	PIN_L36
DDR4A_BA1	Bank Select [1]	SSTL-12	PIN_T35
DDR4A_BG0	Bank Group Select [0]	SSTL-12	PIN_R36
DDR4A_BG1	Bank Group Select [1]	SSTL-12	PIN_D40
DDR4A_CK	Clock p	DIFFERENTIAL 1.2-V SSTL	PIN_F39
DDR4A_CK_n	Clock n	DIFFERENTIAL 1.2-V SSTL	PIN_G39
DDR4A_CKE0	Clock Enable pin	SSTL-12	PIN_L40
DDR4A_CKE1	Clock Enable pin	SSTL-12	PIN_K40

DDR4A_ODT0	On Die Termination	SSTL-12	PIN_G40
DDR4A_ODT1	On Die Termination	SSTL-12	PIN_F40
DDR4A_CS_n0	Chip Select	SSTL-12	PIN_G38
DDR4A_CS_n1	Chip Select	SSTL-12	PIN_J40
DDR4A_PAR	Command and Address Parity Input	SSTL-12	PIN_H40
DDR4A_ALERT_n	Register ALERT_n output	1.2 V	PIN_A38
DDR4A_ACT_n	Activation Command Input	SSTL-12	PIN_H38
DDR4A_RESET_n	Chip Reset	1.2 V	PIN_E40
DDR4A_REFCLK_p	DDR4 A port Reference Clock p	LVDS	PIN_M35
DDR4A_REFCLK_n	DDR4 A port Reference Clock n	LVDS	PIN_N35
DDR4A_RZQ	External precision resistor	1.2 V	PIN_P34

Table 2-23 DDR4B Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Stratix 10 Pin Number
DDR4B_DQ0	Data [0]	1.2-V POD	PIN_BH20
DDR4B_DQ1	Data [1]	1.2-V POD	PIN_BJ18
DDR4B_DQ2	Data [2]	1.2-V POD	PIN_BH21
DDR4B_DQ3	Data [3]	1.2-V POD	PIN_BG17
DDR4B_DQ4	Data [4]	1.2-V POD	PIN_BG18
DDR4B_DQ5	Data [5]	1.2-V POD	PIN_BF17
DDR4B_DQ6	Data [6]	1.2-V POD	PIN_BG19
DDR4B_DQ7	Data [7]	1.2-V POD	PIN_BE17
DDR4B_DQ8	Data [8]	1.2-V POD	PIN_BE18
DDR4B_DQ9	Data [9]	1.2-V POD	PIN_BD20

DDR4B_DQ10	Data [10]	1.2-V POD	PIN_BC18
DDR4B_DQ11	Data [11]	1.2-V POD	PIN_BG20
DDR4B_DQ12	Data [12]	1.2-V POD	PIN_BD18
DDR4B_DQ13	Data [13]	1.2-V POD	PIN_BE21
DDR4B_DQ14	Data [14]	1.2-V POD	PIN_BB18
DDR4B_DQ15	Data [15]	1.2-V POD	PIN_BD19
DDR4B_DQ16	Data [16]	1.2-V POD	PIN_AT19
DDR4B_DQ17	Data [17]	1.2-V POD	PIN_AT20
DDR4B_DQ18	Data [18]	1.2-V POD	PIN_AR19
DDR4B_DQ19	Data [19]	1.2-V POD	PIN_AU20
DDR4B_DQ20	Data [20]	1.2-V POD	PIN_AP20
DDR4B_DQ21	Data [21]	1.2-V POD	PIN_AR21
DDR4B_DQ22	Data [22]	1.2-V POD	PIN_AN20
DDR4B_DQ23	Data [23]	1.2-V POD	PIN_AV20
DDR4B_DQ24	Data [24]	1.2-V POD	PIN_BC20
DDR4B_DQ25	Data [25]	1.2-V POD	PIN_BB19
DDR4B_DQ26	Data [26]	1.2-V POD	PIN_BC21
DDR4B_DQ27	Data [27]	1.2-V POD	PIN_BA19
DDR4B_DQ28	Data [28]	1.2-V POD	PIN_BD21
DDR4B_DQ29	Data [29]	1.2-V POD	PIN_AW20
DDR4B_DQ30	Data [30]	1.2-V POD	PIN_BA21
DDR4B_DQ31	Data [31]	1.2-V POD	PIN_AW19
DDR4B_DQ32	Data [32]	1.2-V POD	PIN_AY16
DDR4B_DQ33	Data [33]	1.2-V POD	PIN_AY17
DDR4B_DQ34	Data [34]	1.2-V POD	PIN_AV16
DDR4B_DQ35	Data [35]	1.2-V POD	PIN_BB17
DDR4B_DQ36	Data [36]	1.2-V POD	PIN_AW16
DDR4B_DQ37	Data [37]	1.2-V POD	PIN_AY18
DDR4B_DQ38	Data [38]	1.2-V POD	PIN_AV17
DDR4B_DQ39	Data [39]	1.2-V POD	PIN_BC17
DDR4B_DQ40	Data [40]	1.2-V POD	PIN_AY14
DDR4B_DQ41	Data [41]	1.2-V POD	PIN_BA16
DDR4B_DQ42	Data [42]	1.2-V POD	PIN_AW15
DDR4B_DQ43	Data [43]	1.2-V POD	PIN_BC13
DDR4B_DQ44	Data [44]	1.2-V POD	PIN_AW14

DDR4B_DQ45	Data [45]	1.2-V POD	PIN_BA15
DDR4B_DQ46	Data [46]	1.2-V POD	PIN_AV15
DDR4B_DQ47	Data [47]	1.2-V POD	PIN_BB13
DDR4B_DQ48	Data [48]	1.2-V POD	PIN_BJ16
DDR4B_DQ49	Data [49]	1.2-V POD	PIN_BJ14
DDR4B_DQ50	Data [50]	1.2-V POD	PIN_BG14
DDR4B_DQ51	Data [51]	1.2-V POD	PIN_BH12
DDR4B_DQ52	Data [52]	1.2-V POD	PIN_BH16
DDR4B_DQ53	Data [53]	1.2-V POD	PIN_BG12
DDR4B_DQ54	Data [54]	1.2-V POD	PIN_BG13
DDR4B_DQ55	Data [55]	1.2-V POD	PIN_BF12
DDR4B_DQ56	Data [56]	1.2-V POD	PIN_BD16
DDR4B_DQ57	Data [57]	1.2-V POD	PIN_BG15
DDR4B_DQ58	Data [58]	1.2-V POD	PIN_BD15
DDR4B_DQ59	Data [59]	1.2-V POD	PIN_BF14
DDR4B_DQ60	Data [60]	1.2-V POD	PIN_BC16
DDR4B_DQ61	Data [61]	1.2-V POD	PIN_BE13
DDR4B_DQ62	Data [62]	1.2-V POD	PIN_BF15
DDR4B_DQ63	Data [63]	1.2-V POD	PIN_BD13
DDR4B_DQ64	Data [64]	1.2-V POD	PIN_AP13
DDR4B_DQ65	Data [65]	1.2-V POD	PIN_AR14
DDR4B_DQ66	Data [66]	1.2-V POD	PIN_AP16
DDR4B_DQ67	Data [67]	1.2-V POD	PIN_AU13
DDR4B_DQ68	Data [68]	1.2-V POD	PIN_AP15
DDR4B_DQ69	Data [69]	1.2-V POD	PIN_AT14
DDR4B_DQ70	Data [70]	1.2-V POD	PIN_AT12
DDR4B_DQ71	Data [71]	1.2-V POD	PIN_AU12
DDR4B_DQS0	Data Strobe p[0]	DIFFERENTIAL 1.2-V POD	PIN_BJ19
DDR4B_DQS_n0	Data Strobe n[0]	DIFFERENTIAL 1.2-V POD	PIN_BJ20
DDR4B_DQS1	Data Strobe p[1]	DIFFERENTIAL 1.2-V POD	PIN_BE19
DDR4B_DQS_n1	Data Strobe n[1]	DIFFERENTIAL 1.2-V POD	PIN_BF19

DDR4B_DQS2	Data Strobe p[2]	DIFFERENTIAL 1.2-V POD	PIN_AN21
DDR4B_DQS_n2	Data Strobe n[2]	DIFFERENTIAL 1.2-V POD	PIN_AP21
DDR4B_DQS3	Data Strobe p[3]	DIFFERENTIAL 1.2-V POD	PIN_AW21
DDR4B_DQS_n3	Data Strobe n[3]	DIFFERENTIAL 1.2-V POD	PIN_AY21
DDR4B_DQS4	Data Strobe p[4]	DIFFERENTIAL 1.2-V POD	PIN_AW18
DDR4B_DQS_n4	Data Strobe n[4]	DIFFERENTIAL 1.2-V POD	PIN_AV18
DDR4B_DQS5	Data Strobe p[5]	DIFFERENTIAL 1.2-V POD	PIN_BA14
DDR4B_DQS_n5	Data Strobe n[5]	DIFFERENTIAL 1.2-V POD	PIN_BB14
DDR4B_DQS6	Data Strobe p[6]	DIFFERENTIAL 1.2-V POD	PIN_BJ15
DDR4B_DQS_n6	Data Strobe n[6]	DIFFERENTIAL 1.2-V POD	PIN_BH15
DDR4B_DQS7	Data Strobe p[7]	DIFFERENTIAL 1.2-V POD	PIN_BF16
DDR4B_DQS_n7	Data Strobe n[7]	DIFFERENTIAL 1.2-V POD	PIN_BE16
DDR4B_DQS8	Data Strobe p[8]	DIFFERENTIAL 1.2-V POD	PIN_AP12
DDR4B_DQS_n8	Data Strobe n[8]	DIFFERENTIAL 1.2-V POD	PIN_AR13
DDR4B_DBI_n0	Data Bus Inversion [0]	1.2-V POD	PIN_BH17
DDR4B_DBI_n1	Data Bus Inversion [1]	1.2-V POD	PIN_BF20
DDR4B_DBI_n2	Data Bus Inversion [2]	1.2-V POD	PIN_AT21
DDR4B_DBI_n3	Data Bus Inversion [3]	1.2-V POD	PIN_BA20

DDR4B_DBI_n4	Data Bus Inversion [4]	1.2-V POD	PIN_BA17
DDR4B_DBI_n5	Data Bus Inversion [5]	1.2-V POD	PIN_BC15
DDR4B_DBI_n6	Data Bus Inversion [6]	1.2-V POD	PIN_BJ13
DDR4B_DBI_n7	Data Bus Inversion [7]	1.2-V POD	PIN_BD14
DDR4B_DBI_n8	Data Bus Inversion [8]	1.2-V POD	PIN_AV13
DDR4B_A0	Address [0]	SSTL-12	PIN_AY11
DDR4B_A1	Address [1]	SSTL-12	PIN_AW11
DDR4B_A2	Address [2]	SSTL-12	PIN_BA10
DDR4B_A3	Address [3]	SSTL-12	PIN_BA11
DDR4B_A4	Address [4]	SSTL-12	PIN_BA12
DDR4B_A5	Address [5]	SSTL-12	PIN_AY12
DDR4B_A6	Address [6]	SSTL-12	PIN_AV11
DDR4B_A7	Address [7]	SSTL-12	PIN_AV12
DDR4B_A8	Address [8]	SSTL-12	PIN_AW13
DDR4B_A9	Address [9]	SSTL-12	PIN_AY13
DDR4B_A10	Address [10]	SSTL-12	PIN_AW10
DDR4B_A11	Address [11]	SSTL-12	PIN_AV10
DDR4B_A12	Address [12]	SSTL-12	PIN_AN18
DDR4B_A13	Address [13]	SSTL-12	PIN_AR17
DDR4B_A14	Address [14]/ WE_n	SSTL-12	PIN_AR16
DDR4B_A15	Address [15]/ CAS_n	SSTL-12	PIN_AT15
DDR4B_A16	Address [16]/ RAS_n	SSTL-12	PIN_AT16
DDR4B_A17	Address [17]/ NC	SSTL-12	PIN_AU15
DDR4B_BA0	Bank Select [0]	SSTL-12	PIN_AU14
DDR4B_BA1	Bank Select [1]	SSTL-12	PIN_AP18
DDR4B_BG0	Bank Group Select [0]	SSTL-12	PIN_AR18

DDR4B_BG1	Bank Group Select [1]	SSTL-12	PIN_BF11
DDR4B_CK	Clock p	DIFFERENTIAL 1.2-V SSTL	PIN_BC12
DDR4B_CK_n	Clock n	DIFFERENTIAL 1.2-V SSTL	PIN_BB12
DDR4B_CKE0	Clock Enable pin	SSTL-12	PIN_BC10
DDR4B_CKE1	Clock Enable pin	SSTL-12	PIN_BB10
DDR4B_ODT0	On Die Termination	SSTL-12	PIN_BE12
DDR4B_ODT1	On Die Termination	SSTL-12	PIN_BE11
DDR4B_CS_n0	Chip Select	SSTL-12	PIN_BE10
DDR4B_CS_n1	Chip Select	SSTL-12	PIN_BD11
DDR4B_PAR	Command and Address Parity Input	SSTL-12	PIN_BC11
DDR4B_ALERT_n	Register ALERT_n output	1.2 V	PIN_BH18
DDR4B_ACT_n	Activation Command Input	SSTL-12	PIN_BD10
DDR4B_RESET_n	Chip Reset	1.2 V	PIN_BF10
DDR4B_REFCLK_p	DDR4 B port Reference Clock p	LVDS	PIN_AT17
DDR4B_RZQ	External precision resistor	1.2 V	PIN_AN17

2.10 USB 2.0 OTG PHY

The board provides USB interfaces using the SMSC USB3300 controller. A SMSC USB3300 device in a 32-pin QFN package device is used to interface to a single Type AB Micro-USB connector. This device supports UTMI+ Low Pin Interface (ULPI) to communicate to USB 2.0 controller in HPS. As defined by OTG mode, the PHY can operate in Host or Device modes. When operating in Host mode, the interface will supply the power to the device through the Micro-USB interface. **Figure 2-15** shows the connections of USB PTG PHY to the HPS.

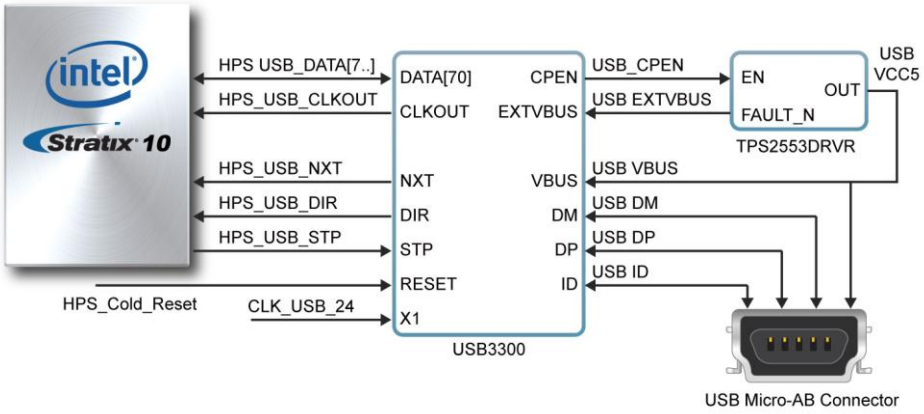


Figure 2-15 Connections between the HPS of Apollo S10 and USB controller

Table 2-24 Pin Assignment of USB OTG PHY

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_USB_CLK	PIN_E29	60MHz Reference Clock Output	1.8V
HPS_USB_DATA[0]	PIN_A30	HPS USB_DATA[0]	1.8V
HPS_USB_DATA[1]	PIN_C32	HPS USB_DATA[1]	1.8V
HPS_USB_DATA[2]	PIN_A29	HPS USB_DATA[2]	1.8V
HPS_USB_DATA[3]	PIN_E33	HPS USB_DATA[3]	1.8V
HPS_USB_DATA[4]	PIN_F29	HPS USB_DATA[4]	1.8V
HPS_USB_DATA[5]	PIN_E32	HPS USB_DATA[5]	1.8V
HPS_USB_DATA[6]	PIN_B30	HPS USB_DATA[6]	1.8V
HPS_USB_DATA[7]	PIN_D29	HPS USB_DATA[7]	1.8V
HPS_USB_DIR	PIN_D30	Direction of the Data Bus	1.8V
HPS_USB_NXT	PIN_A27	Throttle the Data	1.8V
HPS_USB_STP	PIN_C33	Stop Data Stream on the Bus	1.8V

2.11 Gigabit Ethernet

The board supports Gigabit Ethernet transfer by an external Micrel KSZ9031RN PHY chip and HPS Ethernet MAC function. The KSZ9031RN chip with integrated 10/100/1000 Mbps Gigabit Ethernet transceiver also supports RGMII MAC interface. **Figure 2-16** shows the connections between the HPS, Gigabit Ethernet PHY, and RJ-45 connector.

For more information about the KSZ9031RN PHY chip and its datasheet, as well as the application notes, which are available on the manufacturer's website.

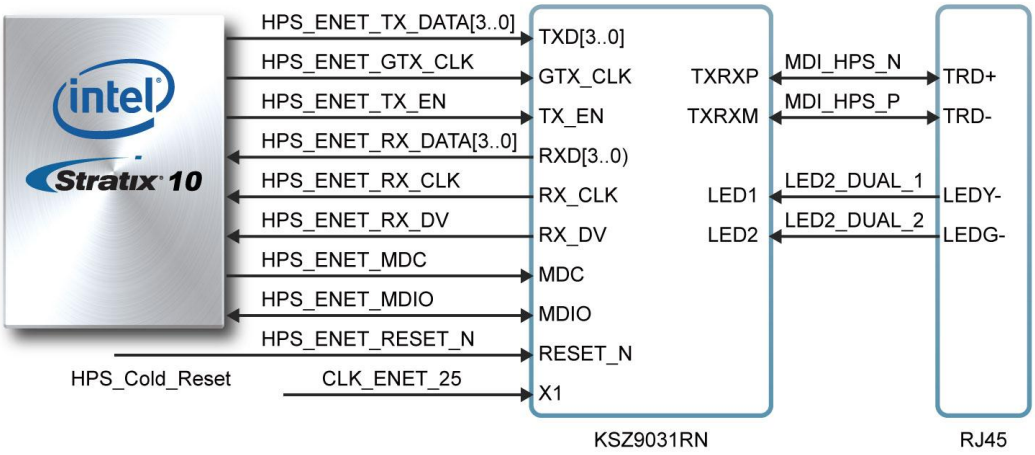


Figure 2-16 Connections between the HPS of Apollo S10 and RGMII MAC

There are two LEDs, a green LED (LEDG) and a yellow LED (LEDY), which represent the status of the Ethernet PHY (KSZ9031RN). The LED control signals are connected to the LEDs on the RJ45 connector. The state and the definition of LEDG and LEDY are listed in **Table 2-25**. For instance, the connection from board to Gigabit Ethernet is established once the LEDG lights on.

Table 2-25 State and Definition of LED Mode Pins

LED (State)		LED (Definition)		Link /Activity
LEDG	LEDY	LEDG	LEDY	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000 Link / No Activity
Toggle	H	Blinking	OFF	1000 Link / Activity (RX, TX)
H	L	OFF	ON	100 Link / No Activity
H	Toggle	OFF	Blinking	100 Link / Activity (RX, TX)
L	L	ON	ON	10 Link/ No Activity
Toggle	Toggle	Blinking	Blinking	Link / Activity (RX, TX)

Table 2-26 Pin Assignment of Gigabit Ethernet PHY

Signal Name	FPGA Pin No	Description	I/O Standard

HPS_ENET_TX_CTL	PIN_R29	GMII and MII transmit enable	1.8V
HPS_ENET_TX_DATA[0]	PIN_J28	MII transmit data[0]	1.8V
HPS_ENET_TX_DATA[1]	PIN_E28	MII transmit data[1]	1.8V
HPS_ENET_TX_DATA[2]	PIN_P29	MII transmit data[2]	1.8V
HPS_ENET_TX_DATA[3]	PIN_B32	MII transmit data[3]	1.8V
HPS_ENET_RX_CTL	PIN_F30	GMII and MII receive data valid	1.8V
HPS_ENET_RX_DATA[0]	PIN_B34	GMII and MII receive data[0]	1.8V
HPS_ENET_RX_DATA[1]	PIN_E31	GMII and MII receive data[1]	1.8V
HPS_ENET_RX_DATA[2]	PIN_G29	GMII and MII receive data[2]	1.8V
HPS_ENET_RX_DATA[3]	PIN_H28	GMII and MII receive data[3]	1.8V
HPS_ENET_RX_CLK	PIN_G28	GMII and MII receive clock	1.8V
HPS_ENET_MDIO	PIN_K31	Management Data	1.8V
HPS_ENET_MDC	PIN_B28	Management Data Clock Reference	1.8V
HPS_ENET_TX_CLK	PIN_F31	GMII Transmit Clock	1.8V

2.12 1x6 GPIO Header

The Apollo S10 board provides a 1x6 pin GPIO header to expand the HPS I/O of Stratix 10 FPGA (See **Figure 2-17**). In addition to having 4 pins connected to HPS I/O, this header also provides 3.3v power and GND pin. Users can configure and use these I/O for applications through HPS.

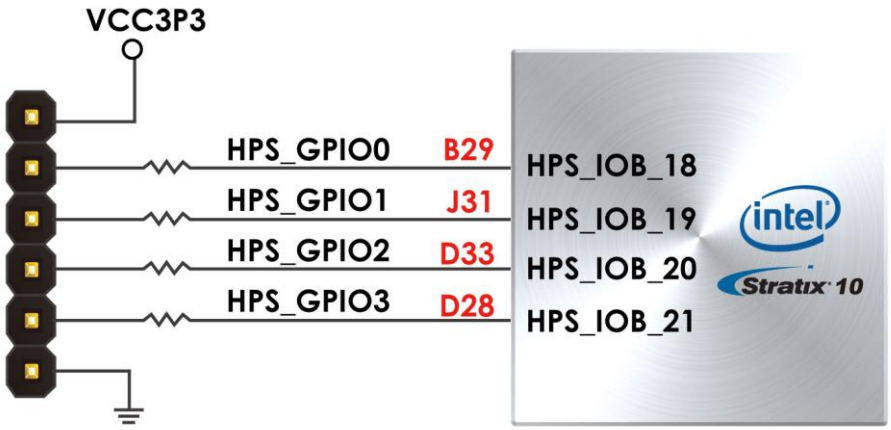


Figure 2-17 Connection between the 1x6 header and Stratix 10 FPGA

Table 2-27 Pin Assignment of USB OTG PHY

Signal Name	FPGA Pin No.	Description	I/O Standard

HPS_GPIO[0]	PIN_B29	HPS GPIO0	1.8V
HPS_GPIO[1]	PIN_J31	HPS GPIO1	1.8V
HPS_GPIO[2]	PIN_D33	HPS GPIO2	1.8V
HPS_GPIO[3]	PIN_D28	HPS GPIO3	1.8V

2.13 System Status Interface

As shown in **Figure 2-18**, the Apollo S10 board provides several sensors to monitor the status of the board, such as FPGA temperature, board power monitor, and fan speed status. These interfaces are connected to the System MAX FPGA on the board. The board management logic (Dashboard) in the system MAX FPGA will monitor these status and perform corresponding control according to the status. For example, when the temperature of the FPGA increases, the system will automatically increase the fan speed to reduce the temperature. When the temperature of the FPGA continues to exceed the working range (such as a fan failure condition), the FPGA power will be cut to protect the board.

In addition, the board also provides USB to UART interface to connect with the System MAX, so that users can monitor the status of the board from the host through the UART interface. See chapter 8 for details.

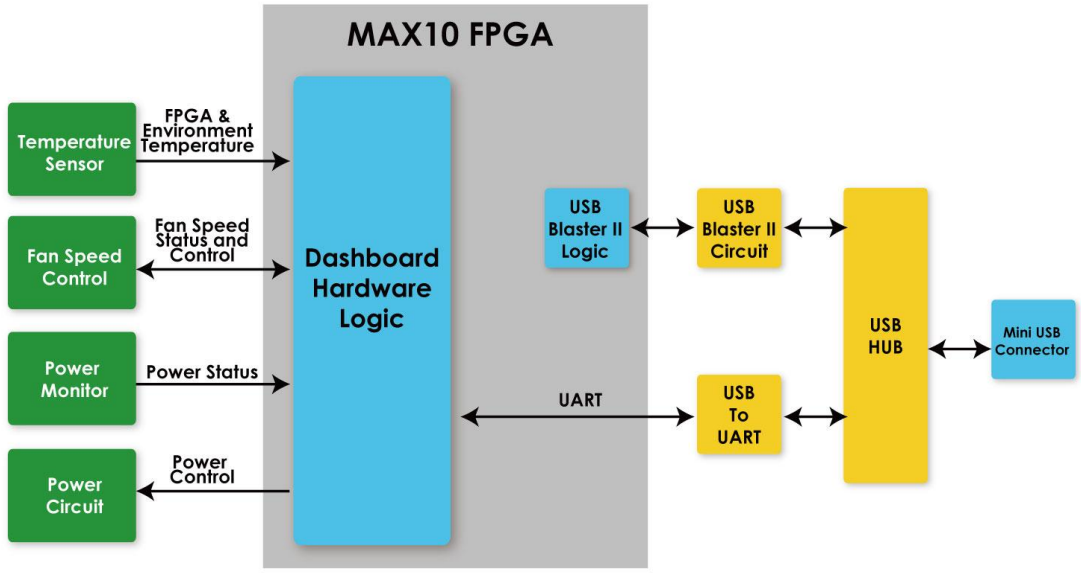


Figure 2-18 Block diagram of the system status interface

Chapter 3

System Builder

This chapter describes how users can create a custom design project for the FPGA board from a software tool named System Builder.

3.1 Introduction

The System Builder is a Windows based software utility. It is designed to help users create a Quartus Prime project for the FPGA board within minutes. The Quartus Prime project files generated include:

- Quartus Prime Project File (.qpf)
- Quartus Prime Setting File (.qsf)
- Top-Level Design File (.v)
- External PLL Controller (.v)
- Synopsis Design Constraints file (.sdc)
- Pin Assignment Document (.htm)

The System Builder not only can generate the files above, but can also provide error-checking rules to handle situation that are prone to errors. The common mistakes that users encounter are the following:

- Board damaged for wrong pin/bank voltage assignment.
- Board malfunction caused by wrong device connections or missing pin counts for connected ends.
- Performance dropped because of improper pin assignments

3.2 General Design Flow

This section will introduce the general design flow to build a project for the FPGA board via the System Builder. The general design flow is illustrated in **Figure 3-1**.

Users should launch System Builder and create a new project according to their design requirements. When users complete the settings, the System Builder will generate two major files which include top-level design file (.v) and the Quartus Prime setting file (.qsf).

The top-level design file contains top-level Verilog wrapper for users to add their own design/logic. The Quartus Prime setting file contains information such as FPGA device type, top-level pin assignment, and I/O standard for each user-defined I/O pin.

Finally, the Quartus Prime programmer must be used to download SOF file to the FPGA board using JTAG interface.

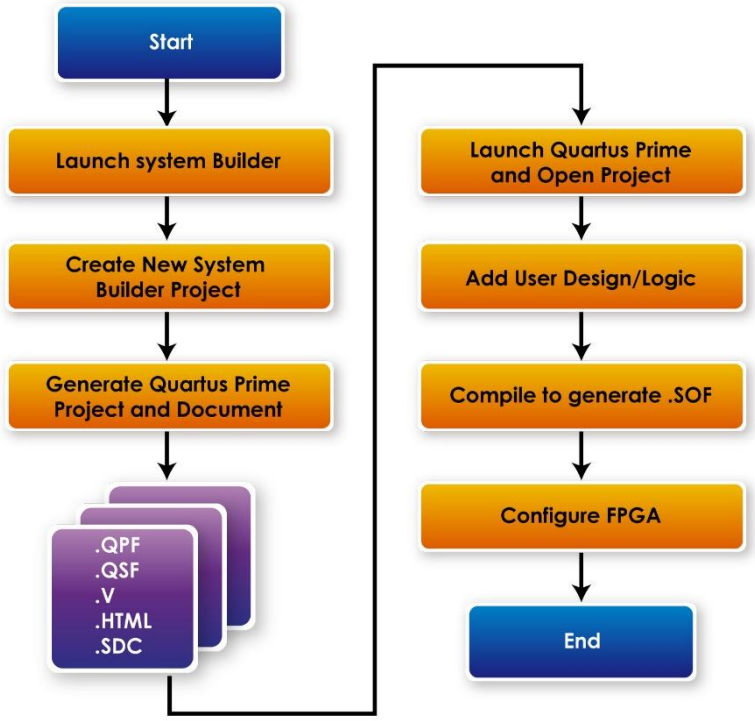


Figure 3-1 the general design flow of building a project

3.3 Using System Builder

This section provides detailed procedures on how the System Builder is used.

■ Install and Launch the System Builder

The System Builder is located under the directory: **"Tools\SystemBuilder"** in the System CD. Users can copy the entire folder to the host computer without installing the utility. Please execute the SystemBuilder.exe on the host computer, as shown in **Figure 3-2**.

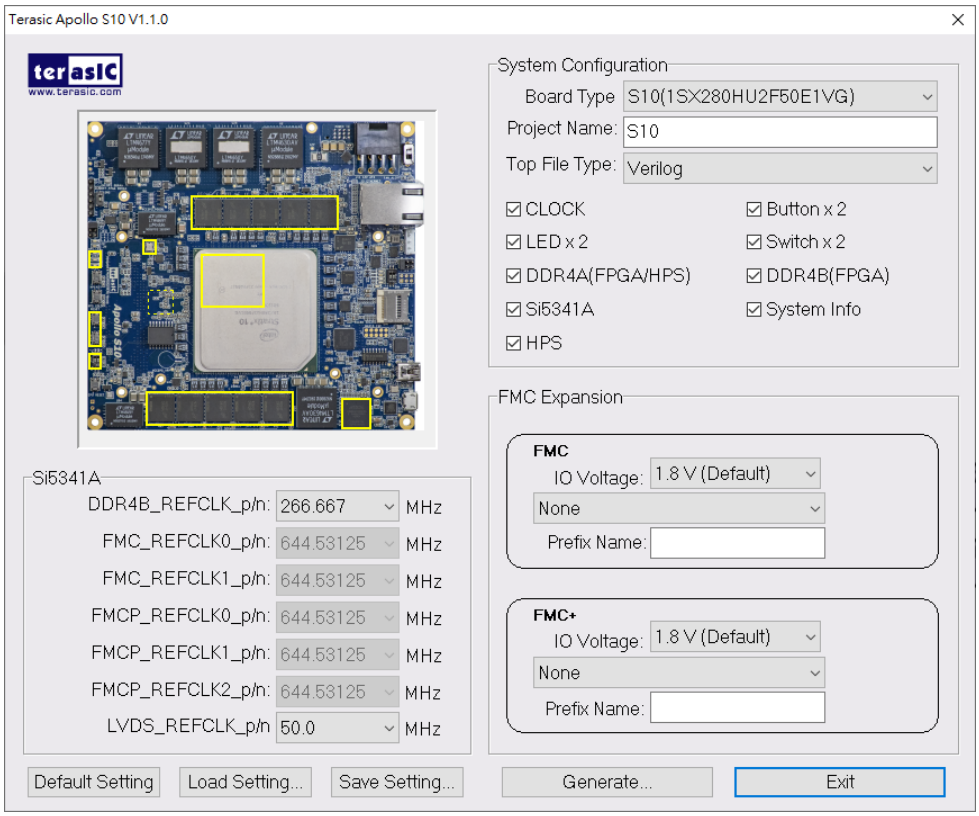


Figure 3-2 The System Builder window

■ Enter Project Name

The project name entered in the circled area as shown in **Figure 3-4**, will be assigned automatically as the name of the top-level design entry.

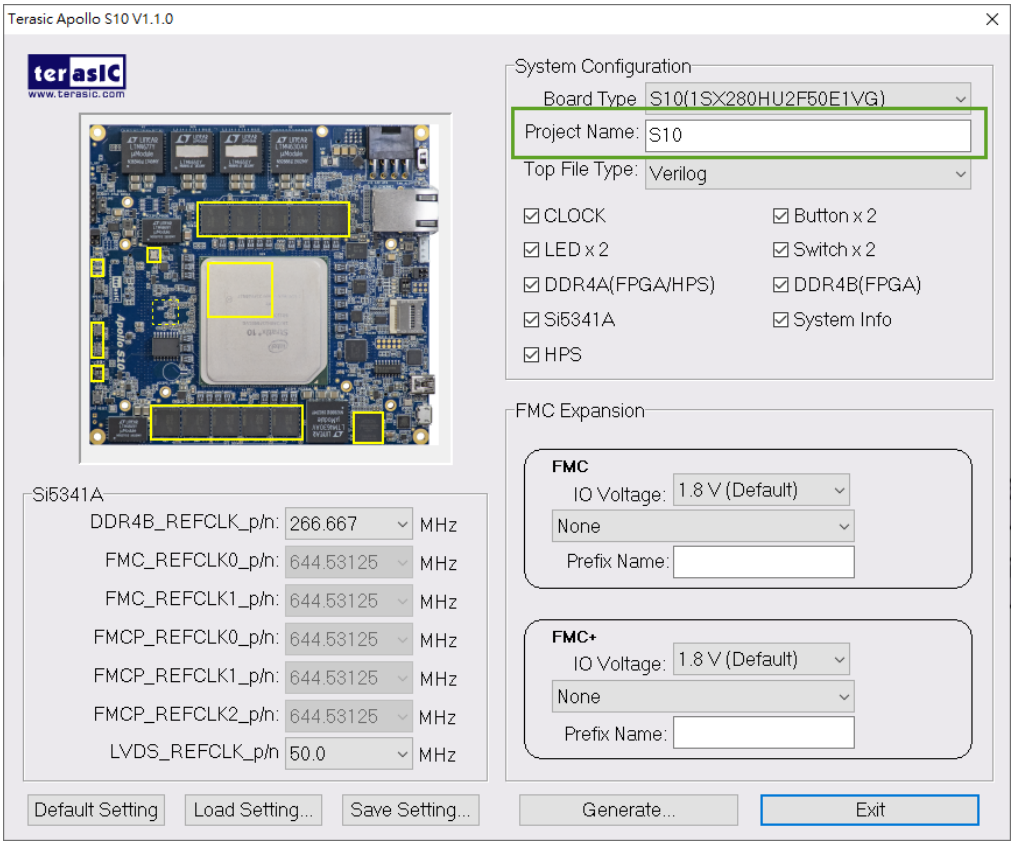


Figure 3-4 Project Name in the System Builder window

■ Select Top File Type

The system builder can generate Verilog or VHDL Quartus top file according to the users' requirements. Users can select their desired file type in the Top File Type list-box shown in **Figure 3-5**.

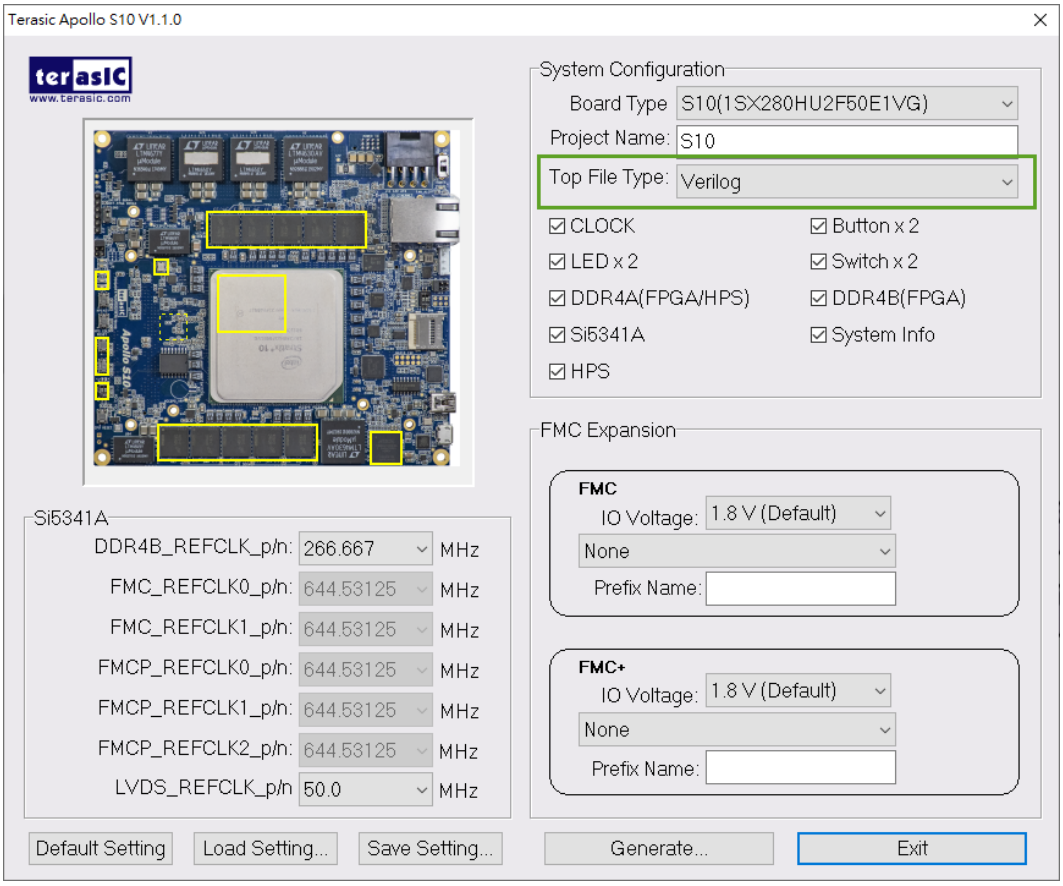


Figure 3-5 Top File Type in the System Builder window

■ System Configuration

Users are given the flexibility of enabling their choices of components connected to the FPGA under System Configuration, as shown in **Figure 3-6**. Each component of the FPGA board is listed to be enabled or disabled according to users' needs. If a component is enabled, the System Builder will automatically generate the associated pin assignments including its pin name, pin location, pin direction, and I/O standards.

Note: The pin assignments for some components (e.g. DDR4) require associated controller codes in the Quartus project or it would result in compilation error. Hence please do not select them if they are not needed in the design. To use the DDR4 controller, please refer to the DDR4 SDRAM demonstration in Chapter **?**.

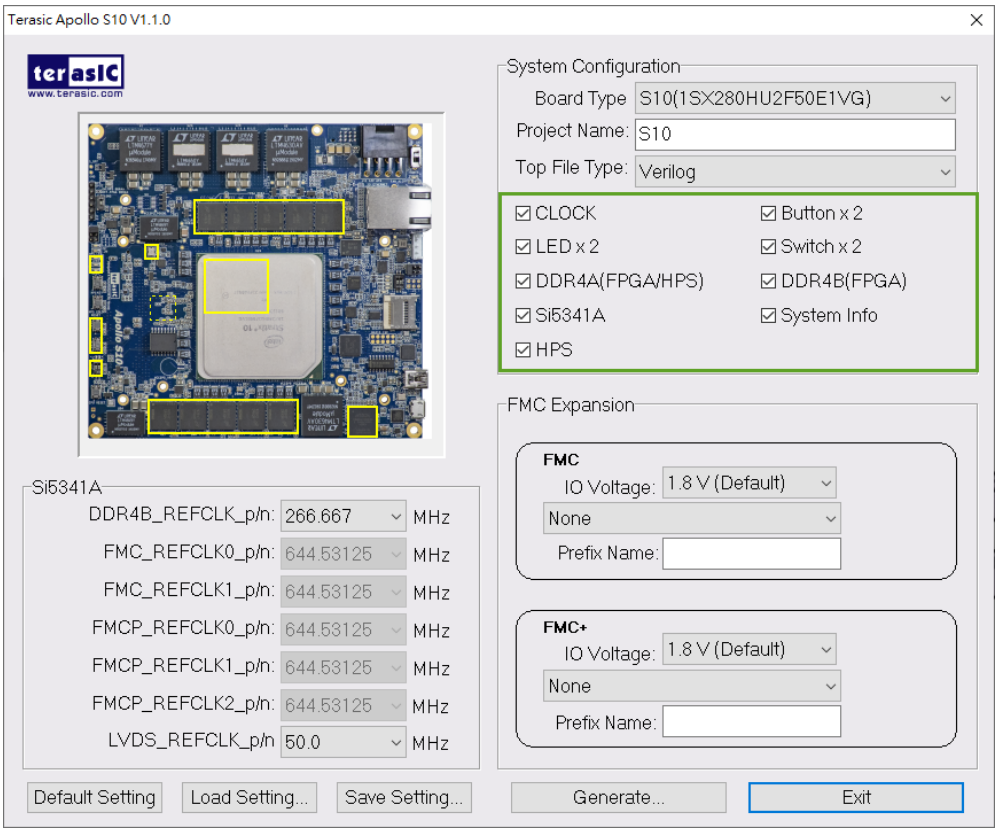


Figure 3-6 System Configuration Group

■ Programmable Clock Generator

There are two external clock generator Si5341A on-board that provide reference clocks for the following signals:

- DDR4B_REFCLK
- FMC_REFCLK0
- FMC_REFCLK1
- FMCP_REFCLK0
- FMCP_REFCLK1
- FMCP_REFCLK2
- DDR4C_REFCLK
- LVDS_REFCLK

To use these clock, users can select the desired frequency on the Si5341A, as shown in **Figure 3-7**. DDR4 or FMC/FMC+ must be checked before users can start to specify the desired frequency in the programmable oscillators.

As the Quartus project is created, System Builder automatically generates the associated controller according to users' desired frequency in Verilog which facilitates users' implementation as no additional control code is required to configure the programmable oscillator.

Note: If users need to dynamically change the frequency, they would need to modify the generated control code themselves.

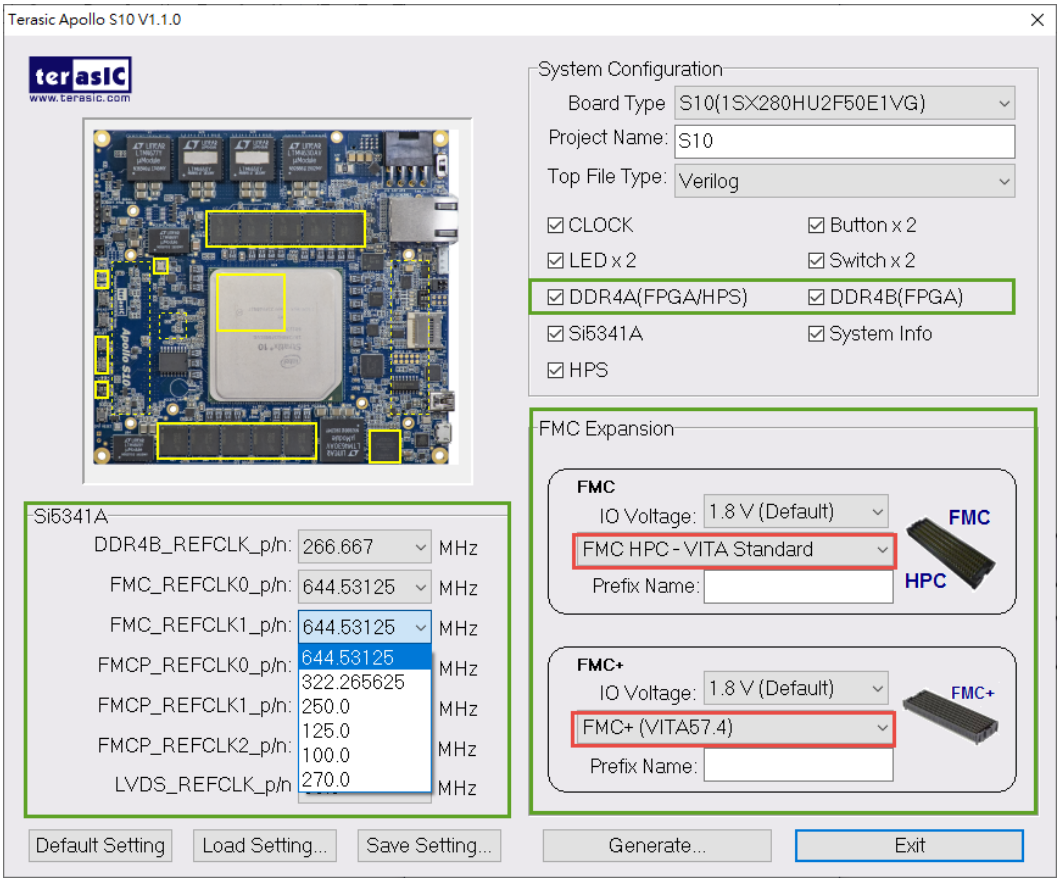


Figure 3-7 External programmable oscillators

■ Project Setting Management

The System Builder also provides functions to restore default DDR4/QDR-II+/QDR-IV setting, load a pre-saved setting, and save board configuration file, as shown in **Figure 3-8**. Users can save the current board configuration information into a .cfg file and load it into the System Builder later.

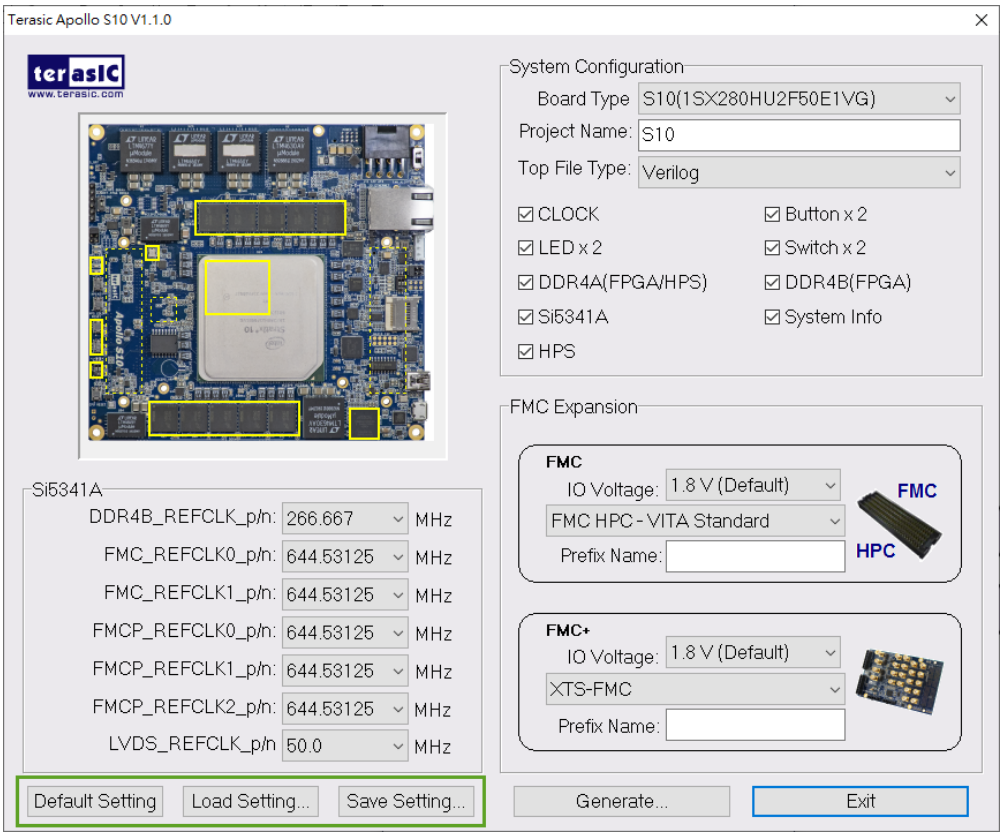


Figure 3-8 Project Settings

■ Project Generation

When users press the Generate button, the System Builder will generate the corresponding Quartus Prime files and documents as listed in the **Table 3-1** directory specified by the user.

Table 3-1 Files generated by the System Builder

No.	Filename	Description
1	<Project name>.v or <Project name>.vhdl	Top Level Verilog/VHDL File for Quartus Prime
2	si5340_controller (*)	Si5341A Clock Generator Controller IP
3	<Project name>.qpf	Quartus Prime Project File
4	<Project name>.qsf	Quartus Prime Setting File
5	<Project name>.sdc	Synopsis Design Constraints File for Quartus Prime

6	<Project name>.htm	Pin Assignment Document

(*) The si5340_controller is a folder which contains the Verilog files for the configuration of Si5341A clock generator chips.

Users can add custom logic into the project and compile the project in Quartus Prime to generate the SRAM Object File (.sof).

Note that when the Si5341A clock frequency in the System Builder tool is **modified**, the top-level file in the Quartus project will show the Si5341A controller IP and associated setting as shown in below. If nothing is changed to keep the default setting in the System Builder, the top-level file of the generated Quartus project will not show these components.

```
//=======================================================
//  Configure SI5341A
//=======================================================
`define XCVR_REF_644M53125      4'h0
`define XCVR_REF_322M265625     4'h1
`define XCVR_REF_250M           4'h2
`define XCVR_REF_125M           4'h3
`define XCVR_REF_100M           4'h4
`define XCVR_REF_270M           4'h5  // for Displayport

`define MEM_REF_300M      4'h0  // for DDR4 2400 MT/s
`define MEM_REF_266M667   4'h1  // for DDR4 2133 MT/s
`define MEM_REF_233M333   4'h2  // for DDR4 1866 MT/s
`define MEM_REF_166M667   4'h3  // for DDR4 2666 MT/s

`define LVDS_REF_50M      4'h0  // ref clock for LVDS IP
`define LVDS_REF_100M     4'h1  // ref clock for LVDS IP

wire si5341a_controller_start;
assign si5341a_controller_start = ~BUTTON[0];
wire si5341a_config_done;


//  Configure SI5341
S10_SI5341A_CONFIG si5341a_controller(
    .iCLK(CLK_50_B3C),
    .iRST_n(1'b1),
    .iStart(si5341a_controller_start),
    .iDDR4B_REFCLK(`MEM_REF_266M667),
    .iFMC_REFCLK0(`XCVR_REF_644M53125),
    .iFMC_REFCLK1(`XCVR_REF_644M53125),
    .iFMCP_REFCLK0(`XCVR_REF_322M265625),
    .iFMCP_REFCLK1(`XCVR_REF_644M53125),
    .iFMCP_REFCLK2(`XCVR_REF_644M53125),
    .iLVDS_REFCLK(`LVDS_REF_50M),
    .I2C_CLK(SI5341A_I2C_SCL),
    .I2C_DATA(SI5341A_I2C_SDA),
    .oPLL_REG_CONFIG_DONE(si5341a_config_done)
);
```

The following clock information also be automatically added in .sdc file.

```
#**************************************************************
# Create Clock
#**************************************************************
create_clock -period "100.000000 MHz" [get_ports CLK_100_B3I]
create_clock -period "50.000000 MHz" [get_ports CLK_50_B2F]
create_clock -period "50.000000 MHz" [get_ports CLK_50_B2L]
create_clock -period "50.000000 MHz" [get_ports CLK_50_B3C]
create_clock -period "50.000000 MHz" [get_ports CLK_50_B3I]
create_clock -period "644.531250 MHz" [get_ports LVDS_REFCLK_p]
create_clock -period "644.531250 MHz" [get_ports FMC_REFCLK0_p]
create_clock -period "644.531250 MHz" [get_ports FMC_REFCLK1_p]
create_clock -period "322.265625 MHz" [get_ports FMCP_REFCLK0_p]
create_clock -period "644.531250 MHz" [get_ports FMCP_REFCLK1_p]
create_clock -period "644.531250 MHz" [get_ports FMCP_REFCLK2_p]
create_clock -period "266.666992 MHz" [get_ports DDR4A_REFCLK_p]
create_clock -period "266.666656 MHz" [get_ports DDR4B_REFCLK_p]
```

If the dynamic configurations for the Si5341A clock generators are required, users need to modify the code according to users' desired behavior.

Chapter 4

Dashboard GUI

The Apollo S10 Dashboard GUI is a board management system. This system is connected from the Host to the system max on the Apollo S10 board through the UART interface, and reads various status on the board (See section 2.13 for detailed). The reported status includes FPGA/Board temperature, fan speed, FPGA core power and 12V input power. **Figure 4-1** shows the block diagram of the Apollo S10 Dashboard..

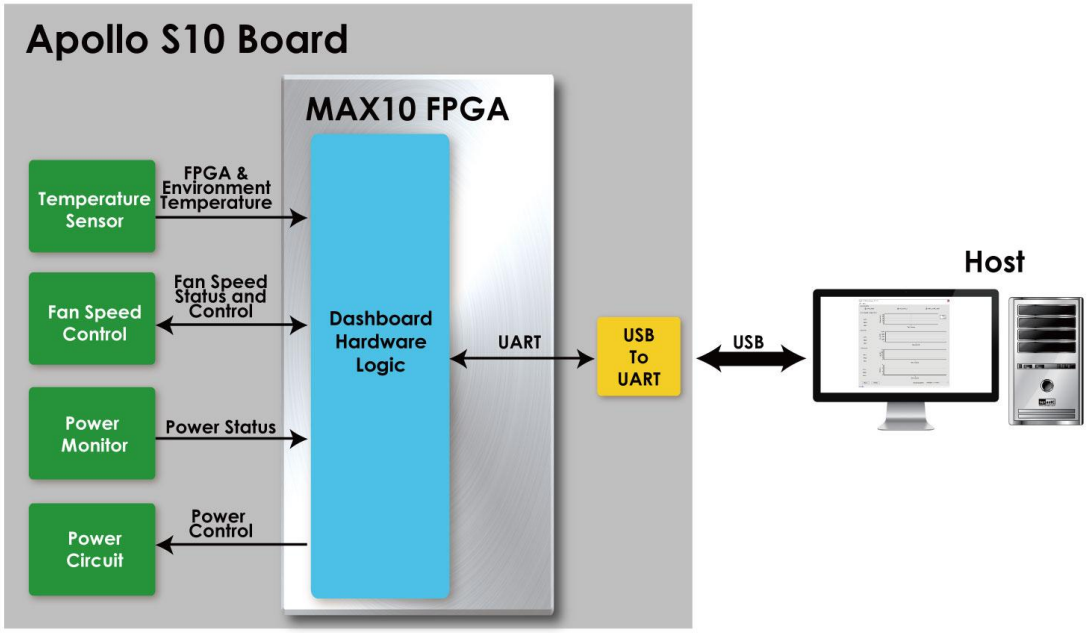


Figure 4-1 Block Diagram of the Apollo S10 Dashboard

4.1 Driver Installed on Host

To use the dashboard system, users need to install the USB to UART driver on the host first, so that user can establish a connection with the Apollo S10 board. This section will describe how to install USB to UART driver on the windows OS host.

■ USB to UART driver location

Users can find it from the path: Tool\dashboard_gui\Driver in the Apollo S10 system CD and copy it to the host PC.

■ Connection Setting

1. Connect the USB Mini USB connector of the Apollo S10 board to the host PC USB port through mini USB cable.
2. Connect power to the Apollo S10 board.
3. Power on the Apollo S10 board.

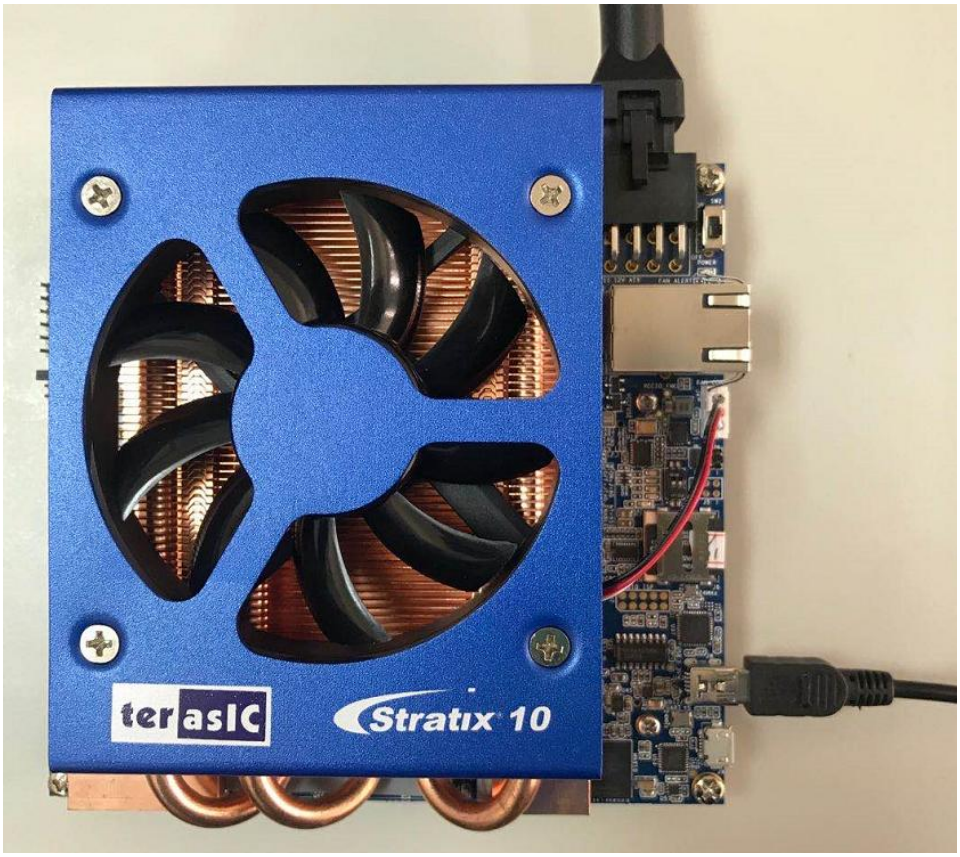


Figure 4-2 Connection setup for using dashboard system

■ Install Driver

When connect the Apollo S10 board to the host PC. As shown in **Figure 4-3**, one USB to UART device is shown in PC Device Manager.

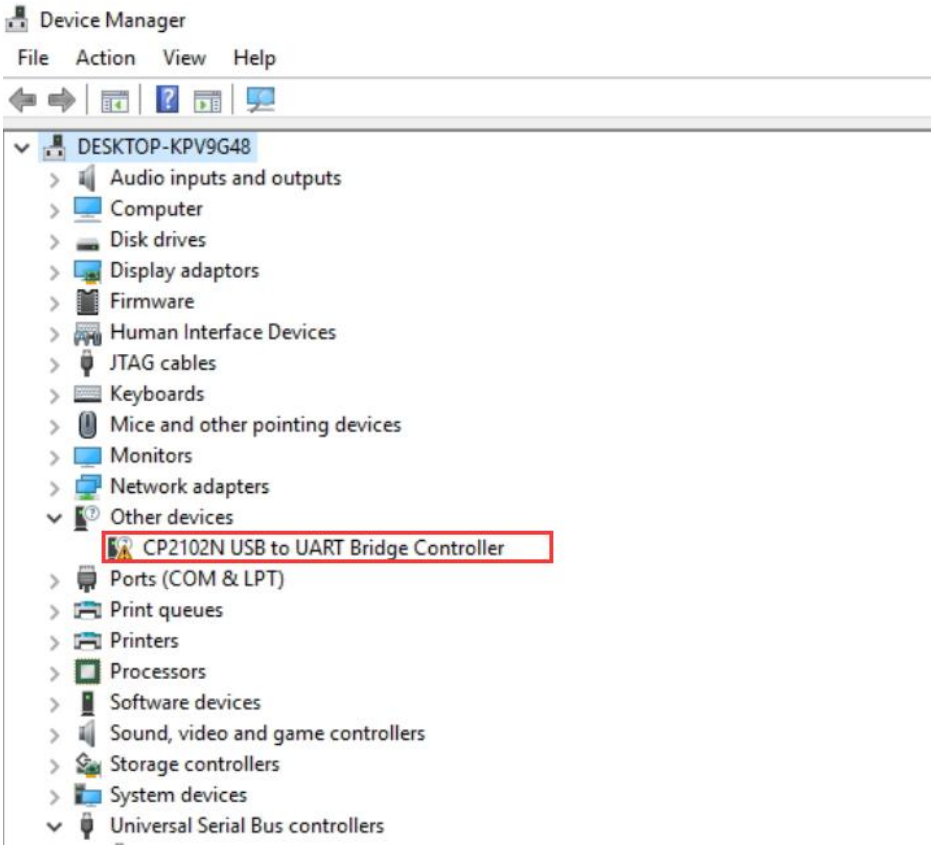


Figure 4-3 Uninstalled USB to UART device

As described in previous steps, copy the device driver to the host PC and install it, as shown in **Figure 4-4.** Please note that the COM Port number is different in different host PC.

Figure 4-4 Install USB to UART driver

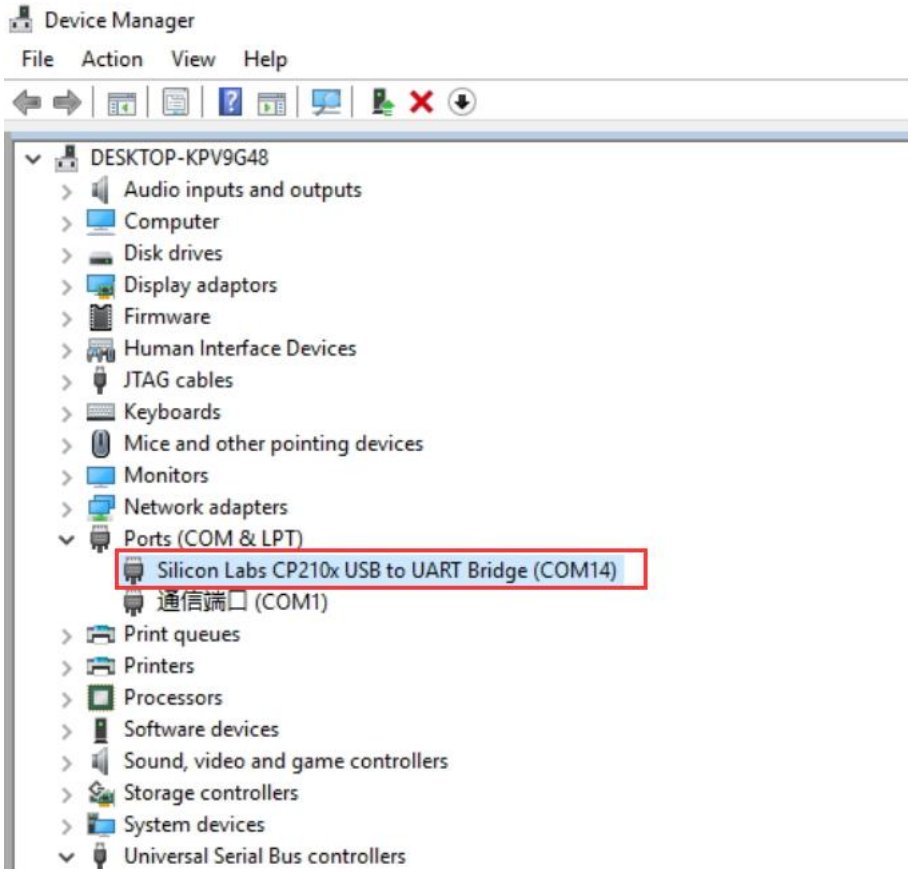


Figure 4-5 The USB to UART device after driver is installed successfully

4.2 Run Dashboard GUI

■ Dashboard GUI software location

Users can find it from the path: Tool\dashboard_gui\Dashboard.exe in the Apollo S10 system CD and copy it to the host PC.

Execute the Dashboard.exe, a window will show as **Figure 4-6**. It will describe the detail functions as below.

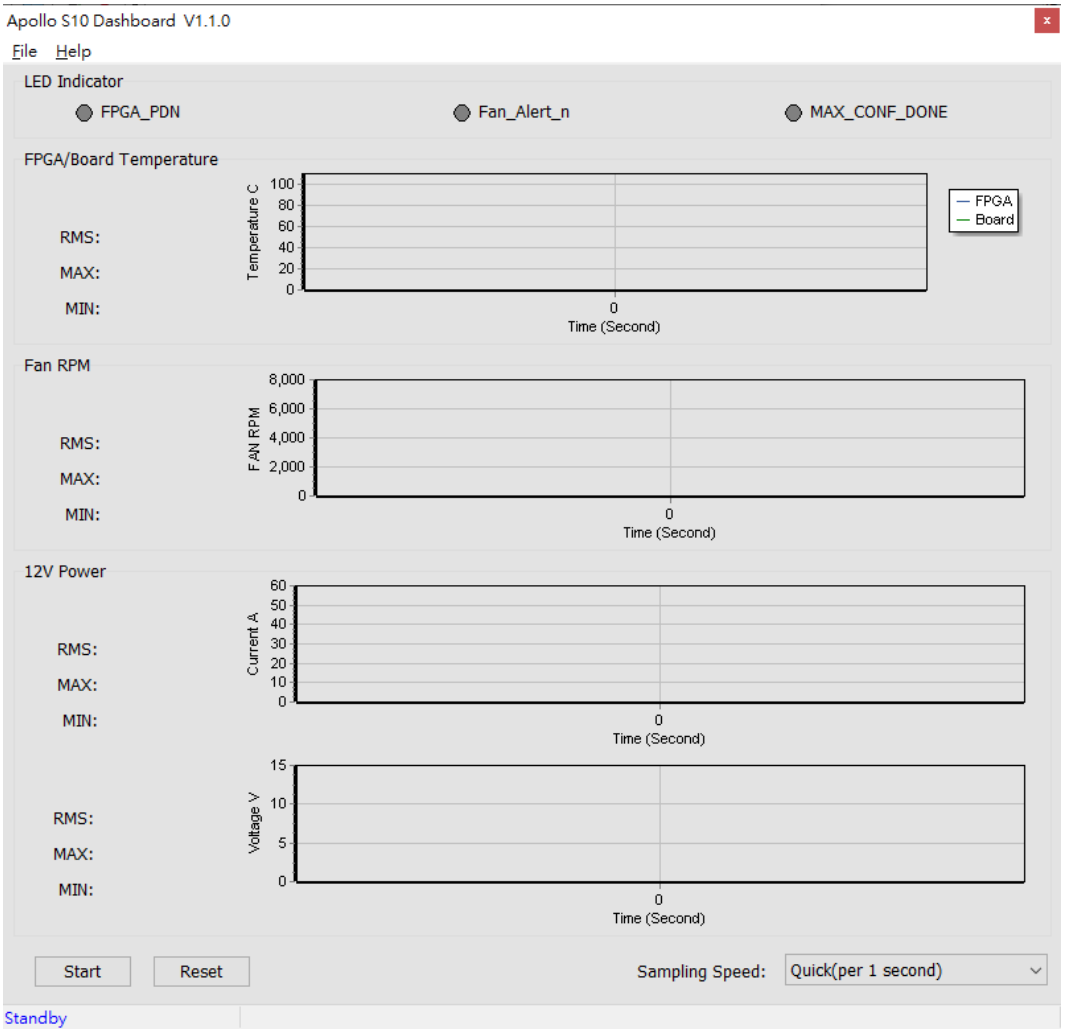


Figure 4-6 Dashboard GUI

■ Dashboard GUI function introduction

- **Start/Stop**: As shown in **Figure 4-7**, there is a Start button at the bottom-left of the GUI window. Click it to run the program (Start will change to Stop), it will show the Apollo S10 board status. Users can press Stop button to stop the status data transmission and display.
- **Reset Button**: Press this button to clear the historical data shown in GUI, and record the data again.

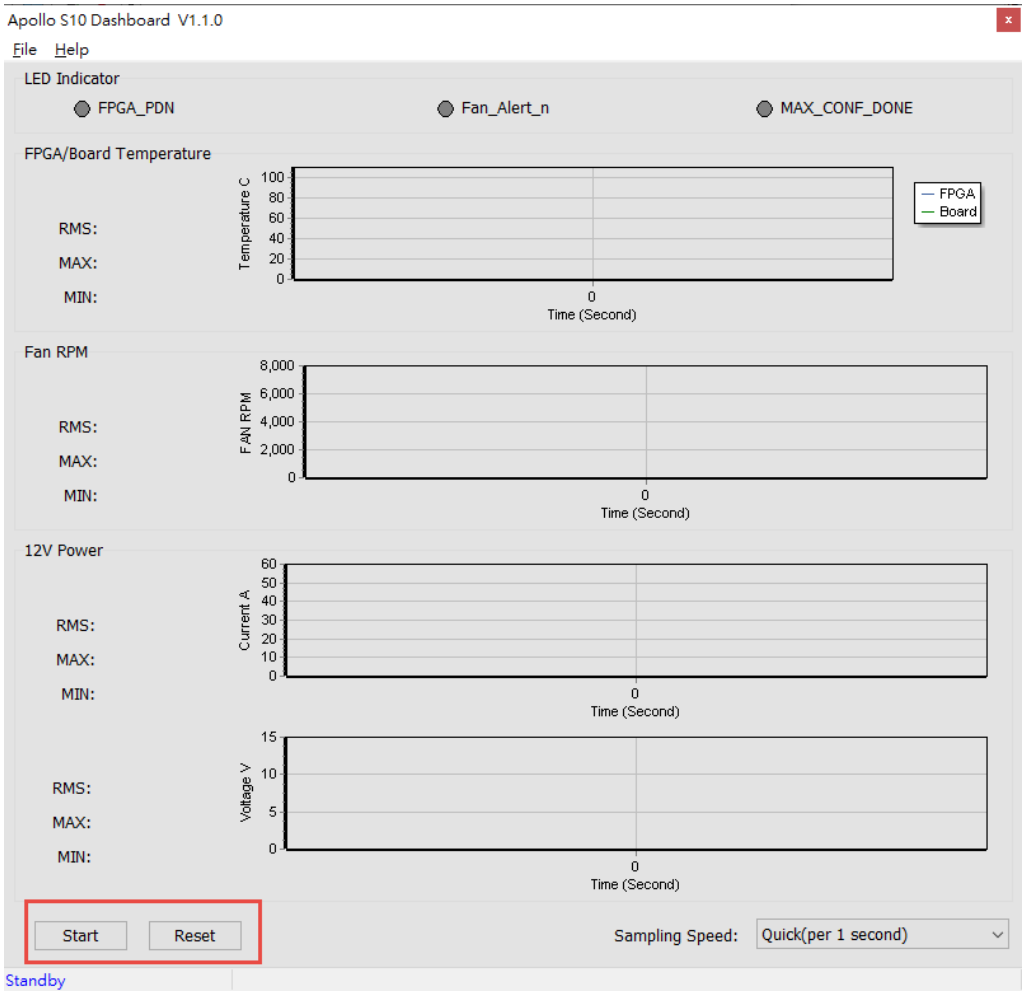


Figure 4-7 Start and Reset button

- **FPGA Status**: As shown in **Figure 4-8**, it will show the status LED number on the Apollo S10 board. For these LEDs function, please refer to section 2.2. Note that "**MAX_CONF_DONE**" stands for FPGA configure done status. There is no LED on Apollo S10 board to display status. When this status is shown in green on the GUI, it means that FPGA configuration has been completed.

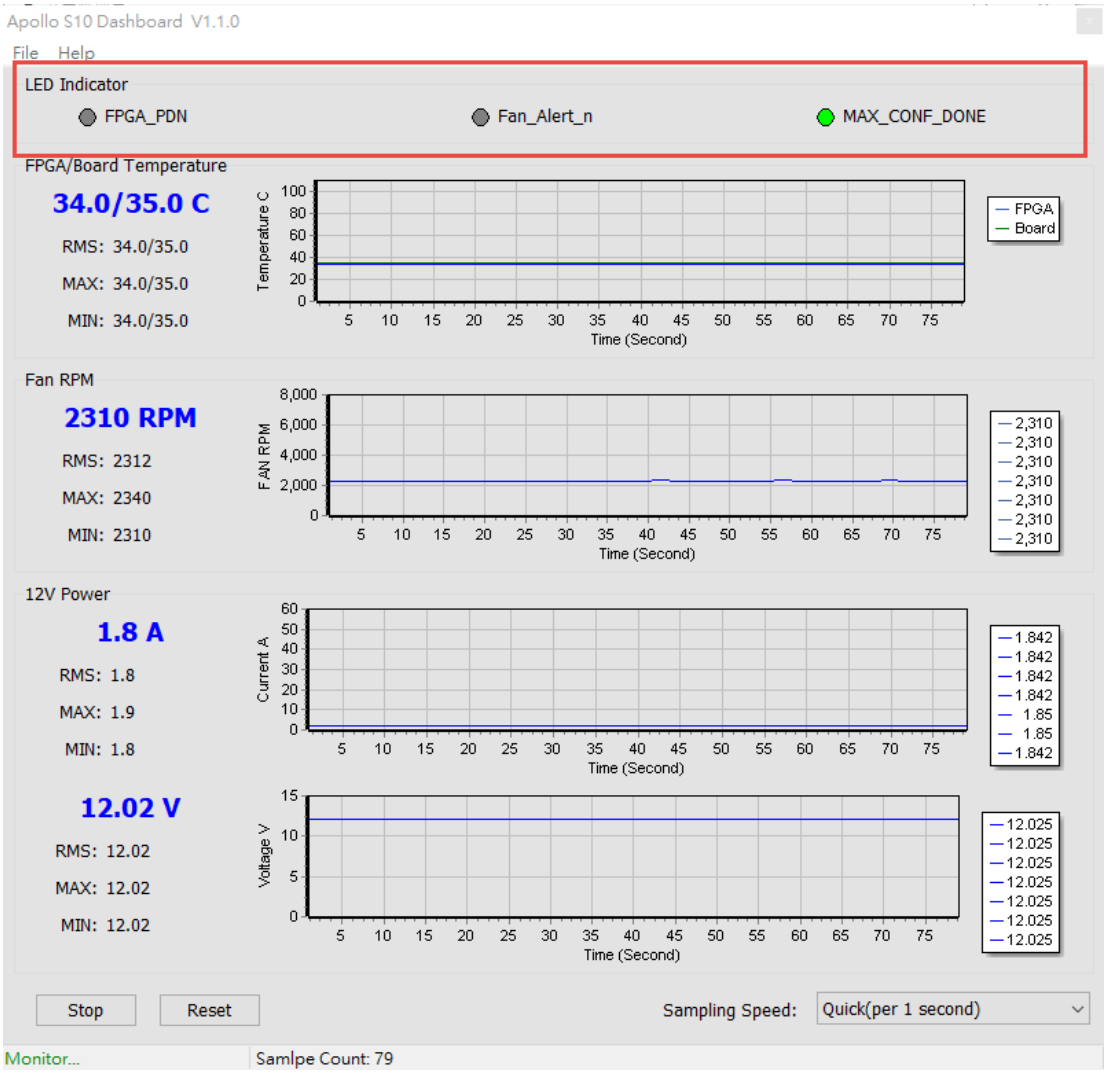


Figure 4-8 FPGA Status section

- **FPGA/Board Temperature**: The Dashboard GUI will real-time show the fan speed, Apollo S10 board ambient and FPGA temperature. Users can know the board temperature in time. The information will be refreshed per 1 second, and displays through diagram and number, as shown in **Figure 4-9**.

Figure 4-9 Temperature section

- **Fan RPM**: It displays the real-time speed of the fan on the Apollo S10 board, as shown in **Figure 4-10**.

Figure 4-10 FAN RPM section

- **12V/Core Power monitor**: It displays the real-time 12V/Core Power (0.9V) voltage and consumption current on the Apollo S10 board, as shown in **Figure 4-11**.

Figure 4-11 Power Monitor Section

- **Sampling Speed**: It can change interval time that the Dashboard GUI sample the board status. Users can adjust it to 1s/10s/1min/Full Speed (0.1s) to sample the board status, as shown in **Figure 4-12** and **Figure 4-13**.

Figure 4-12 Sampling Speed section

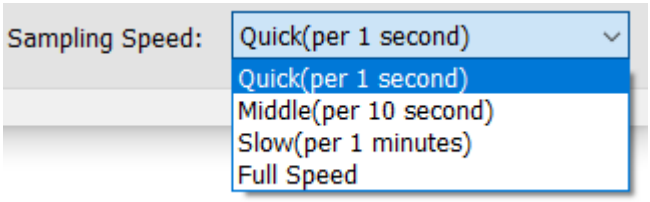


Figure 4-13 Options of Sampling Speed

- **Board Information**: There is a File page on the upper left of the Dashboard GUI program window, click the Board Information to get the current software version and the Apollo S10 board version, as shown in **Figure 4-14**.

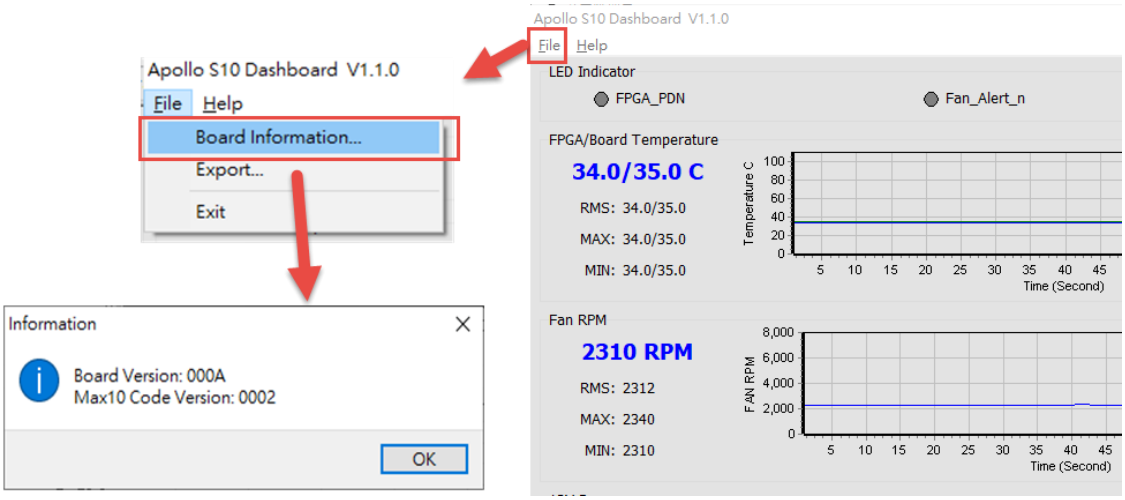


Figure 4-14 Board Information

- **Log File**: On the upper left of the Dashboard GUI program window, click the Export in the File page to save the board temperature, fan speed and voltage data in .csv format document, as shown in **Figure 4-15** and **Figure 4-16**.

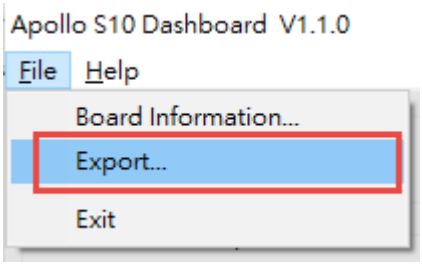


Figure 4-15 Export the log file

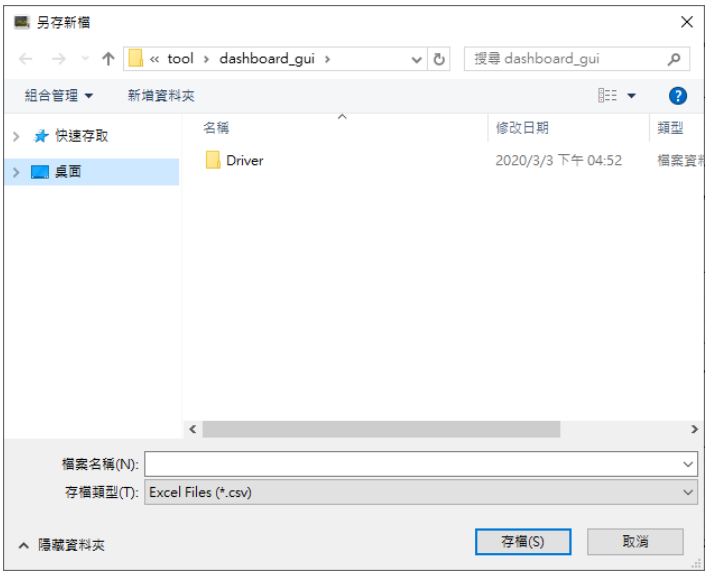


Figure 4-16 Export the log file in .csv format

Chapter 5

Additional Information

5.1 Getting Help

Here are the addresses where you can get help if you encounter problems:

■ Terasic Technologies

9F., No.176, Sec.2, Gongdao 5th Rd,
East Dist, HsinChu City, Taiwan, 30070
Email: support@terasic.com
Web: www.terasic.com
Apollo S10 Web: Apollo S10.terasic.com

■ Revision History

Date	Version	Changes
2020.03	First publication	
2020.04	V1.1	Modify overview and add Figure 1-7
2020.04	V1.2	Add Figure 2-9 and 2-11 pin out table of the FMC and FMC+ connector
2020.05	V1.3	Add section 1.5 The Purpose of Screw Set