NVIDIA Jetson Xavier NX

Design Guide

DG-09693-001_v0.91 | February 2020
PRELIMINARY INFORMATION

Document History

DG-09693-001_v0.91

Version	Date	Description of Change
0.9	November 6, 2019	Preliminary Information
0.91	February 7, 2020	• Updated Table 2-2 • Removed >1 min recommendation for power rail charging • Updated Table 3-1 • Added PCIe x1 interface support for Root Port operation • Updated Table 4-1 • Corrected controller # for PCIE0 pins, updated x1 PCIe to come from Xavier PEX Lane 11, and updated PEX lane changes in Table 4-2 • Updated Table 4-3 • Updated USB2 pin numbers and removed 4.7uF cap on VDD_5V_USB to match P3509 implementation in Figure 4-1 • Moved PCIe x1 to Lane 11, corrected PCIE0_TX3 and RX0 pin numbers, corrected x4 controller, and removed AC cap values on TX lines in Figure 4-8 • Corrected controller # or x4 PCIe I/F, removed AC cap values on TX lines, and corrected PCIE0_TX3 and RX0 pin numbers in Figure 4-9 • Updated PCIe controller numbers in Table 4-10 • Changed pull ups on RST and INT to go to 3.3V and added level shifter to INT to SoC in Figure 4-10 • Updated ethernet connections in Table 4-13 • Updated DP_AUX_CH0_N and DP_AUX_CH0_N pin type since the interface can be used for HDMI in Table 5-1 • Updated with 100Kohm PD and series resistors on DPx_HPD on connector side of level shifter in Figure 5-1 • Updated DPx_HPD pin termination description in Table 5-4 • Updated notes to Table 7-1 • Updated notes to Table 8-1 • Updated Figure 8-1 with Jetson module • Corrected PM3_PWM3 to GP_PWM6 in the fan section, Section 9.5 • Corrected the Xavier signal connected GPIO14 pin in Table 9-12 and Figure 9-7 • Updated TX and RX to match module name in Table 9-13 • Updated checklist Table 12-1 • Updated Table 13-1 • Updated Table 13-2

Table of Contents

List of Figures

List of Tables

Chapter 1. Introduction

This design guide contains recommendations and guidelines for engineers to follow to create a product that is optimized to achieve the best performance from the common interfaces supported by the NVIDIA® Jetson Xavier™ NX System-on-Module (SOM).

This design guide provides detailed information on the capabilities of the hardware module, which may differ from supported configurations by provided software. Refer to software release documentation for information on supported capabilities.

1.1 References

Refer to the following list of documents or models for more information. Use the latest revision of all documents.

- Jetson Xavier NX Data Sheet
- Xavier (SoC) Technical Reference Manual
- Jetson Xavier NX Pinmux
- Jetson Xavier NX Thermal Design Guide
- Jetson Xavier NX SCL (Supported Component List)

1.2 Abbreviations and Definitions

Table 1-1 lists the abbreviations that may be used throughout this design and guide and their definitions.

Table 1-1. Abbreviations and Definitions

Abbreviation	Definition
CAN	Controller Area Network
CEC	Consumer Electronic Control
CSI	Camera Serial Interface
Diff	Differential
DP	DisplayPort

Abbreviation	Definition
eDP	Embedded DisplayPort
ESD	Electrostatic Discharge
eMMC	Embedded MMC
EMI	Electromagnetic Interference
FET	Field Effect Transistor
GPIO	General Purpose Input Output
HDCP	High-bandwidth Digital Content Protection
HDMI	High Definition Multimedia Interface
I2C	Inter IC Interface
I2S	Inter IC Sound Interface
LCD	Liquid Crystal Display
LDO	Low Dropout (voltage regulator)
LPDDR4x	Low Power Double Data Rate DRAM, Fourth generation
MDI	Medium-Dependent Interface
MIL	1/1000th of an inch
MIPI	Mobile Industry Processor Interface
mm	Millimeter
PCIe	Peripheral Component Interconnect Express interface
PCM	Pulse Code Modulation
PHY	Physical Interface (i.e. USB PHY)
ps	Pico-Seconds
PMIC	Power Management Integrated Circuit
RJ45	8P8C modular connector used in Ethernet and other data links
RTC	Real Time Clock
SD Card	Secure Digital Card
SDIO	Secure Digital I/O Interface
SE	Single-Ended
SPI	Serial Peripheral Interface
TMDS	Transition-minimized differential signaling
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

Chapter 2. Jetson Xavier NX

The Jetson Xavier NX resides at the center of the embedded system solution and includes:

- Power (PMIC/Regulators, etc.)
- DRAM (8 GB, 128-bit LPDDR4x)
- eMMC (16 GB)
- Gigabit Ethernet Controller
- Power Monitor
- QSPI NOR (32 MB – Boot device)

In addition, a wide range of interfaces are available at the main connector for use on the carrier board as shown in Table 2-1 and Figure 2-1.

Table 2-1. Jetson Xavier NX Interfaces

Category	Function		Category	Function
USB	USB 2.0 Interface (3x)		LAN	Gigabit Ethernet
	USB 3.1 (1x)		I2C	4x
PCIe	PCIe (x1 and x4)		UART	3x
Camera	CSI (3 x4 or 6 x2)		SPI	2x
	Control, Clock		CAN	1x
Display	HDMI/eDP/DP (2x)		Wi-Fi/BT/Modem	PCIe/UART/I2S, Control/handshake
	DP_AUX/HPD (2x), CEC (1x)		Fan	FAN PWM and Tach Input
Audio	I2S Interface (2x) and Clock		Debug	UART
	Master clock		System	Power Control, Reset, alerts
SD Card/SDIO	SD Card or SDIO Interface (1x)		Power	Main Input and battery back-up for RTC

Figure 2-1. Jetson Xavier NX Block Diagram

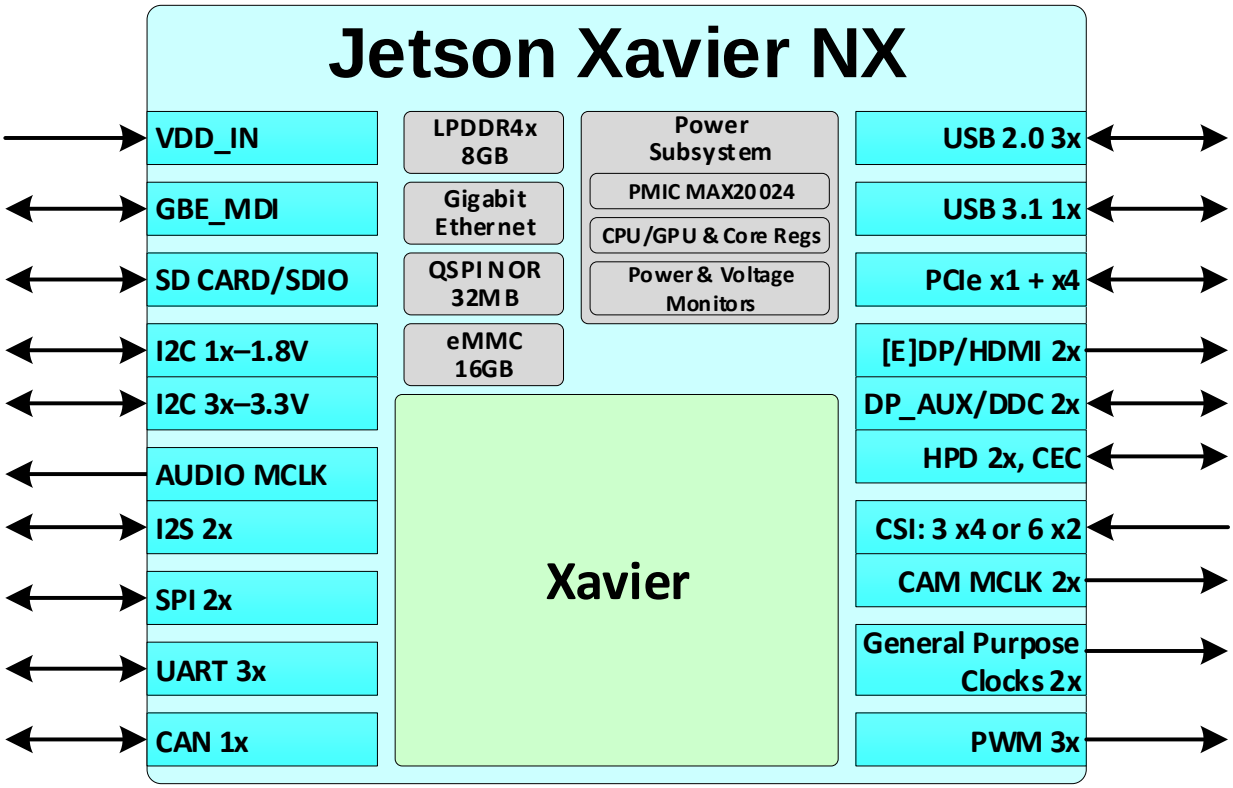


Table 2-2. Jetson Xavier NX Connector (260-Pin SO-DIMM) Pin Out Matrix

Module Signal Name	Pin #		Pin #	Module Signal Name
GND	1		2	GND
CSI1_D0_N	3		4	CSI0_D0_N
CSI1_D0_P	5		6	CSI0_D0_P
GND	7		8	GND
CSI1_CLK_N	9		10	CSI0_CLK_N
CSI1_CLK_P	11		12	CSI0_CLK_P
GND	13		14	GND
CSI1_D1_N	15		16	CSI0_D1_N
CSI1_D1_P	17		18	CSI0_D1_P
GND	19		20	GND
CSI3_D0_N	21		22	CSI2_D0_N
CSI3_D0_P	23		24	CSI2_D0_P
GND	25		26	GND
CSI3_CLK_N	27		28	CSI2_CLK_N
CSI3_CLK_P	29		30	CSI2_CLK_P
GND	31		32	GND
CSI3_D1_N	33		34	CSI2_D1_N
CSI3_D1_P	35		36	CSI2_D1_P
GND	37		38	GND
DP0_TXD0_N	39		40	CSI4_D2_N
DP0_TXD0_P	41		42	CSI4_D2_P
GND	43		44	GND
DP0_TXD1_N	45		46	CSI4_D0_N
DP0_TXD1_P	47		48	CSI4_D0_P
GND	49		50	GND
DP0_TXD2_N	51		52	CSI4_CLK_N
DP0_TXD2_P	53		54	CSI4_CLK_P
GND	55		56	GND
DP0_TXD3_N	57		58	CSI4_D1_N
DP0_TXD3_P	59		60	CSI4_D1_P
GND	61		62	GND
DP1_TXD0_N	63		64	CSI4_D3_N
DP1_TXD0_P	65		66	CSI4_D3_P
GND	67		68	GND
DP1_TXD1_N	69		70	DSI_D0_N
DP1_TXD1_P	71		72	DSI_D0_P
GND	73		74	GND
DP1_TXD2_N	75		76	DSI_CLK_N
DP1_TXD2_P	77		78	DSI_CLK_P
GND	79		80	GND
DP1_TXD3_N	81		82	DSI_D1_N
DP1_TXD3_P	83		84	DSI_D1_P
GND	85		86	GND
GPIO00	87		88	DP0_HPD
SPI0_MOSI	89		90	DP0_AUX_N
SPI0_SCK	91		92	DP0_AUX_P
SPI0_MISO	93		94	HDMI_CEC
SPI0_CS0*	95		96	DP1_HPD
SPI0_CS1*	97		98	DP1_AUX_N
UART0_TXD	99		100	DP1_AUX_P
UART0_RXD	101		102	GND
UART0_RTS*	103		104	SPI1_MOSI
UART0_CTS*	105		106	SPI1_SCK
GND	107		108	SPI1_MISO
USB0_D_N	109		110	SPI1_CS0*
USB0_D_P	111		112	SPI1_CS1*
GND	113		114	CAM0_PWDN
USB1_D_N	115		116	CAM0_MCLK
USB1_D_P	117		118	GPIO01
GND	119		120	CAM1_PWDN
USB2_D_N	121		122	CAM1_MCLK
USB2_D_P	123		124	GPIO02
GND	125		126	GPIO03
GPIO04	127		128	GPIO05
GND	129		130	GPIO06
PCIE0_RX0_N	131		132	GND

Module Signal Name	Pin #		Pin #	Module Signal Name
PCIE0_RX0_P	133		134	PCIE0_TX0_N
GND	135		136	PCIE0_TX0_P
PCIE0_RX1_N	137		138	GND
PCIE0_RX1_P	139		140	PCIE0_TX1_N
GND	141		142	PCIE0_TX1_P
CAN_RX	143		144	GND
KEY	KEY		KEY	KEY
CAN_TX	145		146	GND
GND	147		148	PCIE0_TX2_N
PCIE0_RX2_N	149		150	PCIE0_TX2_P
PCIE0_RX2_P	151		152	GND
GND	153		154	PCIE0_TX3_N
PCIE0_RX3_N	155		156	PCIE0_TX3_P
PCIE0_RX3_P	157		158	GND
GND	159		160	PCIE0_CLK_N
USBSS_RX_N	161		162	PCIE0_CLK_P
USBSS_RX_P	163		164	GND
GND	165		166	USBSS_TX_N
PCIE1_RX0_N	167		168	USBSS_TX_P
PCIE1_RX0_P	169		170	GND
GND	171		172	PCIE1_TX0_N
PCIE1_CLK_N	173		174	PCIE1_TX0_P
PCIE1_CLK_P	175		176	GND
GND	177		178	MOD_SLEEP*
PCIE_WAKE*	179		180	PCIE0_CLKREQ*
PCIE0_RST*	181		182	PCIE1_CLKREQ*
PCIE1_RST*	183		184	GBE_MDI0_N
I2C0_SCL	185		186	GBE_MDI0_P
I2C0_SDA	187		188	GBE_LED_LINK
I2C1_SCL	189		190	GBE_MDI1_N
I2C1_SDA	191		192	GBE_MDI1_P
I2S0_DOUT	193		194	GBE_LED_ACT
I2S0_DIN	195		196	GBE_MDI2_N
I2S0_FS	197		198	GBE_MDI2_P
I2S0_SCLK	199		200	GND
GND	201		202	GBE_MDI3_N
UART1_TXD	203		204	GBE_MDI3_P
UART1_RXD	205		206	GPIO07
UART1_RTS*	207		208	GPIO08
UART1_CTS*	209		210	CLK_32K_OUT
GPIO09	211		212	GPIO10
CAM_I2C_SCL	213		214	FORCE_RECOVERY*
CAM_I2C_SDA	215		216	GPIO11
GND	217		218	GPIO12
SDMMC_DAT0	219		220	I2S1_DOUT
SDMMC_DAT1	221		222	I2S1_DIN
SDMMC_DAT2	223		224	I2S1_FS
SDMMC_DAT3	225		226	I2S1_SCLK
SDMMC_CMD	227		228	GPIO13
SDMMC_CLK	229		230	GPIO14
GND	231		232	I2C2_SCL
SHUTDOWN_REQ*	233		234	I2C2_SDA
PMIC_BBAT	235		236	UART2_TXD
POWER_EN	237		238	UART2_RXD
SYS_RESET*	239		240	SLEEP/WAKE*
GND	241		242	GND
GND	243		244	GND
GND	245		246	GND
GND	247		248	GND
GND	249		250	GND
VDD_IN	251		252	VDD_IN
VDD_IN	253		254	VDD_IN
VDD_IN	255		256	VDD_IN
VDD_IN	257		258	VDD_IN
VDD_IN	259		260	VDD_IN

Legend Ground | Power

Chapter 3. Power

Power for the module is supplied on the VDD_IN pins and is nominally 5.0V (see the Jetson Xavier NX Data Sheet for supply tolerance and maximum current).

> **!** CAUTION: Jetson Xavier NX is not hot-pluggable. Before installing or removing the module, the main power supply (to VDD_IN pins) must be disconnected and adequate time allowed for the various power rails to fully discharge.

Table 3-1. Jetson Xavier NX Power and System Pin Description

Pin #	Module Pin Name	Xavier Pin Name	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
251 ↓ 260	VDD_IN	–	Main power – Supplies PMIC and other regulators	Main DC input	Input	5.0V		
235	PMIC_BBAT	–	PMIC Battery Back-up. Optionally used to provide back-up power for the Real-Time-Clock (RTC). Connects to Lithium Cell or super capacitor on Carrier Board. PMIC is supply when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power. Charging is enabled by default in software. If non-rechargeable battery is to be used, charging should be disabled.	Battery Back-up using coin cell.	Bidir	1.65V-5.5V		
214	FORCE_ RECOVERY*	SOC_GPIO00	Force Recovery strap pin	System	Input	CMOS – 1.8V	ST	pu
240	SLEEP/WAKE*	POWER_ON	Sleep/Wake. Configured as GPIO for optional use to indicate the system should enter or exit sleep mode.	System	Input	CMOS – 5.0V	ST	pd
233	SHUTDOWN_ REQ*	–	When driven/pulled low by the module, requests the carrier board shut down. ~5kΩ pull-up to VDD_IN (5V) on the module.	System	Output	Open Drain, 5.0V	–	–
237	POWER_EN	(PMIC EN0 through converter logic)	**Signal for module on/off: high level on, low level off. Connects to module PMIC EN0 through converter logic. POWER_EN is routed to a Schmitt trigger buffer on the module. A 100kΩ pulldown is also on the module.**	System	Input	Analog 5.0V	–	–
239	SYS_RESET*	SYS_RESET_IN_N	Module Reset. Reset to the module when driven low by the carrier board.	System	Bidir	Open Drain, 1.8V	JT_RST	z

Pin #	Module Pin Name	Xavier Pin Name	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
			Used as carrier board supply enable when pulled high by the module when module power sequence is complete. Used to ensure proper power on/off sequencing between module and carrier board supplies. 1kΩ pull-up to 1.8V on the module.					
178	MOD_SLEEP*	SOC_PWR_REQ	Module Sleep. When active (low), indicates module has gone to Sleep (SC7) mode.	HDMI termination pull-down FET control disable	Output	CMOS – 1.8V	ST	1
210	CLK_32K_OUT	(PMIC GPIO4 32K CLK Out)	Sleep/Suspend clock	Sleep/suspend clock for devices such as M.2 Key E	Output	CMOS – 1.8V	–	–

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

3.1 Power Supply and Sequencing

The carrier board receives the main power source and uses this to generate the enable to Jetson Xavier NX (POWER_EN) after the carrier board has ensured the main supply is stable and the associated decoupling capacitors have charged. The carrier board supplies are not enabled at this time. Once POWER_EN is driven active (high), Jetson Xavier NX begins to Power-ON. When the module Power-ON sequence has completed, the SYS_RESET* signal is driven inactive (high) and this is used by the carrier board to enable its various supplies. SYS_RESET* is bidirectional and can be driven by the carrier board to reset Jetson Xavier NX, which results in a full system power cycle. The SHUTDOWN_REQ* signal from Jetson Xavier NX can be driven active (low) if the system must be shut down, due to a critical thermal issue, etc. The power control logic on the carrier board should drive POWER_EN inactive (low) if SHUTDOWN_REQ* is asserted.

Figure 3-1. System Power and Control Block Diagram

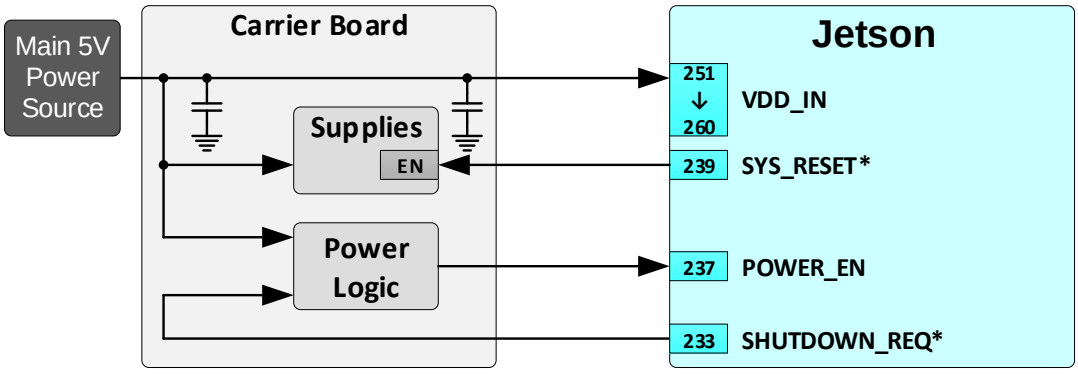


Figure 3-2. Power Up Sequence (No Power Button – Auto Power On)

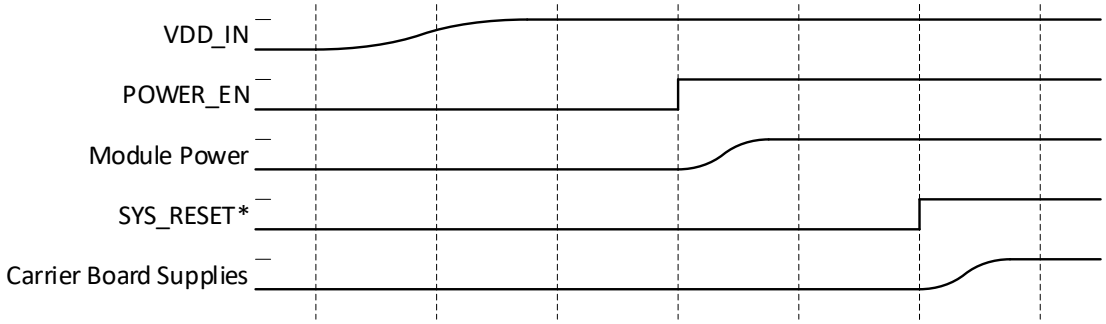


Figure 3-3. Power Down (Initiated by SHUTDOWN_REQ* Assertion)

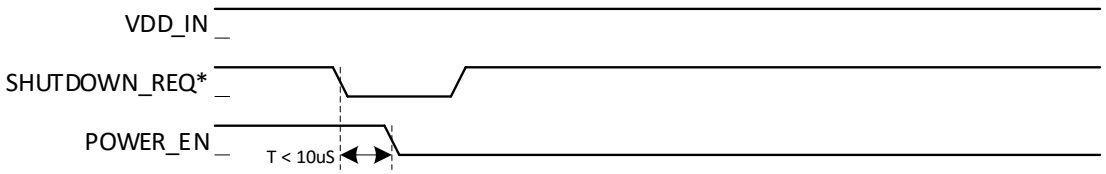
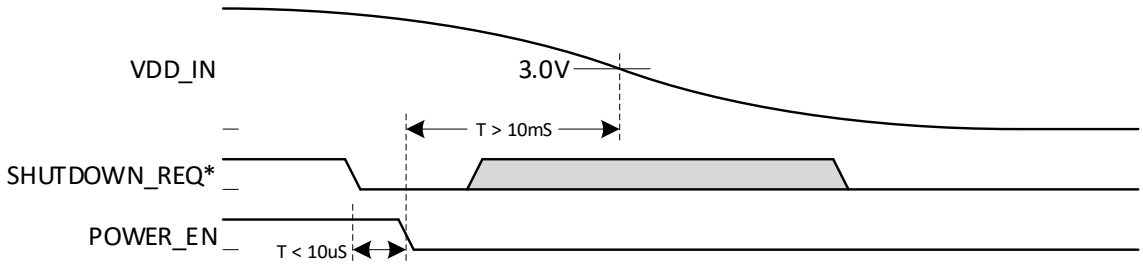


Figure 3-4. Power Down (Sudden Power Loss)



Note: SHUTDOWN_REQ* must always be serviced by the carrier board to toggle POWER_EN from high to low, even in cases of sudden power loss.

Chapter 4. USB and PCIe

Jetson Xavier NX allows multiple USB 2.0, USB 3.1 and PCIe interfaces to be brought out of the module.

- USB 2.0: 3x
- USB 3.1: 1x
- PCIe: x1 + x4

The PCIe x4 interface supports both Root Port and Endpoint operation. The PCIe x1 interface supports only Root Port operation.

Table 4-1. Jetson Xavier NX USB 2.0 Pin Description

Pin #	Module Pin Name	Xavier Pin Name	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
87	GPIO00	USB_VBUS_EN0	GPIO #0 (USB 0 VBUS Detect)	USB 2.0 Micro B	Bidir	Open Drain, 1.8V	DD	0
109	USB0_D_N	USB0_DN	USB 2.0 Port 0 Data	USB conn/device/hub (i.e. Micro B)	Bidir	USB PHY	–	0
111	USB0_D_P	USB0_DP					–	0
115	USB1_D_N	USB1_DN	USB 2.0 Port 1 Data	USB conn/device/hub (i.e. USB 3.1 Hub)	Bidir	USB PHY	–	0
117	USB1_D_P	USB1_DP					–	0
121	USB2_D_N	USB2_DN	USB 2.0, Port 2 Data	USB conn/device/hub (i.e. M.2 Key E)	Bidir	USB PHY	–	0
123	USB2_D_P	USB2_DP					–	0

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 4-2. Jetson Xavier NX USB 3.1 and PCIe Pin Description

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
131	PCIE0_RX0_N	NVHS0_RX0_N	PCIe #0 Receive 0 (PCIe Ctrl #5 Lane 0)	PCIe x4 conn/device (i.e. M.2 Key M)	Input	PCIe PHY, AC-Coupled for PCIe on carrier board if direct connect.	–	z
133	PCIE0_RX0_P	NVHS0_RX0_P					–	z
137	PCIE0_RX1_N	NVHS0_RX1_N	PCIe #0 Receive 1 (PCIe Ctrl #5 Lane 1)				–	z
139	PCIE0_RX1_P	NVHS0_RX1_P					–	z
149	PCIE0_RX2_N	NVHS0_RX2_N	PCIe #0 Receive 2 (PCIe Ctrl #5 Lane 2)				–	z
151	PCIE0_RX2_P	NVHS0_RX2_P					–	z
155	PCIE0_RX3_N	NVHS0_RX3_N	PCIe #0 Receive 3 (PCIe Ctrl #5 Lane 3)				–	z
157	PCIE0_RX3_P	NVHS0_RX3_P					–	z
134	PCIE0_TX0_N	NVHS0_TX0_N	PCIe #0 Transmit 0 (PCIe Ctrl #5 Lane 0)		Output	PCIe PHY, AC-Coupled on carrier board	–	z
136	PCIE0_TX0_P	NVHS0_TX0_P					–	z
140	PCIE0_TX1_N	NVHS0_TX1_N	PCIe #0 Transmit 1 PCIe Ctrl #5 Lane 1)				–	z
142	PCIE0_TX1_P	NVHS0_TX1_P					–	z
148	PCIE0_TX2_N	NVHS0_TX2_N	PCIe #0 Transmit 2 (PCIe Ctrl #5 Lane 2)				–	z
150	PCIE0_TX2_P	NVHS0_TX2_P					–	z
154	PCIE0_TX3_N	NVHS0_TX3_N	PCIe #0 Transmit 3 (PCIe Ctrl #5 Lane 3)				–	z
156	PCIE0_TX3_P	NVHS0_TX3_P					–	z
181	PCIE0_RST*	PEX_L5_RST_N	PCIe #0 Reset (PCIe Ctrl #5). 4.7kΩ pull-up to 3.3V on the module. Output when module is Root Port - input when module Endpoint.		Bidir	Open Drain 3.3V, Pull-up on the module	DD	0
180	PCIE0_CLKREQ*	PEX_L5_CLKREQ_N	PCIE #0 Clock Request (PCIe Ctrl #5). 47kΩ pull-up to 3.3V on the module. Input when module is Root Port - output when module is Endpoint.				DD	z
160	PCIE0_CLK_N	PEX_CLK5N or NVHS0_REFCLK_N	PCIe #0 Reference Clock controlled by on-module mux by SoC CAN0_EN. When CAN0_EN is low, PEX_CLK5 is selected (reference clock when module is Root Port). When CAN0_EN is high, NVHS0_REFCLK is selected (reference clock input when Jetson Xavier NX is an Endpoint).		Bidir	PCIe PHY	–	0
162	PCIE0_CLK_P	PEX_CLK5P or NVHS0_REFCLK_P					–	0
167	PCIE1_RX0_N	PEX_RX11_N	PCIe #1 Receive 0 (PCIe Ctrl #4 Lane 0)	PCIe x1 conn/device (i.e. M.2 Key E)	Input	PCIe PHY	–	z
169	PCIE1_RX0_P	PEX_RX11_P					–	z
172	PCIE1_TX0_N	PEX_TX11_N	PCIe #1 Transmit 0 (PCIe Ctrl #4 Lane 0)		Output	PCIe PHY, AC-Coupled on carrier board	–	z
174	PCIE1_TX0_P	PEX_TX11_P					–	z
183	PCIE1_RST*	PEX_L4_RST_N	PCIe #1 Reset (PCIe Ctrl #4). 4.7kΩ pull-up to 3.3V on the module.		Output	Open Drain 3.3V, Pull-up on the module	DD	0
182	PCIE1_CLKREQ*	PEX_L4_CLKREQ_N	PCIE #1 Clock Request (PCIe Ctrl #4). 47kΩ pull-up to 3.3V on the module.		Bidir	Open Drain 3.3V, Pull-up on the module	DD	z
173	PCIE1_CLK_N	PEX_CLK4N	PCIe #1 Reference Clock (PCIe Ctrl #4)		Output	PCIe PHY	–	0
175	PCIE1_CLK_P	PEX_CLK4P					–	0

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
179	PCIE_WAKE*	PEX_WAKE_N	PCIe Wake. 100kΩ pull-up to 3.3V on the module.	Shared between x1 and x4 PCIe interfaces.	Input	Open Drain 3.3V, Pull-up on the module	DD	z
161	USBSS_RX_N	PEX_RX1_N	USB SS Receive (USB 3.1 Ctrl #2)	USB 3.1 connector, device or hub	Input	USB SS PHY, AC-Coupled on carrier board only if direct connect to device	–	z
163	USBSS_RX_P	PEX_RX1_P					–	z
166	USBSS_TX_N	PEX_TX1_N	USB SS Transmit (USB 3.1 Ctrl #2)		Output	USB SS PHY, AC-Coupled on carrier board	–	z
168	USBSS_TX_P	PEX_TX1_P					–	z

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 4-3 shows the mapping options for Jetson Xavier NX.

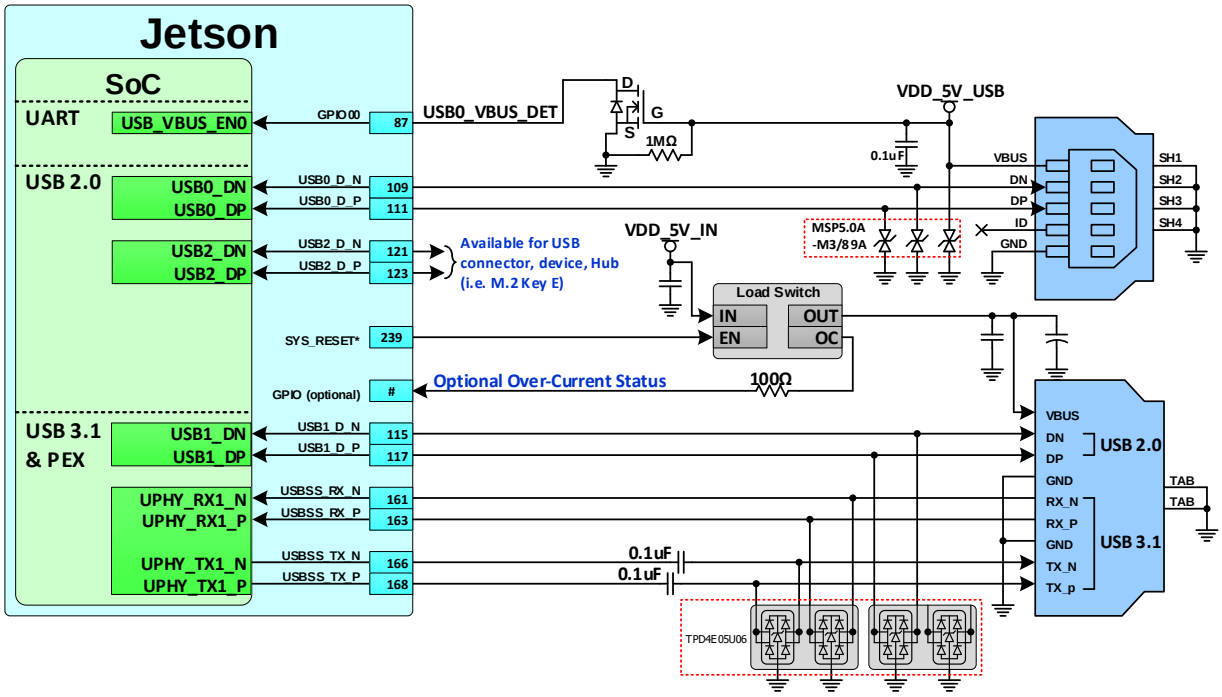
Table 4-3. Jetson Xavier NX USB 3.10 and PCIe Lane Mapping Configurations

Module Pin Names		PCIE0_RX3_N/P PCIE0_TX3_N/P	PCIE0_RX2_N/P PCIE0_TX2_N/P	PCIE0_RX1_N/P PCIE0_TX1_N/P	PCIE0_RX0_N/P PCIE0_TX0_N/P	PCIE1_RX0_N/P PCIE1_TX0_N/P	USBSS_RX_N/P USBSS_TX_P/N
Xavier Lanes		Lane 5	Lane 4	Lane 3	Lane 2	Lane 11	Lane 1
USB 3.1	PCIe						
1	1x4 + 1x1	PCIe 0 lane 3 Controller #5	PCIe 0 lane 2 Controller #5	PCIe 0 lane 1 Controller #5	PCIe 0 lane 0 Controller #5	PCIe 1 lane 0 Controller #4	USB_SS Port #2
Recommended Usage		PCIe x4 connector or device (I.E. M.2 Key M)				PCIe x1 connector or device (i.e. M.2 Key E)	USB 3.1 connector, device or hub

4.1 USB

Figure 4-1 shows the USB connection example.

Figure 4-1. USB Connection Example



Notes:

1. AC capacitors should be located close to either the USB connector, or the Jetson Xavier NX pins.
2. For USB 3.1 IF shown above (USBSS_TX/RX), AC caps are required on the TX lines. If routed directly to a peripheral, AC caps are needed on the peripheral TX lines as well. The AC caps are recommended to be located near the Jetson Xavier NX connector pins, although locating the caps near the peripheral RX pins is acceptable.
3. USB0 must be available to use as USB Device for USB Recovery Mode.
4. Load switch can be enabled by SYS_RESET* or an available GPIO.
5. Connector used must be USB Implementers Forum certified if USB 3.1 is implemented.

4.1.1 USB 2.0 Design Guidelines

These requirements apply to the USB 2.0 controller PHY interfaces: **USB[2:0]_D_N/P**

Table 4-4. USB 2.0 Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Max frequency (high speed)	Bit Rate/UI period/Frequency	480/2.083/240	Mbps/ns/MHz	
Max loading	High Speed / Full Speed / Low Speed	10 / 150 / 600	pF	
Reference plane		GND		
Trace impedance	Diff pair / SE	90 / 50	Ω	±15%
Via proximity (signal to reference)		< 3.8 (24)	mm (ps)	See Note 1
Max trace length/delay	Microstrip / Stripline	6 (960)	In (ps)	
Max intra-pair skew between **USBx_D_P** and **USBx_D_N**		7.5	ps	

Notes:
1. Up to four signal vias can share a single GND return via.
2. Adjustments to the USB drive strength, slew rate, termination value settings should not be necessary, but if any are made, they MUST be done as an offset to default values instead of overwriting those values.

4.1.2 USB 3.1 Design Guidelines

The following requirements apply to the USB 3.1 Port #2 PHY interface: **USBSS_TX_N/P**, **USBSS_RX_N/P**.

Table 4-5. USB 3.1 Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Specification				
Data Rate / UI period	GEN1 GEN2	5.0 / 200 10.0 / 100	Gbps / ps	Device mode supports GEN1 speed only.
Max Number of Loads		1	load	
Termination		90 differential	Ω	On-die termination at TX & RX
Electrical Specification				
Insertion Loss (IL - Min)				
Host				
	GEN1 (Type C)	-2	dB	@ 2.5GHz
	GEN1 (Type A)	-7		@ 2.5GHz
	GEN2	-5.4		@ 5GHz
Device				
	GEN1 (Micro AB)	≤ 1		@ 2.5GHz
	Resonance Dip Frequency	> 8	GHz	The resonance dip could be caused by a via stub for layer transition or trace stub for co-layout.
Time-domain Reflectometer (TDR) Dip	GEN1 GEN2	75 75	Ω	@ Tr = 200ps (10%-90%) @ Tr = 61ps (10%-90%)
Near End Crosstalk (NEXT)		≤ –45	dB	DC – 5GHz per each TX-RX NEXT
Impedance				

Parameter		Requirement	Units	Notes
Trace Impedance	Diff pair / Single Ended	85 / 43	Ω	±15%. Intrinsic Zdf, does not account for coupling from other trace pairs
Reference plane		GND		
Trace Length/Skew				
Trace loss characteristic (max):	GEN1 GEN2	0.7 0.8	dB/in	@ 2.5GHz (see Figure 4-2) @ 5GHz (See Figure 4-3) The following max length is derived based on this characteristic. The length constraint must be re-defined if loss characteristic is changed.
Breakout Region – Max length	GEN1 GEN2	11 3	mm	Minimum trace width and spacing
Max Trace Length (Host)	GEN1 or GEN2	152 (1014)	mm (ps)	
Max Trace Length (Device)	GEN1 only	51 (334)	mm (ps)	
Max Intra-Pair Skew (**RX/TX_N** to **RX/TX_P**)		0.15 (1)	mm (ps)	Do not perform length matching within breakout region. Trace length matching should be done before discontinuities. See Note 2
Differential pair uncoupled length		6.29 (41.9)	mm (ps)	
Trace Spacing for TX/RX Interleaving				
Trace Spacing (Microstrip / Stripline)	Pair-Pair To Ref plane and SMT pad To unrelated high-speed signals	4x / 3x 4x / 3x 4x / 3x	Dielectric height	
Trace Spacing for TX/RX Non-interleaving				
TX-RX Xtalk is very critical in PCB trace routing. The ideal solution is to route TX and RX on different layers.				
If routing on the same layer, strongly recommend not interleaving TX and RX lanes				
If have to have interleaving routing in breakout, all the inter-pair spacing should follow the rule of inter-S_{NEXT} (between TX/RX pair spacing)				
The breakout trace width is suggested to be the minimum to increase inter-pair spacing				
Do not perform serpentine routing for intra-pair skew compensation in the breakout region				
Min Inter-S_{NEXT} (between TX/RX)	Breakout Main-route	4.85x 3x	Dielectric height	This is the recommended dimensions for meeting the NEXT requirement. Stripline structure in a GSSG structure is assumed (holds in broadside-coupled stripline structure)
Max length	Breakout Main-route	11 Max trace length - L_{BRK}	mm	
Via				
Via proximity (Signal via to GND return via)		< 3.8 (24)	mm (ps)	See Note 1
Topology		Y-pattern is recommended Keep symmetry		Y-pattern helps with Xtalk suppression. It can also reduce the limit of the pair-pair distance. Review needed (NEXT/FEXT check) if via placement does not use Y-pattern. See Figure **4-4**.
GND via		Place **GND** via as symmetrically as possible to data pair vias. Up to 4 signal vias (2 diff pairs) can share a single **GND** return via		**GND** via is used to maintain return path, while its Xtalk suppression is limited
Max # of Vias	PTH vias Micro Vias	4 if all vias are PTH via Not limited as long as total channel loss meets IL spec		
Max Via Stub Length		0.4	mm	long via stub requires review (IL and resonance dip check)
Additional Component Placement Order				
		Chip – AC capacitor (TX only) – common mode choke – ESD – Connector		
		See Figure 4-5.		See Figure 4-6.
AC Cap				
Value	Min/Max	0.075 / 0.2	uF	Only required for TX pair when routed to connector
Location (max length to adjacent discontinuity)		8	mm	Discontinuity is connector, via, or component pad
Voiding		**GND**/**PWR** void under/above cap is preferred		Voiding is required if AC cap size is 0603 or larger
ESD				
Max Junction capacitance (IO to GND)		0.8	pF	e.g. SEMTECH RClamp0524p
Footprint		Pad should be on the net – not trace stub		See Figure 4-7.
Location (max length to adjacent discontinuity)		8	mm	Discontinuity is connector, via, or component pad
Common-mode Choke (Not recommended – only used if absolutely required for EMI issues). See Appendix A for details on CMC if implemented.				
FPC (Additional length of Flexible Printed Circuit Board)				
The FPC routing should be included for PCB trace calculations (max length, etc.)				
Characteristic Impedance		Same as PCB		
Loss characteristic		Strongly recommend being the same as the PCB or better		If worse than PCB, the PCB and FPC length must be re-estimated
Connector				

Parameter	Requirement	Units	Notes
SMT Connector **GND** Voiding	**GND** plane under signal pad should be voided. Size of void should be the same size as the pad.		
Connector used must be USB-IF certified			
General: See Chapter 14 for guidelines related to serpentine routing, routing over voids and noise coupling			

Notes:

1. Up to 4 signal Vias can share a single **GND** return Via.
2. Recommend trace length matching to <1ps before Vias or any discontinuity to minimize common mode conversion.
3. Place GND Vias as symmetrically as possible to data pair Vias.

The following figures show the USB 31. Interface signal routing requirements.

Figure 4-2. IL/NEXT Plot (GEN1)

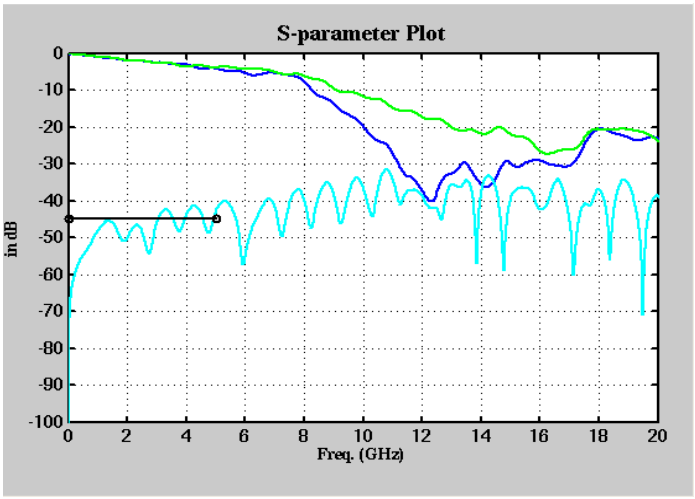


Figure 4-3. IL/NEXT Plot (GEN2)

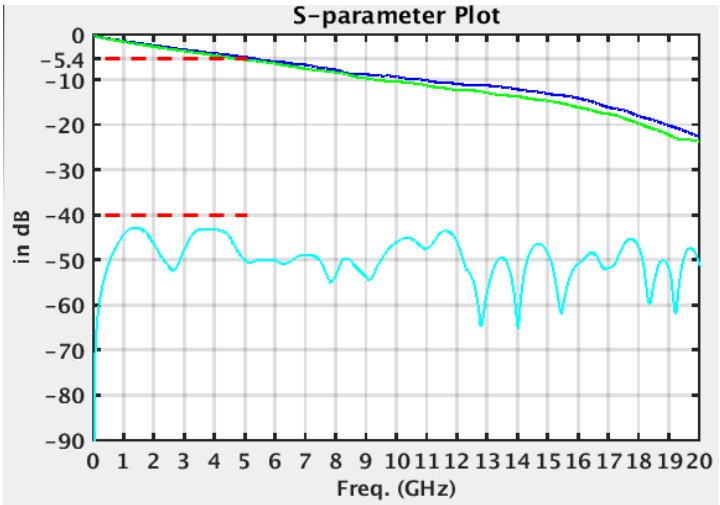


Figure 4-4. Via Topology

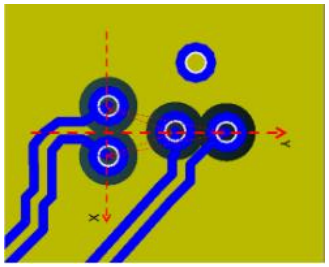


Figure 4-5. Component Order

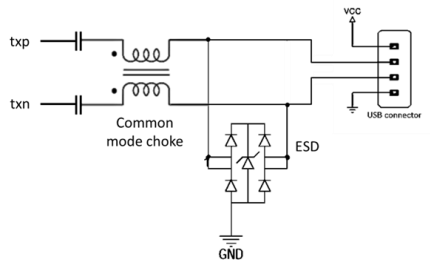


Figure 4-6. Component Placement

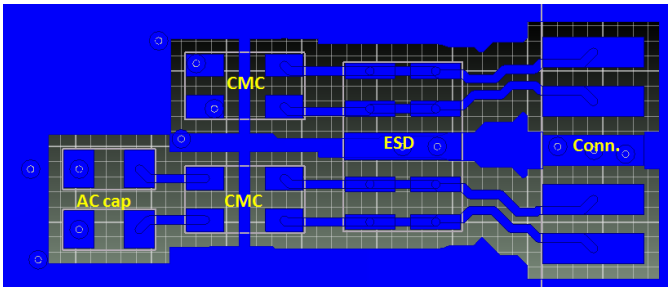
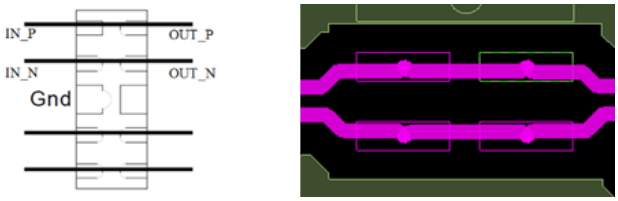


Figure 4-7. ESD Layout Recommendations



4.1.2.1 Common USB Routing Guidelines

If routing to USB device or USB connector includes a flex or 2nd PCB, the total routing including all PCBs/flexes must be used for the max trace and skew calculations.

Keep critical USB related traces away from other signal traces or unrelated power traces/areas or power supply components

Table 4-6. Xavier USB 2.0 Signal Connections

Module Ball Name	Type	Termination	Description
USB[2:0]_D_P USB[2:0]_D_N	DIFF I/O	If used, 90Ω common-mode chokes close to connector. ESD Protection between choke and connector on each line to GND	USB Differential Data Pair: Connect to USB connector, Mini-Card socket, hub or another device on the PCB.

Table 4-7. Miscellaneous USB 2.0 Signal Connections

Module Pin Name	Type	Termination	Description
GPIO00	A	5V to 1.8V level shifter	USB0 VBUS Enable: Connect to VBUS pin of USB connector receiving USB0_+/– interface through level shifter. Also connects to VBUS power supply if host mode supported.

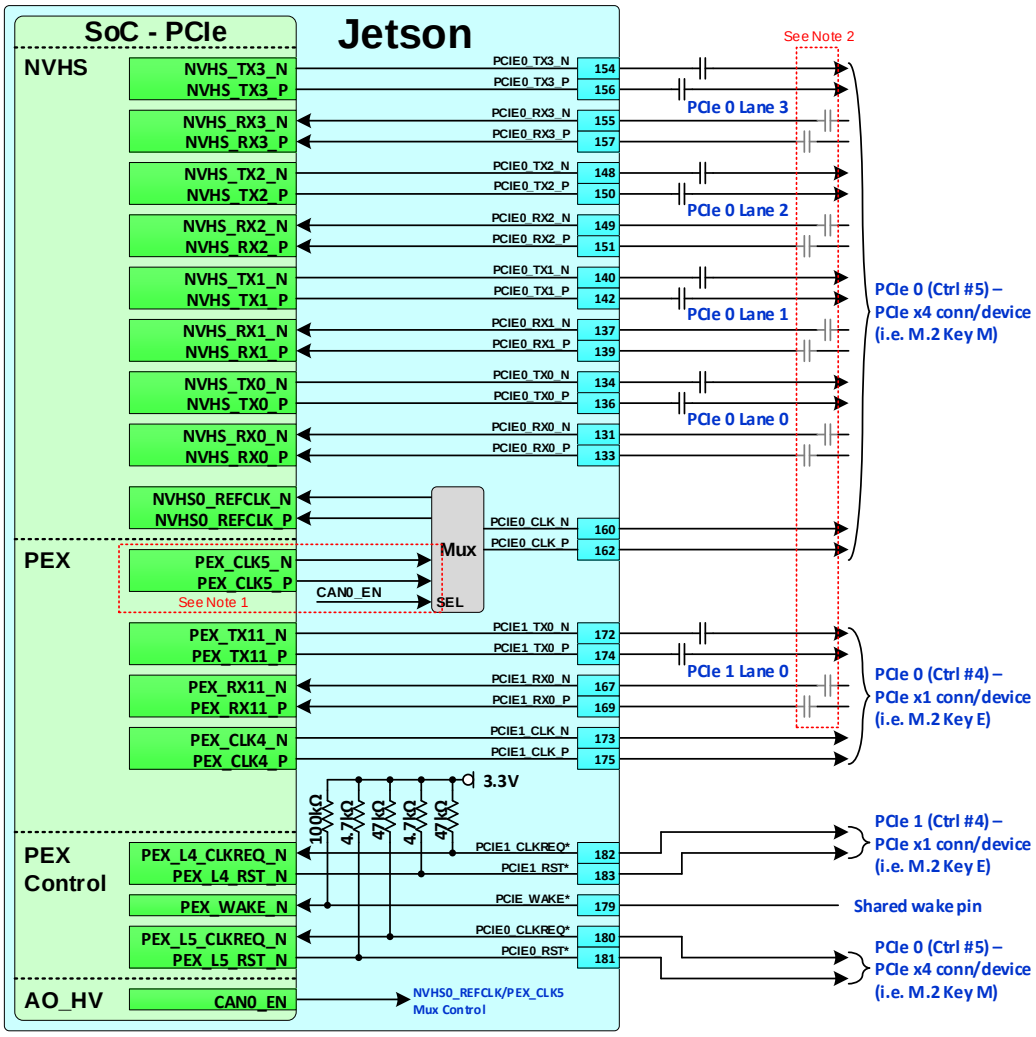
Table 4-8. Xavier USB 3.1 Signal Connections

Module Pin Name	Type	Termination	Description
USBSS_TX_N/P (USB 3.1 Port #2)	DIFF Out	Series 0.1uF caps. ESD Protection near connector if required.	USB 3.1 Differential Transmit Data Pairs: Connect to USB 3.1 connectors, hubs or other devices on the PCB.
USBSS_RX_N/P (USB 3.1 Port #2)	DIFF In	If routed directly to a peripheral on the board, AC caps are needed for the peripheral TX lines. ESD protection near connector if required.	USB 3.1 Differential Receive Data Pairs: Connect to USB 3.1 connectors, hubs or other devices on the PCB.

4.2 PCIe

Jetson Xavier NX brings two PCIe interfaces to the module pins for up to 5 total lanes (1 x4 + 1 x1) for use on the carrier board. Both the x1 and x4 interfaces are Root Port as shown in Figure 4-8.

Figure 4-8. PCIe Root Port Connections Example

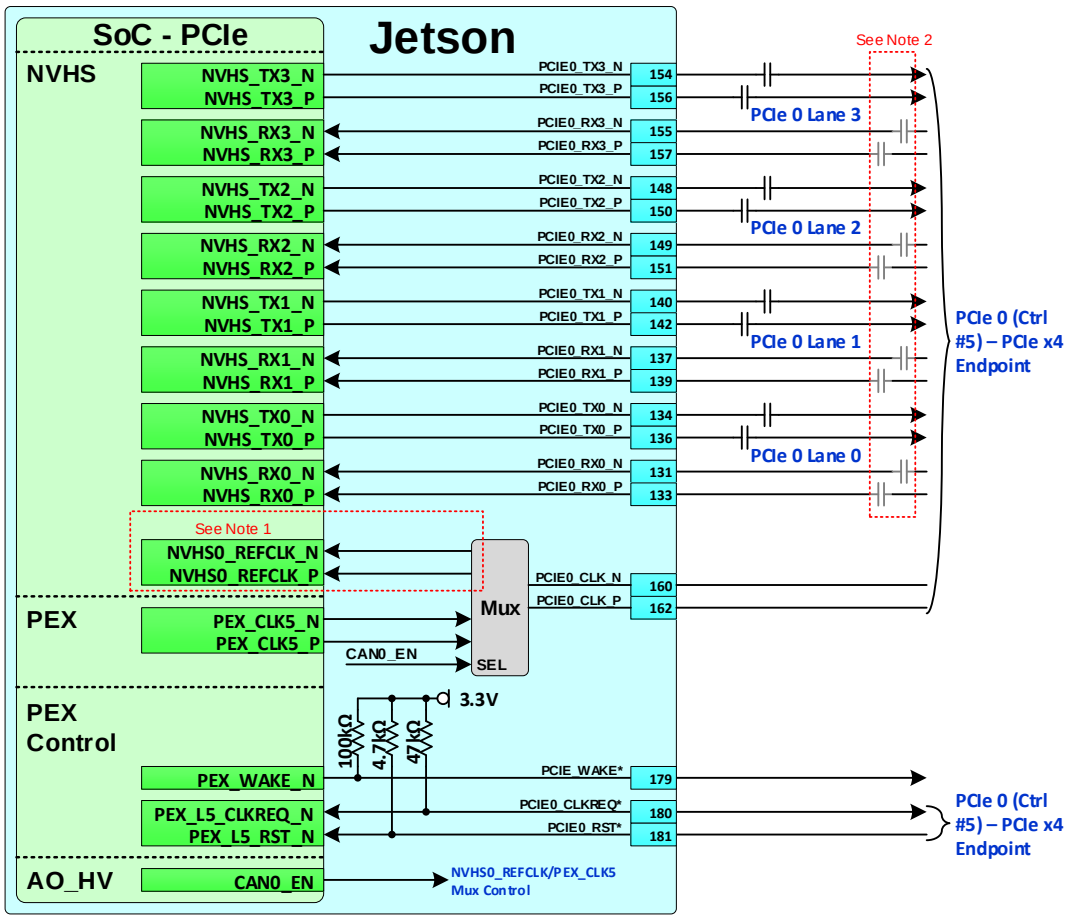


Notes:

1. For Root Port operation, the mux should be set to output the PEX_CLK5 signals. CAN0_EN which is used for the mux select should be set low.
2. AC Capacitors required on RX lines on carrier board if connected directly to device. They should not be on the carrier board if connected to PCIe connector, M.2 Key M, etc. In those cases, the AC caps are on the board connected to those connectors.
3. See design guidelines for correct AC capacitor values.

Figure 4-9 shows the x4 interface configured as Endpoint for the PCIe Endpoint connections.

Figure 4-9. PCIe Endpoint Connections Example



Notes:

1. For Endpoint operation, the mux should be set to input the reference clock from the PCIe Root Port device to the NVIDIA® Xavier™ NVHS0_REFCLK pins. CAN0_EN which is used for the mux select should be set high.
2. AC Capacitors required on RX lines on carrier board if connected directly to device. They should not be on the carrier board if connected to PCIe connector, M.2 Key M, etc. In those cases, the AC caps are on the board connected to those connectors.
3. See design guidelines for correct AC capacitor values.

4.2.1 PCIe Design Guidelines

The following signal requirements meet the PCIe design guidelines.

Table 4-9. PCIe Interface Signal Routing Requirements (to Gen3)

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI Period	8.0 / 125	Gbps / ps	4.0GHz, half-rate architecture
Configuration / Device Organization	1	Load	
Topology	Point-point		Unidirectional, differential
Termination	50	Ω	To **GND** Single Ended for P & N
Impedance			
Trace Impedance differential / Single Ended	85 / 50	Ω	±15%. See Note 1
Reference plane	**GND**		
Spacing			
Trace Spacing (Stripline/Microstrip) Pair – Pair To plane and capacitor pad To unrelated high-speed signals	3x / 4x 3x / 4x 3x / 4x	Dielectric	TX and RX should not be routed on the same layer. See Note 2.
Length/Skew			
Breakout region (Max Length)	41.9	ps	Minimum width and spacing. 4x or wider dielectric height spacing is preferred
Max trace length To PCIe Connector Stripline Microstrip Direct to PCIe Device Stripline Microstrip	 5.5 (979) 5.5 (825) 9 (1602) 9 (1250)	in (ps)	Assumption used is 178ps/in for Stripline routing and 150ps/in for Microstrip.
Max PCB via distance from the BGA	41.9	ps	Max distance from BGA ball to first PCB via.
PCB within pair (intra-pair) skew	0.075 (0.5)	mm (ps)	Do trace length matching before hitting discontinuities
Within pair (intra-pair) matching between subsequent discontinuities	0.075 (0.5)	mm (ps)	
Differential pair uncoupled length	41.9	ps	
Via			
Via placement	Place **GND** vias as symmetrically as possible to data pair vias. **GND** via distance should be placed less than 1x the diff pair via pitch		
Max # of Vias PTH Vias Micro-Vias	2 for TX traces and 2 for RX trace No requirement		
Max Via stub length	0.4	mm	Longer via stubs would require review
Routing signals over antipads	Not allowed		
AC Cap			
Value GEN1/GEN2: Min/Max GEN3: Min/Max	0.075 / 0.265 0.176 / 0.265	uF	0.1uF or 0.22uF recommended for GEN1 or GEN2. 0.22uF recommended for GEN3. Only required for TX pair when routed to connector
Location (max length to adjacent discontinuity)	8	mm	Discontinuity such as edge finger, component pad
Voiding	Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.		See Figure 4-10.

Parameter	Requirement	Units	Notes
Connector			
Voiding	Voiding the plane directly under the pad 5.7 mils larger than the pad size is recommended.		See Figure 4-11.
General: See Chapter 14 for guidelines related to serpentine routing, routing over voids and noise coupling			

Notes:

1. The PCIe spec. has 40-60Ω absolute min/max trace impedance, which can be used instead of the 50Ω, ± 15%.
2. If routing in the same layer is necessary, route group TX and RX separately without mixing RX/TX routes and keep distance between nearest TX/RX trace and RX to other signals 3x RX-RX separation.
3. For trace loss >= 0.7dB/in @ 2.5GHz, the max trace length should be 7 inches. To reduce trace loss, ensure the loss tangent of the dielectric material and roughness of the metal are tightly controlled.
4. The average of the differential signals is used for length matching.
5. Do length matching before Via transitions to different layers or any discontinuity to minimize common mode conversion.

Figure 4-10. AC Cap Voiding

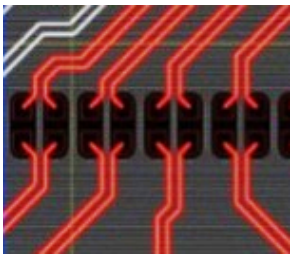


Figure 4-11. Connector Voiding

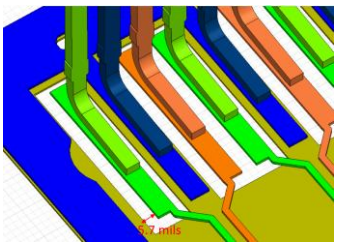


Table 4-10. PCIe Signal Connections

Module Pin Name	Type	Termination	Description
PCIe Interface 0 (x4 – Controller #5)			
PCIE0_TX3_N/P **PCIE0_TX2_N/P** **PCIE0_TX1_N/P** **PCIE0_TX0_N/P**	DIFF OUT	Series 0.22uF Capacitor	**Differential Transmit Data Pairs:** Connect to TX_N/P pins of PCIe connector or RX_N/P pin of PCIe device through AC cap according to supported configuration.
PCIE0_RX3_N/P **PCIE0_RX2_N/P** **PCIE0_RX1_N/P** **PCIE0_RX0_N/P**	DIFF IN	Series 0.22uF capacitors near Jetson Xavier NX pins or device if device on main PCB.	**Differential Receive Data Pairs:** Connect to RX_N/P pins of PCIe connector or TX_N/P pin of PCIe device through AC cap according to supported configuration.
PCIE0_CLK_N/P	DIFF OUT (Rootport) DIFF IN (Endpoint)		**Differential Reference Clock Output:** Connected to a mux on the module that selects either PEX_CLK5 or NVHS0_REFCLK. Connect to REFCLK_N/P pins of PCIe device/connector. For Root Port operation, set the mux to select PEX_CLK3 (CAN0_EN = 0). For Endpoint, set the mux to select NVHS0_REFCLK (CAN_EN = 1).
PCIE0_CLKREQ*	I/O (Root Port) I (Endpoint)	47kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Clock Request for PCIE0_CLK:** Connect to **CLKREQ** pins on device/connector(s)
PCIE0_RST*	O (Root Port) I (Endpoint)	4.7kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Reset:** Connect to **PERST** pins on device/connector(s)
PCIe Interface 1 (x1 – Controller #4)			
PCIE1_TX0_N/P	DIFF OUT	Series 0.22uF Capacitor	**Differential Transmit Data Pair:** Connect to TX_N/P pins of PCIe connector or RX_N/P pin of PCIe device through AC cap according to supported configuration.
PCIE1_RX0_N/P	DIFF IN	Series 0.22uF capacitors near Jetson Xavier NX pins or device if device on main PCB.	**Differential Receive Data Pair:** Connect to RX_N/P pins of PCIe connector or TX_N/P pin of PCIe device through AC cap according to supported configuration.
PCIE1_CLK_N/P	DIFF OUT		**Differential Reference Clock Output:** Connect to REFCLK_N/P pins **of PCIe device/connector**
PCIE1_CLKREQ*	I/O	47kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Clock Request for PCIE1_CLK:** Connect to **CLKREQ** pins on device/connector(s)
PCIE1_RST*	O	4.7kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Reset:** Connect to **PERST** pins on device/connector(s)
Common			
PCIE_WAKE*	I	100kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Wake:** Connect to **WAKE** pins on device or connector

4.3 Gigabit Ethernet

Jetson Xavier NX integrates a Realtek RTL8211FDI Gigabit Ethernet PHY. The magnetics and RJ45 connector would be implemented on the carrier board.

Table 4-11. Jetson Xavier NX Gigabit Ethernet Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
194	GBE_LED_ACT	–	Ethernet Activity LED (Yellow)	LAN	Output		–	–
188	GBE_LED_LINK	–	Ethernet Link LED (Green)		Output		–	–
184	GBE_MDI0_N	–	GbE Transformer Data 0		Bidir	MDI	–	–
186	GBE_MDI0_P	–					–	–
190	GBE_MDI1_N	–	GbE Transformer Data 1				–	–
192	GBE_MDI1_P	–					–	–

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
196	GBE_MDI2_N	–	GbE Transformer Data 2				–	–
198	GBE_MDI2_P	–					–	–
202	GBE_MDI3_N	–	GbE Transformer Data 3				–	–
204	GBE_MDI3_P	–					–	–

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Figure 4-12. Jetson Xavier NX Ethernet Connections

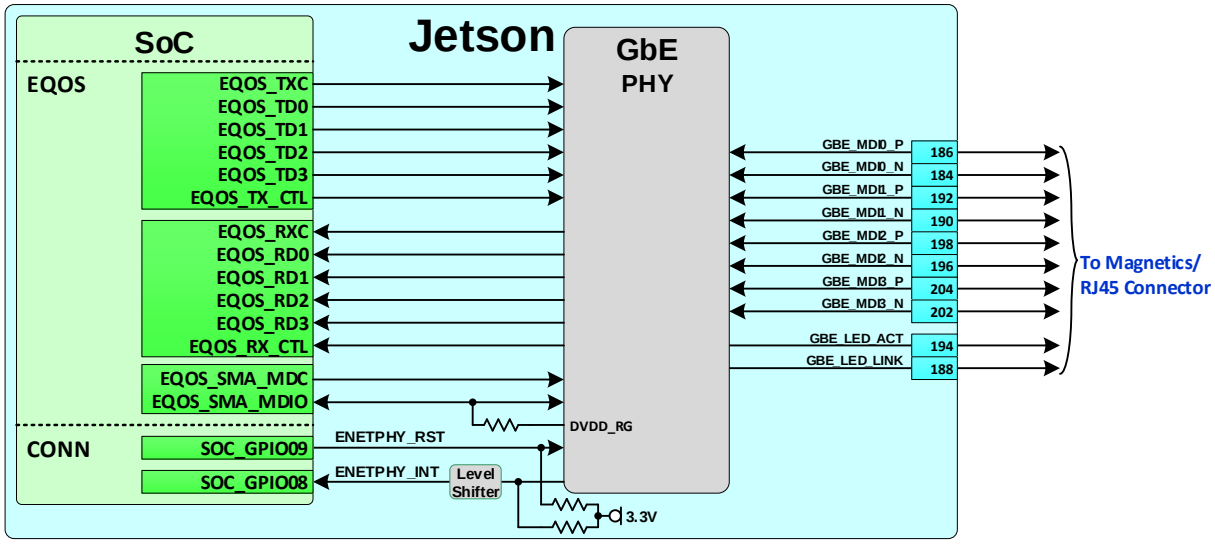


Figure 4-13. Gigabit Ethernet Magnetics and RJ45 Connections

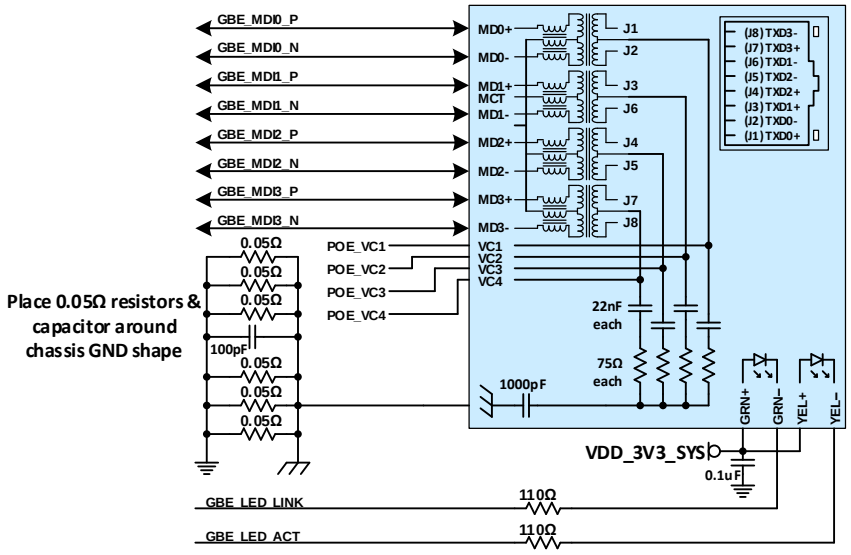


Table 4-12. Ethernet MDI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	GND		
Trace impedance Diff pair / Single Ended	100 / 50	Ω	±15%. Differential impedance target is 100Ω. 90Ω can be used if 100Ω is not achievable
Min trace spacing (pair-pair)	0.763	mm	
Max trace length/delay	109 (690)	mm (ps)	
Max within pair (intra-pair) skew	0.15 (1)	mm (ps)	
Number of vias	minimum		Ideally there should be no vias, but if required for breakout to Ethernet controller or magnetics, keep very close to either device.

Table 4-13. Ethernet Signal Connections

Module Pin Name	Type	Termination	Description
GBE_MDI[3:0]_N/P	DIFF I/O		Gigabit Ethernet MDI IF Pairs: Connect to Magnetics -/+ pins
GBE_LED_LINK	O	110Ω series resistor	Gigabit Ethernet Link LED: Connect to green LED cathode on RJ45 connector. Anode connected to VDD_3V3_SYS
GBE_LED_ACT	O	110Ω series resistor	Gigabit Ethernet Activity LED: Connect to yellow LED cathode on RJ45 connector. Anode connected to VDD_3V3_SYS

Chapter 5. Display

Jetson Xavier NX designs can select from several display options including VESA® Embedded DisplayPort® (eDP) for embedded displays, and HDMI™ or DisplayPort (DP) for external displays. The two display interfaces can be run simultaneously.

Table 5-1. Jetson Xavier NX eDP and DP Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
90	DP0_AUX_N	DP_AUX_CH0_N	DisplayPort 0 Aux– or HDMI DDC SDA	DP connector	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC)	DP_AUX	z
92	DP0_AUX_P	DP_AUX_CH0_P	DisplayPort 0 Aux+ or HDMI DDC SCL				DP_AUX	z
39	DP0_TXD0_N	HDMI_DP0_TXDN0	DisplayPort 0 Lane 0 or HDMI Lane 2		Output	AC-Coupled on carrier board	–	z
41	DP0_TXD0_P	HDMI_DP0_TXDP0					–	z
45	DP0_TXD1_N	HDMI_DP0_TXDN1	DisplayPort 0 or HDMI Lane 1				–	z
47	DP0_TXD1_P	HDMI_DP0_TXDP1					–	z
51	DP0_TXD2_N	HDMI_DP0_TXDN2	DisplayPort 0 Lane 2 or HDMI Lane 0				–	z
53	DP0_TXD2_P	HDMI_DP0_TXDP2					–	z
57	DP0_TXD3_N	HDMI_DP0_TXDN3	DisplayPort 0 Lane 3– or HDMI Clk Lane				–	z
59	DP0_TXD3_P	HDMI_DP0_TXDP3					–	z
88	DP0_HPD	DP_AUX_CH0_HPD	HDMI or DisplayPort 0 Hot Plug Detect		Input	CMOS – 1.8V	DD	pd
98	DP1_AUX_N	DP_AUX_CH1_N	Display Port 1 Aux– or HDMI DDC SDA	HDMI Connector	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC)	DP_AUX	z
100	DP1_AUX_P	DP_AUX_CH1_P	Display Port 1 Aux+ or HDMI DDC SCL				DP_AUX	z
63	DP1_TXD0_N	HDMI_DP1_TXDN0	DisplayPort 1 Lane 0 or HDMI Lane 2		Output	AC-Coupled on carrier board	–	z
65	DP1_TXD0_P	HDMI_DP1_TXDP0					–	z
69	DP1_TXD1_N	HDMI_DP1_TXDN1	DisplayPort 1 or HDMI Lane 1				–	z
71	DP1_TXD1_P	HDMI_DP1_TXDP1					–	z
75	DP1_TXD2_N	HDMI_DP1_TXDN2	DisplayPort 1 Lane 2 or HDMI Lane 0				–	z
77	DP1_TXD2_P	HDMI_DP1_TXDP2					–	z
81	DP1_TXD3_N	HDMI_DP1_TXDN3	DisplayPort 1 Lane 3 or HDMI Clk Lane				–	z
83	DP1_TXD3_P	HDMI_DP1_TXDP3					–	z

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
96	DP1_HPD	DP_AUX_CH1_HPD	Display Port 1 or HDMI Hot Plug Detect		Input	CMOS – 1.8V	DD	pd
94	HDMI_CEC	HDMI_CEC	HDMI CEC		Bidir	Open Drain, 1.8V	DD	z

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

A standard DP 1.4 or HDMI V2.0 interface is supported. These share the same set of interface pins, so either DisplayPort or HDMI can be supported natively.

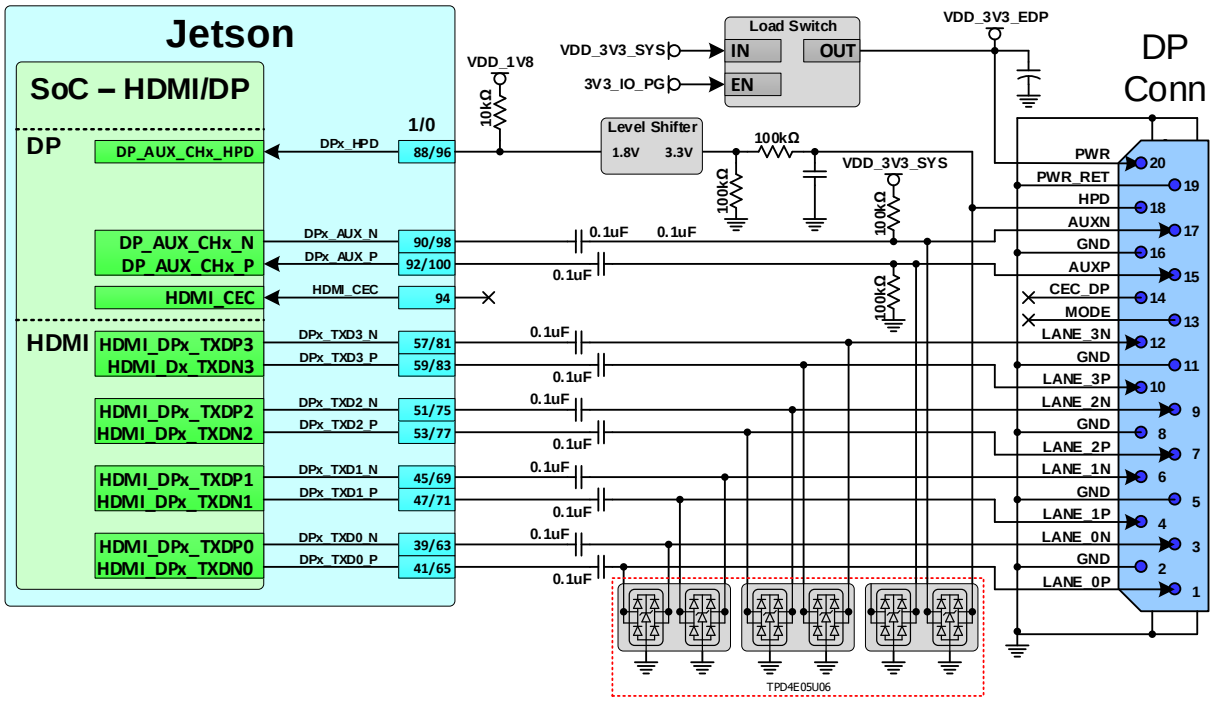
Table 5-2. DP and HDMI Pin Mapping

Module Pin Name	Module Pin #s	HDMI	DP
DP[1:0]_TXD3_P DP[1:0]_TXD3_N	59/83 57/81	TXC+ TXC –	TX3+ TX3–
DP[1:0]_TXD2_P DP[1:0]_TXD2_N	53/77 51/75	TX0+ TX0–	TX2+ TX2–
DP[1:0]_TXD1_P DP[1:0]_TXD1_N	47/71 45/69	TX1+ TX1–	TX1+ TX1–
DP[1:0]_TXD0_P DP[1:0]_TXD0_N	41/65 39/63	TX2+ TX2–	TX0+ TX0–

5.1 eDP and DP

Figure 5-1 shows the DP and eDP connection example.

Figure 5-1. DP and eDP Connection Example



Notes: Level shifter required on DP0_HPD to avoid the pin from being driven when Jetson Xavier NX is off. The level shifter must be non-inverting (preserve the polarity of the HPD signal from the display).

Load Switch enable is from powergood pin of main 3.3V supply.

5.1.1 eDP and DP Routing Guidelines

The following routing requirements meet the eDP and DP routing guidelines.

Figure 5-2. eDP and DP Differential Main Link Topology

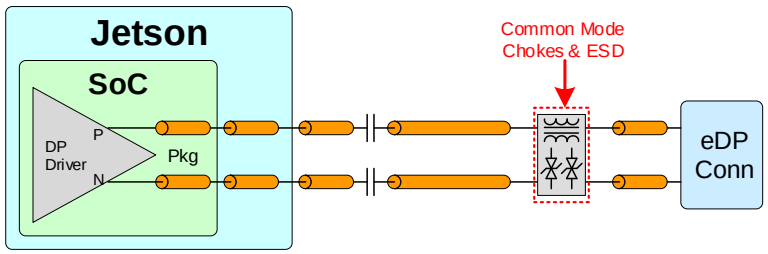


Table 5-3. ePD and DP Main Link Signal Requirements Including DP_AUX

Parameter		Requirement	Units	Notes
Specification				
Max data rate / Min UI	RBR HBR HBR2 HBR3	1.62 / 617 2.7 / 370 5.4 / 185 8.1 / 123	Gbps / ps	Per data lane
Number of loads / topology		1	load	Point-Point, differential, unidirectional
Termination		100	Ω	On die at TX/RX
Electrical Spec				
IL (min)	RBR HBR HBR2 HBR3	0.7 1.2 2.4 4.0	dB @ 0.81GHz dB @ 1.35GHz dB @ 2.7GHz dB @ 4.05GHz	
Resonance dip frequency (min)		8	GHz	
TDR dip (min)		85	Ω	@ Tr-200ps (10%-90%)
FEXT (max)		40 30 30	dB @ DC dB @ 2.7GHz dB @ 2.7GHz	See Figure 5-3 and TBD
Impedance				
Trace impedance	Diff pair	90-100 85	Ω (±15%)	90Ω–100Ω is the spec. target. 85Ω is an implementation option (Zdiff does not account for trace coupling) 85Ω is preferable as it can provide better trace loss characteristic performance. See Note 1.
Reference plane		GND		
Trace Length, Spacing and Skew				

Parameter	Requirement	Units	Notes
Trace loss characteristic (max) Up to HBR2 HBR3	0.81 0.80	dB/in@ 2.7GHz dB/in@ 4.0GHz	The following max length is derived based on this characteristic. See Note 2.
Max PCB via dist. from connector RBR/HBR HBR2/HBR3	No requirement 7.63 (0.3)	mm (in)	
Max trace length/delay from Jetson Xavier NX TX to connector Up to HBR2 (Stripline/Microstrip) HBR3 (Stripline/Microstrip)	 100 (700)/100 (600) 63.5 (440)/63.5(375)	mm (ps)	175ps/inch assumption for stripline, 150ps/inch for microstrip.
Trace spacing (pair-pair) Stripline Microstrip (HBR/RBR) Microstrip (HBR2/HBR3)	3x 4x 5x	dielectric	
Trace spacing (Main link to AUX) Stripline/Microstrip	3x / 5x	dielectric	
Max intra-pair (within pair) skew	0.15 (1)	mm (ps)	See Note 3
Maxinter-pair (pair-pair) skew	150	ps	See Note 4
Via			
Max GND transition via distance	< 1x	diff pair pitch	For signals switching reference layers, add symmetrical GND stitching via near signal vias.
Via Structure			
Impedance dip (min) Recommended via dimension Drill/Pad for impedance control Antipad (min) Via pitch (min)	97 92 200/400 840 880	Ω @ 200ps Ω @ 35ps um um um	The via dimension is required for HDMI-DP co-layout.
Topology	Y-pattern is recommended keep symmetry		Y-pattern helps with Xtalk suppression. It can also reduce the limit of pair-pair distance. Need review (NEXT/FEXT check) if via placement is not Y-pattern. See eDP/DP guideline Figure 5-5
	For in-line via, the distance from a via of one lane to the adjacent via from another lane >= 1.2mm center-center.		See eDP/DP guideline Figure 5-6
GND via	Place GND via as symmetrically as possible to data pair vias. Up to four signal vias (2 diff pairs) can share a single GND return via		GND via is used to maintain a return path, while its Xtalk suppression is limited.
Max # of vias PTH vias Micro vias	2 if all vias are PTH via Not limited as long as total channel loss meets IL spec		
Max via stub length	0.4	mm	
AC Cap			
Value	0.1	uF	Discrete 0402
Max distance from AC cap to connector RBR/HBR HBR2	No requirement 0.5	 in	
Voiding RBR/HBR HBR2	No requirement Voiding required		HBR2: Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.

Parameter		Requirement	Units	Notes
Connector				
Voiding	RBR/HBR HBR2	No requirement Voiding required		HBR2: Standard DP connector: Voiding requirement is stack-up dependent. For typical stack-ups, voiding on the layer under the connector pad is required to be 5.7 mil larger than the connector pad.
General: See Chapter 14 for guidelines related to Serpentine routing, routing over voids and noise coupling				

Notes:

1. For eDP/DP, the spec puts a higher priority on the trace loss characteristic than on the impedance. However, before selecting 85Ω for impedance, it is important to make sure the selected stack-up, material and trace dimension can achieve the needed low loss characteristic.
2. Longer trace lengths may be possible if the total trace loss is equal to or better than the target. If the loss is greater, the max trace lengths will need to be reduced.
3. Do not perform length matching within breakout region. Recommend doing trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion.
4. The average of the differential signals is used for length matching.

The following figures show the eDP and DP interface signal routing requirements.

Figure 5-3. S-Parameter (up to HBR2)

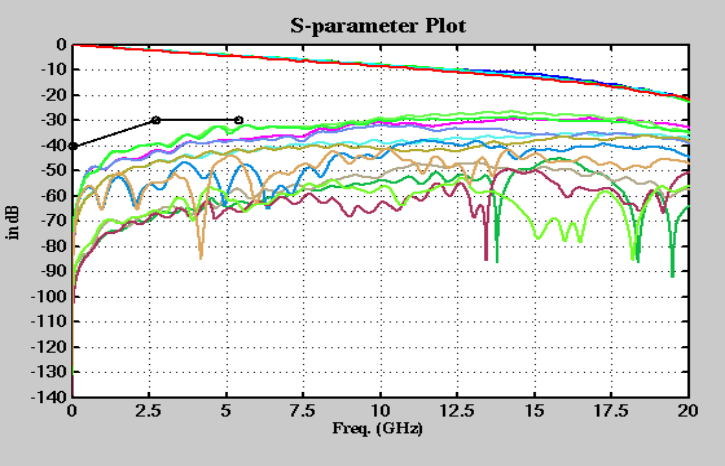


Figure 5-4. S-Parameter (up to HBR3)

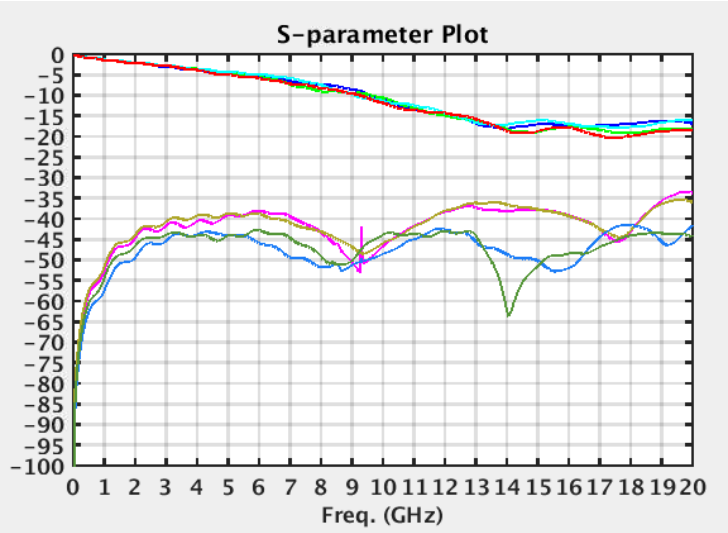


Figure 5-5. Via Topology #1

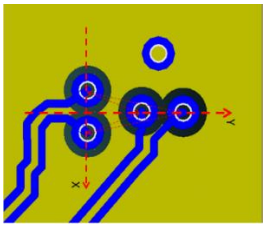


Figure 5-6. Via Topology #2

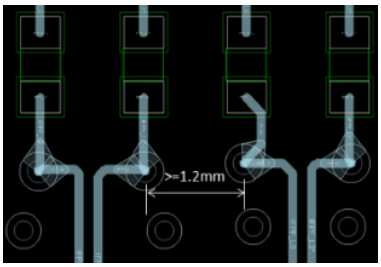


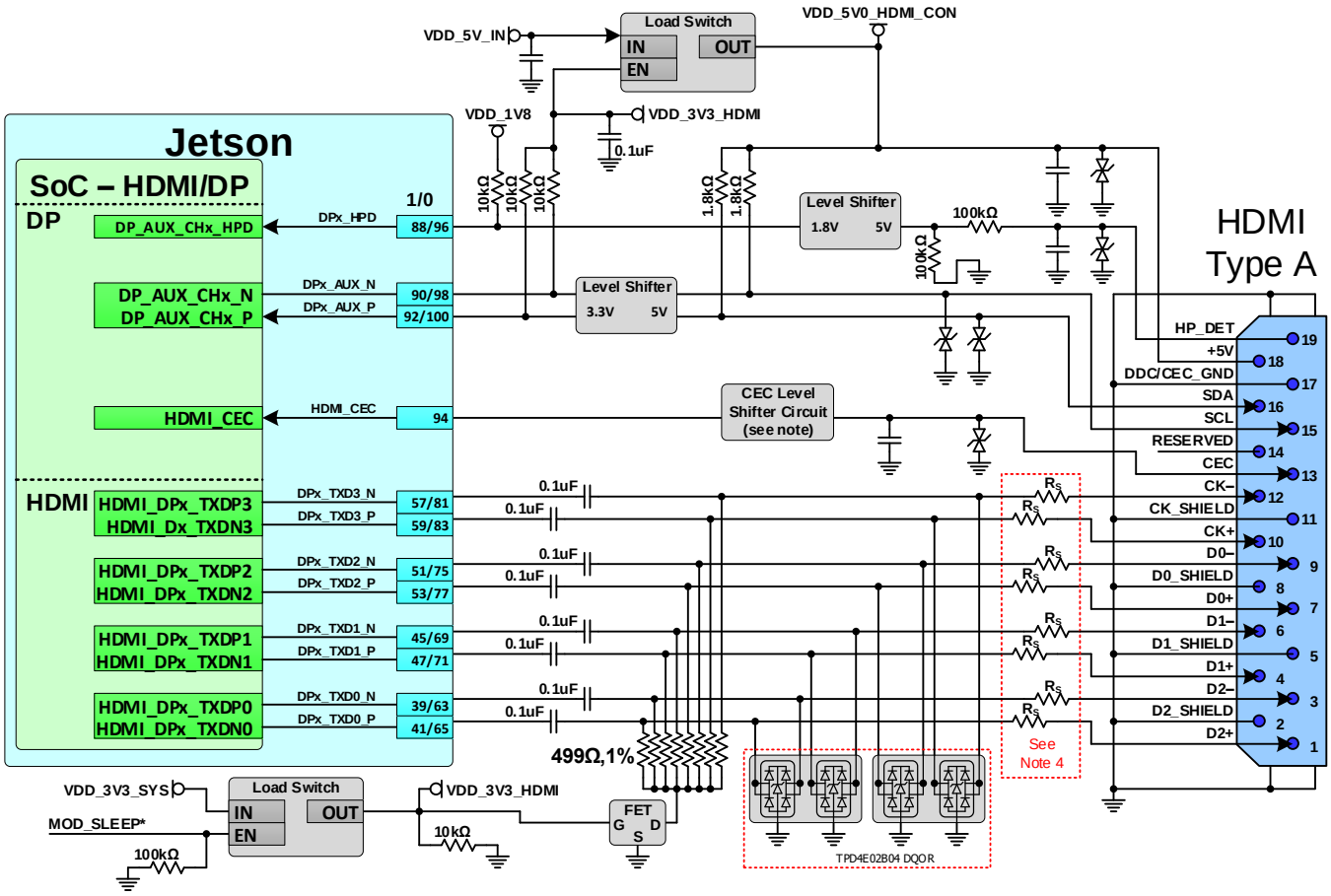
Table 5-4. eDP and DP Signal Connections

Module Pin Name	Type	Termination	Description
DPx_TXD[3:0]_N/P	O	Series 0.1uF capacitors and ESD to GND on all.	**eDP/DP Differential CLK/Data Lanes:** Connect to matching pins on display connector.
DPx_AUX_N/P	I/OD	Series 0.1uF capacitors. 100kΩ pulldown on DP0_AUX_P and 100kΩ pull-up to VDD_3V3_SYS on DP0_AUX_N. ESD to GND on both.	**eDP/DP: Auxiliary Channels:** Connect to AUX_CH-/+ on display connector.
DPx_HPD	I	From module pin: 10kΩ pull-up to 1.8V, level shifter and 100kΩ pulldown, 100kΩ series resistor on connector side of shifter, and ESD to GND.	**eDP/DP: Hot Plug Detect:** Connect to HPD pin on display connector through level shifter.

5.2 HDMI

A standard DP 1.2a or HDMI V2.0 interface is supported. See Figure 5-7 for more details.

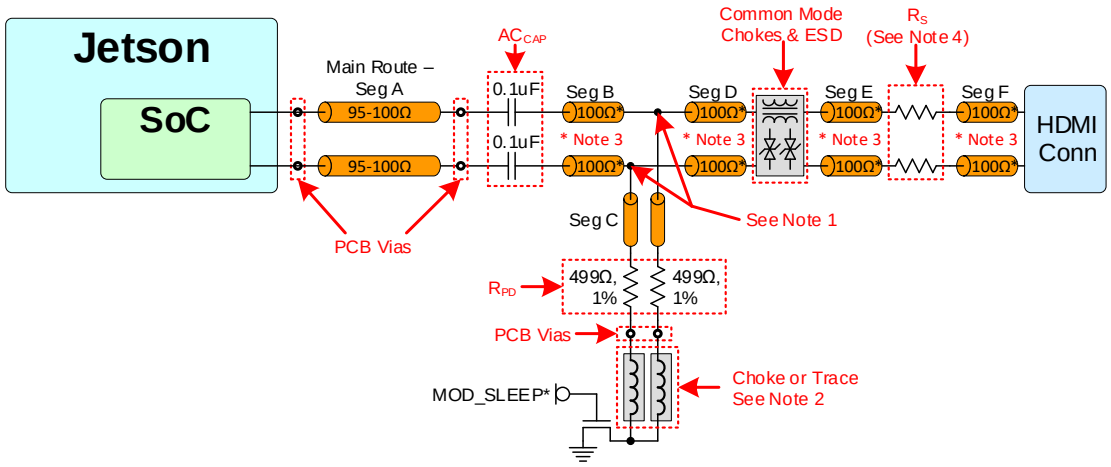
Figure 5-7. HDMI Connection Example



Notes:

1. Level shifters required on DDC/HPD. Xavier pads are not 5V tolerant and cannot directly meet HDMI VIL/VIH requirements. HPD level shifter can be non-inverting or inverting. The HPD level shifter in the reference design is inverting.
2. If EMI/ESD devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing and electrical requirements of the HDMI specification for the modes to be supported. See requirements and recommendations in the related sections of the "HDMI Interface Signal Routing Requirements" table (Table 5-5).
3. The DP1_TXx pads are native DP pads and require series AC capacitors (ACCAP) and pull-downs (RPD) to be HDMI compliant. The 499Ω, 1% pull-downs must be disabled when Jetson Xavier NX is off or in sleep mode to meet the HDMI VOFF requirement. The enable to the FET, enables the pull-downs when the HDMI interface is to be used. Chokes between pull-downs and FET are optional improvements for HDMI 2.0 operation.
4. Series resistors RS are required. See the RS section in Table 5-5 for details.
5. See reference design for CEC level shifting/blocking circuit.

Figure 5-8. HDMI Clk and Data Topology



Notes:

1. RPD pad must be on the main trace. RPD and ACCAP must be on same layer.
2. Chokes (600 Ω @ 100 MHz) or narrow traces (1 uH @ DC-100 MHz) between pull-downs and FET are chokes between pull-downs and FET are optional improvements for HDMI 2.0 operation.
3. The trace after the main route via should be routed on the top or bottom layer of the PCB, and either with 100 ohm differential impedance, or as uncoupled 50 ohm SE traces.
4. RS series resistor is required to meet HDMI 2.0 compliance. See the RS section in Table 5-5 for details.

Table 5-5. HDMI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Max frequency / UI	5.94 / 168	Gbps / ps	Per lane – not total link bandwidth
Topology	Point to point		Unidirectional, differential
Termination At receiver On-board	100 500	Ω	Differential To **3.3V** at receiver To **GND** near connector
Electrical Specification			
IL resonance dip frequency	<= 1.7 <= 2 <= 3 < 6 > 12	dB @ 1GHz dB @ 1.5GHz dB @ 3GHz dB @ 6GHz GHz	
TDR dip	>= 85	Ω @ Tr=200ps	10%-90%. If TDR dip is 75~85ohm that dip width should < 250ps
FEXT (PSFEXT)	<= -50 <= -40 <= -40	dB at DC dB at 3GHz dB at 6GHz	PSNEXT is derived from an algebraic summation of the individual NEXT effects on each pair by the other pairs
	IL/FEXT plot: See HDMI Guideline Figure 5-9		TDR plot: See Figure 5-10
Impedance			
Trace impedance Diff pair	100	Ω	±10%. Target is 100Ω. 95Ω for the breakout and main route is an implementation option.
Reference plane	**GND**		
Trace spacing/Length/Skew			

Parameter	Requirement	Units	Notes
Trace loss characteristic:	< 0.8 < 0.4	dB/in. @ 3GHz dB/in. @ 1.5GHz	The max length is derived based on this characteristic. See Note 1.
Trace spacing (pair-pair) Stripline Microstrip: pre 1.4b Microstrip: 1.4b/2.0	 3x 4x 5x to 7x	dielectric	For Stripline, this is 3x of the thinner of above and below.
Trace spacing (Main link to DDC) Stripline Microstrip	3x 5x	dielectric	For Stripline, this is 3x of the thinner of above and below.
Max total length/delay (1.4b/2.0 - up to 5.94Gbps) Stripline Microstrip (5x spacing) Microstrip (7x spacing)	 63.5/2.5 (437) 50.8/2.0 (300) 63.5/2.5 (375)	 mm/in (ps)	Propagation delay: 175ps/in. for stripline, 150ps/in. for microstrip).
Max Total Length/Delay (Pre-1.4b) (up to 165Mhz) Microstrip Stripline	 254/10 (1500) 225/8.5 (1500)	mm/in (ps)	Propagation delay: 175ps/in. for stripline, 150ps/in. for microstrip).
Max intra-pair (within pair) skew	0.15 (1)	mm (ps)	See notes 1, 2, and 3
Max inter-pair (pair to pair) skew	150	ps	See notes 1, 2, and 3
Max **GND** transition via distance	1x	Diff pair via pitch	For signals switching reference layers, add one or two ground stitching vias. It is recommended they be symmetrical to signal vias.
Via			
Topology	- Y-pattern is recommended - keep symmetry		Xtalk suppression is the best by Y-pattern. Also it can reduce the limit of pair-pair distance. Need review (NEXT/FEXT check) if via placement is not Y-pattern. See Figure 5-11
Minimum impedance dip	97 92	Ω@200ps Ω@35ps	
Recommended via dimension drill/pad Antipad via pitch	 200/400 840 880	 uM	
GND via	Place **GND** via as symmetrically as possible to data pair vias. Up to four signal vias (2 diff pairs) can share a single **GND** return via		**GND** via is used to maintain return path, while its Xtalk suppression is limited
Max # of vias PTH via u-via	4 if all vias are PTH via Not limited as long as total channel loss meets IL spec.		
Max via stub length	0.4	mm	long via stub requires review (IL and resonance dip check)
Topology			
The main route via dimensions should comply with the via structure rules (See via section)			See topology in Figure 5-8
For the connector pin vias, follow the rules for the connector pin vias (See via section)			
The traces after main route via should be routed as 100Ω differential or as uncoupled 50ohm SE traces on PCB top or bottom.			
Max distance from R_{PD} to main trace (seg B)	1	mm	
Max distance from AC cap to RPD stubbing point (seg A)	~0	mm	
Max distance between ESD and signal via	3	mm	
Add-on Components			
Example of a case where space is limited for placing components.	Top: See Figure 5-12		Bottom: See Figure 5-12
AC Cap			
Value	0.1	uF	
Max via distance from BGA	7.62 (52.5)	mm (ps)	
Location	must be placed before pull-down resistor		The distance between the AC cap and the HDMI connector is not restricted.
Placement PTH design Micro-via design	Place cap on bottom layer if main route above core Place cap on top layer if main route below core Not Restricted		
Void	GND (or PWR) void under/above the cap is needed. Void size = SMT area + 1x dielectric height keepout distance		See Figure 5-13
Pull-down Resistor (R_{PD}), choke/FET			

Parameter	Requirement	Units	Notes
Value	500	Ω	
Location.	Must be placed after AC cap		Placement: See Figure 5-15
Layer of placement	Same layer as AC cap. The FET and choke can be placed on the opposite layer thru a PTH via		
Choke between R_{PD} and FET choke Max trace Rdc Max trace length	600 or 1 ≤20 4	Ω@100MHz uH@DC-100MHz mΩ mm	Can be choke or Trace. Recommended option for HDMI2.0 HF1-9 improvement.
Void	**GND/PWR** void under/above cap is preferred		
Common-mode Choke (Not recommended – only used if absolutely required for EMI issues) **See Chapter 14 for details on CMC if implemented.**			
ESD (On-chip protection diode can withstand 2kV HMM. External ESD is optional. Designs should include ESD footprint as a stuffing option)			
Max junction capacitance (IO to **GND**)	0.35	pF	e.g. Texas Instruments TPD4E02B04DQAR
Footprint	Pad right on the net instead of trace stub		See Figure 5-16
Location	After pull-down resistor/CMC and before R_S		
Void	**GND/PWR** void under/above the cap is needed. Void size = 1mm x 2mm for 1 pair		See Figure 5-17
Series Resistor (R_S) – Series resistor on N/P path for HDMI 2.0 (mandatory)			
Value	≤ 6	Ω	± 10%. 0ohm is acceptable if the design passes the HDMI2.0 HF1-9 test. Otherwise, adjust the R_S value to ensure the HDMI2.0 tests pass: Eye diagram, Vlow test and HF1-9 TDR test
Location	After all components and before HDMI connector		
Void	**GND/PWR** void under/above the R_S device is needed. Void size = SMT area + 1x dielectric height keepout distance.		
Trace at Component Region			
Value	100	Ω	± 10%
Location	At component region (Microstrip)		
Trace entering the SMT pad	One 45°		See Figure 5-18
Trace between components	Uncoupled structure		See Figure 5-19
HDMI connector			
Connector voiding	Voiding the ground below the signal lanes 0.1448(5.7mil) larger than the pin itself		See Figure 5-20
General: See Chapter 14 for guidelines related to Serpentine routing, routing over voids and noise coupling			

Notes:

1. Longer trace lengths may be possible if the total trace loss is equal to or better than the target. If the loss is greater, the max trace lengths will need to be reduced.
2. The average of the differential signals is used for length matching.
3. Do not perform length matching within breakout region. Recommend doing trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion
4. If routing includes a flex or 2nd PCB, the max trace delay and skew calculations must include all the PCBs/flex routing. Solutions with flex/2nd PCB may not achieve maximum frequency operation.

The following figures show the HDMI interface signal routing requirements.

Figure 5-9. IL/FEXT Plot

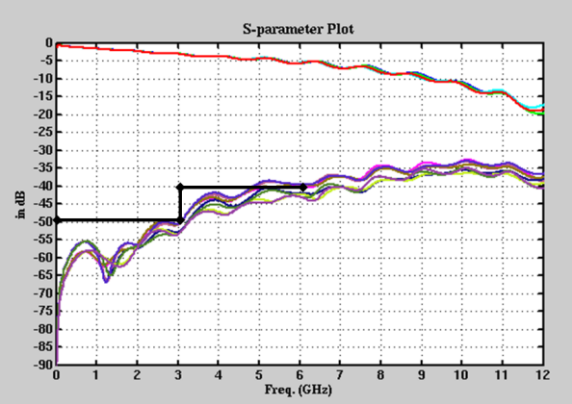


Figure 5-10. TDR Plot

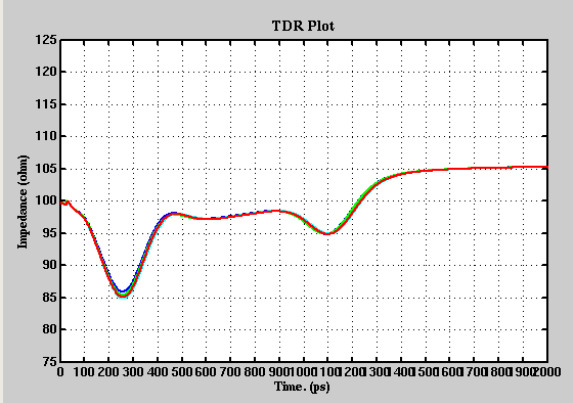


Figure 5-11. HDMI Via Topology

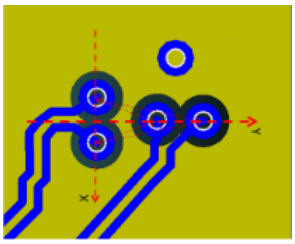


Figure 5-12. Add-On Components – Top

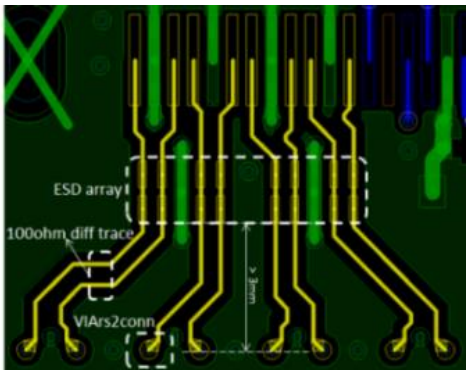


Figure 5-13. Add-on Components – Bottom

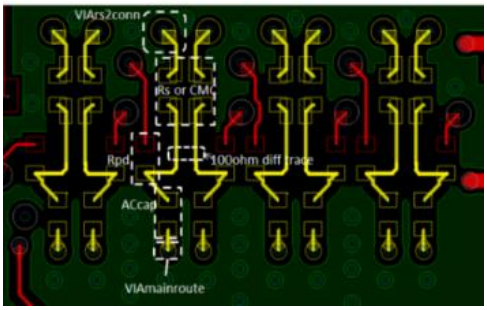


Figure 5-14. AC Cap Void

Figure 5-15. RPD/Choke, FET Placement

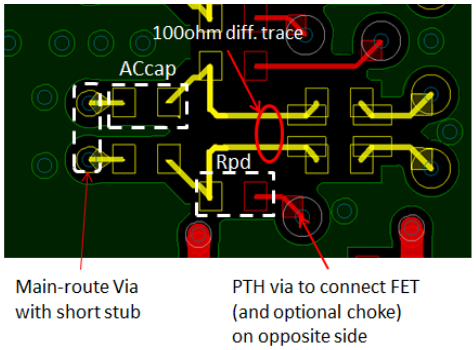


Figure 5-16. ESD Footprint

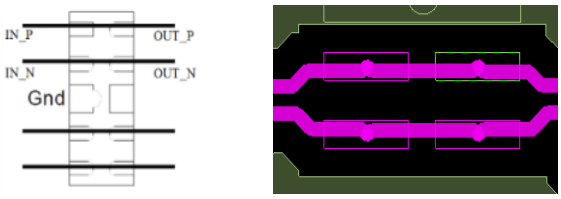


Figure 5-17. ESD Void

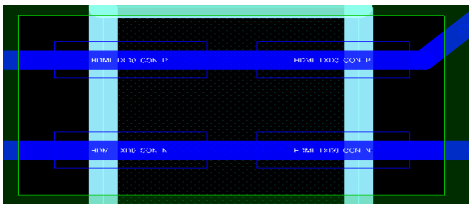


Figure 5-18. SMT Pad Trace Entering

Figure 5-19. SMT Pad Trace Between

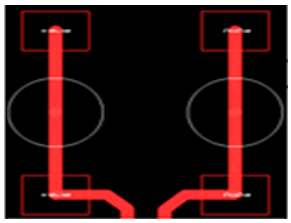


Figure 5-20. Connector Voiding

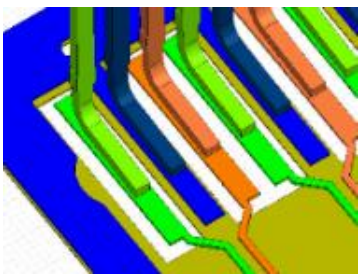


Table 5-6. HDMI Signal Connections

Module Pin Name	Type	Termination (see note on ESD)	Description
DPx_TXD3_N/P	DIFF OUT	0.1uF series AC_{CAP} → 500Ω R_{PD} (controlled by FET) → ESD to **GND** →.≤6Ω R_S (series resistor)	**HDMI Differential Clock:** Connect to **C–/C+** and pins on HDMI connector
DPx_TXD[2:0]_N/P	DIFF OUT		**HDMI Differential Data:** Connect to HDMI Data pins (See Table 5-2)
DPx_HPD	I	From module pin: 10kΩ PU to 1.8V → level shifter → 100kΩ series resistor. 100kΩ to **GND** on connector side → 100pF/12pF caps to **GND** → ESD to **GND**.	**HDMI Hot Plug Detect:** Connect to **HPD** pin on HDMI connector
HDMI_CEC	I/OD	Gating circuitry, See connection figure for details.	**HDMI Consumer Electronics Control:** Connect to CEC on HDMI connector through circuitry.
DPx_AUX_N/P	I/OD	From module pins: 10kΩ PU to 3.3V → level shifter → 1.8kΩ PU to 5V → ESD to **GND**	**HDMI: DDC Interface –** Clock and Data: Connect **DP1_AUX_N** to **SDA** and **DP1_AUX_P** to **SCL** on HDMI connector
HDMI 5V Supply	P	Adequate decoupling (0.1uF and 10uF recommended) on supply near connector and ESD to **GND**.	**HDMI 5V supply to connector:** Connect to +5V on HDMI connector.

Note: Any ESD and/or EMI solutions must support targeted modes (frequencies).

Chapter 6. MIPI CSI Video Input

Jetson Xavier NX brings twelve MIPI CSI lanes to the connector. Up to three quad-lane camera streams or six dual-lane camera streams are supported. Each data lane has a peak bandwidth of up to 2.5 Gbps.

Table 6-1. Jetson Xavier NX CSI Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
10	CSI0_CLK_N	CSI_A_CLK_N	Camera, CSI 0 Clock	2-lane Camera #1, 4-lane Camera #1 (lower 2 lanes)	Input	MIPI D-PHY	–	z
12	CSI0_CLK_P	CSI_A_CLK_P					–	z
4	CSI0_D0_N	CSI_A_D0_N	Camera, CSI 0 Data 0				–	z
6	CSI0_D0_P	CSI_A_D0_P					–	z
16	CSI0_D1_N	CSI_A_D1_N	Camera, CSI 0 Data 1				–	z
18	CSI0_D1_P	CSI_A_D1_P					–	z
9	CSI1_CLK_N	CSI_B_CLK_N	Camera, CSI 1 Clock	2-lane Camera #2, 4-lane Camera #1 (upper 2 lanes)			–	z
11	CSI1_CLK_P	CSI_B_CLK_P					–	z
3	CSI1_D0_N	CSI_B_D0_N	Camera, CSI 1 Data 0				–	z
5	CSI1_D0_P	CSI_B_D0_P					–	z
15	CSI1_D1_N	CSI_B_D1_N	Camera, CSI 1 Data 1				–	z
17	CSI1_D1_P	CSI_B_D1_P					–	z
28	CSI2_CLK_N	CSI_C_CLK_N	Camera, CSI 2 Clock	2-lane Camera #3, 4-lane Camera #2 (lower 2 lanes)			–	z
30	CSI2_CLK_P	CSI_C_CLK_P					–	z
22	CSI2_D0_N	CSI_C_D0_N	Camera, CSI 2 Data 0				–	z
24	CSI2_D0_P	CSI_C_D0_P					–	z
34	CSI2_D1_N	CSI_C_D1_N	Camera, CSI 2 Data 1				–	z
36	CSI2_D1_P	CSI_C_D1_P					–	z
27	CSI3_CLK_N	CSI_D_CLK_N	Camera, CSI 3 Clock	2-lane Camera #4, 4-lane Camera #2 (upper 2 lanes)			–	z
29	CSI3_CLK_P	CSI_D_CLK_P					–	z
21	CSI3_D0_N	CSI_D_D0_N	Camera, CSI 3 Data 0				–	z
23	CSI3_D0_P	CSI_D_D0_P					–	z
33	CSI3_D1_N	CSI_D_D1_N	Camera, CSI 3 Data 1				–	z
35	CSI3_D1_P	CSI_D_D1_P					–	z
52	CSI4_CLK_N	CSI_E_CLK_N	Camera, CSI 4 Clock				–	z

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
54	CSI4_CLK_P	CSI_E_CLK_P		2-lane Camera #5, 4-lane Camera #3 (lower 2 lanes)			–	z
46	CSI4_D0_N	CSI_E_D0_N	Camera, CSI 4 Data 0				–	z
48	CSI4_D0_P	CSI_E_D0_P					–	z
58	CSI4_D1_N	CSI_E_D1_N	Camera, CSI 4 Data 1				–	z
60	CSI4_D1_P	CSI_E_D1_P					–	z
40	CSI4_D2_N	CSI_F_D0_N	Camera, CSI 4 Data 2	4-lane Camera #3 (upper 2 lanes)			–	z
42	CSI4_D2_P	CSI_F_D0_P					–	z
64	CSI4_D3_N	CSI_F_D1_N	Camera, CSI 4 Data 3				–	z
66	CSI4_D3_P	CSI_F_D1_P					–	z
76	DSI_CLK_N	CSI_G_CLK_N	Camera, CSI 5 Clock	2-lane Camera #6			–	z
78	DSI_CLK_P	CSI_G_CLK_P					–	z
70	DSI_D0_N	CSI_G_D0_N	Camera, CSI 5 Data 0				–	z
72	DSI_D0_P	CSI_G_D0_P					–	z
82	DSI_D1_N	CSI_G_D1_N	Camera, CSI 5 Data 1				–	z
84	DSI_D1_P	CSI_G_D1_P					–	z

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 6-2. Jetson Xavier NX Camera Miscellaneous Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
213	CAM_I2C_SCL	CAM_I2C_SCL	Camera I2C Clock. 2.2kΩ pull-up to 3.3V on the module.	Cameras (shared)	Bidir	Open Drain – 3.3V	DD	z
215	CAM_I2C_SDA	CAM_I2C_SDA	Camera I2C Data. 2.2kΩ pull-up to 3.3V on the module.				DD	z
116	CAM0_MCLK	EXTPERIPH1_CLK	Camera 0 Reference Clock	Camera #1	Output	CMOS – 1.8V	ST	pd
114	CAM0_PWDN	SOC_GPIO04	Camera 0 Powerdown or GPIO				ST	pd
122	CAM1_MCLK	EXTPERIPH2_CLK	Camera 1 Reference Clock	Camera #2			ST	pd
120	CAM1_PWDN	SOC_GPIO05	Camera 1 Powerdown or GPIO				ST	pd
118	GPIO01	SOC_GPIO41	GPIO #1 or Generic Clock Output #1	Camera #3	Output (note)		DD	pd
216	GPIO11	SOC_GPIO42	GPIO #11 or Generic Clock Output #2	Camera #4			DD	pd

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.
4. The direction indicated for GPIO01 and GPIO11 is associated with their use as clock outputs.

Figure 6-1. 4 Lane CSI Camera Connection Example

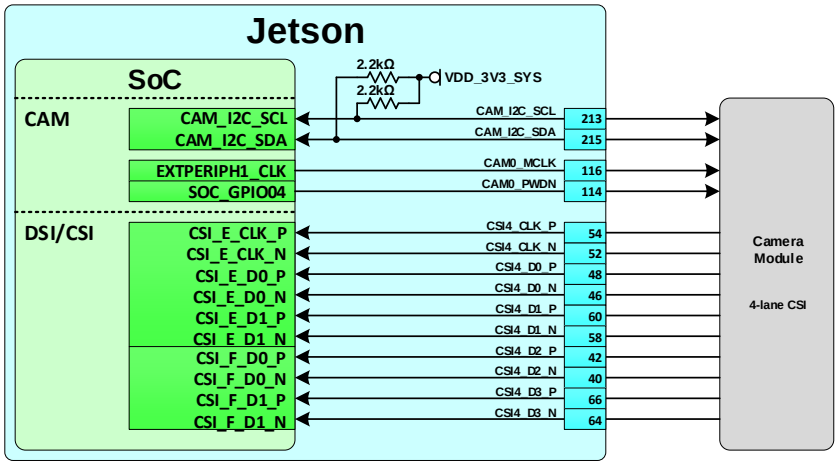


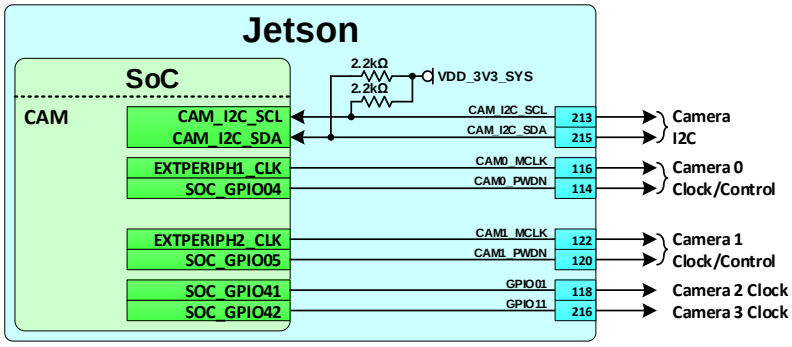
Table 6-3. CSI Configurations

Cameras	CSI0 CLK/Data[1:0]	CSI1 CLK	CSI1 Data[1:0]	CSI2 CLK/Data[1:0]	CSI3 CLK	CSI3 Data[1:0]	CSI4 CLK/Data[1:0]	CSI4 DATA[3:2]	CSI5 (DSI pins) CLK/Data[1:0]
2-Lanes Each									
1 of 6 cameras	√								
2 of 6 cameras		√	√						
3 of 6 cameras				√					
4 of 6 cameras					√	√			
5 of 6 cameras							√		
6 of 6 cameras									√
4-Lanes Each									
1 of 3 cameras	√		√						
2 of 3 cameras				√		√			
3 of 3 cameras							√	√	

Notes:

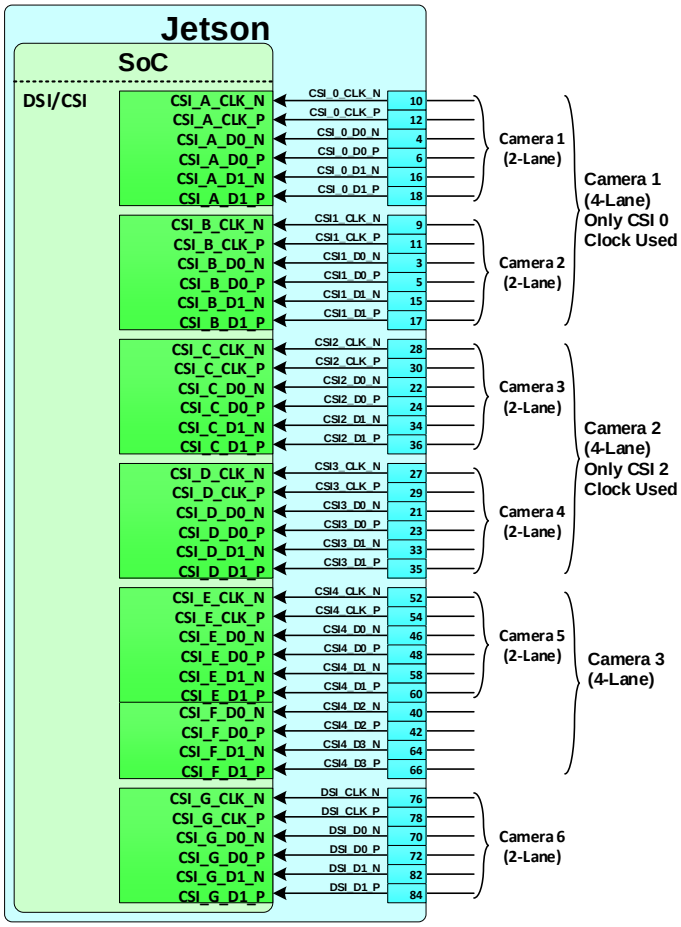
1. CSI 4 can be used as as a x1, x2, or x4 CSI interface.
2. Each 2-lane options shown can also be used for one single lane camera.

Figure 6-2. Available Camera Control Pins



Note: The CAM_I2C interface is connected to the power monitor device on the module which uses I2C address 7'h40.

Figure 6-3. CSI Connection Options



6.1 CSI Design Guidelines

The following tables describe the design guidelines for the CSI design.

Table 6-4. MIPI CSI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate (per data lane) for High-Speed mode Max Frequency (for Low Power mode)	2.5 10	Gbps MHz	
Number of loads	1	load	
Max Loading (per pin)	10	pF	
Reference plane	GND		
Trace impedance Diff pair / SE	90-100 / 45-50	Ω	±10%
Via proximity (signal to reference)	< 0.65 (3.8)	mm (ps)	
Intra-pair trace spacing	0.15mm	mm	Can be adjusted to meet Differential Impedance. Loosely Coupled Diff. Pair recommended by Spec.
Trace spacing Microstrip / Stripline	2x / 2x	dielectric	
Max PCB breakout delay	48	ps	
Max trace delay 1 Gbps 1.5 Gbps 2.5 Gbps	1100 800 350	ps	
Max intra-pair skew	1	ps	
Max trace delay skew between **DQ** and **CLK** **1 / 1.5 / 2.5 Gbps**	10 / 26.7 / 16	ps	DQ includes all the data lines associated with a single clock. This may be 2 differential data lanes for a x2 interface, or 4 differential data lanes for a x4 interface.
Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components			

Note: Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing and Vil/Vih requirements at the receiver and maintain signal quality and meet requirements for the frequencies supported by the design.

Table 6-5. MIPI CSI Signal Connections

Module Pin Name	Type	Termination	Description
CSI[4:0]_CLK_N/P Camera #[5:1] DSI_CLK_N/P Camera #6	I	See note	**CSI Differential Clocks:** Connect to clock pins of camera. See Table 6-3 for details
CSI[3:0]_D[1:0]_N/P Camera #[4:1] CSI4_D[3:0]_N/P Camera #5 DSI_D[1:0]_N/P Camera #6	I/O	See note	**CSI Differential Data Lanes:** Connect to data pins of camera. See Table 6-3 for details

Table 6-6. Miscellaneous Camera Connections

Module Pin Name	Type	Termination	Description
CAM_I2C_CLK CAM_I2C_DAT	O I/O	2.2kΩ pull-ups **VDD_3V3_SYS** (on Jetson Xavier NX).	**Camera I2C Interface:** Connect to I2C SCL and SDA pins of imager. The CAM_I2C interface is connected to the power monitor device on the module which uses I2C address 7'h40.
CAM[1:0]_MCLK GPIO01 (opt. MCLK2) GPIO11 (opt. MCLK3)	O		**Camera Master Clocks:** Connect to camera reference clock inputs.
CAM[1:0]_PWDN	O		**Camera Power Control signals (or GPIOs [1:0]):** Connect to power down pins on camera(s).

Chapter 7. SD Card and SDIO

Jetson Xavier NX uses one SDMMC interface for on-module eMMC (SDMMC4 on Xavier) and brings one to the connector pins for SD Card or SDIO use.

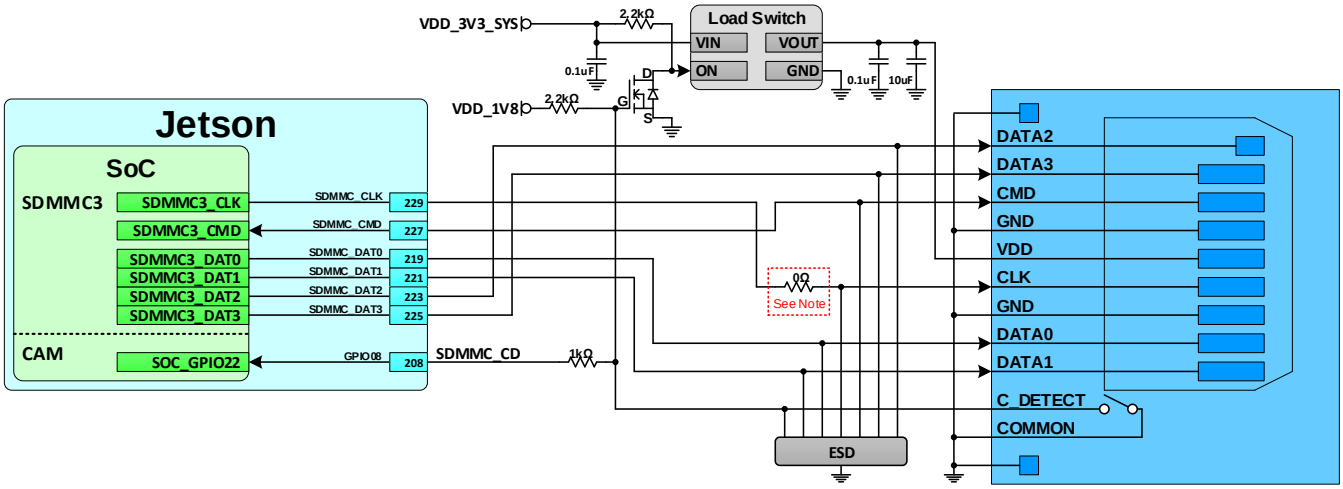
Table 7-1. Jetson Xavier NX SDIO Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
229	SDMMC_CLK	SDMMC3_CLK	SD Card or SDIO Clock	SD Card or SDIO Device	Output	CMOS – 1.8V/3.3V	CZ	pd
227	SDMMC_CMD	SDMMC3_CMD	SD Card or SDIO Command		Bidir		CZ	pd
219	SDMMC_DAT0	SDMMC3_DAT0	SD Card or SDIO Data 0				CZ	pd
221	SDMMC_DAT1	SDMMC3_DAT1	SD Card or SDIO Data 1				CZ	pd
223	SDMMC_DAT2	SDMMC3_DAT2	SD Card or SDIO Data 2				CZ	pd
225	SDMMC_DAT3	SDMMC3_DAT3	SD Card or SDIO Data 3				CZ	pd
208	GPIO08	SOC_GPIO22	GPIO #8 or SD Card Detect	SD Card Detect or Fan Tach	Input (note)	CMOS – 1.8V	ST	pd

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. If the SDMMC pins are connected to a 1.8V only device, the interface voltage should be configured for 1.8V operation in the Pinmux.
3. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
4. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.
5. The direction indicated for GPIO08 is associated with its use as SD Card Select.

Figure 7-1. SD Card Connection Example



Note: Having 0Ω, 0402 resistor is recommended in case of issues with EMI where it can be replaced with an appropriate device.

Table 7-2. SD Card and SDIO Interface Signal Routing Requirements

Parameter			Requirement	Units	Notes
Max frequency	3.3V Signaling	DS	25 (12.5)	MHz (MB/s)	See Note 1
		HS	50 (25)		
	1.8V Signaling	SDR12	25 (12.5)		
		SDR25	50 (25)		
		SDR50	100 (50)		
		SDR104	208 (104)		
		DDR50	50 (50)		
Topology			Point to point		
Reference plane			GND or PWR		See Note 2
Trace impedance			50	Ω	±15%. 45Ω optional depending on stack-up
Max via count		PTH	4		Independent of stack-up layers.
		HDI	10		Depends on stack-up layers.
Via proximity (Signal to reference)			< 3.8 (24)	mm (ps)	Up to four signal vias can share 1 GND return via
Trace spacing	Microstrip / Stripline		4x / 3x	dielectric	
Trace length					
SDR50 / SDR25 / SDR12 / HS / DS		Min	16 (100)	mm (ps)	
		Max	139 (876)		
SDR104 / DDR50		Min	16 (100)		
		Max	83 (521)		
Max trace length/delay skew in/between CLK and CMD/DAT					See Note 3

Parameter	Requirement	Units	Notes
SDR50 / SDR25 / SDR12 / HS / DS SDR104 / DDR50	14 (87.5) 2 (12.5)	mm (ps)	
Keep CLK, CMD and DATA traces away from other signal traces or unrelated power traces/areas or power supply components			

Notes:
1. Actual frequencies may be lower due to clock source/divider limitations.
2. If PWR, 0.01uF decoupling cap required for return current.

Table 7-3. SD Card and SDIO Signal Connections

Function Signal Name	Type	Termination	Description
SDMMC_CLK	O		SD Card / SDIO Clock: Connect to CLK pin of device.
SDMMC_CMD	I/O		SD Card / SDIO Command: Connect to CMD pin of device
SDMMC_D[3:0]	I/O		SD Card / SDIO Data: Connect to Data pins of device
GPIO08	I		SD Card Detect (Optional): Connect to CD pin of SD Card socket.

Chapter 8. Audio

Xavier supports multiple PCM and I2S audio interfaces. It also includes a flexible audio port switching architecture.

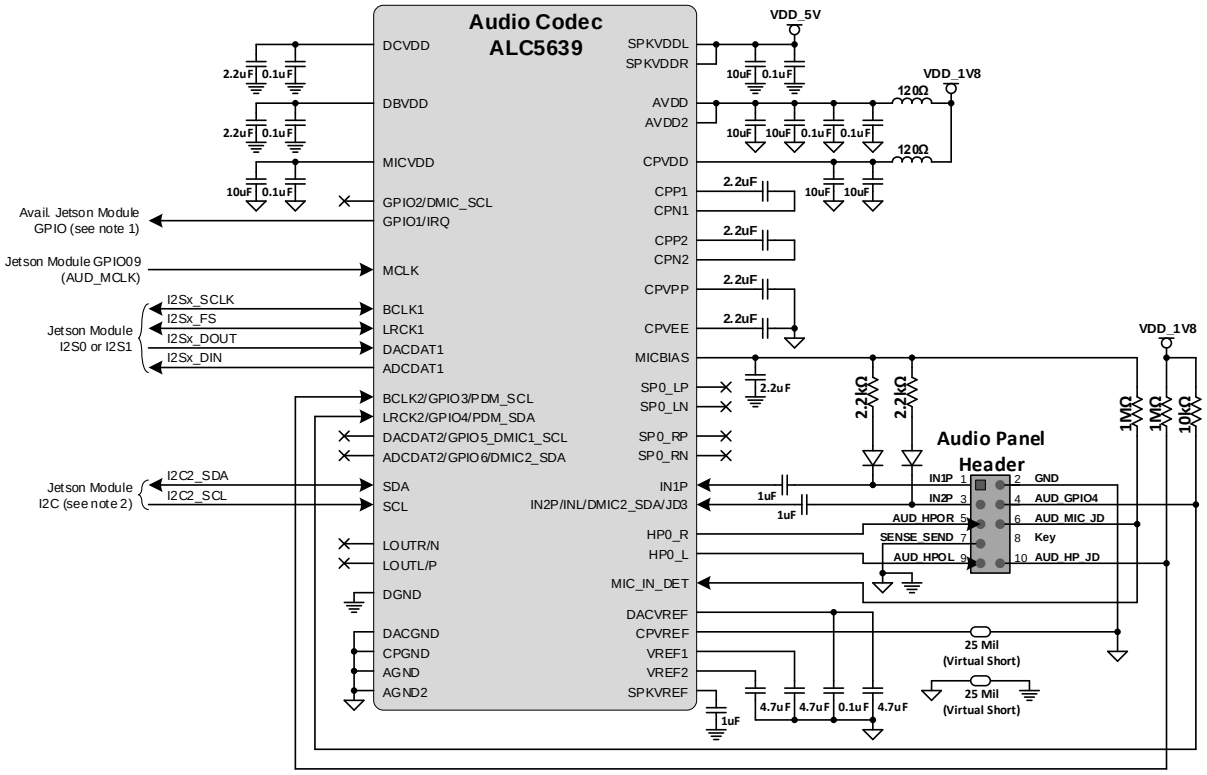
Table 8-1. Jetson Xavier NX Audio Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
199	I2S0_SCLK	DAP5_SCLK	I2S Audio Port 0 Clock	Audio Device	Bidir	CMOS – 1.8V	ST	pd
197	I2S0_FS	DAP5_FS	I2S Audio Port 0 Left/Right Clock		Bidir		ST	pd
193	I2S0_DOUT	DAP5_DOUT	I2S Audio Port 0 Data Out		Output (note)		ST	pd
195	I2S0_DIN	DAP5_DIN	I2S Audio Port 0 Data In		Input (note)		ST	pd
226	I2S1_SCLK	DAP3_SCLK	I2S Audio Port 1 Clock	Audio Device (i.e. M.2 Key E)	Bidir		ST	pd
224	I2S1_FS	DAP3_FS	I2S Audio Port 1 Left/Right Clock		Bidir		ST	pd
220	I2S1_DOUT	DAP3_DOUT	I2S Audio Port 1 Data Out		Output (note)		ST	pd
222	I2S1_DIN	DAP3_DIN	I2S Audio Port 1 Data In		Input (note)		ST	pd
211	GPIO09	AUD_MCLK	GPIO #9 or Audio Codec Master Clock	Audio Device	Output (note)		ST	pd

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described *in the Xavier Series (SoC) Technical Reference* Manual "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.
4. The direction indicated for I2S[1:0]_DOUT and _DIN are associated with their use as I2S data lines. The direction for GPIO09 is associated with its use as Audio Master Clock.

Figure 8-1. Audio Codec Connection Example



Notes:

1. The Interrupt pin from the audio codec can connect to any available Jetson Xavier NX GPIO. If the pin must be wake-capable, choose one of the GPIOs that supports this function.
2. I2C2 supports 1.8V operation since the interface is pulled to 1.8V through 4.7kΩ resistors on the module. If another I2C interface on Jetson Xavier NX is used, a level shifter will be required as all the others are 3.3V.

Table 8-2. I2S Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Configuration / device organization	1	load	
Max loading	8	pF	
Reference plane	GND		
Breakout region impedance	Min width/spacing		
Trace impedance	50	Ω	±20%
Via proximity (signal to reference)	< 3.8 (24)	mm (ps)	See note 1
Trace spacing Microstrip or Stripline	2x	dielectric	
Max trace length/delay	~22 (3600)	In (ps)	See note 2
Max trace length/delay skew between **SCLK** and SDATA_**OUT/IN**	~1.6 (250)	In (ps)	See note 2

Note: Up to four signal vias can share a single GND return via.

Table 8-3. Audio Signal Connection

Module Pin Name	Type	Termination	Description
I2S[1:0]_SCLK	I/O		**I2S Serial Clock:** Connect to I2S/PCM CLK pin of audio device.
I2S[1:0]_FS	I/O		**I2S Frame Select (Left/Right Clock):** Connect to corresponding pin of audio device.
I2S[1:0]_DOUT	I/O		**I2S Data Output:** Connect to data input pin of audio device.
I2S[1:0]_DIN	I		**I2S Data Input:** Connect to data output pin of audio device.
GPIO09	O		**Audio Codec Master Clock:** Connect to clock pin of audio codec.

Chapter 9. Miscellaneous Interfaces

9.1 I2C

Jetson Xavier NX brings four I2C interfaces to the connector pins. **CAM_I2C** is included in the camera pin description table earlier in this design guide. The assignments in the "I2C Interface Mapping" table should be used where applicable for the I2C interfaces.

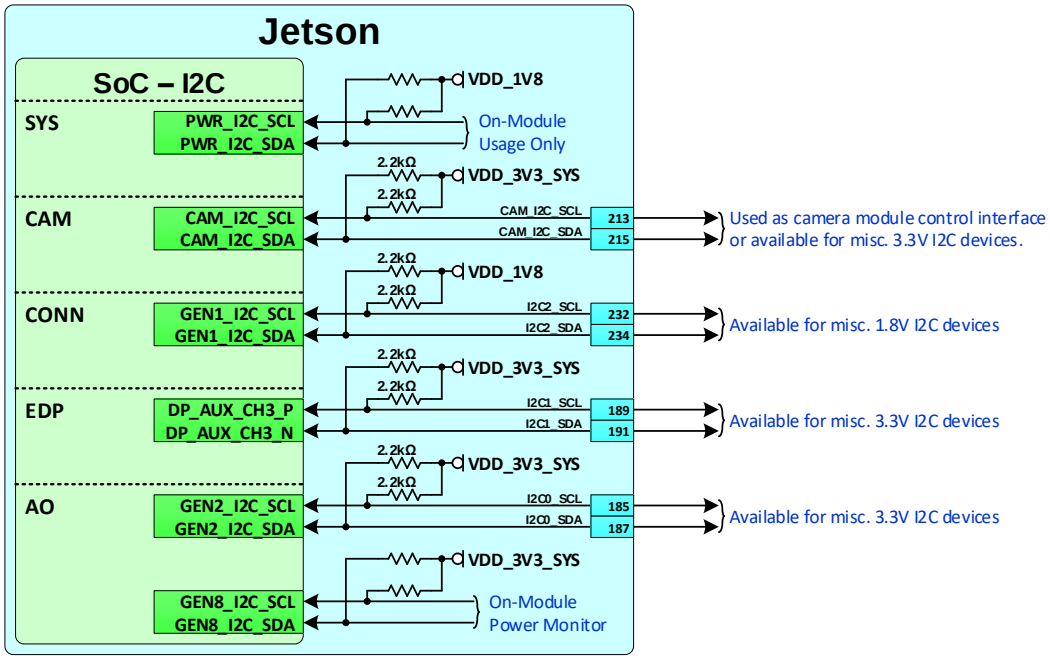
Table 9-1. Jetson Xavier NX I2C Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
185	I2C0_SCL	GEN2_I2C_SCL	General I2C 0 Clock. 2.2kΩ pull-up to 3.3V on module.	I2C (general)	Bidir	Open Drain – 3.3V	DD	z
187	I2C0_SDA	GEN2_I2C_SDA	General I2C 0 Data. 2.2kΩ pull-up to 3.3V on the module.			Open Drain – 3.3V	DD	z
189	I2C1_SCL	DP_AUX_CH3_P	General I2C 1 Clock. 2.2kΩ pull-up to 3.3V on the module.			Open Drain – 3.3V	DP_AUX	z
191	I2C1_SDA	DP_AUX_CH3_N	General I2C 1 Data. 2.2kΩ pull-up to 3.3V on the module.			Open Drain – 3.3V	DP_AUX	z
232	I2C2_SCL	GEN1_I2C_SCL	General I2C 2 Clock. 2.2kΩ pull-up to 1.8V on the module.			Open Drain – 1.8V	DD	z
234	I2C2_SDA	GEN1_I2C_SDA	General I2C 2 Data. 2.2kΩ pull-up to 1.8V on the module.			Open Drain – 1.8V	DD	z

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Figure 9-1. I2C Connections



9.1.1 I2C Design Guidelines

Care must be taken to ensure I2C peripherals on same I2C bus connected to Jetson Xavier NX do not have duplicate addresses. Addresses can be in two forms: 7-bit, with the read/write bit removed or 8-bit including the read/write bit. Be sure to compare I2C device addresses using the same form (all 7-bit or all 8-bit format). The I2C2 interface is connected to an EEPROM on the module which uses I2C address 7'h50. The CAM_I2C interface is connected to the power monitor device on the module which uses I2C address 7'h40.

Note: The Jetson Xavier NX I2C interfaces have 2.2 kΩ pull-ups on the module. Pads for additional pull-ups are recommended in case a stronger pull-up is required due to additional loading on the interfaces.

Table 9-2. I2C Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Max frequency	Standard-mode / Fm / Fm+	100 / 400 / 1000	kHz	See Note 1
Topology		Single ended, bi-directional, multiple masters/slaves		
Max loading	Standard-mode / Fm / Fm+	400	pF	Total of all loads
Reference plane		**GND** or **PWR**		
Trace impedance		50 – 60	Ω	±15%
Trace spacing		1x	dielectric	
Max trace length/delay	Standard Mode Fm, Fm+ Modes	3400 (~20) 1700 (~10)	ps (in)	

Notes:

1. Fm = Fast-mode, Fm+ = Fast-mode Plus
2. Avoid routing I2C signals near noisy traces, supplies or components such as a switching power regulator.
3. No requirement for decoupling caps for PWR reference.

Table 9-3. I2C Signal Connections

Module Pin Name	Type	Termination	Description
I2C0_SCL/SDA	I/OD	2.2kΩ pull-ups to **VDD_3V3_SYS** on Jetson Xavier NX	**I2C #0 Clock and Data.** Connect to CLK and Data pins of any 3.3V devices
I2C1_SCL/SDA	I/OD	2.2kΩ pull-ups to **VDD_3V3_SYS** on Jetson Xavier NX	**I2C #1 Clock and Data.** Connect to CLK and Data pins of 3.3V devices.
I2C2_SCL/SDA	I/OD	2.2kΩ pull-ups to **VDD_1V8** on Jetson Xavier NX	**I2C #2 Clock and Data.** Connect to CLK and Data pins of any 1.8V devices
CAM_I2C_SCL/SDA	I/OD	2.2kΩ pull-ups to **VDD_3V3_SYS** on Jetson Xavier NX	**Camera I2C Clock and Data.** Connect to CLK and Data pins of any 3.3V devices

Notes:

1. If some devices require a different voltage level than others connected to the same I2C bus, level shifters are required.
2. For I2C interfaces that are pulled up to 1.8V, disable the E_IO_HV option for these pads. For I2C interfaces that are pulled up to 3.3V, enable the E_IO_HV option. The E_IO_HV option is selected in the Pinmux registers.

9.2 SPI

The Jetson Xavier NX brings out two of the Xavier SPI interfaces. See Figure 9-2.

Table 9-4. Jetson Xavier NX SPI Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
91	SPI0_SCK	SPI1_SCK	SPI 0 Clock	SPI #0 Device #0 or #1	Bidir	CMOS – 1.8V	ST	pd
93	SPI0_MISO	SPI1_MISO	SPI 0 Master In / Slave Out				ST	pu
89	SPI0_MOSI	SPI1_MOSI	SPI 0 Master Out / Slave In				ST	pu
95	SPI0_CS0*	SPI1_CS0	SPI 0 Chip Select 0	SPI #0 Device #0			ST	pu
97	SPI0_CS1*	SPI1_CS1	SPI 0 Chip Select 1	SPI #0 Device #1			ST	pu
106	SPI1_SCK	SPI3_SCK	SPI 1 Clock	SPI #1 Device #0 or #1			DD	pd
108	SPI1_MISO	SPI3_MISO	SPI 1 Master In / Slave Out				DD	pd
104	SPI1_MOSI	SPI3_MOSI	SPI 1 Master Out / Slave In				DD	pd

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
110	SPI1_CS0*	SPI3_CS0	SPI 1 Chip Select 0	SPI #1 Device #0			DD	z
112	SPI1_CS1*	SPI3_CS1	SPI 1 Chip Select 1	SPI #1 Device #1			DD	z

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Figure 9-2. SPI Connections

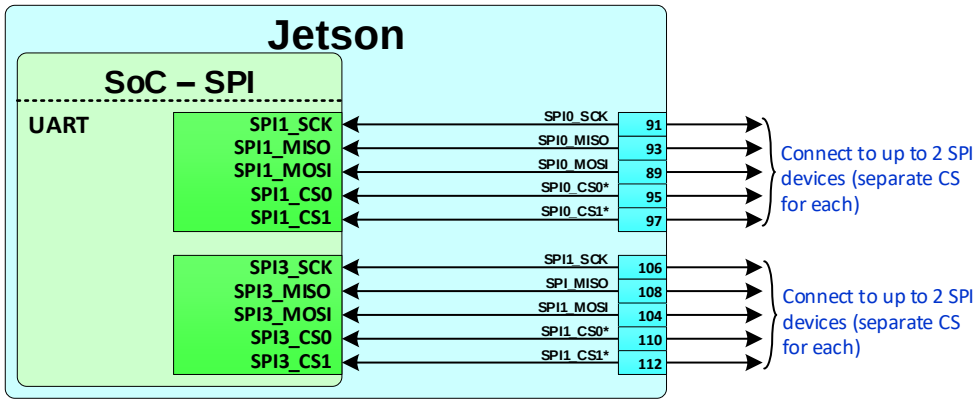
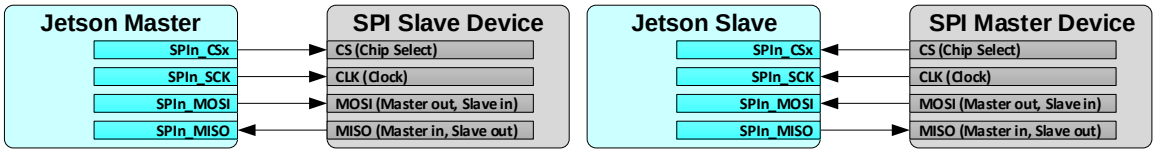


Figure 9-3 shows the basic connections used.

Figure 9-3. Basic SPI Master and Slave Connections



9.2.1 SPI Design Guidelines

The following guidelines meet the SPI design guidelines.

Figure 9-4. SPI Topologies

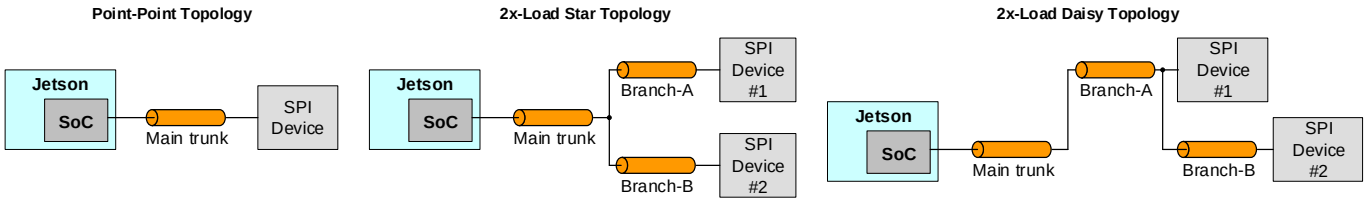


Table 9-5. SPI Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Max frequency		65	MHz	
Configuration / device organization		4	load	
Max loading (total of all loads)		15	pF	
Reference plane		**GND**		
Breakout region impedance		Minimum width and spacing		
Max PCB breakout delay		75	ps	
Trace impedance		50 – 60	Ω	±15%
Via proximity (signal to reference)		< 3.8 (24)	mm (ps)	See Note 1
Trace spacing	Microstrip / Stripline	4x / 3x	dielectric	
Max trace length/delay (PCB main trunk) For **MOSI, MISO, SCK** and **CS**	Point-point 2x-load star/daisy	195 (1228) 120 (756)	mm (ps)	
Max trace length/delay (Branch-A) for **MOSI, MISO, SCK** and **CS**	2x-load star/daisy	75 (472)	mm (ps)	
Max trace length/delay skew from **MOSI, MISO** and **CS** to **SCK**		16 (100)	mm (ps)	At any point

Note: Up to four signal vias can share a single GND return via

Table 9-6. SPI Signal Connections

Module Pin Names (Function)	Type	Termination	Description
SPI[1:0]_CLK **GPIO03 (SPI2_SCK)**	I/O		**SPI Clock.:** Connect to peripheral CLK pin(s)
SPI[1:0]_MOSI **GPIO05 (SPI2_MOSI)**	I/O		**SPI Data Output:** Connect to slave peripheral MOSI pin(s)
SPI[1:0]_MISO **GPIO04 (SPI2_MISO)**	I/O		**SPI Data Input:** Connect to slave peripheral MISO pin(s)
SPI[1:0]_CS[1:0]* **GPIO06 (SPI2_CS0*)**	I/O		**SPI Chip Selects.:** Connect one CSx* pin per SPI interface to each slave peripheral CS pin on the interface

9.3 UART

The Jetson Xavier NX brings three UARTs out to the main connector. See Figure 9-5 for typical assignments of the three available UARTs.

Table 9-7. Jetson Xavier NX UART Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
99	UART0_TXD	UART2_TX	UART 0 Transmit	UART general (i.e. M.2 Key E)	Output	CMOS – 1.8V	DD	pd
101	UART0_RXD	UART2_RX	UART 0 Receive		Input		DD	pd
103	UART0_RTS*	UART2_RTS	UART 0 Request to Send		Output		ST	pd
105	UART0_CTS*	UART2_CTS	UART 0 Clear to Send		Input		ST	pu
203	UART1_TXD	UART1_TX	UART 1 Transmit	UART general	Output		DD	pd
205	UART1_RXD	UART1_RX	UART 1 Receive		Input		DD	z
207	UART1_RTS*	UART1_RTS	UART 1 Request to Send		Output		ST	pd
209	UART1_CTS*	UART1_CTS	UART 1 Clear to Send		Input		ST	pu
236	UART2_TXD	UART3_TX	UART 2 Transmit.	Debug UART	Output		DD	pd
238	UART2_RXD	UART3_RX	UART 2 Receive		Input		DD	pd

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Figure 9-5. Jetson Xavier NX UART Connections

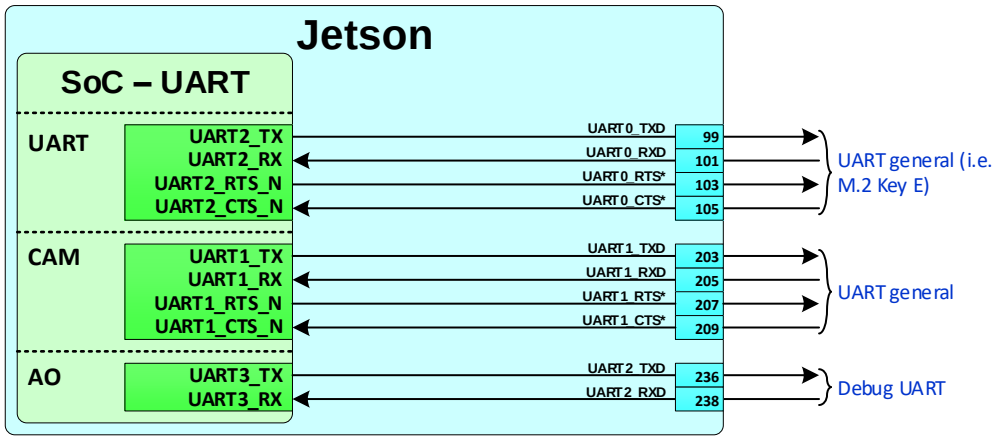


Table 9-8. UART Signal Connections

Ball Name	Type	Termination	Description
UART[2:0]_TXD	O		UART Transmit: Connect to peripheral RXD pin of device
UART[2:0]_RXD	I		UART Receive: Connect to peripheral TXD pin of device
UART[1:0]_CTS*	I		UART Clear to Send: Connect to peripheral RTS pin of device
UART[1:0]_RTS*	O		UART Request to Send: Connect to peripheral CTS pin of device

9.4 CAN

Jetson Xavier NX brings a single controlled area network (CAN) interface to the main connector.

Table 9-9. Jetson Xavier NX CAN Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
143	CAN_RX	CAN0_DIN	CAN Receive	CAN PHY	Input	CMOS – 3.3V	CZ	pu
145	CAN_TX	CAN0_DOUT	CAN Transmit		Output	CMOS – 3.3V	CZ	pu

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Figure 9-6. Jetson Xavier NX CAN Connections

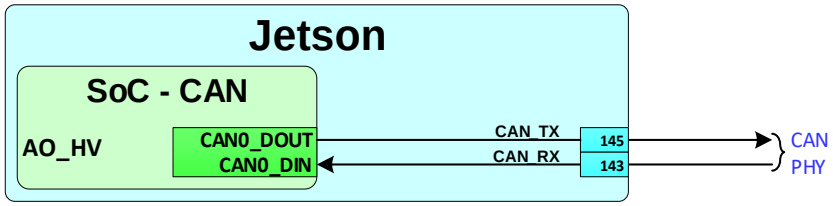


Table 9-10. CAN Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate / Frequency	1	Mbps / MHz	
Configuration / Device Organization	1	load	
Reference plane	**GND**		
Trace Impedance	50	Ω	±15%
Via proximity (Signal via to **GND** return via)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing Microstrip / Stripline	4x / 3x	dielectric	
Max Trace Length (for **RX** & **TX** only)	223 (1360)	mm (ps)	See Note 2
Max Trace Length/Delay Skew from **RX** to **TX**	8 (50)	mm (ps)	See Note 2

Table 9-11. CAN Signal Connections

Module Pin Name	Type	Termination	Description
CAN_TX	O		CAN Transmit: Connect to matching pin of device
CAN_RX	I		CAN Receive: Connect to Peripheral pin of device

9.5 Fan

Jetson Xavier NX provides PWM and Tachometer functionality for controlling a fan as part of the thermal solution. Information on the PWM and Tachometer pins and functions can be found in the following locations:

- Jetson Xavier NX Pin Mux
  - This is used to configure GPIO14 (PWM) for **FAN_PWM** and GPIO08 (SDMMC_CD) for **FAN_TACH**. The pin used for **FAN_PWM** is configured as **GP_PWM6**. The pin used for **FAN_TACH** is configured as a GPIO.
- Xavier (SoC) Technical Reference Manual (TRM)
  - Functional descriptions and related registers can be found in the TRM for the **FAN_PWM** (PWM chapter).

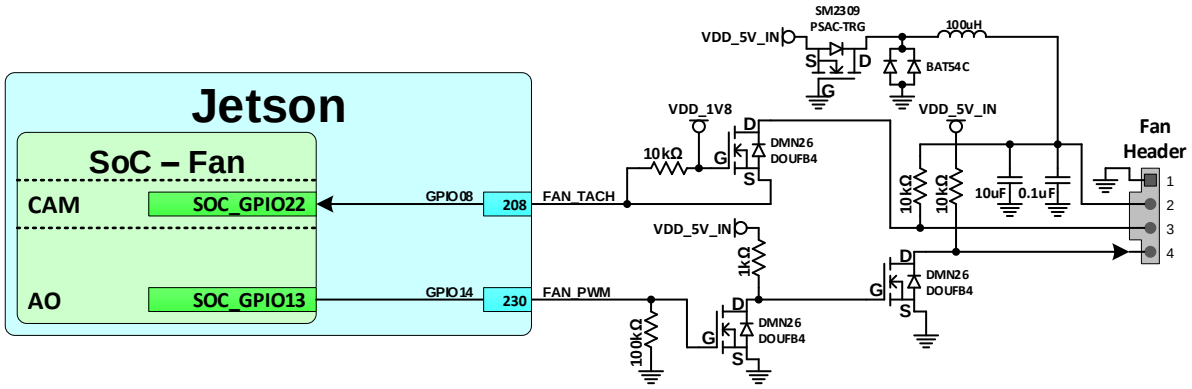
Table 9-12. Jetson Xavier NX Fan Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
230	GPIO14	SOC_GPIO13	Fan PWM	Fan	Output (note)	CMOS – 1.8V	ST	z
208	GPIO08	SOC_GPIO22	Fan tachometer	Fan	Input (note)	CMOS – 1.8V	ST	pd

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.
4. The direction indicated for GPIO014 and GPIO08 is associated with their use as Fan PWM/Tach.

Figure 9-7. Jetson Xavier NX Fan Connections



9.6 Debug

Jetson Xavier NX supports UART for debugging purposes. The UART intended for debug is UART2 with is routed to a level shifter then to a 6-pin UART header on the Developer Kit Carrier Board.

Table 9-13. Jetson Xavier NX Debug UART Pin Descriptions

Pin #	Module Pin Name (see note 4)	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
238	UART2_RXD	UART3_TX	UART 2 receive	Serial port	Input	CMOS – 1.8V	DD	pd
236	UART2_TXD	UART3_RX	UART 2 transmit		Output		DD	pd

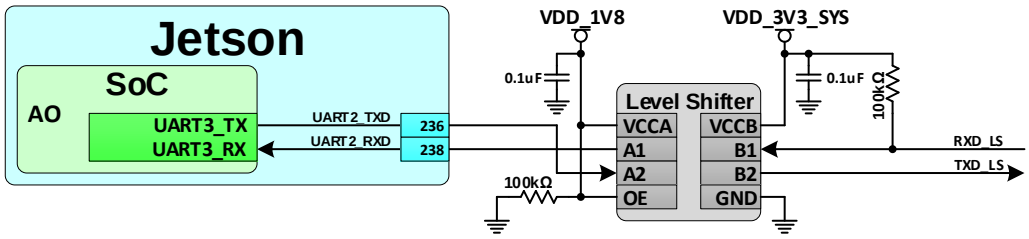
Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 9-14. Debug UART Connections

Module Pin Name	Type	Termination	Description
UART2_TXD	O		UART #2 Transmit: Connect to RX pin of serial device
UART2_RXD	I	If level shifter implemented, 100kΩ to supply on the non-Jetson Xavier NX side of the device.	UART #2 Receive: Connect to TX pin of serial device

Figure 9-8. Debug UART Connections



Note: If level shifter is implemented, pull-up is required on the RXD line on the non-Jetson Xavier NX side of the level shifter. This is required to keep the input from floating and toggling when no device is connected to the debug UART.

Chapter 10. PADS

Jetson Xavier NX signals that come from the SoC may glitch when the associated power rail is enabled. This may affect pins that are used as GPIO outputs. Designers should take this into account. GPIO outputs that must maintain a low state even while the power rail is being ramped up may require special handling.

10.1 Internal Pull-ups for Dual Voltage Block Pins Power at 1.8V

Several of the MPIO pads are on blocks designed to be powered at either 1.8V or 3.3V. These blocks are powered at 1.8V on Jetson Xavier NX, and the internal pull-up at initial Power-ON is not effective. The signal may only be pulled up a fraction of the 1.8V rail. Once the system boots, software can configure the pins for 1.8V operation and the internal pull-ups will work correctly. If these signals need the pull-ups during Power-ON, external pull-up resistors should be added. The following pins listed are the affected pins. These are the Jetson Xavier NX pins on the dual voltage blocks powered at 1.8V with Power-ON reset default of Internal pull-up enabled.

- SDMMC_DAT0
- SDMMC_DAT1
- SDMMC_DAT2
- SDMMC_DAT3
- SDMMC_CMD
- SPI1_CS0*
- SPI1_CS1*

10.2 Schmitt Trigger Usage

The MPIO pins have an option to enable or disable Schmitt-trigger mode on a per-pin basis. This mode is recommended for pins used for edge-sensitive functions such as input clocks, or other functions where each edge detected will affect the operation of a device. Schmitt-trigger mode provides better noise immunity and can help avoid extra edges from being “seen” by the Xavier inputs. Input clocks include the I2S and SPI clocks (**I2Sx_SCLK** and **SPIx_SCK**) when Xavier

is in slave mode. The FAN_TACH pin [GPIO8] is another input that could be affected by noise on the signal edges. The SDMMC_CLK pin, while used to output the clock, also sample the clock at the input to help with read timing. Therefore, the SDMMC_CLK pin may benefit from enabling Schmitt-trigger mode. Care should be taken if the Schmitt-trigger mode setting is changed from the default initialization mode as this can influence interface timing.

10.3 Pins Pulled or Driven High During Power-ON

The Jetson Xavier NX is powered up before the carrier board (See Section 3.1 for power sequencing). Table 10-1 lists the pins on Jetson Xavier NX that default to being pulled or driven high. Care must be taken on the carrier board design to ensure that any of these pins that connect to devices on the carrier board (or devices connected to the carrier board) do not cause damage or excessive leakage to those devices. Some of the ways to avoid issues with sensitive devices are:

- External pull-downs on the carrier board that are strong enough to keep the signals low are one solution, given that this does not affect the function of the pin.
- Buffers or level shifters can be used to separate the signals from devices that may be affected. The buffer/shifter should be disabled until the device power is enabled.

Table 10-1. Pins Pulled or Driven High by Xavier Prior to SYS_REST* Inactive

Jetson Xavier NX Pin	Power-ON reset Default	Pull-up Strength (kΩ)		Jetson Xavier NX Pin	Power-ON reset Default	Pull-up Strength (kΩ)
SYS_RESET*	Driven high	na		SPI0_CS0*	Internal pull-up	~15
SLEEP/WAKE*	Internal pull-up	~100		SPI0_CS1*	Internal pull-up	~15
FORCE_RECOVERY*	Internal pull-up	~100		SPI1_CS0*	Internal pull-up	~18
UART1_RXD	Internal pull-up	~100		SPI1_CS1*	Internal pull-up	~18

Table 10-2. Pins with External Pull-ups to Supply on before SYS_RESET_IN* Inactive

Jetson Xavier NX Pin	Pull-up Supply Voltage (V)	External Pull-up (kΩ)		Jetson Xavier NX Pin	Pull-up Supply Voltage (V)	External Pull-up (kΩ)
I2C0_SCL/SDA	3.3	2.2		SPI1_CS0*	1.8	100
I2C1_SCL/SDA	3.3	2.2		SPI1_CS1*	1.8	100
I2C2_SCL/SDA	1.8	2.2		PCIE[1:0]_CLKREQ*	3.3	47
CAM_I2C_SCL/SDA	3.3	2.2		PCIE[1:0]_RST*	3.3	4.7
				PCIE_WAKEN	3.3	100

Chapter 11. Unused Interface Terminations

11.1 Unused Multi-purpose Standard CMOS Pad Interfaces

The following Jetson Xavier NX pins (and groups of pins) are Xavier MPIO pins that support either special function IOs (SFIO) and/or GPIO capabilities. Any unused pins or portions of pin groups listed in Table 11-1 that are not used can be left unconnected.

Table 11-1. Unused MPIO Pins and Pin Group

Jetson Xavier NX Pins / Pin Groups		Jetson Xavier NX Pins / Pin Groups
FORCE_RECOVERY*		SDMMC
GPIO00		I2S
PCIE[1:0]_CLK/RST/CLKREQ/WAKE		UART
GPIO xx		I2C
DP0_HPD, DP1_HPD, HDMI_CEC		SPI
CAM Control, Clock		

11.2 Unused Dedicated Special Purpose Pad Interfaces

See the Unused SFIO (Special Function I/O) interface pins section in the design checklist (Table 12-1).

Chapter 12. Design Checklist

The following checklist is intended to help ensure that the correct connections have been made in a design. The check items describe connections for the various interfaces and the "Same/Diff/NA" column is intended to be used to indicate whether the design matches the check item description, is different, or is not applicable to the design.

Table 12-1. Checklist

Check Item Description			Same/Diff/NA
Carrier Board Signal Terminations (To be implemented on the carrier board for interfaces that are used)			
	Parallel Termination	Series Termination	
USB/PCIe			
USBSS_TX_N/P (USB 3.1)	–	0.1uF capacitors	
USBSS_RX_N/P (USB 3.1)	–	0.1uF capacitors if directly connected to device	
PCIE0_TX[3:0]_N/P	–	0.1uF capacitors	
PCIE0_RX[3:0]_N/P	–	0.1uF capacitors if directly connected to device	
Ethernet			
GBE_MDI0_N/P	–	Magnetics near or in RJ45 connector	
GBE_MDI1_N/P	–	Magnetics near or in RJ45 connector	
GBE_MDI2_N/P	–	Magnetics near or in RJ45 connector	
GBE_MDI3_N/P	–	Magnetics near or in RJ45 connector	
GBE_ACT	0.1uF capacitor to **GND**	series resistor – value depends on LED used. Max current limit must be met.	
GBE_LINK	0.1uF capacitor to **GND**		
DP[1:0] for eDP/DP			
DPx_TXD3_N/P	ESD to **GND**	0.1uF capacitors	
DPx_TXD2_N/P	ESD to **GND**	0.1uF capacitors	
DPx_TXD1_N/P	ESD to **GND**	0.1uF capacitors	
DPx_TXD0_N/P	ESD to **GND**	0.1uF capacitors	
DPx_AUX_P	100kΩ pull-down to GND near connector and ESD to **GND**	0.1uF capacitor	
DPx_AUX_N	100kΩ pull-up to 3.3V near connector and ESD to **GND**	0.1uF capacitor	
DPx_HPD	10kΩ pull-up to 1.8V near module and 100kΩ pull-down to **GND** on DP side of level shifter. ESD to **GND**	Level Shifter (w/output toward module) and 100kΩ resistor to DP connector. Level shifter must be non-inverting.	
DP[1:0] for HDMI			
DPx_TXD3_N/P	499Ω, 1% resistor to 600Ω bead to **GND.** ESD to **GND** just before series resistors.	0.1uF capacitors then series resistors (see Section 5.2 about value)	
DPx_TX[2:0]_N/P	499Ω, 1% resistor to 600Ω bead to **GND**	0.1uF capacitors then series resistors (see Section 5.2 about value)	

DPx_AUX_N/P		10kΩ pull-up to 3.3V near module and 1.8kΩ pull-up to 5V near HDMI conn.		Bidirectional level shifter between Pull-ups in Parallel Termination column		
DPx_HPD		10kΩ pull-up to 1.8V near module and 100kΩ pull-down to **GND** near HDMI conn. ESD to **GND**.		Level shifter (w/output toward module) between Pull-up and Pull-down in Parallel Termination column. Level shifter can be inverting or non-inverting. 100kΩ series resistor between pull-down and HDMI connector.		
Power						
Module Power Supplies						
Supply (Carrier Board)	Usage	(V)	Supply Type	Source	Enable	
VDD_IN	Main Supply from Adapter	5V	Adapter	na	na	
PMIC_BBAT	Real-time clock supply	1.65-5.5	PMIC is supply when charging cap or coin-cell	Super-cap or coin-cell is source when system power removed	na	
Carrier Board Supplies						
Main 3.3V Supply	Main 3.3V supply	3.3		Main Input	**SYS_RESET***	
Main 1.8V Supply	Main 1.8V supply	1.8		Main Input	**SYS_RESET***	
Power Control						
SYS_RESET* is used as enable for carrier board supplies (can also be driven low to force module reset)						
SHUTDOWN_REQ* - when active, causes the carrier board to power off						
MOD_SLEEP* is connected to supplies/devices to be disabled during module deep sleep (LP0)						
SLEEP/WAKE* is optional signal to wake system from sleep mode.						
USB/PCIe Connections						
USB 2.0						
USB0_D_N/P available to be used as device for USB recovery at a minimum						
VBUS from connector connects to load switch (if host supported) and through level shifter to **GPIO00 (USB0_VBUS_EN0)** on the module.						
USB[2:0]_D_N/P connected to **D-/D+** pins on USB 2.0 connector/device.						
Any EMI/ESD devices used are suitable for USB High-speed						
USB 3.1						
USBSS_RX_N/P connected to **RX-/+** pins on USB 3.1 connector. (See Signal Terminations section)						
USBSS_TX_N/P connected to **TX-/+** pins on USB 3.1 conn., device, hub, etc. (See Signal Terminations section)						
AC caps are provided for device **TX** pins (those connected to the module **RX_N/P**) if device is on the carrier board (See Signal Terminations section)						
If external ESD protection needed, Texas Instruments TPD4E05U06 device is recommended						
PCIe						
PCIe Controller #0 (supports up to x4)						
PCIE0_TX0/RX0 used for 3.3V single-lane device/connector						
PCIE0_TX[1:0]/RX[1:0] used for 3.3V 2-lane device/connector						
PCIE0_TX[3:0]/RX[3:0] used for 3.3V 4-lane device/connector						
Reference clock used for PCIe is **PCIE0_CLK1_N/P**						
Clock Request and Reset for PCIe **PCIE0_CLKREQ* and PCIE0_RST***. Pull-ups are provided on the module						
PCIe Controller #1 (supports up to x1)						
PCIE1_TX0/RX0 used for 3.3V single-lane device/connector						
Reference clock used for PCIe is **PCIE1_CLK_N/P**						
Clock Request and Reset for PCIe **PCIE1_CLKREQ* and PCIE1_RST***. Pull-ups are provided on the module						
Common PCIe Connections						
TX_N/P connected to corresponding pins on connector, or **RX_N/P** on device on the carrier board (See Signal Terminations section)						
RX_N/P connected to corresponding pins on connector, or **TX_N/P** on device on the carrier board (See Signal Terminations section)						
AC caps are provided for device **TX_N/P** pins (those connected to the module **RX_N/P**) if device is on the carrier board (See Signal Terminations section)						
PCIE_WAKE* connected to **WAKE** pins on devices/connectors. Pull-up is provided on the module.						

Ethernet	
GBE_MDI[3:0]_N/P connected to equivalent pins on magnetics device (See Signal Terminations)	
GBE_LED_LINK connected to Link LED (green) pins on connector (See Signal Terminations)	
GBE_LED_ACT connected to Activity LED (yellow) pins on connector (See Signal Terminations)	
SDMMC Connections	
SDMMC_CLK connected to **CLK** pin of device/socket	
SDMMC_CMD connected to **CMD** pin of device/socket. (See Signal Terminations)	
SDMMC_D[3:0] connected to **DATA[3:0]** pins of device/socket. (See Signal Terminations)	
GPIO08 connected to SD Card card-detect pin if implemented.	
Any EMI/ESD devices used are suitable for highest frequencies supported (low capacitive load: <1pf recommended).	
Display Connections	
DP[1:0] for eDP / DP	
DPx_TXD[3:0]_N/P connected to **D[3:0]-/+** pins on eDP/DP connector (See DP/HDMI Pin Mapping table and Signal Terminations)	
DPx_AUX_N/P connected to Aux Lane of panel/connector (See Signal Terminations)	
DPx_HPD connected to **HPD** pin of panel/connector (See Signal Terminations)	
Any EMI/ESD devices used are suitable for highest frequencies supported (Texas Instruments TPD4E05U06 recommended)	
DP[1:0] for HDMI	
DPx_TXD3_N/P connected to **C-/C+** pins on HDMI connector (See Signal Terminations)	
DPx_TXD[2:0]_N/P connected to **D[0:2]_-/+** pins (See DP/HDMI Pin Mapping table) (See Signal Terminations)	
DPx_HPD connected to **HPD** pin on HDMI connector (See Signal Terminations)	
HDMI_CEC connected to **CEC** on HDMI connector through gating circuitry (see HDMI connection figure for details).	
DPx_AUX_P connected to **SCL** and **DP1_AUX_N** to **SDA** on HDMI connector (See Signal Terminations)	
HDMI 5V Supply connected to **+5V** on HDMI connector.	
See Common High-Speed Interface Requirements section for common-mode choke requirements if this is needed (not recommended unless EMI issues seen)	
See HDMI section for ESD requirements. Texas Instruments TPD4E02B04 recommended	
Video Input	
Camera (CSI)	
CSI[4:0]_CLK_N/P, DSI_CLK_N/P (CSI5_CLK) connected to clock pins of camera. See Table 6-3 for details	
DSI_D[1:0]_N/P (CSI5_D[1:0]), CSI[3:0]_D[1:0]_N/P & CSI4_D[3:0]_N/P connected to data pins of camera. See Table 6-3 for details	
Any EMI/ESD devices used are suitable for highest frequencies supported (low capacitive load: <1pf recommended)	
Control	
CAM_I2C_SCL/SDA connected to I2C **SCL** and **SDA** pins of imager (See Signal Terminations).	
CAM[1:0]_MCLK connected to Camera reference clock inputs.	
CAM[1:0]_PWDN connected to power-down pins on camera(s) or used as GPIO for other purposes.	
Audio	
Codec/I2S/MCLK	
Either **I2S0** or **I2S1** are used for audio codec if present in design	
Either **I2S0** or **I2S1** are used for Bluetooth if present in design	
I2Sx_SCLK Connect to I2S/PCM **CLK** pin of audio device.	
I2Sx_FS Connect to left/right clock pin of audio device.	
I2Sx_DOUT Connect to data input pin of audio device.	
I2Sx_DIN Connect to data output pin of audio device.	
GPIO09 Connect to clock pin of audio codec.	
Available GPIO connected to interrupt pin of audio codec (wake capable GPIO used if this is required).	
I2C/SPI/UART	
I2C	
I2C devices on same I2C interface do not have address conflicts (comparisons are done 7-bit to 7-bit format or 8-bit to 8-bit format)	
I2C0_SCL/SDA, I2C1_SCL/SDA and CAM_I2C_SCL/SDA are used for 3.3V devices (or level shifters employed) and do not have pull-ups on the carrier board since the devices are pulled to 3.3V on the module with 2.2kΩ resistors.	
I2C2_SCL/SDA is used for 1.8V devices (or level shifters employed) and does not have pull-ups on the carrier board since the devices are pulled to 1.8V on the module with 2.2kΩ resistors.	

Pull-up resistors are provided on the non-module side of any level shifters.	
Pull-up resistor values after any level shifters are based on frequency/load (check I2C Spec)	
I2C[2:0]_SCL/SDA and CAM_I2C_SCL/SDA pins connect to SCL/SDA pins of devices	
SPI	
SPI[1:0]_CLK connected to peripheral **CLK** pin(s)	
SPI[1:0]_MOSI connected to slave peripheral **MOSI** pin(s)	
SPI[1:0]_MISO connected to slave peripheral **MISO** pin(s)	
SPI[1:0]_CS[1:0]* connected one **CS** pin per SPI IF to each slave peripheral **CS** pin on the interface	
UART	
UARTx_TX connects to peripheral **RX** pin of device	
UARTx_RX connects to peripheral **TX** pin of device	
UARTx_CTS* connects to peripheral **RTS#** pin of device	
UARTx_RTS* connects to peripheral **CTS#** pin of device	
CAN	
CAN_DOUT connected to input data (RX) pins of respective CAN device	
CAN_DIN connected to output data (TX) pin of respective CAN device	
Strapping	
FORCE_RECOVERY*: To enter Forced Recovery mode, pin is connected to **GND** when system is powered on.	

Unused Dedicated Special Function Interface Pins		
Ball Name	Termination	
USB 2.0		
USB[2:1]_D_N/P	Leave NC any unused pins	
USB 3.1 / PCIe		
PCIE[1:0]_TXx_N/P, USBSS_TX_N/P	Leave NC any unused TX lines	
PCIE[1:0]_RXx_N/P, USBSS_RX_N/P	Leave NC any unused RX lanes	
PCIE[1:0]_CLKx_N/P	Leave NC if not used	
Ethernet		
GBE_MDIx	Leave NC if not used	
GBE_LED_LINK, GBE_LED_ACT	Leave NC any not used	
CSI (& CSI pins on DSI pins)		
CSIx_CLK_N/P, DSI_CLK_N/P	Leave NC any unused CSI clock lanes	
CSIx_Dx_N/P, DSI_Dx_N/P	Leave NC any unused CSI data lanes	
eDP/DP/HDMI		
DPx_TXDx_N/P	Leave NC any unused lanes	
DPx_AUX_N/P	Leave NC if not used	
DPx_HPD	Leave NC if not used	
HDMI_CEC	Leave NC if not used	

Chapter 13. Jetson Xavier NX Pin Descriptions

The following tables gives the pin description for the Jetson Xavier NX connector (260-pin S)-DIMM).

Table 13-1. Jetson Xavier NX Connector Pin Descriptions – Odd Side

Pin #	Module Signal Name	SoC Pin Name	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
1	GND	–	GND	GND	–	GND	–	–
3	CSI1_D0_N	CSI_B_D0_N	Camera, CSI 1 Data 0	2-lane Camera #2, 4-lane Camera #1	Input	MIPI D-PHY	–	z
5	CSI1_D0_P	CSI_B_D0_P					–	z
7	GND	–	GND	GND	–	GND	–	–
9	CSI1_CLK_N	CSI_B_CLK_N	Camera, CSI 1 Clock	2-lane Camera #2, 4-lane Camera #1	Input	MIPI D-PHY	–	z
11	CSI1_CLK_P	CSI_B_CLK_P					–	z
13	GND	–	GND	GND	–	GND	–	–
15	CSI1_D1_N	CSI_B_D1_N	Camera, CSI 1 Data 1	2-lane Camera #2, 4-lane Camera #1	Input	MIPI D-PHY	–	z
17	CSI1_D1_P	CSI_B_D1_P					–	z
19	GND	–	GND	GND	–	GND	–	–
21	CSI3_D0_N	CSI_D_D0_N	Camera, CSI 3 Data 0	2-lane Camera #4, 4-lane Camera #2	Input	MIPI D-PHY	–	z
23	CSI3_D0_P	CSI_D_D0_P					–	z
25	GND	–	GND	GND	–	GND	–	–
27	CSI3_CLK_N	CSI_D_CLK_N	Camera, CSI 3 Clock	2-lane Camera #4, 4-lane Camera #2	Input	MIPI D-PHY	–	z
29	CSI3_CLK_P	CSI_D_CLK_P					–	z
31	GND	–	GND	GND	–	GND	–	–
33	CSI3_D1_N	CSI_D_D1_N	Camera, CSI 3 Data 1	2-lane Camera #4, 4-lane Camera #2	Input	MIPI D-PHY	–	z
35	CSI3_D1_P	CSI_D_D1_P					–	z
37	GND	–	GND	GND	–	GND	–	–
39	DP0_TXD0_N	HDMI_DP0_TXDN0	DisplayPort 0 Lane 0 or HDMI Lane 2	HDMI/DP Connector #0	Output	AC-Coupled on carrier board	–	z
41	DP0_TXD0_P	HDMI_DP0_TXDP0					–	z
43	GND	–	GND	GND	–	GND	–	–
45	DP0_TXD1_N	HDMI_DP0_TXDN1	DisplayPort 0 or HDMI Lane 1	HDMI/DP Connector #0	Output	AC-Coupled on carrier board	–	z
47	DP0_TXD1_P	HDMI_DP0_TXDP1					–	z
49	GND	–	GND	GND	–	GND	–	–
51	DP0_TXD2_N	HDMI_DP0_TXDN2	DisplayPort 0 Lane 2 or HDMI Lane 0	HDMI/DP Connector #0	Output	AC-Coupled on carrier board	–	z
53	DP0_TXD2_P	HDMI_DP0_TXDP2					–	z
55	GND	–	GND	GND	–	GND	–	–
57	DP0_TXD3_N	HDMI_DP0_TXDN3	DisplayPort 0 Lane 3 or HDMI Clk Lane	HDMI/DP Connector #0	Output	AC-Coupled on carrier board	–	z
59	DP0_TXD3_P	HDMI_DP0_TXDP3					–	z
61	GND	–	GND	GND	–	GND	–	–
63	DP1_TXD0_N	HDMI_DP1_TXDN0	DisplayPort 1 Lane 0 or HDMI Lane 2	HDMI/DP Connector #1	Output	AC-Coupled on carrier board	–	z
65	DP1_TXD0_P	HDMI_DP1_TXDP0					–	z
67	GND	–	GND	GND	–	GND	–	–
69	DP1_TXD1_N	HDMI_DP1_TXDN1	DisplayPort 1 or HDMI Lane 1	HDMI/DP Connector #1	Output	AC-Coupled on carrier board	–	z
71	DP1_TXD1_P	HDMI_DP1_TXDP1					–	z
73	GND	–	GND	GND	–	GND	–	–

Pin #	Module Signal Name	SoC Pin Name	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
75	DP1_TXD2_N	HDMI_DP1_TXDN2	DisplayPort 1 Lane 2 or HDMI Lane 0	HDMI/DP Connector #1	Output	AC-Coupled on carrier board	–	z
77	DP1_TXD2_P	HDMI_DP1_TXDP2					–	z
79	GND	–	GND	GND	–	GND	–	–
81	DP1_TXD3_N	HDMI_DP1_TXDN3	DisplayPort 1 Lane 3 or HDMI Clk Lane	HDMI/DP Connector #1	Output	AC-Coupled on carrier board	–	z
83	DP1_TXD3_P	HDMI_DP1_TXDP3					–	z
85	GND	–	GND	GND	–	GND	–	–
87	GPIO00	USB_VBUS_EN0	GPIO #0 or USB 0 VBUS Enable #0	GPIO or USB Load Switch Enable	Bidir	CMOS – 1.8V	DD	0
89	SPI0_MOSI	SPI1_MOSI	SPI 0 Master Out / Slave In	SPI #0 Device #0 or 1	Bidir	CMOS – 1.8V	ST	pu
91	SPI0_SCK	SPI1_SCK	SPI 0 Clock				ST	pd
93	SPI0_MISO	SPI1_MISO	SPI 0 Master In / Slave Out				ST	pu
95	SPI0_CS0*	SPI1_CS0	SPI 0 Chip Select 0				ST	pu
97	SPI0_CS1*	SPI1_CS1	SPI 0 Chip Select 1				ST	pu
99	UART0_TXD	UART2_TX	UART #0 Transmit	UART general (i.e. M.2 Key E)	Output	CMOS – 1.8V	DD	pd
101	UART0_RXD	UART2_RX	UART #0 Receive		Input		DD	pd
103	UART0_RTS*	UART2_RTS	UART #0 Request to Send		Output		ST	pd
105	UART0_CTS*	UART2_CTS	UART #0 Clear to Send		Input		ST	pu
107	GND	–	GND	GND	–	GND	–	–
109	USB0_D_N	USB0_DN	USB 2.0 Port 0 Data	USB connector/device/hub (i.e. Micro B)	Bidir	USB PHY	–	0
111	USB0_D_P	USB0_DP					–	0
113	GND	–	GND	GND	–	GND	–	–
115	USB1_D_N	USB1_DN	USB 2.0 Port 1 Data	USB connector/device/hub (i.e. USB 3.1 Hub)	Bidir	USB PHY	–	0
117	USB1_D_P	USB1_DP					–	0
119	GND	–	GND	GND	–	GND	–	–
121	USB2_D_N	USB2_DN	USB 2.0, Port 2 Data	USB connector/device/hub (i.e. M.2 Key E)	Bidir	USB PHY	–	0
123	USB2_D_P	USB2_DP					–	0
125	GND	–	GND	GND	–	GND	–	–
127	GPIO04	SPI2_MISO	GPIO #4	GPIO	Bidir	CMOS – 1.8V	DD	pd
129	GND	–	GND	GND	–	GND	–	–
131	PCIE0_RX0_N	NVHS0_RX0_N	PCIe 0 Receive 0 (PCIe Ctrl #5 Lane 0)	PCIe x4 conn/device (i.e. M.2 Key M)	Input	PCIe PHY, AC-Coupled for PCIe on carrier board if direct connect.	–	z
133	PCIE0_RX0_P	NVHS0_RX0_P					–	z
135	GND	–	GND	GND	–	GND	–	–
137	PCIE0_RX1_N	NVHS0_RX1_N	PCIe 0 Receive 1 (PCIe Ctrl #5 Lane 1)	PCIe x4 conn/device (i.e. M.2 Key M)	Input	PCIe PHY, AC-Coupled for PCIe on carrier board if direct connect.	–	z
139	PCIE0_RX1_P	NVHS0_RX1_P					–	z
141	GND	–	GND	GND	–	GND	–	–
143	CAN_RX	CAN0_DIN	CAN Receive	CAN PHY	Input	CMOS – 3.3V	CZ	pu
145	CAN_TX	CAN0_DOUT	CAN Transmit		Output		CZ	pu
147	GND	–	GND	GND	–	GND	–	–
149	PCIE0_RX2_N	NVHS0_RX2_N	PCIe 0 Receive 2 (PCIe Ctrl #5 Lane 2)	PCIe x4 conn/device (i.e. M.2 Key M)	Input	PCIe PHY, AC-Coupled for PCIe on carrier board if direct connect.	–	z
151	PCIE0_RX2_P	NVHS0_RX2_P					–	z
153	GND	–	GND	GND	–	GND	–	–
155	PCIE0_RX3_N	NVHS0_RX3_N	PCIe 0 Receive 3 (PCIe Ctrl #5 Lane 3)	PCIe x4 conn/device (i.e. M.2 Key M)	Input	PCIe PHY, AC-Coupled for PCIe on carrier board if direct connect.	–	z
157	PCIE0_RX3_P	NVHS0_RX3_P					–	z
159	GND	–	GND	GND	–	GND	–	–
161	USBSS_RX_N	PEX_RX1_N	USB SS Receive (USB 3.0 Ctrl #2)	USB 3.0 Connector/Device/Hub	Input	USB SS PHY, AC-Coupled (off the module)	–	z
163	USBSS_RX_P	PEX_RX1_P					–	z
165	GND	–	GND	GND	–	GND	–	–
167	PCIE1_RX0_N	PEX_RX11_N	PCIe 1 Receive 0 (PCIe Ctrl #4 Lane 0)	PCIe x1 conn/device (i.e. M.2 Key E)	Input	PCIe PHY, AC-Coupled on carrier board if direct connect.	–	z
169	PCIE1_RX0_P	PEX_RX11_P					–	z
171	GND	–	GND	GND	–	GND	–	–
173	PCIE1_CLK_N	PEX_CLK4N	PCIe 1 Reference Clock (PCIe Ctrl #4)	PCIe x1 conn/device (i.e. M.2 Key E)	Output	PCIe PHY	–	0
175	PCIE1_CLK_P	PEX_CLK4P					–	0

Pin #	Module Signal Name	SoC Pin Name	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
177	GND	–	GND	GND	–	GND	–	–
179	PCIE_WAKE*	PEX_WAKE_N	PCIe Wake. 100kΩ pull-up to 3.3V on the module.	PCIe (Shared)	Input	Open Drain 3.3V, Pull-up on the module	DD	z
181	PCIE0_RST*	PEX_L5_RST_N	PCIe 0 Reset (PCIe Ctrl #5). 4.7kΩ pull-up to 3.3V on the module. Output when Jetson Xavier NX is Root Port or input when Jetson Xavier NX is Endpoint.	PCIe x4 conn/device (i.e. M.2 Key M)	Bidir	Open Drain 3.3V, Pull-up on the module	DD	0
183	PCIE1_RST*	PEX_L4_RST_N	PCIe 1 Reset (PCIe Ctrl #4). 4.7kΩ pull-up to 3.3V on the module.	PCIe x1 conn/device (i.e. M.2 Key E)	Output		DD	0
185	I2C0_SCL	GEN2_I2C_SCL	General I2C 0 Clock. 2.2kΩ pull-up to 3.3V on module.	I2C (General)	Bidir	Open Drain – 3.3V	DD	z
187	I2C0_SDA	GEN2_I2C_SDA	General I2C 0 Data. 2.2kΩ pull-up to 3.3V on the module.				DD	z
189	I2C1_SCL	DP_AUX_CH3_P	General I2C 1 Clock. 2.2kΩ pull-up to 3.3V on the module.				DP_AUX	z
191	I2C1_SDA	DP_AUX_CH3_N	General I2C 1 Data. 2.2kΩ pull-up to 3.3V on the module.				DP_AUX	z
193	I2S0_DOUT	DAP5_DOUT	I2S Audio Port 0 Data Out	Audio Device	Output	CMOS – 1.8V	ST	pd
195	I2S0_DIN	DAP5_DIN	I2S Audio Port 0 Data In		Input		ST	pd
197	I2S0_FS	DAP5_FS	I2S Audio Port 0 Left/Right Clock		Bidir		ST	pd
199	I2S0_SCLK	DAP5_SCLK	I2S Audio Port 0 Clock		Bidir		ST	pd
201	GND	–	GND	GND	–	GND	–	–
203	UART1_TXD	UART1_TX	UART #1 Transmit	UART general	Output	CMOS – 1.8V	DD	pd
205	UART1_RXD	UART1_RX	UART #1 Receive		Input		DD	z
207	UART1_RTS*	UART1_RTS	UART #1 Request to Send		Output		ST	pd
209	UART1_CTS*	UART1_CTS	UART #1 Clear to Send		Input		ST	pu
211	GPIO09	AUD_MCLK	GPIO #9 or Audio Codec Master Clock	GPIO or Audio MCLK	Bidir	CMOS – 1.8V	ST	pd
213	CAM_I2C_SCL	CAM_I2C_SCL	Camera I2C Clock. 2.2kΩ pull-up to 3.3V on the module.	Cameras (shared)	Bidir	Open Drain – 3.3V	DD	z
215	CAM_I2C_SDA	CAM_I2C_SDA	Camera I2C Data. 2.2kΩ pull-up to 3.3V on the module.				DD	z
217	GND	–	GND	GND	–	GND	–	–
219	SDMMC_DAT0	SDMMC3_DAT0	SD Card or SDIO Data 0	SD Card or SDIO Device	Bidir	CMOS – 1.8V	CZ	pd
221	SDMMC_DAT1	SDMMC3_DAT1	SD Card or SDIO Data 1			CMOS – 1.8V	CZ	pd
223	SDMMC_DAT2	SDMMC3_DAT2	SD Card or SDIO Data 2			CMOS – 1.8V	CZ	pd
225	SDMMC_DAT3	SDMMC3_DAT3	SD Card or SDIO Data 3			CMOS – 1.8V	CZ	pd
227	SDMMC_CMD	SDMMC3_CMD	SD Card or SDIO Command			CMOS – 1.8V	CZ	pd
229	SDMMC_CLK	SDMMC3_CLK	SD Card or SDIO Clock		Output	CMOS – 1.8V	CZ	pd
231	GND	–	GND	GND	–	GND	–	–
233	SHUTDOWN_REQ*	–	Used by the module to request a shutdown from the carrier board. 100kΩ pull-up to VDD_IN (5V) on the module.	System	Input	CMOS – 5.0V	–	–
235	PMIC_BBAT	(PMIC BBATT)	PMIC Battery Back-up. Optionally used to provide back-up power for the Real-Time-Clock (RTC). See Power section for details.	Battery Back-up using Super-capacitor	Bidir	1.65V-5.5V	–	–
237	POWER_EN	(PMIC EN0 through converter logic)	Signal for module on/off: high level on, low level off. Connects to module PMIC EN0 through converter logic. 100kΩ puldown on the module.	System	Input	Input	–	–
239	SYS_RESET*	SYS_RESET_IN_N	Module Reset. Reset to the module when driven low by the carrier board. See Power section for details.	System	Bidir	Open Drain, 1.8V	JT_RST	z
241	GND	–	GND	GND	–	GND	–	–
243	GND						–	–
245	GND						–	–
247	GND						–	–
249	GND						–	–

Pin #	Module Signal Name	SoC Pin Name	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
251	VDD_IN	–	Main power – Supplies PMIC and other regs	Main DC input	Input	5.0V	–	–
253	VDD_IN						–	–
255	VDD_IN						–	–
257	VDD_IN						–	–
259	VDD_IN						–	–

Notes:

1. Green highlighting for Ground pins and Red for Power.
2. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
3. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
4. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Legend Ground | Power

Table 13-2. Jetson Xavier NX Connector Pin Descriptions – Even Side

Pin #	Module Signal Name	Xavier Pin Name	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
2	GND	–	GND	GND	–	GND	–	–
4	CSI0_D0_N	CSI_A_D0_N	Camera, CSI 0 Data 0	2-lane Camera #1, 4-lane Camera #1	Input	MIPI D-PHY	–	z
6	CSI0_D0_P	CSI_A_D0_P					–	z
8	GND	–	GND	GND	–	GND	–	–
10	CSI0_CLK_N	CSI_A_CLK_N	Camera, CSI 0 Clock	2-lane Camera #1, 4-lane Camera #1	Input	MIPI D-PHY	–	z
12	CSI0_CLK_P	CSI_A_CLK_P					–	z
14	GND	–	GND	GND	–	GND	–	–
16	CSI0_D1_N	CSI_A_D1_N	Camera, CSI 0 Data 1	2-lane Camera #1, 4-lane Camera #1	Input	MIPI D-PHY	–	z
18	CSI0_D1_P	CSI_A_D1_P					–	z
20	GND	–	GND	GND	–	GND	–	–
22	CSI2_D0_N	CSI_C_D0_N	Camera, CSI 2 Data 0	2-lane Camera #3, 4-lane Camera #2	Input	MIPI D-PHY	–	z
24	CSI2_D0_P	CSI_C_D0_P					–	z
26	GND	–	GND	GND	–	GND	–	–
28	CSI2_CLK_N	CSI_C_CLK_N	Camera, CSI 2 Clock	2-lane Camera #3, 4-lane Camera #2	Input	MIPI D-PHY	–	z
30	CSI2_CLK_P	CSI_C_CLK_P					–	z
32	GND	–	GND	GND	–	GND	–	–
34	CSI2_D1_N	CSI_C_D1_N	Camera, CSI 2 Data 1	2-lane Camera #3, 4-lane Camera #2	Input	MIPI D-PHY	–	z
36	CSI2_D1_P	CSI_C_D1_P					–	z
38	GND	–	GND	GND	–	GND	–	–
40	CSI4_D2_N	CSI_F_D0_N	Camera, CSI 4 Data 2	4-lane Camera #3	Input	MIPI D-PHY	–	z
42	CSI4_D2_P	CSI_F_D0_P					–	z
44	GND	–	GND	GND	–	GND	–	–
46	CSI4_D0_N	CSI_E_D0_N	Camera, CSI 4 Data 0	2-lane Camera #5, 4-lane Camera #3	Input	MIPI D-PHY	–	z
48	CSI4_D0_P	CSI_E_D0_P					–	z
50	GND	–	GND	GND	–	GND	–	–
52	CSI4_CLK_N	CSI_E_CLK_N	Camera, CSI 4 Clock	2-lane Camera #5, 4-lane Camera #3	Input	MIPI D-PHY	–	z
54	CSI4_CLK_P	CSI_E_CLK_P					–	z
56	GND	–	GND	GND	–	GND	–	–
58	CSI4_D1_N	CSI_E_D1_N	Camera, CSI 4 Data 1	2-lane Camera #5, 4-lane Camera #3	Input	MIPI D-PHY	–	z
60	CSI4_D1_P	CSI_E_D1_P					–	z
62	GND	–	GND	GND	–	GND	–	–
64	CSI4_D3_N	CSI_F_D1_N	Camera, CSI 4 Data 3	4-lane Camera #3	Input	MIPI D-PHY	–	z
66	CSI4_D3_P	CSI_F_D1_P					–	z
68	GND	–	GND	GND	–	GND	–	–
70	DSI_D0_N	CSI_G_D0_N	Camera, CSI 5 Data 0	2-lane Camera #6	Input	MIPI D-PHY	–	z
72	DSI_D0_P	CSI_G_D0_P					–	z
74	GND	–	GND	GND	–	GND	–	
76	DSI_CLK_N	CSI_G_CLK_N	Camera, CSI 5 Clock	2-lane Camera #6	Input	MIPI D-PHY	–	z
78	DSI_CLK_P	CSI_G_CLK_P					–	z

Pin #	Module Signal Name	Xavier Pin Name	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
80	GND	–	GND	GND	–	GND	–	–
82	DSI_D1_N	CSI_G_D1_N	Camera, CSI 5 Data 1	2-lane Camera #6	Input	MIPI D-PHY	–	z
84	DSI_D1_P	CSI_G_D1_P					–	z
86	GND	–	GND	GND	–	GND	–	–
88	DP0_HPD	DP_AUX_CH0_HPD	Display Port 0 or HDMI Hot Plug Detect	HDMI/DP Connector #0	Input	CMOS – 1.8V	DD	pd
90	DP0_AUX_N	DP_AUX_CH0_N	Display Port 0 Aux– or HDMI DDC SDA		Bidir	AC-Coupled on Carrier Board (eDP/DP)	DP_AUX	z
92	DP0_AUX_P	DP_AUX_CH0_P	Display Port 0 Aux+ or HDMI DDC SCL				DP_AUX	z
94	HDMI_CEC	HDMI_CEC	HDMI CEC	HDMI Connector	Bidir	Open Drain, 1.8V	DD	z
96	DP1_HPD	DP_AUX_CH1_HPD	Display Port 1 or HDMI Hot Plug Detect	HDMI/DP Connector #1	Input	CMOS – 1.8V	DD	pd
98	DP1_AUX_N	DP_AUX_CH1_N	Display Port 1 Aux– or HDMI DDC SDA		Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC)	DP_AUX	z
100	DP1_AUX_P	DP_AUX_CH1_P	Display Port 1 Aux+ or HDMI DDC SCL				DP_AUX	z
102	GND	–	GND	GND	–	GND	–	–
104	SPI1_MOSI	SPI3_MOSI	SPI 1 Master Out / Slave In	SPI #1 Device #0 or 1	Bidir	CMOS – 1.8V	DD	pd
106	SPI1_SCK	SPI3_SCK	SPI 1 Clock				DD	pd
108	SPI1_MISO	SPI3_MISO	SPI 1 Master In / Slave Out				DD	pd
110	SPI1_CS0*	SPI3_CS0	SPI 1 Chip Select 0				DD	z
112	SPI1_CS1*	SPI3_CS1	SPI 1 Chip Select 1				DD	z
114	CAM0_PWDN	SOC_GPIO04	Camera 0 Powerdown or GPIO	Camera #1	Output	CMOS – 1.8V	ST	pd
116	CAM0_MCLK	EXTPERIPH1_CLK	Camera 0 Reference Clock				ST	pd
118	GPIO01	SOC_GPIO41	GPIO #1 or Generic Output Clock #1	GPIO or Generic Clock	Bidir	CMOS – 1.8V	DD	pd
120	CAM1_PWDN	SOC_GPIO05	Camera 1 Powerdown or GPIO	Camera #2	Output	CMOS – 1.8V	ST	pd
122	CAM1_MCLK	EXTPERIPH2_CLK	Camera 1 Reference Clock	Camera #2	Output	CMOS – 1.8V	ST	pd
124	GPIO02	SOC_GPIO23	GPIO #2	GPIO	Bidir	CMOS – 1.8V	ST	1
126	GPIO03	SPI2_SCK	GPIO #3		Bidir	CMOS – 1.8V	DD	pd
128	GPIO05	SPI2_MOSI	GPIO #5		Bidir	CMOS – 1.8V	DD	pd
130	GPIO06	SPI2_CS0_N	GPIO #6		Bidir	CMOS – 1.8V	DD	z
132	GND	–	GND	GND	–	GND	–	–
134	PCIE0_TX0_N	NVHS0_TX0_N	PCIe #0 Transmit 0 (PCIe Ctrl #0 Lane 0)	PCIe x4 conn/device (i.e. M.2 Key M)	Output	PCIe PHY, AC-Coupled on carrier board	–	z
136	PCIE0_TX0_P	NVHS0_TX0_P					–	z
138	GND	–	GND	GND	–	GND	–	–
140	PCIE0_TX1_N	NVHS0_TX1_N	PCIe #0 Transmit 1 PCIe Ctrl #0 Lane 1)	PCIe x4 conn/device (i.e. M.2 Key M)	Output	PCIe PHY, AC-Coupled on carrier board	–	z
142	PCIE0_TX1_P	NVHS0_TX1_P					–	z
144	GND	–	GND	GND	–	GND	–	–
146	GND						–	–
148	PCIE0_TX2_N	NVHS0_TX2_N	PCIe #0 Transmit 2 (PCIe Ctrl #0 Lane 2)	PCIe x4 conn/device (i.e. M.2 Key M)	Output	PCIe PHY, AC-Coupled on carrier board	–	z
150	PCIE0_TX2_P	NVHS0_TX2_P					–	z
152	GND	–	GND	GND	–	GND	–	–
154	PCIE0_TX3_N	NVHS0_TX3_N	PCIe #0 Transmit 3 (PCIe Ctrl #0 Lane 3)	PCIe x4 conn/device (i.e. M.2 Key M)	Output	PCIe PHY, AC-Coupled on carrier board	–	z
156	PCIE0_TX3_P	NVHS0_TX3_P					–	z
158	GND	–	GND	GND	–	GND	–	–
160	PCIE0_CLK_N	PEX_CLK5N or NVHS0_REFCLK_N	PCIe #0 Reference Clock depending on setting of on-module mux controlled by Xavier CAN0_EN. See PCIe section for details.	PCIe x4 conn/device (i.e. M.2 Key M)	Bidir	PCIe PHY	–	0
162	PCIE0_CLK_P	PEX_CLK5P or NVHS0_REFCLK_P			Output		–	0
164	GND	–	GND	GND	–	GND	–	–
166	USBSS_TX_N	UPHY_TX1_N	USB SS Transmit (USB 3.0 Ctrl #2)	USB 3.0 Connector/Device/Hub	Output	USB SS PHY, AC-Coupled on carrier board	–	z
168	USBSS_TX_P	UPHY_TX1_P					–	z
170	GND	–	GND	GND	–	GND	–	–
172	PCIE1_TX0_N	UPHY_TX0_N	PCIe #1 Transmit 0 (PCIe Ctrl #1 Lane 0)	PCIe x1 conn/device (i.e. M.2 Key E)	Output	PCIe PHY, AC-Coupled on carrier board	–	z
174	PCIE1_TX0_P	UPHY_TX0_P					–	z
176	GND	–	GND	GND	–	GND	–	–
178	MOD_SLEEP*	SOC_PWR_REQ	Module Sleep. When active (low), indicates module has gone to Sleep (SC7) mode.	System	Output	CMOS – 1.8V	ST	1

Pin #	Module Signal Name	Xavier Pin Name	Usage/Description	Recommended Usage	Direction	Pin Type	MPIO Pad Code	Power-on Reset
180	PCIE0_CLKREQ*	PEX_L5_CLKREQ_N	PCIE #0 Clock Request (PCIe Ctrl #0). 47kΩ pull-up to 3.3V on the module. Input when Jetson Xavier NX is Root Port or output when Jetson Xavier NX is Endpoint.	PCIe x4 conn/device (i.e. M.2 Key M)	Bidir	Open Drain 3.3V, Pull-up on the module	DD	z
182	PCIE1_CLKREQ_N	PEX_L1_CLKREQ_N	PCIE #1 Clock Request (PCIe Ctrl #1). 47kΩ pull-up to 3.3V on the module.				DD	z
184	GBE_MDI0_N	–	GbE Transformer Data 0	LAN	Bidir	MDI	–	–
186	GBE_MDI0_P	–					–	–
188	GBE_LED_LINK	–	Ethernet Link LED (Green)		Output		–	–
190	GBE_MDI1_N	–	GbE Transformer Data 1		Bidir	MDI	–	–
192	GBE_MDI1_P	–					–	–
194	GBE_LED_ACT	–	Ethernet Activity LED (Yellow)		Output		–	–
196	GBE_MDI2_N	–	GbE Transformer Data 2		Bidir	MDI	–	–
198	GBE_MDI2_P	–					–	–
200	GND	–	GND	GND	–	GND	–	–
202	GBE_MDI3_N	–	GbE Transformer Data 3	LAN	Bidir	MDI	–	–
204	GBE_MDI3_P	–					–	–
206	GPIO07	SOC_GPIO44	GPIO #7 or Pulse Width Modulator	GPIO or PWM	Output	CMOS – 1.8V	DD	pd
208	GPIO08	SOC_GPIO22	GPIO #8 or SD Card Detect	GPIO (i.e. SD Card Detect or Fan Tach)	Bidir	CMOS – 1.8V	ST	pd
210	CLK_32K_OUT	(PMIC GPIO4 32K CLK Out)	Sleep/Suspend clock	System	Bidir	CMOS – 1.8V	–	
212	GPIO10	SOC_GPIO21	GPIO #10	GPIO	Bidir	CMOS – 1.8V	ST	pd
214	FORCE_ RECOVERY*	FORCE_ RECOVERY_N	Force Recovery strap pin	System	Input	CMOS – 1.8V	ST	pu
216	GPIO11	AUD_MCLK	GPIO #11 or Generic Output Clock #2	GPIO or Generic Clock	Bidir	CMOS – 1.8V	DD	pd
218	GPIO12	TOUCH_CLK	GPIO #12 or Pulse Width Modulator	GPIO	Bidir	CMOS – 1.8V	ST	pd
220	I2S1_DOUT	DAP3_DOUT	I2S Audio Port 1 Data Out	Audio Device (i.e. M.2 Key E)	Bidir	CMOS – 1.8V	ST	pd
222	I2S1_DIN	DAP3_DIN	I2S Audio Port 1 Data In		Input		ST	pd
224	I2S1_FS	DAP3_FS	I2S Audio Port 1 Left/Right Clock		Bidir		ST	pd
226	I2S1_SCLK	DAP3_SCLK	I2S Audio Port 1 Clock		Bidir		ST	pd
228	GPIO13	SOC_GPIO54	GPIO #13 or Pulse Width Modulator	GPIO or PWM	Bidir	CMOS – 1.8V	ST	pd
230	GPIO14	SOC_GPIO12	GPIO #14 or Pulse Width Modulator	GPIO or PWM (i.e. Fan PWM)	Bidir	CMOS – 1.8V	ST	z
232	I2C2_SCL	GEN1_I2C_SCL	General I2C 2 Clock. 2.2kΩ pull-up to 1.8V on the module.	I2C (General)	Bidir	Open Drain – 1.8V	DD	z
234	I2C2_SDA	GEN1_I2C_SDA	General I2C 2 Data. 2.2kΩ pull-up to 1.8V on the module.				DD	z
236	UART2_TXD	UART3_TX	UART #2 Transmit.	Debug UART	Output	CMOS – 1.8V	DD	pd
238	UART2_RXD	UART3_RX	UART #2 Receive		Input		DD	pd
240	SLEEP/WAKE*	POWER_ON	Configured as GPIO for optional use to indicate the system should enter or exit sleep mode.	System	Input	CMOS – 5.0V	ST	pd
242	GND	–	GND	GND	–	GND	–	–
244	GND						–	–
246	GND						–	–
248	GND						–	–
250	GND						–	–
252	VDD_IN	–	Main power – Supplies PMIC and other regs	Main DC input	Input	5.0V	–	–
254	VDD_IN						–	–
256	VDD_IN						–	–
258	VDD_IN						–	–
260	VDD_IN						–	–

Notes:

1. Green highlighting for Ground pins and Red for Power
2. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
3. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
4. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated, before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Legend Ground | Power

Chapter 14. General Routing Guidelines

14.1 Signal Name Conventions

The following conventions are used in describing the signals for Xavier:

- Signal names use a mnemonic to represent the function of the signal. For example, Secure Digital Interface #3 Command signal is represented as **SDMMC_CMD**, written in bold to distinguish it from other text. All active-low signals are identified by an asterisk (*) after the signal name. For example, **SYS_RESET*** indicates an active-low signal. Active-high signals do not have the underscore-N (**_N**) after the signal names. For example, **SDMMC_CMD** indicates an active-high signal. Differential signals are identified as a pair with the same names that end with **_P** and **_N** or for USB 2.0, DP and DN (for positive and negative, respectively). For example, **CSI_0_D0_P** and **CSI_0_D0_N** indicate a differential signal pair.
- The signal I/O type is represented as a code to indicate the operational characteristics of the signal. The following table lists the I/O codes used in the signal description tables.

Table 14-1. Signal Type Codes

Code	Definition
A	Analog
DIFF I/O	Bidirectional Differential Input/Output
DIFF IN	Differential Input
DIFF OUT	Differential Output
I/O	Bidirectional Input/Output
I	Input
O	Output
OD	Open Drain Output
I/OD	Bidirectional Input / Open Drain Output
P	Power

14.2 Routing Guideline Format

The routing guidelines have the following format to specify how a signal should be routed.

- Breakout traces are traces routed from BGA ball either to a point beyond the ball array, or to another layer where full normal spacing guidelines can be met. Breakout trace delay limited to 500 mils (1/1000 of an inch) unless otherwise specified.
- After breakout, signal should be routed according to specified impedance for differential, single-ended, or both (for example: HDMI). Trace spacing to other signals also specified.
- Follow max and min trace delays where specified. Trace delays are typically shown in "mm" (millimeter) or "in" (inch) or in terms of signal delay in "ps" (pico-seconds) or both.
  - For differential signals, trace spacing to other signals must be larger of specified × dielectric height or inter-pair spacing
  - Spacing to other signals/pairs cannot be smaller than spacing between complementary signals (intra-pair).
  - Total trace delay depends on signal velocity which is different between outer (microstrip) and inner (stripline) layers of a PCB.

14.3 Signal Routing Conventions

Throughout this design guide, the following signal routing conventions are used:

- SE Impedance (/ Diff Impedance) at x Dielectric Height Spacing
  - SE impedance of trace (along with diff impedance for diff pairs) is achieved by spacing requirement. Spacing is multiple of dielectric height. Dielectric height is typically different for microstrip and stripline. Note: 1 mil = 1/1000th of an inch.

Note: Trace spacing requirement applies to SE traces or differential pairs to other SE traces or differential pairs. It does not apply to traces making up a differential pair. For this case, spacing/trace widths are chosen to meet differential impedance requirement.

14.4 Routing Guidelines

Pay close attention when routing high speed interfaces, such as HDMI/DP, USB 3.1, PCIe or DSI/CSI. Each of these interfaces has strict routing rules for the trace impedance, width, spacing, total delay, and delay/flight time matching. The following guidelines provide an overview of the routing guidelines and notations used in this document.

- Controlled Impedance
  Each interface has different trace impedance requirements and spacing to other traces. It is up to designer to calculate trace width and spacing required to achieve specified SE and Diff impedances. Unless otherwise noted, trace impedance values are ±15%.

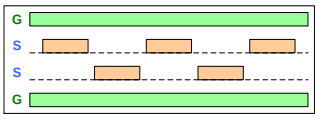
- Max Trace Lengths/Delays
  Trace lengths/delays should include the carrier board PCB routing (where the Jetson Xavier NX mating connector resides) and any additional routing on a Flex/ secondary PCB segment connected to main PCB. The max length/delay should be from Jetson Xavier NX to the actual connector (i.e. USB, HDMI, etc.) or device (i.e. onboard USB device, Display driver IC, camera imager IC, etc.)
- Trace Delay/Flight Time Matching
  Signal flight time is the time it takes for a signal to propagate from one end (driver) to other end (receiver). One way to get same flight time for signal within signal group is to match trace lengths within specified delay in the signal group.
  - Total trace delay = Carrier PCB trace delay only. Do not exceed maximum trace delay specified.
  - For six layers or more, it is recommended to match trace delays based on flight time of signals. For example, outer-layer signal velocity could be 150psi (ps/inch) and inner-layer 180psi. If one signal is routed 10 inches on outer layer and second signal is routed 10 inches in inner layer, difference in flight time between two signals will be 300ps! That is a big difference if required matching is 15ps (trace delay matching). To fix this, inner trace needs to be 1.7 inches shorter or outer trace needs to be 2 inches longer.
  - In this design guide, terms such as intra-pair and inter-pair are used when describing differential pair delays. Intra-pair refers to matching traces within differential pair (for example, true to complement trace matching). Inter-pair matching refers to matching differential pairs average delays to other differential pair average delays.

14.4.1 General PCB Routing Guidelines

For GSSG stack-up to minimize crosstalk, signal should be routed in such a way that they are not on top of each other in two routing layers (see Figure 14-1).

Do not route other signals or power traces/areas directly under or over critical high-speed interface signals.

Figure 14-1. General PCB Routing Guidelines



Note: The requirements detailed in the interface signal routing requirements tables must be met for all interfaces implemented or proper operation cannot be guaranteed.

14.5 Common High-Speed Interface Requirements

The following table describes the common high-speed interface requirements.

Table 14-2. Common High-Speed Interface Requirements

Parameter	Requirement	Units	Notes
Common-mode Choke (Not recommended – only used if absolutely required for EMI issues)			
Preferred device			Type: TDK ACM2012D-900-2P. Only if needed. Place near connector. Refer to Common Mode Choke Requirement section.
Location - Max distance from to adjacent discontinuities – ex, connector, AC cap)	8 (53)	mm (ps)	TDK ACM2012D-900-2P See Figure 14-2
Common-mode impedance @ 100MHz Min/Max	65/90	Ω	
Max Rdc	0.3	Ω	
Differential TDR impedance	90	Ω	@T_R-200ps (10%-90%)
Min Sdd21 @ 2.5GHz	2.22	dB	
Max Scc21 @ 2.5GHz	19.2	dB	
Serpentine			
Min bend angle	135	deg (α)	S1 must be taken care in order to consider Xtalk to adjacent pair. See USB 3.1 Guideline in Figure 14-3.
Dimension Min A Spacing Min B, C Length Min Jog Width	4x 1.5x 3x	Trace width	
General			
Routing over Voids	Routing over voids not allowed except void around device ball/pin the signal is routed to.		
Noise Coupling	Keep critical high-speed traces away from other signal traces or unrelated power traces/areas or power supply components		

The following figures show the common high-speed interface signal routing requirements.

Figure 14-2. Common Mode Chok

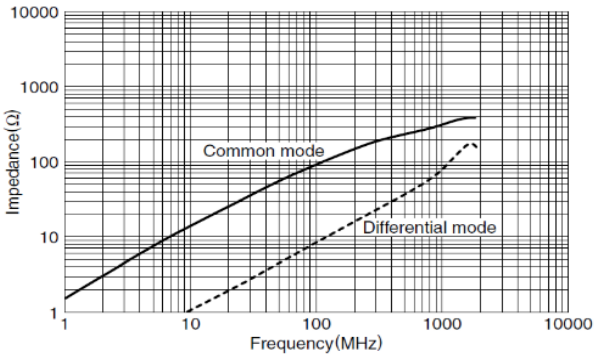
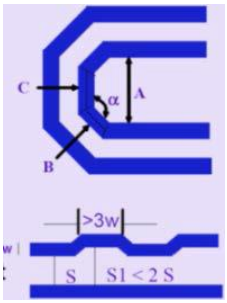


Figure 14-3. Serpentine



Notice

This document is provided for information purposes only and shall not be regarded as a warranty of a certain functionality, condition, or quality of a product. NVIDIA Corporation ("NVIDIA") makes no representations or warranties, expressed or implied, as to the accuracy or completeness of the information contained in this document and assumes no responsibility for any errors contained herein. NVIDIA shall have no liability for the consequences or use of such information or for any infringement of patents or other rights of third parties that may result from its use. This document is not a commitment to develop, release, or deliver any Material (defined below), code, or functionality.

NVIDIA reserves the right to make corrections, modifications, enhancements, improvements, and any other changes to this document, at any time without notice.

Customer should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

NVIDIA products are sold subject to the NVIDIA standard terms and conditions of sale supplied at the time of order acknowledgement, unless otherwise agreed in an individual sales agreement signed by authorized representatives of NVIDIA and customer ("Terms of Sale"). NVIDIA hereby expressly objects to applying any customer general terms and conditions with regards to the purchase of the NVIDIA product referenced in this document. No contractual obligations are formed either directly or indirectly by this document.

Unless specifically agreed to in writing by NVIDIA, NVIDIA products are not designed, authorized, or warranted to be suitable for use in medical, military, aircraft, space, or life support equipment, nor in applications where failure or malfunction of the NVIDIA product can reasonably be expected to result in personal injury, death, or property or environmental damage. NVIDIA accepts no liability for inclusion and/or use of NVIDIA products in such equipment or applications and therefore such inclusion and/or use is at customer's own risk.

NVIDIA makes no representation or warranty that products based on this document will be suitable for any specified use. Testing of all parameters of each product is not necessarily performed by NVIDIA. It is customer's sole responsibility to evaluate and determine the applicability of any information contained in this document, ensure the product is suitable and fit for the application planned by customer, and perform the necessary testing for the application in order to avoid a default of the application or the product. Weaknesses in customer's product designs may affect the quality and reliability of the NVIDIA product and may result in additional or different conditions and/or requirements beyond those contained in this document. NVIDIA accepts no liability related to any default, damage, costs, or problem which may be based on or attributable to: (i) the use of the NVIDIA product in any manner that is contrary to this document or (ii) customer product designs.

No license, either expressed or implied, is granted under any NVIDIA patent right, copyright, or other NVIDIA intellectual property right under this document. Information published by NVIDIA regarding third-party products or services does not constitute a license from NVIDIA to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property rights of the third party, or a license from NVIDIA under the patents or other intellectual property rights of NVIDIA.

Reproduction of information in this document is permissible only if approved in advance by NVIDIA in writing, reproduced without alteration and in full compliance with all applicable export laws and regulations, and accompanied by all associated conditions, limitations, and notices.

THIS DOCUMENT AND ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY, OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NONINFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE. TO THE EXTENT NOT PROHIBITED BY LAW, IN NO EVENT WILL NVIDIA BE LIABLE FOR ANY DAMAGES, INCLUDING WITHOUT LIMITATION ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES, HOWEVER CAUSED AND REGARDLESS OF THE THEORY OF LIABILITY, ARISING OUT OF ANY USE OF THIS DOCUMENT, EVEN IF NVIDIA HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. Notwithstanding any damages that customer might incur for any reason whatsoever, NVIDIA's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms of Sale for the product.

VESA DisplayPort

DisplayPort and DisplayPort Compliance Logo, DisplayPort Compliance Logo for Dual-mode Sources, and DisplayPort Compliance Logo for Active Cables are trademarks owned by the Video Electronics Standards Association in the United States and other countries.

HDMI

HDMI, the HDMI logo, and High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing LLC.

Trademarks

NVIDIA, the NVIDIA logo, Jetson, Jetson Xavier, and Xavier are trademarks and/or registered trademarks of NVIDIA Corporation in the U.S. and other countries. Other company and product names may be trademarks of the respective companies with which they are associated.

Copyright

NVIDIA Corporation | 2788 San Tomas Expressway, Santa Clara, CA 95051
http://www.nvidia.com