MT7622 Reference Manual for Development Board

Version: v1.0
Release date: 2018-12-19

Document Revision History

Revision	Date	Author	Description
1.0	2018-12-07	PeterCT Wu	Initial Release

Table of Contents

1 General System

1.1 Top-Clock Generator

1.1.1 Introduction

This chapter introduces the clock generator (TOPCKGEN) inside CKSYS.

1.1.2 Features

TOPCKGEN is responsible for generating the following clock signals:

- Free clock generation for whole chip
- Cortex-A53 CPU clock
- Infrastructure and peripheral system clock, including the top level AXI fabric clock
- Ethernet DMA system clock
- Pad clocks to be synchronized with one of the above system

TOPCKGEN provides a serious of clock of every IPs. Each clock has several clock sources and can be turned off as well. When switching certain clock from frequency A to frequency B, make sure frequency A and B are available or system could be hang. It also comprises glitch-free clock MUX and digital clock divider to generate various clock frequencies.

1.1.3 Block Diagram

1.1.3.1 CKSYS

There are four critical modules inside CKSYS. First one is strap controller, used to capture HW strap value while PAD_SYSRSTB is released. The HW strap definition is described in the begging of this programming guide. The second is TOPCKGEN, this is the major module of this chapter mentioned in next paragraph. The third one is top reset generation unit (TOPRGU), it's a miscellaneous controller of POR, system SW reset and system watch dog reset. And the latest module is RTC controller. Its basic function is real time and alarm clocks.

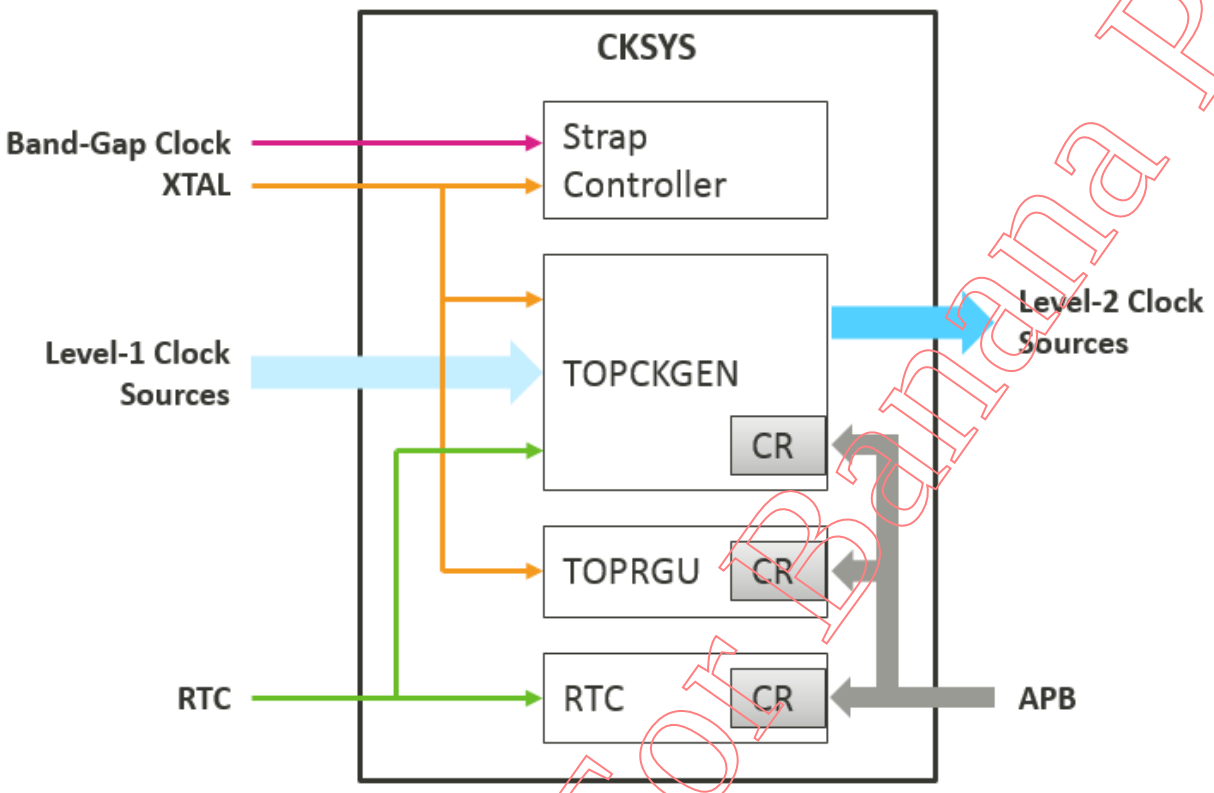


Figure 1-1. CKSYS Block Diagram

1.1.3.2 TOPCKGEN

TOPCKGEN is constructed by clock dividers, multiplexers (MUXs), meter modules and top dynamic clock management (DCM) modules.

The clock dividers divide level-1 clock sources into several divided clocks. And the divided number of each dividers are difference base on level-2 clock requirements.

Table 1-1 TOPCKGEN Divider List

Level-1 Clock Source	Divided Number	Divided Clock Source (MHz)
MEMPLL_CK	1/2/4/8	400/200/100/50
MAINPLL_Div2_CK	1/2/4/8/16	560/280/140/70/35
MAINPLL_Div3_CK	1/2/4/8/16	373.33/186.67/93.33/46.67/23.33
MAINPLL_Div5_CK	1/2/4/8/16	224/112/56/28/14
MAINPLL_Div7_CK	1/2/4/8/16	160/80/40/20/10
UNIVPLL_Div2_CK	1/2/4/8/16	600/300/150/75/37.5
UNIVPLL_Div3_CK	1/2/4/8/16	400/200/100/50/25
UNIVPLL_Div5_CK	1/2/4/8/16	240/120/60/30/15
UNIVPLL_Div7_CK	1/2/4/8	171.43/85.71/42.86/21.43/10.71
UNIVPLL_Div80_CK	1/2/4	15/7.5/3.75

SGMIIPLL_CK	**1/2**	650/325
XTAL	**1/2**	25/12.5 or 40/20 base on HW strap

There is a group of regular MUXs or buffers to choose the suitable sources from divided clocks or level-1 clocks directly to become level-2. All the clock MUXs have three kinds of control function (as shown in Table). XTAL always be one of the clock MUXs' sources and also selected as default value to avoid system hang when PLL was broken.

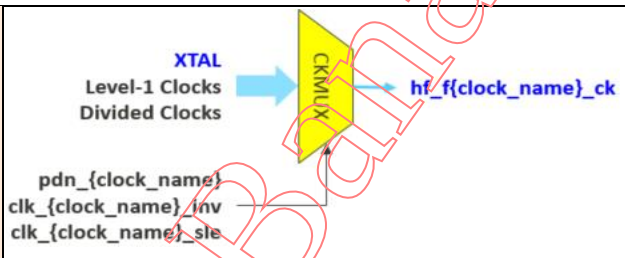
Related Registers: **CLK_CFG_0~7** **CLK_CFG_0~7_SET** **CLK_CFG_0~7_CLR**	
Control Function 0 - pdn_*	Turn off CKMUX output
Control Function 1 - clk_*_inv	Inverse CKMUX output phase
Control Function 2 - clk_*_sel	Select CKMUX source

Figure 1-2 TOPCKGEN Clock Multiplexer

There are also some clock gating related functions inside TOPCKGEN listed in following table below.

***Table 1-2* TOPCKGEN Clock Gating Setting**

Register name	Bit	Function name	Description
CLK_MODE	[0]	topckgen_pdn	Gating clock MUXs control function's clock
CLK_SCP_CFG_0	[0]	sc_26ck_off_en	Enable SCPSYS to control XTAL gating function
	[4]	sc_armck_off_en	Enable SCPSYS to control hf_farm_ck gating function
CLK_SCP_CFG_1	[0]	sc_axi_26m_sel_en	Enable SCPSYS to control hf_faxi_ck MUX function

Except clock dividers and clock MUXs, there are also two DCM modules which is used to gate the top level AXI fabric clocks (hf_faxi_ck and hf_fmem_ck) when bus was idle. And finally there are also building in two clock monitor modules used to measure and probe out the level-1 and 2 clocks for testing.

1.1.4 Register Definition

Module name: TOPCKGEN Base address: (+10210000h)

Address	Name	Width	Register Function
10210000	CLK_MODE	32	**Clock 26M, 32K PDN Control Register**
10210004	DCM_CFG	32	**AXI Bus Clock DCM Control Register**
10210020	TST_SEL_0	32	**Test Clock Selection Register 0**
10210024	TST_SEL_1	32	**Test Clock Selection Register 1**

Address	Name	Width	Register Function
10210028	TST_SEL_2	32	Test Clock Selection Register 2
10210040	CLK_CFG_0	32	Function Clock Selection Register 0
10210044	CLK_CFG_0_SET	32	SET Control of CLK_CFG_0
10210048	CLK_CFG_0_CLR	32	CLR Control of CLK_CFG_0
10210050	CLK_CFG_1	32	Function Clock Selection Register 1
10210054	CLK_CFG_1_SET	32	SET Control of CLK_CFG_1
10210058	CLK_CFG_1_CLR	32	CLR Control of CLK_CFG_1
10210060	CLK_CFG_2	32	Function Clock Selection Register 2
10210064	CLK_CFG_2_SET	32	SET Control of CLK_CFG_2
10210068	CLK_CFG_2_CLR	32	CLR Control of CLK_CFG_2
10210070	CLK_CFG_3	32	Function Clock Selection Register 3
10210074	CLK_CFG_3_SET	32	SET Control of CLK_CFG_3
10210078	CLK_CFG_3_CLR	32	CLR Control of CLK_CFG_3
10210080	CLK_CFG_4	32	Function Clock Selection Register 4
10210084	CLK_CFG_4_SET	32	SET Control of CLK_CFG_4
10210088	CLK_CFG_4_CLR	32	CLR Control of CLK_CFG_4
10210090	CLK_CFG_5	32	Function Clock Selection Register 5
10210094	CLK_CFG_5_SET	32	SET Control of CLK_CFG_5
10210098	CLK_CFG_5_CLR	32	CLR Control of CLK_CFG_5
102100A0	CLK_CFG_6	32	Function Clock Selection Register 6
102100A4	CLK_CFG_6_SET	32	SET Control of CLK_CFG_6
102100A8	CLK_CFG_6_CLR	32	CLR Control of CLK_CFG_6
102100B0	CLK_CFG_7	32	Function Clock Selection Register 7
102100B4	CLK_CFG_7_SET	32	SET Control of CLK_CFG_7
102100B8	CLK_CFG_7_CLR	32	CLR Control of CLK_CFG_7
10210100	CLK_CFG_8	32	Function Clock Selection Register 8
10210104	CLK_CFG_9	32	Function Clock Selection Register 9
10210108	CLK_CFG_10	32	Debug Monitor Clock Selection Register
1021010C	CLK_CFG_11	32	Debug Monitor Divider Control Register
10210120	CLK_AUDDIV_0	32	Audio Clock Divider Control Register 0
10210124	CLK_AUDDIV_1	32	Audio Clock Divider Control Register 1
10210128	CLK_AUDDIV_2	32	Audio Clock Divider Control Register 2
10210200	CLK_SCP_CFG_0	32	SCP Control Register 0
10210204	CLK_SCP_CFG_1	32	SCP Control Register 1
10210210	CLK_MISC_CFG_0	32	MCU Clock Jitter Measurement Control Register
10210214	CLK_MISC_CFG_1	32	Frequency Meter Divider Control Register
10210218	CLK_MISC_CFG_2	32	MEM DCM Idle Signal Force Control
10210220	CLK26CALI_0	32	Frequency Meter Control Register 0
10210224	CLK26CALI_1	32	Frequency Meter Control Register 1
10210228	CLK26CALI_2	32	Frequency Meter Control Register 2
1021022C	CKSTA_REG	32	Function Clock Selection Status Register
10210230	TEST_MODE_CFG	32	Test Mode Control Register

Address	Name	Width	Register Function
10210308	MBIST_CFG_0	32	Debug Monitor Selection Register 0
1021030C	MBIST_CFG_1	32	Debug Monitor Selection Register 1
10210310	MBIST_CFG_2	32	Reset Deglitch Enable Key Register
10210314	MBIST_CFG_3	32	Debug Monitor Selection Register 3
10210500	WDT_MODE_DUMMY	32	Dummy register for WDT
10210508	WDT_RESTART_DUMMY	32	Dummy register for WDT
10210518	WDT_SWSYSRST_DUMMY	32	Dummy register for WDT
10210520	WDT_NONRST_REG_DUMMY	32	Dummy register for WDT
10210550	WDT_INTERCORE_SYNC_DUMMY	32	Dummy register for WDT
10210554	WDT_INTERCORE_SYNC_DUMMY_SET	32	Dummy register for WDT
10210558	WDT_INTERCORE_SYNC_DUMMY_CLR	32	Dummy register for WDT

10210000 CLK_MODE Clock 26M, 32K PDN Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													rtc_sel		pdn_25k	pdn_topckgen
Type													RW		RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3:2	rtc_sel	**RTC clock selection** 0: ~24K or ~39K from XTAL divide 1024 1: 32K form RTC 2: ~25K from PMU bandgap clock 3: ~24K or ~39K from XTAL divide 1024
1	pdn_25k	**Turns off 25K clock generator** 0: Disable 1: Enable
0	pdn_topckgen	**Turns off TOPCKGEN clock** 0: Disable 1: Enable

10210004 **DCM_CFG** **AXI Bus Clock DCM Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mem_dcm_dbc_enable	mem_dcm_dbc_cnt							mem_dcm_enable	mem_dcm_idle_align	mem_dcm_cfg_latch	mem_dcm_full_fsel				
Type	RW	RW							RW	RW	RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcm_dbc_enable	dcm_dbc_cnt							dcm_enable			dcm_full_fsel				
Type	RW	RW							RW			RW				
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Name	Description
31	mem_dcm_dbc_enable	**Enables DCM de-bounce counter** 0: Disble DCM de-bounce counter 1: Enable DCM de-bounce counter
30:24	mem_dcm_dbc_cnt	**DCM de-bounce counter**
23	mem_dcm_enable	**Enables hf_fmem_ck DCM** 0: Disable DCM 1: Enable DCM
22	mem_dcm_idle_align	**Enables hf_fmem_ck DCM idle align** 0: Disable hf_fmem_ck DCM idle align 1: Enable hf_fmem_ck DCM idle align
21	mem_dcm_cfg_latch	**Latches rising edge trigger mem_dcm configuration** 0->1: Trigger 1->0: Trigger
20:16	mem_dcm_full_fsel	**Selects hf_fmem_ck DCM clock** 1xxxx: hd_fmem_ck = hf_fmem_ck 01xxx: hd_fmem_ck = hf_fmem_ck/2 001xx: hd_fmem_ck = hf_fmem_ck/4 0001x: hd_fmem_ck = hf_fmem_ck/8 00001: hd_fmem_ck = hf_fmem_ck/16 00000: hd_fmem_ck = hf_fmem_ck/32
15	dcm_dbc_enable	**Enables DCM de-bounce counter** 0: Disble DCM de-bounce counter 1: Enable DCM de-bounce counter
14:8	dcm_dbc_cnt	**DCM de-bounce counter**
7	dcm_enable	**Enables hf_faxi_ck DCM** 0: Disable DCM 1: Enable DCM
4:0	dcm_full_fsel	**Selects hf_faxi_ck DCM clock** 1xxxx: hd_faxi_ck = hf_faxi_ck 01xxx: hd_faxi_ck = hf_faxi_ck/2

Bit(s)	Name	Description
		001xx: hd_faxi_ck = hf_faxi_ck/4 0001x: hd_faxi_ck = hf_faxi_ck/8 00001: hd_faxi_ck = hf_faxi_ck/16 00000: hd_faxi_ck = hf_faxi_ck/32

10210020 TST_SEL_0 Test Clock Selection Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10210024 TST_SEL_1 Test Clock Selection Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10210028 TST_SEL_2 Test Clock Selection Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																

Type																
Reset																

Bit(s)	Name	Description

10210040 CLK_CFG_0 Function Clock Selection Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_eth			clk_eth_inv		clk_eth_sel			pdn_ddrphycfg			clk_ddrphycfg_inv				clk_ddrphycfg_sel
Type	RW			RW		RW			RW			RW				RW
Reset	0			0		0	0	0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_mem			clk_mem_inv				clk_mem_sel	pdn_axi			clk_axi_inv		clk_axi_sel		
Type	RW			RW				RW	RW			RW		RW		
Reset	0			0				0	0			0		0	0	0

Bit(s)	Name	Description
31	pdn_eth	**Turns off hf_feth_ck** 1: Enable clock off
28	clk_eth_inv	**hf_feth_ck clock phase invert** 1: Enable phase invert
26:24	clk_eth_sel	**hf_feth_ck clock mux select** 0: clkxtal 1: syspll1_d2_280MHz 2: univpll1_d2_300MHz 3: syspll1_d4_140MHz 4: univpll_d5_240MHz 5: sgmiipll_d2_325MHz 6: univpll_d7_171P429MHz 7: dmpll_ck_400MHz
23	pdn_ddrphycfg	**Turns off hf_fddrphycfg_ck** 1: Enable clock off
20	clk_ddrphycfg_inv	**hf_fddrphycfg_ck clock phase invert** 1: Enable phase invert
16	clk_ddrphycfg_sel	**hf_fddrphycfg_ck clock mux select** 0: clkxtal 1: syspll1_d8_70MHz
15	pdn_mem	**Turns off hf_fmem_ck** 1: Enable clock off
12	clk_mem_inv	**hf_fmem_ck clock phase invert**

Bit(s)	Name	Description
		1: Enable phase invert
8	clk_mem_sel	**hf_fmem_ck clock mux select** 0: clkxtal 1: dmpll_ck_400MHz
7	pdn_axi	**Turns off hf_faxi_ck** 1: Enable clock off
4	clk_axi_inv	**hf_faxi_ck clock phase invert** 1: Enable phase invert
2:0	clk_axi_sel	**hf_faxi_ck clock mux select** 0: clkxtal 1: syspll1_d2_280MHz 2: syspll_d5_224MHz 3: syspll1_d4_140MHz 4: univpll_d5_240MHz 5: univpll2_d2_200MHz 6: univpll_d7_171P429MHz 7: dmpll_ck_400MHz

10210044 CLK_CFG_0_SET SET Control of CLK_CFG_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_0_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_0_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_0_set	**Sets the correspondent bit of CLG_CFG_SEL_0** 0: Unchange 1: Set 1'b1 to the correspondent bit

10210048 CLK_CFG_0_CLR CLR Control of CLK_CFG_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_0_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_0_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_0_clr	**Clears the correspondent bit of CLG_CFG_SEL_0** 0: Unchange 1: Set 1'b0 to the correspondent bit

10210050 CLK_CFG_1 Function Clock Selection Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_flash			clk_flash_inv		clk_flash_sel			pdn_spinfi_infra_bclk			clk_spinfi_infra_bclk_inv	clk_spinfi_infra_bclk_sel			
Type	RW			RW		RW			RW			RW	RW			
Reset	0			0		0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_f10m_ref			clk_f10m_ref_inv				clk_f10m_ref_sel	pdn_pwm			clk_pwm_inv			clk_pwm_sel	
Type	RW			RW				RW	RW			RW			RW	
Reset	0			0				0	0			0			0	0

Bit(s)	Name	Description
31	pdn_flash	**Turns off hf_fflash_ck** 1: Enable clock off
28	clk_flash_inv	**hf_fflash_ck clock phase invert** 1: Enable phase invert
26:24	clk_flash_sel	**hf_fflash_ck clock mux select** 0: clkxtal 1: univpll_div80_d4_3P75MHz 2: syspll2_d8_46P667MHz 3: syspll3_d4_56MHz 4: univpll3_d4_60MHz 5: univpll1_d8_75MHz 6: syspll2_d4_93P333MHz 7: univpll2_d4_100MHz
23	pdn_spinfi_infra_bclk	**Turns off hf_fspinfi_infra_bclk_ck** 1: Enable clock off
20	clk_spinfi_infra_bclk_inv	**hf_fspinfi_infra_bclk_ck clock phase invert** 1: Enable phase invert
19:16	clk_spinfi_infra_bclk_sel	**hf_fspinfi_infra_bclk_ck clock mux select** 0: clkxtal 1: clkxtal 2: clkxtal 3: clkxtal

Bit(s)	Name	Description
		4: clkxtal 5: clkxtal 6: clkxtal 7: clkxtal 8: univpll2_d8_50MHz 9: syspll1_d8_70MHz 10: univpll1_d8_75MHz 11: syspll4_d2_80MHz 12: univpll2_d4_100MHz 13: univpll3_d2_120MHz 14: syspll1_d4_140MHz 15: syspll_d7_160MHz
15	pdn_f10m_ref	**Turns off hf_f10m_ck** 1: Enable clock off
12	clk_f10m_ref_inv	**hf_f10m_ck clock phase invert** 1: Enable phase invert
8	clk_f10m_ref_sel	**hf_f10m_ck clock mux select** 0: clkxtal 1: syspll4_d16_10MHz
7	pdn_pwm	**Turns off f_fpwm_ck** 1: Enable clock off
4	clk_pwm_inv	**f_fpwm_ck clock phase invert** 1: Enable phase invert
1:0	clk_pwm_sel	**f_fpwm_ck clock mux select** 0: clkxtal 1: univpll2_d4_100MHz 2: univpll3_d2_120MHz 3: univpll1_d4_150MHz

10210054 CLK_CFG_1_SET SET Control of CLK_CFG_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_1_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_1_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_1_set	**Sets the correspondent bit of CLG_CFG_SEL_1** 0: Unchange 1: Set 1'b1 to the correspondent bit

10210058 CLK_CFG_1_CLR CLR Control of CLK_CFG_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_1_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_1_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_1_clr	**Clears the correspondent bit of CLG_CFG_SEL_1** 0: Unchange 1: Set 1'b0 to the correspondent bit

10210060 CLK_CFG_2 Function Clock Selection Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_msdc50_0			clk_msdc50_0_inv		clk_msdc50_0_sel			pdn_spi1			clk_spi1_inv		clk_spi1_sel		
Type	RW			RW		RW			RW			RW		RW		
Reset	0			0		0	0	0	0			0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_spi0			clk_spi0_inv		clk_spi0_sel			pdn_uart			clk_uart_inv				clk_uart_sel
Type	RW			RW		RW			RW			RW				RW
Reset	0			0		0	0	0	0			0				0

Bit(s)	Name	Description
31	pdn_msdc50_0	**Turns off hf_fmsdc50_0_ck** 1: Enable clock off
28	clk_msdc50_0_inv	**hf_fmsdc50_0_ck clock phase invert** 1: Enable phase invert
26:24	clk_msdc50_0_sel	**hf_fmsdc50_0_ck clock mux select** 0: clkxtal 1: univpll2_d8_50MHz 2: univpll2_d4_100MHz 3: syspll_d7_160MHz 4: univpll2_d2_200MHz 5: univpll_d5_240MHz 6: univpll1_d2_300MHz 7: univpll_d3_400MHz
23	pdn_spi1	**Turns off hf_fspi1_ck**

Bit(s)	Name	Description
		1: Enable clock off
20	clk_spi1_inv	**hf_fspi1_ck clock phase invert** 1: Enable phase invert
18:16	clk_spi1_sel	**hf_fspi1_ck clock mux select** 0: clkxtal 1: syspll3_d2_112MHz 2: clkxtal 3: syspll2_d4_93P333MHz 4: syspll4_d2_80MHz 5: univpll2_d4_100MHz 6: univpll1_d8_75MHz 7: clkxtal
15	pdn_spi0	**Turns off hf_fspi0_ck** 1: Enable clock off
12	clk_spi0_inv	**hf_fspi0_ck clock phase invert** 1: Enable phase invert
10:8	clk_spi0_sel	**hf_fspi0_ck clock mux select** 0: clkxtal 1: syspll3_d2_112MHz 2: clkxtal 3: syspll2_d4_93P333MHz 4: syspll4_d2_80MHz 5: univpll2_d4_100MHz 6: univpll1_d8_75MHz 7: clkxtal
7	pdn_uart	**Turns off f_fuart_ck** 1: Enable clock off
4	clk_uart_inv	**f_fuart_ck clock phase invert** 1: Enable phase invert
0	clk_uart_sel	**f_fuart_ck clock mux select** 0: clkxtal 1: univpll2_d8_50MHz

10210064 CLK_CFG_2_SET SET Control of CLK_CFG_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_2_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_2_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_2_set	**Sets the correspondent bit of CLG_CFG_SEL_2** 0: Unchange

Bit(s)	Name	Description
		1: Set 1'b1 to the correspondent bit

10210068 CLK_CFG_2_CLR CLR Control of CLK_CFG_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_2_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_2_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_2_clr	**Clears the correspondent bit of CLG_CFG_SEL_2** 0: Unchange 1: Set 1'b0 to the correspondent bit

10210070 CLK_CFG_3 Function Clock Selection Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_a2sys_hp			clk_a2sys_hp_inv			clk_a2sys_hp_sel		pdn_a1sys_hp			clk_a1sys_hp_inv			clk_a1sys_hp_sel	
Type	RW			RW			RW		RW			RW			RW	
Reset	0			0			0	0	0			0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_msdc30_1			clk_msdc30_1_inv		clk_msdc30_1_sel			pdn_msdc30_0			clk_msdc30_0_inv		clk_msdc30_0_sel		
Type	RW			RW		RW			RW			RW		RW		
Reset	0			0		0	0	0	0			0		0	0	0

Bit(s)	Name	Description
31	pdn_a2sys_hp	**Turns off hf_fa2sys_hp_ck** 1: Enable clock off
28	clk_a2sys_hp_inv	**hf_fa2sys_hp_ck clock phase invert** 1: Enable phase invert
25:24	clk_a2sys_hp_sel	**hf_fa2sys_hp_ck clock mux select** 0: clkxtal 1: aud1pll_ck_294P912MHz

Bit(s)	Name	Description
		2: aud2pll_ck_270P9504MHz
		3: clkxtal
23	pdn_a1sys_hp	**Turns off hf_fa1sys_hp_ck** 1: Enable clock off
20	clk_a1sys_hp_inv	**hf_fa1sys_hp_ck clock phase invert** 1: Enable phase invert
17:16	clk_a1sys_hp_sel	**hf_fa1sys_hp_ck clock mux select** 0: clkxtal 1: aud1pll_ck_294P912MHz 2: aud2pll_ck_270P9504MHz 3: clkxtal
15	pdn_msdc30_1	**Turns off hf_fmsdc30_1_ck** 1: Enable clock off
12	clk_msdc30_1_inv	**hf_fmsdc30_1_ck clock phase invert** 1: Enable phase invert
10:8	clk_msdc30_1_sel	**hf_fmsdc30_1_ck clock mux select** 0: clkxtal 1: univpll2_d16_25MHz 2: univ48m_ck 3: syspll2_d4_93P333MHz 4: univpll2_d4_100MHz 5: syspll_d7_160MHz 6: syspll2_d2_186P667MHz 7: univpll2_d2_200MHz
7	pdn_msdc30_0	**Turns off hf_fmsdc30_0_ck** 1: Enable clock off
4	clk_msdc30_0_inv	**hf_fmsdc30_0_ck clock phase invert** 1: Enable phase invert
2:0	clk_msdc30_0_sel	**hf_fmsdc30_0_ck clock mux select** 0: clkxtal 1: univpll2_d16_25MHz 2: univ48m_ck 3: syspll2_d4_93P333MHz 4: univpll2_d4_100MHz 5: syspll_d7_160MHz 6: syspll2_d2_186P667MHz 7: univpll2_d2_200MHz

10210074 CLK_CFG_3_SET SET Control of CLK_CFG_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_3_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_3_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_3_set	**Sets the correspondent bit of CLG_CFG_SEL_3** 0: Unchange 1: Set 1'b1 to the correspondent bit

10210078 CLK_CFG_3_CLR CLR Control of CLK_CFG_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_3_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_3_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_3_clr	**Clears the correspondent bit of CLG_CFG_SEL_3** 0: Unchange 1: Set 1'b0 to the correspondent bit

10210080 CLK_CFG_4 Function Clock Selection Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_scp			clk_scp_inv			clk_scp_sel		pdn_pmicspi			clk_pmicspi_inv		clk_pmicspi_sel		
Type	RW			RW			RW		RW			RW		RW		
Reset	0			0			0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_aud_intbus			clk_aud_intbus_inv			clk_aud_intbus_sel		pdn_intdir			clk_intdir_inv			clk_intdir_sel	
Type	RW			RW			RW		RW			RW			RW	
Reset	0			0			0	0	0			0			0	0

Bit(s)	Name	Description
31	pdn_scp	**Turns off hf_fscp_ck** 1: Enable clock off
28	clk_scp_inv	**hf_fscp_ck clock phase invert**

Bit(s)	Name	Description
		1: Enable phase invert
25:24	clk_scp_sel	**hf_fscp_ck clock mux select** 0: clkxtal 1: syspll1_d8_70MHz 2: univpll2_d2_200MHz 3: univpll2_d4_100MHz
23:21	pdn_pmicspi	**Turns off hf_fpmicspi_ck** 1: Enable clock off
20	clk_pmicspi_inv	**hf_fpmicspi_ck clock phase invert** 1: Enable phase invert
18:16	clk_pmicspi_sel	**hf_fpmicspi_ck clock mux select** 0: clkxtal 1: syspll1_d8_70MHz 2: syspll3_d4_56MHz 3: syspll1_d16_35MHz 4: univpll3_d4_60MHz 5: univpll2_d16_25MHz 6: univpll2_d4_100MHz 7: dmpll_d8_50MHz
15	pdn_aud_intbus	**Turns off hf_faud_intbus_ck** 1: Enable clock off
12	clk_aud_intbus_inv	**hf_faud_intbus_ck clock phase invert** 1: Enable phase invert
9:8	clk_aud_intbus_sel	**hf_faud_intbus_ck clock mux select** 0: clkxtal 1: syspll1_d4_140MHz 2: syspll4_d2_80MHz 3: syspll3_d2_112MHz
7	pdn_intdir	**Turns off hf_fintdir_ck** 1: Enable clock off
4	clk_intdir_inv	**hf_fintdir_ck clock phase invert** 1: Enable phase invert
1:0	clk_intdir_sel	**hf_fintdir_ck clock mux select** 0: clkxtal 1: syspll_d2_560MHz 2: univpll_d2_600MHz 3: sgmiipll_ck_650MHz

10210084 CLK_CFG_4_SET SET Control of CLK_CFG_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_4_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_4_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_4_set	**Sets the correspondent bit of CLG_CFG_SEL_4** 0: Unchange 1: Set 1'b1 to the correspondent bit

10210088 CLK_CFG_4_CLR CLR Control of CLK_CFG_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_4_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_4_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_4_clr	**Clears the correspondent bit of CLG_CFG_SEL_4** 0: Unchange 1: Set 1'b0 to the correspondent bit

10210090 CLK_CFG_5 Function Clock Selection Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_usb20			clk_usb20_inv			clk_usb20_sel		pdn_audio			clk_audio_inv			clk_audio_sel	
Type	RW			RW			RW		RW			RW			RW	
Reset	0			0			0	0	0			0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_hif			clk_hif_inv		clk_hif_sel			pdn_atb			clk_atb_inv			clk_atb_sel	
Type	RW			RW		RW			RW			RW			RW	
Reset	0			0		0	0	0	0			0			0	0

Bit(s)	Name	Description
31	pdn_usb20	**Turns off hf_fusb20_ck** 1: Enable clock off
28	clk_usb20_inv	**hf_fusb20_ck clock phase invert** 1: Enable phase invert
25:24	clk_usb20_sel	**hf_fusb20_ck clock mux select**

Bit(s)	Name	Description
		0: clkxtal 1: univpll3_d4_60MHz 2: syspll1_d8_70MHz 3: clkxtal
23	pdn_audio	**Turns off f_faudio_ck** 1: Enable clock off
20	clk_audio_inv	**f_faudio_ck clock phase invert** 1: Enable phase invert
17:16	clk_audio_sel	**f_faudio_ck clock mux select** 0: clkxtal 1: syspll3_d4_56MHz 2: syspll4_d4_40MHz 3: univpll1_d16_37P5MHz
15	pdn_hif	**Turns off hf_fhif_ck** 1: Enable clock off
12	clk_hif_inv	**hf_fhif_ck clock phase invert** 1: Enable phase invert
10:8	clk_hif_sel	**hf_fhif_ck clock mux select** 0: clkxtal 1: syspll1_d2_280MHz 2: univpll1_d2_300MHz 3: syspll1_d4_140MHz 4: univpll_d5_240MHz 5: sgmiipll_d2_325MHz 6: univpll_d7_171P429MHz 7: dmpll_ck_400MHz
7	pdn_atb	**Turns off hf_fatb_ck** 1: Enable clock off
4	clk_atb_inv	**hf_fatb_ck clock phase invert** 1: Enable phase invert
1:0	clk_atb_sel	**hf_fatb_ck clock mux select** 0: clkxtal 1: syspll1_d2_280MHz 2: syspll_d5_224MHz 3: dmpll_ck_400MHz

10210094 CLK_CFG_5_SET SET Control of CLK_CFG_5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_5_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_5_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_5_set	**Sets the correspondent bit of CLG_CFG_SEL_5** 0: Unchange 1: Set 1'b1 to the correspondent bit

10210098 CLK_CFG_5_CLR CLR Control of CLK_CFG_5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_5_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_5_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_5_clr	**Clears the correspondent bit of CLG_CFG_SEL_5** 0: Unchange 1: Set 1'b0 to the correspondent bit

102100A0 CLK_CFG_6 Function Clock Selection Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_irtx			clk_irtx_inv				clk_irtx_sel	pdn_irrx			clk_irrx_inv				clk_irrx_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_aud2			clk_aud2_inv				clk_aud2_sel	pdn_aud1			clk_aud1_inv				clk_aud1_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0

Bit(s)	Name	Description
31	pdn_irtx	**Turns off hf_firtx_ck** 1: Enable clock off
28	clk_irtx_inv	**hf_firtx_ck clock phase invert** 1: Enable phase invert
24	clk_irtx_sel	**hf_firtx_ck clock mux select** 0: clkxtal 1: syspll4_d16_10MHz

Bit(s)	Name	Description
23	pdn_irrx	**Turns off hf_firrx_ck** 1: Enable clock off
20	clk_irrx_inv	**hf_firrx_ck clock phase invert** 1: Enable phase invert
16	clk_irrx_sel	**hf_firrx_ck clock mux select** 0: clkxtal 1: syspll4_d16_10MHz
15	pdn_aud2	**Turns off f_faud2_ck** 1: Enable clock off
12	clk_aud2_inv	**f_faud2_ck clock phase invert** 1: Enable phase invert
8	clk_aud2_sel	**f_faud2_ck clock mux select** 0: clkxtal 1: aud2pll_ck_270P9504MHz
7	pdn_aud1	**Turns off f_faud1_ck** 1: Enable clock off
4	clk_aud1_inv	**f_faud1_ck clock phase invert** 1: Enable phase invert
0	clk_aud1_sel	**f_faud1_ck clock mux select** 0: clkxtal 1: aud1pll_ck_294P912MHz

102100A4 CLK_CFG_6_SET SET Control of CLK_CFG_6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_6_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_6_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_6_set	**Sets the correspondent bit of CLG_CFG_SEL_6** 0: Unchange 1: Set 1'b1 to the correspondent bit

102100A8 CLK_CFG_6_CLR CLR Control of CLK_CFG_6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_6_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	clk_cfg_6_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_6_clr	**Clears the correspondent bit of CLG_CFG_SEL_6** 0: Unchange 1: Set 1'b0 to the correspondent bit

102100B0 CLK_CFG_7 Function Clock Selection Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									pdn_asm_h			clk_asm_h_inv			clk_asm_h_sel	
Type									RW			RW			RW	
Reset									0			0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_asm_m			clk_asm_m_inv			clk_asm_m_sel		pdn_asm_l			clk_asm_l_inv			clk_asm_l_sel	
Type	RW			RW			RW		RW			RW			RW	
Reset	0			0			0	0	0			0			0	0

Bit(s)	Name	Description
23	pdn_asm_h	**Turns off hf_fasm_h_ck** 1: Enable clock off
20	clk_asm_h_inv	**hf_fasm_h_ck clock phase invert** 1: Enable phase invert
17:16	clk_asm_h_sel	**hf_fasm_h_ck clock mux select** 0: clkxtal 1: syspll_d5_224MHz 2: univpll2_d2_200MHz 3: univpll2_d4_100MHz
15	pdn_asm_m	**Turns off hf_fasm_m_ck** 1: Enable clock off
12	clk_asm_m_inv	**hf_fasm_m_ck clock phase invert** 1: Enable phase invert
9:8	clk_asm_m_sel	**hf_fasm_m_ck clock mux select** 0: clkxtal 1: syspll_d5_224MHz 2: univpll2_d2_200MHz 3: univpll2_d4_100MHz
7	pdn_asm_l	**Turns off hf_fasm_l_ck** 1: Enable clock off

Bit(s)	Name	Description
4	clk_asm_l_inv	**hf_fasm_l_ck clock phase invert** 1: Enable phase invert
1:0	clk_asm_l_sel	**hf_fasm_l_ck clock mux select** 0: clkxtal 1: syspll_d5_224MHz 2: univpll2_d2_200MHz 3: univpll2_d4_100MHz

102100B4 CLK_CFG_7_SET SET Control of CLK_CFG_7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_7_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_7_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_7_set	**Sets the correspondent bit of CLG_CFG_SEL_7** 0: Unchange 1: Set 1'b1 to the correspondent bit

102100B8 CLK_CFG_7_CLR CLR Control of CLK_CFG_7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_7_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_7_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_7_clr	**Clears the correspondent bit of CLG_CFG_SEL_7** 0: Unchange 1: Set 1'b0 to the correspondent bit

10210100 CLK_CFG_8 Function Clock Selection Register 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			abist_clk_sel													
Type			RW													
Reset			0	0	0	0	0	0								

Bit(s)	Name	Description
13:8	abist_clk_sel	**Selects f_fabist_ck clock mux** Not glitch free 00: Power down 01: AD_MEMPLL2_CKOUT0_PRE_ISO 02: AD_MAIN_DIV2_CK 03: AD_MAIN_DIV3_CK 04: AD_MAIN_DIV5_CK 05: AD_MAIN_DIV7_CK 06: AD_UNIV_DIV2_CK 07: AD_UNIV_DIV3_CK 08: AD_UNIV_DIV5_CK 09: AD_UNIV_DIV7_CK 10: AD_UNIV_DIV80_CK 11: AD_UNIV_48M_CK 12: AD_SGMIIPLL_CK 13: XTAL 14: AD_AUD1PLL_CK 15: AD_AUD2PLL_CK 16: RTC 17: AD_ARMPLL_TOP_TST_CK 18: AD_USB_48M_CK 19: abist_clk01 - AD_MAINPLL_CORE_CK 20: abist_clk02 - AD_TRGPLL_CK 21: abist_clk03 - AD_MEM_25M_CK 22: abist_clk04 - AD_PLLGP_TST_CK 23: abist_clk05 - AD_ETH1PLL_CK 24: abist_clk06 - AD_ETH2PLL_CK 25: abist_clk07 - AD_UNIVPLL_CK 26: abist_clk08 - AD_MEM2MIPI_26M_CK 27: abist_clk09 - AD_MEMPLL_MONCLK 28: abist_clk10 - AD_MEMPLL2_MONCLK 29: abist_clk11 - AD_MEMPLL3_MONCLK 30: abist_clk12 - AD_MEMPLL4_MONCLK 31: abist_clk13 - AD_MEMPLL_REFCLK_BUF 32: abist_clk14 - AD_MEMPLL_FBCLK_BUF 33: abist_clk15 - AD_MEMPLL2_REFCLK_BUF 34: abist_clk16 - AD_MEMPLL2_FBCLK_BUF 35: abist_clk17 - AD_MEMPLL3_REFCLK_BUF 36: abist_clk18 - AD_MEMPLL3_FBCLK_BUF

Bit(s)	Name	Description
		37: abist_clk19 - AD_MEMPLL4_REFCLK_BUF 38: abist_clk20 - AD_MEMPLL4_FBCLK_BUF 39: abist_clk21 - AD_MEMPLL_TSTDIV2_CK 40~63: Reserved

10210104 CLK_CFG_9 Function Clock Selection Register 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											ckgen_clk_sel					
Type											RW					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
21:16	ckgen_clk_sel	**Selects f_fckgen_ck clock mux Not glitch free** 00: Power down 01: hf_fmem_ck 02: hf_fddrphycfg_ck 03: hf_feth_ck 04: f_fpwm_ck 05: hf_f10m_ck 06: hf_fspinfi_infra_bclk_ck 07: hf_fflash_ck 08: f_fuart_ck 09: hf_fspi0_ck 10: hf_fspi1_ck 11: hf_fmsdc50_0_ck 12: hf_fmsdc30_0_ck 13: hf_fmsdc30_1_ck 14: f_fa1sys_hp_ck 15: f_fa2sys_hp_ck 16: hf_fintdir_ck 17: hf_faud_intbus_ck 18: hf_fpmicspi_ck 19: hf_fscp_ck 20: hf_fatb_ck 21: hf_fhif_ck 22: hf_faudio_ck 23: hf_fusb20_ck 24: f_faud1_ck 25: f_faud2_ck 26: hf_firrx_ck 27: hf_firtx_ck

Bit(s)	Name	Description
		28: hf_fasm_l_ck 29: hf_fasm_m_ck 30: hf_fasm_h_ck 31: f_faud26m_ck 32: hf_fpmicspi_ck_scan 33: hf_fsgmii_ref_ck 34: f_fsata_ck 35: f_f75k_ck 36: f_fmsdc_ext_ck 37: hf_fddrphycfg_ck_scan 38: f_frtc_fddrphyperi_ck 39: f_fddrphyperi_ck_scan 40: f_fckrtc_ck_scan 41: f_frtc_ck 42: f_fxtal_ck 43: f_fckbus_ck_scan 44: f_fxtal_ck_cg 45: hd_qaxidcm_ck 46: hf_fspi0_pad_ck 47: hf_fspi1_pad_ck 48: f_fefuse_ck 49: f_fapmixed_ck 50: f_fclkmux_ck 51: f_frtc_apmixed_ck 52: f_fsata_ref_ck 53: f_fpcie_ref_ck 54: f_fssusb_ref_ck 55: f_funivpll3_d16_ck 56: f_fauxadc_ck 57: hf_fap2wbmcu_ck 58: hf_fap2wbhif_ck 59: hf_fsata_mcu_ck 60: hf_fpcie0_mcu_ck 61: hf_fpcie1_mcu_ck 62: hf_fssusb_mcu_ck 63: f_fpcie_2ln_ck

10210108 CLK_CFG_10 Debug Monitor Clock Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					clk_ckmon2_sel											
Type					RW											

Reset					0	0	0	0								

Bit(s)	Name	Description
11:8	clk_ckmon2_sel	**Selects f_fckmon2_ck clock mux** Not glitch free 00: Power down 01: AD_SYS_26M_CK 02: rtc32k_ck_i 03: Reserved 04: Reserved 05: Reserved 06: Reserved 07: clkph_MCLK_o 08: Reserved 09: Reserved 10: Reserved 11: AD_UNIV_178P3M_CK 12: AD_MAIN_H156M_CK 13: Reserved 14: Reserved 15: Reserved

1021010C **CLK_CFG_11** **Debug Monitor Divider Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ckmon2_k1															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Name	Description
15:8	ckmon2_k1	**Frequency = (clk_ckmon2_sel) / (ckmon_k2 + 1)**

10210120 **CLK_AUDDIV_0** **Audio Clock Divider Control Register 0** **11000084**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		apll2_ck_div				apll1_ck_div					i2s3_mck_inv	i2s2_mck_inv	i2s1_mck_inv	i2s0_mck_	apll2_ck_inv	apll1_ck_inv
Type		RW				RW					RW	RW	RW	RW	RW	RW
Reset		0	0	1		0	0	1			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					i2s3_mck_mux_sel	i2s2_mck_mux_sel	i2s1_mck_mux_sel	i2s0_mck_mux_sel	apll2_ck_mux_sel	apll1_ck_mux_sel	i2s3_mck_div_pdn	i2s2_mck_div_pdn	i2s1_mck_div_pdn	i2s0_mck_div_pdn	apll2_ck_div_pdn	apll1_ck_div_pdn
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	1	0	0	0	0	1	0	0

Bit(s)	Name	Description
30:28	apll2_ck_div	Divide value: CR value add 1 (0 = div1, 1 = div2, etc)
26:24	apll1_ck_div	Divide value: CR value add 1 (0 = div1, 1 = div2, etc)
21	i2s3_mck_inv	
20	i2s2_mck_inv	
19	i2s1_mck_inv	
18	i2s0_mck_	
17	apll2_ck_inv	
16	apll1_ck_inv	
11	i2s3_mck_mux_sel	0: AUD1PLL - 294.912MHz 1: AUD2PLL - 270.9504MHz
10	i2s2_mck_mux_sel	0: AUD1PLL - 294.912MHz 1: AUD2PLL - 270.9504MHz
9	i2s1_mck_mux_sel	0: AUD1PLL - 294.912MHz 1: AUD2PLL - 270.9504MHz
8	i2s0_mck_mux_sel	0: AUD1PLL - 294.912MHz 1: AUD2PLL - 270.9504MHz
7	apll2_ck_mux_sel	0: AUD2PLL - 270.9504MHz 1: AUD1PLL - 294.912MHz
6	apll1_ck_mux_sel	0: AUD1PLL - 294.912MHz 1: AUD2PLL - 270.9504MHz
5	i2s3_mck_div_pdn	
4	i2s2_mck_div_pdn	
3	i2s1_mck_div_pdn	
2	i2s0_mck_div_pdn	
1	apll2_ck_div_pdn	
0	apll1_ck_div_pdn	

10210124 CLK_AUDDIV_1 Audio Clock Divider Control Register 1 0B0B0B0B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		i2s3_mck_div								i2s2_mck_div						
Type		RW								RW						
Reset		0	0	0	1	0	1	1		0	0	0	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		i2s1_mck_div								i2s0_mck_div						
Type		RW								RW						
Reset		0	0	0	1	0	1	1		0	0	0	1	0	1	1

Bit(s)	Name	Description
30:24	i2s3_mck_div	Divide value: CR value add 1 (0 = div1, 1 = div2, etc)
22:16	i2s2_mck_div	Divide value: CR value add 1 (0 = div1, 1 = div2, etc)
14:8	i2s1_mck_div	Divide value: CR value add 1 (0 = div1, 1 = div2, etc)
6:0	i2s0_mck_div	Divide value: CR value add 1 (0 = div1, 1 = div2, etc)

10210128 CLK_AUDDIV_2 Audio Clock Divider Control Register 2 05000500

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		a2sys_hp_ck_div													a2sys_hp_ck_inv	a2sys_hp_ck_div_pdn
Type		RW													RW	RW
Reset		0	0	0	0	1	0	1							0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		a1sys_hp_ck_div													a1sys_hp_ck_inv	a1sys_hp_ck_div_pdn
Type		RW													RW	RW
Reset		0	0	0	0	1	0	1							0	0

Bit(s)	Name	Description
30:24	a2sys_hp_ck_div	Divide value: CR value add 1 (0 = div1, 1 = div2, etc)
17	a2sys_hp_ck_inv	
16	a2sys_hp_ck_div_pdn	
14:8	a1sys_hp_ck_div	Divide value: CR value add 1 (0 = div1, 1 = div2, etc)
1	a1sys_hp_ck_inv	
0	a1sys_hp_ck_div_pdn	

10210200 CLK_SCP_CFG_0 SCP Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												sc_armck_off_en				sc_26ck_off_en
Type												RW				RW

Reset												0				0

Bit(s)	Name	Description
4	sc_armck_off_en	0: Disable scpsys clock-off control 1: Enable scpsys clock-off control
0	sc_26ck_off_en	0: Disable scpsys clock-off control 1: Enable scpsys clock-off control

10210204 CLK_SCP_CFG_1 SCP Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**sc_axick_dcm_dis_en**				**sc_axick_26m_sel_en**
Type												RW				RW
Reset												0				0

Bit(s)	Name	Description
4	sc_axick_dcm_dis_en	0: Disable scpsys hf_faxi_ck dcm control 1: Enable scpsys hf_faxi_ck dcm control
0	sc_axick_26m_sel_en	0: Disable scpsys clock-off control 1: Enable scpsys clock-off control

10210210 CLK_MISC_CFG_0 MCU Clock Jitter Measurement Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10210214 CLK_MISC_CFG_1 Frequency Meter Divider Control Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ckgen_k1															
Type	RW															
Reset	1	1	1	1	1	1	1	1								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	arm_k1								abist_k1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	ckgen_k1	**Divider setting of f_fckgen_ck** Frequency = (ckgen_clk_sel) / (ckgen_k1 + 1)
15:8	arm_k1	**Divider setting of hf_farm_ck** Frequency = (arm_clk_sel) / (arm_k1 + 1) 0xFF: Gating
7:0	abist_k1	**Divider setting of f_fabist_ck** Frequency = (abist_clk_sel) / (abist_k1 + 1)

10210218 CLK_MISC_CFG_2 MEM DCM Idle Signal Force Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															fmem_dcm_force_mcusys_idle	fmem_dcm_force_infra_idle
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	fmem_dcm_force_mcusys_idle	0: Does not force idle 1: Force idle to high
0	fmem_dcm_force_infra_idle	0: Does not force idle 1: Force idle to high

10210220 CLK26CALI_0 Frequency Meter Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									rg_abist_clk_en		ckgen_clk_exc	ckgen_tri_cal		clk_exc		abist_tri_cal
Type									RW		RW	RW		RW		RW
Reset									0		0	0		0		0

Bit(s)	Name	Description
7	rg_abist_clk_en	0: Disable frequency meter related clock source 1: Enable frequency meter related clock source
5	ckgen_clk_exc	**Selects measuring clock** 0: Not exchange calculation (measured clock count XTAL) 1: Exchange calculation (XTAL count measured clock)
4	ckgen_tri_cal	**Triggers frequency meter on f_fckgen_ck** Auto-cleared when calibration is done 0: Disable frequency meter calculation 1: Enable frequency meter calculation
2	clk_exc	**Selects measuring clock** 0: Not exchange calculation (measured clock count XTAL) 1: Exchange calculation (XTAL count measured clock)
0	abist_tri_cal	**Triggers frequency meter on f_fabist_ck** Auto-cleared when calibration is done 0: Disable frequency meter calculation 1: Enable frequency meter calculation

10210224 CLK26CALI_1 Frequency Meter Control Register 1 03FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							abist_load_cnt									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	abist_cal_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	abist_load_cnt	
15:0	abist_cal_cnt	**Frequency meter result of f_fabist_ck**

Bit(s)	Name	Description
		Frequency = (XTAL*cal_cnt) / (abist_load_cnt+1)

10210228 CLK26CALI_2 Frequency Meter Control Register 2 03FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ckgen_load_cnt									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ckgen_cal_cnt															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	ckgen_load_cnt	
15:0	ckgen_cal_cnt	**Frequency meter result of f_fckgen_ck** Frequency = (XTAL*cal_cnt) / (ckgen_load_cnt+1)

1021022C CKSTA_REG Function Clock Selection Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																chg_sta
Type																RU
Reset																0

Bit(s)	Name	Description
0	chg_sta	**Clock switces changing in progress** 0: All clock MUXs are stable 1: At least one of the clock MUXs are changing

10210230 TEST_MODE_CFG Test Mode Control Register 00000300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10210308 MBIST_CFG_0 Debug Monitor Selection Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1021030C MBIST_CFG_1 Debug Monitor Selection Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										ckgen_debug_sel						
Type										RW						
Reset										0	0	0				

Bit(s)	Name	Description
6:4	ckgen_debug_sel	**Selects TOPCKGEN debug monitor**

10210310 MBIST_CFG_2 Reset Deglitch Enable Key Register 67D2A357

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10210314 MBIST_CFG_3 Debug Monitor Selection Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10210500 WDT_MODE_DUMMY Dummy register for WDT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10210508 WDT_RESTART_DUMMY Dummy register for WDT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10210518 WDT_SWSYSRST_DUMMY Dummy register for WDT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10210520 WDT_NONRST_REG_DUMMY Dummy register for WDT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10210550 WDT_INTERCORE_SYNC_DUMMY Dummy register for WDT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10210554 **WDT_INTERCORE_SYNC_DUMMY_SET** **Dummy register for WDT** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10210558 **WDT_INTERCORE_SYNC_DUMMY_CLR** **Dummy register for WDT** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1.2 TOP Reset Generate Unit

1.2.1 Introduction

The top reset generator unit (TOPRGU) generates reset signals and distributes to each system. A watchdog timer is also included in this module.

1.2.2 Features

- Hardware reset signals for the whole chip
- Software controllable reset for each system (except for infrastructure and apmixedsys system)
- Watchdog timer
- Reset output signals for companion chips

1.2.3 Block Diagram

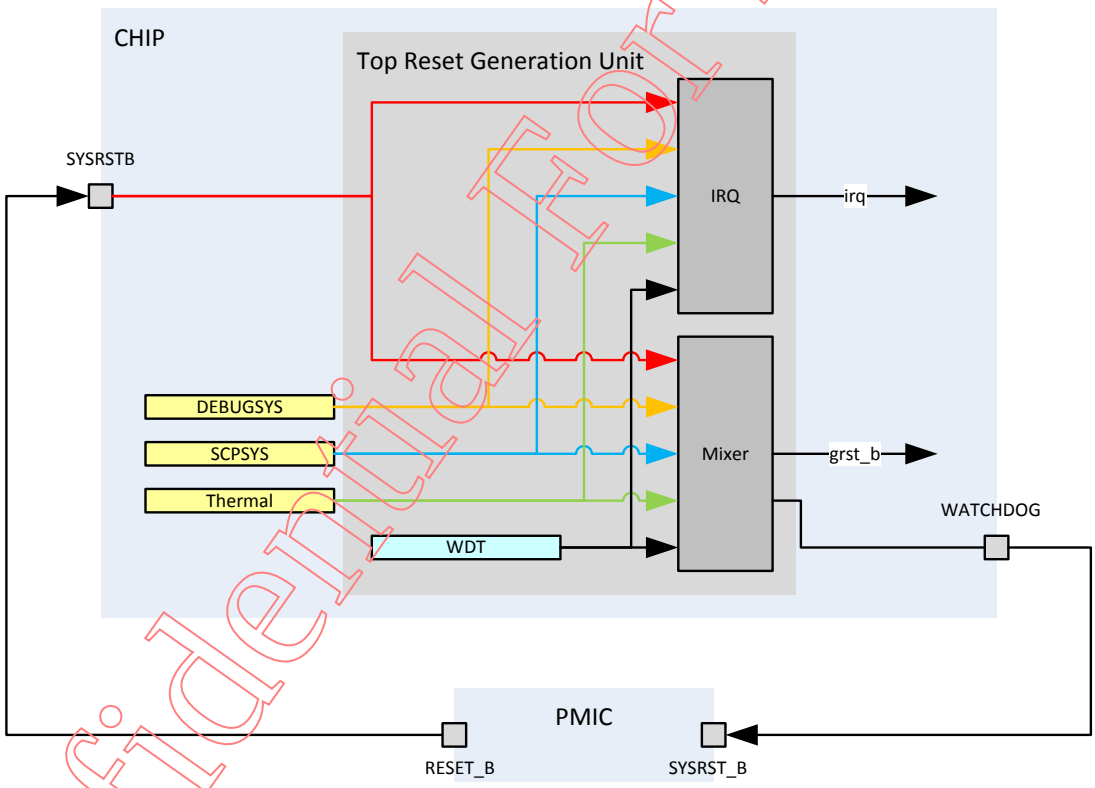


Figure 1-3. Block diagram of top reset generation unit

1.2.4 Register Definition

Module name: TOPRGU Base address: (+10212000h)

Address	Name	Width	Register Function
10212000	TOPRGUWDT_MODE	32	Watchdog Mode Register
10212004	TOPRGUWDT_LENGTH	32	Watchdog Counter Setting Register
10212008	TOPRGUWDT_RESTART	32	Watchdog Counter Restart Register
1021200C	TOPRGUWDT_STA	32	Watchdog Status Register
10212010	TOPRGUWDT_INTERVAL	32	Watchdog Reset Pulse Width Register
10212014	TOPRGUWDT_SWRST	32	Software Watchdog Reset Register
10212018	TOPRGUWDT_SWSYSRST	32	System Software Reset Register
1021201C	TOPRGUWDT_SWSYSRST_PULSE	32	System Software Reset Pulse Enable
10212020	TOPRGUWDT_NONRST_REG	32	Watchdog Non-Reset Register
10212024	TOPRGUWDT_NONRST_REG2	32	Watchdog Non-Reset Register
10212030	TOPRGUWDT_REQ_MODE	32	Reset Request Mode Register
10212034	TOPRGUWDT_REQ_IRQ_EN	32	Reset Request IRQ Enable Register
10212040	TOPRGUWDT_DRAMC_CTL	32	Debug Control Register
10212050	TOPRGUWDT_INTERCORE_SYNC	32	Intercore Sync Register
10212054	TOPRGUWDT_INTERCORE_SYNC_SET	32	Set Control of Intercore Sync Register
10212058	TOPRGUWDT_INTERCORE_SYNC_CLR	32	Clear Control of Intercore Sync Register
10212060	TOPRGUSTRAP_PAR	32	Parallel HW Trap
10212064	TOPRGUSTRAP_SER_31	32	Serial Strap LSB
10212068	TOPRGUSTRAP_SER_63	32	Serial Strap MSB
1021206C	TOPRGUSTRAP_SER_64	32	Serial Strap MSB BIT64
10212500	TOPRGUDEBUG_0_REG	32	Shadow Register of WDT_MODE
10212504	TOPRGUDEBUG_1_REG	32	Shadow Register of WDT_STA
10212508	TOPRGUDEBUG_2_REG	32	Shadow Register of WDT_DEBUG_CTL
1021250C	TOPRGUDEBUG_3_REG	32	Shadow Register of WDT_REQ_MODE
10212510	TOPRGUDEBUG_4_REG	32	Shadow Register of WDT_REG_IRQ_EN

10212000 TOPRGUWDT_MODE Watchdog Mode Register 2200004D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key															
Type	WO															
Reset	0	0	1	0	0	0	1	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								wdt_cnt_reset_sel	ddr_reserve_mode	dual_mode	irq_lvl_en		wdt_irq	exten	extpol	wdt_en

Type								RW	RW	RW	RW		RW	RW	RW	RW
Reset								0	0	1	0		1	1	0	1

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x22 to unlock the write protection of this register**
8	wdt_cnt_reset_sel	**Selects reset source of watchdog timer** 0: Reset only by external reset 1: Reset by TOPRGU
7	ddr_reserve_mode	**Enables ddr_reserve_mode** 0: Disable 1: Enable
6	dual_mode	**Enables dual_mode** Turns on watchdog timer and enables the corresponding irq_en and wdt_en if dual_mode is used 0: Disable 1: Enable
5	irq_lvl_en	**Selects IRQ type** 0: Edge (32K) 1: Level
3	wdt_irq	**Enables watchdog timer IRQ** 0: Trigger reset 1: Trigger IRQ
2	exten	**Enables watchdog output reset signal** 0: Disable 1: Enable
1	extpol	**Watchdog output reset signal polarity** 0: Active low 1: Active high
0	wdt_en	**Enables watchdog timer** 0: Disable 1: Enable

10212004 TOPRGUWDT_LENGTH Watchdog Counter Setting Register 0000FFE8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdt_length											unlock_key				
Type	RW											WO				
Reset	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0

Bit(s)	Name	Description
15:5	wdt_length	**Watchdog time-out counter setting** The counter is restarted with {wdt_length [10:0], 1_1111_1111b}, and therefore the watchdog timer time-out period is a multiple of 512*T32k=15.6ms
4:0	unlock_key	**Write 0x8 to unlock the write protection of this register**

10212008 TOPRGUWDT_RESTART Watchdog Counter Restart Register 00001971

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdt_restart															
Type	WO															
Reset	0	0	0	1	1	0	0	1	0	1	1	1	0	0	1	0	1

Bit(s)	Name	Description
15:0	wdt_restart	**Write 0x1971 to reset the watchdog time-out counter**

1021200C TOPRGUWDT_STA Watchdog Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hw_wdt_rst	sw_wdt_rst	irq_assert	security_rst									debug_rst	thermal_ctl_rst		
Type	RO	RO	RO	RO									RO	RO		
Reset	0	0	0	0									0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															spm_rst	spm_thermal_rst
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
31	hw_wdt_rst	**Indicates hardware watchdog generated reset is asserted**
30	sw_wdt_rst	**Indicates software watchdog generated reset is asserted**
29	irq_assert	**Indicates IRQ is asserted instead of reset**
28	security_rst	**Indicates security reset is asserted**
19	debug_rst	**Indicates debug generated reset is asserted**
18	thermal_ctl_rst	**Indicates thermal reset generated by thermal controller is asserted**
1	spm_rst	**Indicates scpsys time-out generated reset is asserted**
0	spm_thermal_rst	**Indicates thermal reset generated by scpsys reset is asserted**

10212010 TOPRGUWDT_INTERVAL Watchdog Reset Pulse Width Register 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					wdt_reset_interval											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11:0	wdt_reset_interval	**Resets pulse width generated by watchdog**

Bit(s)	Name	Description
		2T 32K duration is required for TD modem. Unit: 1T=1x32kHz

10212014 TOPRGUWDT_SWRST Software Watchdog Reset Register 00001209

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unlock_key															
Type	WO															
Reset	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	1

Bit(s)	Name	Description
15:0	unlock_key	**Write 0x1209 to generate a software watchdog reset**

10212018 TOPRGUWDT_SWSYSRST System Software Reset Register 88008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key															
Type	WO															
Reset	1	0	0	0	1	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				conn_mcu_rst		apmixed_rst	conn_rst	infra_ao_rst		ddrphy_rst					ethdma_rst	infra_rst
Type				RW		RW	RW	RW		RW					RW	RW
Reset				0		0	0	0		0					0	0

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x88 to unlock the write protection of this register**
12	conn_mcu_rst	**Write 1 to reset CONNSYS**
10	apmixed_rst	**Write 1 to reset APMIXEDSYS**
9	conn_rst	**Write 1 to reset CONNSYS**
8	infra_ao_rst	**Write 1 to reset INFRA_AO**
6	ddrphy_rst	**Write 1 to reset DDRPHY and MEMPLL**
1	ethdma_rst	**Write 1 to reset ETHDMASYS**
0	infra_rst	**Write 1 to reset INFRASYS and its related pad macro (NLI, EFUSE)**

1021201C TOPRGUWDT_SWSYSRST_PULSE System Software Reset Pulse Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																
Type																
Reset																

Bit(s)	Name	Description

10212020 TOPRGUWDT_NONRST_REG Watchdog Non-Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10212024 TOPRGUWDT_NONRST_REG2 Watchdog Non-Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10212030 TOPRGUWDT_REQ_MODE Reset Request Mode Register 333C0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key												debug_en	thermal_ctl_en		
Type	WO												RW	RW		
Reset	0	0	1	1	0	0	1	1					1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															spm_en	spm_thermal_en
Type															RW	RW

Reset															1	1

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x33 to unlock the write protection of this register**
19	debug_en	**Enables debugsys reset** 0: Disable 1: Enable
18	thermal_ctl_en	**Enables thermal controller reset** 0: Disable 1: Enable
1	spm_en	**Enables scpsys reset** 0: Disable 1: Enable
0	spm_thermal_en	**Enables scpsys thermal reset** 0: Disable 1: Enable

10212034 TOPRGUWDT_REQ_IRQ_EN Reset Request IRQ Enable Register 443C0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key												debug_irq	thermal_ctl_irq		
Type	WO												RW	RW		
Reset	0	1	0	0	0	1	0	0					1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															scpsys_irq	thermal_irq
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x44 to unlock the write protection of this register**
19	debug_irq	**Triggers IRQ instead of reset when debugsys reset is enabled** 0: Trigger reset 1: Trigger IRQ
18	thermal_ctl_irq	**Triggers IRQ instead of reset when thermal controller reset is enabled** 0: Trigger reset 1: Trigger IRQ
1	scpsys_irq	**Triggers IRQ instead of reset when scpsys reset is enabled** 0: Trigger reset 1: Trigger IRQ
0	thermal_irq	**Triggers IRQ instead of reset when scpsys thermal reset is enabled** 0: Trigger reset 1: Trigger IRQ

10212040 TOPRGUWDT_DRAMC_CTL Debug Control Register 590000F1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key														ddr_sref_sta	ddr_reserve_sta
Type	WO														RU	RO
Reset	0	1	0	1	1	0	0	1							0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						rg_dramc_conf_iso	rg_dramc_iso	rg_dramc_sref	rg_dramc_timeout						rg_mcu_lath_en	rg_ddr_protect_en
Type						RW	RW	RW	RW						RW	RW
Reset						0	0	0	1	1	1	1			0	1

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x59 to unlock the write protection of this register**
17	ddr_sref_sta	**Indicates the current DDR status** 0: Currently not in self-refresh mode 1: Currently in self-refresh mode
16	ddr_reserve_sta	**Indicates ddr_reserve_mode is successful** 0: Failed 1: Succeed
10	rg_dramc_conf_iso	**ddr_reserve_mode related register**
9	rg_dramc_iso	**ddr_reserve_mode related register**
8	rg_dramc_sref	**ddr_reserve_mode related register**
7:4	rg_dramc_timeout	**ddr_reserve_mode related register**
1	rg_mcu_lath_en	
0	rg_ddr_protect_en	**Enables ddr_protect_mode** When ddr_reserve_mode is enabled, ddr_protect_en will be overridden automatically. 0: Disable 1: Enable

10212050 TOPRGUWDT_INTERCORE_SYNC intercore Sync Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_intercore_sync															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_intercore_sync															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rg_intercore_sync	**Register for using intercore sync**

10212054 TOPRGUWDT_INTERCORE_SYNC_SET Set Control of Intercore Sync Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_intercore_sync_set															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_intercore_sync_set															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rg_intercore_sync_set	**Sets 1'b1 to the corresponding bit of rg_intercore_sync**

10212058 TOPRGUWDT_INTERCORE_SYNC_CLR Clear Control of Intercore Sync Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_intercore_sync_clr															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_intercore_sync_clr															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rg_intercore_sync_clr	**Sets 1'b0 to the corresponding bit of rg_intercore_sync**

10212060 TOPRGUSTRAP_PAR Parallel HW Trap 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV								testmode	jtag_mode	boot_seq			ext_bgck	osc_sel	
Type	RO								RO	RO	RO			RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	RESV	**Reserved**
7	testmode	**PAD_TESTMODE Value** 0: Default 1: PAD_TESTMODE is set
6	jtag_mode	**Host JTAG mode** (note*) Chip will have JTAG interface from power-on when the mode is set. User still can change the pinmux after the host CPU is running. 0: Default 1: JTAG enabled
5:3	boot_seq	**Host CPU Boot Sequence.** (Note*) When PAD_TESTMODE is tied to high during power-on period , the chip will enter the debug mode and the field shows the different configurations.

Bit(s)	Name	Description
		DBG_MODE[2:0] -- 000: SERIAL mode (by serial test codes -RBIST FT, RFDIG scan, FT test mode) 001: JTAG mode(CA53 & N9) 010: WIFI RF RXADC 011: WIFI RF RSSI 100: BT AFE DAC mode 101: BT RF mode 110: BT AFE DAC/ADC mode 111: UTIF mode (default: power-on signals) BOOT_SEQ[2:0] 000:SPI-NOR -> SDXC 001: SPI-NAND -> SDXC 010: NAND -> SDXC 011: SDXC -> eMMC
2	ext_bgck	**Bandgap Clock Source** 0: Internal BG Clock 1: External BG Clock
1:0	osc_sel	**XTAL input type** 00: 25MHz DIP XTAL 01: 25MHz SMD XTAL 1x: 40MHz Co-clokc (from 7615)

10212064 TOPRGUSTRAP_SER_31 Serial Strap LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10212068 TOPRGUSTRAP_SER_63 Serial Strap MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1021206C TOPRGUSTRAP_SER_64 Serial Strap MSB BIT64 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10212500 TOPRGUDEBUG_0_REG Shadow Register of WDT_MODE 0000004D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								shadow_wdt_cnt_reset_sel	shadow_ddr_reserve_mode	shadow_dual_mode	shadow_irq_lvl_en	shadow_wdt_restart_dummy_en	shadow_wdt_irq	shadow_exten	shadow_extpol	shadow_wdt_en
Type								RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset								0	0	1	0	0	1	1	0	1

Bit(s)	Name	Description
8	shadow_wdt_cnt_reset_sel	
7	shadow_ddr_reserve_mode	
6	shadow_dual_mode	
5	shadow_irq_lvl_en	
4	shadow_wdt_restart_dummy_en	
3	shadow_wdt_irq	
2	shadow_exten	
1	shadow_extpol	
0	shadow_wdt_en	

10212504 TOPRGUDEBUG_1_REG Shadow Register of WDT_STA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	shadow_hw_wdt_rst	shadow_sw_wdt_rst	shadow_irq_assert	shadow_security_rst									shadow_debug_rst	shadow_thermal_ctl_rst		
Type	RO	RO	RO	RO									RO	RO		
Reset	0	0	0	0									0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															shadow_spm_wdt_rst	shadow_thermal_rst

Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
31	shadow_hw_wdt_rst	
30	shadow_sw_wdt_rst	
29	shadow_irq_assert	
28	shadow_security_rst	
19	shadow_debug_rst	
18	shadow_thermal_ctl_rst	
1	shadow_spm_wdt_rst	
0	shadow_thermal_rst	

10212508 TOPRGUDEBUG_2_REG Shadow Register of WDT_DEBUG_CTL 000000F1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															shadow_ddr_sref_sta	shadow_ddr_reserve_sta
Type															RU	RO
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						rg_shadow_dramc_conf_iso	rg_shadow_dramc_iso	rg_shadow_dramc_sref	rg_shadow_dramc_timeout						rg_shadow_mcu_lath_en	rg_shadow_ddr_protect_en
Type						RO	RO	RO	RO						RO	RO
Reset						0	0	0	1	1	1	1			0	1

Bit(s)	Name	Description
17	shadow_ddr_sref_sta	
16	shadow_ddr_reserve_sta	
10	rg_shadow_dramc_conf_iso	
9	rg_shadow_dramc_iso	
8	rg_shadow_dramc_sref	
7:4	rg_shadow_dramc_timeout	
1	rg_shadow_mcu_lath_en	
0	rg_shadow_ddr_protect_en	

1021250C TOPRGUDEBUG_3_REG Shadow Register of WDT_REQ_MODE 003C0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													shadow_debug_en	shadow_thermal_ctl_en		
Type													RO	RO		
Reset													1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															shadow_scpsys_en	shadow_thermal_en

Type															RO	RO
Reset															1	1

Bit(s)	Name	Description
19	shadow_debug_en	
18	shadow_thermal_ctl_en	
1	shadow_scpsys_en	
0	shadow_thermal_en	

10212510 TOPRGUDEBUG_4_REG Shadow Register of WDT_REG_IRQ_EN 003C0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													shadow_debug_irq	shadow_thermal_ctl_irq		
Type													RO	RO		
Reset													1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															shadow_scpsys_irq	shadow_thermal_irq
Type															RO	RO
Reset															1	1

Bit(s)	Name	Description
19	shadow_debug_irq	
18	shadow_thermal_ctl_irq	
1	shadow_scpsys_irq	
0	shadow_thermal_irq	

1.3 Real-Time Clock

1.3.1 Introduction

Real Time Clock, RTC, consists of pure digital circuit, and is driven by a standard 32.768 KHz crystal clock. With asynchronous circuit facility, it is easy to set the time and the alarm time.

1.3.2 Features

The three operation modes for RTC are Time, Alarm and Timer.

Table 1-3. Operation mode of RTC

Mode	Description
Time	Hexadecimal number representation for second, minutes, hour, day, month and year
Alarm	Alarm function
Timer	Timer for interrupt or external power control

1.3.2.1 Time

The RTC represents time with the hexadecimal format. For “YEAR”, there are 7 bits to represent 00~99. Since 2000 is leap year, only the least two bits of year is needed to decide leap year if 7’h00 represent year 2000.

1.3.2.2 Alarm

The RTC has the capability to setup an alarm interrupt generated at a specified time. A enable register sets(ALMCTL) is used to control alarm on second, minute, hour, day, month, year, or some combination of them.

1.3.2.3 Timer function

The timer supports a resolution of 32.25ms resolution time tick generation. With 16 bits counter, the period of timer can be from 0 ~ 2047s.

1.3.3 Register Definition

Module name: RTC Base address: (+10212800h)

Address	Name	Width	Register Function
10212804	RTC_PWRCHK1	8	RTC power ready check1
10212808	RTC_PWRCHK2	8	RTC power ready check2
1021280C	RTC_KEY	8	RTC security-check protection key
10212810	RTC_PROT1	8	RTC security-check protection write test 1

Address	Name	Width	Register Function
10212814	RTC_PROT2	8	RTC security-check protection write test 2
10212818	RTC_PROT3	8	RTC security-check protection write test 3
1021281C	RTC_PROT4	8	RTC security-check protection write test 4
10212820	RTC_CTL	8	RTC internal control registers
10212824	RTC_LPD_CTL	8	RTC low power detection
10212828	RTC_XOSC_CFG	8	RTC XOSC control registers
1021282C	RTC_DEBNCE	8	RTC de-bounce control
10212830	RTC_PMU_EN	8	RTC PMU_EN control
1021283C	RTC_WAVEOUT	8	RTC waveout for internal test
10212840	RTC_TC_YEA	8	RTC time counter year
10212844	RTC_TC_MON	8	RTC time counter month
10212848	RTC_TC_DOM	8	RTC time counter day of month
1021284C	RTC_TC_DOW	8	RTC time counter day of week
10212850	RTC_TC_HOU	8	RTC time counter hour
10212854	RTC_TC_MIN	8	RTC time counter minute
10212858	RTC_TC_SEC	8	RTC time counter second
10212860	RTC_AL_YEAR	8	RTC alarm year
10212864	RTC_AL_MON	8	RTC alarm month
10212868	RTC_AL_DOM	8	RTC alarm day of month
1021286C	RTC_AL_DOW	8	RTC alarm day of week
10212870	RTC_AL_HOUR	8	RTC alarm hour
10212874	RTC_AL_MIN	8	RTC alarm minute
10212878	RTC_AL_SEC	8	RTC alarm second
1021287C	RTC_AL_CTL	8	RTC alarm control
10212880	RTC_RIP_CTL	8	RTC ripple counter read control
10212884	RTC_RIP_CNTH	8	RTC ripple counter bits [14:8]
10212888	RTC_RIP_CNTL	8	RTC ripple counter bits [7:0]
10212890	RTC_TIMER_CTL	8	RTC timer function control
10212894	RTC_TIMER_CNTH	8	RTC timer count bits [15:8]
10212898	RTC_TIMER_CNTL	8	RTC timer count bits [7:0]
102128C0	RTC_SPARE0	8	RTC spare registers 0
102128C4	RTC_SPARE1	8	RTC spare registers 1
102128C8	RTC_SPARE2	8	RTC spare registers 2
102128CC	RTC_SPARE3	8	RTC spare registers 3
102128D0	RTC_SPARE4	8	RTC spare registers 4
102128D4	RTC_SPARE5	8	RTC spare registers 5
102128D8	RTC_SPARE6	8	RTC spare registers 6
102128DC	RTC_SPARE7	8	RTC spare registers 7
102128E0	RTC_SPARE8	8	RTC spare registers 8
102128E4	RTC_SPARE9	8	RTC spare registers 9
102128E8	RTC_SPARE10	8	RTC spare registers 10
102128EC	RTC_SPARE11	8	RTC spare registers 11
102128F0	RTC_SPARE12	8	RTC spare registers 12
102128F4	RTC_SPARE13	8	RTC spare registers 13
102128F8	RTC_SPARE14	8	RTC spare registers 14

Address	Name	Width	Register Function
102128FC	RTC_SPARE15	8	RTC spare registers 15
10212900	RTC_COREPDN	8	Core domain power down indicator
10212904	MSTIME3	8	Correlator MS counter bit[31:24]
10212908	MSTIME2	8	Correlator MS counter bit[23:16]
1021290C	MSTIME1	8	Correlator MS counter bit[15:8]
10212910	MSTIME0	8	Correlator MS counter bit[7:0]
10212914	SUBMSTIME1	8	Correlator SUBMS counter bit[14:8]
10212918	SUBMSTIME0	8	Correlator SUBMS counter bit[7:0]
1021291C	MSDIFF3	8	MS counter difference bit[31:24]
10212920	MSDIFF2	8	MS counter difference bit[23:16]
10212924	MSDIFF1	8	MS counter difference bit[15:8]
10212928	MSDIFF0	8	MS counter difference bit[7:0]
1021292C	SUBMSDIFF1	8	SUBMS counter difference bit[14:8]
10212930	SUBMSDIFF0	8	SUBMS counter difference bit[7:0]
10212934	MSTIMEMOD	8	Correlator ms time modification control
10212940	RTC_BACKUP00	32	RTC backup memory 00
10212944	RTC_BACKUP01	32	RTC backup memory 01
10212948	RTC_BACKUP02	32	RTC backup memory 02
1021294C	RTC_BACKUP03	32	RTC backup memory 03
10212950	RTC_BACKUP04	32	RTC backup memory 04
10212954	RTC_BACKUP05	32	RTC backup memory 05
10212958	RTC_BACKUP06	32	RTC backup memory 06
1021295C	RTC_BACKUP07	32	RTC backup memory 07
10212960	RTC_BACKUP08	32	RTC backup memory 08
10212964	RTC_BACKUP09	32	RTC backup memory 09
10212968	RTC_BACKUP10	32	RTC backup memory 10
1021296C	RTC_BACKUP11	32	RTC backup memory 11
10212970	RTC_BACKUP12	32	RTC backup memory 12
10212974	RTC_BACKUP13	32	RTC backup memory 13
10212978	RTC_BACKUP14	32	RTC backup memory 14
1021297C	RTC_BACKUP15	32	RTC backup memory 15
10212980	RTC_BACKUP16	32	RTC backup memory 16
10212984	RTC_BACKUP17	32	RTC backup memory 17
10212988	RTC_BACKUP18	32	RTC backup memory 18
1021298C	RTC_BACKUP19	32	RTC backup memory 19
10212990	RTC_BACKUP20	32	RTC backup memory 20
10212994	RTC_BACKUP21	32	RTC backup memory 21
10212998	RTC_BACKUP22	32	RTC backup memory 22
1021299C	RTC_BACKUP23	32	RTC backup memory 23
102129A0	RTC_BACKUP24	32	RTC backup memory 24
102129A4	RTC_BACKUP25	32	RTC backup memory 25
102129A8	RTC_BACKUP26	32	RTC backup memory 26
102129AC	RTC_BACKUP27	32	RTC backup memory 27
102129B0	RTC_BACKUP28	32	RTC backup memory 28
102129B4	RTC_BACKUP29	32	RTC backup memory 29

Address	Name	Width	Register Function
102129B8	RTC_BACKUP30	32	RTC backup memory 30
102129BC	RTC_BACKUP31	32	RTC backup memory 31
102129C0	RTC_BACKUP32	32	RTC backup memory 32
102129C4	RTC_BACKUP33	32	RTC backup memory 33
102129C8	RTC_BACKUP34	32	RTC backup memory 34
102129CC	RTC_BACKUP35	32	RTC backup memory 35

10212804 RTC_PWRCHK1 RTC power ready check1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWRCHK1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	PWRCHK1	RTC power ready check 1 (0xC6)

10212808 RTC_PWRCHK2 RTC power ready check2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWRCHK2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	PWRCHK2	RTC power ready check 2 (0x9A)

1021280C RTC_KEY RTC security-check protection key 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTCKEY							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTCKEY	RTC write protection KEY (0x59)

10212810 RTC_PROT1 RTC security-check protection write test 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTCPROT1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTCPROT1	RTC security-check protection write test 1 (0xA3)

10212814 RTC_PROT2 RTC security-check protection write test 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTCPROT2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTCPROT2	RTC security-check protection write test 2 (0x57)

10212818 RTC_PROT3 RTC security-check protection write test 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTCPROT3							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTCPROT3	RTC security-check protection write test 3 (0x67)

1021281C RTC_PROT4 RTC security-check protection write test 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTCPROT4							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTCPROT4	**RTC security-check protection write test 4 (0xD2)**

10212820 RTC_CTL RTC internal control registers 00000080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DEBNCE_OK	INHIBIT		PROT_PASS	KEY_PASS	PWR_PASS	SIM_RTC	RC_STOP
Type									RU	RU		RU	RU	RU	RW	RW
Reset									1	0		0	0	0	0	0

Bit(s)	Name	Description
7	DEBNCE_OK	**De-bounce period finish indicator** 0: RTC is still de-bouncing. 1: RTC de-bounce ready.
6	INHIBIT	**Inhibit status indicator.** Before reading the registers of YEAR, MONTH, WEEK, DAY, HOUR, MIN, and SEC, read this bit first. If timer is enabled, this bit must also be checked before writing or reading the registers of TIMERCTL, TIMERH, and TIMERL. 0: UP is OK to read/write RTC 1: RTC is updating RTC clock, inhibit UP write timer related registers and read following command YEAR, MONTH, WEEK, DAY, HOUR, MIN, SEC, TIMERCTL, TIMERH, and TIMERL.
4	PROT_PASS	**RTC security-check protection** 0: Fail to pass RTC security-check protection. 1: Pass RTC security check protection.
3	KEY_PASS	**RTC write protection key check** 0: Fail to pass RTC write protection. 1: Pass RTC write protection.
2	PWR_PASS	**RTC power stable check** 0: Fail to pass RTC power stable check. 1: Pass RTC power stable check.
1	SIM_RTC	**For RTC simulation** 0: Normal operation, divided clock = 1Hz 1: Simulation, divided clock = 39.0625Hz
0	RC_STOP	**Stop the ripple counter**

Bit(s)	Name	Description
		0: normal operation. 1: stop and reset ripple counter.

10212824 RTC_LPD_CTL RTC low power detection 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10212828 RTC_XOSC_CFG RTC XOSC control registers 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									OSCPDN		AMPCTL_EN	AMP_GSEL	OSCCALI			
Type									RW		RW	RW	RW			
Reset									0		0	0	0	1	1	1

Bit(s)	Name	Description
7	OSCPDN	**Clock 32K Power down control** 0: Normal operation 1: Power down 32k clock
5	AMPCTL_EN	**Amplitude control function enable**
4	AMP_GSEL	**Amplitude control loop gain select**
3:0	OSCCALI	**Clock 32K PAD drive control** 0000: 0001: 0010: 0011: 0100: 0101: 0110: 0111: 1000: 1001: 1010: 1011: 1100: 1101: 1110: 1111:

Bit(s)	Name	Description

1021282C RTC_DEBNCE RTC de-bounce control 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_DMY					DEBOUNCE		
Type									RW					RW		
Reset									0	0	0	0	0	0	1	1

Bit(s)	Name	Description
7:3	RTC_DMY	**Dummy registers for ECO purpose**
2:0	DEBOUNCE	**RTC de-bounce time setting** This duration prevent abnormal write during losing core power 000: Wait 2^5-1 ~ 2^5 cycle of RTC clock 001: Wait 2^6-4 ~ 2^6 cycle of RTC clock 010: Wait 2^8-2^4~2^8 cycle of RTC clock 011: Wait 2^10-2^6~2^10 cycle of RTC clock 100: Wait 2^12-2^8~2^12 cycle of RTC clock 101: Wait 2^13-2^9~2^13 cycle of RTC clock 110: Wait 2^14-2^10~2^14 cycle of RTC clock 111: Wait 2^15-2^11~2^15 cycle of RTC clock Default value of DEBOUNCE[2:0] before passing RTC security check is 3'b011. This register must be setup after passing RTC security check.

10212830 RTC_PMU_EN RTC PMU_EN control 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TIMER_STA	ALARM_STA	PMU_EN_STATE		PMU_EN_EXT	PMU_EN
Type											W1C	W1C	RO		RO	RW
Reset											0	0	1	1	1	1

Bit(s)	Name	Description
5	TIMER_STA	**Interrupt Status of timer, asserted with timer_hit** Write 1 to clear this bit
4	ALARM_STA	**Interrupt Status of alarm, asserted with alarm_hit** Write 1 to clear this bit
3:2	PMU_EN_STATE	**State Machine controlling PMU Enable signals** 11: PMU is enabled 10: PMU is about to be disabled 00: PMU is disabled
1	PMU_EN_EXT	**PMU Enable signal sent to external power switch** 1: rtc_pmu_en_ext is high

Bit(s)	Name	Description
0	PMU_EN	0: rtc_pmu_en_ext is low **PMU Enable signal sent to PMU** Write 0 to disable PMU_EN, and PMU_EN_EXT will be disabled afterwards Write 1 to enable both PMU_EN and PMU_EN_EXT at the same time 1: rtc_pmu_en is high 0: rtc_pmu_en is low

1021283C RTC_WAVEOUT RTC waveout for internal test 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												WAVEOUT_EN	WAVEOUT_SEL			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	WAVEOUT_EN	**RTC debug clock output enable** 0: waveout = 0 1: Enable waveout signal output.
3:0	WAVEOUT_SEL	**RTC debug clock output select** 0000: ripple counter [14] 0001: ripple counter [13] 0010: ripple counter [12] 0011: ripple counter [11] 0100: ripple counter [10] 0101: ripple counter [9] 0110: ripple counter [8] 0111: ripple counter [7] 1000: ripple counter [6] 1001: ripple counter [5] 1010: ripple counter [4] 1011: ripple counter [3] 1100: ripple counter [2] 1101: ripple counter [1] 1110: ripple counter [0] 1111: 32K clock output

10212840 RTC_TC_YEA RTC time counter year 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										YEAR						
Type										RW						

Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	YEAR	**Year.** Value: 0x0 ~ 0x63 (0 ~ 99)

10212844 RTC_TC_MON RTC time counter month 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MONTH			
Type													RW			
Reset													0	0	0	1

Bit(s)	Name	Description
3:0	MONTH	**Month.** Value: 0x1 ~ 0xc (1 ~ 12)

10212848 RTC_TC_DOM RTC time counter day of month 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												DOM				
Type												RW				
Reset												0	0	0	0	1

Bit(s)	Name	Description
4:0	DOM	**Day of month.** Value: 0x1 ~ 0x1f (1 ~ 31)

1021284C RTC_TC_DOW RTC time counter day of week 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DOW		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	DOW	**Day of week.** Value: 0~6

10212850 RTC_TC_HOU RTC time counter hour 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												HOUR				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	HOUR	**Hour.** Value: 0x0 ~ 0x17 (0 ~ 23)

10212854 RTC_TC_MIN RTC time counter minute 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MIN					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	MIN	**Minute.** Value: 0x0 ~ 0x3b (0 ~ 59)

10212858 RTC_TC_SEC RTC time counter second 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											SEC					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	SEC	**Second.** Value: 0x0 ~ 0x3b (0 ~ 59)

Bit(s)	Name	Description

10212860 RTC_AL_YEAR RTC alarm year 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										AYEAR						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	AYEAR	**Alarm year** Value: 0x0 ~ 0x63 (0 ~ 99)

10212864 RTC_AL_MON RTC alarm month 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													AMONTH			
Type													RW			
Reset													0	0	0	1

Bit(s)	Name	Description
3:0	AMONTH	**Alarm month** Value: 0x1 ~ 0xc (1 ~ 12)

10212868 RTC_AL_DOM RTC alarm day of month 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												ADOM				
Type												RW				
Reset												0	0	0	0	1

Bit(s)	Name	Description
4:0	ADOM	**Alarm day of month** Value: 0x1 ~ 0x1f (1 ~ 31)

1021286C RTC_AL_DOW RTC alarm day of week 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														ADOW		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	ADOW	**Alarm day of week.** Value: 0~6

10212870 RTC_AL_HOUR RTC alarm hour 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												AHOUR				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	AHOUR	**Alarm hour.** Value: 0x0 ~ 0x17 (0 ~ 23)

10212874 RTC_AL_MIN RTC alarm minute 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											AMIN					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	AMIN	**Alarm minute.** Value: 0x0 ~ 0x3b (0 ~ 59)

10212878 RTC_AL_SEC RTC alarm second 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ASEC					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	ASEC	**Alarm second.** Value: 0x0 ~ 0x3b (0 ~ 59)

10212870 RTC_AL_CTL RTC alarm control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ALMYR	ALMMON	ALMDOM	ALMDOW	ALMHR	ALMMIN	ALMSEC	ALMEN
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	ALMYR	**Alarm year enable** 0: Alarm does not compare year. 1: Alarm compares year.
6	ALMMON	**Alarm month enable** 0: Alarm does not compare month. 1: Alarm compares month.
5	ALMDOM	**Alarm day of month enable** 0: Alarm does not compare day of month. 1: Alarm compares day of month.
4	ALMDOW	**Alarm day of week enable** 0: Alarm does not compare day of week. 1: Alarm compares day of week.
3	ALMHR	**Alarm hour enable** 0: Alarm does not compare hour. 1: Alarm compares hour.
2	ALMMIN	**Alarm minute enable** 0: Alarm does not compare minute. 1: Alarm compares minute.
1	ALMSEC	**Alarm second enable** 0: Alarm does not compare second. 1: Alarm compares second.
0	ALMEN	**Alarm enable** 0: Disable alarm. 1: Enable alarm.

10212880 RTC_RIP_CTL RTC ripple counter read control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RIP_RD_OK	RIP_TRG_RD
Type															RU	RW
Reset															0	0

Bit(s)	Name	Description
1	RIP_RD_OK	**Ripple counter read status** 0: RIP_CNT is not ready yet. 1: RIP_CNT is ready for read.
0	RIP_TRG_RD	**Ripple counter read trigger signal** It should be paired with RIP_RD_OK 0: clear RIP_RD_OK status 1: trigger read RTC ripple counter

10212884 RTC_RIP_CNTH RTC ripple counter bits [14:8] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RIP_CNT							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	RIP_CNT	**RTC ripple counter bit[14:8]**

10212888 RTC_RIP_CNTL RTC ripple counter bits [7:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RIP_CNT							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RIP_CNT	**RTC ripple counter bit[7:0]**

10212890 RTC_TIMER_CTL RTC timer function control 000000D0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															TR_INTEN	
Type															RW	
Reset															0	

Bit(s)	Name	Description
1	TR_INTEN	**Enable timer to generate internal interrupt** 0: Disable timer interrupt. 1: Start to count down TIMER_CNT.

10212894 RTC_TIMER_CNTH RTC timer count bits [15:8] 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TIMER_CNT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	TIMER_CNT	**Timer count control bit[15:8]** Count down every 1/32 sec. When TIMER_CNT equals to 0, assert internal interrupt or external pull down pad. Modify TIMER_CNT during TR_INTEN = 0 and TR_EXTEN = 0 in RTC_TIMER_CTL bit 1 and bit 0. If TR_INTEN = 1 or/and TR_EXTEN = 1, TIMER_CNT can read to show the countdown status.

10212898 RTC_TIMER_CNTL RTC timer count bits [7:0] 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TIMER_CNT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	TIMER_CNT	**Timer count control bit[7:0]** Count down every 1/32 sec. When TIMER_CNT equals to 0, assert internal interrupt or external pull down pad. Modify TIMER_CNT during TR_INTEN = 0 and TR_EXTEN = 0 in RTC_TIMER_CTL bit 1 and bit 0.

Bit(s)	Name	Description
		If TR_INTEN = 1 or/and TR_EXTEN = 1, TIMER_CNT can read to show the countdown status.

102128C0 RTC_SPARE0 RTC spare registers 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE0							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE0	RTC spare registers

102128C4 RTC_SPARE1 RTC spare registers 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE1	RTC spare registers

102128C8 RTC_SPARE2 RTC spare registers 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE2	RTC spare registers

102128CC RTC_SPARE3 RTC spare registers 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE3							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE3	RTC spare registers

102128D0 RTC_SPARE4 RTC spare registers 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE4							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE4	RTC spare registers

102128D4 RTC_SPARE5 RTC spare registers 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE5							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE5	RTC spare registers

102128D8 RTC_SPARE6 RTC spare registers 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE6							

Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE6	**RTC spare registers**

102128DC RTC_SPARE7 RTC spare registers 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE7							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE7	**RTC spare registers**

102128E0 RTC_SPARE8 RTC spare registers 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE8							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE8	**RTC spare registers**

102128E4 RTC_SPARE9 RTC spare registers 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE9							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE9	**RTC spare registers**

Bit(s)	Name	Description

102128E8 RTC_SPARE10 RTC spare registers 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE10							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE10	RTC spare registers

102128EC RTC_SPARE11 RTC spare registers 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE11							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE11	RTC spare registers

102128F0 RTC_SPARE12 RTC spare registers 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE12							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE12	RTC spare registers

102128F4 RTC_SPARE13 RTC spare registers 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE13							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE13	**RTC spare registers**

102128F8 RTC_SPARE14 RTC spare registers 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE14							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE14	**RTC spare registers**

102128FC RTC_SPARE15 RTC spare registers 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RTC_SPARE15							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RTC_SPARE15	**RTC spare registers**

10212900 RTC_COREPDN Core domain power down indicator 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															G_ENABLE	CORE_SHU

																TDOWN
Type															RU	RW
Reset															1	0

Bit(s)	Name	Description
1	G_ENABLE	**RTC domain R/W enable indicator** 0: ARM can not access RTC domain. 1: When the protection does not pass, ARM can only write protection pass. When the protection passes, ARM can write all RTC command registers.
0	CORE_SHUTDOWN	**Core domain power down indicator for RTC domain.** 0: disable. 1: Trigger core_shutdown signal for RTC domain. Before core power shut down, write this bit to disable RTC domain interface.

10212904 MSTIME3 Correlator MS counter bit[31:24] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10212908 MSTIME2 Correlator MS counter bit[23:16] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1021290C MSTIME1 Correlator MS counter bit[15:8] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10212910 MSTIME0 Correlator MS counter bit[7:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10212914 SUBMSTIME1 Correlator SUBMS counter bit[14:8] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10212918 SUBMSTIME0 Correlator SUBMS counter bit[7:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1021291C MSDIFF3 MS counter difference bit[31:24] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10212920 MSDIFF2 MS counter difference bit[23:16] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10212924 MSDIFF1 MS counter difference bit[15:8] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10212928 MSDIFF0 MS counter difference bit[7:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																

Reset																

Bit(s)	Name	Description

1021292C SUBMSDIFF1 SUBMS counter difference bit[14:8] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10212930 SUBMSDIFF0 SUBMS counter difference bit[7:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10212934 MSTIMEMOD Correlator ms time modification control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

10212940 RTC_BACKUP00 RTC backup memory 00 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP00															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP00															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP00	RTC backup memory

10212944 RTC_BACKUP01 RTC backup memory 01 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP01															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP01															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP01	RTC backup memory

10212948 RTC_BACKUP02 RTC backup memory 02 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP02															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP02															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP02	RTC backup memory

1021294C RTC_BACKUP03 RTC backup memory 03 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP03															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP03															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP03	**RTC backup memory**

10212950 RTC_BACKUP04 RTC backup memory 04 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP04															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP04															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP04	**RTC backup memory**

10212954 RTC_BACKUP05 RTC backup memory 05 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP05															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP05															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP05	**RTC backup memory**

10212958 RTC_BACKUP06 RTC backup memory 06 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP06															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP06															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP06	**RTC backup memory**

1021295C RTC_BACKUP07 RTC backup memory 07 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RTC_BACKUP07															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP07															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP07	**RTC backup memory**

10212960 RTC_BACKUP08 RTC backup memory 08 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP08															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP08															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP08	**RTC backup memory**

10212964 RTC_BACKUP09 RTC backup memory 09 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP09															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP09															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP09	**RTC backup memory**

10212968 RTC_BACKUP10 RTC backup memory 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP10	**RTC backup memory**

1021296C RTC_BACKUP11 RTC backup memory 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP11	**RTC backup memory**

10212970 RTC_BACKUP12 RTC backup memory 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP12	**RTC backup memory**

10212974 RTC_BACKUP13 RTC backup memory 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP13	**RTC backup memory**

10212978 RTC_BACKUP14 RTC backup memory 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP14															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP14	**RTC backup memory**

1021297C RTC_BACKUP15 RTC backup memory 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP15	**RTC backup memory**

10212980 RTC_BACKUP16 RTC backup memory 16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP16															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP16															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP16	**RTC backup memory**

10212984 RTC_BACKUP17 RTC backup memory 17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP17															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP17															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP17	RTC backup memory

10212988 RTC_BACKUP18 RTC backup memory 18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP18															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP18															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP18	RTC backup memory

1021298C RTC_BACKUP19 RTC backup memory 19 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP19															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP19															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP19	RTC backup memory

10212990 RTC_BACKUP20 RTC backup memory 20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP20															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP20															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP20	RTC backup memory

10212994 RTC_BACKUP21 RTC backup memory 21 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP21															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP21															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP21	**RTC backup memory**

10212998 RTC_BACKUP22 RTC backup memory 22 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP22															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP22															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP22	**RTC backup memory**

1021299C RTC_BACKUP23 RTC backup memory 23 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP23															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP23															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP23	**RTC backup memory**

102129A0 RTC_BACKUP24 RTC backup memory 24 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP24															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP24															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP24	**RTC backup memory**

102129A4 RTC_BACKUP25 RTC backup memory 25 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP25															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP25															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP25	**RTC backup memory**

102129A8 RTC_BACKUP26 RTC backup memory 26 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP26															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP26															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP26	**RTC backup memory**

102129AC RTC_BACKUP27 RTC backup memory 27 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP27															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP27															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP27	**RTC backup memory**

102129B0 RTC_BACKUP28 RTC backup memory 28 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP28															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP28															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP28	**RTC backup memory**

102129B4 RTC_BACKUP29 RTC backup memory 29 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP29															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP29															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP29	**RTC backup memory**

102129B8 RTC_BACKUP30 RTC backup memory 30 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP30															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP30															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP30	**RTC backup memory**

102129BC RTC_BACKUP31 RTC backup memory 31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP31															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP31															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP31	**RTC backup memory**

102129C0 RTC_BACKUP32 RTC backup memory 32 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP32	**RTC backup memory**

102129C4 RTC_BACKUP33 RTC backup memory 33 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP33															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP33															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP33	**RTC backup memory**

102129C8 RTC_BACKUP34 RTC backup memory 34 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP34															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP34															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP34	**RTC backup memory**

102129CC RTC_BACKUP35 RTC backup memory 35 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RTC_BACKUP35															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_BACKUP35															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RTC_BACKUP35	**RTC backup memory**

1.4 External Interrupt Controller

1.4.1 Introduction

The external interrupt controller (EINTC) processes all off-chip interrupt sources and forwards interrupt request signals to MCU/DSP and AP MCU.

1.4.2 Features

EINTC supports up to 224 external interrupt signals and performs the following processes to the interrupt signals coming from external sources:
Polarity inversion
Edge/level trigger selection
De-bounce with a configurable 32kHz clock (optional)

According to the register configuration, the external interrupt source will be forwarded to the Cortex-A7 built-in interrupt controller with different IRQ signals, eint_irq or eint_direct_irq. EINTC generates wake up events to SPM controller.

1.4.3 Register Definition

Module name: ap_cirq_eint Base address: (+10005000h)

Address	Name	Width	Register Function
10005000	EINT_STA0	32	External Interrupt Status Register
10005004	EINT_STA1	32	External Interrupt Status Register
10005008	EINT_STA2	32	External Interrupt Status Register
1000500C	EINT_STA3	32	External Interrupt Status Register
10005010	EINT_STA4	32	External Interrupt Status Register
10005014	EINT_STA5	32	External Interrupt Status Register
10005018	EINT_STA6	32	External Interrupt Status Register
10005040	EINT_ACK0	32	External Interrupt Acknowledge Register
10005044	EINT_ACK1	32	External Interrupt Acknowledge Register
10005048	EINT_ACK2	32	External Interrupt Acknowledge Register
1000504C	EINT_ACK3	32	External Interrupt Acknowledge Register
10005050	EINT_ACK4	32	External Interrupt Acknowledge Register
10005054	EINT_ACK5	32	External Interrupt Acknowledge Register
10005058	EINT_ACK6	32	External Interrupt Acknowledge Register
10005080	EINT_MASK0	32	External Interrupt Mask Register
10005084	EINT_MASK1	32	External Interrupt Mask Register
10005088	EINT_MASK2	32	External Interrupt Mask Register
1000508C	EINT_MASK3	32	External Interrupt Mask Register
10005090	EINT_MASK4	32	External Interrupt Mask Register
10005094	EINT_MASK5	32	External Interrupt Mask Register
10005098	EINT_MASK6	32	External Interrupt Mask Register
100050C0	EINT_MASK_SET0	32	External Interrupt Mask Set Register
100050C4	EINT_MASK_SET1	32	External Interrupt Mask Set Register

Address	Name	Width	Register Function
100050C8	EINT_MASK_SET2	32	External Interrupt Mask Set Register
100050CC	EINT_MASK_SET3	32	External Interrupt Mask Set Register
100050D0	EINT_MASK_SET4	32	External Interrupt Mask Set Register
100050D4	EINT_MASK_SET5	32	External Interrupt Mask Set Register
100050D8	EINT_MASK_SET6	32	External Interrupt Mask Set Register
10005100	EINT_MASK_CLR0	32	External Interrupt Mask Set Register
10005104	EINT_MASK_CLR1	32	External Interrupt Mask Set Register
10005108	EINT_MASK_CLR2	32	External Interrupt Mask Set Register
1000510C	EINT_MASK_CLR3	32	External Interrupt Mask Set Register
10005110	EINT_MASK_CLR4	32	External Interrupt Mask Set Register
10005114	EINT_MASK_CLR5	32	External Interrupt Mask Set Register
10005118	EINT_MASK_CLR6	32	External Interrupt Mask Set Register
10005140	EINT_SENS0	32	External Interrupt Sensitivity Register
10005144	EINT_SENS1	32	External Interrupt Sensitivity Register
10005148	EINT_SENS2	32	External Interrupt Sensitivity Register
1000514C	EINT_SENS3	32	External Interrupt Sensitivity Register
10005150	EINT_SENS4	32	External Interrupt Sensitivity Register
10005154	EINT_SENS5	32	External Interrupt Sensitivity Register
10005158	EINT_SENS6	32	External Interrupt Sensitivity Register
10005180	EINT_SENS_SET0	32	External Interrupt Sensitivity Set Register
10005184	EINT_SENS_SET1	32	External Interrupt Sensitivity Set Register
10005188	EINT_SENS_SET2	32	External Interrupt Sensitivity Set Register
1000518C	EINT_SENS_SET3	32	External Interrupt Sensitivity Set Register
10005190	EINT_SENS_SET4	32	External Interrupt Sensitivity Set Register
10005194	EINT_SENS_SET5	32	External Interrupt Sensitivity Set Register
10005198	EINT_SENS_SET6	32	External Interrupt Sensitivity Set Register
100051C0	EINT_SENS_CLR0	32	External Interrupt Sensitivity Clear Register
100051C4	EINT_SENS_CLR1	32	External Interrupt Sensitivity Clear Register
100051C8	EINT_SENS_CLR2	32	External Interrupt Sensitivity Clear Register
100051CC	EINT_SENS_CLR3	32	External Interrupt Sensitivity Clear Register
100051D0	EINT_SENS_CLR4	32	External Interrupt Sensitivity Clear Register
100051D4	EINT_SENS_CLR5	32	External Interrupt Sensitivity Clear Register
100051D8	EINT_SENS_CLR6	32	External Interrupt Sensitivity Clear Register
10005200	EINT_SOFT0	32	Software Interrupt Register
10005204	EINT_SOFT1	32	Software Interrupt Register
10005208	EINT_SOFT2	32	Software Interrupt Register
1000520C	EINT_SOFT3	32	Software Interrupt Register
10005210	EINT_SOFT4	32	Software Interrupt Register
10005214	EINT_SOFT5	32	Software Interrupt Register
10005218	EINT_SOFT6	32	Software Interrupt Register

Address	Name	Width	Register Function
10005240	EINT_SOFT_SET0	32	Software Interrupt Set Register
10005244	EINT_SOFT_SET1	32	Software Interrupt Set Register
10005248	EINT_SOFT_SET2	32	Software Interrupt Set Register
1000524C	EINT_SOFT_SET3	32	Software Interrupt Set Register
10005250	EINT_SOFT_SET4	32	Software Interrupt Set Register
10005254	EINT_SOFT_SET5	32	Software Interrupt Set Register
10005258	EINT_SOFT_SET6	32	Software Interrupt Set Register
10005280	EINT_SOFT_CLR0	32	Software Interrupt Clear Register
10005284	EINT_SOFT_CLR1	32	Software Interrupt Clear Register
10005288	EINT_SOFT_CLR2	32	Software Interrupt Clear Register
1000528C	EINT_SOFT_CLR3	32	Software Interrupt Clear Register
10005290	EINT_SOFT_CLR4	32	Software Interrupt Clear Register
10005294	EINT_SOFT_CLR5	32	Software Interrupt Clear Register
10005298	EINT_SOFT_CLR6	32	Software Interrupt Clear Register
10005300	EINT_POL0	32	External Interrupt Polarity Register
10005304	EINT_POL1	32	External Interrupt Polarity Register
10005308	EINT_POL2	32	External Interrupt Polarity Register
1000530C	EINT_POL3	32	External Interrupt Polarity Register
10005310	EINT_POL4	32	External Interrupt Polarity Register
10005314	EINT_POL5	32	External Interrupt Polarity Register
10005318	EINT_POL6	32	External Interrupt Polarity Register
10005340	EINT_POL_SET0	32	External Interrupt Polarity Set Register
10005344	EINT_POL_SET1	32	External Interrupt Polarity Set Register
10005348	EINT_POL_SET2	32	External Interrupt Polarity Set Register
1000534C	EINT_POL_SET3	32	External Interrupt Polarity Set Register
10005350	EINT_POL_SET4	32	External Interrupt Polarity Set Register
10005354	EINT_POL_SET5	32	External Interrupt Polarity Set Register
10005358	EINT_POL_SET6	32	External Interrupt Polarity Set Register
10005380	EINT_POL_CLR0	32	External Interrupt Polarity Clear Register
10005384	EINT_POL_CLR1	32	External Interrupt Polarity Clear Register
10005388	EINT_POL_CLR2	32	External Interrupt Polarity Clear Register
1000538C	EINT_POL_CLR3	32	External Interrupt Polarity Clear Register
10005390	EINT_POL_CLR4	32	External Interrupt Polarity Clear Register
10005394	EINT_POL_CLR5	32	External Interrupt Polarity Clear Register
10005398	EINT_POL_CLR6	32	External Interrupt Polarity Clear Register
10005400	EINT_D0EN0	32	Domain 0 External Interrupt Enable Control Register
10005404	EINT_D0EN1	32	Domain 0 External Interrupt Enable Control Register
10005408	EINT_D0EN2	32	Domain 0 External Interrupt Enable Control Register
1000540C	EINT_D0EN3	32	Domain 0 External Interrupt Enable Control Register
10005410	EINT_D0EN4	32	Domain 0 External Interrupt Enable Control Register
10005414	EINT_D0EN5	32	Domain 0 External Interrupt Enable Control Register

Address	Name	Width	Register Function
10005418	EINT_DoEN6	32	Domain 0 External Interrupt Enable Control Register
10005500	EINT_DBNC_3_0	32	External Interrupt Debounce Control Register
10005600	EINT_DBNC_SET_3_0	32	External Interrupt Debounce Control Register
10005700	EINT_DBNC_CLR_3_0	32	External Interrupt Debounce Control Register
10005800	DEINT_CON	32	Direct Couple EINT Control Register
10005840	DEINT_SEL_3_0	32	Direct Couple EINT Select Control Register
10005880	DEINT_SEL_SET_3_0	32	Direct Couple EINT Select Control Set Register
100058C0	DEINT_SEL_CLR_3_0	32	Direct Couple EINT Select Control Clear Register
10005900	EINT_EEVT	32	EINT Wakeup Event Status Register
10005A00	EINT_RAW_STA0	32	External Interrupt Raw Status Register
10005A04	EINT_RAW_STA1	32	External Interrupt Raw Status Register
10005A08	EINT_RAW_STA2	32	External Interrupt Raw Status Register
10005A0C	EINT_RAW_STA3	32	External Interrupt Raw Status Register
10005A10	EINT_RAW_STA4	32	External Interrupt Raw Status Register
10005A14	EINT_RAW_STA5	32	External Interrupt Raw Status Register
10005A18	EINT_RAW_STA6	32	External Interrupt Raw Status Register
10005504	EINT_DBNC_7_4	32	External Interrupt Debounce Control Register
10005604	EINT_DBNC_SET_7_4	32	External Interrupt Debounce Control Register
10005704	EINT_DBNC_CLR_7_4	32	External Interrupt Debounce Control Register
10005508	EINT_DBNC_B_8	32	External Interrupt Debounce Control Register
10005608	EINT_DBNC_SET_B_8	32	External Interrupt Debounce Control Register
10005708	EINT_DBNC_CLR_B_8	32	External Interrupt Debounce Control Register
1000550C	EINT_DBNC_F_C	32	External Interrupt Debounce Control Register
1000560C	EINT_DBNC_SET_F_C	32	External Interrupt Debounce Control Register
1000570C	EINT_DBNC_CLR_F_C	32	External Interrupt Debounce Control Register
100055CC	EINT_DBNC_C_F_C	32	External Interrupt Debounce Control Register
100056CC	EINT_DBNC_SET_C_F_C	32	External Interrupt Debounce Control Register
100057CC	EINT_DBNC_CLR_C_F_C	32	External Interrupt Debounce Control Register

10005000 EINT_STA0 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND0															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND0	Each bit read as 1 indicates the corresponding external interrupt is pending

10005004 EINT_STA1 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND1	Each bit read as 1 indicates the corresponding external interrupt is pending

10005008 EINT_STA2 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND2	Each bit read as 1 indicates the corresponding external interrupt is pending

1000500C EINT_STA3 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND3	Each bit read as 1 indicates the corresponding external interrupt is pending

10005010 EINT_STA4 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND4	Each bit read as 1 indicates the corresponding external interrupt is pending

10005014 EINT_STA5 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND5	Each bit read as 1 indicates the corresponding external interrupt is pending

10005018 EINT_STA6 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_PEND6				
Type												RO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_PEND6	Each bit read as 1 indicates the corresponding external interrupt is pending

10005040 EINT_ACK0 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK0	Write 1 to specific bit to acknowledge the corresponding external interrupt.

10005044 EINT_ACK1 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK1	Write 1 to specific bit to acknowledge the corresponding external interrupt.

10005048 EINT_ACK2 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK2	Write 1 to specific bit to acknowledge the corresponding external interrupt.

1000504C EINT_ACK3 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK3	**Write 1 to specific bit to acknowledge the corresponding external interrupt.**

10005050 EINT_ACK4 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK4	**Write 1 to specific bit to acknowledge the corresponding external interrupt.**

10005054 EINT_ACK5 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK5	**Write 1 to specific bit to acknowledge the corresponding external interrupt.**

10005058 EINT_ACK6 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_ACK6				
Type												WO				

Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_ACK6	**Write 1 to specific bit to acknowledge the corresponding external interrupt.**

10005080 EINT_MASK0 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK0	**External interrupt mask value**

10005084 EINT_MASK1 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK1	**External interrupt mask value**

10005088 EINT_MASK2 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK2	External interrupt mask value

1000508C EINT_MASK3 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK3	External interrupt mask value

10005090 EINT_MASK4 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK4															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK4															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK4	External interrupt mask value

10005094 EINT_MASK5 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK5															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK5															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK5	External interrupt mask value

10005098 EINT_MASK6 External Interrupt Mask Register 001FFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_MASK6				

Type												RO				
Reset												1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK6															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
20:0		EINT_MASK6	**External interrupt mask value**

100050C0 EINT_MASK_SET0 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET0	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

100050C4 EINT_MASK_SET1 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET1	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

100050C8 EINT_MASK_SET2 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET2	Write 1 to specific bit to set up the mask of corresponding external interrupt.

100050CC EINT_MASK_SET3 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET3	Write 1 to specific bit to set up the mask of corresponding external interrupt.

100050D0 EINT_MASK_SET4 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET4	Write 1 to specific bit to set up the mask of corresponding external interrupt.

100050D4 EINT_MASK_SET5 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET5	Write 1 to specific bit to set up the mask of corresponding external interrupt.

100050D8 EINT_MASK_SET6 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_MASK_SET6				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_MASK_SET6	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

10005100 EINT_MASK_CLR0 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR0	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

10005104 EINT_MASK_CLR1 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR1	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

10005108 EINT_MASK_CLR2 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR2	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

1000510C EINT_MASK_CLR3 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR3	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

10005110 EINT_MASK_CLR4 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR4	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

10005114 EINT_MASK_CLR5 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR5	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

10005118 EINT_MASK_CLR6 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_MASK_CLR6				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_MASK_CLR6	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

10005140 EINT_SENS0 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS0	**External interrupt sensitivity value**

10005144 EINT_SENS1 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS1	**External interrupt sensitivity value**

10005148 EINT_SENS2 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS2	External interrupt sensitivity value

1000514C EINT_SENS3 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS3	External interrupt sensitivity value

10005150 EINT_SENS4 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS4															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS4															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS4	External interrupt sensitivity value

10005154 EINT_SENS5 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS5															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS5															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS5	External interrupt sensitivity value

10005158 EINT_SENS6 External Interrupt Sensitivity Register 001FFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_SENS6				
Type												RO				
Reset												1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS6															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
20:0		EINT_SENS6	External interrupt sensitivity value

10005180 EINT_SENS_SET0 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET0	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

10005184 EINT_SENS_SET1 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET1	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

10005188 EINT_SENS_SET2 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET2	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

1000518C EINT_SENS_SET3 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET3	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

10005190 EINT_SENS_SET4 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET4	Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.

10005194 EINT_SENS_SET5 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET5	**Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.**

10005198 EINT_SENS_SET6 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_SENS_SET6				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_SENS_SET6	**Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.**

100051C0 EINT_SENS_CLR0 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR0	**Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.**

100051C4 EINT_SENS_CLR1 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR1															
Type	WO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR1	**Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.**

100051C8 EINT_SENS_CLR2 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR2	**Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.**

100051CC EINT_SENS_CLR3 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR3	**Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.**

100051D0 EINT_SENS_CLR4 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR4															

Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR4	**Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.**

100051D4 EINT_SENS_CLR5 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR5	**Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.**

100051D8 EINT_SENS_CLR6 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_SENS_CLR6				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_SENS_CLR6	**Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.**

10005200 EINT_SOFT0 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT0	Software interrupt value

10005204 EINT_SOFT1 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT1	Software interrupt value

10005208 EINT_SOFT2 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT2	Software interrupt value

1000520C EINT_SOFT3 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT3	Software interrupt value

10005210 EINT_SOFT4 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT4															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT4	Software interrupt value

10005214 EINT_SOFT5 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT5	Software interrupt value

10005218 EINT_SOFT6 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_SOFT6				
Type												RO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_SOFT6	Software interrupt value

10005240 EINT_SOFT_SET0 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET0	Write 1 to specific bit to set up the corresponding software interrupt.

10005244 EINT_SOFT_SET1 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET1	Write 1 to specific bit to set up the corresponding software interrupt.

10005248 EINT_SOFT_SET2 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET2	Write 1 to specific bit to set up the corresponding software interrupt.

1000524C EINT_SOFT_SET3 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET3	Write 1 to specific bit to set up the corresponding software interrupt.

10005250 EINT_SOFT_SET4 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET4	**Write 1 to specific bit to set up the corresponding software interrupt.**

10005254 EINT_SOFT_SET5 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET5	**Write 1 to specific bit to set up the corresponding software interrupt.**

10005258 EINT_SOFT_SET6 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_SOFT_SET6				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_SOFT_SET6	**Write 1 to specific bit to set up the corresponding software interrupt.**

10005280 EINT_SOFT_CLR0 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR0	**Write 1 to specific bit to set up the corresponding software interrupt.**

10005284 EINT_SOFT_CLR1 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR1	**Write 1 to specific bit to set up the corresponding software interrupt.**

10005288 EINT_SOFT_CLR2 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR2	**Write 1 to specific bit to set up the corresponding software interrupt.**

1000528C EINT_SOFT_CLR3 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR3	Write 1 to specific bit to set up the corresponding software interrupt.

10005290 EINT_SOFT_CLR4 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR4	Write 1 to specific bit to set up the corresponding software interrupt.

10005294 EINT_SOFT_CLR5 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR5	Write 1 to specific bit to set up the corresponding software interrupt.

10005298 EINT_SOFT_CLR6 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_SOFT_CLR6				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_SOFT_CLR6	Write 1 to specific bit to set up the corresponding software interrupt.

10005300 EINT_POL0 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL0	External interrupt polarity value

10005304 EINT_POL1 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL1	External interrupt polarity value

10005308 EINT_POL2 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL2	External interrupt polarity value

1000530C EINT_POL3 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL3															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL3	External interrupt polarity value

10005310 EINT_POL4 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL4	External interrupt polarity value

10005314 EINT_POL5 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL5	External interrupt polarity value

10005318 EINT_POL6 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_POL6				
Type												RO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_POL6	External interrupt polarity value

10005340 EINT_POL_SET0 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET0	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

10005344 EINT_POL_SET1 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET1	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

10005348 EINT_POL_SET2 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET2	Write 1 to specific bit to set up the polarity of corresponding external interrupt.

1000534C EINT_POL_SET3 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	EINT_POL_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET3	**Write 1 to specific bit to set up the polarity of corresponding external interrupt.**

10005350 EINT_POL_SET4 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET4	**Write 1 to specific bit to set up the polarity of corresponding external interrupt.**

10005354 EINT_POL_SET5 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET5	**Write 1 to specific bit to set up the polarity of corresponding external interrupt.**

10005358 EINT_POL_SET6 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_POL_SET6				
Type												WO				
Reset												0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_POL_SET6	**Write 1 to specific bit to set up the polarity of corresponding external interrupt.**

10005380 EINT_POL_CLR0 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR0	**Write 1 to specific bit to clear the polarity of corresponding external interrupt.**

10005384 EINT_POL_CLR1 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR1	**Write 1 to specific bit to clear the polarity of corresponding external interrupt.**

10005388 EINT_POL_CLR2 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR2															
Type	WO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR2	**Write 1 to specific bit to clear the polarity of corresponding external interrupt.**

1000538C EINT_POL_CLR3 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR3	**Write 1 to specific bit to clear the polarity of corresponding external interrupt.**

10005390 EINT_POL_CLR4 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR4	**Write 1 to specific bit to clear the polarity of corresponding external interrupt.**

10005394 EINT_POL_CLR5 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR5	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

10005398 EINT_POL_CLR6 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_POL_CLR6				
Type												WO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_POL_CLR6	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

10005400 EINT_DOEN0 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DOEN0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DOEN0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_DOEN0	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

10005404 EINT_DOEN1 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DOEN1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DOEN1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_DOEN1	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

10005408 EINT_DOEN2 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DOEN2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DOEN2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_DOEN2	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

1000540C EINT_DOEN3 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DOEN3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DOEN3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_DOEN3	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

10005410 EINT_DOEN4 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DOEN4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DOEN4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_DOEN4	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

10005414 EINT_DOEN5 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DOEN5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DOEN5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_DOEN5	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

10005418 EINT_DOEN6 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_DOEN6				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DOEN6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_DOEN6	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

10005500 EINT_DBNC_3_0 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING3						DBNC_RST3	EN3	DBNC_SETTING2						DBNC_RST2	EN2
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING1						DBNC_RST1	EN1	DBNC_SETTING0						DBNC_RST0	EN0

Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING3	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
25		DBNC_RST3	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN3	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING2	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
17		DBNC_RST2	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN2	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING1	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms

Bit(s)	Mnemonic	Name	Description
			1000: 256ms 1001: 512ms others: 0.5ms
9		DBNC_RST1	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN1	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING0	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
1		DBNC_RST0	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN0	**Enables de-bounce function** 0: Disable 1: Enable

10005600 EINT_DBNC_SET_3_0 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET3						DBNC_RST_SET3	EN_SET3	DBNC_SETTING_SET2						DBNC_RST_SET2	EN_SET2
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET1						DBNC_RST_SET1	EN_SET1	DBNC_SETTING_SET0						DBNC_RST_SET0	EN_SET0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET3	**De-bounce setting** 0000: 0.125ms

Bit(s)	Mnemonic	Name	Description
			0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
25		DBNC_RST_SET3	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET3	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET2	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
17		DBNC_RST_SET2	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_SET2	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_SET1	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
9		DBNC_RST_SET1	**Resets de-bounce counter** 0: Negative

Bit(s)	Mnemonic	Name	Description
			1: Positive
8		EN_SET1	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_SET0	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
1		DBNC_RST_SET0	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_SET0	**Enables de-bounce function** 0: Disable 1: Enable

10005700 EINT_DBNC_CLR_3_0 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR3						DBNC_RST3	EN_CLR3		DBNC_SETTING_CLR_CLR2					DBNC_RST2	EN_CLR2
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR1						DBNC_RST1	EN_CLR1	DBNC_SETTING_CLR_CLR0						DBNC_RST0	EN_CLR0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR3	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms

Bit(s)	Mnemonic	Name	Description
			1000: 256ms 1001: 512ms others: 0.5ms
25		DBNC_RST3	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR3	**Enables de-bounce function** 0: Disable 1: Enable
22:20		DBNC_SETTING_CLR_CLR2	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
17		DBNC_RST2	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR2	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_CLR_CLR1	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
9		DBNC_RST1	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR1	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR0	**De-bounce setting** 0000: 0.125ms

Bit(s)	Mnemonic	Name	Description
			0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
1		DBNC_RST0	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR0	**Enables de-bounce function** 0: Disable 1: Enable

10005800 DEINT_CON Direct Couple EINT Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DEINT_CON3	DEINT_CON2	DEINT_CON1	DEINT_CON0
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3		DEINT_CON3	**Controls direct couple EINT3** 0: Disable 1: Enable
2		DEINT_CON2	**Controls direct couple EINT2** 0: Disable 1: Enable
1		DEINT_CON1	**Controls direct couple EINT1** 0: Disable 1: Enable
0		DEINT_CON0	**Controls direct couple EINT0** 0: Disable 1: Enable

10005840 DEINT_SEL_3_0 Direct Couple EINT Select Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEINT_SEL3								DEINT_SEL2							
Type	RO								RO							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEINT_SEL1								DEINT_SEL0							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		DEINT_SEL3	**Selects direct couple EINT3** #: EINT number
23:16		DEINT_SEL2	**Selects direct couple EINT2** #: EINT number
15:8		DEINT_SEL1	**Selects direct couple EINT1** #: EINT number
7:0		DEINT_SEL0	**Selects direct couple EINT0** #: EINT number

10005880 DEINT_SEL_SET_3_0 Direct Couple EINT Select Control Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEINT_SEL3								DEINT_SEL2							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEINT_SEL1								DEINT_SEL0							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		DEINT_SEL3	**Sets up direct couple EINT3 selection** #: EINT number
23:16		DEINT_SEL2	**Sets up direct couple EINT2 selection** #: EINT number
15:8		DEINT_SEL1	**Sets up direct couple EINT1 selection** #: EINT number
7:0		DEINT_SEL0	**Sets up direct couple EINT0 selection** #: EINT number

100058C0 DEINT_SEL_CLR_3_0 Direct Couple EINT Select Control Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEINT_SEL3								DEINT_SEL2							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEINT_SEL1								DEINT_SEL0							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		DEINT_SEL3	**Clears direct couple EINT3 selection** #: EINT number
23:16		DEINT_SEL2	**Clears direct couple EINT2 selection** #: EINT number
15:8		DEINT_SEL1	**Clears direct couple EINT1 selection** #: EINT number
7:0		DEINT_SEL0	**Clears direct couple EINT0 selection** #: EINT number

10005900 EINT_EEVT EINT Wakeup Event Status Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EINT_EEVT
Type																RO
Reset																1

Bit(s)	Mnemonic	Name	Description
0		EINT_EEVT	**EINT wakeup event status**

10005A00 EINT_RAW_STA0 External Interrupt Raw Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND0	**Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)**

10005A04 EINT_RAW_STA1 External Interrupt Raw Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND1															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND1	Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)

10005A08 EINT_RAW_STA2 External Interrupt Raw Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND2	Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)

10005A0C EINT_RAW_STA3 External Interrupt Raw Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND3	Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)

10005A10 EINT_RAW_STA4 External Interrupt Raw Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND4	Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)

10005A14 EINT_RAW_STA5 External Interrupt Raw Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND5	Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)

10005A18 EINT_RAW_STA6 External Interrupt Raw Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												EINT_RAW_PEND6				
Type												RO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:0		EINT_RAW_PEND6	Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)

10005504 EINT_DBNC_7_4 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING7						DBNC_RST7	EN7	DBNC_SETTING6						DBNC_RST6	EN6
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING5						DBNC_RST5	EN5	DBNC_SETTING4						DBNC_RST4	EN4
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING7	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
25		DBNC_RST7	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN7	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING6	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
17		DBNC_RST6	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN6	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING5	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms

Bit(s)	Mnemonic	Name	Description
			others: 0.5ms
9		DBNC_RST5	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN5	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING4	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
1		DBNC_RST4	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN4	**Enables de-bounce function** 0: Disable 1: Enable

10005604 EINT_DBNC_SET_7_4 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET7						DBNC_RST_SET7	EN_SET7	DBNC_SETTING_SET6						DBNC_RST_SET6	EN_SET6
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET5						DBNC_RST_SET5	EN_SET5	DBNC_SETTING_SET4						DBNC_RST_SET4	EN_SET4
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET7	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms

Bit(s)	Mnemonic	Name	Description
			0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
25		DBNC_RST_SET7	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET7	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET6	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
17		DBNC_RST_SET6	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_SET6	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_SET5	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
9		DBNC_RST_SET5	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_SET5	**Enables de-bounce function**

Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable
7:4		DBNC_SETTING_SET4	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
1		DBNC_RST_SET4	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_SET4	**Enables de-bounce function** 0: Disable 1: Enable

10005704 EINT_DBNC_CLR_7_4 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR7						DBNC_RST_7	EN_CLR7		DBNC_SETTING_CLR_CLR6					DBNC_RST_6	EN_CLR6
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR5						DBNC_RST_5	EN_CLR5	DBNC_SETTING_CLR_CLR4						DBNC_RST_4	EN_CLR4
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR7	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms

Bit(s)	Mnemonic	Name	Description
			others: 0.5ms
25		DBNC_RST7	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR7	**Enables de-bounce function** 0: Disable 1: Enable
22:20		DBNC_SETTING_CLR_CLR6	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
17		DBNC_RST6	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR6	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_CLR_CLR5	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
9		DBNC_RST5	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR5	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR4	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms

Bit(s)	Mnemonic	Name	Description
			0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
1		DBNC_RST4	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR4	**Enables de-bounce function** 0: Disable 1: Enable

10005508 EINT_DBNC_B_8 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING11						DBNC_RST11	EN11	DBNC_SETTING10						DBNC_RST10	EN10
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING9						DBNC_RST9	EN9	DBNC_SETTING8						DBNC_RST8	EN8
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING11	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
25		DBNC_RST11	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN11	**Enables de-bounce function** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
23:20		DBNC_SETTING10	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
17		DBNC_RST10	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN10	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING9	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
9		DBNC_RST9	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN9	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING8	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms

Bit(s)	Mnemonic	Name	Description
			others: 0.5ms
1		DBNC_RST8	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN8	**Enables de-bounce function** 0: Disable 1: Enable

10005608 EINT_DBNC_SET_B_8 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET11						DBNC_RST_SET11	EN_SET11	DBNC_SETTING_SET10						DBNC_RST_SET10	EN_SET10
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET9						DBNC_RST_SET9	EN_SET9	DBNC_SETTING_SET8						DBNC_RST_SET8	EN_SET8
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET11	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
25		DBNC_RST_SET11	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET11	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET10	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms

Bit(s)	Mnemonic	Name	Description
			0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
17		DBNC_RST_SET10	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_SET10	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_SET9	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
9		DBNC_RST_SET9	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_SET9	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_SET8	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
1		DBNC_RST_SET8	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_SET8	**Enables de-bounce function**

Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable

10005708 EINT_DBNC_CLR_B_8 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR11						DBNC_RST11	EN_CLR11		DBNC_SETTING_CLR_CLR10					DBNC_RST10	EN_CLR10
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR9						DBNC_RST9	EN_CLR9	DBNC_SETTING_CLR_CLR8						DBNC_RST8	EN_CLR8
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR11	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
25		DBNC_RST11	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR11	**Enables de-bounce function** 0: Disable 1: Enable
22:20		DBNC_SETTING_CLR_CLR10	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms

Bit(s)	Mnemonic	Name	Description
			others: 0.5ms
17		DBNC_RST10	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR10	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_CLR_CLR9	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
9		DBNC_RST9	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR9	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR8	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
1		DBNC_RST8	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR8	**Enables de-bounce function** 0: Disable 1: Enable

1000550C EINT_DBNC_F_C External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING15						DBNC_RST15	EN15	DBNC_SETTING14						DBNC_RST14	EN14
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING13						DBNC_RST13	EN13	DBNC_SETTING12						DBNC_RST12	EN12
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING15	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
25		DBNC_RST15	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN15	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING14	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
17		DBNC_RST14	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN14	**Enables de-bounce function** 0: Disable 1: Enable

Bit(s)	Mnemonic	Name	Description
15:12		DBNC_SETTING13	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
9		DBNC_RST13	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN13	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING12	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
1		DBNC_RST12	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN12	**Enables de-bounce function** 0: Disable 1: Enable

1000560C EINT_DBNC_SET_F_C External Interrupt Debounce Control Register **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET15						DBNC_RST_SET15	EN_SET15	DBNC_SETTING_SET14						DBNC_RST_SET14	EN_SET14
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	DBNC_SETTING_SET13						DBNC_RST_SET13	EN_SET13	DBNC_SETTING_SET12						DBNC_RST_SET12	EN_SET12
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET15	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
25		DBNC_RST_SET15	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET15	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET14	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
17		DBNC_RST_SET14	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_SET14	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_SET13	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms

Bit(s)	Mnemonic	Name	Description
			0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
9		DBNC_RST_SET13	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_SET13	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_SET12	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
1		DBNC_RST_SET12	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_SET12	**Enables de-bounce function** 0: Disable 1: Enable

1000570C EINT_DBNC_CLR_F_C External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR15						DBNC_RST15	EN_CLR15		DBNC_SETTING_CLR_CLR14					DBNC_RST14	EN_CLR14
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR13						DBNC_RST13	EN_CLR13	DBNC_SETTING_CLR_CLR12						DBNC_RST12	EN_CLR12
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR15	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
25		DBNC_RST15	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR15	**Enables de-bounce function** 0: Disable 1: Enable
22:20		DBNC_SETTING_CLR_CLR14	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
17		DBNC_RST14	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR14	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_CLR_CLR13	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms

Bit(s)	Mnemonic	Name	Description
9		DBNC_RST13	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR13	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR12	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms others: 0.5ms
1		DBNC_RST12	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR12	**Enables de-bounce function** 0: Disable 1: Enable

100055CC EINT_DBNC_C_F_C External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING207						DBNC_RST207	EN207	DBNC_SETTING206						DBNC_RST206	EN206
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING205						DBNC_RST205	EN205	DBNC_SETTING204						DBNC_RST204	EN204
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING207	
25		DBNC_RST207	
24		EN207	
23:20		DBNC_SETTING206	

Bit(s)	Mnemonic	Name	Description
17		DBNC_RST206	
16		EN206	
15:12		DBNC_SETTING205	
9		DBNC_RST205	
8		EN205	
7:4		DBNC_SETTING204	
1		DBNC_RST204	
0		EN204	

100056CC EINT_DBNC_SET_C_FC External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET207						DBNC_RST_SET207	EN_SET207	DBNC_SETTING_SET206						DBNC_RST_SET206	EN_SET206
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET205						DBNC_RST_SET205	EN_SET205	DBNC_SETTING_SET204						DBNC_RST_SET204	EN_SET204
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET207	
25		DBNC_RST_SET207	
24		EN_SET207	
23:20		DBNC_SETTING_SET206	
17		DBNC_RST_SET206	
16		EN_SET206	
15:12		DBNC_SETTING_SET205	

Bit(s)	Mnemonic	Name	Description
9		DBNC_RST_SET205	
8		EN_SET205	
7:4		DBNC_SETTING_SET204	
1		DBNC_RST_SET204	
0		EN_SET204	

100057CC EINT_DBNC_CLR_C_FC External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR207						DBNC_RST207	EN_CLR207		DBNC_SETTING_CLR_CLR206					DBNC_RST206	EN_CLR206
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR205						DBNC_RST205	EN_CLR205	DBNC_SETTING_CLR_CLR204						DBNC_RST204	EN_CLR204
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR207	
25		DBNC_RST207	
24		EN_CLR207	
22:20		DBNC_SETTING_CLR_CLR206	
17		DBNC_RST206	
16		EN_CLR206	
15:12		DBNC_SETTING_CLR_CLR205	
9		DBNC_RST205	
8		EN_CLR205	
7:4		DBNC_SETTING_CLR_CLR204	

Bit(s)	Mnemonic	Name	Description
1		DBNC_RST204	
0		EN_CLR204	

1.5 System Interrupt Controller

1.5.1 Introduction

For processors like CA7 or CA9 which has embedded interrupt controllers (GIC), the part of the MCUSYS will need to keep feeding clock and Fpower to make the interrupt functional. However, due to power/leakage overhead introduced by higher clock ratio and deep submicron processes, reserving an always on (or frequently turned on) domain in MCUSYS has become power ineffective. The system interrupt controller (SYS_CIRQ) is a low power interrupt controller is designed to work outside MCUSYS as a second level interrupt controller. With SYS_CIRQ, MCUSYS can be completely turned off to improve the system power consumption without losing interrupts.

1.5.2 Features

SYS_CIRQ supports up to 219 interrupts which can configure the following attributes individually.

- Polarity inversion
- Edge/level trigger selection

The 219 interrupts will feed through SYS_CIRQ and connect to GIC in MCUSYS. When SYS_CIRQ is enabled, it will record the edge-sensitive interrupts and generate a pulse signal to CPU GIC when the flush command is executed.

1.5.3 Block Diagram

The SYS_CIRQ controller is integrated in between MCUSYS and other interrupt sources as the second level interrupt controller. All interrupts are fed through SYS_CIRQ controller then bypassed to MCUSYS. In normal mode (where MCUSYS GIC is active), SYS_CIRQ is disabled and interrupts will directly issued to MCUSYS. When MCUSYS enters the sleep mode, where GIC is power downed. SYS_CIRQ controller will be enabled and monitor all edge-trigger interrupts (only edge-triggered interrupt will be lost in this scenario). When an edge-trigger interrupt is triggered, it will be recorded in the SYS_CIRQ_STA register and can be restored to GIC by SW context restore or the SYS_CIRQ flush function.

Below figure is the architecture of SYS_CIRQ. SYS_CIRQ_REG stores the mask/sensitivity/polarity attributes of each interrupt signals and SYS_CIRQ_CON is used to mask and detect edge-triggered interrupts.

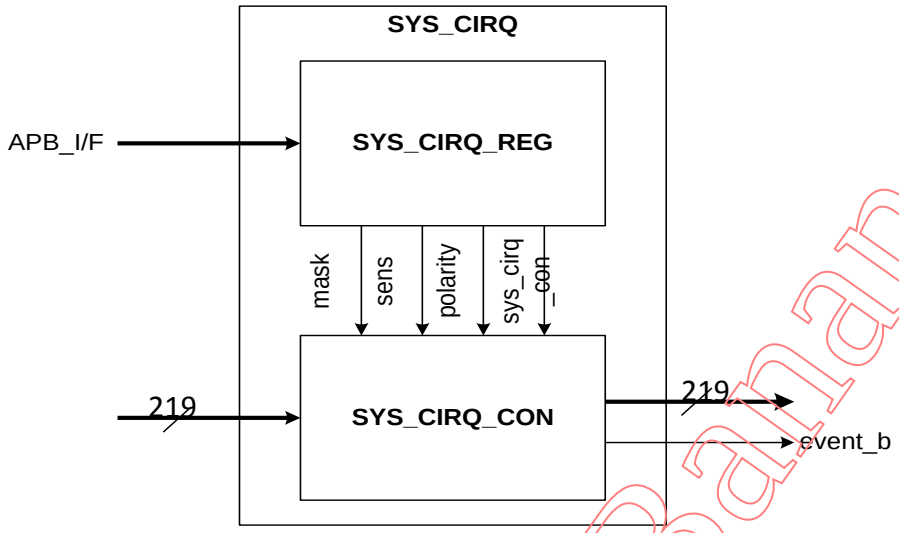


Figure 1-4. Block diagram of system interrupt controller

1.5.4 Register Definition

Module name: sys_cirq Base address: (+10204000h)

Address	Name	Width	Register Function
10204000	CIRQ_STA0	32	System CIRQ status register
10204004	CIRQ_STA1	32	System CIRQ status register
10204008	CIRQ_STA2	32	System CIRQ status register
1020400C	CIRQ_STA3	32	System CIRQ status register
10204010	CIRQ_STA4	32	System CIRQ status register
10204040	CIRQ_ACK0	32	System CIRQ acknowledge register
10204044	CIRQ_ACK1	32	System CIRQ acknowledge register
10204048	CIRQ_ACK2	32	System CIRQ acknowledge register
1020404C	CIRQ_ACK3	32	System CIRQ acknowledge register
10204050	CIRQ_ACK4	32	System CIRQ acknowledge register
10204080	CIRQ_MASK0	32	System CIRQ mask register
10204084	CIRQ_MASK1	32	System CIRQ mask register
10204088	CIRQ_MASK2	32	System CIRQ mask register
1020408C	CIRQ_MASK3	32	System CIRQ mask register
10204090	CIRQ_MASK4	32	System CIRQ mask register
102040C0	CIRQ_MASK_SET0	32	System CIRQ mask set register
102040C4	CIRQ_MASK_SET1	32	System CIRQ mask set register
102040C8	CIRQ_MASK_SET2	32	System CIRQ mask set register
102040CC	CIRQ_MASK_SET3	32	System CIRQ mask set register
102040D0	CIRQ_MASK_SET4	32	System CIRQ mask set register
10204100	CIRQ_MASK_CLR0	32	System CIRQ mask set register
10204104	CIRQ_MASK_CLR1	32	System CIRQ mask set register
10204108	CIRQ_MASK_CLR2	32	System CIRQ mask set register
1020410C	CIRQ_MASK_CLR3	32	System CIRQ mask set register
10204110	CIRQ_MASK_CLR4	32	System CIRQ mask set register

Address	Name	Width	Register Function
10204140	CIRQ_SENS0	32	System CIRQ sensitivity register
10204144	CIRQ_SENS1	32	System CIRQ sensitivity register
10204148	CIRQ_SENS2	32	System CIRQ sensitivity register
1020414C	CIRQ_SENS3	32	System CIRQ sensitivity register
10204150	CIRQ_SENS4	32	System CIRQ sensitivity register
10204180	CIRQ_SENS_SET0	32	System CIRQ sensitivity set register
10204184	CIRQ_SENS_SET1	32	System CIRQ sensitivity set register
10204188	CIRQ_SENS_SET2	32	System CIRQ sensitivity set register
1020418C	CIRQ_SENS_SET3	32	System CIRQ sensitivity set register
10204190	CIRQ_SENS_SET4	32	System CIRQ sensitivity set register
102041C0	CIRQ_SENS_CLR0	32	System CIRQ sensitivity clear register
102041C4	CIRQ_SENS_CLR1	32	System CIRQ sensitivity clear register
102041C8	CIRQ_SENS_CLR2	32	System CIRQ sensitivity clear register
102041CC	CIRQ_SENS_CLR3	32	System CIRQ sensitivity clear register
102041D0	CIRQ_SENS_CLR4	32	System CIRQ sensitivity clear register
10204200	CIRQ_POL0	32	External interrupt polarity register
10204204	CIRQ_POL1	32	External interrupt polarity register
10204208	CIRQ_POL2	32	External interrupt polarity register
1020420C	CIRQ_POL3	32	External interrupt polarity register
10204210	CIRQ_POL4	32	External interrupt polarity register
10204240	CIRQ_POL_SET0	32	External interrupt polarity set register
10204244	CIRQ_POL_SET1	32	External interrupt polarity set register
10204248	CIRQ_POL_SET2	32	External interrupt polarity set register
1020424C	CIRQ_POL_SET3	32	External interrupt polarity set register
10204250	CIRQ_POL_SET4	32	External interrupt polarity set register
10204280	CIRQ_POL_CLR0	32	External interrupt polarity clear register
10204284	CIRQ_POL_CLR1	32	External interrupt polarity clear register
10204288	CIRQ_POL_CLR2	32	External interrupt polarity clear register
1020428C	CIRQ_POL_CLR3	32	External interrupt polarity clear register
10204290	CIRQ_POL_CLR4	32	External interrupt polarity clear register
10204300	CIRQ_CON	32	Sytem CIRQ control register

10204000 CIRQ_STA0 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND0	Each bit read as 1 indicates the corresponding system CIRQ is pending

Bit(s)	Mnemonic	Name	Description

10204004 CIRQ_STA1 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND1	Each bit read as 1 indicates the corresponding system CIRQ is pending

10204008 CIRQ_STA2 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND2	Each bit read as 1 indicates the corresponding system CIRQ is pending

1020400C CIRQ_STA3 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_PEND3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND3	Each bit read as 1 indicates the corresponding system CIRQ is pending

10204010 CIRQ_STA4 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name		CIRQ_PEND4														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_PEND4	Each bit read as 1 indicates the corresponding system CIRQ is pending

10204040 CIRQ_ACK0 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK0	Write 1 to specific bit acknowledges the corresponding system CIRQ

10204044 CIRQ_ACK1 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK1	Write 1 to specific bit acknowledges the corresponding system CIRQ

10204048 CIRQ_ACK2 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK2															
Type	WO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK2	Write 1 to specific bit acknowledges the corresponding system CIRQ

1020404C CIRQ_ACK3 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK3	Write 1 to specific bit acknowledges the corresponding system CIRQ

10204050 CIRQ_ACK4 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_ACK4														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_ACK4	Write 1 to specific bit acknowledges the corresponding system CIRQ

10204080 CIRQ_MASK0 System CIRQ mask register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK0	system CIRQ mask value

10204084 CIRQ_MASK1 System CIRQ mask register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK1	system CIRQ mask value

10204088 CIRQ_MASK2 System CIRQ mask register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK2	system CIRQ mask value

1020408C CIRQ_MASK3 System CIRQ mask register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK3	system CIRQ mask value

10204090 CIRQ_MASK4 System CIRQ mask register 7FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_MASK4														
Type		RO														
Reset		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK4															

Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_MASK4	system CIRQ mask value

102040C0 CIRQ_MASK_SET0 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET0	Write 1 to specific bit sets the mask of corresponding system CIRQ

102040C4 CIRQ_MASK_SET1 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET1	Write 1 to specific bit sets the mask of corresponding system CIRQ

102040C8 CIRQ_MASK_SET2 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET2	Write 1 to specific bit sets the mask of corresponding system CIRQ

Bit(s)	Mnemonic	Name	Description

102040CC CIRQ_MASK_SET3 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET3	Write 1 to specific bit sets the mask of corresponding system CIRQ

102040D0 CIRQ_MASK_SET4 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_MASK_SET4														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_MASK_SET4	Write 1 to specific bit sets the mask of corresponding system CIRQ

10204100 CIRQ_MASK_CLR0 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR0	Write 1 to specific bit clear the mask of corresponding system CIRQ

10204104 CIRQ_MASK_CLR1 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	CIRQ_MASK_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR1	**Write 1 to specific bit clear the mask of corresponding system CIRQ**

10204108 CIRQ_MASK_CLR2 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR2	**Write 1 to specific bit clear the mask of corresponding system CIRQ**

1020410C CIRQ_MASK_CLR3 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR3	**Write 1 to specific bit clear the mask of corresponding system CIRQ**

10204110 CIRQ_MASK_CLR4 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR4															
Type	WO															
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR4															
Type	WO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_MASK_CLR4	**Write 1 to specific bit clear the mask of corresponding system CIRQ**

10204140 CIRQ_SENS0 System CIRQ sensitivity register FFFFFFE3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS0	**system CIRQ sensitivity value**

10204144 CIRQ_SENS1 System CIRQ sensitivity register FEFC7FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS1															
Type	RO															
Reset	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS1															
Type	RO															
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS1	**system CIRQ sensitivity value**

10204148 CIRQ_SENS2 System CIRQ sensitivity register FFEFDFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS2															
Type	RO															
Reset	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS2	**system CIRQ sensitivity value**

1020414C CIRQ_SENS3 System CIRQ sensitivity register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS3	system CIRQ sensitivity value

10204150 CIRQ_SENS4 System CIRQ sensitivity register 7F77FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_SENS4														
Type		RO														
Reset		1	1	1	1	1	1	1	0	1	1	1	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS4															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_SENS4	system CIRQ sensitivity value

10204180 CIRQ_SENS_SET0 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET0	Write 1 to specific bit sets the sensitivity of corresponding system CIRQ

10204184 CIRQ_SENS_SET1 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET1															

Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET1	Write 1 to specific bit sets the sensitivity of corresponding system CIRQ

10204188 CIRQ_SENS_SET2 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET2	Write 1 to specific bit sets the sensitivity of corresponding system CIRQ

1020418C CIRQ_SENS_SET3 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET3	Write 1 to specific bit sets the sensitivity of corresponding system CIRQ

10204190 CIRQ_SENS_SET4 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_SENS_SET4	Write 1 to specific bit sets the sensitivity of corresponding system CIRQ

102041C0 CIRQ_SENS_CLR0 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR0	Write 1 to specific bit clear the sensitivity of corresponding system CIRQ

102041C4 CIRQ_SENS_CLR1 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR1	Write 1 to specific bit clear the sensitivity of corresponding system CIRQ

102041C8 CIRQ_SENS_CLR2 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR2	Write 1 to specific bit clear the sensitivity of corresponding system CIRQ

102041CC CIRQ_SENS_CLR3 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR3	Write 1 to specific bit clear the sensitivity of corresponding system CIRQ

102041D0 CIRQ_SENS_CLR4 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_SENS_CLR4														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_SENS_CLR4	Write 1 to specific bit clear the sensitivity of corresponding system CIRQ

10204200 CIRQ_POL0 External interrupt polarity register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL0	system CIRQ polarity value

10204204 CIRQ_POL1 External interrupt polarity register 00038000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CIRQ_POL1															
Type	RO															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL1	system CIRQ polarity value

10204208 CIRQ_POL2 External interrupt polarity register 00102001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL2															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL2	system CIRQ polarity value

1020420C CIRQ_POL3 External interrupt polarity register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL3	system CIRQ polarity value

10204210 CIRQ_POL4 External interrupt polarity register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_POL4														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_POL4	system CIRQ polarity value

10204240 CIRQ_POL_SET0 External interrupt polarity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET0	**Write 1 to specific bit sets the polarity of corresponding system CIRQ**

10204244 CIRQ_POL_SET1 External interrupt polarity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET1	**Write 1 to specific bit sets the polarity of corresponding system CIRQ**

10204248 CIRQ_POL_SET2 External interrupt polarity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET2	**Write 1 to specific bit sets the polarity of corresponding system CIRQ**

1020424C CIRQ_POL_SET3 External interrupt polarity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET3	**Write 1 to specific bit sets the polarity of corresponding system CIRQ**

10204250 CIRQ_POL_SET4 External interrupt polarity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_POL_SET4														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_POL_SET4	**Write 1 to specific bit sets the polarity of corresponding system CIRQ**

10204280 CIRQ_POL_CLR0 External interrupt polarity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR0	**Write 1 to specific bit clear the polarity of corresponding system CIRQ**

10204284 CIRQ_POL_CLR1 External interrupt polarity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR1															
Type	WO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR1	**Write 1 to specific bit clear the polarity of corresponding system CIRQ**

10204288 CIRQ_POL_CLR2 External interrupt polarity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR2	**Write 1 to specific bit clear the polarity of corresponding system CIRQ**

1020428C CIRQ_POL_CLR3 External interrupt polarity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR3	**Write 1 to specific bit clear the polarity of corresponding system CIRQ**

10204290 CIRQ_POL_CLR4 External interrupt polarity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_POL_CLR4														
Type		WO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_POL_CLR4	**Write 1 to specific bit clear the polarity of corresponding system CIRQ**

10204300 CIRQ_CON Sytem CIRQ control register 80000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_EVENT_B															
Type	RO															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CIRQ_FLUSH	CIRQ_EDGE_ONLY	CIRQ_EN
Type														WO	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
31		CIRQ_EVENT_B	**Indicate sys_cirq_irq_b is triggered**
2		CIRQ_FLUSH	**Flush pending interrupts**
1		CIRQ_EDGE_ONLY	**Set edge-only mode, only edge-triggered interrupt will be recorded**
0		CIRQ_EN	**Enable bit of system CIRQ controller**

1.6 General-Purpose Timer

1.6.1 Introduction

The GPT includes five 32-bit timers and one 64-bit timer. Each timer has four operation modes, which are ONE-SHOT, REPEAT, KEEP-GO and FREERUN, and can operate on one of the two clock sources, RTC clock (32.768kHz) and system clock (13MHz).

1.6.2 Features

The Module contains four operation modes for GPT are ONE-SHOT, REPEAT, KEEP-GO and FREERUN.

Table 1-4. Operation mode of GPT

Mode	Auto Stop	Interrupt	Increases when EN=1 and …	When COUNTn equals COMPAREn	Example: Compare is set to 2 **Bold means interrupt*
ONE-SHOT	Yes	Yes	Stops when COUNTn equals to COMPAREn	EN is reset to 0.	0,1,**2**,2,2,2,2,2,2,2,2,…
REPEAT	No	Yes		Count is reset to 0.	0,1,**2**,0,1,**2**,0,1,**2**,0,1,**2**…
KEEP-GO	No	Yes	Reset to 0 when overflow		0,1,**2**,3,4,5,6,7,8,9,10,…
FREERUN	No	No	Reset to 0 when overflow		0,1,2,3,4,5,6,7,8,9,10,…

Each timer can be programmed to select the clock source, RTC clock (32.76kHz) or system clock (13MHz). After the clock source is determined, the division ratio of the selected clock can be programmed. The division ratio can be fine-granulated as 1, 2, 3, 4 to 13 and coarse-granulated as 16, 32 and 64.

1.6.3 Block Diagram

APXGPT consist of five 32-bits gpts and one 64-bits gpt.

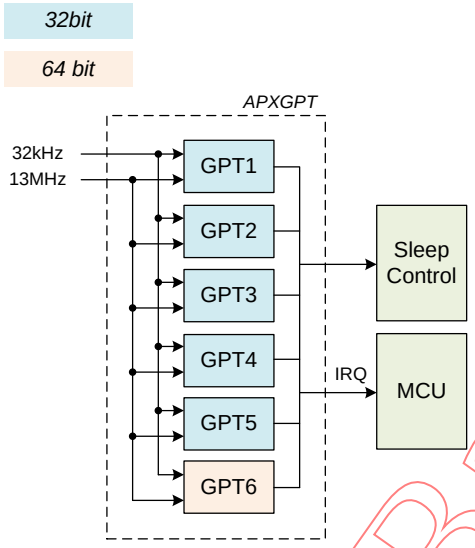


Figure 1-5. APXGPT Block Diagram.

To program and use GPT, please note:
The counter value can be read any time even when the clock source is RTC clock.

- The compare value can be programmed any time.

For the GPT6 64-bit timer, the read operation of the 64-bit timer value will be separated into two APB reads since an APB read is 32-bit wide. To perform the read of 64-bit timer value, the lower word should be read first then the higher word. The read operation of the lower word will freeze the “read value” of the higher word but not freeze the timer counting. This ensures that the separated read operation acquires the correct timer value. If both two tasks, e.g. task A and task B, perform the read of 64-bit timer value, task A will first read the lower word of the value then task B reads the lower word of the value. Either task reads the higher word of the timer value, or the obtained value will be the time when task B reads the lower word of the timer value. To guarantee task A reads the correct 64-bit timer value, some software procedures are required, e.g. semaphore.

1.6.4 Register Definition

Module name: apxgpt Base address: (+10004000h)

Address	*Name*	*Width*	*Register Function*
10004000	GPT_IRQEN	32	GPT IRQ enabling
10004004	GPT_IRQSTA	32	GPT IRQ status
10004008	GPT_IRQACK	32	GPT IRQ acknowledgement
10004010	GPT1_CON	32	GPT1 control
10004014	GPT1_CLK	32	GPT1 clock setting
10004018	GPT1_COUNT	32	GPT1 counter
1000401C	GPT1_COMPARE	32	GPT1 compare value
10004020	GPT2_CON	32	GPT2 control
10004024	GPT2_CLK	32	GPT2 clock setting
10004028	GPT2_COUNT	32	GPT2 counter

Address	Name	Width	Register Function
1000402C	GPT2_COMPARE	32	GPT2 compare value
10004030	GPT3_CON	32	GPT3 control
10004034	GPT3_CLK	32	GPT3 clock setting
10004038	GPT3_COUNT	32	GPT3 counter
1000403C	GPT3_COMPARE	32	GPT3 compare value
10004040	GPT4_CON	32	GPT4 control
10004044	GPT4_CLK	32	GPT4 clock setting
10004048	GPT4_COUNT	32	GPT4 counter
1000404C	GPT4_COMPARE	32	GPT4 compare value
10004050	GPT5_CON	32	GPT5 control
10004054	GPT5_CLK	32	GPT5 clock setting
10004058	GPT5_COUNT	32	GPT5 counter
1000405C	GPT5_COMPARE	32	GPT5 compare value
10004060	GPT6_CON	32	GPT6 control
10004064	GPT6_CLK	32	GPT6 clock setting
10004068	GPT6_COUNTL	32	GPT6 counter L
1000406C	GPT6_COMPAREL	32	GPT6 compare value L
10004078	GPT6_COUNTH	32	GPT6 counter L
1000407C	GPT6_COMPAREH	32	GPT6 compare value H

10004000 GPT_IRQEN GPT IRQ enabling 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IRQEN					
Type											RW					
Reset											0	0	0	0	0	0

[1]	Bit(s) [2]	Name	[3] Description
	5:0	IRQEN	**Enables interrupt of each GPT** 0: Disable associated interrupt of GPT 1: Enable associated interrupt of GPT

10004004 GPT_IRQSTA GPT IRQ status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IRQSTA					

Type											RO					
Reset											0	0	0	0	0	0

[4] Bit(s)	[5] Name	[6] Description
5:0	IRQSTA	**Interrupt status of each GPT** 0: No associated interrupt is generated 1: Associated interrupt is pending and waiting for service

10004008 ***GPT_IRQACK*** ***GPT IRQ acknowledgement*** ***00000000***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**IRQACK**					
Type											WO					
Reset											0	0	0	0	0	0

[7] Bit(s)	[8] Name	[9] Description
5:0	IRQACK	**Interrupt acknowledgement for each GPT** 0: No effect 1: Associated interrupt request is acknowledged and should be relinquished

10004010 ***GPT1_CON*** ***GPT1 control*** ***00000000***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**MODE1**				**CLR1**	**EN1**
Type											RW				WO	RW
Reset											0	0			0	0

[10] Bit(s)	[11] Name	[12] Description
5:4	MODE1	**Operation mode of GPT1** 00: ONE-SHOT mode 01: REPEAT mode 10: KEEP-GO mode 11: FREERUN mode
1	CLR1	**Clears the counter of GPT1 to 0**

[10]	Bit(s)	[11] Name	[12] Description
			0: No effect 1: Clear
0		EN1	**Enables GPT1** 0: Disable 1: Enable

10004014 ***GPT1_CLK*** ***GPT1 clock setting*** ***00000000***

Bit	31	30	29	28	27
Name					
Type					
Reset					
Bit	15	14	13	12	11
Name					
Type					
Reset					

[13]	Bit(s)	[14] Name	[15] Description
[16] [19] [22]	4	[17] CLK1	**Set clock source of GPT1** 0: System clock (13 MHz) 1: RTC clock (32 kHz)
[25] [28] [31] [34] [37] [40] [43] [46] [49] [52] [55] [58] [61] [64] [67] [70] [73]	3:0	[26] CLKDIV1	**Setting of GPT1 input clock frequency divider** 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64
[76]		[77]	[78]

10004018 ***GPT1_COUNT*** ***GPT1 counter*** ***00000000***

Bit	31	30	29	28	27
Name			COUNTER1		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			COUNTER1		
Type			RO		
Reset	0	0	0	0	0

[79]	Bit(s) [80]	Name	[81]	Description
[82]	31:0 [83]	COUNTER1	[84]	**Timer counter of GPT1**
[85]	[86]		[87]	

1000401C GPT1_COMPARE GPT1 compare value 00000000

Bit	31	30	29	28	27
Name			COMPARE1		
Type			RW		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			COMPARE1		
Type			RW		
Reset	0	0	0	0	0

[88]	Bit(s) [89]	Name	[90]	Description
[91]	31:0 [92]	COMPARE1	[93]	**Compare value of GPT1**
[94]	[95]		[96]	

10004020 GPT2_CON GPT2 control 00000000

Bit	31	30	29	28	27
Name					
Type					
Reset					
Bit	15	14	13	12	11
Name					
Type					
Reset					

[97]	Bit(s) [98]	Name	[99]	Description
[100]	5:4 [101]	MODE2	[102]	**Operation mode of GPT2**
[103]	[104]		[105]	00: ONE-SHOT mode
[106]	[107]		[108]	01: REPEAT mode

[97]	Bit(s)	[98]	Name	[99]	Description
[109]		[110]		[111]	10: KEEP-GO mode
[112]		[113]		[114]	11: FREERUN mode
[115]	1	[116]	CLR2	[117]	**Clears the counter of GPT2 to 0**
[118]		[119]		[120]	0: No effect
[121]		[122]		[123]	1: Clear
[124]	0	[125]	EN2	[126]	**Enables GPT2**
[127]		[128]		[129]	0: Disable
[130]		[131]		[132]	1: Enable
[133]		[134]		[135]	

10004024 ***GPT2_CLK*** ***GPT2 clock setting*** ***00000000***

Bit	31	30	29	28	27
Name					
Type					
Reset					
Bit	15	14	13	12	11
Name					
Type					
Reset					

[136]	Bit(s)	[137]	Name	[138]	Description
[139]	4	[140]	CLK2	[141]	**Set clock source of GPT2**
[142]		[143]		[144]	0: System clock (13 MHz)
[145]		[146]		[147]	1: RTC clock (32 kHz)
[148]	3:0	[149]	CLKDIV2	[150]	**Setting of GPT2 input clock frequency divider**
[151]		[152]		[153]	0000: Clock source divided by 1
[154]		[155]		[156]	0001: Clock source divided by 2
[157]		[158]		[159]	0010: Clock source divided by 3
[160]		[161]		[162]	0011: Clock source divided by 4
[163]		[164]		[165]	0100: Clock source divided by 5
[166]		[167]		[168]	0101: Clock source divided by 6
[169]		[170]		[171]	0110: Clock source divided by 7
[172]		[173]		[174]	0111: Clock source divided by 8
[175]		[176]		[177]	1000: Clock source divided by 9
[178]		[179]		[180]	1001: Clock source divided by 10
[181]		[182]		[183]	1010: Clock source divided by 11
[184]		[185]		[186]	1011: Clock source divided by 12
[187]		[188]		[189]	1100: Clock source divided by 13
[190]		[191]		[192]	1101: Clock source divided by 16
[193]		[194]		[195]	1110: Clock source divided by 32
[196]		[197]		[198]	1111: Clock source divided by 64
[199]		[200]		[201]	

10004028 ***GPT2_COUNT*** ***GPT2 counter*** ***00000000***

Bit	31	30	29	28	27
Name			COUNTER2		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			COUNTER2		
Type			RO		
Reset	0	0	0	0	0

[202]	Bit(s)	[203] Name	[204] Description
[205]	31:0	[206] COUNTER2	[207] **Timer counter of GPT2**
[208]		[209]	[210]

1000402C GPT2_COMPARE GPT2 compare value 00000000

Bit	31	30	29	28	27
Name			COMPARE2		
Type			RW		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			COMPARE2		
Type			RW		
Reset	0	0	0	0	0

[211]	Bit(s)	[212] Name	[213] Description
[214]	31:0	[215] COMPARE2	[216] **Compare value of GPT2**
[217]		[218]	[219]

10004030 GPT3_CON GPT3 control 00000000

Bit	31	30	29	28	27
Name					
Type					
Reset					
Bit	15	14	13	12	11
Name					
Type					
Reset					

[220]	Bit(s)	[221] Name	[222] Description
[223]	5:4	[224] MODE3	[225] **Operation mode of GPT3** [228] 00: ONE-SHOT mode [231] 01: REPEAT mode
[226]		[227]	
[229]		[230]	

[220]	Bit(s)	[221]	Name	[222]	Description
[232]		[233]		[234]	10: KEEP-GO mode
[235]		[236]		[237]	11: FREERUN mode
[238]	1	[239]	CLR3	[240]	**Clears the counter of GPT3 to 0**
[241]		[242]		[243]	0: No effect
[244]		[245]		[246]	1: Clear
[247]	0	[248]	EN3	[249]	**Enables GPT3**
[250]		[251]		[252]	0: Disable
[253]		[254]		[255]	1: Enable
[256]		[257]		[258]	

10004034 GPT3_CLK GPT3 clock setting 00000000

Bit	31	30	29	28	27
Name					
Type					
Reset					
Bit	15	14	13	12	11
Name					
Type					
Reset					

[259]	Bit(s)	[260]	Name	[261]	Description
[262]	4	[263]	CLK3	[264]	**Set clock source of GPT3**
[265]		[266]		[267]	0: System clock (13 MHz)
[268]		[269]		[270]	1: RTC clock (32 kHz)
[271]	3:0	[272]	CLKDIV3	[273]	**Setting of GPT3 input clock frequency divider**
[274]		[275]		[276]	0000: Clock source divided by 1
[277]		[278]		[279]	0001: Clock source divided by 2
[280]		[281]		[282]	0010: Clock source divided by 3
[283]		[284]		[285]	0011: Clock source divided by 4
[286]		[287]		[288]	0100: Clock source divided by 5
[289]		[290]		[291]	0101: Clock source divided by 6
[292]		[293]		[294]	0110: Clock source divided by 7
[295]		[296]		[297]	0111: Clock source divided by 8
[298]		[299]		[300]	1000: Clock source divided by 9
[301]		[302]		[303]	1001: Clock source divided by 10
[304]		[305]		[306]	1010: Clock source divided by 11
[307]		[308]		[309]	1011: Clock source divided by 12
[310]		[311]		[312]	1100: Clock source divided by 13
[313]		[314]		[315]	1101: Clock source divided by 16
[316]		[317]		[318]	1110: Clock source divided by 32
[319]		[320]		[321]	1111: Clock source divided by 64
[322]		[323]		[324]	

10004038 GPT3_COUNT GPT3 counter 00000000

Bit	31	30	29	28	27
Name			COUNTER3		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			COUNTER3		
Type			RO		
Reset	0	0	0	0	0

[325]	Bit(s)	[326] Name	[327] Description
[328]	31:0	[329] COUNTER3	[330] **Timer counter of GPT3**
[331]		[332]	[333]

1000403C ***GPT3_COMPARE*** ***GPT3 compare value*** ***00000000***

Bit	31	30	29	28	27
Name			COMPARE3		
Type			RW		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			COMPARE3		
Type			RW		
Reset	0	0	0	0	0

[334]	Bit(s)	[335] Name	[336] Description
[337]	31:0	[338] COMPARE3	[339] **Compare value of GPT3**
[340]		[341]	[342]

10004040 ***GPT4_CON*** ***GPT4 control*** ***00000000***

Bit	31	30	29	28	27
Name					
Type					
Reset					
Bit	15	14	13	12	11
Name					
Type					
Reset					

[343]	Bit(s)	[344] Name	[345] Description
[346]	5:4	[347] MODE4	[348] **Operation mode of GPT4** [351] 00: ONE-SHOT mode [354] 01: REPEAT mode
[349]		[350]	
[352]		[353]	

[343]	Bit(s)	[344]	Name	[345]	Description
[355]		[356]		[357]	10: KEEP-GO mode
[358]		[359]		[360]	11: FREERUN mode
[361]	1	[362]	CLR4	[363]	**Clears the counter of GPT4 to 0**
[364]		[365]		[366]	0: No effect
[367]		[368]		[369]	1: Clear
[370]	0	[371]	EN4	[372]	**Enables GPT4**
[373]		[374]		[375]	0: Disable
[376]		[377]		[378]	1: Enable
[379]		[380]		[381]	

10004044 GPT4_CLK GPT4 clock setting 00000000

Bit	31	30	29	28	27
Name					
Type					
Reset					
Bit	15	14	13	12	11
Name					
Type					
Reset					

[382]	Bit(s)	[383]	Name	[384]	Description
[385]	4	[386]	CLK4	[387]	**Set clock source of GPT4**
[388]		[389]		[390]	0: System clock (13 MHz)
[391]		[392]		[393]	1: RTC clock (32 kHz)
[394]	3:0	[395]	CLKDIV4	[396]	**Setting of GPT4 input clock frequency divider**
[397]		[398]		[399]	0000: Clock source divided by 1
[400]		[401]		[402]	0001: Clock source divided by 2
[403]		[404]		[405]	0010: Clock source divided by 3
[406]		[407]		[408]	0011: Clock source divided by 4
[409]		[410]		[411]	0100: Clock source divided by 5
[412]		[413]		[414]	0101: Clock source divided by 6
[415]		[416]		[417]	0110: Clock source divided by 7
[418]		[419]		[420]	0111: Clock source divided by 8
[421]		[422]		[423]	1000: Clock source divided by 9
[424]		[425]		[426]	1001: Clock source divided by 10
[427]		[428]		[429]	1010: Clock source divided by 11
[430]		[431]		[432]	1011: Clock source divided by 12
[433]		[434]		[435]	1100: Clock source divided by 13
[436]		[437]		[438]	1101: Clock source divided by 16
[439]		[440]		[441]	1110: Clock source divided by 32
[442]		[443]		[444]	1111: Clock source divided by 64
[445]		[446]		[447]	

10004048 GPT4_COUNT GPT4 counter 00000000

Bit	31	30	29	28	27
Name			COUNTER4		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			COUNTER4		
Type			RO		
Reset	0	0	0	0	0

[448]	Bit(s)	[449]	Name	[450]	Description
[451]	31:0	[452]	COUNTER4	[453]	**Timer counter of GPT4**
[454]		[455]		[456]	

1000404C GPT4_COMPARE GPT4 compare value 00000000

Bit	31	30	29	28	27
Name			COMPARE4		
Type			RW		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			COMPARE4		
Type			RW		
Reset	0	0	0	0	0

[457]	Bit(s)	[458]	Name	[459]	Description
[460]	31:0	[461]	COMPARE4	[462]	**Compare value of GPT4**
[463]		[464]		[465]	

10004050 GPT5_CON GPT5 control 00000000

Bit	31	30	29	28	27
Name					
Type					
Reset					
Bit	15	14	13	12	11
Name					
Type					
Reset					

[466]	Bit(s)	[467]	Name	[468]	Description
[469]	5:4	[470]	MODE5	[471]	**Operation mode of GPT5**
[472]		[473]		[474]	00: ONE-SHOT mode
[475]		[476]		[477]	01: REPEAT mode

[466]	Bit(s)	[467]	Name	[468]	Description
[478]		[479]		[480]	10: KEEP-GO mode
[481]		[482]		[483]	11: FREERUN mode
[484]	1	[485]	CLR5	[486]	**Clears the counter of GPT5 to 0**
[487]		[488]		[489]	0: No effect
[490]		[491]		[492]	1: Clear
[493]	0	[494]	EN5	[495]	**Enables GPT5**
[496]		[497]		[498]	0: Disable
[499]		[500]		[501]	1: Enable
[502]		[503]		[504]	

10004054 ***GPT5_CLK*** ***GPT5 clock setting*** ***00000000***

Bit	31	30	29	28	27
Name					
Type					
Reset					
Bit	15	14	13	12	11
Name					
Type					
Reset					

[505]	Bit(s)	[506]	Name	[507]	Description
[508]	4	[509]	CLK5	[510]	**Set clock source of GPT5**
[511]		[512]		[513]	0: System clock (13 MHz)
[514]		[515]		[516]	1: RTC clock (32 kHz)
[517]	3:0	[518]	CLKDIV5	[519]	**Setting of GPT5 input clock frequency divider**
[520]		[521]		[522]	0000: Clock source divided by 1
[523]		[524]		[525]	0001: Clock source divided by 2
[526]		[527]		[528]	0010: Clock source divided by 3
[529]		[530]		[531]	0011: Clock source divided by 4
[532]		[533]		[534]	0100: Clock source divided by 5
[535]		[536]		[537]	0101: Clock source divided by 6
[538]		[539]		[540]	0110: Clock source divided by 7
[541]		[542]		[543]	0111: Clock source divided by 8
[544]		[545]		[546]	1000: Clock source divided by 9
[547]		[548]		[549]	1001: Clock source divided by 10
[550]		[551]		[552]	1010: Clock source divided by 11
[553]		[554]		[555]	1011: Clock source divided by 12
[556]		[557]		[558]	1100: Clock source divided by 13
[559]		[560]		[561]	1101: Clock source divided by 16
[562]		[563]		[564]	1110: Clock source divided by 32
[565]		[566]		[567]	1111: Clock source divided by 64
[568]		[569]		[570]	

10004058 ***GPT5_COUNT*** ***GPT5 counter*** ***00000000***

Bit	31	30	29	28	27
Name			COUNTER5		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			COUNTER5		
Type			RO		
Reset	0	0	0	0	0

[571]	Bit(s)	[572] Name	[573] Description
[574]	31:0	[575] COUNTER5	[576] **Timer counter of GPT5**
[577]		[578]	[579]

1000405C ***GPT5_COMPARE*** ***GPT5 compare value*** ***00000000***

Bit	31	30	29	28	27
Name			COMPARE5		
Type			RW		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			COMPARE5		
Type			RW		
Reset	0	0	0	0	0

[580]	Bit(s)	[581] Name	[582] Description
[583]	31:0	[584] COMPARE5	[585] **Compare value of GPT5**
[586]		[587]	[588]

10004060 ***GPT6_CON*** ***GPT6 control*** ***00000000***

Bit	31	30	29	28	27
Name					
Type					
Reset					
Bit	15	14	13	12	11
Name					
Type					
Reset					

[589]	Bit(s)	[590] Name	[591] Description
[592]	5:4	[593] MODE6	[594] **Operation mode of GPT3**
[595]		[596]	[597] 00: ONE-SHOT mode
[598]		[599]	[600] 01: REPEAT mode

[589]	Bit(s)	[590]	Name	[591]	Description
[601]		[602]		[603]	10: KEEP-GO mode
[604]		[605]		[606]	11: FREERUN mode
[607]	1	[608]	CLR6	[609]	**Clears the counter of GPT3 to 0**
[610]		[611]		[612]	0: No effect
[613]		[614]		[615]	1: Clear
[616]	0	[617]	EN6	[618]	**Enables GPT3**
[619]		[620]		[621]	0: Disable
[622]		[623]		[624]	1: Enable
[625]		[626]		[627]	

10004064 ***GPT6_CLK*** ***GPT6 clock setting*** ***00000000***

Bit	31	30	29	28	27
Name					
Type					
Reset					
Bit	**15**	**14**	**13**	**12**	**11**
Name					
Type					
Reset					

[628]	Bit(s)	[629]	Name	[630]	Description
[631]	4	[632]	CLK6	[633]	**Set clock source of GPT3**
[634]		[635]		[636]	0: System clock (13 MHz)
[637]		[638]		[639]	1: RTC clock (32 kHz)
[640]	3:0	[641]	CLKDIV6	[642]	**Setting of GPT3 input clock frequency divider**
[643]		[644]		[645]	0000: Clock source divided by 1
[646]		[647]		[648]	0001: Clock source divided by 2
[649]		[650]		[651]	0010: Clock source divided by 3
[652]		[653]		[654]	0011: Clock source divided by 4
[655]		[656]		[657]	0100: Clock source divided by 5
[658]		[659]		[660]	0101: Clock source divided by 6
[661]		[662]		[663]	0110: Clock source divided by 7
[664]		[665]		[666]	0111: Clock source divided by 8
[667]		[668]		[669]	1000: Clock source divided by 9
[670]		[671]		[672]	1001: Clock source divided by 10
[673]		[674]		[675]	1010: Clock source divided by 11
[676]		[677]		[678]	1011: Clock source divided by 12
[679]		[680]		[681]	1100: Clock source divided by 13
[682]		[683]		[684]	1101: Clock source divided by 16
[685]		[686]		[687]	1110: Clock source divided by 32
[688]		[689]		[690]	1111: Clock source divided by 64
[691]		[692]		[693]	

10004068 ***GPT6_COUNTL*** ***GPT6 counter L*** ***00000000***

Bit	31	30	29	28	27
Name			COUNTER6L		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			COUNTER6L		
Type			RO		
Reset	0	0	0	0	0

[694]	Bit(s)	[695] Name	[696] Description
[697]	31:0	[698] COUNTER6L	[699] **Lower word of timer count of GPT6** [700] A read operation of GPT6_COUNTL will make GPT6_COUNTH fixed until the next read operation of GPT6_COUNTL

[701] [702] [703]

1000406C GPT6_COMPAREL GPT6 compare value L 00000000

Bit	31	30	29	28	27
Name			COMPARE6L		
Type			RW		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			COMPARE6L		
Type			RW		
Reset	0	0	0	0	0

[704]	Bit(s)	[705] Name	[706] Description
[707]	31:0	[708] COMPARE6L	[709] **Lower word of compare value of GPT6**

[710] [711] [712]

10004078 GPT6_COUNTH GPT6 counter L 00000000

Bit	31	30	29	28	27
Name			COUNTER6H		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			COUNTER6H		
Type			RO		
Reset	0	0	0	0	0

[713]	Bit(s)	[714] Name	[715] Description
[716]	31:0	[717] COUNTER6H	[718] **Higher word of timer count of GPT6**

[713]	Bit(s)	[714]	Name	[715]	Description
[719]		[720]		[721]	

1000407C GPT6_COMPAREH GPT6 compare value H 00000000

Bit	31	30	29	28	27
Name			COMPARE6H		
Type			RW		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			COMPARE6H		
Type			RW		
Reset	0	0	0	0	0

[722]	Bit(s)	[723]	Name	[724]	Description
[725]	31:0	[726]	COMPARE6H	[727]	**Higher word of compare of GPT6**
[728]		[729]		[730]	

1.7 IR-RX

1.7.1 Introduction

The IRRX module can receive the Infra-Red signal and can support NEC protocol, RC5 protocol, RC6 protocol.

This IR receiver can decode various IR transmission protocols. They could be divided into two groups. One is pulse-width coding such as NEC IR transmission protocol, the other is bi-phase coding, for example, RC5, RC6, RCMM. Below figure is an example for pulse-width coding. We can decode the signal by the length of pulse width. Below figure is an example for bi-phase coding. We can decode the signal by a constant period sampling pulse.

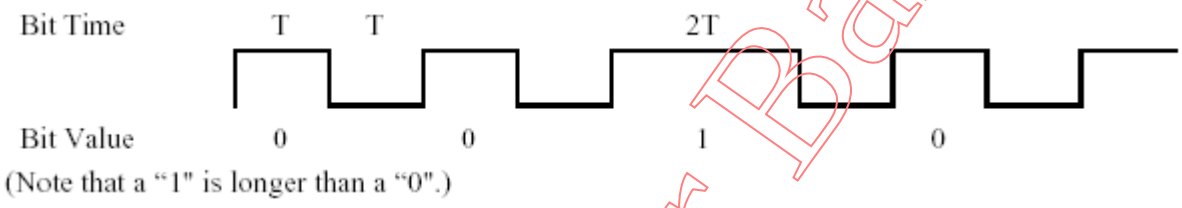


Figure 1-1 Pulse-width coding

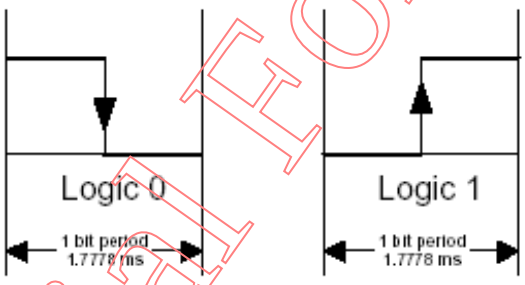


Figure 1-2 Bi-phase coding

1.7.2 Block Diagram

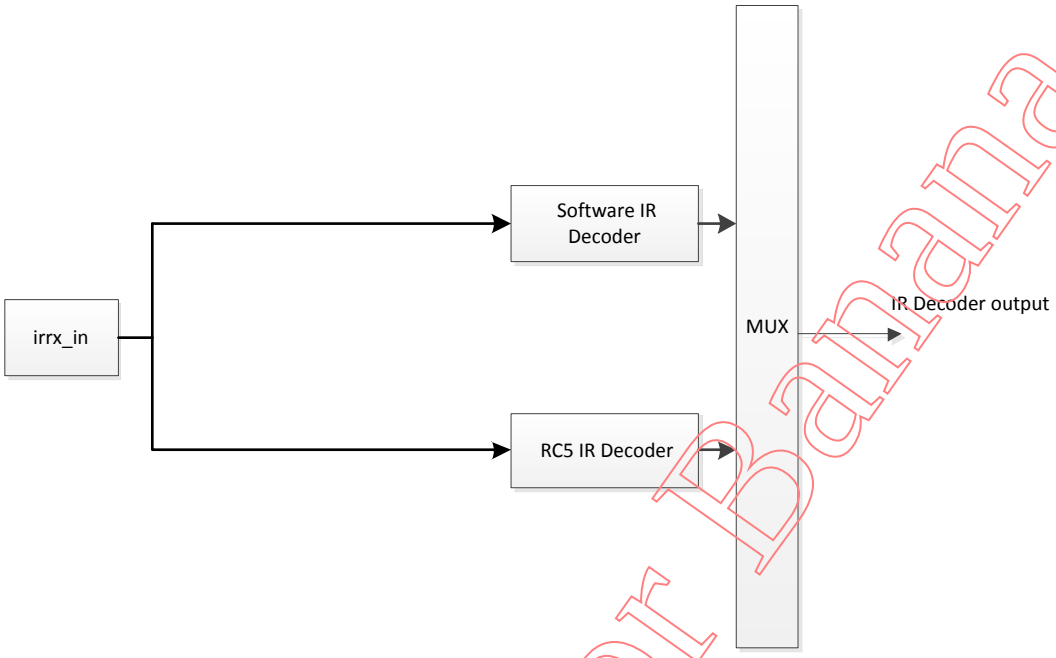


Figure 1-3. Infrared-Receiver Block Diagram

1.7.3 Register Definition

Module name: irrx Base address: (+10009000h)

Address	*Name*	*Width*	*Register Function*
10009000	IRH	32	IR COUNT HIGH REGISTER
10009004	IRM	32	IR COUNT MIDIUM REGISTER
10009008	IRL	32	
1000900C	IRCFGH	32	IR CONFIGURATION HIGH REGISTER
10009010	IRCFGL	32	IR CONFIGURATION LOW
10009014	IRTHD	32	IR THRESHOLD REGISTER
10009018	IRCLR	32	IR CLEAR REGISTER
10009020	IR_INTCLR	32	PDWNC INTERRUPT CLEAR REGISTER
10009024	IRCFGLL	32	IR CONFIGURATION LOW LOW
10009030	CHK_DATA0	32	IR Pulse Width Length Value
10009034	CHK_DATA1	32	IR Pulse Width Length Value
10009038	CHK_DATA2	32	IR Pulse Width Length Value
1000903C	CHK_DATA3	32	IR Pulse Width Length Value
10009040	CHK_DATA4	32	IR Pulse Width Length Value
10009044	CHK_DATA5	32	IR Pulse Width Length Value
10009048	CHK_DATA6	32	IR Pulse Width Length Value
1000904C	CHK_DATA7	32	IR Pulse Width Length Value
10009050	CHK_DATA8	32	IR Pulse Width Length Value
10009054	CHK_DATA9	32	IR Pulse Width Length Value
10009058	CHK_DATA10	32	IR Pulse Width Length Value

Address	Name	Width	Register Function
1000905C	CHK_DATA11	32	IR Pulse Width Length Value
10009060	CHK_DATA12	32	IR Pulse Width Length Value
10009064	CHK_DATA13	32	IR Pulse Width Length Value
10009068	CHK_DATA14	32	IR Pulse Width Length Value
1000906C	CHK_DATA15	32	IR Pulse Width Length Value
10009070	CHK_DATA16	32	IR Pulse Width Length Value

10009000 ***IRH*** ***IR COUNT HIGH REGISTER*** ***00000000***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											BIT_CNT					
Type											RO					
Reset											0	0	0	0	0	0

[731] Bit(s)	[732] Name	[733] Description
5:0	BIT_CNT	Present how many bit is decoded

10009004 ***IRM*** ***IR COUNT MIDIUM REGISTER*** ***00000000***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BIT_REG3								BIT_REG2							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIT_REG1								BIT_REG0							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[734] Bit(s)	[735] Name	[736] Description
31:24	BIT_REG3	Decoded Bit Output Register 3
23:16	BIT_REG2	Decoded Bit Output Register 2
15:8	BIT_REG1	Decoded Bit Output Register 1
7:0	BIT_REG0	Decoded Bit Output Register 0

10009008 ***IRL*** ***00000000***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BIT_REG6							
Type									RO							

Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIT_REG5								BIT_REG4							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[737] Bit(s)	[738] Name	[739] Description
23:16	BIT_REG6	**Decoded Bit Output Register 6**
15:8	BIT_REG5	**Decoded Bit Output Register 5**
7:0	BIT_REG4	**Decoded Bit Output Register 4**

1000900C IRCFGH IR CONFIGURATION HIGH REGISTER 000F0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						IR_FSM			OK_PERIOD							
Type						RO			RW							
Reset						0	0	0	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVED	IGBo	CHK_EN						DISH	DISL	RESERVED	ORDINV	RESERVED		IRINV	IREN
Type	RW	RW	RW						RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0						0	0	0	0	0	0	0	0

[740] Bit(s)	[741] Name	[742] Description
26:24	IR_FSM	**The FSM of IR RX Module**
23:16	OK_PERIOD	**IR end patterns length** When the value of the sampling counter is IREND+1, the IR end signal is active. Then, IR decoder completes this IR command.
15	RESERVED	**RESERVED**
14	IGBo	**Ignore bit o** Ignore o bit count IR pulse in order to reduce noise disturbance. o: Ignore o bit count disable 1: Ignore o bit count enable
13	CHK_EN	**Enable IR pulse width detection**
7	DISH	**Disable high** Disable sampling counter when IR high.
6	DISL	**Disable low** Disable sampling counter when IR low.
5	RESERVED	**RESERVED**
4	ORDINV	**Order inverse. The decoded IR pulse is bit-reversed.** o: Keep the order of decoded bit 1: Inverse the order of decoded bit
3:2	RESERVED	**RESERVED**
1	IRINV	**IR inverse** The IR pulse is inversed before decoded.
0	IREN	**IR Enable** Enable IR hardware receiver function.

10009010 ***IRCFGL*** ***IR CONFIGURATION LOW*** ***00FFFFFF***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									SAPERIOD							
Type									RW							
Reset									1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SAPERIOD															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

[743] Bit(s)	[744] Name	[745] Description
23:0	SAPERIOD	**Sampling period** This field decides the working frequency of the sampling counter. Period is SA_PERIOD[23:0] * PERIOD of IR Clock.

10009014 ***IRTHD*** ***IR THRESHOLD REGISTER*** ***00000600***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DG_SEL					INTCLR_IRCLR	RESERVED						
Type				RW					RW	RW						
Reset				0	0	1	1	0	0	0	0	0	0	0	0	0

[746] Bit(s)	[747] Name	[748] Description
12:8	DG_SEL	**De-glitch Select. When IR signal stays at "High" or "Low" shorter than time defined by DE_SEL, it will be viewed as "glitch" and be ignored.** DG_SEL * IR Clock Period
7	INTCLR_IRCLR	**Interrupt clear reset IR** Activate this bit to clear IR state machine and IRH/IRM/IRL when users clear IR interrupt by IR_INTCLR.
6:0	RESERVED	**RESERVED**

10009018 ***IRCLR*** ***IR CLEAR REGISTER*** ***00000000***

Bit	31	30	29	28	27
Name					
Type					
Reset					
Bit	15	14	13	12	11
Name					
Type					
Reset					

[749] Bit(s)	[750] Name	[751] Description
[752] o	[753] IRCLR	[754] **IR clear** [755] Clear IR state machine and IRH/IRM/IRL. Before IRRX decode input IR signal, CPU has to write this register.

[756] [757] [758]

10009020 ***IR_INTCLR*** ***PDWNC INTERRUPT CLEAR REGISTER*** ***00000000***

Bit	31	30	29	28	27
Name					
Type					
Reset					
Bit	15	14	13	12	11
Name					
Type					
Reset					

[759] Bit(s)	[760] Name	[761] Description
[762] o	[763] IR_INTCLR	[764] **IR receiver interrupt clear bit**

[765] [766] [767]

10009024 ***IRCFGLL*** ***IR CONFIGURATION LOW LOW*** ***00FFFFFF***

Bit	31	30	29	28	27
Name					
Type					
Reset					
Bit	15	14	13	12	11
Name	CHK_PERIOD				
Type	RW				
Reset	1	1	1	1	1

[768]	Bit(s)	[769] Name	[770] Description
[771]	23:0	[772] CHK_PERIOD	[773] **Check IR pulse width sampling period** [774] This field decides the working frequency of the sampling counter for IR pulse width detection. Period is CHK_PERIOD[23:0] * PERIOD of Bus Clock.

[775] [776] [777]

10009030 CHK_DATA0 IR Pulse Width Length Value 00000000

Bit	31	30	29	28	27
Name			CHK_DATA0		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			CHK_DATA0		
Type			RO		
Reset	0	0	0	0	0

[778]	Bit(s)	[779] Name	[780] Description
[781]	31:0	[782] CHK_DATA0	[783] **IR 1-4 pulse width length value, each pulse length is 1byte**

[784] [785] [786]

10009034 CHK_DATA1 IR Pulse Width Length Value 00000000

Bit	31	30	29	28	27
Name			CHK_DATA1		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			CHK_DATA1		
Type			RO		
Reset	0	0	0	0	0

[787]	Bit(s)	[788] Name	[789] Description
[790]	31:0	[791] CHK_DATA1	[792] **IR 5-8 pulse width length value, each pulse length is 1byte**

[793] [794] [795]

10009038 CHK_DATA2 IR Pulse Width Length Value 00000000

Bit	31	30	29	28	27
Name			CHK_DATA2		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			CHK_DATA2		
Type			RO		
Reset	0	0	0	0	0

[796] Bit(s)	[797] Name	[798] Description
[799] 31:0	[800] CHK_DATA2	[801] **IR 9-12 pulse width length value, each pulse length is 1byte**

[802] [803] [804]

1000903C ***CHK_DATA3*** ***IR Pulse Width Length Value*** ***00000000***

Bit	31	30	29	28	27
Name			CHK_DATA3		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			CHK_DATA3		
Type			RO		
Reset	0	0	0	0	0

[805] Bit(s)	[806] Name	[807] Description
[808] 31:0	[809] CHK_DATA3	[810] **IR 13-16 pulse width length value, each pulse length is 1byte**

[811] [812] [813]

10009040 ***CHK_DATA4*** ***IR Pulse Width Length Value*** ***00000000***

Bit	31	30	29	28	27
Name			CHK_DATA4		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			CHK_DATA4		
Type			RO		
Reset	0	0	0	0	0

[814] Bit(s)	[815] Name	[816] Description
[817] 31:0	[818] CHK_DATA4	[819] **IR 17-20 pulse width length value, each pulse length is 1byte**

[820] [821] [822]

10009044 ***CHK_DATA5*** ***IR Pulse Width Length Value*** ***00000000***

Bit	31	30	29	28	27
Name	CHK_DATA5				
Type	RO				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	CHK_DATA5				
Type	RO				
Reset	0	0	0	0	0

[823]	Bit(s)	[824]	Name	[825]	Description
[826]	31:0	[827]	CHK_DATA5	[828]	**IR 21-24 pulse width length value, each pulse length is 1byte**

[829] [830] [831]

10009048 ***CHK_DATA6*** ***IR Pulse Width Length Value*** ***00000000***

Bit	31	30	29	28	27
Name	CHK_DATA6				
Type	RO				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	CHK_DATA6				
Type	RO				
Reset	0	0	0	0	0

[832]	Bit(s)	[833]	Name	[834]	Description
[835]	31:0	[836]	CHK_DATA6	[837]	**IR 25-28 pulse width length value, each pulse length is 1byte**

[838] [839] [840]

1000904C ***CHK_DATA7*** ***IR Pulse Width Length Value*** ***00000000***

Bit	31	30	29	28	27
Name	CHK_DATA7				
Type	RO				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	CHK_DATA7				
Type	RO				
Reset	0	0	0	0	0

[841]	Bit(s)	[842]	Name	[843]	Description
[844]	31:0	[845]	CHK_DATA7	[846]	**IR 29-32 pulse width length value, each pulse length is 1byte**

[841]	Bit(s)	[842]	Name	[843]	Description
[847]		[848]		[849]	

10009050 CHK_DATA8 IR Pulse Width Length Value 00000000

Bit	31	30	29	28	27
Name			CHK_DATA8		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			CHK_DATA8		
Type			RO		
Reset	0	0	0	0	0

[850]	Bit(s)	[851]	Name	[852]	Description
[853]	31:0	[854]	CHK_DATA8	[855]	IR 33-36 pulse width length value, each pulse length is 1byte
[856]		[857]		[858]	

10009054 CHK_DATA9 IR Pulse Width Length Value 00000000

Bit	31	30	29	28	27
Name			CHK_DATA9		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			CHK_DATA9		
Type			RO		
Reset	0	0	0	0	0

[859]	Bit(s)	[860]	Name	[861]	Description
[862]	31:0	[863]	CHK_DATA9	[864]	IR 37-40 pulse width length value, each pulse length is 1byte
[865]		[866]		[867]	

10009058 CHK_DATA10 IR Pulse Width Length Value 00000000

Bit	31	30	29	28	27
Name			CHK_DATA10		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			CHK_DATA10		
Type			RO		
Reset	0	0	0	0	0

[868]	Bit(s)	[869]	Name	[870]	Description
[871]	31:0	[872]	CHK_DATA10	[873]	IR 41-44 pulse width length value, each pulse length is 1byte

[874]	[875]	[876]

1000905C ***CHK_DATA11*** ***IR Pulse Width Length Value*** ***00000000***

Bit	31	30	29	28	27
Name	CHK_DATA11				
Type	RO				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	CHK_DATA11				
Type	RO				
Reset	0	0	0	0	0

[877]	Bit(s)	[878]	Name	[879]	Description
[880]	31:0	[881]	CHK_DATA11	[882]	IR 45-48 pulse width length value, each pulse length is 1byte

[883]	[884]	[885]

10009060 ***CHK_DATA12*** ***IR Pulse Width Length Value*** ***00000000***

Bit	31	30	29	28	27
Name	CHK_DATA12				
Type	RO				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	CHK_DATA12				
Type	RO				
Reset	0	0	0	0	0

[886]	Bit(s)	[887]	Name	[888]	Description
[889]	31:0	[890]	CHK_DATA12	[891]	IR 49-52 pulse width length value, each pulse length is 1byte

[892]	[893]	[894]

10009064 ***CHK_DATA13*** ***IR Pulse Width Length Value*** ***00000000***

Bit	31	30	29	28	27
Name			CHK_DATA13		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			CHK_DATA13		
Type			RO		
Reset	0	0	0	0	0

[895]	Bit(s)	[896]	Name	[897]	Description
[898]	31:0	[899]	CHK_DATA13	[900]	**IR 53-56 pulse width length value, each pulse length is 1byte**
[901]		[902]		[903]	

10009068 ***CHK_DATA14*** ***IR Pulse Width Length Value*** ***00000000***

Bit	31	30	29	28	27
Name			CHK_DATA14		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			CHK_DATA14		
Type			RO		
Reset	0	0	0	0	0

[904]	Bit(s)	[905]	Name	[906]	Description
[907]	31:0	[908]	CHK_DATA14	[909]	**IR 57-60 pulse width length value, each pulse length is 1byte**
[910]		[911]		[912]	

1000906C ***CHK_DATA15*** ***IR Pulse Width Length Value*** ***00000000***

Bit	31	30	29	28	27
Name			CHK_DATA15		
Type			RO		
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name			CHK_DATA15		
Type			RO		
Reset	0	0	0	0	0

[913]	Bit(s)	[914]	Name	[915]	Description
[916]	31:0	[917]	CHK_DATA15	[918]	**IR 61-64 pulse width length value, each pulse length is 1byte**
[919]		[920]		[921]	

10009070 ***CHK_DATA16*** ***IR Pulse Width Length Value*** ***00000000***

Bit	31	30	29	28	27
Name	CHK_DATA16				
Type	RO				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	CHK_DATA16				
Type	RO				
Reset	0	0	0	0	0

[922]	Bit(s)	[923] Name	[924] Description
[925]	31:0	[926] CHK_DATA16	[927] **IR 65-68 pulse width length value, each pulse length is 1byte**

[928] [929] [930]

1.8 GPIO Controller

1.8.1 Introduction

All functions should comply with the priority rule. When there are more than one IO set as the same output function, all of the selected IOs are able to output specific signals. When there are more than one IO set as the same input (or bi-directional) function, only the IO with the largest GPIO index works functionally.

1.8.2 Features

Each GPIO controls the auxlillary mode by programming GPIO_MODE_SELx command register. Besides, the dedicated register bits can be set to 1 or 0 by writing the bits of GPIO_MODE_SETx or GPIO_MODE_RESETx to 1.
GPIO_DIR, GPIO_DOUT and GPIO_PULLEN are also programmable by the same method of GPIO_MODE.

1.8.3 Block Diagram

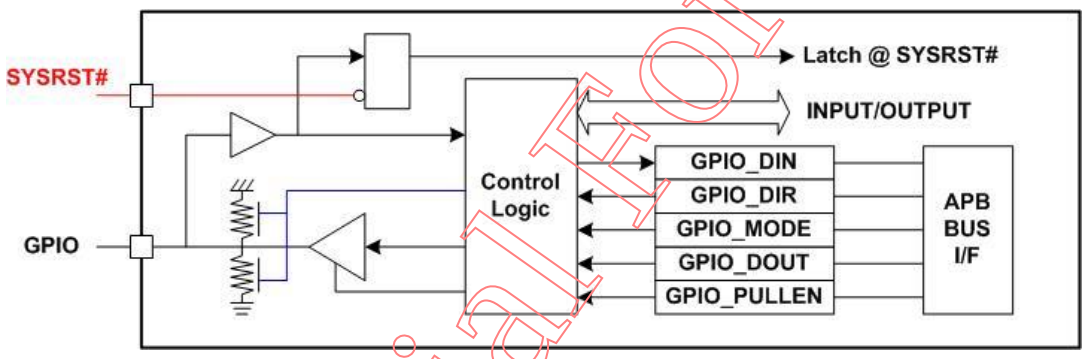


Figure 1-6. GPIO block diagram

1.8.4 Register Definition

Module name: GPIO Base address: (+10211000h)

Address	Name	Width	Register Function
10211000	GPIO_DIR1	32	GPIO Direction Control Register 1
10211010	GPIO_DIR2	32	GPIO Direction Control Register 2
10211020	GPIO_DIR3	32	GPIO Direction Control Register 3
10211030	GPIO_DIR4	32	GPIO Direction Control Register 4
10211100	GPIO_DOUT1	32	GPIO Data Output Register 1
10211110	GPIO_DOUT2	32	GPIO Data Output Register 2
10211120	GPIO_DOUT3	32	GPIO Data Output Register 3
10211130	GPIO_DOUT4	32	GPIO Data Output Register 4
10211200	GPIO_DIN1	32	GPIO Data Input Register 1
10211210	GPIO_DIN2	32	GPIO Data Input Register 2
10211220	GPIO_DIN3	32	GPIO Data Input Register 3
10211230	GPIO_DIN4	32	GPIO Data Input Register 4

Address	Name	Width	Register Function
10211300	GPIO_MODE0	32	GPIO Mode Control Register 0
10211310	GPIO_MODE1	32	GPIO Mode Control Register 1
10211320	GPIO_MODE2	32	GPIO Mode Control Register 2
10211330	GPIO_MODE3	32	GPIO Mode Control Register 3
10211340	GPIO_MODE4	32	GPIO Mode Control Register 4
10211350	GPIO_MODE5	32	GPIO Mode Control Register 5
10211360	GPIO_MODE6	32	GPIO Mode Control Register 6
10211370	GPIO_MODE7	32	GPIO Mode Control Register 7
10211380	GPIO_MODE8	32	GPIO Mode Control Register 8
10211390	GPIO_MODE9	32	GPIO Mode Control Register 9
102113A0	GPIO_MODE10	32	GPIO Mode Control Register 10

10211000 GPIO_DIR1 GPIO Direction Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31_DIR	GPIO30_DIR	GPIO29_DIR	GPIO28_DIR	GPIO27_DIR	GPIO26_DIR	GPIO25_DIR	GPIO24_DIR	GPIO23_DIR	GPIO22_DIR	GPIO21_DIR	GPIO20_DIR	GPIO19_DIR	GPIO18_DIR	GPIO17_DIR	GPIO16_DIR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15_DIR	GPIO14_DIR	GPIO13_DIR	GPIO12_DIR	GPIO11_DIR	GPIO10_DIR	GPIO9_DIR	GPIO8_DIR	GPIO7_DIR	GPIO6_DIR	GPIO5_DIR	GPIO4_DIR	GPIO3_DIR	GPIO2_DIR	GPIO1_DIR	GPIO0_DIR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPIO31_D**	GPIO31_DIR	**GPIO 31 direction control** 0: Input 1: Output
30	**GPIO30_D**	GPIO30_DIR	**GPIO 30 direction control** 0: Input 1: Output
29	**GPIO29_D**	GPIO29_DIR	**GPIO 29 direction control** 0: Input 1: Output
28	**GPIO28_D**	GPIO28_DIR	**GPIO 28 direction control** 0: Input 1: Output
27	**GPIO27_D**	GPIO27_DIR	**GPIO 27 direction control** 0: Input 1: Output
26	**GPIO26_D**	GPIO26_DIR	**GPIO 26 direction control** 0: Input 1: Output
25	**GPIO25_D**	GPIO25_DIR	**GPIO 25 direction control** 0: Input 1: Output
24	**GPIO24_D**	GPIO24_DIR	**GPIO 24 direction control**

Bit(s)	Mnemonic	Name	Description
			0: Input 1: Output
23	**GPIO23_D**	GPIO23_DIR	**GPIO 23 direction control** 0: Input 1: Output
22	**GPIO22_D**	GPIO22_DIR	**GPIO 22 direction control** 0: Input 1: Output
21	**GPIO21_D**	GPIO21_DIR	**GPIO 21 direction control** 0: Input 1: Output
20	**GPIO20_D**	GPIO20_DIR	**GPIO 20 direction control** 0: Input 1: Output
19	**GPIO19_D**	GPIO19_DIR	**GPIO 19 direction control** 0: Input 1: Output
18	**GPIO18_D**	GPIO18_DIR	**GPIO 18 direction control** 0: Input 1: Output
17	**GPIO17_D**	GPIO17_DIR	**GPIO 17 direction control** 0: Input 1: Output
16	**GPIO16_D**	GPIO16_DIR	**GPIO 16 direction control** 0: Input 1: Output
15	**GPIO15_D**	GPIO15_DIR	**GPIO 15 direction control** 0: Input 1: Output
14	**GPIO14_D**	GPIO14_DIR	**GPIO 14 direction control** 0: Input 1: Output
13	**GPIO13_D**	GPIO13_DIR	**GPIO 13 direction control** 0: Input 1: Output
12	**GPIO12_D**	GPIO12_DIR	**GPIO 12 direction control** 0: Input 1: Output
11	**GPIO11_D**	GPIO11_DIR	**GPIO 11 direction control** 0: Input 1: Output
10	**GPIO10_D**	GPIO10_DIR	**GPIO 10 direction control** 0: Input 1: Output
9	**GPIO9_D**	GPIO9_DIR	**GPIO 9 direction control** 0: Input 1: Output
8	**GPIO8_D**	GPIO8_DIR	**GPIO 8 direction control** 0: Input 1: Output
7	**GPIO7_D**	GPIO7_DIR	**GPIO 7 direction control**

Bit(s)	Mnemonic	Name	Description
			0: Input 1: Output
6	**GPIO6_D**	GPIO6_DIR	**GPIO 6 direction control** 0: Input 1: Output
5	**GPIO5_D**	GPIO5_DIR	**GPIO 5 direction control** 0: Input 1: Output
4	**GPIO4_D**	GPIO4_DIR	**GPIO 4 direction control** 0: Input 1: Output
3	**GPIO3_D**	GPIO3_DIR	**GPIO 3 direction control** 0: Input 1: Output
2	**GPIO2_D**	GPIO2_DIR	**GPIO 2 direction control** 0: Input 1: Output
1	**GPIO1_D**	GPIO1_DIR	**GPIO 1 direction control** 0: Input 1: Output
0	**GPIO0_D**	GPIO0_DIR	**GPIO 0 direction control** 0: Input 1: Output

10211010 GPIO_DIR2 GPIO Direction Control Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO63_DIR	GPIO62_DIR	GPIO61_DIR	GPIO60_DIR	GPIO59_DIR	GPIO58_DIR	GPIO57_DIR	GPIO56_DIR	GPIO55_DIR	GPIO54_DIR	GPIO53_DIR	GPIO52_DIR	GPIO51_DIR	GPIO50_DIR	GPIO49_DIR	GPIO48_DIR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47_DIR	GPIO46_DIR	GPIO45_DIR	GPIO44_DIR	GPIO43_DIR	GPIO42_DIR	GPIO41_DIR	GPIO40_DIR	GPIO39_DIR	GPIO38_DIR	GPIO37_DIR	GPIO36_DIR	GPIO35_DIR	GPIO34_DIR	GPIO33_DIR	GPIO32_DIR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPIO63_D**	GPIO63_DIR	**GPIO 63 direction control** 0: Input 1: Output
30	**GPIO62_D**	GPIO62_DIR	**GPIO 62 direction control** 0: Input 1: Output
29	**GPIO61_D**	GPIO61_DIR	**GPIO 61 direction control**

Bit(s)	Mnemonic	Name	Description
			0: Input 1: Output
28	**GPIO60_D**	GPIO60_DIR	**GPIO 60 direction control** 0: Input 1: Output
27	**GPIO59_D**	GPIO59_DIR	**GPIO 59 direction control** 0: Input 1: Output
26	**GPIO58_D**	GPIO58_DIR	**GPIO 58 direction control** 0: Input 1: Output
25	**GPIO57_D**	GPIO57_DIR	**GPIO 57 direction control** 0: Input 1: Output
24	**GPIO56_D**	GPIO56_DIR	**GPIO 56 direction control** 0: Input 1: Output
23	**GPIO55_D**	GPIO55_DIR	**GPIO 55 direction control** 0: Input 1: Output
22	**GPIO54_D**	GPIO54_DIR	**GPIO 54 direction control** 0: Input 1: Output
21	**GPIO53_D**	GPIO53_DIR	**GPIO 53 direction control** 0: Input 1: Output
20	**GPIO52_D**	GPIO52_DIR	**GPIO 52 direction control** 0: Input 1: Output
19	**GPIO51_D**	GPIO51_DIR	**GPIO 51 direction control** 0: Input 1: Output
18	**GPIO50_D**	GPIO50_DIR	**GPIO 50 direction control** 0: Input 1: Output
17	**GPIO49_D**	GPIO49_DIR	**GPIO 49 direction control** 0: Input 1: Output
16	**GPIO48_D**	GPIO48_DIR	**GPIO 48 direction control** 0: Input 1: Output
15	**GPIO47_D**	GPIO47_DIR	**GPIO 47 direction control** 0: Input 1: Output
14	**GPIO46_D**	GPIO46_DIR	**GPIO 46 direction control** 0: Input 1: Output
13	**GPIO45_D**	GPIO45_DIR	**GPIO 45 direction control** 0: Input 1: Output
12	**GPIO44_D**	GPIO44_DIR	**GPIO 44 direction control**

Bit(s)	Mnemonic	Name	Description
			0: Input 1: Output
11	**GPIO43_D**	GPIO43_DIR	**GPIO 43 direction control** 0: Input 1: Output
10	**GPIO42_D**	GPIO42_DIR	**GPIO 42 direction control** 0: Input 1: Output
9	**GPIO41_D**	GPIO41_DIR	**GPIO 41 direction control** 0: Input 1: Output
8	**GPIO40_D**	GPIO40_DIR	**GPIO 40 direction control** 0: Input 1: Output
7	**GPIO39_D**	GPIO39_DIR	**GPIO 39 direction control** 0: Input 1: Output
6	**GPIO38_D**	GPIO38_DIR	**GPIO 38 direction control** 0: Input 1: Output
5	**GPIO37_D**	GPIO37_DIR	**GPIO 37 direction control** 0: Input 1: Output
4	**GPIO36_D**	GPIO36_DIR	**GPIO 36 direction control** 0: Input 1: Output
3	**GPIO35_D**	GPIO35_DIR	**GPIO 35 direction control** 0: Input 1: Output
2	**GPIO34_D**	GPIO34_DIR	**GPIO 34 direction control** 0: Input 1: Output
1	**GPIO33_D**	GPIO33_DIR	**GPIO 33 direction control** 0: Input 1: Output
0	**GPIO32_D**	GPIO32_DIR	**GPIO 32 direction control** 0: Input 1: Output

10211020 GPIO_DIR3 GPIO Direction Control Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO95_DIR	GPIO94_DIR	GPIO93_DIR	GPIO92_DIR	GPIO91_DIR	GPIO90_DIR	GPIO89_DIR	GPIO88_DIR	GPIO87_DIR	GPIO86_DIR	GPIO85_DIR	GPIO84_DIR	GPIO83_DIR	GPIO82_DIR	GPIO81_DIR	GPIO80_DIR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	GPIO79_DIR	GPIO78_DIR	GPIO77_DIR	GPIO76_DIR	GPIO75_DIR	GPIO74_DIR	GPIO73_DIR	GPIO72_DIR	GPIO71_DIR	GPIO70_DIR	GPIO69_DIR	GPIO68_DIR	GPIO67_DIR	GPIO66_DIR	GPIO65_DIR	GPIO64_DIR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPIO95_D**	GPIO95_DIR	**GPIO 95 direction control** 0: Input 1: Output
30	**GPIO94_D**	GPIO94_DIR	**GPIO 94 direction control** 0: Input 1: Output
29	**GPIO93_D**	GPIO93_DIR	**GPIO 93 direction control** 0: Input 1: Output
28	**GPIO92_D**	GPIO92_DIR	**GPIO 92 direction control** 0: Input 1: Output
27	**GPIO91_D**	GPIO91_DIR	**GPIO 91 direction control** 0: Input 1: Output
26	**GPIO90_D**	GPIO90_DIR	**GPIO 90 direction control** 0: Input 1: Output
25	**GPIO89_D**	GPIO89_DIR	**GPIO 89 direction control** 0: Input 1: Output
24	**GPIO88_D**	GPIO88_DIR	**GPIO 88 direction control** 0: Input 1: Output
23	**GPIO87_D**	GPIO87_DIR	**GPIO 87 direction control** 0: Input 1: Output
22	**GPIO86_D**	GPIO86_DIR	**GPIO 86 direction control** 0: Input 1: Output
21	**GPIO85_D**	GPIO85_DIR	**GPIO 85 direction control** 0: Input 1: Output
20	**GPIO84_D**	GPIO84_DIR	**GPIO 84 direction control** 0: Input 1: Output
19	**GPIO83_D**	GPIO83_DIR	**GPIO 83 direction control** 0: Input 1: Output
18	**GPIO82_D**	GPIO82_DIR	**GPIO 82 direction control** 0: Input 1: Output
17	**GPIO81_D**	GPIO81_DIR	**GPIO 81 direction control**

Bit(s)	Mnemonic	Name	Description
			0: Input 1: Output
16	**GPIO80_D**	GPIO80_DIR	**GPIO 80 direction control** 0: Input 1: Output
15	**GPIO79_D**	GPIO79_DIR	**GPIO 79 direction control** 0: Input 1: Output
14	**GPIO78_D**	GPIO78_DIR	**GPIO 78 direction control** 0: Input 1: Output
13	**GPIO77_D**	GPIO77_DIR	**GPIO 77 direction control** 0: Input 1: Output
12	**GPIO76_D**	GPIO76_DIR	**GPIO 76 direction control** 0: Input 1: Output
11	**GPIO75_D**	GPIO75_DIR	**GPIO 75 direction control** 0: Input 1: Output
10	**GPIO74_D**	GPIO74_DIR	**GPIO 74 direction control** 0: Input 1: Output
9	**GPIO73_D**	GPIO73_DIR	**GPIO 73 direction control** 0: Input 1: Output
8	**GPIO72_D**	GPIO72_DIR	**GPIO 72 direction control** 0: Input 1: Output
7	**GPIO71_D**	GPIO71_DIR	**GPIO 71 direction control** 0: Input 1: Output
6	**GPIO70_D**	GPIO70_DIR	**GPIO 70 direction control** 0: Input 1: Output
5	**GPIO69_D**	GPIO69_DIR	**GPIO 69 direction control** 0: Input 1: Output
4	**GPIO68_D**	GPIO68_DIR	**GPIO 68 direction control** 0: Input 1: Output
3	**GPIO67_D**	GPIO67_DIR	**GPIO 67 direction control** 0: Input 1: Output
2	**GPIO66_D**	GPIO66_DIR	**GPIO 66 direction control** 0: Input 1: Output
1	**GPIO65_D**	GPIO65_DIR	**GPIO 65 direction control** 0: Input 1: Output
0	**GPIO64_D**	GPIO64_DIR	**GPIO 64 direction control**

Bit(s)	Mnemonic	Name	Description
			0: Input 1: Output

10211030 GPIO_DIR4 GPIO Direction Control Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO127_DIR	GPIO126_DIR	GPIO125_DIR	GPIO124_DIR	GPIO123_DIR	GPIO122_DIR	GPIO121_DIR	GPIO120_DIR	GPIO119_DIR	GPIO118_DIR	GPIO117_DIR	GPIO116_DIR	GPIO115_DIR	GPIO114_DIR	GPIO113_DIR	GPIO112_DIR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO111_DIR	GPIO110_DIR	GPIO109_DIR	GPIO108_DIR	GPIO107_DIR	GPIO106_DIR	GPIO105_DIR	GPIO104_DIR	GPIO103_DIR	GPIO102_DIR	GPIO101_DIR	GPIO100_DIR	GPIO99_DIR	GPIO98_DIR	GPIO97_DIR	GPIO96_DIR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPIO127_D**	GPIO127_DIR	**GPIO 127 direction control** 0: Input 1: Output
30	**GPIO126_D**	GPIO126_DIR	**GPIO 126 direction control** 0: Input 1: Output
29	**GPIO125_D**	GPIO125_DIR	**GPIO 125 direction control** 0: Input 1: Output
28	**GPIO124_D**	GPIO124_DIR	**GPIO 124 direction control** 0: Input 1: Output
27	**GPIO123_D**	GPIO123_DIR	**GPIO 123 direction control** 0: Input 1: Output
26	**GPIO122_D**	GPIO122_DIR	**GPIO 122 direction control** 0: Input 1: Output
25	**GPIO121_D**	GPIO121_DIR	**GPIO 121 direction control** 0: Input 1: Output
24	**GPIO120_D**	GPIO120_DIR	**GPIO 120 direction control** 0: Input 1: Output
23	**GPIO119_D**	GPIO119_DIR	**GPIO 119 direction control** 0: Input 1: Output
22	**GPIO118_D**	GPIO118_DIR	**GPIO 118 direction control**

Bit(s)	Mnemonic	Name	Description
			0: Input 1: Output
21	**GPIO117_D**	GPIO117_DIR	**GPIO 117 direction control** 0: Input 1: Output
20	**GPIO116_D**	GPIO116_DIR	**GPIO 116 direction control** 0: Input 1: Output
19	**GPIO115_D**	GPIO115_DIR	**GPIO 115 direction control** 0: Input 1: Output
18	**GPIO114_D**	GPIO114_DIR	**GPIO 114 direction control** 0: Input 1: Output
17	**GPIO113_D**	GPIO113_DIR	**GPIO 113 direction control** 0: Input 1: Output
16	**GPIO112_D**	GPIO112_DIR	**GPIO 112 direction control** 0: Input 1: Output
15	**GPIO111_D**	GPIO111_DIR	**GPIO 111 direction control** 0: Input 1: Output
14	**GPIO110_D**	GPIO110_DIR	**GPIO 110 direction control** 0: Input 1: Output
13	**GPIO109_D**	GPIO109_DIR	**GPIO 109 direction control** 0: Input 1: Output
12	**GPIO108_D**	GPIO108_DIR	**GPIO 108 direction control** 0: Input 1: Output
11	**GPIO107_D**	GPIO107_DIR	**GPIO 107 direction control** 0: Input 1: Output
10	**GPIO106_D**	GPIO106_DIR	**GPIO 106 direction control** 0: Input 1: Output
9	**GPIO105_D**	GPIO105_DIR	**GPIO 105 direction control** 0: Input 1: Output
8	**GPIO104_D**	GPIO104_DIR	**GPIO 104 direction control** 0: Input 1: Output
7	**GPIO103_D**	GPIO103_DIR	**GPIO 103 direction control** 0: Input 1: Output
6	**GPIO102_D**	GPIO102_DIR	**GPIO 102 direction control** 0: Input 1: Output
5	**GPIO101_D**	GPIO101_DIR	**GPIO 101 direction control**

Bit(s)	Mnemonic	Name	Description
			0: Input 1: Output
4	**GPIO100_D**	GPIO100_DIR	**GPIO 100 direction control** 0: Input 1: Output
3	**GPIO99_D**	GPIO99_DIR	**GPIO 99 direction control** 0: Input 1: Output
2	**GPIO98_D**	GPIO98_DIR	**GPIO 98 direction control** 0: Input 1: Output
1	**GPIO97_D**	GPIO97_DIR	**GPIO 97 direction control** 0: Input 1: Output
0	**GPIO96_D**	GPIO96_DIR	**GPIO 96 direction control** 0: Input 1: Output

10211100 GPIO_DOUT1 GPIO Data Output Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31_DOUT	GPIO30_DOUT	GPIO29_DOUT	GPIO28_DOUT	GPIO27_DOUT	GPIO26_DOUT	GPIO25_DOUT	GPIO24_DOUT	GPIO23_DOUT	GPIO22_DOUT	GPIO21_DOUT	GPIO20_DOUT	GPIO19_DOUT	GPIO18_DOUT	GPIO17_DOUT	GPIO16_DOUT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15_DOUT	GPIO14_DOUT	GPIO13_DOUT	GPIO12_DOUT	GPIO11_DOUT	GPIO10_DOUT	GPIO9_DOUT	GPIO8_DOUT	GPIO7_DOUT	GPIO6_DOUT	GPIO5_DOUT	GPIO4_DOUT	GPIO3_DOUT	GPIO2_DOUT	GPIO1_DOUT	GPIO0_DOUT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPO31**	GPIO31_DOUT	**GPIO 31 data output value** 0: Output 0 1: Output 1
30	**GPO30**	GPIO30_DOUT	**GPIO 30 data output value** 0: Output 0 1: Output 1
29	**GPO29**	GPIO29_DOUT	**GPIO 29 data output value** 0: Output 0 1: Output 1
28	**GPO28**	GPIO28_DOUT	**GPIO 28 data output value** 0: Output 0 1: Output 1
27	**GPO27**	GPIO27_DOUT	**GPIO 27 data output value**

Bit(s)	Mnemonic	Name	Description
			0: Output 0 1: Output 1
26	**GPO26**	GPIO26_DOUT	**GPIO 26 data output value** 0: Output 0 1: Output 1
25	**GPO25**	GPIO25_DOUT	**GPIO 25 data output value** 0: Output 0 1: Output 1
24	**GPO24**	GPIO24_DOUT	**GPIO 24 data output value** 0: Output 0 1: Output 1
23	**GPO23**	GPIO23_DOUT	**GPIO 23 data output value** 0: Output 0 1: Output 1
22	**GPO22**	GPIO22_DOUT	**GPIO 22 data output value** 0: Output 0 1: Output 1
21	**GPO21**	GPIO21_DOUT	**GPIO 21 data output value** 0: Output 0 1: Output 1
20	**GPO20**	GPIO20_DOUT	**GPIO 20 data output value** 0: Output 0 1: Output 1
19	**GPO19**	GPIO19_DOUT	**GPIO 19 data output value** 0: Output 0 1: Output 1
18	**GPO18**	GPIO18_DOUT	**GPIO 18 data output value** 0: Output 0 1: Output 1
17	**GPO17**	GPIO17_DOUT	**GPIO 17 data output value** 0: Output 0 1: Output 1
16	**GPO16**	GPIO16_DOUT	**GPIO 16 data output value** 0: Output 0 1: Output 1
15	**GPO15**	GPIO15_DOUT	**GPIO 15 data output value** 0: Output 0 1: Output 1
14	**GPO14**	GPIO14_DOUT	**GPIO 14 data output value** 0: Output 0 1: Output 1
13	**GPO13**	GPIO13_DOUT	**GPIO 13 data output value** 0: Output 0 1: Output 1
12	**GPO12**	GPIO12_DOUT	**GPIO 12 data output value** 0: Output 0 1: Output 1
11	**GPO11**	GPIO11_DOUT	**GPIO 11 data output value** 0: Output 0 1: Output 1
10	**GPO10**	GPIO10_DOUT	**GPIO 10 data output value**

Bit(s)	Mnemonic	Name	Description
			0: Output 0 1: Output 1
9	**GPO9**	GPIO9_DOUT	**GPIO 9 data output value** 0: Output 0 1: Output 1
8	**GPO8**	GPIO8_DOUT	**GPIO 8 data output value** 0: Output 0 1: Output 1
7	**GPO7**	GPIO7_DOUT	**GPIO 7 data output value** 0: Output 0 1: Output 1
6	**GPO6**	GPIO6_DOUT	**GPIO 6 data output value** 0: Output 0 1: Output 1
5	**GPO5**	GPIO5_DOUT	**GPIO 5 data output value** 0: Output 0 1: Output 1
4	**GPO4**	GPIO4_DOUT	**GPIO 4 data output value** 0: Output 0 1: Output 1
3	**GPO3**	GPIO3_DOUT	**GPIO 3 data output value** 0: Output 0 1: Output 1
2	**GPO2**	GPIO2_DOUT	**GPIO 2 data output value** 0: Output 0 1: Output 1
1	**GPO1**	GPIO1_DOUT	**GPIO 1 data output value** 0: Output 0 1: Output 1
0	**GPO0**	GPIO0_DOUT	**GPIO 0 data output value** 0: Output 0 1: Output 1

10211110 GPIO_DOUT2 GPIO Data Output Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO63_DOUT	GPIO62_DOUT	GPIO61_DOUT	GPIO60_DOUT	GPIO59_DOUT	GPIO58_DOUT	GPIO57_DOUT	GPIO56_DOUT	GPIO55_DOUT	GPIO54_DOUT	GPIO53_DOUT	GPIO52_DOUT	GPIO51_DOUT	GPIO50_DOUT	GPIO49_DOUT	GPIO48_DOUT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47_DOUT	GPIO46_DOUT	GPIO45_DOUT	GPIO44_DOUT	GPIO43_DOUT	GPIO42_DOUT	GPIO41_DOUT	GPIO40_DOUT	GPIO39_DOUT	GPIO38_DOUT	GPIO37_DOUT	GPIO36_DOUT	GPIO35_DOUT	GPIO34_DOUT	GPIO33_DOUT	GPIO32_DOUT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPO63**	GPIO63_DOUT	**GPIO 63 data output value** 0: Output 0 1: Output 1
30	**GPO62**	GPIO62_DOUT	**GPIO 62 data output value** 0: Output 0 1: Output 1
29	**GPO61**	GPIO61_DOUT	**GPIO 61 data output value** 0: Output 0 1: Output 1
28	**GPO60**	GPIO60_DOUT	**GPIO 60 data output value** 0: Output 0 1: Output 1
27	**GPO59**	GPIO59_DOUT	**GPIO 59 data output value** 0: Output 0 1: Output 1
26	**GPO58**	GPIO58_DOUT	**GPIO 58 data output value** 0: Output 0 1: Output 1
25	**GPO57**	GPIO57_DOUT	**GPIO 57 data output value** 0: Output 0 1: Output 1
24	**GPO56**	GPIO56_DOUT	**GPIO 56 data output value** 0: Output 0 1: Output 1
23	**GPO55**	GPIO55_DOUT	**GPIO 55 data output value** 0: Output 0 1: Output 1
22	**GPO54**	GPIO54_DOUT	**GPIO 54 data output value** 0: Output 0 1: Output 1
21	**GPO53**	GPIO53_DOUT	**GPIO 53 data output value** 0: Output 0 1: Output 1
20	**GPO52**	GPIO52_DOUT	**GPIO 52 data output value** 0: Output 0 1: Output 1
19	**GPO51**	GPIO51_DOUT	**GPIO 51 data output value** 0: Output 0 1: Output 1
18	**GPO50**	GPIO50_DOUT	**GPIO 50 data output value** 0: Output 0 1: Output 1
17	**GPO49**	GPIO49_DOUT	**GPIO 49 data output value** 0: Output 0 1: Output 1
16	**GPO48**	GPIO48_DOUT	**GPIO 48 data output value** 0: Output 0 1: Output 1
15	**GPO47**	GPIO47_DOUT	**GPIO 47 data output value** 0: Output 0

Bit(s)	Mnemonic	Name	Description
			1: Output 1
14	**GPO46**	GPIO46_DOUT	**GPIO 46 data output value** 0: Output 0 1: Output 1
13	**GPO45**	GPIO45_DOUT	**GPIO 45 data output value** 0: Output 0 1: Output 1
12	**GPO44**	GPIO44_DOUT	**GPIO 44 data output value** 0: Output 0 1: Output 1
11	**GPO43**	GPIO43_DOUT	**GPIO 43 data output value** 0: Output 0 1: Output 1
10	**GPO42**	GPIO42_DOUT	**GPIO 42 data output value** 0: Output 0 1: Output 1
9	**GPO41**	GPIO41_DOUT	**GPIO 41 data output value** 0: Output 0 1: Output 1
8	**GPO40**	GPIO40_DOUT	**GPIO 40 data output value** 0: Output 0 1: Output 1
7	**GPO39**	GPIO39_DOUT	**GPIO 39 data output value** 0: Output 0 1: Output 1
6	**GPO38**	GPIO38_DOUT	**GPIO 38 data output value** 0: Output 0 1: Output 1
5	**GPO37**	GPIO37_DOUT	**GPIO 37 data output value** 0: Output 0 1: Output 1
4	**GPO36**	GPIO36_DOUT	**GPIO 36 data output value** 0: Output 0 1: Output 1
3	**GPO35**	GPIO35_DOUT	**GPIO 35 data output value** 0: Output 0 1: Output 1
2	**GPO34**	GPIO34_DOUT	**GPIO 34 data output value** 0: Output 0 1: Output 1
1	**GPO33**	GPIO33_DOUT	**GPIO 33 data output value** 0: Output 0 1: Output 1
0	**GPO32**	GPIO32_DOUT	**GPIO 32 data output value** 0: Output 0 1: Output 1

10211120 GPIO_DOUT3 GPIO Data Output Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	GPIO95_DOUT	GPIO94_DOUT	GPIO93_DOUT	GPIO92_DOUT	GPIO91_DOUT	GPIO90_DOUT	GPIO89_DOUT	GPIO88_DOUT	GPIO87_DOUT	GPIO86_DOUT	GPIO85_DOUT	GPIO84_DOUT	GPIO83_DOUT	GPIO82_DOUT	GPIO81_DOUT	GPIO80_DOUT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO79_DOUT	GPIO78_DOUT	GPIO77_DOUT	GPIO76_DOUT	GPIO75_DOUT	GPIO74_DOUT	GPIO73_DOUT	GPIO72_DOUT	GPIO71_DOUT	GPIO70_DOUT	GPIO69_DOUT	GPIO68_DOUT	GPIO67_DOUT	GPIO66_DOUT	GPIO65_DOUT	GPIO64_DOUT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPO95**	GPIO95_DOUT	**GPIO 95 data output value** 0: Output 0 1: Output 1
30	**GPO94**	GPIO94_DOUT	**GPIO 94 data output value** 0: Output 0 1: Output 1
29	**GPO93**	GPIO93_DOUT	**GPIO 93 data output value** 0: Output 0 1: Output 1
28	**GPO92**	GPIO92_DOUT	**GPIO 92 data output value** 0: Output 0 1: Output 1
27	**GPO91**	GPIO91_DOUT	**GPIO 91 data output value** 0: Output 0 1: Output 1
26	**GPO90**	GPIO90_DOUT	**GPIO 90 data output value** 0: Output 0 1: Output 1
25	**GPO89**	GPIO89_DOUT	**GPIO 89 data output value** 0: Output 0 1: Output 1
24	**GPO88**	GPIO88_DOUT	**GPIO 88 data output value** 0: Output 0 1: Output 1
23	**GPO87**	GPIO87_DOUT	**GPIO 87 data output value** 0: Output 0 1: Output 1
22	**GPO86**	GPIO86_DOUT	**GPIO 86 data output value** 0: Output 0 1: Output 1
21	**GPO85**	GPIO85_DOUT	**GPIO 85 data output value** 0: Output 0 1: Output 1
20	**GPO84**	GPIO84_DOUT	**GPIO 84 data output value** 0: Output 0 1: Output 1

Bit(s)	Mnemonic	Name	Description
19	**GPO83**	GPIO83_DOUT	**GPIO 83 data output value** 0: Output 0 1: Output 1
18	**GPO82**	GPIO82_DOUT	**GPIO 82 data output value** 0: Output 0 1: Output 1
17	**GPO81**	GPIO81_DOUT	**GPIO 81 data output value** 0: Output 0 1: Output 1
16	**GPO80**	GPIO80_DOUT	**GPIO 80 data output value** 0: Output 0 1: Output 1
15	**GPO79**	GPIO79_DOUT	**GPIO 79 data output value** 0: Output 0 1: Output 1
14	**GPO78**	GPIO78_DOUT	**GPIO 78 data output value** 0: Output 0 1: Output 1
13	**GPO77**	GPIO77_DOUT	**GPIO 77 data output value** 0: Output 0 1: Output 1
12	**GPO76**	GPIO76_DOUT	**GPIO 76 data output value** 0: Output 0 1: Output 1
11	**GPO75**	GPIO75_DOUT	**GPIO 75 data output value** 0: Output 0 1: Output 1
10	**GPO74**	GPIO74_DOUT	**GPIO 74 data output value** 0: Output 0 1: Output 1
9	**GPO73**	GPIO73_DOUT	**GPIO 73 data output value** 0: Output 0 1: Output 1
8	**GPO72**	GPIO72_DOUT	**GPIO 72 data output value** 0: Output 0 1: Output 1
7	**GPO71**	GPIO71_DOUT	**GPIO 71 data output value** 0: Output 0 1: Output 1
6	**GPO70**	GPIO70_DOUT	**GPIO 70 data output value** 0: Output 0 1: Output 1
5	**GPO69**	GPIO69_DOUT	**GPIO 69 data output value** 0: Output 0 1: Output 1
4	**GPO68**	GPIO68_DOUT	**GPIO 68 data output value** 0: Output 0 1: Output 1
3	**GPO67**	GPIO67_DOUT	**GPIO 67 data output value** 0: Output 0 1: Output 1

Bit(s)	Mnemonic	Name	Description
2	**GPO66**	GPIO66_DOUT	**GPIO 66 data output value** 0: Output 0 1: Output 1
1	**GPO65**	GPIO65_DOUT	**GPIO 65 data output value** 0: Output 0 1: Output 1
0	**GPO64**	GPIO64_DOUT	**GPIO 64 data output value** 0: Output 0 1: Output 1

10211130 GPIO_DOUT4 GPIO Data Output Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO127_DOUT	GPIO126_DOUT	GPIO125_DOUT	GPIO124_DOUT	GPIO123_DOUT	GPIO122_DOUT	GPIO121_DOUT	GPIO120_DOUT	GPIO119_DOUT	GPIO118_DOUT	GPIO117_DOUT	GPIO116_DOUT	GPIO115_DOUT	GPIO114_DOUT	GPIO113_DOUT	GPIO112_DOUT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO111_DOUT	GPIO110_DOUT	GPIO109_DOUT	GPIO108_DOUT	GPIO107_DOUT	GPIO106_DOUT	GPIO105_DOUT	GPIO104_DOUT	GPIO103_DOUT	GPIO102_DOUT	GPIO101_DOUT	GPIO100_DOUT	GPIO99_DOUT	GPIO98_DOUT	GPIO97_DOUT	GPIO96_DOUT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPO127**	GPIO127_DOUT	**GPIO 127 data output value** 0: Output 0 1: Output 1
30	**GPO126**	GPIO126_DOUT	**GPIO 126 data output value** 0: Output 0 1: Output 1
29	**GPO125**	GPIO125_DOUT	**GPIO 125 data output value** 0: Output 0 1: Output 1
28	**GPO124**	GPIO124_DOUT	**GPIO 124 data output value** 0: Output 0 1: Output 1
27	**GPO123**	GPIO123_DOUT	**GPIO 123 data output value** 0: Output 0 1: Output 1
26	**GPO122**	GPIO122_DOUT	**GPIO 122 data output value** 0: Output 0 1: Output 1
25	**GPO121**	GPIO121_DOUT	**GPIO 121 data output value** 0: Output 0 1: Output 1
24	**GPO120**	GPIO120_DOUT	**GPIO 120 data output value** 0: Output 0 1: Output 1
23	**GPO119**	GPIO119_DOUT	**GPIO 119 data output value**

Bit(s)	Mnemonic	Name	Description
			0: Output 0 1: Output 1
22	**GPO118**	GPIO118_DOUT	**GPIO 118 data output value** 0: Output 0 1: Output 1
21	**GPO117**	GPIO117_DOUT	**GPIO 117 data output value** 0: Output 0 1: Output 1
20	**GPO116**	GPIO116_DOUT	**GPIO 116 data output value** 0: Output 0 1: Output 1
19	**GPO115**	GPIO115_DOUT	**GPIO 115 data output value** 0: Output 0 1: Output 1
18	**GPO114**	GPIO114_DOUT	**GPIO 114 data output value** 0: Output 0 1: Output 1
17	**GPO113**	GPIO113_DOUT	**GPIO 113 data output value** 0: Output 0 1: Output 1
16	**GPO112**	GPIO112_DOUT	**GPIO 112 data output value** 0: Output 0 1: Output 1
15	**GPO111**	GPIO111_DOUT	**GPIO 111 data output value** 0: Output 0 1: Output 1
14	**GPO110**	GPIO110_DOUT	**GPIO 110 data output value** 0: Output 0 1: Output 1
13	**GPO109**	GPIO109_DOUT	**GPIO 109 data output value** 0: Output 0 1: Output 1
12	**GPO108**	GPIO108_DOUT	**GPIO 108 data output value** 0: Output 0 1: Output 1
11	**GPO107**	GPIO107_DOUT	**GPIO 107 data output value** 0: Output 0 1: Output 1
10	**GPO106**	GPIO106_DOUT	**GPIO 106 data output value** 0: Output 0 1: Output 1
9	**GPO105**	GPIO105_DOUT	**GPIO 105 data output value** 0: Output 0 1: Output 1
8	**GPO104**	GPIO104_DOUT	**GPIO 104 data output value** 0: Output 0 1: Output 1
7	**GPO103**	GPIO103_DOUT	**GPIO 103 data output value** 0: Output 0 1: Output 1
6	**GPO102**	GPIO102_DOUT	**GPIO 102 data output value**

Bit(s)	Mnemonic	Name	Description
			0: Output 0 1: Output 1
5	**GPO101**	GPIO101_DOUT	**GPIO 101 data output value** 0: Output 0 1: Output 1
4	**GPO100**	GPIO100_DOUT	**GPIO 100 data output value** 0: Output 0 1: Output 1
3	**GPO99**	GPIO99_DOUT	**GPIO 99 data output value** 0: Output 0 1: Output 1
2	**GPO98**	GPIO98_DOUT	**GPIO 98 data output value** 0: Output 0 1: Output 1
1	**GPO97**	GPIO97_DOUT	**GPIO 97 data output value** 0: Output 0 1: Output 1
0	**GPO96**	GPIO96_DOUT	**GPIO 96 data output value** 0: Output 0 1: Output 1

10211200 GPIO_DIN1 GPIO Data Input Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31_DIN	GPIO30_DIN	GPIO29_DIN	GPIO28_DIN	GPIO27_DIN	GPIO26_DIN	GPIO25_DIN	GPIO24_DIN	GPIO23_DIN	GPIO22_DIN	GPIO21_DIN	GPIO20_DIN	GPIO19_DIN	GPIO18_DIN	GPIO17_DIN	GPIO16_DIN
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15_DIN	GPIO14_DIN	GPIO13_DIN	GPIO12_DIN	GPIO11_DIN	GPIO10_DIN	GPIO9_DIN	GPIO8_DIN	GPIO7_DIN	GPIO6_DIN	GPIO5_DIN	GPIO4_DIN	GPIO3_DIN	GPIO2_DIN	GPIO1_DIN	GPIO0_DIN
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPI31**	GPIO31_DIN	**GPIO 31 data input value**
30	**GPI30**	GPIO30_DIN	**GPIO 30 data input value**
29	**GPI29**	GPIO29_DIN	**GPIO 29 data input value**
28	**GPI28**	GPIO28_DIN	**GPIO 28 data input value**
27	**GPI27**	GPIO27_DIN	**GPIO 27 data input value**
26	**GPI26**	GPIO26_DIN	**GPIO 26 data input value**
25	**GPI25**	GPIO25_DIN	**GPIO 25 data input value**
24	**GPI24**	GPIO24_DIN	**GPIO 24 data input value**
23	**GPI23**	GPIO23_DIN	**GPIO 23 data input value**
22	**GPI22**	GPIO22_DIN	**GPIO 22 data input value**
21	**GPI21**	GPIO21_DIN	**GPIO 21 data input value**
20	**GPI20**	GPIO20_DIN	**GPIO 20 data input value**
19	**GPI19**	GPIO19_DIN	**GPIO 19 data input value**
18	**GPI18**	GPIO18_DIN	**GPIO 18 data input value**
17	**GPI17**	GPIO17_DIN	**GPIO 17 data input value**

Bit(s)	Mnemonic	Name	Description
16	**GPI16**	GPIO16_DIN	**GPIO 16 data input value**
15	**GPI15**	GPIO15_DIN	**GPIO 15 data input value**
14	**GPI14**	GPIO14_DIN	**GPIO 14 data input value**
13	**GPI13**	GPIO13_DIN	**GPIO 13 data input value**
12	**GPI12**	GPIO12_DIN	**GPIO 12 data input value**
11	**GPI11**	GPIO11_DIN	**GPIO 11 data input value**
10	**GPI10**	GPIO10_DIN	**GPIO 10 data input value**
9	**GPI9**	GPIO9_DIN	**GPIO 9 data input value**
8	**GPI8**	GPIO8_DIN	**GPIO 8 data input value**
7	**GPI7**	GPIO7_DIN	**GPIO 7 data input value**
6	**GPI6**	GPIO6_DIN	**GPIO 6 data input value**
5	**GPI5**	GPIO5_DIN	**GPIO 5 data input value**
4	**GPI4**	GPIO4_DIN	**GPIO 4 data input value**
3	**GPI3**	GPIO3_DIN	**GPIO 3 data input value**
2	**GPI2**	GPIO2_DIN	**GPIO 2 data input value**
1	**GPI1**	GPIO1_DIN	**GPIO 1 data input value**
0	**GPI0**	GPIO0_DIN	**GPIO 0 data input value**

10211210 GPIO_DIN2 GPIO Data Input Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO63_DIN	GPIO62_DIN	GPIO61_DIN	GPIO60_DIN	GPIO59_DIN	GPIO58_DIN	GPIO57_DIN	GPIO56_DIN	GPIO55_DIN	GPIO54_DIN	GPIO53_DIN	GPIO52_DIN	GPIO51_DIN	GPIO50_DIN	GPIO49_DIN	GPIO48_DIN
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47_DIN	GPIO46_DIN	GPIO45_DIN	GPIO44_DIN	GPIO43_DIN	GPIO42_DIN	GPIO41_DIN	GPIO40_DIN	GPIO39_DIN	GPIO38_DIN	GPIO37_DIN	GPIO36_DIN	GPIO35_DIN	GPIO34_DIN	GPIO33_DIN	GPIO32_DIN
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPI63**	GPIO63_DIN	**GPIO 63 data input value**
30	**GPI62**	GPIO62_DIN	**GPIO 62 data input value**
29	**GPI61**	GPIO61_DIN	**GPIO 61 data input value**
28	**GPI60**	GPIO60_DIN	**GPIO 60 data input value**
27	**GPI59**	GPIO59_DIN	**GPIO 59 data input value**
26	**GPI58**	GPIO58_DIN	**GPIO 58 data input value**
25	**GPI57**	GPIO57_DIN	**GPIO 57 data input value**
24	**GPI56**	GPIO56_DIN	**GPIO 56 data input value**
23	**GPI55**	GPIO55_DIN	**GPIO 55 data input value**
22	**GPI54**	GPIO54_DIN	**GPIO 54 data input value**
21	**GPI53**	GPIO53_DIN	**GPIO 53 data input value**
20	**GPI52**	GPIO52_DIN	**GPIO 52 data input value**
19	**GPI51**	GPIO51_DIN	**GPIO 51 data input value**
18	**GPI50**	GPIO50_DIN	**GPIO 50 data input value**
17	**GPI49**	GPIO49_DIN	**GPIO 49 data input value**
16	**GPI48**	GPIO48_DIN	**GPIO 48 data input value**
15	**GPI47**	GPIO47_DIN	**GPIO 47 data input value**
14	**GPI46**	GPIO46_DIN	**GPIO 46 data input value**
13	**GPI45**	GPIO45_DIN	**GPIO 45 data input value**
12	**GPI44**	GPIO44_DIN	**GPIO 44 data input value**

Bit(s)	Mnemonic	Name	Description
11	**GPI43**	GPIO43_DIN	**GPIO 43 data input value**
10	**GPI42**	GPIO42_DIN	**GPIO 42 data input value**
9	**GPI41**	GPIO41_DIN	**GPIO 41 data input value**
8	**GPI40**	GPIO40_DIN	**GPIO 40 data input value**
7	**GPI39**	GPIO39_DIN	**GPIO 39 data input value**
6	**GPI38**	GPIO38_DIN	**GPIO 38 data input value**
5	**GPI37**	GPIO37_DIN	**GPIO 37 data input value**
4	**GPI36**	GPIO36_DIN	**GPIO 36 data input value**
3	**GPI35**	GPIO35_DIN	**GPIO 35 data input value**
2	**GPI34**	GPIO34_DIN	**GPIO 34 data input value**
1	**GPI33**	GPIO33_DIN	**GPIO 33 data input value**
0	**GPI32**	GPIO32_DIN	**GPIO 32 data input value**

10211220 GPIO_DIN3 GPIO Data Input Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO95_DIN	GPIO94_DIN	GPIO93_DIN	GPIO92_DIN	GPIO91_DIN	GPIO90_DIN	GPIO89_DIN	GPIO88_DIN	GPIO87_DIN	GPIO86_DIN	GPIO85_DIN	GPIO84_DIN	GPIO83_DIN	GPIO82_DIN	GPIO81_DIN	GPIO80_DIN
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO79_DIN	GPIO78_DIN	GPIO77_DIN	GPIO76_DIN	GPIO75_DIN	GPIO74_DIN	GPIO73_DIN	GPIO72_DIN	GPIO71_DIN	GPIO70_DIN	GPIO69_DIN	GPIO68_DIN	GPIO67_DIN	GPIO66_DIN	GPIO65_DIN	GPIO64_DIN
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPI95**	GPIO95_DIN	**GPIO 95 data input value**
30	**GPI94**	GPIO94_DIN	**GPIO 94 data input value**
29	**GPI93**	GPIO93_DIN	**GPIO 93 data input value**
28	**GPI92**	GPIO92_DIN	**GPIO 92 data input value**
27	**GPI91**	GPIO91_DIN	**GPIO 91 data input value**
26	**GPI90**	GPIO90_DIN	**GPIO 90 data input value**
25	**GPI89**	GPIO89_DIN	**GPIO 89 data input value**
24	**GPI88**	GPIO88_DIN	**GPIO 88 data input value**
23	**GPI87**	GPIO87_DIN	**GPIO 87 data input value**
22	**GPI86**	GPIO86_DIN	**GPIO 86 data input value**
21	**GPI85**	GPIO85_DIN	**GPIO 85 data input value**
20	**GPI84**	GPIO84_DIN	**GPIO 84 data input value**
19	**GPI83**	GPIO83_DIN	**GPIO 83 data input value**
18	**GPI82**	GPIO82_DIN	**GPIO 82 data input value**
17	**GPI81**	GPIO81_DIN	**GPIO 81 data input value**
16	**GPI80**	GPIO80_DIN	**GPIO 80 data input value**
15	**GPI79**	GPIO79_DIN	**GPIO 79 data input value**
14	**GPI78**	GPIO78_DIN	**GPIO 78 data input value**
13	**GPI77**	GPIO77_DIN	**GPIO 77 data input value**
12	**GPI76**	GPIO76_DIN	**GPIO 76 data input value**
11	**GPI75**	GPIO75_DIN	**GPIO 75 data input value**
10	**GPI74**	GPIO74_DIN	**GPIO 74 data input value**
9	**GPI73**	GPIO73_DIN	**GPIO 73 data input value**
8	**GPI72**	GPIO72_DIN	**GPIO 72 data input value**
7	**GPI71**	GPIO71_DIN	**GPIO 71 data input value**

Bit(s)	Mnemonic	Name	Description
6	**GPI70**	GPIO70_DIN	**GPIO 70 data input value**
5	**GPI69**	GPIO69_DIN	**GPIO 69 data input value**
4	**GPI68**	GPIO68_DIN	**GPIO 68 data input value**
3	**GPI67**	GPIO67_DIN	**GPIO 67 data input value**
2	**GPI66**	GPIO66_DIN	**GPIO 66 data input value**
1	**GPI65**	GPIO65_DIN	**GPIO 65 data input value**
0	**GPI64**	GPIO64_DIN	**GPIO 64 data input value**

10211230 GPIO_DIN4 GPIO Data Input Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO127_DIN	GPIO126_DIN	GPIO125_DIN	GPIO124_DIN	GPIO123_DIN	GPIO122_DIN	GPIO121_DIN	GPIO120_DIN	GPIO119_DIN	GPIO118_DIN	GPIO117_DIN	GPIO116_DIN	GPIO115_DIN	GPIO114_DIN	GPIO113_DIN	GPIO112_DIN
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO111_DIN	GPIO110_DIN	GPIO109_DIN	GPIO108_DIN	GPIO107_DIN	GPIO106_DIN	GPIO105_DIN	GPIO104_DIN	GPIO103_DIN	GPIO102_DIN	GPIO101_DIN	GPIO100_DIN	GPIO99_DIN	GPIO98_DIN	GPIO97_DIN	GPIO96_DIN
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPI127**	GPIO127_DIN	**GPIO 127 data input value**
30	**GPI126**	GPIO126_DIN	**GPIO 126 data input value**
29	**GPI125**	GPIO125_DIN	**GPIO 125 data input value**
28	**GPI124**	GPIO124_DIN	**GPIO 124 data input value**
27	**GPI123**	GPIO123_DIN	**GPIO 123 data input value**
26	**GPI122**	GPIO122_DIN	**GPIO 122 data input value**
25	**GPI121**	GPIO121_DIN	**GPIO 121 data input value**
24	**GPI120**	GPIO120_DIN	**GPIO 120 data input value**
23	**GPI119**	GPIO119_DIN	**GPIO 119 data input value**
22	**GPI118**	GPIO118_DIN	**GPIO 118 data input value**
21	**GPI117**	GPIO117_DIN	**GPIO 117 data input value**
20	**GPI116**	GPIO116_DIN	**GPIO 116 data input value**
19	**GPI115**	GPIO115_DIN	**GPIO 115 data input value**
18	**GPI114**	GPIO114_DIN	**GPIO 114 data input value**
17	**GPI113**	GPIO113_DIN	**GPIO 113 data input value**
16	**GPI112**	GPIO112_DIN	**GPIO 112 data input value**
15	**GPI111**	GPIO111_DIN	**GPIO 111 data input value**
14	**GPI110**	GPIO110_DIN	**GPIO 110 data input value**
13	**GPI109**	GPIO109_DIN	**GPIO 109 data input value**
12	**GPI108**	GPIO108_DIN	**GPIO 108 data input value**
11	**GPI107**	GPIO107_DIN	**GPIO 107 data input value**
10	**GPI106**	GPIO106_DIN	**GPIO 106 data input value**
9	**GPI105**	GPIO105_DIN	**GPIO 105 data input value**
8	**GPI104**	GPIO104_DIN	**GPIO 104 data input value**
7	**GPI103**	GPIO103_DIN	**GPIO 103 data input value**
6	**GPI102**	GPIO102_DIN	**GPIO 102 data input value**
5	**GPI101**	GPIO101_DIN	**GPIO 101 data input value**
4	**GPI100**	GPIO100_DIN	**GPIO 100 data input value**
3	**GPI99**	GPIO99_DIN	**GPIO 99 data input value**
2	**GPI98**	GPIO98_DIN	**GPIO 98 data input value**

Bit(s)	Mnemonic	Name	Description
1	**GPI97**	GPIO97_DIN	**GPIO 97 data input value**
0	**GPI96**	GPIO96_DIN	**GPIO 96 data input value**

10211300 GPIO_MODE0 GPIO Mode Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSV1				MDIO_MODE				NAND_MODE				PMIC_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RGMII_MODE				SPI_MODE				UART0_MODE				RSV0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		RSV1	**Reserved**
27:24	**MDIO**	MDIO_MODE	**Selects MDIO mode** 0: MDIO 1: GPIO 23-24 2-7: Reserved
23:20	**NAND**	NAND_MODE	**Selects NAND mode** 0: Parallel NAND Flash 1: GPIO 37-50 2: EMMC 3-7: Reserved
19:16	**PMIC**	PMIC_MODE	**Selects PMIC mode** 0: PMIC I2C 1: GPIO 71-72 2-7: Reserved
15:12	**RGMII**	RGMII_MODE	**Selects RGMII mode** 0: RGMII (GMAC2) 1: GPIO 25-36 2: SDXC 3-7: Reserved
11:8	**SPI**	SPI_MODE	**Selects SPI mode** 0: SPI NOR Flash 1: GPIO 10-13 2: SPI NAND Flash 3 -7 : Reserved
7:4	**UART0**	UART0_MODE	**Selects UART 0 mode** 0: UART0 1: GPIO 6-7 2-7 : Reserved
3:0		RSV0	**Reserved**

10211310 GPIO_MODE1 GPIO Mode Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO21_MODE				GPIO20_MODE				GPIO19_MODE				GPIO18_MODE			

Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO76_MODE				GPIO75_MODE				GPIO74_MODE				GPIO73_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**GPIO21_M**	GPIO21_MODE	**Selects GPIO 21 mode** 0: I2S4_OUT (O) 1: GPIO21 (IO) 2: SD_CMD (O) 3: Reserved 4: Reserved 5: ANTSEL[29] (O) 6: BT_SPXT_C0 (O) 7: DBG_UTIF[15] (IO)
27:24	**GPIO20_M**	GPIO20_MODE	**Selects GPIO 20 mode** 0: I2S3_OUT (O) 1: GPIO20 (IO) 2: SD_CLK (O) 3: Reserved 4: Reserved 5: ANTSEL[28] (O) 6: BT_SPXT_C1 (O) 7: DBG_UTIF[14] (IO)
23:20	**GPIO19_M**	GPIO19_MODE	**Selects GPIO 19 mode** 0: I2S2_OUT (O) 1: GPIO19 (IO) 2: SD_D0 (IO) 3: Reserved 4: Reserved 5: ANTSEL[27] (O) 6: BT_IPATH_EN (O) 7: DBG_UTIF[13] (IO)
19:16	**GPIO18_M**	GPIO18_MODE	**Selects GPIO 18 mode** 0: I2S4_IN (I) 1: GPIO18 (IO) 2: SD_D1 (IO) 3: Reserved 4: Reserved 5: ANTSEL[26] (O) 6: BT_ERX_EN (O) 7: DBG_UTIF[12] (IO)
15:12	**GPIO76_M**	GPIO76_MODE	**Selects GPIO 76 mode** 0:SPIC1_CS (O) 1: GPIO76 (IO) 2: UART CTS1 (I) 3: I2C2_SDA (IO) 4: PWM_CH4 (O) 5: ANTSEL[15](O)

Bit(s)	Mnemonic	Name	Description
			6: Reserved 7: DBG_UTIF[3](IO)
11:8	**GPIO75_M**	GPIO75_MODE	**Selects GPIO 75 mode** 0:SPIC1_MISO (I) 1: GPIO75 (IO) 2: UART RTS1 (O) 3: I2C2_SCL (IO) 4: PWM_CH3 (O) 5: ANTSEL[14](O) 6: Reserved 7: DBG_UTIF[2](IO)
7:4	**GPIO74_M**	GPIO74_MODE	**Selects GPIO 74 mode** 0:SPIC1_MOSI (O) 1: GPIO74 (IO) 2: UART RXD1 (I) 3: I2C1_SDA (IO) 4: PWM_CH2 (O) 5: ANTSEL[13](O) 6: Reserved 7: DBG_UTIF[1](IO)
3:0	**GPIO73_M**	GPIO73_MODE	**Selects GPIO 73 mode** 0: SPIC1_CLK (O) 1: GPIO73 (IO) 2: UART TXD1 (O) 3: I2C1_SCL (IO) 4: PWM_CH1 (O) 5: ANTSEL[12](O) 6: Reserved 7: DBG_UTIF[0](IO)

10211320 GPIO_MODE2 GPIO Mode Control Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO77_MODE				GPIO17_MODE				GPIO16_MODE				GPIO0_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO78_MODE				GPIO35_MODE				GPIO34_MODE				GPIO5_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**GPIO77_M**	GPIO77_MODE	**Selects GPIO 77 mode** 0: GPIO_D/GPIO77 (IO) 1: GPIO77 (IO) 2: Reserved 3: Reserved 4: PWM_CH5 (O) 5: ANTSEL[16] (O)

Bit(s)	Mnemonic	Name	Description
			6: Reserved 7: DBG_UTIF [4] (IO)
27:24	**GPIO17_M**	GPIO17_MODE	**Selects GPIO 17 mode** 0: I2S3_IN (I) 1: GPIO17 (IO) 2: SD_D2 (IO) 3: Reserved 4: IR_R (I) 5: ANTSEL[25] (O) 6: BT_ELNA_EN (O) 7: DBG_UTIF[11] (IO)
23:20	**GPIO16_M**	GPIO16_MODE	**Selects GPIO 16 mode** 0:I2S2_IN (I) 1: GPIO16 (IO) 2: SD_D3 (IO) 3: Reserved 4: IR_T (O) 5: ANTSEL[24] (O) 6: BT_EPA_EN (O) 7: DBG_UTIF[10] (IO)
19:16	**GPIO0_M**	GPIO0_MODE	**Selects GPIO 0 mode** 0: GPIO_A/GPIO0 (IO) 1: GPIO0 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
15:12	**GPIO78_M**	GPIO78_MODE	**Selects GPIO 78 mode** 0:WATCHDOG (O) 1: GPIO78 (IO) 2: Reserved 3: Reserved 4: PWM_CH6 5: Reserved 6: Reserved 7: DBG_UTIF[5]
11:8	**GPIO35_M**	GPIO35_MODE	**Selects GPIO 35 mode** 0: I2C0_SCL (IO) 1: GPIO35 (IO) 2: PCIE0_PAD_CLKREQ (IO) 3: PCIE1_PAD_CLKREQ (IO) 4: Reserved 5: ANTSEL[23] (O) 6: Reserved 7: Reserved
7:4	**GPIO34_M**	GPIO34_MODE	**Selects GPIO 34 mode** 0: I2C0_SDA (IO) 1: GPIO34 (IO)

Bit(s)	Mnemonic	Name	Description
			2: PCIE0_PAD_WAKE (IO) 3: PCIE1_PAD_WAKE (IO) 4: Reserved 5: ANTSEL[22] (O) 6: Reserved 7: EXT_BGCK (I)
3:0	**GPIO5_M**	GPIO5_MODE	**Selects GPIO 5 mode** 0: I2S_MCLK(O) 1: GPIO5 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: DBG_UTIF[17] (IO)

10211330 GPIO_MODE3 GPIO Mode Control Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO57_MODE				GPIO56_MODE				GPIO55_MODE				GPIO54_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO53_MODE				GPIO52_MODE				GPIO51_MODE				GPIO84_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**GPIO57_M**	GPIO57_MODE	**Selects GPIO 57 mode** [Analog PAD] MDI_RP_P1 0: I2C2_SCL (IO) 1: GPIO57 (IO) 2: UART_RTS1 (O) 3: TDM_OUT_MCLK (O) 4: Reserved 5: Reserved 6: Reserved 7: Reserved
27:24	**GPIO56_M**	GPIO56_MODE	**Selects GPIO 56 mode** [Analog PAD] MDI_TN_P1 0: I2C1_SDA (IO) 1: GPIO56 (IO) 2: UART_RXD1 (I) 3: TDM_IN_DATA (I) 4: Reserved 5: Reserved

Bit(s)	Mnemonic	Name	Description
			6: Reserved 7: Reserved
23:20	**GPIO55_M**	GPIO55_MODE	**Selects GPIO 55 mode** [Analog PAD] MDI_TP_P01 0: I2C1_SCL (IO) 1: GPIO55 (IO) 2: UART_TXD1 (O) 3: TDM_OUT_DATA (O) 4: Reserved 5: Reserved 6: Reserved 7: Reserved
19:16	**GPIO54_M**	GPIO54_MODE	**Selects GPIO 54 mode** [Analog PAD] MDI_RN_P0 0: UART_CTS2 (I) 1: GPIO54 (IO) 2: Reserved 3: PWM_CH4 (O) 4: Reserved 5: Reserved 6: Reserved 7: Reserved
15:12	**GPIO53_M**	GPIO53_MODE	**Selects GPIO 53 mode** [Analog PAD] MDI_RP_P0 0: UART_RTS2 (O) 1: GPIO53 (IO) 2: Reserved 3: PWM_CH3 (O) 4: Reserved 5: Reserved 6: Reserved 7: Reserved
11:8	**GPIO52_M**	GPIO52_MODE	**Selects GPIO 52 mode** [Analog PAD] MDI_TN_P0 0: UART_RXD2 (I) 1: GPIO52 (IO) 2: Reserved 3: PWM_CH2 (O) 4: Reserved 5: Reserved 6: Reserved 7: Reserved
7:4	**GPIO51_M**	GPIO51_MODE	**Selects GPIO 51 mode** [Analog PAD] MDI_TP_P0 0: UART_TXD2 (O) 1: GPIO51 (IO) 2: Reserved 3: PWM_CH1 (O) 4: Reserved 5: Reserved 6: Reserved

Bit(s)	Mnemonic	Name	Description
			7: Reserved
3:0	**GPIO84_M**	GPIO84_MODE	**Selects GPIO 84 mode** 0: PCIE1_PAD_PERST (O) 1: GPIO84 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved

10211340 GPIO_MODE4 GPIO Mode Control Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO65_MODE				GPIO64_MODE				GPIO63_MODE				GPIO62_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO61_MODE				GPIO60_MODE				GPIO59_MODE				GPIO58_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**GPIO65_M**	GPIO65_MODE	**Selects GPIO 65 mode** [Analog PAD] MDI_RP_P3 0: ESW_RXD[0] (IO) 1: GPIO65 (IO) 2: G1_RXD[0] (IO) 3: Reserved 4: SPIC0_MISO (I) 5: Reserved 6: Reserved 7: Reserved
27:24	**GPIO64_M**	GPIO64_MODE	**Selects GPIO 64 mode** [Analog PAD] MDI_TN_P3 0: ESW_TXC (IO) 1: GPIO64 (IO) 2: G1_TXC (IO) 3: Reserved 4: SPIC0_MOSI (O) 5: Reserved 6: Reserved 7: Reserved
23:20	**GPIO63_M**	GPIO63_MODE	**Selects GPIO 63 mode** [Analog PAD] MDI_TP_P3 0: ESW_TXEN (IO) 1: GPIO63 (IO)

Bit(s)	Mnemonic	Name	Description
			2: G1_TXEN (IO) 3: Reserved 4: SPIC0_CLK (O) 5: Reserved 6: Reserved 7: Reserved
19:16	**GPIO62_M**	GPIO62_MODE	**Selects GPIO 62 mode** [Analog PAD] MDI_TN_P2 0: ESW_TXD[3] (IO) 1: GPIO62 (IO) 2: G1_TXD[3] (IO) 3: TDM_IN_WS (O) 4: UART_CTS2_N (I) 5: UART_RXD4 (I) 6: Reserved 7: Reserved
15:12	**GPIO61_M**	GPIO61_MODE	**Selects GPIO 61 mode** [Analog PAD] MDI_TP_P2 0: ESW_TXD[2] (IO) 1: GPIO61 (IO) 2: G1_TXD[2] (IO) 3: TDM_IN_BCLK (O) (O) 4: UART_RTS2_N (O) 5: UART_TXD4 (O) 6: Reserved 7: Reserved
11:8	**GPIO60_M**	GPIO60_MODE	**Selects GPIO 60 mode** [Analog PAD] MDI_RN_P2 0: ESW_TXD[1] (IO) 1: GPIO60 (IO) 2: G1_TXD[1] (IO) 3: TDM_IN_MCLK (O) 4: UART_RXD2 (I) 5: IR_R (I) 6: Reserved 7: Reserved
7:4	**GPIO59_M**	GPIO59_MODE	**Selects GPIO 59 mode** [Analog PAD] MDI_RP_P2 0: ESW_TXD[0] (IO) 1: GPIO59 (IO) 2: G1_TXD[0] (IO) 3: TMD_OUT_WS (O) 4: UART_TXD2 (O) 5: IR_T (O) 6: Reserved 7: Reserved
3:0	**GPIO58_M**	GPIO58_MODE	**Selects GPIO 58 mode** [Analog PAD] MDI_RN_P1 0: I2C2_SDA (IO) 1: GPIO58 (IO) 2: UART_CTS1 (I)

Bit(s)	Mnemonic	Name	Description
			3: TDM_OUT_BCLK (O) 4: Reserved 5: Reserved 6: Reserved 7: Reserved

10211350 GPIO_MODE5 GPIO Mode Control Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO83_MODE				GPIO9_MODE				GPIO8_MODE				GPIO70_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO69_MODE				GPIO68_MODE				GPIO67_MODE				GPIO66_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**GPIO83_M**	GPIO83_MODE	**Selects GPIO 83 mode** 0: PCIE0_PAD_PERST (O) 1: GPIO83 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7:Reserved
27:24	**GPIO9_M**	GPIO9_MODE	**Selects GPIO 9 mode** 0: SPI_HOLD (IO) 1: GPIO9 (IO) 2: SNFI_HOLD (IO) 3: TDM_OUT_BCLK (O) 4: Reserved 5: Reserved 6: FPC_DL_STS (O) 7: Reserved
23:20	**GPIO8_M**	GPIO8_MODE	**Selects GPIO 8 mode** 0: SPI_WP (IO) 1: GPIO8 (IO) 2: SNFI_WP (IO) 3: TDM_OUT_MCLK (O) 4: Reserved 5: Reserved 6: FPC_DAT_STS (O) 7: Reserved
19:16	**GPIO70_M**	GPIO70_MODE	**Selects GPIO 70 mode**

Bit(s)	Mnemonic	Name	Description
			[Analog PAD] MDI_TN_P4 0: ESW_RXC (IO) 1: GPIO70 (IO) 2: G1_RXCV (IO) 3: PWM_CH7 (O) 4: SPIC1_CS (O) 5: Reserved 6: Reserved 7: Reserved
15:12	**GPIO69_M**	GPIO69_MODE	**Selects GPIO 69 mode** [Analog PAD] MDI_TP_P4 0: ESW_RXDV (IO) 1: GPIO69 (IO) 2: G1_RXDV (IO) 3: PWM_CH6 (O) 4: SPIC1_MISO (I) 5: Reserved 6: Reserved 7: Reserved
11:8	**GPIO68_M**	GPIO68_MODE	**Selects GPIO 68 mode** [Analog PAD] MDI_RN_P4 0: ESW_RXD[3] (IO) 1: GPIO68 (IO) 2: G1_RXD[3] (IO) 3: PWM_CH5 (O) 4: SPIC1_MOSI (O) 5: Reserved 6: Reserved 7: Reserved
7:4	**GPIO67_M**	GPIO67_MODE	**Selects GPIO 67 mode** [Analog PAD] MDI_RP_P4 0: ESW_RXD[2] (IO) 1: GPIO67 (IO) 2: G1_RXD[2] (IO) 3: PWM_CH4 (O) 4: SPIC1_CLK (O) 5: Reserved 6: Reserved 7: Reserved
3:0	**GPIO66_M**	GPIO66_MODE	**Selects GPIO 66 mode** [Analog PAD] MDI_RN_P3 0: ESW_RXD[1] (IO) 1: GPIO66 (IO) 2: G1_RXD[1] (IO) 3: Reserved 4: SPIC0_CS (O) 5: Reserved 6: Reserved 7: Reserved

10211360 GPIO_MODE6 GPIO Mode Control Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV				GPIO90_MODE				GPIO89_MODE				GPIO88_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO87_MODE				GPIO86_MODE				GPIO85_MODE				GPIO102_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		RESV	**Reserved**
27:24	**GPIO90_M**	GPIO90_MODE	**Selects GPIO 90 mode** [Analog PAD] PAD_AUXIN3 0: I2C2_SDA (IO) 1: GPIO90 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
23:20	**GPIO89_M**	GPIO89_MODE	**Selects GPIO 89 mode** [Analog PAD] PAD_AUXIN2 0: I2C2_SCL (IO) 1: GPIO89 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
19:16	**GPIO88_M**	GPIO88_MODE	**Selects GPIO 88 mode** [Analog PAD] PAD_AUXIN1 0: I2C1_SDA (IO) 1: GPIO88 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
15:12	**GPIO87_M**	GPIO87_MODE	**Selects GPIO 87 mode** [Analog PAD] PAD_AUXIN0 0: I2C1_SCL (IO) 1: GPIO87 (IO) 2: Reserved 3: Reserved

Bit(s)	Mnemonic	Name	Description
			4: Reserved 5: Reserved 6: Reserved 7: Reserved
11:8	**GPIO86_M**	GPIO86_MODE	**Selects GPIO 86 mode** 0: EPHY_LED0_N (O) 1: GPIO86 (IO) 2: Reserved 3: Reserved 4: CPUM_HW_SEL (I) 5: Reserved 6: FPC_CTL[0] (I) 7: JTRST_N (I)
7:4	**GPIO85_M**	GPIO85_MODE	**Selects GPIO 85 mode** 0: WLED_N (IO) 1: GPIO85 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
3:0	**GPIO102_M**	GPIO102_MODE	**Selects GPIO 102 mode** 0: GPIO_E/GPIO102 (IO) 1: GPIO102 (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: ANTSEL [11] (O) 7: FPC_DATA[7] (I)

10211370 GPIO_MODE7 GPIO Mode Control Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		RESV	**Reserved**

10211380 GPIO_MODE8 GPIO Mode Control Register 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	GPIO97_MODE				GPIO96_MODE				GPIO95_MODE				GPIO22_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**GPIO97_M**	GPIO97_MODE	**Selects GPIO 97 mode** 0: PWM_CH3 (O) 1: GPIO97 (IO) 2: UART_TXD4 (O) 3: Reserved 4: AICE_TCKC (I) 5: ANTSEL[6] (O) 6: FPC_DATA[2] (I) 7: W_JTCLK (I)
27:24	**GPIO96_M**	GPIO96_MODE	**Selects GPIO 96 mode** 0: PWM_CH2 (O) 1: GPIO96 (IO) 2: UART_CTS4 (I) 3: UART_RXD2 (I) 4: CPUM_CK_XI (I) 5: ANTSEL[5] (O) 6: FPC_DATA[1] (I) 7: W_DBGACK (O)
23:20	**GPIO95_M**	GPIO95_MODE	**Selects GPIO 95 mode** 0: PWM_CH1 (O) 1: GPIO95 (IO) 2: UART_RTS4 (O) 3: UART_TXD2 (O) 4: CPUM[3] (IO) 5: ANTSEL[4] (O) 6: FPC_DATA[0] (I) 7: W_DBGIN (I)
19:16	**GPIO22_M**	GPIO22_MODE	**Selects GPIO 22 mode** 0: GPIO_B/GPIO22 (IO) 1: GPIO22 (IO) 2: Reserved 3: TSF_INTR (I) 4: Reserved 5: Reserved 6: ANTSEL[17] (O) 7: DBG_UTIF[16] (IO)
15:0		RESV	**Reserved**

10211390 GPIO_MODE9 GPIO Mode Control Register 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO94_MODE				GPIO93_MODE				GPIO92_MODE				GPIO91_MODE			

Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO101_MODE				GPIO100_MODE				GPIO99_MODE				GPIO98_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**GPIO94_M**	GPIO94_MODE	**Selects GPIO 94 mode** 0: UART_CTS4 (I) 1: GPIO94 (IO) 2: EPHY_LED4_N (O) 3: DFD_TMS (I) 4: CPUM[2] (IO) 5: ANTSEL[3] (O) 6: FPC_CTL[3] (I) 7: JTMS (IO)
27:24	**GPIO93_M**	GPIO93_MODE	**Selects GPIO 93 mode** 0: UART_RTS4 (O) 1: GPIO93 (IO) 2: EPHY_LED3_N (O) 3: DFD_TCK (I) 4: CPUM[1] (IO) 5: ANTSEL[2] (O) 6: FPC_CTL[2] (I) 7: JTCLK (I)
23:20	**GPIO92_M**	GPIO92_MODE	**Selects GPIO 92 mode** 0: UART_RXD4 (I) 1: GPIO92 (IO) 2: EPHY_LED2_N (O) 3: DFD_TDO (O) 4: CPUM[0] (IO) 5: ANTSEL[1] (O) 6: FPC_CTL[1] (I) 7: JTDO (O)
19:16	**GPIO91_M**	GPIO91_MODE	**Selects GPIO 91 mode** 0: UART_TXD4 (O) 1: GPIO91 (IO) 2: EPHY_LED1_N (O) 3: DFD_TDI (I) 4: CPUM_2B_SEL (I) 5: ANTSEL[0] (O) 6: FPC_CK_XI (I) 7: JTDI (I)
15:12	**GPIO101_M**	GPIO101_MODE	**Selects GPIO 101 mode** 0: PWM_CH7 (O) 1: GPIO101 (IO) 2: Reserved 3: Reserved 4: Reserved 5: ANTSEL[10] (O)

Bit(s)	Mnemonic	Name	Description
			6: FPC_DATA[6] (I) 7: DBG_UART_TXD (O)
11:8	**GPIO100_M**	GPIO100_MODE	**Selects GPIO 100 mode** 0: PWM_CH6 (O) 1: GPIO100 (IO) 2: Reserved 3: IR_R (I) 4: Reserved 5: ANTSEL[9] (O) 6: FPC_DATA[5] (I) 7: W_JTRST_N (I)
7:4	**GPIO99_M**	GPIO99_MODE	**Selects GPIO 99 mode** 0: PWM_CH5 (O) 1: GPIO99 (IO) 2: Reserved 3: IR_T (O) 4: AICE_TMSC (IO) 5: ANTSEL[8] (O) 6: FPC_DATA[4] (I) 7: W_JTMS (I)
3:0	**GPIO98_M**	GPIO98_MODE	**Selects GPIO 98 mode** 0: PWM_CH4 (O) 1: GPIO98 (IO) 2: UART_RXD4 (I) 3: Reserved 4: Reserved 5: ANTSEL[7] (O) 6: FPC_DATA[3] (I) 7: W_JTDI (I)

102113A0 GPIO_MODE10 GPIO Mode Control Register 10 00000000

Ar3	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO4_MODE				GPIO3_MODE				GPIO2_MODE				GPIO1_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO82_MODE				GPIO81_MODE				GPIO80_MODE				GPIO79_MODE			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28	**GPIO4_M**	GPIO4_MODE	**Selects GPIO 4 mode** 0: I2S_WS_OUT (O) 1: GPIO4 (IO) 2: UART_RXD2 (I) 3: i2S_WS_IN (I) 4: Reserved

Bit(s)	Mnemonic	Name	Description
			5: Reserved 6: Reserved 7: Reserved
27:24	**GPIO3_M**	GPIO3_MODE	**Selects GPIO 3 mode** 0: I2S_BCLK_OUT (O) 1: GPIO3 (IO) 2: UART_TXD2 (O) 3: i2S_BCLK_IN (I) 4: Reserved 5: Reserved 6: Reserved 7: Reserved
23:20	**GPIO2_M**	GPIO2_MODE	**Selects GPIO 2 mode** 0: I2S1_OUT (O)) 1: GPIO2 (IO) 2: UART_CTS2_N (I) 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
19:16	**GPIO1_M**	GPIO1_MODE	**Selects GPIO 1 mode** 0: I2S1_IN (I) 1: GPIO1 (IO) 2: UART_RTS2_N (O) 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
15:12	**GPIO82_M**	GPIO82_MODE	**Selects GPIO 82 mode** 0: UART_RXD3 (I) 1: GPIO82 (IO) 2: SPDIF_R (I) 3: SPIC0_MOSI (O) 4: PWM_CH7 (O) 5: ANTSEL[21] (O) 6: Reserved 7: DBG_UTIF[9] (IO)
11:8	**GPIO81_M**	GPIO81_MODE	**Selects GPIO 81 mode** 0: UART_TXD3 (O) 1: GPIO81 (IO) 2: SPDIF_T (O) 3: SPIC0_CLK (O) 4: PWM_CH6 (O) 5: ANTSEL[20] (O) 6: Reserved 7: DBG_UTIF[8] (IO)
7:4	**GPIO80_M**	GPIO80_MODE	**Selects GPIO 80 mode** 0: UART_CTS3 (I)

Bit(s)	Mnemonic	Name	Description
			1: GPIO80 (IO) 2: Reserved 3: SPIC0_CS (O) 4: CPIE0_PAD_CLKREQ (IO) 5: ANTSEL[19] (O) 6: Reserved 7: DBG_UTIF[7] (IO)
3:0	**GPIO79_M**	GPIO79_MODE	**Selects GPIO 79 mode** 0: UART_RTS3 (O) 1: GPIO79 (IO) 2: Reserved 3: SPIC0_MISO (I) 4: PCIE0_PAD_WAKE (IO) 5: ANTSEL[18] (O) 6: Reserved 7: DBG_UTIF[6] (IO)

1.9 AP DMA

1.9.1 Introduction

There is always a DMA in a platform. The purpose of DMA is performing data transfer between different slaves. There are several slaves in a platform, and the major one is external memory, e.g. DRAM. There are also internal SRAM and some slave ports for the peripheral to transfer data. For saving software efforts, DMA delivers a virtual FIFO concept to help the software maintain read and write pointer when the software accesses data from a ring buffer. As the bus goes more and more efficient, the old DMA still utilizes the AHB bus protocol and may decrease its performance. Another problem is that when the old DMA meets byte alignment addresses or byte alignment sizes, it will need some software efforts to help solve head and tail non word alignment problems or let DMA to simply issues single-1-byte requests to conquer the byte-alignment problem. This will harm the overall system because the single-1-byte transaction is quite inefficient. Now the DMA efficiency is now improved by increasing its bus efficiency, including data buffering and overcoming byte alignment problems.

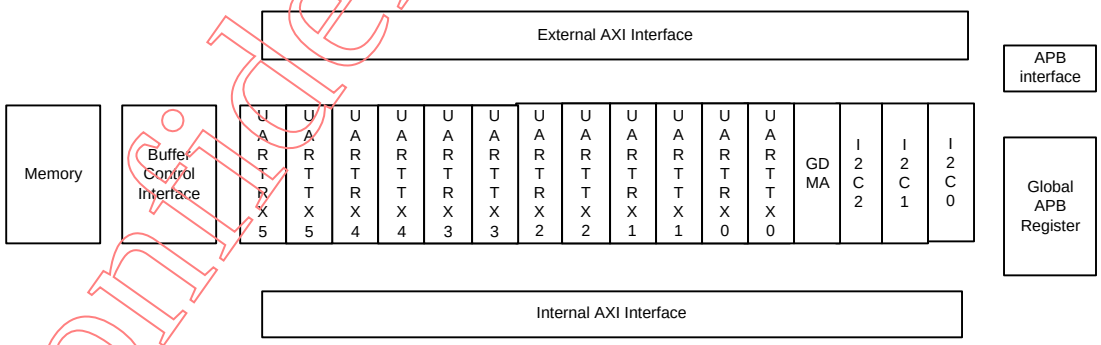
1.9.2 Features

APDMA has the following DMA engines.

- I2C DMA engine*3
- UART TX DMA engine*6
- UART RX DMA engine*6
- GDMA engine*1

1.9.3 Block Diagram

There are total 18 channels in DMA. The external AXI interface is connected to the peripheral AXI bus fabric to provide external memory access ability. The internal AXI interface is also connected to the peripheral AXI bus fabric and is re-directed to related peripherals, e.g. I2C and UART. A memory block is used as a buffer which makes the transfer on the AXI bus interface more efficient. An APB interface is used to program registers for both global registers and local registers existing in every individual DMA channel.



1.9.4 Register Definition

Module name: AP_DMA Base address: (+11000000h)

Address	Name	Width	Register Function
11000000	AP_DMA_GLOBAL_INT_FLAG	32	**AP DMA Global Interrupt Flag Register**
11000004	AP_DMA_GLOBAL_RST	32	**AP DMA Reset Register**
11000008	AP_DMA_GLOBAL_RUNNING_STATUS	32	**AP DMA Global Running Status Register** Indicates if each DMA engine is running or not.
1100000C	AP_DMA_GLOBAL_SLOW_DOWN	32	**AP DMA AXI Slow Down Register**
11000010	AP_DMA_GLOBAL_SEC_EN	32	**AP DMA Security Enable Register**
11000014	AP_DMA_GLOBAL_GSEC_EN	32	**AP DMA Global Security Enable Register**
11000018	AP_DMA_GLOBAL_VIO_DBG1	32	**AP DMA Security Latch Address Register**
1100001C	AP_DMA_GLOBAL_VIO_DBG0	32	**AP DMA Global Security Abort Register**
11000020	AP_DMA_GDMA0_SEC_EN	32	**AP GDMA0 Security Enable Register**
11000024	AP_DMA_I2C0_SEC_EN	32	**AP I2C0 Security Enable Register**
11000028	AP_DMA_I2C1_SEC_EN	32	**AP I2C1 Security Enable Register**
1100002C	AP_DMA_I2C2_SEC_EN	32	**AP I2C2 Security Enable Register**
11000030	AP_DMA_UART0_TX_SEC_EN	32	**AP UART0 TX Security Enable Register**
11000034	AP_DMA_UART0_RX_SEC_EN	32	**AP UART0 RX Security Enable Register**
11000038	AP_DMA_UART1_TX_SEC_EN	32	**AP UART1 TX Security Enable Register**
1100003C	AP_DMA_UART1_RX_SEC_EN	32	**AP UART1 RX Security Enable Register**
11000040	AP_DMA_UART2_TX_SEC_EN	32	**AP UART2 TX Security Enable Register**
11000044	AP_DMA_UART2_RX_SEC_EN	32	**AP UART2 RX Security Enable Register**
11000048	AP_DMA_UART3_TX_SEC_EN	32	**AP UART3 TX Security Enable Register**

1100004C	AP_DMA_UART3_RX_SEC_EN	32	AP UART3 RX Security Enable Register
11000050	AP_DMA_UART4_TX_SEC_EN	32	AP UART4 TX Security Enable Register
11000054	AP_DMA_UART4_RX_SEC_EN	32	AP UART4 RX Security Enable Register
11000058	AP_DMA_UART5_TX_SEC_EN	32	AP UART5 TX Security Enable Register
1100005C	AP_DMA_UART5_RX_SEC_EN	32	AP UART5 RX Security Enable Register
11000070	AP_DMA_MD_INT_EN	32	AP DMA MD Interrupt Enable Register
11000074	AP_DMA_GLOBAL_DOMAIN_CFG0	32	AP DMA Domain Configuration Register 0
1100007C	FPC	32	FPC
11000080	AP_DMA_G_DMA_0_INT_FLAG	32	General DMA Interrupt Flag Register
11000084	AP_DMA_G_DMA_0_INT_EN	32	General DMA Interrupt Enable Register
11000088	AP_DMA_G_DMA_0_EN	32	General DMA Enable Register
1100008C	AP_DMA_G_DMA_0_RST	32	General DMA Reset Register
11000090	AP_DMA_G_DMA_0_STOP	32	General DMA Enable Register
11000094	AP_DMA_G_DMA_0_FLUSH	32	General DMA Flush Register
11000098	AP_DMA_G_DMA_0_CON	32	General DMA Control Register
1100009C	AP_DMA_G_DMA_0_SRC_ADDR	32	General DMA SRC Address Register
110000A0	AP_DMA_G_DMA_0_DST_ADDR	32	General DMA DST Address Register
110000A4	AP_DMA_G_DMA_0_LEN1	32	General DMA Transfer Length 1 Register
110000A8	AP_DMA_G_DMA_0_LEN2	32	General DMA Transfer Length 2 Register
110000AC	AP_DMA_G_DMA_0_JUMP_ADDR	32	General DMA Jump Address Register
110000B0	AP_DMA_G_DMA_0_INT_BUF_SIZE	32	General DMA Internal Buffer Size Register
110000B4	AP_DMA_G_DMA_0_CONNECT	32	General DMA Connect Register
110000B8	AP_DMA_G_DMA_0_AXIATTR	32	General DMA AXI Attribute Register

110000D0	AP_DMA_G_DMA_0_DEBUG_STATUS_00	32	General DMA Debug Status 00 Register
11000100	AP_DMA_I2C_0_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000104	AP_DMA_I2C_0_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000108	AP_DMA_I2C_0_EN	32	Peripheral DMA Enable Register
1100010C	AP_DMA_I2C_0_RST	32	Peripheral DMA Reset Register
11000110	AP_DMA_I2C_0_STOP	32	Peripheral DMA Enable Register
11000114	AP_DMA_I2C_0_FLUSH	32	Peripheral DMA Flush Register
11000118	AP_DMA_I2C_0_CON	32	Peripheral DMA Control Register
1100011C	AP_DMA_I2C_0_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000120	AP_DMA_I2C_0_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000124	AP_DMA_I2C_0_TX_LEN	32	Peripheral DMA Transfer Length Register
11000128	AP_DMA_I2C_0_RX_LEN	32	Peripheral DMA Transfer Length Register
11000138	AP_DMA_I2C_0_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
11000150	AP_DMA_I2C_0_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
11000180	AP_DMA_I2C_1_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000184	AP_DMA_I2C_1_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000188	AP_DMA_I2C_1_EN	32	Peripheral DMA Enable Register
1100018C	AP_DMA_I2C_1_RST	32	Peripheral DMA Reset Register
11000190	AP_DMA_I2C_1_STOP	32	Peripheral DMA Enable Register
11000194	AP_DMA_I2C_1_FLUSH	32	Peripheral DMA Flush Register
11000198	AP_DMA_I2C_1_CON	32	Peripheral DMA Control Register
1100019C	AP_DMA_I2C_1_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
110001A0	AP_DMA_I2C_1_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
110001A4	AP_DMA_I2C_1_TX_LEN	32	Peripheral DMA Transfer Length Register
110001A8	AP_DMA_I2C_1_RX_LEN	32	Peripheral DMA Transfer Length Register

110001B8	AP_DMA_I2C_1_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
110001D0	AP_DMA_I2C_1_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
11000200	AP_DMA_I2C_2_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
11000204	AP_DMA_I2C_2_INT_EN	32	Peripheral DMA Interrupt Enable Register
11000208	AP_DMA_I2C_2_EN	32	Peripheral DMA Enable Register
1100020C	AP_DMA_I2C_2_RST	32	Peripheral DMA Reset Register
11000210	AP_DMA_I2C_2_STOP	32	Peripheral DMA Enable Register
11000214	AP_DMA_I2C_2_FLUSH	32	Peripheral DMA Flush Register
11000218	AP_DMA_I2C_2_CON	32	Peripheral DMA Control Register
1100021C	AP_DMA_I2C_2_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000220	AP_DMA_I2C_2_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
11000224	AP_DMA_I2C_2_TX_LEN	32	Peripheral DMA Transfer Length Register
11000228	AP_DMA_I2C_2_RX_LEN	32	Peripheral DMA Transfer Length Register
11000238	AP_DMA_I2C_2_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
11000250	AP_DMA_I2C_2_DEBUG_STATUS_00	32	Peripheral DMA Debug Status 00 Register
11000280	AP_DMA_UART_0_TX_INT_FLAG	32	UART0 TX Virtual FIFO Interrupt Flag Register
11000284	AP_DMA_UART_0_TX_INT_EN	32	UART0 TX Virtual FIFO Interrupt Enable Register
11000288	AP_DMA_UART_0_TX_EN	32	UART0 TX Virtual FIFO Enable Register
1100028C	AP_DMA_UART_0_TX_RST	32	UART0 TX Virtual FIFO Reset Register
11000290	AP_DMA_UART_0_TX_STOP	32	UART0 TX Virtual FIFO Enable Register
11000294	AP_DMA_UART_0_TX_FLUSH	32	UART0 TX Virtual FIFO Flush Register
1100029C	AP_DMA_UART_0_TX_VFF_ADDR	32	UART0 TX Virtual FIFO Base Address Register
110002A4	AP_DMA_UART_0_TX_VFF_LEN	32	UART0 TX Virtual FIFO Length Register

110002A8	AP_DMA_UART_0_TX_VFF_THRE	32	UART0 TX Virtual FIFO Threshold Register
110002AC	AP_DMA_UART_0_TX_VFF_WPT	32	UART0 TX Virtual FIFO Write Pointer Register
110002B0	AP_DMA_UART_0_TX_VFF_RPT	32	UART0 TX Virtual FIFO Read Pointer Register
110002B8	AP_DMA_UART_0_TX_INT_BUF_SIZE	32	UART0 Tx Internal Buffer Size Register
110002BC	AP_DMA_UART_0_TX_VFF_VALID_SIZE	32	UART0 Tx Virtual FIFO Valid Size Register
110002C0	AP_DMA_UART_0_TX_VFF_LEFT_SIZE	32	UART0 Tx Virtual FIFO Left Size Register
110002D0	AP_DMA_UART_0_TX_DEBUG_STATUS_00	32	UART0 Tx Debug Status 00
110002D8	AP_DMA_UART_0_TX_VFF_WPT_VALID	32	UART0 TX Virtual FIFO Write Pointer Register by HW Control
110002E0	AP_DMA_UART_0_TX_FLUSH_ACT	32	UART0 TX Virtual FIFO Flush Status Register
110002E4	AP_DMA_UART_0_TX_HW_FLUSH	32	UART0 TX Virtual FIFO HW Flush Register
11000300	AP_DMA_UART_0_RX_INT_FLAG	32	UART0 RX Virtual FIFO Interrupt Flag Register
11000304	AP_DMA_UART_0_RX_INT_EN	32	UART0 RX Virtual FIFO Interrupt Enable Register
11000308	AP_DMA_UART_0_RX_EN	32	UART0 RX Virtual FIFO Enable Register
1100030C	AP_DMA_UART_0_RX_RST	32	UART0 RX Virtual FIFO Reset Register
11000310	AP_DMA_UART_0_RX_STOP	32	UART0 RX Virtual FIFO Enable Register
11000314	AP_DMA_UART_0_RX_FLUSH	32	UART0 RX Virtual FIFO Flush Register
1100031C	AP_DMA_UART_0_RX_VFF_ADDR	32	UART0 RX Virtual FIFO Base Address Register
11000324	AP_DMA_UART_0_RX_VFF_LEN	32	UART0 RX Virtual FIFO Length Register
11000328	AP_DMA_UART_0_RX_VFF_THRE	32	UART0 RX Virtual FIFO Threshold Register
1100032C	AP_DMA_UART_0_RX_VFF_WPT	32	UART0 RX Virtual FIFO Write Pointer Register

11000330	AP_DMA_UART_0_RX_VFF_RPT	32	UART0 RX Virtual FIFO Read Pointer Register
11000334	AP_DMA_UART_0_RX_FLOW_CTRL_THRE	32	UART0 RX Virtual FIFO Flow Control Threshold
11000338	AP_DMA_UART_0_RX_INT_BUF_SIZE	32	UART0 Rx Internal Buffer Size Register
1100033C	AP_DMA_UART_0_RX_VFF_VALID_SIZE	32	UART0 Rx Virtual FIFO Valid Size Register
11000340	AP_DMA_UART_0_RX_VFF_LEFT_SIZE	32	UART0 Rx Virtual FIFO Left Size Register
11000350	AP_DMA_UART_0_RX_DEBUG_STATUS_00	32	UART0 Rx Debug Status 00
11000380	AP_DMA_UART_1_TX_INT_FLAG	32	UART1 TX Virtual FIFO Interrupt Flag Register
11000384	AP_DMA_UART_1_TX_INT_EN	32	UART1 TX Virtual FIFO Interrupt Enable Register
11000388	AP_DMA_UART_1_TX_EN	32	UART1 TX Virtual FIFO Enable Register
1100038C	AP_DMA_UART_1_TX_RST	32	UART1 TX Virtual FIFO Reset Register
11000390	AP_DMA_UART_1_TX_STOP	32	UART1 TX Virtual FIFO Enable Register
11000394	AP_DMA_UART_1_TX_FLUSH	32	UART1 TX Virtual FIFO Flush Register
1100039C	AP_DMA_UART_1_TX_VFF_ADDR	32	UART1 TX Virtual FIFO Base Address Register
110003A4	AP_DMA_UART_1_TX_VFF_LEN	32	UART1 TX Virtual FIFO Length Register
110003A8	AP_DMA_UART_1_TX_VFF_THRE	32	UART1 TX Virtual FIFO Threshold Register
110003AC	AP_DMA_UART_1_TX_VFF_WPT	32	UART1 TX Virtual FIFO Write Pointer Register
110003B0	AP_DMA_UART_1_TX_VFF_RPT	32	UART1 TX Virtual FIFO Read Pointer Register
110003B8	AP_DMA_UART_1_TX_INT_BUF_SIZE	32	UART1 Tx Internal Buffer Size Register
110003BC	AP_DMA_UART_1_TX_VFF_VALID_SIZE	32	UART1 Tx Virtual FIFO Valid Size Register
110003C0	AP_DMA_UART_1_TX_VFF_LEFT_SIZE	32	UART1 Tx Virtual FIFO Left Size Register

110003D0	AP_DMA_UART_1_TX_DEBUG_STATUS_00	32	UART1 Tx Debug Status 00
110003D8	AP_DMA_UART_1_TX_VFF_WPT_VALID	32	UART1 TX Virtual FIFO Write Pointer Register by HW Control
110003E0	AP_DMA_UART_1_TX_FLUSH_ACT	32	UART1 TX Virtual FIFO Flush Status Register
110003E4	AP_DMA_UART_1_TX_HW_FLUSH	32	UART1 TX Virtual FIFO HW Flush Register
11000400	AP_DMA_UART_1_RX_INT_FLAG	32	UART1 RX Virtual FIFO Interrupt Flag Register
11000404	AP_DMA_UART_1_RX_INT_EN	32	UART1 RX Virtual FIFO Interrupt Enable Register
11000408	AP_DMA_UART_1_RX_EN	32	UART1 RX Virtual FIFO Enable Register
1100040C	AP_DMA_UART_1_RX_RST	32	UART1 RX Virtual FIFO Reset Register
11000410	AP_DMA_UART_1_RX_STOP	32	UART1 RX Virtual FIFO Enable Register
11000414	AP_DMA_UART_1_RX_FLUSH	32	UART1 RX Virtual FIFO Flush Register
1100041C	AP_DMA_UART_1_RX_VFF_ADDR	32	UART1 RX Virtual FIFO Base Address Register
11000424	AP_DMA_UART_1_RX_VFF_LEN	32	UART1 RX Virtual FIFO Length Register
11000428	AP_DMA_UART_1_RX_VFF_THRE	32	UART1 RX Virtual FIFO Threshold Register
1100042C	AP_DMA_UART_1_RX_VFF_WPT	32	UART1 RX Virtual FIFO Write Pointer Register
11000430	AP_DMA_UART_1_RX_VFF_RPT	32	UART1 RX Virtual FIFO Read Pointer Register
11000434	AP_DMA_UART_1_RX_FLOW_CTRL_THRE	32	UART1 RX Virtual FIFO Flow Control Threshold
11000438	AP_DMA_UART_1_RX_INT_BUF_SIZE	32	UART1 Rx Internal Buffer Size Register
1100043C	AP_DMA_UART_1_RX_VFF_VALID_SIZE	32	UART1 Rx Virtual FIFO Valid Size Register
11000440	AP_DMA_UART_1_RX_VFF_LEFT_SIZE	32	UART1 Rx Virtual FIFO Left Size Register
11000450	AP_DMA_UART_1_RX_DEBUG_STATUS_00	32	UART1 Rx Debug Status 00

11000480	AP_DMA_UART_2_TX_INT_FLAG	32	UART2 TX Virtual FIFO Interrupt Flag Register
11000484	AP_DMA_UART_2_TX_INT_EN	32	UART2 TX Virtual FIFO Interrupt Enable Register
11000488	AP_DMA_UART_2_TX_EN	32	UART2 TX Virtual FIFO Enable Register
1100048C	AP_DMA_UART_2_TX_RST	32	UART2 TX Virtual FIFO Reset Register
11000490	AP_DMA_UART_2_TX_STOP	32	UART2 TX Virtual FIFO Enable Register
11000494	AP_DMA_UART_2_TX_FLUSH	32	UART2 TX Virtual FIFO Flush Register
1100049C	AP_DMA_UART_2_TX_VFF_ADDR	32	UART2 TX Virtual FIFO Base Address Register
110004A4	AP_DMA_UART_2_TX_VFF_LEN	32	UART2 TX Virtual FIFO Length Register
110004A8	AP_DMA_UART_2_TX_VFF_THRE	32	UART2 TX Virtual FIFO Threshold Register
110004AC	AP_DMA_UART_2_TX_VFF_WPT	32	UART2 TX Virtual FIFO Write Pointer Register
110004B0	AP_DMA_UART_2_TX_VFF_RPT	32	UART2 TX Virtual FIFO Read Pointer Register
110004B8	AP_DMA_UART_2_TX_INT_BUF_SIZE	32	UART2 Tx Internal Buffer Size Register
110004BC	AP_DMA_UART_2_TX_VFF_VALID_SIZE	32	UART2 Tx Virtual FIFO Valid Size Register
110004C0	AP_DMA_UART_2_TX_VFF_LEFT_SIZE	32	UART2 Tx Virtual FIFO Left Size Register
110004D0	AP_DMA_UART_2_TX_DEBUG_STATUS_00	32	UART2 Tx Debug Status 00
110004D8	AP_DMA_UART_2_TX_VFF_WPT_VALID	32	UART2 TX Virtual FIFO Write Pointer Register by HW Control
110004E0	AP_DMA_UART_2_TX_FLUSH_ACT	32	UART2 TX Virtual FIFO Flush Status Register
110004E4	AP_DMA_UART_2_TX_HW_FLUSH	32	UART2 TX Virtual FIFO HW Flush Register
11000500	AP_DMA_UART_2_RX_INT_FLAG	32	UART2 RX Virtual FIFO Interrupt Flag Register
11000504	AP_DMA_UART_2_RX_INT_EN	32	UART2 RX Virtual FIFO Interrupt Enable Register
11000508	AP_DMA_UART_2_RX_EN	32	UART2 RX Virtual FIFO Enable Register

1100050C	AP_DMA_UART_2_RX_RST	32	UART2 RX Virtual FIFO Reset Register
11000510	AP_DMA_UART_2_RX_STOP	32	UART2 RX Virtual FIFO Enable Register
11000514	AP_DMA_UART_2_RX_FLUSH	32	UART2 RX Virtual FIFO Flush Register
1100051C	AP_DMA_UART_2_RX_VFF_ADDR	32	UART2 RX Virtual FIFO Base Address Register
11000524	AP_DMA_UART_2_RX_VFF_LEN	32	UART2 RX Virtual FIFO Length Register
11000528	AP_DMA_UART_2_RX_VFF_THRE	32	UART2 RX Virtual FIFO Threshold Register
1100052C	AP_DMA_UART_2_RX_VFF_WPT	32	UART2 RX Virtual FIFO Write Pointer Register
11000530	AP_DMA_UART_2_RX_VFF_RPT	32	UART2 RX Virtual FIFO Read Pointer Register
11000534	AP_DMA_UART_2_RX_FLOW_CTRL_THRE	32	UART2 RX Virtual FIFO Flow Control Threshold
11000538	AP_DMA_UART_2_RX_INT_BUF_SIZE	32	UART2 Rx Internal Buffer Size Register
1100053C	AP_DMA_UART_2_RX_VFF_VALID_SIZE	32	UART2 Rx Virtual FIFO Valid Size Register
11000540	AP_DMA_UART_2_RX_VFF_LEFT_SIZE	32	UART2 Rx Virtual FIFO Left Size Register
11000550	AP_DMA_UART_2_RX_DEBUG_STATUS_00	32	UART2 Rx Debug Status 00
11000580	AP_DMA_UART_3_TX_INT_FLAG	32	UART3 TX Virtual FIFO Interrupt Flag Register
11000584	AP_DMA_UART_3_TX_INT_EN	32	UART3 TX Virtual FIFO Interrupt Enable Register
11000588	AP_DMA_UART_3_TX_EN	32	UART3 TX Virtual FIFO Enable Register
1100058C	AP_DMA_UART_3_TX_RST	32	UART3 TX Virtual FIFO Reset Register
11000590	AP_DMA_UART_3_TX_STOP	32	UART3 TX Virtual FIFO Enable Register
11000594	AP_DMA_UART_3_TX_FLUSH	32	UART3 TX Virtual FIFO Flush Register
1100059C	AP_DMA_UART_3_TX_VFF_ADDR	32	UART3 TX Virtual FIFO Base Address Register
110005A4	AP_DMA_UART_3_TX_VFF_LEN	32	UART3 TX Virtual FIFO Length Register

110005A8	AP_DMA_UART_3_TX_VFF_THRE	32	UART3 TX Virtual FIFO Threshold Register
110005AC	AP_DMA_UART_3_TX_VFF_WPT	32	UART3 TX Virtual FIFO Write Pointer Register
110005B0	AP_DMA_UART_3_TX_VFF_RPT	32	UART3 TX Virtual FIFO Read Pointer Register
110005B8	AP_DMA_UART_3_TX_INT_BUF_SIZE	32	UART3 Tx Internal Buffer Size Register
110005BC	AP_DMA_UART_3_TX_VFF_VALID_SIZE	32	UART3 Tx Virtual FIFO Valid Size Register
110005C0	AP_DMA_UART_3_TX_VFF_LEFT_SIZE	32	UART3 Tx Virtual FIFO Left Size Register
110005D0	AP_DMA_UART_3_TX_DEBUG_STATUS_00	32	UART3 Tx Debug Status 00
110005D8	AP_DMA_UART_3_TX_VFF_WPT_VALID	32	UART3 TX Virtual FIFO Write Pointer Register by HW Control
110005E0	AP_DMA_UART_3_TX_FLUSH_ACT	32	UART3 TX Virtual FIFO Flush Status Register
110005E4	AP_DMA_UART_3_TX_HW_FLUSH	32	UART3 TX Virtual FIFO HW Flush Register
11000600	AP_DMA_UART_3_RX_INT_FLAG	32	UART3 RX Virtual FIFO Interrupt Flag Register
11000604	AP_DMA_UART_3_RX_INT_EN	32	UART3 RX Virtual FIFO Interrupt Enable Register
11000608	AP_DMA_UART_3_RX_EN	32	UART3 RX Virtual FIFO Enable Register
1100060C	AP_DMA_UART_3_RX_RST	32	UART3 RX Virtual FIFO Reset Register
11000610	AP_DMA_UART_3_RX_STOP	32	UART3 RX Virtual FIFO Enable Register
11000614	AP_DMA_UART_3_RX_FLUSH	32	UART3 RX Virtual FIFO Flush Register
1100061C	AP_DMA_UART_3_RX_VFF_ADDR	32	UART3 RX Virtual FIFO Base Address Register
11000624	AP_DMA_UART_3_RX_VFF_LEN	32	UART3 RX Virtual FIFO Length Register
11000628	AP_DMA_UART_3_RX_VFF_THRE	32	UART3 RX Virtual FIFO Threshold Register
1100062C	AP_DMA_UART_3_RX_VFF_WPT	32	UART3 RX Virtual FIFO Write Pointer Register

11000630	AP_DMA_UART_3_RX_VFF_RPT	32	UART3 RX Virtual FIFO Read Pointer Register
11000634	AP_DMA_UART_3_RX_FLOW_CTRL_THRE	32	UART3 RX Virtual FIFO Flow Control Threshold
11000638	AP_DMA_UART_3_RX_INT_BUF_SIZE	32	UART3 Rx Internal Buffer Size Register
1100063C	AP_DMA_UART_3_RX_VFF_VALID_SIZE	32	UART3 Rx Virtual FIFO Valid Size Register
11000640	AP_DMA_UART_3_RX_VFF_LEFT_SIZE	32	UART3 Rx Virtual FIFO Left Size Register
11000650	AP_DMA_UART_3_RX_DEBUG_STATUS_00	32	UART3 Rx Debug Status 00
11000680	AP_DMA_UART_4_TX_INT_FLAG	32	UART4 TX Virtual FIFO Interrupt Flag Register
11000684	AP_DMA_UART_4_TX_INT_EN	32	UART4 TX Virtual FIFO Interrupt Enable Register
11000688	AP_DMA_UART_4_TX_EN	32	UART4 TX Virtual FIFO Enable Register
1100068C	AP_DMA_UART_4_TX_RST	32	UART4 TX Virtual FIFO Reset Register
11000690	AP_DMA_UART_4_TX_STOP	32	UART4 TX Virtual FIFO Enable Register
11000694	AP_DMA_UART_4_TX_FLUSH	32	UART4 TX Virtual FIFO Flush Register
1100069C	AP_DMA_UART_4_TX_VFF_ADDR	32	UART4 TX Virtual FIFO Base Address Register
110006A4	AP_DMA_UART_4_TX_VFF_LEN	32	UART4 TX Virtual FIFO Length Register
110006A8	AP_DMA_UART_4_TX_VFF_THRE	32	UART4 TX Virtual FIFO Threshold Register
110006AC	AP_DMA_UART_4_TX_VFF_WPT	32	UART4 TX Virtual FIFO Write Pointer Register
110006B0	AP_DMA_UART_4_TX_VFF_RPT	32	UART4 TX Virtual FIFO Read Pointer Register
110006B8	AP_DMA_UART_4_TX_INT_BUF_SIZE	32	UART4 Tx Internal Buffer Size Register
110006BC	AP_DMA_UART_4_TX_VFF_VALID_SIZE	32	UART4 Tx Virtual FIFO Valid Size Register
110006C0	AP_DMA_UART_4_TX_VFF_LEFT_SIZE	32	UART4 Tx Virtual FIFO Left Size Register

110006D0	AP_DMA_UART_4_TX_DEBUG_STATUS_00	32	UART4 Tx Debug Status 00
110006D8	AP_DMA_UART_4_TX_VFF_WPT_VALID	32	UART4 TX Virtual FIFO Write Pointer Register by HW Control
110006E0	AP_DMA_UART_4_TX_FLUSH_ACT	32	UART4 TX Virtual FIFO Flush Status Register
110006E4	AP_DMA_UART_4_TX_HW_FLUSH	32	UART4 TX Virtual FIFO HW Flush Register
11000700	AP_DMA_UART_4_RX_INT_FLAG	32	UART4 RX Virtual FIFO Interrupt Flag Register
11000704	AP_DMA_UART_4_RX_INT_EN	32	UART4 RX Virtual FIFO Interrupt Enable Register
11000708	AP_DMA_UART_4_RX_EN	32	UART4 RX Virtual FIFO Enable Register
1100070C	AP_DMA_UART_4_RX_RST	32	UART4 RX Virtual FIFO Reset Register
11000710	AP_DMA_UART_4_RX_STOP	32	UART4 RX Virtual FIFO Enable Register
11000714	AP_DMA_UART_4_RX_FLUSH	32	UART4 RX Virtual FIFO Flush Register
1100071C	AP_DMA_UART_4_RX_VFF_ADDR	32	UART4 RX Virtual FIFO Base Address Register
11000724	AP_DMA_UART_4_RX_VFF_LEN	32	UART4 RX Virtual FIFO Length Register
11000728	AP_DMA_UART_4_RX_VFF_THRE	32	UART4 RX Virtual FIFO Threshold Register
1100072C	AP_DMA_UART_4_RX_VFF_WPT	32	UART4 RX Virtual FIFO Write Pointer Register
11000730	AP_DMA_UART_4_RX_VFF_RPT	32	UART4 RX Virtual FIFO Read Pointer Register
11000734	AP_DMA_UART_4_RX_FLOW_CTRL_THRE	32	UART4 RX Virtual FIFO Flow Control Threshold
11000738	AP_DMA_UART_4_RX_INT_BUF_SIZE	32	UART4 Rx Internal Buffer Size Register
1100073C	AP_DMA_UART_4_RX_VFF_VALID_SIZE	32	UART4 Rx Virtual FIFO Valid Size Register
11000740	AP_DMA_UART_4_RX_VFF_LEFT_SIZE	32	UART4 Rx Virtual FIFO Left Size Register
11000750	AP_DMA_UART_4_RX_DEBUG_STATUS_00	32	UART4 Rx Debug Status 00

11000780	AP_DMA_UART_5_TX_INT_FLAG	32	UART5 TX Virtual FIFO Interrupt Flag Register
11000784	AP_DMA_UART_5_TX_INT_EN	32	UART5 TX Virtual FIFO Interrupt Enable Register
11000788	AP_DMA_UART_5_TX_EN	32	UART5 TX Virtual FIFO Enable Register
1100078C	AP_DMA_UART_5_TX_RST	32	UART5 TX Virtual FIFO Reset Register
11000790	AP_DMA_UART_5_TX_STOP	32	UART5 TX Virtual FIFO Enable Register
11000794	AP_DMA_UART_5_TX_FLUSH	32	UART5 TX Virtual FIFO Flush Register
1100079C	AP_DMA_UART_5_TX_VFF_ADDR	32	UART5 TX Virtual FIFO Base Address Register
110007A4	AP_DMA_UART_5_TX_VFF_LEN	32	UART5 TX Virtual FIFO Length Register
110007A8	AP_DMA_UART_5_TX_VFF_THRE	32	UART5 TX Virtual FIFO Threshold Register
110007AC	AP_DMA_UART_5_TX_VFF_WPT	32	UART5 TX Virtual FIFO Write Pointer Register
110007B0	AP_DMA_UART_5_TX_VFF_RPT	32	UART5 TX Virtual FIFO Read Pointer Register
110007B8	AP_DMA_UART_5_TX_INT_BUF_SIZE	32	UART5 Tx Internal Buffer Size Register
110007BC	AP_DMA_UART_5_TX_VFF_VALID_SIZE	32	UART5 Tx Virtual FIFO Valid Size Register
110007C0	AP_DMA_UART_5_TX_VFF_LEFT_SIZE	32	UART5 Tx Virtual FIFO Left Size Register
110007D0	AP_DMA_UART_5_TX_DEBUG_STATUS_00	32	UART5 Tx Debug Status 00
110007D8	AP_DMA_UART_5_TX_VFF_WPT_VALID	32	UART5 TX Virtual FIFO Write Pointer Register by HW Control
110007E0	AP_DMA_UART_5_TX_FLUSH_ACT	32	UART5 TX Virtual FIFO Flush Status Register
110007E4	AP_DMA_UART_5_TX_HW_FLUSH	32	UART5 TX Virtual FIFO HW Flush Register
11000800	AP_DMA_UART_5_RX_INT_FLAG	32	UART5 RX Virtual FIFO Interrupt Flag Register
11000804	AP_DMA_UART_5_RX_INT_EN	32	UART5 RX Virtual FIFO Interrupt Enable Register
11000808	AP_DMA_UART_5_RX_EN	32	UART5 RX Virtual FIFO Enable Register

1100080C	AP_DMA_UART_5_RX_RST	32	UART5 RX Virtual FIFO Reset Register
11000810	AP_DMA_UART_5_RX_STOP	32	UART5 RX Virtual FIFO Enable Register
11000814	AP_DMA_UART_5_RX_FLUSH	32	UART5 RX Virtual FIFO Flush Register
1100081C	AP_DMA_UART_5_RX_VFF_ADDR	32	UART5 RX Virtual FIFO Base Address Register
11000824	AP_DMA_UART_5_RX_VFF_LEN	32	UART5 RX Virtual FIFO Length Register
11000828	AP_DMA_UART_5_RX_VFF_THRE	32	UART5 RX Virtual FIFO Threshold Register
1100082C	AP_DMA_UART_5_RX_VFF_WPT	32	UART5 RX Virtual FIFO Write Pointer Register
11000830	AP_DMA_UART_5_RX_VFF_RPT	32	UART5 RX Virtual FIFO Read Pointer Register
11000834	AP_DMA_UART_5_RX_FLOW_CTRL_THRE	32	UART5 RX Virtual FIFO Flow Control Threshold
11000838	AP_DMA_UART_5_RX_INT_BUF_SIZE	32	UART5 Rx Internal Buffer Size Register
1100083C	AP_DMA_UART_5_RX_VFF_VALID_SIZE	32	UART5 Rx Virtual FIFO Valid Size Register
11000840	AP_DMA_UART_5_RX_VFF_LEFT_SIZE	32	UART5 Rx Virtual FIFO Left Size Register
11000850	AP_DMA_UART_5_RX_DEBUG_STATUS_00	32	UART5 Rx Debug Status 00

11000000 AP_DMA_GLOBAL_INT_FLAG AP DMA Global Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UART5_RX	UART5_TX	UART4_RX	UART4_TX	UART3_RX	UART3_TX	UART2_RX	UART2_TX	UART1_RX	UART1_TX	UART0_RX	UART0_TX	I2C2	I2C1	I2C0	GDMA0
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	UART5_RX	

Bit(s)	Name	Description
14	UART5_TX	
13	UART4_RX	
12	UART4_TX	
11	UART3_RX	
10	UART3_TX	
9	UART2_RX	
8	UART2_TX	
7	UART1_RX	
6	UART1_TX	
5	UART0_RX	
4	UART0_TX	
3	I2C2	
2	I2C1	
1	I2C0	
0	GDMA0	

11000004 **AP_DMA_GLOBAL_RST** **AP DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**General DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**General DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 then waits for all running statuses to be 0 and sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000008 **AP_DMA_GLOBAL_RUNNING_STATUS** **AP DMA Global Running Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UART5_RX	UART5_TX	UART4_RX	UART4_TX	UART3_RX	UART3_TX	UART2_RX	UART2_TX	UART1_RX	UART1_TX	UART0_RX	UART0_TX	I2C2	I2C1	I2C0	GDMA0
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	UART5_RX	0: Idle 1: Running
14	UART5_TX	0: Idle 1: Running
13	UART4_RX	0: Idle 1: Running
12	UART4_TX	0: Idle 1: Running
11	UART3_RX	0: Idle 1: Running
10	UART3_TX	0: Idle 1: Running
9	UART2_RX	0: Idle 1: Running
8	UART2_TX	0: Idle 1: Running
7	UART1_RX	0: Idle 1: Running
6	UART1_TX	0: Idle 1: Running
5	UART0_RX	0: Idle 1: Running
4	UART0_TX	0: Idle 1: Running
3	I2C2	0: Idle 1: Running
2	I2C1	0: Idle 1: Running
1	I2C0	0: Idle 1: Running
0	GDMA0	0: Idle 1: Running

1100000C AP_DMA_GLOBAL_SLOW_DOWN AP DMA AXI Slow Down Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	W_SLOW_CNT															W_SLOW_EN
Type	RW															RW

Reset	0	0	0	0	0	0	0	0	0	0						0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R_SLOW_CNT															R_SLOW_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0						0

Bit(s)	Name	Description
31:22	W_SLOW_CNT	**AXI write to external AXI slow-down counter** 0 ~ 1023; the number means cycle. 0: Wait for 0 cycle then issue request 1: Wait for 1 cycle then issue request
16	W_SLOW_EN	**Enables AXI write to external AXI slow-down** 0: No slow down 1: Slow down
15:6	R_SLOW_CNT	**AXI read from external AXI slow-down counter** 0 ~ 1023; the number means cycle. 0: Wait for 0 cycle then issue request 1: Wait for 1 cycle then issue request
0	R_SLOW_EN	**Enables ARM side AXI read from external AXI slow-down** 0: No slow down 1: Slow down

11000010 **AP_DMA_GLOBAL_SEC_EN** **AP DMA Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LOCK	DLOCK														
Type	RW	RW														
Reset	0	0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UART5_RX	UART5_TX	UART4_RX	UART4_TX	UART3_RX	UART3_TX	UART2_RX	UART2_TX	UART1_RX	UART1_TX	UART0_RX	UART0_TX	I2C2	I2C1	I2C0	GDMA0
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	LOCK	**Locks secure bit** 0: Un-lock channel secure bit write 1: Lock channel secure bit
30	DLOCK	**Locks domain registers** 0: Un-lock channel domain register write 1: Lock channel domain register write
15	UART5_RX	0: This channel is non-secure. 1: This channel is secure.
14	UART5_TX	0: This channel is non-secure. 1: This channel is secure.

Bit(s)	Name	Description
13	UART4_RX	0: This channel is non-secure. 1: This channel is secure.
12	UART4_TX	0: This channel is non-secure. 1: This channel is secure.
11	UART3_RX	0: This channel is non-secure. 1: This channel is secure.
10	UART3_TX	0: This channel is non-secure. 1: This channel is secure.
9	UART2_RX	0: This channel is non-secure. 1: This channel is secure.
8	UART2_TX	0: This channel is non-secure. 1: This channel is secure.
7	UART1_RX	0: This channel is non-secure. 1: This channel is secure.
6	UART1_TX	0: This channel is non-secure. 1: This channel is secure.
5	UART0_RX	0: This channel is non-secure. 1: This channel is secure.
4	UART0_TX	0: This channel is non-secure. 1: This channel is secure.
3	I2C2	0: This channel is non-secure. 1: This channel is secure.
2	I2C1	0: This channel is non-secure. 1: This channel is secure.
1	I2C0	0: This channel is non-secure. 1: This channel is secure.
0	GDMA0	0: This channel is non-secure. 1: This channel is secure.

11000014 **AP_DMA_GLOBAL_GSEC_EN** **AP DMA Global Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GLOCK															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																GSEC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31	GLOCK	**This base address is locked.** 0: Un-lock 1: Lock
0	GSEC_EN	**Controls flobal security enable**

Bit(s)	Name	Description
		When this bit is set to 0, the overall channel will be treated as non-security channel. When the this bit is set to 1, the security property will depend on each channel's sec_en. 0: Disable, 1: Enable

11000018 **AP_DMA_GLOBAL_VIO_DBG1** **AP DMA Security Latch Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LAT_ADDR[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LAT_ADDR[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LAT_ADDR	**When any non-security transaction accesses DMA security zone and when R_VID or W_VID is not 1, DMA will latch the address of this transaction.**

1100001C **AP_DMA_GLOBAL_VIO_DBG0** **AP DMA Global Security Abort Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLR		R_VID	W_VID				APB_ABORT								
Type	WO		RO	RO				RO								
Reset	0		0	0				0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	CLR	**SW writes 1 to CLR to clear R_VID, W_VID and APB_ABORT to 0.** 0: Keep status 1: Clear status
29	R_VID	**Read violation** 0: No APB read is aborted 1: Read is aborted
28	W_VID	**Write violation** 0: No APB write is aborted 1: Write is aborted

Bit(s)	Name	Description
24	APB_ABORT	**When any non-security transaction accesses DMA security zone, DMA will set R_VID or W_VID to 1 then issue ABORT to security engine.** 0: No APB access is aborted 1: Aborted

11000020 **AP_DMA_GDMA0_SEC_EN** **AP GDMA0 Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**DOMAIN_CFG**		**SEC_EN**
Type														A0		A0
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000024 **AP_DMA_I2C0_SEC_EN** **AP I2C0 Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**DOMAIN_CFG**		**SEC_EN**
Type														A0		A0
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000028 **AP_DMA_I2C1_SEC_EN** **AP I2C1 Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DOMAIN_CFG		SEC_EN
Type														A0		A0
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

1100002C **AP_DMA_I2C2_SEC_EN** **AP I2C2 Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DOMAIN_CFG		SEC_EN
Type														A0		A0
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000030 **AP_DMA_UART0_TX_SEC_EN** **AP UART0 TX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name														DOMAIN_CFG		SEC_EN
Type														A0		A0
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000034 **AP_DMA_UART0_RX_SEC_EN** **AP UART0 RX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DOMAIN_CFG		SEC_EN
Type														A0		A0
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000038 **AP_DMA_UART1_TX_SEC_EN** **AP UART1 TX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DOMAIN_CFG		SEC_EN
Type														A0		A0
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

1100003C **AP_DMA_UART1_RX_SEC_EN** **AP UART1 RX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DOMAIN_CFG		SEC_EN
Type														A0		A0
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000040 **AP_DMA_UART2_TX_SEC_EN** **AP UART2 TX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DOMAIN_CFG		SEC_EN
Type														A0		A0
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000044 **AP_DMA_UART2_RX_SEC_EN** **AP UART2 RX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DOMAIN_CFG		SEC_EN
Type														A0		A0
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000048 **AP_DMA_UART3_TX_SEC_EN** **AP UART3 TX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DOMAIN_CFG		SEC_EN
Type														A0		A0
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

1100004C **AP_DMA_UART3_RX_SEC_EN** **AP UART3 RX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name														DOMAIN_CFG		SEC_EN
Type														A0		A0
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000050 AP_DMA_UART4_TX_SEC_EN AP UART4 TX Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DOMAIN_CFG		SEC_EN
Type														A0		A0
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000054 AP_DMA_UART4_RX_SEC_EN AP UART4 RX Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DOMAIN_CFG		SEC_EN
Type														A0		A0

Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000058 **AP_DMA_UART5_TX_SEC_EN** **AP UART5 TX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**DOMAIN_CFG**		**SEC_EN**
Type														A0		A0
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable** When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

1100005C **AP_DMA_UART5_RX_SEC_EN** **AP UART5 RX Security Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**DOMAIN_CFG**		**SEC_EN**
Type														A0		A0
Reset														0	0	0

Bit(s)	Name	Description
2:1	DOMAIN_CFG	**Sets up domain value**
0	SEC_EN	**Controls security enable**

Bit(s)	Name	Description
		When the corresponding bit is set to 1, the corresponding channel will be treated as security channel. 0: Disable 1: Enable

11000070 **AP_DMA_MD_INT_EN** **AP DMA MD Interrupt Enable Register** **8000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GLB_en															
Type	RU															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcm_en_uart5_rx	dcm_en_uart5_tx	dcm_en_uart4_rx	dcm_en_uart4_tx	dcm_en_uart3_rx	dcm_en_uart3_tx	dcm_en_uart2_rx	dcm_en_uart2_tx	dcm_en_uart1_rx	dcm_en_uart1_tx	dcm_en_uart0_rx	dcm_en_uart0_tx	i2c2	i2c1	i2c0	gdma0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	GLB_en	0: Disable DCM 1: Enable DCM
15	dcm_en_uart5_rx	**UART5 RX** 0: Disable DCM 1: Enable DCM
14	dcm_en_uart5_tx	**UART5 TX** 0: Disable DCM 1: Enable DCM
13	dcm_en_uart4_rx	**UART4 RX** 0: Disable DCM 1: Enable DCM
12	dcm_en_uart4_tx	**UART4 TX** 0: Disable DCM 1: Enable DCM
11	dcm_en_uart3_rx	**UART3 RX** 0: Disable DCM 1: Enable DCM
10	dcm_en_uart3_tx	**UART3 RX** 0: Disable DCM 1: Enable DCM
9	dcm_en_uart2_rx	**UART2 RX** 0: Disable DCM 1: Enable DCM
8	dcm_en_uart2_tx	**UART2 TX** 0: Disable DCM 1: Enable DCM
7	dcm_en_uart1_rx	**UART1 RX**

Bit(s)	Name	Description
		0: Disable DCM 1: Enable DCM
6	dcm_en_uart1_tx	**UART1 TX** 0: Disable DCM 1: Enable DCM
5	dcm_en_uart0_rx	**UART0 RX** 0: Disable DCM 1: Enable DCM
4	dcm_en_uart0_tx	**UART0 TX** 0: Disable DCM 1: Enable DCM
3	i2c2	**I2C2** 0: Disable DCM 1: Enable DCM
2	i2c1	**I2C1** 0: Disable DCM 1: Enable DCM
1	i2c0	**I2C0** 0: Disable DCM 1: Enable DCM
0	gdma0	**GDMA0** 0: Disable DCM 1: Enable DCM

11000074 **AP_DMA_GLOBAL_DOMAIN_CFG0** **AP DMA Domain Configuration Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UART5_RX		UART5_TX		UART4_RX		UART4_TX		UART3_RX		UART3_TX		UART2_RX		UART2_TX	
Type	RO		RO		RO		RO		RO		RO		RO		RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UART1_RX		UART1_TX		UART0_RX		UART0_TX		I2C2		I2C1		I2C0		GDMA0	
Type	RO		RO		RO		RO		RO		RO		RO		RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	UART5_RX	
29:28	UART5_TX	
27:26	UART4_RX	
25:24	UART4_TX	
23:22	UART3_RX	
21:20	UART3_TX	
19:18	UART2_RX	
17:16	UART2_TX	
15:14	UART1_RX	
13:12	UART1_TX	

Bit(s)	Name	Description
11:10	UART0_RX	
9:8	UART0_TX	
7:6	I2C2	
5:4	I2C1	
3:2	I2C0	
1:0	GDMA0	

1100007C FPC FPC 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											en	fpc_mode	fpc_dl_mode	fpc_data_mode	fpc_write_en	fpc_last
Type											RO	RO	RO	RO	RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5	en	
4	fpc_mode	
3	fpc_dl_mode	
2	fpc_data_mode	
1	fpc_write_en	
0	fpc_last	

11000080 AP_DMA_GDMA_0_INT_FLAG General DMA Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG_0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG_0	**This flag is raised when DMA is finished. Write 0 to clear it.** 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt

Bit(s)	Name	Description
		flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000084 **AP_DMA_GDMA_0_INT_EN** **General DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN_FLAG_0
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable

11000088 **AP_DMA_GDMA_0_EN** **General DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA when other control registers are set. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished.

Bit(s)	Name	Description
		0: Disable 1: Enable

1100008C **AP_DMA_GDMA_0_RST** **General DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	A0
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000090 **AP_DMA_GDMA_0_STOP** **General DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	A0
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA.

Bit(s)	Name	Description
		Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000094 **AP_DMA_GDMA_0_FLUSH** **General DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000098 **AP_DMA_GDMA_0_CON** **General DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RSIZE				WSIZE					WRAP_SEL		BURST_LEN		
Type			RW				RW					RW		RW		
Reset			0	0			0	0				0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WRAP_EN	SLOW_CNT										RADDR_FIX_EN	WADDR_FIX_EN	SLOW_EN	FIX_EN	
Type	RW	RW										RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
29:28	RSIZE	**General DMA read size** Only take effect when RADDR_FIX_EN = 1. 0: Transaction size is 1 byte.

Bit(s)	Name	Description
		1: Transaction size is 2 byte. 2: Transaction size is 4 byte. 3: Transaction size is 1 byte.
25:24	WSIZE	**General DMA write size** Only takes effect when WADDR_FIX_EN = 1 0: Transaction size is 1 byte. 1: Transaction size is 2 bytes. 2: Transaction size is 4 byte. 3: Transaction size is 1 bytes.
20	WRAP_SEL	**Selects general DMA wrap** 0: Read pointer (source) 1: Write pointer (destination)
18:16	BURST_LEN	**General DMA burst length** Valid value: 0 ~ 7. The best case is to set to 3(4-8). 0: 1-8 1: 2-8 2: 3-8 3: 4-8 4: 5-8 5: 6-8 6: 7-8 7: 7-8
15	WRAP_EN	**Enables general DMA wrap or double buffer** Its priority is higher than RADDR_FIX_EN or WADDR_FIX_EN. If WRAP_EN = 1 and WRAP_SEL =1, WADDR_FIX_EN will have no function. Likewise, if WRAP_EN = 1 and WRAP_SEL = 0, RADDR_FIX_EN will have no function. When FIX_EN = 1, if WRAP_EN = 1, WRAP_SEL can only be set to 1, and the read side cannot be set to wrap. 0: Disable 1: Enable
14:5	SLOW_CNT	**General DMA slow-down counter** We only slow down the read side, and the overall throughput will also be decreased. Supports up to 1,023 cycles. 0: 0 cycle 1: 1 cycle
4	RADDR_FIX_EN	**General DMA fixed read address** When FIX_EN = 1 or (WRAP_EN = 1 and WRAP_SEL=0), this bit will have no function. When this function is enabled, DMA has the following constrains: 1. src_addr must be 8-byte aligned. 2. The read transaction size will depend on RSIZE. 3. The burst length will be always single. 4. dst_addr must not be at EMI. 0: No fix 1: Fix
3	WADDR_FIX_EN	**General DMA fixed write address** When WRAP_EN = 1 and WRAP_SEL = 1, this bit will have no function. When this function is enabled, DMA has following constrains: 1. dst_addr must be 8-byte aligned. 2. The write transaction size will depend on WSIZE. 3. The burst length will be always single. 4. dst_addr must not be at EMI. 0: No fix 1: Fix
2	SLOW_EN	**Enables general DMA slow-down**

Bit(s)	Name	Description
1	FIX_EN	0: Disable 1: Enable **General DMA repeat inserting fixed pattern** Its priority is higher than RADDR_FIX_EN, that is when FIX_EN = 1, RADDR_FIX_EN will be ignored. 0: Does not use fix pattern 1: Use fix pattern

1100009C AP_DMA_G_DMA_0_SRC_ADDR General DMA SRC Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_ADDR[31:16]															
Type	A0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_ADDR[15:0]															
Type	A0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC_ADDR	**General DMA source address** It can be any byte alignment. When DIR=1 (Rx mode), src_addr equals the HIF FIFO address and must be 4-byte aligned. When FIX_EN = 1, SRC_ADDR will be treated as FIX_PATTERN. dir=1: HIF FIFO address dir=0: Memory address

110000A0 AP_DMA_G_DMA_0_DST_ADDR General DMA DST Address Register 00000020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DST_ADDR[31:16]															
Type	A0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST_ADDR[15:0]															
Type	A0															
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:0	DST_ADDR	**Peripheral DMA destination address** This address is the HIF FIFO address when in Tx (dir=0) mode or the memory address when in Rx (dir=1) mode. Do not set MEM_ADDR to be within the last 8 bytes before the 4KB boundary when you use SYSRAM as a Tx/Rx memory, e.g. 0xff9 ~ 0xfff is not allowed to be MEM_ADDR when you use SYSRAM as a Tx/Rx memory. dir=1: memory address dir=0: HIF FIFO address

110000A4 AP_DMA_G_DMA_0_LEN1 General DMA Transfer Length 1 Register 000FFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LEN1[19:16]			
Type													RW			
Reset													1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN1[15:0]															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
19:0	LEN1	**General DMA transfer length** It can be any byte alignment. This number will decrease when fetching data from the source side. This number also indicates how many data have not been delivered. 0 means zero byte transfer; 1 means one byte transfer. When read fix and write wrap are set, LEN1 must be multiple number of the byte number indicated by RSIZE.

110000A8 AP_DMA_G_DMA_0_LEN2 General DMA Transfer Length 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LEN2[19:16]			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	LEN2	**General DMA transfer length** It can be any byte alignment. This number will decrease when fetching data from the source side. This number also indicates how many data have not been delivered. 0 means zero byte transfer; 1 means one byte transfer

110000AC AP_DMA_G_DMA_0_JUMP_ADDR General DMA Jump Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	JUMP_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	JUMP_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	JUMP_ADDR	**General DMA end address** It can be any byte alignment. Only takes effect when WRAP_EN = 1.

110000B0 **AP_DMA_GDMA_0_INT_BUF_SIZE** **General DMA Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	**General DMA size of data in internal buffer**

110000B4 **AP_DMA_GDMA_0_CONNECT** **General DMA Connect Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RATIO	DIR	CONNECT	
Type													RW	RW	RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3	RATIO	**General DMA request/ack connection ratio** 0: 1/2 1: 1/1
2	DIR	**General DMA request/ack connection direction** 0: req/ack connects to write side. 1: req/ack connects to read side.
1:0	CONNECT	**General DMA request/ack connection** 1, 2 and 3 only take effect when WADDR_FIX_EN = 1 or RADDR_FIX_EN = 1. 0: No Connection 1: Connect set1 (req/ack) 2: Connect set2 (req/ack) 3: Connect set3 (req/ack)

110000B8 **AP_DMA_GDMA_0_AXIATTR** **General DMA AXI Attribute Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												WUSER	WCACHE			
Type												RW	RW			
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RUSER	RCACHE			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
20	WUSER	**General DMA AXI AWUSER signal** 0: Go through non-coherent bus 1: Go through coherent bus. Set this bit when destination is SYSRAM.
19:16	WCACHE	**General DMA AXI AWCACHE signal**
4	RUSER	**General DMA AXI ARUSER signal** 0: Go through non-coherent bus 1: Go through coherent bus. Set this bit when source is SYSRAM.
3:0	RCACHE	**General DMA AXI ARCACHE signal**

110000D0 **AP_DMA_GDMA_0_DEBUG_STATUS_00** **General DMA Debug Status 00 Register** **00000013**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D											R_CLR	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0				1	0	0	1	1

Bit(s)	Name	Description
31:24	RADDR_D	
23:16	WADDR_D_LH	
15:8	WADDR_D	
4	R_CLR	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

11000100 **AP_DMA_I2C_0_INT_FLAG** **Peripheral DMA Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished. Write 0 to clear it.**
0	TX_FLAG	**This flag is raised when TX DMA is finished. Write 0 to clear it.** 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000104 **AP_DMA_I2C_0_INT_EN** **Peripheral DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLAG	INTEN_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable

Bit(s)	Name	Description
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

11000108 AP_DMA_I2C_0_EN Peripheral DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100010C AP_DMA_I2C_0_RST Peripheral DMA Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	A0
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism.

Bit(s)	Name	Description
		0: Disable 1: Enable

11000110 AP_DMA_I2C_0_STOP Peripheral DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000114 AP_DMA_I2C_0_FLUSH Peripheral DMA Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. Note: STOP and FLUSH cannot be set to 1 in the same operation.

Bit(s)	Name	Description
		0: Disable 1: Enable

11000118 AP_DMA_I2C_0_CON Peripheral DMA Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as Tx. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	0: Tx 1: Rx

1100011C AP_DMA_I2C_0_TX_MEM_ADDR Peripheral DMA Memory Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. DO NOT set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

11000120 **AP_DMA_I2C_0_RX_MEM_ADDR** **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

11000124 **AP_DMA_I2C_0_TX_LEN** **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000128 **AP_DMA_I2C_0_RX_LEN** **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000138 **AP_DMA_I2C_0_INT_BUF_SIZE** **Peripheral DMA Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	

11000150 **AP_DMA_I2C_0_DEBUG_STATUS_00** **Peripheral DMA Debug Status 00 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D											R_CLR	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
31:24	RADDR_D	
23:16	WADDR_D_LH	
15:8	WADDR_D	
4	R_CLR	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

11000180 **AP_DMA_I2C_1_INT_FLAG** **Peripheral DMA Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished. Write 0 to clear it.**
0	TX_FLAG	**This flag is raised when TX DMA is finished. Write 0 to clear it.** 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000184 **AP_DMA_I2C_1_INT_EN** **Peripheral DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLAG	INTEN_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

11000188 **AP_DMA_I2C_1_EN** **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100018C **AP_DMA_I2C_1_RST** **Peripheral DMA Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000190 **AP_DMA_I2C_1_STOP** **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	A0
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000194 **AP_DMA_I2C_1_FLUSH** **Peripheral DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000198 **AP_DMA_I2C_1_CON** **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as Tx. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	0: Tx 1: Rx

1100019C **AP_DMA_I2C_1_TX_MEM_ADDR** **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. DO NOT set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

110001A0 **AP_DMA_I2C_1_RX_MEM_ADDR** **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

110001A4 AP_DMA_I2C_1_TX_LEN Peripheral DMA Transfer Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110001A8 AP_DMA_I2C_1_RX_LEN Peripheral DMA Transfer Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

110001B8 **AP_DMA_I2C_1_INT_BUF_SIZE** **Peripheral DMA Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	

110001D0 **AP_DMA_I2C_1_DEBUG_STATUS_00** **Peripheral DMA Debug Status 00 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D											R_CLR	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
31:24	RADDR_D	
23:16	WADDR_D_LH	
15:8	WADDR_D	
4	R_CLR	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

11000200 **AP_DMA_I2C_2_INT_FLAG** **Peripheral DMA Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name														FLAG_0	RX_FLAG	TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FLAG_0	**Raised when TX-to-RX is asserted when DMA engine is running.**
1	RX_FLAG	**Raised when RX DMA is finished. Write 0 to clear it.**
0	TX_FLAG	**This flag is raised when TX DMA is finished. Write 0 to clear it.** 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH =1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST =1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

11000204 **AP_DMA_I2C_2_INT_EN** **Peripheral DMA Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														INTEN_FLAG_0	INTEN_RX_FLAG	INTEN_TX_FLAG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	INTEN_FLAG_0	**Enables interrupt for FLAG_0** 0: Disable 1: Enable
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

11000208 **AP_DMA_I2C_2_EN** **Peripheral DMA Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1100020C AP_DMA_I2C_2_RST Peripheral DMA Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000210 AP_DMA_I2C_2_STOP Peripheral DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name															PAUSE	STOP
Type															RW	A0
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000214 **AP_DMA_I2C_2_FLUSH** **Peripheral DMA Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000218 **AP_DMA_I2C_2_CON** **Peripheral DMA Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name															FIX_EN	DIR
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as Tx. 0: Does not use fixed pattern 1: Use fixed pattern
0	DIR	0: Tx 1: Rx

1100021C **AP_DMA_I2C_2_TX_MEM_ADDR** **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. DO NOT set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when you use SYSRAM as a source memory.

11000220 **AP_DMA_I2C_2_RX_MEM_ADDR** **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address**

Bit(s)	Name	Description
		It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when you use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when you use SYSRAM as a destination memory.

11000224 **AP_DMA_I2C_2_TX_LEN** **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000228 **AP_DMA_I2C_2_RX_LEN** **Peripheral DMA Transfer Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

11000238 **AP_DMA_I2C_2_INT_BUF_SIZE** **Peripheral DMA Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	

11000250 **AP_DMA_I2C_2_DEBUG_STATUS_00** **Peripheral DMA Debug Status 00 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RADDR_D								WADDR_D_LH							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WADDR_D											R_CLR	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
31:24	RADDR_D	
23:16	WADDR_D_LH	
15:8	WADDR_D	
4	R_CLR	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

11000280 **AP_DMA_UART_0_TX_INT_FLAG** **UART0 TX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.** Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000284 **AP_DMA_UART_0_TX_INT_EN** **UART0 TX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**INTEN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto sets inten back to 0 when tx_vff_left_size >= tx_vff_thrs

11000288 **AP_DMA_UART_0_TX_EN** **UART0 TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**EN**
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART0 TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (a AHB slave port), VFF_W will

Bit(s)	Name	Description
		ignore this command, and the data will not be writte to virtual FIFO. 0: Disable 1: Enable

1100028C AP_DMA_UART_0_TX_RST UART0 TX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000290 AP_DMA_UART_0_TX_STOP UART0 TX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART0 TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation.

Bit(s)	Name	Description
		0: Disable 1: Enable

11000294 AP_DMA_UART_0_TX_FLUSH UART0 TX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART0 TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1100029C AP_DMA_UART_0_TX_VFF_ADDR UART0 TX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART0 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

110002A4 AP_DMA_UART_0_TX_VFF_LEN UART0 TX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110002A8 AP_DMA_UART_0_TX_VFF_THRE UART0 TX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110002AC AP_DMA_UART_0_TX_VFF_WPT UART0 TX Virtual FIFO Write Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit** It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

110002B0 AP_DMA_UART_0_TX_VFF_RPT UART0 TX Virtual FIFO Read Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

110002B8 AP_DMA_UART_0_TX_INT_BUF_SIZE UART0 Tx Internal Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

110002BC AP_DMA_UART_0_TX_VFF_VALID_SIZE UART0 Tx Virtual FIFO Valid Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110002C0 AP_DMA_UART_0_TX_VFF_LEFT_SIZE UART0 Tx Virtual FIFO Left Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

110002D0 AP_DMA_UART_0_TX_DEBUG_STATUS_00 UART0 Tx Debug Status 00 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_	FLUSH_	WD_ACT	RD_ACT	WREQ	RREQ	W_Q_CLR	R_Q_CLR

									ACT	STR						
Type				RO					RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
6	FLUSH_STR	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

110002D8 **AP_DMA_UART_0_TX_VFF_WPT_VALID** **UART0 TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

110002E0 **AP_DMA_UART_0_TX_FLUSH_ACT** **UART0 TX Virtual FIFO Flush Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	**There is a flush command when the UART0 TX channel is flushing.**
0	FLUSH_ACT	**UART0 TX channel flush status**

110002E4 **AP_DMA_UART_0_TX_HW_FLUSH** **UART0 TX Virtual FIFO HW Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update WPT with SW setting 1: Update WPT when flush = 0

11000300 **AP_DMA_UART_0_RX_INT_FLAG** **UART0 RX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.** This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	**Write 1 to clear it.** This flag is raised when RX_VFF_VALID_SIZE >= RX_VFF_THRE. (VFF is almost full and MCU needs to consume those data.)

11000304 **AP_DMA_UART_0_RX_INT_EN** **UART0 RX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enable** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enable** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000308 **AP_DMA_UART_0_RX_EN** **UART0 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART0 RX virtual FIFO**

Bit(s)	Name	Description
		Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1100030C **AP_DMA_UART_0_RX_RST** **UART0 RX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000310 **AP_DMA_UART_0_RX_STOP** **UART0 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART0 RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN

Bit(s)	Name	Description
		will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000314 AP_DMA_UART_0_RX_FLUSH UART0 RX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART0 RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush, there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1100031C AP_DMA_UART_0_RX_VFF_ADDR UART0 RX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART0 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000324 AP_DMA_UART_0_RX_VFF_LEN UART0 RX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000328 AP_DMA_UART_0_RX_VFF_THRE UART0 RX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1100032C AP_DMA_UART_0_RX_VFF_WPT UART0 RX Virtual FIFO Write Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_WPT	**RX VFF write pointer maintained by hardware** In byte alignment.

11000330 **AP_DMA_UART_0_RX_VFF_RPT** **UART0 RX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

11000334 **AP_DMA_UART_0_RX_FLOW_CTRL_THRE** **UART0 RX Virtual FIFO Flow Control Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

11000338 **AP_DMA_UART_0_RX_INT_BUF_SIZE** **UART0 Rx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

1100033C **AP_DMA_UART_0_RX_VFF_VALID_SIZE** **UART0 Rx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000340 **AP_DMA_UART_0_RX_VFF_LEFT_SIZE** **UART0 Rx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000350 **AP_DMA_UART_0_RX_DEBUG_STATUS_00** **UART0 Rx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT		WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

11000380 **AP_DMA_UART_1_TX_INT_FLAG** **UART1 TX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.**

Bit(s)	Name	Description
		Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000384 **AP_DMA_UART_1_TX_INT_EN** **UART1 TX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto sets inten back to 0 when tx_vff_left_size >= tx_vff_thrs

11000388 **AP_DMA_UART_1_TX_EN** **UART1 TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART1 TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (a AHB slave port), VFF_W will ignore this command, and the data will not be writte to virtual FIFO.

Bit(s)	Name	Description
		0: Disable 1: Enable

1100038C AP_DMA_UART_1_TX_RST UART1 TX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000390 AP_DMA_UART_1_TX_STOP UART1 TX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART1 TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000394 AP_DMA_UART_1_TX_FLUSH UART1 TX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART1 TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1100039C AP_DMA_UART_1_TX_VFF_ADDR UART1 TX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART1 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

110003A4 AP_DMA_UART_1_TX_VFF_LEN UART1 TX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110003A8 AP_DMA_UART_1_TX_VFF_THRE UART1 TX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110003AC AP_DMA_UART_1_TX_VFF_WPT UART1 TX Virtual FIFO Write Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit**

Bit(s)	Name	Description
15:0	TX_VFF_WPT	It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software. **Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

110003B0 **AP_DMA_UART_1_TX_VFF_RPT** **UART1 TX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

110003B8 **AP_DMA_UART_1_TX_INT_BUF_SIZE** **UART1 Tx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

110003BC **AP_DMA_UART_1_TX_VFF_VALID_SIZE** **UART1 Tx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110003C0 **AP_DMA_UART_1_TX_VFF_LEFT_SIZE** **UART1 Tx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

110003D0 **AP_DMA_UART_1_TX_DEBUG_STATUS_00** **UART1 Tx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT	FLUSH_STR	WD_ACT	RD_ACT	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type				RO					RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
6	FLUSH_STR	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

110003D8 **AP_DMA_UART_1_TX_VFF_WPT_VALID** **UART1 TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

110003E0 **AP_DMA_UART_1_TX_FLUSH_ACT** **UART1 TX Virtual FIFO Flush Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	**There is a flush command when the UART1 TX channel is flushing.**
0	FLUSH_ACT	**UART1 TX channel flush status**

110003E4 AP_DMA_UART_1_TX_HW_FLUSH UART1 TX Virtual FIFO HW Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update WPT with SW setting 1: Update WPT when flush = 0

11000400 AP_DMA_UART_1_RX_INT_FLAG UART1 RX Virtual FIFO Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.**

Bit(s)	Name	Description
0	FLAG0	This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF. **Write 1 to clear it.** This flag is raised when RX_VFF_VALID_SIZE >= RX_VFF_THRE. (VFF is almost full and MCU needs to consume those data.)

11000404 **AP_DMA_UART_1_RX_INT_EN** **UART1 RX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**INTEN1**	**INTEN0**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enable** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enable** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000408 **AP_DMA_UART_1_RX_EN** **UART1 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**EN**
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART1 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will

Bit(s)	Name	Description
		immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1100040C **AP_DMA_UART_1_RX_RST** **UART1 RX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000410 **AP_DMA_UART_1_RX_STOP** **UART1 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART1 RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000414 AP_DMA_UART_1_RX_FLUSH UART1 RX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART1 RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1100041C AP_DMA_UART_1_RX_VFF_ADDR UART1 RX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART1 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000424 AP_DMA_UART_1_RX_VFF_LEN UART1 RX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000428 AP_DMA_UART_1_RX_VFF_THRE UART1 RX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1100042C AP_DMA_UART_1_RX_VFF_WPT UART1 RX Virtual FIFO Write Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware**

Bit(s)	Name	Description
15:0	RX_VFF_WPT	It is initialized to 0. When wrapped to the ring head again, invert this bit. **RX VFF write pointer maintained by hardware** In byte alignment.

11000430 **AP_DMA_UART_1_RX_VFF_RPT** **UART1 RX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

11000434 **AP_DMA_UART_1_RX_FLOW_CTRL_THRE** **UART1 RX Virtual FIFO Flow Control Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

11000438 **AP_DMA_UART_1_RX_INT_BUF_SIZE** **UART1 Rx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

1100043C **AP_DMA_UART_1_RX_VFF_VALID_SIZE** **UART1 Rx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000440 **AP_DMA_UART_1_RX_VFF_LEFT_SIZE** **UART1 Rx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000450 **AP_DMA_UART_1_RX_DEBUG_STATUS_00** **UART1 Rx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT		WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

11000480 **AP_DMA_UART_2_TX_INT_FLAG** **UART2 TX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.**

Bit(s)	Name	Description
		Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000484 **AP_DMA_UART_2_TX_INT_EN** **UART2 TX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto sets inten back to 0 when tx_vff_left_size >= tx_vff_thrs

11000488 **AP_DMA_UART_2_TX_EN** **UART2 TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART2 TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (a AHB slave port), VFF_W will ignore this command, and the data will not be writte to virtual FIFO.

Bit(s)	Name	Description
		0: Disable 1: Enable

1100048C AP_DMA_UART_2_TX_RST UART2 TX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000490 AP_DMA_UART_2_TX_STOP UART2 TX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART2 TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000494 AP_DMA_UART_2_TX_FLUSH UART2 TX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART2 TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1100049C AP_DMA_UART_2_TX_VFF_ADDR UART2 TX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART2 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

110004A4 AP_DMA_UART_2_TX_VFF_LEN UART2 TX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110004A8 AP_DMA_UART_2_TX_VFF_THRE UART2 TX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110004AC AP_DMA_UART_2_TX_VFF_WPT UART2 TX Virtual FIFO Write Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit**

Bit(s)	Name	Description
		It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

110004B0 **AP_DMA_UART_2_TX_VFF_RPT** **UART2 TX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

110004B8 **AP_DMA_UART_2_TX_INT_BUF_SIZE** **UART2 Tx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

110004BC **AP_DMA_UART_2_TX_VFF_VALID_SIZE** **UART2 Tx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110004C0 **AP_DMA_UART_2_TX_VFF_LEFT_SIZE** **UART2 Tx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

110004D0 **AP_DMA_UART_2_TX_DEBUG_STATUS_00** **UART2 Tx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT	FLUSH_STR	WD_ACT	RD_ACT	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type				RO					RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
6	FLUSH_STR	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

110004D8 **AP_DMA_UART_2_TX_VFF_WPT_VALID** **UART2 TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

110004E0 **AP_DMA_UART_2_TX_FLUSH_ACT** **UART2 TX Virtual FIFO Flush Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	**There is a flush command when the UART2 TX channel is flushing.**
0	FLUSH_ACT	**UART2 TX channel flush status**

110004E4 **AP_DMA_UART_2_TX_HW_FLUSH** **UART2 TX Virtual FIFO HW Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update WPT with SW setting 1: Update WPT when flush = 0

11000500 **AP_DMA_UART_2_RX_INT_FLAG** **UART2 RX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.**

Bit(s)	Name	Description
0	FLAG0	This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF. **Write 1 to clear it.** This flag is raised when RX_VFF_VALID_SIZE >= RX_VFF_THRE. (VFF is almost full and MCU needs to consume those data.)

11000504 **AP_DMA_UART_2_RX_INT_EN** **UART2 RX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**INTEN1**	**INTEN0**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enable** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enable** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000508 **AP_DMA_UART_2_RX_EN** **UART2 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**EN**
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART2 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will

Bit(s)	Name	Description
		immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1100050C AP_DMA_UART_2_RX_RST UART2 RX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000510 AP_DMA_UART_2_RX_STOP UART2 RX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART2 RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000514 AP_DMA_UART_2_RX_FLUSH UART2 RX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART2 RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1100051C AP_DMA_UART_2_RX_VFF_ADDR UART2 RX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART2 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000524 AP_DMA_UART_2_RX_VFF_LEN UART2 RX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000528 AP_DMA_UART_2_RX_VFF_THRE UART2 RX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1100052C AP_DMA_UART_2_RX_VFF_WPT UART2 RX Virtual FIFO Write Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware**

Bit(s)	Name	Description
15:0	RX_VFF_WPT	It is initialized to 0. When wrapped to the ring head again, invert this bit. **RX VFF write pointer maintained by hardware** In byte alignment.

11000530 **AP_DMA_UART_2_RX_VFF_RPT** **UART2 RX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

11000534 **AP_DMA_UART_2_RX_FLOW_CTRL_THRE** **UART2 RX Virtual FIFO Flow Control Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

11000538 AP_DMA_UART_2_RX_INT_BUF_SIZE UART2 Rx Internal Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

1100053C AP_DMA_UART_2_RX_VFF_VALID_SIZE UART2 Rx Virtual FIFO Valid Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000540 AP_DMA_UART_2_RX_VFF_LEFT_SIZE UART2 Rx Virtual FIFO Left Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000550 **AP_DMA_UART_2_RX_DEBUG_STATUS_00** **UART2 Rx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT		WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

11000580 **AP_DMA_UART_3_TX_INT_FLAG** **UART3 TX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.**

Bit(s)	Name	Description
		Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000584 **AP_DMA_UART_3_TX_INT_EN** **UART3 TX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto sets inten back to 0 when tx_vff_left_size >= tx_vff_thrs

11000588 **AP_DMA_UART_3_TX_EN** **UART3 TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART3 TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (a AHB slave port), VFF_W will ignore this command, and the data will not be writte to virtual FIFO.

Bit(s)	Name	Description
		0: Disable 1: Enable

1100058C AP_DMA_UART_3_TX_RST UART3 TX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000590 AP_DMA_UART_3_TX_STOP UART3 TX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART3 TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000594 AP_DMA_UART_3_TX_FLUSH UART3 TX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART3 TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1100059C AP_DMA_UART_3_TX_VFF_ADDR UART3 TX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART3 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

110005A4 AP_DMA_UART_3_TX_VFF_LEN UART3 TX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110005A8 AP_DMA_UART_3_TX_VFF_THRE UART3 TX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110005AC AP_DMA_UART_3_TX_VFF_WPT UART3 TX Virtual FIFO Write Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit**

Bit(s)	Name	Description
		It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

110005B0 **AP_DMA_UART_3_TX_VFF_RPT** **UART3 TX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

110005B8 **AP_DMA_UART_3_TX_INT_BUF_SIZE** **UART3 Tx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

110005BC AP_DMA_UART_3_TX_VFF_VALID_SIZE UART3 Tx Virtual FIFO Valid Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110005C0 AP_DMA_UART_3_TX_VFF_LEFT_SIZE UART3 Tx Virtual FIFO Left Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

110005D0 AP_DMA_UART_3_TX_DEBUG_STATUS_00 UART3 Tx Debug Status 00 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT	FLUSH_STR	WD_ACT	RD_ACT	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type				RO					RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
6	FLUSH_STR	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

110005D8 **AP_DMA_UART_3_TX_VFF_WPT_VALID** **UART3 TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

110005E0 **AP_DMA_UART_3_TX_FLUSH_ACT** **UART3 TX Virtual FIFO Flush Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	**There is a flush command when the UART3 TX channel is flushing.**
0	FLUSH_ACT	**UART3 TX channel flush status**

110005E4 **AP_DMA_UART_3_TX_HW_FLUSH** **UART3 TX Virtual FIFO HW Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update WPT with SW setting 1: Update WPT when flush = 0

11000600 **AP_DMA_UART_3_RX_INT_FLAG** **UART3 RX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.**

Bit(s)	Name	Description
0	FLAG0	This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF. **Write 1 to clear it.** This flag is raised when RX_VFF_VALID_SIZE >= RX_VFF_THRE. (VFF is almost full and MCU needs to consume those data.)

11000604 **AP_DMA_UART_3_RX_INT_EN** **UART3 RX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enable** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enable** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000608 **AP_DMA_UART_3_RX_EN** **UART3 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART3 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will

Bit(s)	Name	Description
		immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1100060C **AP_DMA_UART_3_RX_RST** **UART3 RX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000610 **AP_DMA_UART_3_RX_STOP** **UART3 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART3 RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000614 AP_DMA_UART_3_RX_FLUSH UART3 RX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART3 RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1100061C AP_DMA_UART_3_RX_VFF_ADDR UART3 RX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART3 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000624 AP_DMA_UART_3_RX_VFF_LEN UART3 RX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000628 AP_DMA_UART_3_RX_VFF_THRE UART3 RX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1100062C AP_DMA_UART_3_RX_VFF_WPT UART3 RX Virtual FIFO Write Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware**

Bit(s)	Name	Description
15:0	RX_VFF_WPT	It is initialized to 0. When wrapped to the ring head again, invert this bit. **RX VFF write pointer maintained by hardware** In byte alignment.

11000630 **AP_DMA_UART_3_RX_VFF_RPT** **UART3 RX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

11000634 **AP_DMA_UART_3_RX_FLOW_CTRL_THRE** **UART3 RX Virtual FIFO Flow Control Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

11000638 **AP_DMA_UART_3_RX_INT_BUF_SIZE** **UART3 Rx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

1100063C **AP_DMA_UART_3_RX_VFF_VALID_SIZE** **UART3 Rx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000640 **AP_DMA_UART_3_RX_VFF_LEFT_SIZE** **UART3 Rx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000650 **AP_DMA_UART_3_RX_DEBUG_STATUS_00** **UART3 Rx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT		WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

11000680 **AP_DMA_UART_4_TX_INT_FLAG** **UART4 TX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.**

Bit(s)	Name	Description
		Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000684 AP_DMA_UART_4_TX_INT_EN UART4 TX Virtual FIFO Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto sets inten back to 0 when tx_vff_left_size >= tx_vff_thrs

11000688 AP_DMA_UART_4_TX_EN UART4 TX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART4 TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (a AHB slave port), VFF_W will ignore this command, and the data will not be writte to virtual FIFO.

Bit(s)	Name	Description
		0: Disable 1: Enable

1100068C **AP_DMA_UART_4_TX_RST** **UART4 TX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000690 **AP_DMA_UART_4_TX_STOP** **UART4 TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART4 TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000694 AP_DMA_UART_4_TX_FLUSH UART4 TX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART4 TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1100069C AP_DMA_UART_4_TX_VFF_ADDR UART4 TX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART4 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

110006A4 AP_DMA_UART_4_TX_VFF_LEN UART4 TX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110006A8 AP_DMA_UART_4_TX_VFF_THRE UART4 TX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110006AC AP_DMA_UART_4_TX_VFF_WPT UART4 TX Virtual FIFO Write Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit**

Bit(s)	Name	Description
		It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

110006B0 **AP_DMA_UART_4_TX_VFF_RPT** **UART4 TX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

110006B8 **AP_DMA_UART_4_TX_INT_BUF_SIZE** **UART4 Tx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

110006BC AP_DMA_UART_4_TX_VFF_VALID_SIZE UART4 Tx Virtual FIFO Valid Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110006C0 AP_DMA_UART_4_TX_VFF_LEFT_SIZE UART4 Tx Virtual FIFO Left Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

110006D0 AP_DMA_UART_4_TX_DEBUG_STATUS_00 UART4 Tx Debug Status 00 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT	FLUSH_STR	WD_ACT	RD_ACT	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type				RO					RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
6	FLUSH_STR	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

110006D8 **AP_DMA_UART_4_TX_VFF_WPT_VALID** **UART4 TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

110006E0 **AP_DMA_UART_4_TX_FLUSH_ACT** **UART4 TX Virtual FIFO Flush Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	**There is a flush command when the UART4 TX channel is flushing.**
0	FLUSH_ACT	**UART4 TX channel flush status**

110006E4 **AP_DMA_UART_4_TX_HW_FLUSH** **UART4 TX Virtual FIFO HW Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update WPT with SW setting 1: Update WPT when flush = 0

11000700 **AP_DMA_UART_4_RX_INT_FLAG** **UART4 RX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.**

Bit(s)	Name	Description
0	FLAG0	This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF. **Write 1 to clear it.** This flag is raised when RX_VFF_VALID_SIZE >= RX_VFF_THRE. (VFF is almost full and MCU needs to consume those data.)

11000704 **AP_DMA_UART_4_RX_INT_EN** **UART4 RX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**INTEN1**	**INTEN0**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enable** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enable** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000708 **AP_DMA_UART_4_RX_EN** **UART4 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**EN**
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART4 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will

Bit(s)	Name	Description
		immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1100070C **AP_DMA_UART_4_RX_RST** **UART4 RX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000710 **AP_DMA_UART_4_RX_STOP** **UART4 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART4 RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000714 AP_DMA_UART_4_RX_FLUSH UART4 RX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART4 RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1100071C AP_DMA_UART_4_RX_VFF_ADDR UART4 RX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART4 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000724 AP_DMA_UART_4_RX_VFF_LEN UART4 RX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000728 AP_DMA_UART_4_RX_VFF_THRE UART4 RX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1100072C AP_DMA_UART_4_RX_VFF_WPT UART4 RX Virtual FIFO Write Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware**

Bit(s)	Name	Description
15:0	RX_VFF_WPT	It is initialized to 0. When wrapped to the ring head again, invert this bit. **RX VFF write pointer maintained by hardware** In byte alignment.

11000730 **AP_DMA_UART_4_RX_VFF_RPT** **UART4 RX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

11000734 **AP_DMA_UART_4_RX_FLOW_CTRL_THRE** **UART4 RX Virtual FIFO Flow Control Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

11000738 **AP_DMA_UART_4_RX_INT_BUF_SIZE** **UART4 Rx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

1100073C **AP_DMA_UART_4_RX_VFF_VALID_SIZE** **UART4 Rx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000740 **AP_DMA_UART_4_RX_VFF_LEFT_SIZE** **UART4 Rx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000750 **AP_DMA_UART_4_RX_DEBUG_STATUS_00** **UART4 Rx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT		WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

11000780 **AP_DMA_UART_5_TX_INT_FLAG** **UART5 TX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.**

Bit(s)	Name	Description
		Interrupt will be issued to HW when FLAG=1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN=1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

11000784 **AP_DMA_UART_5_TX_INT_EN** **UART5 TX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enable** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Does not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto sets inten back to 0 when tx_vff_left_size >= tx_vff_thrs

11000788 **AP_DMA_UART_5_TX_EN** **UART5 TX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART3 TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (a AHB slave port), VFF_W will ignore this command, and the data will not be writte to virtual FIFO.

Bit(s)	Name	Description
		0: Disable 1: Enable

1100078C AP_DMA_UART_5_TX_RST UART5 TX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000790 AP_DMA_UART_5_TX_STOP UART5 TX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART3 TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

11000794 AP_DMA_UART_5_TX_FLUSH UART5 TX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART3 TX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1100079C AP_DMA_UART_5_TX_VFF_ADDR UART5 TX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART3 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

110007A4 AP_DMA_UART_5_TX_VFF_LEN UART5 TX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

110007A8 AP_DMA_UART_5_TX_VFF_THRE UART5 TX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

110007AC AP_DMA_UART_5_TX_VFF_WPT UART5 TX Virtual FIFO Write Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit**

Bit(s)	Name	Description
		It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

110007B0 **AP_DMA_UART_5_TX_VFF_RPT** **UART5 TX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

110007B8 **AP_DMA_UART_5_TX_INT_BUF_SIZE** **UART5 Tx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

110007BC AP_DMA_UART_5_TX_VFF_VALID_SIZE UART5 Tx Virtual FIFO Valid Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

110007C0 AP_DMA_UART_5_TX_VFF_LEFT_SIZE UART5 Tx Virtual FIFO Left Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

110007D0 AP_DMA_UART_5_TX_DEBUG_STATUS_00 UART5 Tx Debug Status 00 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT	FLUSH_STR	WD_ACT	RD_ACT	WREQ	RREQ	W_Q_CLR	R_Q_CLR
Type				RO					RO	RO	RO	RO	RO	RO	RO	RO
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
6	FLUSH_STR	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	
1	W_Q_CLR	
0	R_Q_CLR	

110007D8 **AP_DMA_UART_5_TX_VFF_WPT_VALID** **UART5 TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH= 0, sync to TX_VFF_WPT_WRAP. If flush, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH= 0, sync to TX_VFF_WPT. If flush, it will not update the value until the flush is finished.

110007E0 **AP_DMA_UART_5_TX_FLUSH_ACT** **UART5 TX Virtual FIFO Flush Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	**There is a flush command when the UART3 TX channel is flushing.**
0	FLUSH_ACT	**UART3 TX channel flush status**

110007E4 **AP_DMA_UART_5_TX_HW_FLUSH** **UART5 TX Virtual FIFO HW Flush Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update WPT with SW setting 1: Update WPT when flush = 0

11000800 **AP_DMA_UART_5_RX_INT_FLAG** **UART5 RX Virtual FIFO Interrupt Flag Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.**

Bit(s)	Name	Description
0	FLAG0	This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF. **Write 1 to clear it.** This flag is raised when RX_VFF_VALID_SIZE >= RX_VFF_THRE. (VFF is almost full and MCU needs to consume those data.)

11000804 **AP_DMA_UART_5_RX_INT_EN** **UART5 RX Virtual FIFO Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**INTEN1**	**INTEN0**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enable** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enable** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

11000808 **AP_DMA_UART_5_RX_EN** **UART5 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**EN**
Type																A0
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART3 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will

Bit(s)	Name	Description
		immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1100080C **AP_DMA_UART_5_RX_RST** **UART5 RX Virtual FIFO Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

11000810 **AP_DMA_UART_5_RX_STOP** **UART5 RX Virtual FIFO Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																A0
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART3 RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

11000814 AP_DMA_UART_5_RX_FLUSH UART5 RX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																A0
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART3 RX virtual FIFO** Set FLUSH to 1 to allow DMA flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1100081C AP_DMA_UART_5_RX_VFF_ADDR UART5 RX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR[28:13]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR[12:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART3 memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

11000824 AP_DMA_UART_5_RX_VFF_LEN UART5 RX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

11000828 AP_DMA_UART_5_RX_VFF_THRE UART5 RX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1100082C AP_DMA_UART_5_RX_VFF_WPT UART5 RX Virtual FIFO Write Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware**

Bit(s)	Name	Description
15:0	RX_VFF_WPT	It is initialized to 0. When wrapped to the ring head again, invert this bit. **RX VFF write pointer maintained by hardware** In byte alignment.

11000830 **AP_DMA_UART_5_RX_VFF_RPT** **UART5 RX Virtual FIFO Read Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

11000834 **AP_DMA_UART_5_RX_FLOW_CTRL_THRE** **UART5 RX Virtual FIFO Flow Control Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

11000838 AP_DMA_UART_5_RX_INT_BUF_SIZE UART5 Rx Internal Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

1100083C AP_DMA_UART_5_RX_VFF_VALID_SIZE UART5 Rx Virtual FIFO Valid Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

11000840 AP_DMA_UART_5_RX_VFF_LEFT_SIZE UART5 Rx Virtual FIFO Left Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

11000850 **AP_DMA_UART_5_RX_DEBUG_STATUS_00** **UART5 Rx Debug Status 00** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RADDR_D								WADDR_D_LH				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				WADDR_D					FLUSH_ACT		WD_ACT	RD_ACT	WREQ	RREQ		
Type				RO					RO		RO	RO	RO	RO		
Reset				0	0	0	0	0	0		0	0	0	0		

Bit(s)	Name	Description
28:24	RADDR_D	
20:16	WADDR_D_LH	
12:8	WADDR_D	
7	FLUSH_ACT	
5	WD_ACT	
4	RD_ACT	
3	WREQ	
2	RREQ	

1.10 AUXADC

1.10.1 Introduction

The auxiliary ADC unit is used to identify the plugged peripheral and perform voltage/temperature measurement. There are 16 input channels allowing diverse applications in this unit.

1.10.2 Features

Table 1-5 table describes the features of the AUXADC module. The electrical specifications of AUXADC analog circuit and channels are shown in below tables and figure.

Table 1-5. AUXADC: feature list

Item	Main function	Description
1	Immediate analog-digital conversion	In immediate mode, it supports auto-set option.
2	Background detection and interrupt	The related command registers: AUXADC_DET_VOLT, AUXADC_PERIOD, AUXADC_DEBT, AUXADC_SEL
3	Temperature measurement	

Table 1-6. Electrical characteristics or electrical specifications

		Spec.			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
N	Resolution		12		Bit
FC	Clock rate		4		MHz
FS	Sampling rate @ N-Bit		4/(N+4)		MSPS
	Input swing	0		1.5	V
CIN (exc. PAD loading)	Input capacitance Unselected channel Selected channel		50 5		fF pF
RIN	Input resistance Unselected channel	20			MΩ
	Clock latency		N+4		1/FC
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+2.0/-2.0		LSB
SINAD	Signal to noise and distortion ratio (1kHz full swing input & 4.0833MHz clock rate)	56	62		dB
AVDD	Analog power supply	1.71	1.80	1.98	V
DVDD	Digital Power Supply	1.035	1.15	1.265	V
T	Operating temperature	-40		125	°C
	Current consumption Power-up Power-down		600 5		uA uA
	Gain Error W/I calibration W/o calibration	-1 -7		1 7	%
	Offset Error W/I calibration W/o calibration	-10 -50		10 50	mV
Temp. Accuracy		-5		+5	°C

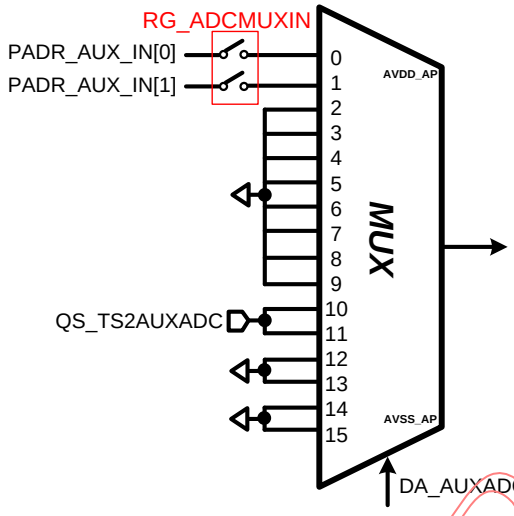


Figure 1-7. AUXADC channels

1.10.3 Block Diagram

The auxiliary ADC includes the following functional blocks:
Analog multiplexer: Selects signal from one of the auxiliary input channels. Some channels are for internal voltage measuring and some for external voltage measuring. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

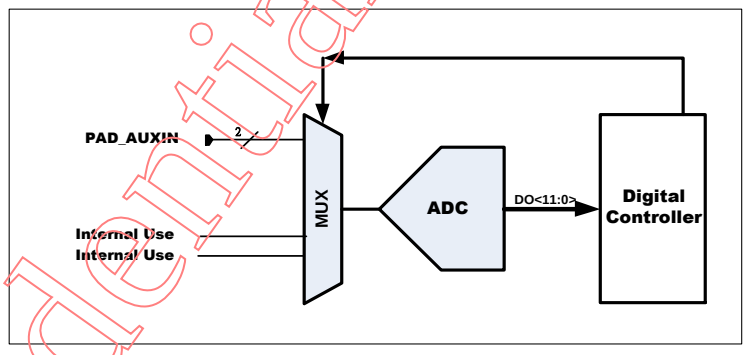


Figure 1-2. Block diagram of AUXADC

1.10.4 Register Definition

Module name: AUXADC_Modify Base address: (+11001000h)

Address	Name	Width	Register Function
11001000	AUXADC_CON0	32	AUXADC Control Register 0

Address	Name	Width	Register Function
			Defines auto-sample mode of the module In auto-sample mode, each channel with its sample register being read can start sampling immediately once the read back channel RDY bit is asserted without configuring the control register AUXADC_CON1 again.
11001004	AUXADC_CON1	32	AUXADC Control Register 1 Controls channel 0~15 immediate mode
11001008	AUXADC_CON1_SET	32	AUXADC Control Set Register 1 Sets up channel 0~15 immediate mode
1100100C	AUXADC_CON1_CLR	32	AUXADC Control Clear Register 1 Clears channel 0~15 immediate mode
11001010	AUXADC_CON2	32	AUXADC Control Register 2 AUXADC SPL control and status
11001014~ 11001050	AUXADC_DAT[n] (n=0~15)	32	AUXADC Channel n Register Stores sampled data of AUXADC channel n
11001084	AUXADC_DET_VOLT	32	AUXADC Background Detected Control Controls background detection
11001088	AUXADC_DET_SEL	32	AUXADC Background Detected Channel Background detection channel
1100108C	AUXADC_DET_PERIOD	32	Background Detection Period Controls background detection period
11001090	AUXADC_DET_DEBT	32	Background Detection Debounce Controls background detection de-bounce
11001094	AUXADC_MISC	32	AUXADC Misc Control Controls ADC clock and misc
1100109C	AUXADC_SAMPLE_LIST	32	AUXADC Sample List For debugging
110010A0	AUXADC_ABIST_PERIOD	32	AUXADC ABIST Control For ABIST mode
110010A4	AUXADC_TST	32	AUXADC Test Control

11001000 AUXADC_CON0 AUXADC Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOSET15	AUTOSET14	AUTOSET13	AUTOSET12	AUTOSET11	AUTOSET10	AUTOSET9	AUTOSET8	AUTOSET7	AUTOSET6	AUTOSET5	AUTOSET4	AUTOSET3	AUTOSET2	AUTOSET1	AUTOSET0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**AUTOSET15**	AUTOSET15	**Enables auto set for CH15** 0: Not AUTOSET mode 1: AUTOSET mode
14	**AUTOSET14**	AUTOSET14	**Enables auto set for CH14** 0: Not AUTOSET mode 1: AUTOSET mode

Bit(s)	Mnemonic	Name	Description
13	**AUTOSET13**	AUTOSET13	**Enables auto set for CH13** 0: Not AUTOSET mode 1: AUTOSET mode
12	**AUTOSET12**	AUTOSET12	**Enables auto set for CH12** 0: Not AUTOSET mode 1: AUTOSET mode
11	**AUTOSET11**	AUTOSET11	**Enables auto set for CH11** 0: Not AUTOSET mode 1: AUTOSET mode
10	**AUTOSET10**	AUTOSET10	**Enables auto set for CH10** 0: Not AUTOSET mode 1: AUTOSET mode
9	**AUTOSET9**	AUTOSET9	**Enables auto set for CH09** 0: Not AUTOSET mode 1: AUTOSET mode
8	**AUTOSET8**	AUTOSET8	**Enables auto set for CH08** 0: Not AUTOSET mode 1: AUTOSET mode
7	**AUTOSET7**	AUTOSET7	**Enables auto set for CH07** 0: Not AUTOSET mode 1: AUTOSET mode
6	**AUTOSET6**	AUTOSET6	**Enables auto set for CH06** 0: Not AUTOSET mode 1: AUTOSET mode
5	**AUTOSET5**	AUTOSET5	**Enables auto set for CH05** 0: Not AUTOSET mode 1: AUTOSET mode
4	**AUTOSET4**	AUTOSET4	**Enables auto set for CH04** 0: Not AUTOSET mode 1: AUTOSET mode
3	**AUTOSET3**	AUTOSET3	**Enables auto set for CH03** 0: Not AUTOSET mode 1: AUTOSET mode
2	**AUTOSET2**	AUTOSET2	**Enables auto set for CH02** 0: Not AUTOSET mode 1: AUTOSET mode
1	**AUTOSET1**	AUTOSET1	**Enables auto set for CH01** 0: Not AUTOSET mode 0: AUTOSET mode
0	**AUTOSET0**	AUTOSET0	**Enables auto set for CH00** 0: Not AUTOSET mode 1: AUTOSET mode

11001004 AUXADC_CON1 AUXADC Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMM15	IMM14	IMM13	IMM12	IMM11	IMM10	IMM9	IMM8	IMM7	IMM6	IMM5	IMM4	IMM3	IMM2	IMM1	IMM0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**IMM15**	IMM15	**Channel 15 immediate mode** 0: Channel 15 is not selected. 1: Channel 15 is selected.
14	**IMM14**	IMM14	**Channel 14 immediate mode** 0: Channel 14 is not selected. 1: Channel 14 is selected.
13	**IMM13**	IMM13	**Channel 13 immediate mode** 0: Channel 13 is not selected. 1: Channel 13 is selected.
12	**IMM12**	IMM12	**Channel 12 immediate mode** 0: Channel 12 is not selected. 1: Channel 12 is selected.
11	**IMM11**	IMM11	**Channel 11 immediate mode** 0: Channel 11 is not selected. 1: Channel 11 is selected.
10	**IMM10**	IMM10	**Channel 10 immediate mode** 0: Channel 10 is not selected. 1: Channel 10 is selected.
9	**IMM9**	IMM9	**Channel 9 immediate mode** 0: Channel 9 is not selected. 1: Channel 9 is selected.
8	**IMM8**	IMM8	**Channel 8 immediate mode** 0: Channel 8 is not selected. 1: Channel 8 is selected.
7	**IMM7**	IMM7	**Channel 7 immediate mode** 0: Channel 7 is not selected. 1: Channel 7 is selected.
6	**IMM6**	IMM6	**Channel 6 immediate mode** 0: Channel 6 is not selected. 1: Channel 6 is selected.
5	**IMM5**	IMM5	**Channel 5 immediate mode** 0: Channel 5 is not selected. 1: Channel 5 is selected.
4	**IMM4**	IMM4	**Channel 4 immediate mode** 0: Channel 4 is not selected. 1: Channel 4 is selected.
3	**IMM3**	IMM3	**Channel 3 immediate mode** 0: Channel 3 is not selected. 1: Channel 3 is selected.
2	**IMM2**	IMM2	**Channel 2 immediate mode** 0: Channel 2 is not selected. 1: Channel 2 is selected.
1	**IMM1**	IMM1	**Channel 1 immediate mode** 0: Channel 1 is not selected. 1: Channel 1 is selected.
0	**IMM0**	IMM0	**Channel 0 immediate mode** 0: Channel 0 is not selected. 1: Channel 0 is selected.

11001008 AUXADC_CON1_SET AUXADC Control Set Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	SET15	SET14	SET13	SET12	SET11	SET10	SET9	SET8	SET7	SET6	SET5	SET4	SET3	SET2	SET1	SET0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	SET15	SET15	Sets up Channel 15 immediate mode
14	SET14	SET14	Sets up Channel 14 immediate mode
13	SET13	SET13	Sets up Channel 13 immediate mode
12	SET12	SET12	Sets up Channel 12 immediate mode
11	SET11	SET11	Sets up Channel 11 immediate mode
10	SET10	SET10	Sets up Channel 10 immediate mode
9	SET9	SET9	Sets up Channel 9 immediate mode
8	SET8	SET8	Sets up Channel 8 immediate mode
7	SET7	SET7	Sets up Channel 7 immediate mode
6	SET6	SET6	Sets up Channel 6 immediate mode
5	SET5	SET5	Sets up Channel 5 immediate mode
4	SET4	SET4	Sets up Channel 4 immediate mode
3	SET3	SET3	Sets up Channel 3 immediate mode
2	SET2	SET2	Sets up Channel 2 immediate mode
1	SET1	SET1	Sets up Channel 1 immediate mode
0	SET0	SET0	Sets up Channel 0 immediate mode

1100100C AUXADC_CON1_CLR AUXADC Control Clear Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLR15	CLR14	CLR13	CLR12	CLR11	CLR10	CLR9	CLR8	CLR7	CLR6	CLR5	CLR4	CLR3	CLR2	CLR1	CLR0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	CLR15	CLR15	Clears Channel 15 immediate mode
14	CLR14	CLR14	Clears Channel 14 immediate mode
13	CLR13	CLR13	Clears Channel 13 immediate mode
12	CLR12	CLR12	Clears Channel 12 immediate mode
11	CLR11	CLR11	Clears Channel 11 immediate mode
10	CLR10	CLR10	Clears Channel 10 immediate mode
9	CLR9	CLR9	Clears Channel 9 immediate mode
8	CLR8	CLR8	Clears Channel 8 immediate mode
7	CLR7	CLR7	Clears Channel 7 immediate mode
6	CLR6	CLR6	Clears Channel 6 immediate mode
5	CLR5	CLR5	Clears Channel 5 immediate mode
4	CLR4	CLR4	Clears Channel 4 immediate mode
3	CLR3	CLR3	Clears Channel 3 immediate mode
2	CLR2	CLR2	Clears Channel 2 immediate mode
1	CLR1	CLR1	Clears Channel 1 immediate mode
0	CLR0	CLR0	Clears Channel 0 immediate mode

1100101O AUXADC_CON2 AUXADC Control Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SOFT_RST							ADC_STA
Type									RW							RO
Reset									0							0

Bit(s)	Mnemonic	Name	Description
7	**RST**	SOFT_RST	**Software resets AUXADC FSM.**
0	**STA**	ADC_STA	**ADC status of AUXADC** 0: Idle status 1: Busy status

11001014~ 11001050 AUXADC_DAT[n](n=0~15) AUXADC Channel n Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RDYn	DATn											
Type				RO	RO											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12	**RDYo**	RDYn	**AUXADC channel n data ready** Cleared after the register is read. 0: Not ready 1: Ready
11:0	**DATo**	DATn	**AUXADC channel n data** Stores the sampled data for channel n.

11001084 AUXADC_DET_VOLT AUXADC Background Detected Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INV				VOL											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**INV**	INV	**Controls background detected**

Bit(s)	Mnemonic	Name	Description
			When the battery voltage is higher or lower than pre-defined voltage (VOLT), the interrupt will be issued to AP. 0: Lower 1: Higher
11:0	**VOL**	VOL	

11001088 AUXADC_DET_SEL AUXADC Background Detected Channel 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**CHSEL**			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**CHSEL**	CHSEL	**Channel to be sampled in background** 0x0: Channel 0 0x1: Channel 1 ... 0xF: Channel 15

1100108C AUXADC_DET_PERIOD Background Detection Period 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**BG_DET_PERIOD**													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13:0	**BGDET**	BG_DET_PERIOD	**Background sample period** When this value is not 0, the background detection will be activated automatically and other ADC sampling functions will be stopped. The counter counts by 32K clock. When counter value is bigger than DET_PERIOD, the detection will be activated.

11001090 AUXADC_DET_DEBT Background Detection Debounce 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			BG_DEBT_TIME													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
13:0	**BGTIME**	BG_DEBT_TIME	**Background de-bounce time** When the number of the detected channel is higher or lower than the pre-defined voltage and exceeds "debounce_time", the interrupt will be issued.

11001094 AUXADC_MISC AUXADC Misc Control 00000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DIV							
Type									RW							
Reset									0	0	0	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DIV**	DIV	**Internal divide count value** 0x0~3: Reserved. Should not be used. 0x4: A/D clock = 26MHz clock/4 0x5: A/D clock = 26MHz clock/5 0x6: A/D clock = 26MHz clock/6 0x7: A/D clock = 26MHz clock/7 0x8: A/D clock = 26MHz clock/8 = 3.25MHz (default) 0x9 ~ 0xFF: Programmable

1100109C AUXADC_SAMPLE_LIST AUXADC Sample List 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SAMPLE_LIST															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**SAMPLE_LIST**	SAMPLE_LIST	**Hardware sample list for debugging**

110010A0 AUXADC_ABIST_PERIOD AUXADC ABIST Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TP_ABIST_EN	ABIST_MODE_EN								ABIST_SPL_PERIOD						
Type	RW	RW								RW						
Reset	0	0								0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**EN**	TP_ABIST_EN	**Enables touch panel ABIST mode** TP will sample when TP_ABIST_EN=1 and ABIST_MODE_EN=1. 0: Disable 1: Enable
14	**MODE_EN**	ABIST_MODE_EN	**Enables ABIST mode** 0: Disable 1: Enable
6:0	**PERIOD**	ABIST_SPL_PERIOD	**Period of two different samples** One period is a ADC clock.

110010A4 AUXADC_TST AUXADC Test Control 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_AUTORPT_PRD													AUXADC_AUTORPT_EN	AUXADC_TEST_SEL	AUXADC_TEST_MODE
Type	RW													RW	RW	RW
Reset	0	0	0	0	0	0	0	1						0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**AUXADC_AUTORPT_PRD**	AUXADC_AUTORPT_PRD	**Period of auto-start**
2	**AUXADC_AUTORPT_EN**	AUXADC_AUTORPT_EN	**Enables AUXADC auto start mode_xoooD_** 0: Disable 1: Enable
1	**AUXADC_TEST_SEL**	AUXADC_TEST_SEL	**Selects AUXADC test mode_xoooD_** 0: In test mode. CHSEL from GPI 1: In test mode. CHSEL from REG
0	**AUXADC_TEST_MODE**	AUXADC_TEST_MODE	**Enables AUXADC test mode_xoooD_** 0: Disable. Normal mode 1: Enable. Use auxadc_test_in from GPI

1.11 UART 0

1.11.1 Introduction

The UART provide full duplex serial communication channels between chip and external devices. The UART has M16C450 and M16550A modes of operation, which are compatible with a range of standard software drivers. The extensions have been designed to be broadly software compatible with 16550A variants, but certain areas offer no consensus.

In common with the M16550A, the UART supports word lengths from 5 to 8 bits, an optional parity bit and one or two stop bits, and is fully programmable by a CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided. The UART also includes two DMA handshake lines, used to indicate when the FIFOs are ready to transfer data to the CPU. Interrupts can be generated from any of the several sources.

After hardware reset, the UART is in M16C450 mode. Its FIFOs can be enabled and the UART can then enter M16550A mode. The UART adds further functionality beyond M16550A mode. Each of the extended functions can be selected individually under software control.

1.11.2 Features

- UART0 is 2 pin (tx, rx) UART channel
- Support both M16C450 and M16550A modes of operation
  - Compatible with standard software drivers
- Transfer system — Asynchronuos
- Data length — 5 to 8 bits
- Software flow control — Use special character Xon/Xoff to do software flow control
- Baud rate — Baud rate is programmable form 300bps to 3Mbps.
- Interrupt request — Received interrupt/Transmit interrupt
- Data transfer — DMA (Transmit/Received) transfer supported.

1.11.3 Block Diagram

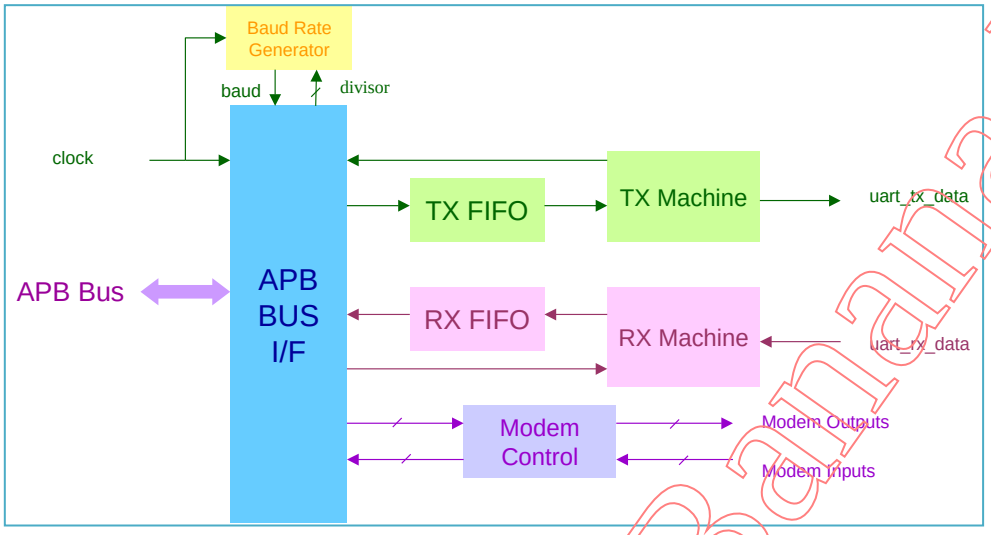


Figure 1-8. Block Diagram of UART

1.11.4 Register Definition

Module name: uart0 Base address: (+11002000h)

Address	Name	Width	Register Function
11002000	RBR_THR	8	RX Buffer Register / TX Holding Register
11002004	IER	8	Interrupt Enable Register By storing a '1' to a specific bit position, the interrupt associated with that bit is enabled. Otherwise, the interrupt is disabled. IER[7:4] are modified when EFR[4] = 1.
11002008	IIR_FCR	8	Interrupt Identification Register / FIFO Control Register priority is from high to low as following .IIR[5:0]==0X1: no interrupt pending .IIR[5:0]==0X6:line status interrup(Under IER[2]=1). IIR[5:0]==0Xc:rx data timeout interrup(Under IER[0]=1). IIR[5:0]==0X4:RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached.(Under IER[0]=1) . IIR[5:0]==0X2: TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level(Under IER[1]=1). IIR[5:0]==0X0: modem status change interrupt(Under IER[3]=1). IIR[5:0]==0X10: XOFF character recieved (Under IER[5]=1,EFR[4] = 1). IIR[5:0]==0X20: CTS or RTS Rising edge (Under IER[7]=1,IER[6]=1,EFR[4] = 1).
1100200C	LCR	8	Line Control Register Line Control Register. Determines characteristics of serial communication signals.
11002010	MCR	8	Modem Control Register Modem Control Register. Control interface signals of the UART. MCR[7] can be read when EFR[4] = 1.

Address	Name	Width	Register Function
11002014	LSR	8	Line Status Register Line Status Register.
11002018	MSR	8	Modem Status Register Note: After a reset, D4-D7 are inputs. A modem status interrupt can be cleared by writing '0' to D0-D3or reading this register. And can be set by writing '1' to D0-D3 or input has changed. D0-D3 can be Modified when != BFh.
1100201C	SCR	8	Scratch Register A general purpose read/write register. After reset, its value is un-defined.
11002090	DLL	8	Divisor Latch (LS) uesd to divid the bclk frequency .
11002094	DLM	8	Divisor Latch (MS) uesd to divid the bclk frequency .
11002098	EFR	8	Enhanced Feature Register
110020A0	XON1	8	XON1 Char Register
110020A4	XON2	8	XON2 Char Register
110020A8	XOFF1	8	XOFF1 Char Register
110020AC	XOFF2	8	XOFF2 Char Register
11002020	AUTOBAUD_EN	8	Auto Baud Detect Enable Register
11002024	HIGHSPEED	8	High Speed Mode Register
11002028	SAMPLE_COUNT	8	Sample Counter Register When HIGHSPEED=3, the sample_count is the threshold value for UART sample counter (sample_num). Count from 0 to sample_count.
1100202C	SAMPLE_POINT	8	Sample Point Register When HIGHSPEED=3, UART gets the input data when sample_count=sample_num. e.g. system clock = 13MHz, 921600 = 13000000 / 14 sample_count = 13 and sample point = 6 (sample the central point to decrease the inaccuracy) The SAMPLE_POINT is usually (SAMPLE_COUNT-1)/2 and remove the decimal.
11002030	AUTOBAUD_REG	8	Auto Baud Monitor Register the autobaud detection state ,it will not change until enable the autobaud_en again.
11002034	RATEFIX_AD	8	Clock Rate Fix Register
11002038	AUTOBAUDSAMPLE	8	Auto Baud Sample Register Since the system clock may change, autobaud sample duration should change as system clock changes. When system clock = 13MHz, autobaudsample = 6; when system clock = 26MHz, autobaudsample = 13;When system clock = 52MHz, autobaudsample = 27.
1100203C	GUARD	8	Guard time added register
11002040	ESCAPE_DAT	8	Escape character register
11002044	ESCAPE_EN	8	Escape enable register
11002048	SLEEP_EN	8	Sleep enable register
1100204C	DMA_EN	8	DMA enable register
11002050	RXTRI_AD	8	Rx Trigger Address
11002054	FRACDIV_L	8	Fractional Divider LSB Address

Address	Name	Width	Register Function
11002058	FRACDIV_M	8	Fractional Divider MSB Address
1100205C	FCR_RD	8	FIFO Control Register
1100209C	FEATURE_SEL	8	UART Feature Select Register For ap mcu side UART ,if use new UART register map feature_sel should keep 1.
110020B0	USB_RX_SEL	8	UART USB rx pin Selection Register
110020B4	SLEEP_REQ	8	uart sleep request register.
110020B8	SLEEP_ACK	8	uart idle register.
110020BC	SPM_SEL	8	SPM interface selection register

11002000 RBR_THR RX Buffer Register / TX Holding Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RBR_THR							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RBR_THR	**For read : The received data can be read by accessing this register.** For write : The data to be transmitted is written to this register, and then sent to the PC via serial communication.

11002004 IER Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CTSI	RTSI	XOFFI		EDSSI	ELSI	ETBEI	ERBFI
Type									RW	RW	RW		RW	RW	RW	RW
Reset									0	0	0		0	0	0	0

Bit(s)	Name	Description
7	CTSI	**Masks an interrupt that is generated when a rising edge is detected on the CTS modem control line.** Note: This interrupt is only enabled when hardware flow control is enabled. 0: Mask an interrupt that is generated when a rising edge is detected on the CTS modem control line. 1: Unmask an interrupt that is generated when a rising edge is detected on the CTS modem control line.
6	RTSI	**Masks an interrupt that is generated when a rising edge is detected on the RTS modem control line.**

Bit(s)	Name	Description
		Note: This interrupt is only enabled when hardware flow control is enabled. 0: Mask an interrupt that is generated when a rising edge is detected on the RTS modem control line. 1: Unmask an interrupt that is generated when a rising edge is detected on the RTS modem control line.
5	XOFFI	**Masks an interrupt that is generated when an XOFF character is received.** Note: This interrupt is only enabled when software flow control is enabled. 0: Mask an interrupt that is generated when an XOFF character is received. 1: Unmask an interrupt that is generated when an XOFF character is received.
3	EDSSI	**When set ("1"), an interrupt is generated if DCTS (MSR[0]) becomes set.** 0: No interrupt is generated if DCTS (MSR[0]) becomes set. 1: An interrupt is generated if DCTS (MSR[0]) becomes set.
2	ELSI	**When set ("1"), an interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.** 0: No interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set. 1: An interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.
1	ETBEI	**When set ("1"), an interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level.** 0: No interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level. 1: An interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level
0	ERBFI	**When set ("1"), an interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached.** 0: No interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. 1: An interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached.

11002008 IIR_FCR Interrupt Identification Register / FIFO Control Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**FIFOE_or_RFTL1_RFTLo**		**ID_or_FIFO_ctrl**					
Type									RW		RW					
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:6	FIFOE_or_RFTL1_RFTL0	**RX FIFO trigger threshold. (RX FIFO contains total 32 bytes.)** 0: 1 1: 6 2: 12 3: RXTRIG
5:0	ID_or_FIFO_ctrl	**IIR_FCR[5:0] for read** Priority Level Interrupt Source 000001 - No interrupt pending 000110 1 Line Status Interrupt: BI, FE, PE or OE set in LSR. (Under IER[2]=1) 001100 2 RX Data Timeout: Timeout on character in RX FIFO. (Under IER[0]=1) 000100 3 RX Data Received: RX Data received or RX Trigger Level reached. (Under IER[0]=1) 000010 4 TX Holding Register Empty: TX Holding Register empty or TX FIFO Trigger Level reached. (Under IER[1]=1) 000000 5 Modem Status change: DDCD, TERI, DDSR or DCTS set in MSR. (Under IER[3]=1) 010000 6 Software Flow Control: XOFF Character received. (Under IER[5]=1) 100000 7 Hardware Flow Control: CTS or RTS Rising Edge. (Under IER[7]=1 or IER[6]=1) Line Status Interrupt: A RX Line Status Interrupt (IIR[5:0] == 000110b) is generated if ELSI (IER[2]) is set and any of BI, FE, PE or OE (LSR[4:1]) becomes set. The interrupt is cleared by reading the Line Status Register. RX Data Timeout Interrupt:When virtual FIFO mode is disabled, RX Data Timeout Interrupt is generated if all of the following apply: 1. FIFO contains at least one character; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register, or on a CPU read from the RX FIFO. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading RX FIFO. When virtual FIFO mode is enabled, RX Data Timeout Interrupt is generated if all of the following apply: 1. FIFO is empty; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register or reading DMA_EN register. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading DMA_EN register. RX Data Received Interrupt: A RX Received interrupt (IER[5:0] == 000100b) is generated if EFRBI (IER[0]) is set and either RX Data is placed in the RX Buffer Register or the RX Trigger

Bit(s)	Name	Description
		Level is reached. The interrupt is cleared by reading the RX Buffer Register or the RX FIFO (if enabled). TX Holding Register Empty Interrupt: A TX Holding Register Empty Interrupt (IIR[5:0] = 000010b) is generated if ETRBI (IER[1]) is set and either the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level. The interrupt is cleared by writing to the TX Holding Register or TX FIFO if FIFO enabled. Modem Status Change Interrupt: A Modem Status Change Interrupt (IIR[5:0] = 000000b) is generated if EDSSI (IER[3]) is set and either DDCD, TERI, DDSR or DCTS (MSR[3:0]) becomes set. The interrupt is cleared by reading the Modem Status Register. Software Flow Control Interrupt: A Software Flow Control Interrupt (IIR[5:0] = 010000b) is generated if Software Flow Control is enabled and XOFFI (IER[5]) becomes set, indicating that an XOFF character has been received. The interrupt is cleared by reading the Interrupt Identification Register. Hardware Flow Control Interrupt: A Hardware Flow Control Interrupt (IER[5:0] = 100000b) is generated if Hardware Flow Control is enabled and either RTSI (IER[6]) or CTSI (IER[7]) becomes set indicating that a rising edge has been detected on either the RTS/CTS Modem Control line. The interrupt is cleared by reading the Interrupt Identification Register. ---------- IIR_FCR [5:0] for write IIR_FCR [5:4] TX FIFO trigger threshold (TX FIFO contains total 32 bytes.) 0: 1 1: 6 2: 12 3: RXTRIG IIR_FCR [2] control bit to clear tx fifo 0: no effect 1: clear RX FIFO IIR_FCR [1] control bit to clear rx fifo 0: no effect 1: clear RX FIFO IIR_FCR [0] FIFO Enabled. This bit must be set to 1 for any of the other bits in the registers to have any effect. 0: Disable both the RX and TX FIFOs. 1: Enable both the RX and TX FIFOs.

1100200C LCR Line Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLAB	SB	SP	EPS	PEN	STB	WLS1_WLS0	
Type									RW	RW	RW	RW	RW	RW	RW	
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	DLAB	**Divisor Latch Access Bit.** 0: The RX and TX Registers are read/written at Address 0 and the IER register is read/written at Address 4. 1: The Divisor Latch LS is read/written at Address 0 and the Divisor Latch MS is read/written at Address 4.
6	SB	**Set Break** 0: No effect 1: SOUT signal is forced into the "0" state.
5	SP	**Stick Parity** 0: No effect. 1: The Parity bit is forced into a defined state, depending on the states of EPS and PEN: If EPS=1 & PEN=1, the Parity bit is set and checked = 0. If EPS=0 & PEN=1, the Parity bit is set and checked = 1.
4	EPS	**Even Parity Select** 0: When EPS=0, an odd number of ones is sent and checked. 1: When EPS=1, an even number of ones is sent and checked.
3	PEN	**Parity Enable** 0: The Parity is neither transmitted nor checked. 1: The Parity is transmitted and checked.
2	STB	**Number of STOP bits** 0: One STOP bit is always added. 1: Two STOP bits are added after each character is sent; unless the character length is 5 when 1 STOP bit is added.
1:0	WLS1_WLS0	**Word Length Select.** 0: 5 bits 1: 6 bits 2: 7 bits 3: 8 bits

11002010 MCR Modem Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF_STATUS			Loop			RTS	
Type									RU			RW			RW	

Reset									0			0			0	

Bit(s)	Name	Description
7	XOFF_STATUS	**This is a read-only bit.** 0: When an XON character is received. 1: When an XOFF character is received.
4	Loop	**Loop-back control bit.** 0: No loop-back is enabled. 1: Loop-back mode is enabled.
1	RTS	**Controls the state of the output NRTS, even in loop mode.** 0: RTS will always output 1. 1: RTS's output will be controled by flow control condition.

11002014 LSR Line Status Register 00000060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO ERR	TEMT	THRE	BI	FE	PE	OE	DR
Type									RU	RU	RU	RU	RU	RU	RU	RU
Reset									0	1	1	0	0	0	0	0

Bit(s)	Name	Description
7	FIFOERR	**RX FIFO Error Indicator.** 0: No PE, FE, BI set in the RX FIFO. 1: Set to 1 when there is at least one PE, FE or BI in the RX FIFO.
6	TEMT	**TX Holding Register (or TX FIFO) and the TX Shift Register are empty.** 0: Empty conditions below are not met. 1: If FIFOs are enabled, the bit is set whenever the TX FIFO and the TX Shift Register are empty. If FIFOs are disabled, the bit is set whenever TX Holding Register and TX Shift Register are empty.
5	THRE	**Indicates if there is room for TX Holding Register or TX FIFO is reduced to its Trigger Level.** 0: Reset whenever the contents of the TX FIFO are more than its Trigger Level (FIFOs are enabled), or whenever TX Holding Register is not empty(FIFOs are disabled). 1: Set whenever the contents of the TX FIFO are reduced to its Trigger Level (FIFOs are enabled), or whenever TX Holding Register is empty and ready to accept new data (FIFOs are disabled).
4	BI	**Break Interrupt.** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit is set whenever the SIN is held in the 0 state for more than one transmission time (START bit + DATA bits + PARITY + STOP bits). If the FIFOs are enabled, this error is associated with a corresponding character in the FIFO and is flagged when this byte is at the top of the FIFO. When a break occurs, only one zero character is loaded into the FIFO: the next character

Bit(s)	Name	Description
		transfer is enabled when SIN goes into the marking state and receives the next valid start bit.
3	FE	**Framing Error.** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit is set if the received data did not have a valid STOP bit. If the FIFOs are enabled, the state of this bit is revealed when the byte it refers to is the next to be read.
2	PE	**Parity Error** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit is set if the received data did not have a valid parity bit. If the FIFOs are enabled, the state of this bit is revealed when the referred byte is the next to be read.
1	OE	**Overrun Error.** 0: Reset by the CPU reading this register. 1: If the FIFOs are disabled, this bit is set if the RX Buffer was not read by the CPU before new data from the RX Shift Register overwrote the previous contents. If the FIFOs are enabled, an overrun error occurs when the RX FIFO is full and the RX Shift Register becomes full. OE is set as soon as this happens. The character in the Shift Register is then overwritten, but not transferred to the FIFO.
0	DR	**Data Ready.** 0: Cleared by the CPU reading the RX Buffer or by reading all the FIFO bytes. 1: Set by the RX Buffer becoming full or by the FIFO becoming no empty.

11002018 MSR Modem Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**CTS**				**DCTS**
Type												RU				RW
Reset												0				0

Bit(s)	Name	Description
4	CTS	**Clear To Send.** When Loop = "0", this value is the complement of the NCTS input signal. When Loop = "1", this value is equal to the RTS bit in the Modem Control Register.
0	DCTS	**Delta Clear To Send** 0: Cleared if the state of CTS has not changed since this register was last read. 1: Set if the state of CTS has changed since this register was last read.

1100201C SCR Scratch Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SCR							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SCR	**A general purpose read/write register. After reset, its value is un-defined.**

11002090 DLL Divisor Latch (LS) 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLL							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:0	DLL	**divisor Latch low 8bit data.**

11002094 DLM Divisor Latch (MS) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLM							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DLM	**divisor Latch high 8bit data.** Note: Division by 1 generates a BAUD signal that is constantly high. Note: DLL & DLM setting formula is {DLH,DLL}=(system clock frequency/baud_pulse/baud_rate). When RATE_FIX(RATEFIX_AD[0])=0, system clock frequency = 52MHz. When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=0, system clock frequency = 26MHz.

Bit(s)	Name	Description
		When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=1, system clock frequency = 13MHz. For baud_pulse value refer to HIGH_SPEED(offset=24H) register. e.g. When 52MHz,default speed mode and 115200 baud rate, the {DLH,DLL}=52MHz/16/115200=28.

11002098 EFR Enhanced Feature Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AUTO_CTS	AUTO_RTS		ENABLE_E	SW_FLOW_CONT			
Type									RW	RW		RW	RW			
Reset									0	0		0	0	0	0	0

Bit(s)	Name	Description
7	AUTO_CTS	**Enables hardware transmission flow control** 0: Disabled. 1: Enabled.
6	AUTO_RTS	**Enables hardware reception flow control** 0: Disabled. 1: Enabled.
4	ENABLE_E	**Enables enhancement feature** 0: Disabled. 1: Enabled.
3:0	SW_FLOW_CONT	**Software flow control bits.** 00xx: No TX Flow Control 10xx: Transmit XON1/XOFF1 as flow control bytes 01xx: Transmit XON2/XOFF2 as flow control bytes xx00: No RX Flow Control xx10: Receive XON1/XOFF1 as flow control bytes xx01: Receive XON2/XOFF2 as flow control bytes

110020A0 XON1 XON1 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON1	**XON1 character for software flow control.**

Bit(s)	Name	Description

110020A4 XON2 XON2 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON2	**XON2 character for software flow control.**

110020A8 XOFF1 XOFF1 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF1	**XOFF1 character for software flow control.**

110020AC XOFF2 XOFF2 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF2	**XOFF2 character for software flow control.**

11002020 AUTOBAUD_EN Auto Baud Detect Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														sleep_ack_sel	AUTOBAUD_SEL	AUTOBAUD_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	sleep_ack_sel	0: can send sleep_ack when autobaud_en is enalbed and autobaud state machine and rx is in idle . 1: can not send sleep_ack when autobaud_en is enabled .
1	AUTOBAUD_SEL	**Auto-baud select** 0: support standard baud rate detection . 1: support non_standard baud rate detection(Just support baud from 300 to 115200, it is recommend to use 52MHZ to auto fix) .
0	AUTOBAUD_EN	**Auto-baud enable signal** 0: Auto-baud function disable 1: Auto-baud function enable (UARTn+0024h SPEED should be set 0) Note: when AUTOBAUD_EN is active, there should not A*/a* char before the auto baud char AT/at, if the A*/a* is Inevitable, the autobaud will fail and please disable the AUTOBAUD_EN to reset the autobaud feature and autobaud_en again.

11002024 HIGHSPEED High Speed Mode Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SPEED	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	SPEED	**UART sample counter base** 0: based on 16*baud_pulse, baud_rate = system clock frequency/16/{DLH, DLL} 1: based on 8*baud_pulse, baud_rate = system clock frequency/8/{DLH, DLL} 2: based on 4*baud_pulse, baud_rate = system clock frequency/4/{DLH, DLL} 3: based on sampe_count * baud_pulse, baud_rate = system clock frequency / (sampe_count+1) / {DLM, DLL}

11002028 SAMPLE_COUNT Sample Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLECOUNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SAMPLECOUNT	**Just be useful when HIGHSPEED mode = 3.**

1100202C SAMPLE_POINT Sample Point Register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLEPOINT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SAMPLEPOINT	**The SAMPLE_POINT is usually (SAMPLE_COUNT-1)/2 and remove the decimal.** sample point, is effective only When HIGHSPEED=3

11002030 AUTOBAUD_REG Auto Baud Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BAUD_STAT				BAUD_RATE			
Type									RU				RU			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:4	BAUD_STAT	**Autobaud format** 0: Autobaud is detecting 1: AT_7N1 2: AT_7O1 3: AT_7E1 4:AT_8N1 5: AT_8O1 6: AT_8E1 7: at_7N1 8: at_7E1

Bit(s)	Name	Description
		9: at_7O1 10: at_8N1 11: at_8E1 12: at_8O1 13: Autobaud detection fails
3:0	BAUD_RATE	**Autobaud baud rate** 0: 115200 1: 57600 2: 38400 3: 19200 4: 9600 5: 4800 6: 2400 7: 1200 8: 300 9: 110

11002034 RATEFIX_AD Clock Rate Fix Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FREQ_SEL	AUTOBAUD_RATE_FIX	RATE_FIX
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FREQ_SEL	**0: system clock = UART_CLK_SRC/2** 1: system clock = UART_CLK_SRC/4
1	AUTOBAUD_RATE_FIX	**0: system clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz)** 1: system clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depends on FREQ_SEL)
0	RATE_FIX	**0: system clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz)** 1: system clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depends on FREQ_SEL)

11002038 AUTOBAUDSAMPLE Auto Baud Sample Register 0000000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											AUTOBAUDSAMPLE					
Type											RW					
Reset											0	0	1	1	0	1

Bit(s)	Name	Description
5:0	AUTOBAUDSAMPLE	**clk diveision for autobaud rate dectection.** for standard baud rate detection. system clk 52m :'d 27 system clk 26m :'d 13 system clk 13m :'d 6 for non-standard baud rate detection. :15.

1100203C GUARD Guard time added register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												GUARD_EN	GUARD_CNT			
Type												RW	RW			
Reset												0	1	1	1	1

Bit(s)	Name	Description
4	GUARD_EN	**Guard interval add enable signal.** 0: No guard interval added. 1: Add guard interval after stop bit.
3:0	GUARD_CNT	**Guard interval count value. Guard interval = (1/(system clock / div_step / div)) * GUARD_CNT.**

11002040 ESCAPE_DAT Escape character register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ESCAPE_DAT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	ESCAPE_DAT	**Escape character added before software flow control data and escape character, i.e. if tx data is xon (31h), with esc_en =1, uart transmits data as esc + CEh (~xon).**

11002044 ESCAPE_EN Escape enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ESC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	ESC_EN	**Add escape character in transmitter and remove escape character in receiver by UART.** 0: Do not deal with the escape character. 1: Add escape character in transmitter and remove escape character in receiver.

11002048 SLEEP_EN Sleep enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_EN	**For sleep mode issue** 0: Do not deal with sleep mode indicate signal 1: To activate hardware flow control or software control according to software initial setting when chip enters sleep mode. Releasing hardware flow when chip wakes up; but for software control, uart sends xon when awaken and when FIFO does not reach threshold level.

1100204C DMA_EN DMA enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FIFO_lsr_sel	TO_CNT_AUTORST	TX_DMA_EN	RX_DMA_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	FIFO_lsr_sel	**fifo lsr mode selection** 0: lsr will update automatically with read data from rx fifo.. 1: lsr will hold the first line status error state until you read the lsr register.
2	TO_CNT_AUTORST	**Timeout counter auto reset register** 0: After RX timeout happen, SW shall reset the interrupt by reading UART 0x4C. 1: The timeout counter will be auto reset. Set this register when Rain's new DMA is used.
1	TX_DMA_EN	**TX_DMA mechanism enable signal** 0: Do not use DMA in TX. 1: Use DMA in TX. When this reguster is enabled, the flow control is based on the DMA threshold, and generates a timeout interrupt for DMA.for DMA.
0	RX_DMA_EN	**RX_DMA mechanism enable signal** 0: Do not use DMA in RX 1: Use DMA in RX. When this reguster is enabled, the flow control is based on the DMA threshold, and generates a timeout interrupt

11002050 RXTRI_AD Rx Trigger Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RXTRIG			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RXTRIG	**When {rtm,rtl}=2'b11, The Rx FIFO threshold will be Rxtrig.** The value is suggested to be less than half of RX FIFO size, which is 32 Bytes.

11002054 FRACDIV_L Fractional Divider LSB Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FRACDIV_L							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FRACDIV_L	**Add sampling count (+1) from state data7 to data0, in order to contribute fractional divisor.only when high_speed==3.**

11002058 FRACDIV_M Fractional Divider MSB Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**FRACDIV_M**	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	FRACDIV_M	**Add sampling count when in state stop to parity, in order to contribute fractional divisor.only when high_speed==3.**

1100205C FCR_RD FIFO Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RFTL1_RFTL0**		**TFTL1_TFTL0**			**CLRT**	**CLRR**	**FIFOE**
Type									RO		RO			RO	RO	RO
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:6	RFTL1_RFTL0	**RX FIFO trigger threshold. (RX FIFO contains total 32 bytes.)** 0: 1 1: 6 2: 12 3: RXTRIG
5:4	TFTL1_TFTL0	**TX FIFO trigger threshold (TX FIFO contains total 32 bytes.)** 0: 1 1: 4 2: 8 3: 14
2	CLRT	0: TX FIFO is not cleared 1: TX FIFO is cleared
1	CLRR	0: RX FIFO is not cleared 1: RX FIFOis cleared

Bit(s)	Name	Description
0	FIFOE	**FIFO Enabled. This bit must be set to 1 for any of the other bits in the registers to have any effect.** 0: the RX and TX FIFOs are not enabled.. 1: RX and TX FIFOs are enabled.

1100209C FEATURE_SEL UART Feature Select Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FEATURE_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	FEATURE_SEL	**For ap mcu side UART ,if use new UART register map feature_sel should keep 1.** 0: Disable new register map. 1: Enable new register map.

110020B0 USB_RX_SEL UART USB rx pin Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																USB_RX_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	USB_RX_SEL	0: uart rx pin is selected. 1: usb rx pin is selected.

110020B4 SLEEP_REQ uart sleep request register. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																SLEEP_REQ
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_REQ	0: cancel sleep request to uart.(after wake up sent by cpu) 1: send sleep request to uart.(before sleep sent by cpu)

110020B8 SLEEP_ACK uart idle register. 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_ACK
Type																RU
Reset																1

Bit(s)	Name	Description
0	SLEEP_ACK	0: uart is not in idle state.(cpu can polling this register to get the uart state) 1: uart is in idle state.(cpu can polling this register to get the uart state)

110020BC SPM_SEL SPM interface selection register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SPM_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	SPM_SEL	0: SPM sleep interface will not be used. 1: SPM sleep interface will be used.

1.12 UART 1

1.12.1 Introduction

The UART provide full duplex serial communication channels between chip and external devices. The UART has M16C450 and M16550A modes of operation, which are compatible with a range of standard software drivers. The extensions have been designed to be broadly software compatible with 16550A variants, but certain areas offer no consensus.

In common with the M16550A, the UART supports word lengths from 5 to 8 bits, an optional parity bit and one or two stop bits, and is fully programmable by a CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided. The UART also includes two DMA handshake lines, used to indicate when the FIFOs are ready to transfer data to the CPU. Interrupts can be generated from any of the several sources.

After hardware reset, the UART is in M16C450 mode. Its FIFOs can be enabled and the UART can then enter M16550A mode. The UART adds further functionality beyond M16550A mode. Each of the extended functions can be selected individually under software control.

1.12.2 Features

- UART0 is 2 pin (tx, rx) UART channel
- Support both M16C450 and M16550A modes of operation
  - Compatible with standard software drivers
- Transfer system Asynchronuos
- Data length 5 to 8 bits
- Software flow control Use special character Xon/Xoff to do software flow control
- Baud rate Baud rate is programmable form 300bps to 3Mbps.
- Interrupt request Received interrupt/Transmit interrupt
- Data transfer DMA (Transmit/Received) transfer supported.

1.12.3 Register Definition

Module name: uart1 Base address: (+11003000h)

Address	Name	Width	Register Function
11002000	RBR_THR	8	RX Buffer Register / TX Holding Register
11002004	IER	8	Interrupt Enable Register By storing a '1' to a specific bit position, the interrupt associated with that bit is enabled. Otherwise, the interrupt is disabled. IER[7:4] are modified when EFR[4] = 1.
11002008	IIR_FCR	8	Interrupt Identification Register / FIFO Control Register priority is from high to low as following .IIR[5:0]==0X1: no interrupt pending .IIR[5:0]==0X6:line status interrup(Under IER[2]=1). IIR[5:0]==0Xc:rx data timeout interrup(Under IER[0]=1). IIR[5:0]==0X4:RX Data is placed in the RX

Address	Name	Width	Register Function
			Buffer Register or the RX Trigger Level is reached.(Under IER[0]=1) . IIR[5:0]==0X2: TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level(Under IER[1]=1). IIR[5:0]==0X0: modem status change interrupt(Under IER[3]=1). IIR[5:0]==0X10: XOFF character recieved (Under IER[5]=1,EFR[4] = 1). IIR[5:0]==0X20: CTS or RTS Rising edge (Under IER[7]=1,IER[6]=1,EFR[4] = 1).
1100200C	LCR	8	Line Control Register Line Control Register. Determines characteristics of serial communication signals.
11002010	MCR	8	Modem Control Register Modem Control Register. Control interface signals of the UART. MCR[7] can be read when EFR[4] = 1.
11002014	LSR	8	Line Status Register Line Status Register.
11002018	MSR	8	Modem Status Register Note: After a reset, D4-D7 are inputs. A modem status interrupt can be cleared by writing '0' to D0-D3or reading this register. And can be set by writing '1' to D0-D3 or input has changed. D0-D3 can be Modified when != BFh.
1100201C	SCR	8	Scratch Register A general purpose read/write register. After reset, its value is un-defined.
11002090	DLL	8	Divisor Latch (LS) uesd to divid the bclk frequency .
11002094	DLM	8	Divisor Latch (MS) uesd to divid the bclk frequency .
11002098	EFR	8	Enhanced Feature Register
110020A0	XON1	8	XON1 Char Register
110020A4	XON2	8	XON2 Char Register
110020A8	XOFF1	8	XOFF1 Char Register
110020AC	XOFF2	8	XOFF2 Char Register
11002020	AUTOBAUD_EN	8	Auto Baud Detect Enable Register
11002024	HIGHSPEED	8	High Speed Mode Register
11002028	SAMPLE_COUNT	8	Sample Counter Register When HIGHSPEED=3, the sample_count is the threshold value for UART sample counter (sample_num). Count from 0 to sample_count.
1100202C	SAMPLE_POINT	8	Sample Point Register When HIGHSPEED=3, UART gets the input data when sample_count=sample_num. e.g. system clock = 13MHz, 921600 = 13000000 / 14 sample_count = 13 and sample point = 6 (sample the central point to decrease the inaccuracy) The SAMPLE_POINT is usually (SAMPLE_COUNT-1)/2 and remove the decimal.
11002030	AUTOBAUD_REG	8	Auto Baud Monitor Register the autobaud detection state ,it will not change until enable the autobaud_en again.

Address	Name	Width	Register Function
11002034	RATEFIX_AD	8	Clock Rate Fix Register
11002038	AUTOBAUDSAMPLE	8	Auto Baud Sample Register Since the system clock may change, autobaud sample duration should change as system clock changes. When system clock = 13MHz, autobaudsample = 6; when system clock = 26MHz, autobaudsample = 13; When system clock = 52MHz, autobaudsample = 27.
1100203C	GUARD	8	Guard time added register
11002040	ESCAPE_DAT	8	Escape character register
11002044	ESCAPE_EN	8	Escape enable register
11002048	SLEEP_EN	8	Sleep enable register
1100204C	DMA_EN	8	DMA enable register
11002050	RXTRI_AD	8	Rx Trigger Address
11002054	FRACDIV_L	8	Fractional Divider LSB Address
11002058	FRACDIV_M	8	Fractional Divider MSB Address
1100205C	FCR_RD	8	FIFO Control Register
1100209C	FEATURE_SEL	8	UART Feature Select Register For ap mcu side UART ,if use new UART register map feature_sel should keep 1.
110020B0	USB_RX_SEL	8	UART USB rx pin Selection Register
110020B4	SLEEP_REQ	8	uart sleep request register.
110020B8	SLEEP_ACK	8	uart idle register.
110020BC	SPM_SEL	8	SPM interface selection register

11002000 RBR_THR RX Buffer Register / TX Holding Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RBR_THR**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RBR_THR	**For read : The received data can be read by accessing this register.** For write : The data to be transmitted is written to this register, and then sent to the PC via serial communication.

11002004 IER Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CTSI	RTSI	XOFFI		EDSSI	ELSI	ETBEI	ERBFI
Type									RW	RW	RW		RW	RW	RW	RW
Reset									0	0	0		0	0	0	0

Bit(s)	Name	Description
7	CTSI	**Masks an interrupt that is generated when a rising edge is detected on the CTS modem control line.** Note: This interrupt is only enabled when hardware flow control is enabled. 0: Mask an interrupt that is generated when a rising edge is detected on the CTS modem control line. 1: Unmask an interrupt that is generated when a rising edge is detected on the CTS modem control line.
6	RTSI	**Masks an interrupt that is generated when a rising edge is detected on the RTS modem control line.** Note: This interrupt is only enabled when hardware flow control is enabled. 0: Mask an interrupt that is generated when a rising edge is detected on the RTS modem control line. 1: Unmask an interrupt that is generated when a rising edge is detected on the RTS modem control line.
5	XOFFI	**Masks an interrupt that is generated when an XOFF character is received.** Note: This interrupt is only enabled when software flow control is enabled. 0: Mask an interrupt that is generated when an XOFF character is received. 1: Unmask an interrupt that is generated when an XOFF character is received.
3	EDSSI	**When set ("1"), an interrupt is generated if DCTS (MSR[0]) becomes set.** 0: No interrupt is generated if DCTS (MSR[0]) becomes set. 1: An interrupt is generated if DCTS (MSR[0]) becomes set.
2	ELSI	**When set ("1"), an interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.** 0: No interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set. 1: An interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.
1	ETBEI	**When set ("1"), an interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level.** 0: No interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level. 1: An interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level
0	ERBFI	**When set ("1"), an interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached.** 0: No interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. 1: An interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached.

11002008 IIR_FCR Interrupt Identification Register / FIFO Control Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOE_or_RFTL1_RFTL0		ID_or_FIFO_ctrl					
Type									RW		RW					
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:6	FIFOE_or_RFTL1_RFTL0	**RX FIFO trigger threshold. (RX FIFO contains total 32 bytes.)** 0: 1 1: 6 2: 12 3: RXTRIG
5:0	ID_or_FIFO_ctrl	**IIR_FCR[5:0] for read** Priority Level Interrupt Source 000001 - No interrupt pending 000110 1 Line Status Interrupt: BI, FE, PE or OE set in LSR. (Under IER[2]=1) 001100 2 RX Data Timeout: Timeout on character in RX FIFO. (Under IER[0]=1) 000100 3 RX Data Received: RX Data received or RX Trigger Level reached. (Under IER[0]=1) 000010 4 TX Holding Register Empty: TX Holding Register empty or TX FIFO Trigger Level reached. (Under IER[1]=1) 000000 5 Modem Status change: DDCD, TERI, DDSR or DCTS set in MSR. (Under IER[3]=1) 010000 6 Software Flow Control: XOFF Character received. (Under IER[5]=1) 100000 7 Hardware Flow Control: CTS or RTS Rising Edge. (Under IER[7]=1 or IER[6]=1) Line Status Interrupt: A RX Line Status Interrupt (IIR[5:0] == 000110b) is generated if ELSI (IER[2]) is set and any of BI, FE, PE or OE (LSR[4:1]) becomes set. The interrupt is cleared by reading the Line Status Register. RX Data Timeout Interrupt:When virtual FIFO mode is disabled, RX Data Timeout Interrupt is generated if all of the following apply: 1. FIFO contains at least one character; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register, or on a CPU read from the RX FIFO. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading RX FIFO.

Bit(s)	Name	Description
		When virtual FIFO mode is enabled, RX Data Timeout Interrupt is generated if all of the following apply: 1. FIFO is empty; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register or reading DMA_EN register. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading DMA_EN register. RX Data Received Interrupt: A RX Received interrupt (IER[5:0] == 000100b) is generated if EFRBI (IER[0]) is set and either RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. The interrupt is cleared by reading the RX Buffer Register or the RX FIFO (if enabled). TX Holding Register Empty Interrupt: A TX Holding Register Empty Interrupt (IIR[5:0] = 000010b) is generated if ETRBI (IER[1]) is set and either the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level. The interrupt is cleared by writing to the TX Holding Register or TX FIFO if FIFO enabled. Modem Status Change Interrupt: A Modem Status Change Interrupt (IIR[5:0] = 000000b) is generated if EDSSI (IER[3]) is set and either DDCD, TERI, DDSR or DCTS (MSR[3:0]) becomes set. The interrupt is cleared by reading the Modem Status Register. Software Flow Control Interrupt: A Software Flow Control Interrupt (IIR[5:0] = 010000b) is generated if Software Flow Control is enabled and XOFFI (IER[5]) becomes set, indicating that an XOFF character has been received. The interrupt is cleared by reading the Interrupt Identification Register. Hardware Flow Control Interrupt: A Hardware Flow Control Interrupt (IER[5:0] = 100000b) is generated if Hardware Flow Control is enabled and either RTSI (IER[6]) or CTSI (IER[7]) becomes set indicating that a rising edge has been detected on either the RTS/CTS Modem Control line. The interrupt is cleared by reading the Interrupt Identification Register. ---------- IIR_FCR [5:0] for write IIR_FCR [5:4] TX FIFO trigger threshold (TX FIFO contains total 32 bytes.) 0: 1 1: 6 2: 12 3: RXTRIG IIR_FCR [2] control bit to clear tx fifo

Bit(s)	Name	Description
		0: no effect 1: clear RX FIFO IIR_FCR [1] control bit to clear rx fifo 0: no effect 1: clear RX FIFO IIR_FCR [0] FIFO Enabled. This bit must be set to 1 for any of the other bits in the registers to have any effect. 0: Disable both the RX and TX FIFOs. 1: Enable both the RX and TX FIFOs.

1100200C LCR Line Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLAB	SB	SP	EPS	PEN	STB	WLS1_WLS0	
Type									RW	RW	RW	RW	RW	RW	RW	
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	DLAB	**Divisor Latch Access Bit.** 0: The RX and TX Registers are read/written at Address 0 and the IER register is read/written at Address 4. 1: The Divisor Latch LS is read/written at Address 0 and the Divisor Latch MS is read/written at Address 4.
6	SB	**Set Break** 0: No effect 1: SOUT signal is forced into the "0" state.
5	SP	**Stick Parity** 0: No effect. 1: The Parity bit is forced into a defined state, depending on the states of EPS and PEN: If EPS=1 & PEN=1, the Parity bit is set and checked = 0. If EPS=0 & PEN=1, the Parity bit is set and checked = 1.
4	EPS	**Even Parity Select** 0: When EPS=0, an odd number of ones is sent and checked. 1: When EPS=1, an even number of ones is sent and checked.
3	PEN	**Parity Enable** 0: The Parity is neither transmitted nor checked. 1: The Parity is transmitted and checked.
2	STB	**Number of STOP bits** 0: One STOP bit is always added. 1: Two STOP bits are added after each character is sent; unless the character length is 5 when 1 STOP bit is added.
1:0	WLS1_WLS0	**Word Length Select.** 0: 5 bits 1: 6 bits

Bit(s)	Name	Description
		2: 7 bits 3: 8 bits

11002010 MCR Modem Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF_STATUS			Loop			RTS	
Type									RU			RW			RW	
Reset									0			0			0	

Bit(s)	Name	Description
7	XOFF_STATUS	**This is a read-only bit.** 0: When an XON character is received. 1: When an XOFF character is received.
4	Loop	**Loop-back control bit.** 0: No loop-back is enabled. 1: Loop-back mode is enabled.
1	RTS	**Controls the state of the output NRTS, even in loop mode.** 0: RTS will always output 1. 1: RTS's output will be controled by flow control condition.

11002014 LSR Line Status Register 00000060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOERR	TEMT	THRE	BI	FE	PE	OE	DR
Type									RU	RU	RU	RU	RU	RU	RU	RU
Reset									0	1	1	0	0	0	0	0

Bit(s)	Name	Description
7	FIFOERR	**RX FIFO Error Indicator.** 0: No PE, FE, BI set in the RX FIFO. 1: Set to 1 when there is at least one PE, FE or BI in the RX FIFO.
6	TEMT	**TX Holding Register (or TX FIFO) and the TX Shift Register are empty.** 0: Empty conditions below are not met. 1: If FIFOs are enabled, the bit is set whenever the TX FIFO and the TX Shift Register are empty. If FIFOs are disabled, the bit is set whenever TX Holding Register and TX Shift Register are empty.

Bit(s)	Name	Description
5	THRE	**Indicates if there is room for TX Holding Register or TX FIFO is reduced to its Trigger Level.** 0: Reset whenever the contents of the TX FIFO are more than its Trigger Level (FIFOs are enabled), or whenever TX Holding Register is not empty(FIFOs are disabled). 1: Set whenever the contents of the TX FIFO are reduced to its Trigger Level (FIFOs are enabled), or whenever TX Holding Register is empty and ready to accept new data (FIFOs are disabled).
4	BI	**Break Interrupt.** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit is set whenever the SIN is held in the 0 state for more than one transmission time (START bit + DATA bits + PARITY + STOP bits). If the FIFOs are enabled, this error is associated with a corresponding character in the FIFO and is flagged when this byte is at the top of the FIFO. When a break occurs, only one zero character is loaded into the FIFO: the next character transfer is enabled when SIN goes into the marking state and receives the next valid start bit.
3	FE	**Framing Error.** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit is set if the received data did not have a valid STOP bit. If the FIFOs are enabled, the state of this bit is revealed when the byte it refers to is the next to be read.
2	PE	**Parity Error** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit is set if the received data did not have a valid parity bit. If the FIFOs are enabled, the state of this bit is revealed when the referred byte is the next to be read.
1	OE	**Overrun Error.** 0: Reset by the CPU reading this register. 1: If the FIFOs are disabled, this bit is set if the RX Buffer was not read by the CPU before new data from the RX Shift Register overwrote the previous contents. If the FIFOs are enabled, an overrun error occurs when the RX FIFO is full and the RX Shift Register becomes full. OE is set as soon as this happens. The character in the Shift Register is then overwritten, but not transferred to the FIFO.
0	DR	**Data Ready.** 0: Cleared by the CPU reading the RX Buffer or by reading all the FIFO bytes. 1: Set by the RX Buffer becoming full or by the FIFO becoming no empty.

11002018 MSR Modem Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**CTS**				**DCTS**
Type												RU				RW

Reset												0				0

Bit(s)	Name	Description
4	CTS	**Clear To Send.** When Loop = "0", this value is the complement of the NCTS input signal. When Loop = "1", this value is equal to the RTS bit in the Modem Control Register.
0	DCTS	**Delta Clear To Send** 0: Cleared if the state of CTS has not changed since this register was last read. 1: Set if the state of CTS has changed since this register was last read.

1100201C SCR Scratch Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SCR**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SCR	**A general purpose read/write register. After reset, its value is un-defined.**

11002090 DLL Divisor Latch (LS) 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**DLL**							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:0	DLL	**divisor Latch low 8bit data.**

11002094 DLM Divisor Latch (MS) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLM							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DLM	**divisor Latch high 8bit data.** Note: Division by 1 generates a BAUD signal that is constantly high. Note: DLL & DLM setting formula is {DLH,DLL}=(system clock frequency/baud_pulse/baud_rate). When RATE_FIX(RATEFIX_AD[0])=0, system clock frequency = 52MHz. When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=0, system clock frequency = 26MHz. When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=1, system clock frequency = 13MHz. For baud_pulse value refer to HIGH_SPEED(offset=24H) register. e.g. When 52MHz,default speed mode and 115200 baud rate, the {DLH,DLL}=52MHz/16/115200=28.

11002098 EFR Enhanced Feature Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AUTO_CTS	AUTO_RTS		ENABLE_E	SW_FLOW_CONT			
Type									RW	RW		RW	RW			
Reset									0	0		0	0	0	0	0

Bit(s)	Name	Description
7	AUTO_CTS	**Enables hardware transmission flow control** 0: Disabled. 1: Enabled.
6	AUTO_RTS	**Enables hardware reception flow control** 0: Disabled. 1: Enabled.
4	ENABLE_E	**Enables enhancement feature** 0: Disabled. 1: Enabled.
3:0	SW_FLOW_CONT	**Software flow control bits.** 00xx: No TX Flow Control 10xx: Transmit XON1/XOFF1 as flow control bytes 01xx: Transmit XON2/XOFF2 as flow control bytes xx00: No RX Flow Control xx10: Receive XON1/XOFF1 as flow control bytes xx01: Receive XON2/XOFF2 as flow control bytes

110020A0 XON1 XON1 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON1	**XON1 character for software flow control.**

110020A4 XON2 XON2 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON2	**XON2 character for software flow control.**

110020A8 XOFF1 XOFF1 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF1	**XOFF1 character for software flow control.**

110020AC XOFF2 XOFF2 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF2	**XOFF2 character for software flow control.**

11002020 AUTOBAUD_EN Auto Baud Detect Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														sleep_ack_sel	AUTOBAUD_SEL	AUTOBAUD_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	sleep_ack_sel	0: can send sleep_ack when autobaud_en is enalbed and autobaud state machine and rx is in idle . 1: can not send sleep_ack when autobaud_en is enabled .
1	AUTOBAUD_SEL	**Auto-baud select** 0: support standard baud rate detection . 1: support non_standard baud rate detection(Just support baud from 300 to 115200, it is recommend to use 52MHZ to auto fix) .
0	AUTOBAUD_EN	**Auto-baud enable signal** 0: Auto-baud function disable 1: Auto-baud function enable (UARTn+0024h SPEED should be set 0) Note: when AUTOBAUD_EN is active, there should not A*/a* char before the auto baud char AT/at, if the A*/a* is Inevitable, the autobaud will fail and please disable the AUTOBAUD_EN to reset the autobaud feature and autobaud_en again.

11002024 HIGHSPEED High Speed Mode Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SPEED	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	SPEED	**UART sample counter base** 0: based on 16*baud_pulse, baud_rate = system clock frequency/16/{DLH, DLL} 1: based on 8*baud_pulse, baud_rate = system clock frequency/8/{DLH, DLL} 2: based on 4*baud_pulse, baud_rate = system clock frequency/4/{DLH, DLL} 3: based on sampe_count * baud_pulse, baud_rate = system clock frequency / (sampe_count+1) / {DLM, DLL}

11002028 SAMPLE_COUNT Sample Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLECOUNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SAMPLECOUNT	**Just be useful when HIGHSPEED mode = 3.**

1100202C SAMPLE_POINT Sample Point Register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLEPOINT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SAMPLEPOINT	**The SAMPLE_POINT is usually (SAMPLE_COUNT-1)/2 and remove the decimal.** sample point , is effective only When HIGHSPEED=3

11002030 AUTOBAUD_REG Auto Baud Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BAUD_STAT				BAUD_RATE			
Type									RU				RU			

Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:4	BAUD_STAT	**Autobaud format** 0: Autobaud is detecting 1: AT_7N1 2: AT_7O1 3: AT_7E1 4:AT_8N1 5: AT_8O1 6: AT_8E1 7: at_7N1 8: at_7E1 9: at_7O1 10: at_8N1 11: at_8E1 12: at_8O1 13: Autobaud detection fails
3:0	BAUD_RATE	**Autobaud baud rate** 0: 115200 1: 57600 2: 38400 3: 19200 4: 9600 5: 4800 6: 2400 7: 1200 8: 300 9: 110

11002034 RATEFIX_AD Clock Rate Fix Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**FREQ_SEL**	**AUTOBAUD_RATE_FIX**	**RATE_FIX**
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FREQ_SEL	**0: system clock = UART_CLK_SRC/2** 1: system clock = UART_CLK_SRC/4
1	AUTOBAUD_RATE_FIX	**0: system clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz)** 1: system clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depends on FREQ_SEL)

Bit(s)	Name	Description
0	RATE_FIX	**0: system clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz)** 1: system clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depends on FREQ_SEL)

11002038 AUTOBAUDSAMPLE Auto Baud Sample Register 0000000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											AUTOBAUDSAMPLE					
Type											RW					
Reset											0	0	1	1	0	1

Bit(s)	Name	Description
5:0	AUTOBAUDSAMPLE	**clk diveision for autobaud rate dectection.** for standard baud rate detection. system clk 52m :'d 27 system clk 26m :'d 13 system clk 13m :'d 6 for non-standard baud rate detection. :15.

1100203C GUARD Guard time added register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												GUARD_EN	GUARD_CNT			
Type												RW	RW			
Reset												0	1	1	1	1

Bit(s)	Name	Description
4	GUARD_EN	**Guard interval add enable signal.** 0: No guard interval added. 1: Add guard interval after stop bit.
3:0	GUARD_CNT	**Guard interval count value. Guard interval = (1/(system clock / div_step / div)) * GUARD_CNT.**

11002040 ESCAPE_DAT Escape character register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ESCAPE_DAT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	ESCAPE_DAT	**Escape character added before software flow control data and escape character, i.e. if tx data is xon (31h), with esc_en =1, uart transmits data as esc + CEh (~xon).**

11002044 ESCAPE_EN Escape enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ESC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	ESC_EN	**Add escape character in transmitter and remove escape character in receiver by UART.** 0: Do not deal with the escape character. 1: Add escape character in transmitter and remove escape character in receiver.

11002048 SLEEP_EN Sleep enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_EN	**For sleep mode issue** 0: Do not deal with sleep mode indicate signal 1: To activate hardware flow control or software control according to software initial setting when chip enters sleep mode. Releasing hardware flow when chip wakes up; but for software control, uart sends xon when awaken and when FIFO does not reach threshold level.

1100204C DMA_EN DMA enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FIFO_lsr_sel	TO_CNT_AUTORST	TX_DMA_EN	RX_DMA_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	FIFO_lsr_sel	**fifo lsr mode selection** 0: lsr will update automatically with read data from rx fifo.. 1: lsr will hold the first line status error state until you read the lsr register.
2	TO_CNT_AUTORST	**Timeout counter auto reset register** 0: After RX timeout happen, SW shall reset the interrupt by reading UART 0x4C. 1: The timeout counter will be auto reset. Set this register when Rain's new DMA is used.
1	TX_DMA_EN	**TX_DMA mechanism enable signal** 0: Do not use DMA in TX. 1: Use DMA in TX. When this reguster is enabled, the flow control is based on the DMA threshold, and generates a timeout interrupt for DMA.for DMA.
0	RX_DMA_EN	**RX_DMA mechanism enable signal** 0: Do not use DMA in RX 1: Use DMA in RX. When this reguster is enabled, the flow control is based on the DMA threshold, and generates a timeout interrupt

11002050 RXTRI_AD Rx Trigger Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RXTRIG			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RXTRIG	**When {rtm,rtl}=2'b11, The Rx FIFO threshold will be Rxtrig.** The value is suggested to be less than half of RX FIFO size, which is 32 Bytes.

11002054 FRACDIV_L Fractional Divider LSB Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FRACDIV_L							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FRACDIV_L	**Add sampling count (+1) from state data7 to data0, in order to contribute fractional divisor.only when high_speed==3.**

11002058 FRACDIV_M Fractional Divider MSB Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FRACDIV_M	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	FRACDIV_M	**Add sampling count when in state stop to parity, in order to contribute fractional divisor.only when high_speed==3.**

1100205C FCR_RD FIFO Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RFTL1_RFTL0		TFTL1_TFTL0			CLRT	CLRR	FIFOE
Type									RO		RO			RO	RO	RO
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:6	RFTL1_RFTL0	**RX FIFO trigger threshold. (RX FIFO contains total 32 bytes.)** 0: 1 1: 6 2: 12

Bit(s)	Name	Description
		3: RXTRIG
5:4	TFTL1_TFTL0	**TX FIFO trigger threshold (TX FIFO contains total 32 bytes.)** 0: 1 1: 4 2: 8 3: 14
2	CLRT	0: TX FIFO is not cleared 1: TX FIFO is cleared
1	CLRR	0: RX FIFO is not cleared 1: RX FIFOis cleared
0	FIFOE	**FIFO Enabled. This bit must be set to 1 for any of the other bits in the registers to have any effect.** 0: the RX and TX FIFOs are not enabled.. 1: RX and TX FIFOs are enabled.

1100209C FEATURE_SEL UART Feature Select Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**FEATURE_SEL**
Type																RW
Reset																0

Bit(s)	Name	Description
0	FEATURE_SEL	**For ap mcu side UART ,if use new UART register map feature_sel should keep 1.** 0: Disable new register map. 1: Enable new register map.

110020B0 USB_RX_SEL UART USB rx pin Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**USB_RX_SEL**
Type																RW
Reset																0

Bit(s)	Name	Description
0	USB_RX_SEL	0: uart rx pin is selected. 1: usb rx pin is selected.

Bit(s)	Name	Description

110020B4 SLEEP_REQ uart sleep request register. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_REQ
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_REQ	0: cancel sleep request to uart.(after wake up sent by cpu) 1: send sleep request to uart.(before sleep sent by cpu)

110020B8 SLEEP_ACK uart idle register. 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_ACK
Type																RU
Reset																1

Bit(s)	Name	Description
0	SLEEP_ACK	0: uart is not in idle state.(cpu can polling this register to get the uart state) 1: uart is in idle state.(cpu can polling this register to get the uart state)

110020BC SPM_SEL SPM interface selection register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SPM_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	SPM_SEL	0: SPM sleep interface will not be used. 1: SPM sleep interface will be used.

1.13 UART 2

1.13.1 Introduction

The UART provide full duplex serial communication channels between chip and external devices. The UART has M16C450 and M16550A modes of operation, which are compatible with a range of standard software drivers. The extensions have been designed to be broadly software compatible with 16550A variants, but certain areas offer no consensus.

In common with the M16550A, the UART supports word lengths from 5 to 8 bits, an optional parity bit and one or two stop bits, and is fully programmable by a CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided. The UART also includes two DMA handshake lines, used to indicate when the FIFOs are ready to transfer data to the CPU. Interrupts can be generated from any of the several sources.

After hardware reset, the UART is in M16C450 mode. Its FIFOs can be enabled and the UART can then enter M16550A mode. The UART adds further functionality beyond M16550A mode. Each of the extended functions can be selected individually under software control.

1.13.2 Features

- UART0 is 2 pin (tx, rx) UART channel
- Support both M16C450 and M16550A modes of operation
  - Compatible with standard software drivers
- Transfer system Asynchronuos
- Data length 5 to 8 bits
- Software flow control Use special character Xon/Xoff to do software flow control
- Baud rate Baud rate is programmable form 300bps to 3Mbps.
- Interrupt request Received interrupt/Transmit interrupt
- Data transfer DMA (Transmit/Received) transfer supported.

1.13.3 Register Definition

Module name: uart2 Base address: (+11004000h)

Address	Name	Width	Register Function
11002000	RBR_THR	8	RX Buffer Register / TX Holding Register
11002004	IER	8	Interrupt Enable Register By storing a '1' to a specific bit position, the interrupt associated with that bit is enabled. Otherwise, the interrupt is disabled. IER[7:4] are modified when EFR[4] = 1.
11002008	IIR_FCR	8	Interrupt Identification Register / FIFO Control Register priority is from high to low as following .IIR[5:0]==0X1: no interrupt pending .IIR[5:0]==0X6:line status interrup(Under IER[2]=1). IIR[5:0]==0Xc:rx data timeout interrup(Under IER[0]=1). IIR[5:0]==0X4:RX Data is placed in the RX

Address	Name	Width	Register Function
			Buffer Register or the RX Trigger Level is reached.(Under IER[0]=1) . IIR[5:0]==0X2: TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level(Under IER[1]=1). IIR[5:0]==0X0: modem status change interrupt(Under IER[3]=1). IIR[5:0]==0X10: XOFF character recieved (Under IER[5]=1,EFR[4] = 1). IIR[5:0]==0X20: CTS or RTS Rising edge (Under IER[7]=1,IER[6]=1,EFR[4] = 1).
1100200C	LCR	8	Line Control Register Line Control Register. Determines characteristics of serial communication signals.
11002010	MCR	8	Modem Control Register Modem Control Register. Control interface signals of the UART. MCR[7] can be read when EFR[4] = 1.
11002014	LSR	8	Line Status Register Line Status Register.
11002018	MSR	8	Modem Status Register Note: After a reset, D4-D7 are inputs. A modem status interrupt can be cleared by writing '0' to D0-D3or reading this register. And can be set by writing '1' to D0-D3 or input has changed. D0-D3 can be Modified when != BFh.
1100201C	SCR	8	Scratch Register A general purpose read/write register. After reset, its value is un-defined.
11002090	DLL	8	Divisor Latch (LS) uesd to divid the bclk frequency .
11002094	DLM	8	Divisor Latch (MS) uesd to divid the bclk frequency .
11002098	EFR	8	Enhanced Feature Register
110020A0	XON1	8	XON1 Char Register
110020A4	XON2	8	XON2 Char Register
110020A8	XOFF1	8	XOFF1 Char Register
110020AC	XOFF2	8	XOFF2 Char Register
11002020	AUTOBAUD_EN	8	Auto Baud Detect Enable Register
11002024	HIGHSPEED	8	High Speed Mode Register
11002028	SAMPLE_COUNT	8	Sample Counter Register When HIGHSPEED=3, the sample_count is the threshold value for UART sample counter (sample_num). Count from 0 to sample_count.
1100202C	SAMPLE_POINT	8	Sample Point Register When HIGHSPEED=3, UART gets the input data when sample_count=sample_num. e.g. system clock = 13MHz, 921600 = 13000000 / 14 sample_count = 13 and sample point = 6 (sample the central point to decrease the inaccuracy) The SAMPLE_POINT is usually (SAMPLE_COUNT-1)/2 and remove the decimal.
11002030	AUTOBAUD_REG	8	Auto Baud Monitor Register the autobaud detection state ,it will not change until enable the autobaud_en again.

Address	Name	Width	Register Function
11002034	RATEFIX_AD	8	Clock Rate Fix Register
11002038	AUTOBAUDSAMPLE	8	Auto Baud Sample Register Since the system clock may change, autobaud sample duration should change as system clock changes. When system clock = 13MHz, autobaudsample = 6; when system clock = 26MHz, autobaudsample = 13; When system clock = 52MHz, autobaudsample = 27.
1100203C	GUARD	8	Guard time added register
11002040	ESCAPE_DAT	8	Escape character register
11002044	ESCAPE_EN	8	Escape enable register
11002048	SLEEP_EN	8	Sleep enable register
1100204C	DMA_EN	8	DMA enable register
11002050	RXTRI_AD	8	Rx Trigger Address
11002054	FRACDIV_L	8	Fractional Divider LSB Address
11002058	FRACDIV_M	8	Fractional Divider MSB Address
1100205C	FCR_RD	8	FIFO Control Register
1100209C	FEATURE_SEL	8	UART Feature Select Register For ap mcu side UART ,if use new UART register map feature_sel should keep 1.
110020B0	USB_RX_SEL	8	UART USB rx pin Selection Register
110020B4	SLEEP_REQ	8	uart sleep request register.
110020B8	SLEEP_ACK	8	uart idle register.
110020BC	SPM_SEL	8	SPM interface selection register

11002000 RBR_THR RX Buffer Register / TX Holding Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RBR_THR**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RBR_THR	**For read : The received data can be read by accessing this register.** For write : The data to be transmitted is written to this register, and then sent to the PC via serial communication.

11002004 IER Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CTSI	RTSI	XOFFI		EDSSI	ELSI	ETBEI	ERBFI
Type									RW	RW	RW		RW	RW	RW	RW
Reset									0	0	0		0	0	0	0

Bit(s)	Name	Description
7	CTSI	**Masks an interrupt that is generated when a rising edge is detected on the CTS modem control line.** Note: This interrupt is only enabled when hardware flow control is enabled. 0: Mask an interrupt that is generated when a rising edge is detected on the CTS modem control line. 1: Unmask an interrupt that is generated when a rising edge is detected on the CTS modem control line.
6	RTSI	**Masks an interrupt that is generated when a rising edge is detected on the RTS modem control line.** Note: This interrupt is only enabled when hardware flow control is enabled. 0: Mask an interrupt that is generated when a rising edge is detected on the RTS modem control line. 1: Unmask an interrupt that is generated when a rising edge is detected on the RTS modem control line.
5	XOFFI	**Masks an interrupt that is generated when an XOFF character is received.** Note: This interrupt is only enabled when software flow control is enabled. 0: Mask an interrupt that is generated when an XOFF character is received. 1: Unmask an interrupt that is generated when an XOFF character is received.
3	EDSSI	**When set ("1"), an interrupt is generated if DCTS (MSR[0]) becomes set.** 0: No interrupt is generated if DCTS (MSR[0]) becomes set. 1: An interrupt is generated if DCTS (MSR[0]) becomes set.
2	ELSI	**When set ("1"), an interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.** 0: No interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set. 1: An interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.
1	ETBEI	**When set ("1"), an interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level.** 0: No interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level. 1: An interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level
0	ERBFI	**When set ("1"), an interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached.** 0: No interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. 1: An interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached.

11002008 IIR_FCR Interrupt Identification Register / FIFO Control Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOE_or_RFTL1_RFTL0		ID_or_FIFO_ctrl					
Type									RW		RW					
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:6	FIFOE_or_RFTL1_RFTL0	**RX FIFO trigger threshold. (RX FIFO contains total 32 bytes.)** 0: 1 1: 6 2: 12 3: RXTRIG
5:0	ID_or_FIFO_ctrl	**IIR_FCR[5:0] for read** Priority Level Interrupt Source 000001 - No interrupt pending 000110 1 Line Status Interrupt: BI, FE, PE or OE set in LSR. (Under IER[2]=1) 001100 2 RX Data Timeout: Timeout on character in RX FIFO. (Under IER[0]=1) 000100 3 RX Data Received: RX Data received or RX Trigger Level reached. (Under IER[0]=1) 000010 4 TX Holding Register Empty: TX Holding Register empty or TX FIFO Trigger Level reached. (Under IER[1]=1) 000000 5 Modem Status change: DDCD, TERI, DDSR or DCTS set in MSR. (Under IER[3]=1) 010000 6 Software Flow Control: XOFF Character received. (Under IER[5]=1) 100000 7 Hardware Flow Control: CTS or RTS Rising Edge. (Under IER[7]=1 or IER[6]=1) Line Status Interrupt: A RX Line Status Interrupt (IIR[5:0] == 000110b) is generated if ELSI (IER[2]) is set and any of BI, FE, PE or OE (LSR[4:1]) becomes set. The interrupt is cleared by reading the Line Status Register. RX Data Timeout Interrupt:When virtual FIFO mode is disabled, RX Data Timeout Interrupt is generated if all of the following apply: 1. FIFO contains at least one character; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register, or on a CPU read from the RX FIFO. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading RX FIFO.

Bit(s)	Name	Description
		When virtual FIFO mode is enabled, RX Data Timeout Interrupt is generated if all of the following apply: 1. FIFO is empty; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register or reading DMA_EN register. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading DMA_EN register. RX Data Received Interrupt: A RX Received interrupt (IER[5:0] == 000100b) is generated if EFRBI (IER[0]) is set and either RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. The interrupt is cleared by reading the RX Buffer Register or the RX FIFO (if enabled). TX Holding Register Empty Interrupt: A TX Holding Register Empty Interrupt (IIR[5:0] = 000010b) is generated if ETRBI (IER[1]) is set and either the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level. The interrupt is cleared by writing to the TX Holding Register or TX FIFO if FIFO enabled. Modem Status Change Interrupt: A Modem Status Change Interrupt (IIR[5:0] = 000000b) is generated if EDSSI (IER[3]) is set and either DDCD, TERI, DDSR or DCTS (MSR[3:0]) becomes set. The interrupt is cleared by reading the Modem Status Register. Software Flow Control Interrupt: A Software Flow Control Interrupt (IIR[5:0] = 010000b) is generated if Software Flow Control is enabled and XOFFI (IER[5]) becomes set, indicating that an XOFF character has been received. The interrupt is cleared by reading the Interrupt Identification Register. Hardware Flow Control Interrupt: A Hardware Flow Control Interrupt (IER[5:0] = 100000b) is generated if Hardware Flow Control is enabled and either RTSI (IER[6]) or CTSI (IER[7]) becomes set indicating that a rising edge has been detected on either the RTS/CTS Modem Control line. The interrupt is cleared by reading the Interrupt Identification Register. --- IIR_FCR [5:0] for write IIR_FCR [5:4] TX FIFO trigger threshold (TX FIFO contains total 32 bytes.) 0: 1 1: 6 2: 12 3: RXTRIG IIR_FCR [2] control bit to clear tx fifo

Bit(s)	Name	Description
		0: no effect 1: clear RX FIFO IIR_FCR [1] control bit to clear rx fifo 0: no effect 1: clear RX FIFO IIR_FCR [0] FIFO Enabled. This bit must be set to 1 for any of the other bits in the registers to have any effect. 0: Disable both the RX and TX FIFOs. 1: Enable both the RX and TX FIFOs.

1100200C LCR Line Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLAB	SB	SP	EPS	PEN	STB	WLS1_WLS0	
Type									RW	RW	RW	RW	RW	RW	RW	
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	DLAB	**Divisor Latch Access Bit.** 0: The RX and TX Registers are read/written at Address 0 and the IER register is read/written at Address 4. 1: The Divisor Latch LS is read/written at Address 0 and the Divisor Latch MS is read/written at Address 4.
6	SB	**Set Break** 0: No effect 1: SOUT signal is forced into the "0" state.
5	SP	**Stick Parity** 0: No effect. 1: The Parity bit is forced into a defined state, depending on the states of EPS and PEN: If EPS=1 & PEN=1, the Parity bit is set and checked = 0. If EPS=0 & PEN=1, the Parity bit is set and checked = 1.
4	EPS	**Even Parity Select** 0: When EPS=0, an odd number of ones is sent and checked. 1: When EPS=1, an even number of ones is sent and checked.
3	PEN	**Parity Enable** 0: The Parity is neither transmitted nor checked. 1: The Parity is transmitted and checked.
2	STB	**Number of STOP bits** 0: One STOP bit is always added. 1: Two STOP bits are added after each character is sent; unless the character length is 5 when 1 STOP bit is added.
1:0	WLS1_WLS0	**Word Length Select.** 0: 5 bits 1: 6 bits

Bit(s)	Name	Description
		2: 7 bits 3: 8 bits

11002010 MCR Modem Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF_STATUS			Loop			RTS	
Type									RU			RW			RW	
Reset									0			0			0	

Bit(s)	Name	Description
7	XOFF_STATUS	**This is a read-only bit.** 0: When an XON character is received. 1: When an XOFF character is received.
4	Loop	**Loop-back control bit.** 0: No loop-back is enabled. 1: Loop-back mode is enabled.
1	RTS	**Controls the state of the output NRTS, even in loop mode.** 0: RTS will always output 1. 1: RTS's output will be controled by flow control condition.

11002014 LSR Line Status Register 00000060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOERR	TEMT	THRE	BI	FE	PE	OE	DR
Type									RU	RU	RU	RU	RU	RU	RU	RU
Reset									0	1	1	0	0	0	0	0

Bit(s)	Name	Description
7	FIFOERR	**RX FIFO Error Indicator.** 0: No PE, FE, BI set in the RX FIFO. 1: Set to 1 when there is at least one PE, FE or BI in the RX FIFO.
6	TEMT	**TX Holding Register (or TX FIFO) and the TX Shift Register are empty.** 0: Empty conditions below are not met. 1: If FIFOs are enabled, the bit is set whenever the TX FIFO and the TX Shift Register are empty. If FIFOs are disabled, the bit is set whenever TX Holding Register and TX Shift Register are empty.

Bit(s)	Name	Description
5	THRE	**Indicates if there is room for TX Holding Register or TX FIFO is reduced to its Trigger Level.** 0: Reset whenever the contents of the TX FIFO are more than its Trigger Level (FIFOs are enabled), or whenever TX Holding Register is not empty(FIFOs are disabled). 1: Set whenever the contents of the TX FIFO are reduced to its Trigger Level (FIFOs are enabled), or whenever TX Holding Register is empty and ready to accept new data (FIFOs are disabled).
4	BI	**Break Interrupt.** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit is set whenever the SIN is held in the 0 state for more than one transmission time (START bit + DATA bits + PARITY + STOP bits). If the FIFOs are enabled, this error is associated with a corresponding character in the FIFO and is flagged when this byte is at the top of the FIFO. When a break occurs, only one zero character is loaded into the FIFO: the next character transfer is enabled when SIN goes into the marking state and receives the next valid start bit.
3	FE	**Framing Error.** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit is set if the received data did not have a valid STOP bit. If the FIFOs are enabled, the state of this bit is revealed when the byte it refers to is the next to be read.
2	PE	**Parity Error** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit is set if the received data did not have a valid parity bit. If the FIFOs are enabled, the state of this bit is revealed when the referred byte is the next to be read.
1	OE	**Overrun Error.** 0: Reset by the CPU reading this register. 1: If the FIFOs are disabled, this bit is set if the RX Buffer was not read by the CPU before new data from the RX Shift Register overwrote the previous contents. If the FIFOs are enabled, an overrun error occurs when the RX FIFO is full and the RX Shift Register becomes full. OE is set as soon as this happens. The character in the Shift Register is then overwritten, but not transferred to the FIFO.
0	DR	**Data Ready.** 0: Cleared by the CPU reading the RX Buffer or by reading all the FIFO bytes. 1: Set by the RX Buffer becoming full or by the FIFO becoming no empty.

11002018 MSR Modem Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**CTS**				**DCTS**
Type												RU				RW

Reset												0				0

Bit(s)	Name	Description
4	CTS	**Clear To Send.** When Loop = "0", this value is the complement of the NCTS input signal. When Loop = "1", this value is equal to the RTS bit in the Modem Control Register.
0	DCTS	**Delta Clear To Send** 0: Cleared if the state of CTS has not changed since this register was last read. 1: Set if the state of CTS has changed since this register was last read.

1100201C SCR Scratch Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SCR**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SCR	**A general purpose read/write register. After reset, its value is un-defined.**

11002090 DLL Divisor Latch (LS) 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**DLL**							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:0	DLL	**divisor Latch low 8bit data.**

11002094 DLM Divisor Latch (MS) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLM							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DLM	**divisor Latch high 8bit data.** Note: Division by 1 generates a BAUD signal that is constantly high. Note: DLL & DLM setting formula is {DLH,DLL}=(system clock frequency/baud_pulse/baud_rate). When RATE_FIX(RATEFIX_AD[0])=0, system clock frequency = 52MHz. When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=0, system clock frequency = 26MHz. When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=1, system clock frequency = 13MHz. For baud_pulse value refer to HIGH_SPEED(offset=24H) register. e.g. When 52MHz,default speed mode and 115200 baud rate, the {DLH,DLL}=52MHz/16/115200=28.

11002098 EFR Enhanced Feature Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AUTO_CTS	AUTO_RTS		ENABLE_E	SW_FLOW_CONT			
Type									RW	RW		RW	RW			
Reset									0	0		0	0	0	0	0

Bit(s)	Name	Description
7	AUTO_CTS	**Enables hardware transmission flow control** 0: Disabled. 1: Enabled.
6	AUTO_RTS	**Enables hardware reception flow control** 0: Disabled. 1: Enabled.
4	ENABLE_E	**Enables enhancement feature** 0: Disabled. 1: Enabled.
3:0	SW_FLOW_CONT	**Software flow control bits.** 00xx: No TX Flow Control 10xx: Transmit XON1/XOFF1 as flow control bytes 01xx: Transmit XON2/XOFF2 as flow control bytes xx00: No RX Flow Control xx10: Receive XON1/XOFF1 as flow control bytes xx01: Receive XON2/XOFF2 as flow control bytes

110020A0 XON1 XON1 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON1	**XON1 character for software flow control.**

110020A4 XON2 XON2 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON2	**XON2 character for software flow control.**

110020A8 XOFF1 XOFF1 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF1	**XOFF1 character for software flow control.**

110020AC XOFF2 XOFF2 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF2	**XOFF2 character for software flow control.**

11002020 AUTOBAUD_EN Auto Baud Detect Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														sleep_ack_sel	AUTOBAUD_SEL	AUTOBAUD_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	sleep_ack_sel	0: can send sleep_ack when autobaud_en is enalbed and autobaud state machine and rx is in idle . 1: can not send sleep_ack when autobaud_en is enabled .
1	AUTOBAUD_SEL	**Auto-baud select** 0: support standard baud rate detection . 1: support non_standard baud rate detection(Just support baud from 300 to 115200, it is recommend to use 52MHZ to auto fix) .
0	AUTOBAUD_EN	**Auto-baud enable signal** 0: Auto-baud function disable 1: Auto-baud function enable (UARTn+0024h SPEED should be set 0) Note: when AUTOBAUD_EN is active, there should not A*/a* char before the auto baud char AT/at, if the A*/a* is Inevitable, the autobaud will fail and please disable the AUTOBAUD_EN to reset the autobaud feature and autobaud_en again.

11002024 HIGHSPEED High Speed Mode Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SPEED	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	SPEED	**UART sample counter base** 0: based on 16*baud_pulse, baud_rate = system clock frequency/16/{DLH, DLL} 1: based on 8*baud_pulse, baud_rate = system clock frequency/8/{DLH, DLL} 2: based on 4*baud_pulse, baud_rate = system clock frequency/4/{DLH, DLL} 3: based on sampe_count * baud_pulse, baud_rate = system clock frequency / (sampe_count+1) / {DLM, DLL}

11002028 SAMPLE_COUNT Sample Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLECOUNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SAMPLECOUNT	**Just be useful when HIGHSPEED mode = 3.**

1100202C SAMPLE_POINT Sample Point Register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLEPOINT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SAMPLEPOINT	**The SAMPLE_POINT is usually (SAMPLE_COUNT-1)/2 and remove the decimal.** sample point , is effective only When HIGHSPEED=3

11002030 AUTOBAUD_REG Auto Baud Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BAUD_STAT				BAUD_RATE			
Type									RU				RU			

Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:4	BAUD_STAT	**Autobaud format** 0: Autobaud is detecting 1: AT_7N1 2: AT_7O1 3: AT_7E1 4:AT_8N1 5: AT_8O1 6: AT_8E1 7: at_7N1 8: at_7E1 9: at_7O1 10: at_8N1 11: at_8E1 12: at_8O1 13: Autobaud detection fails
3:0	BAUD_RATE	**Autobaud baud rate** 0: 115200 1: 57600 2: 38400 3: 19200 4: 9600 5: 4800 6: 2400 7: 1200 8: 300 9: 110

11002034 RATEFIX_AD Clock Rate Fix Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**FREQ_SEL**	**AUTOBAUD_RATE_FIX**	**RATE_FIX**
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FREQ_SEL	**0: system clock = UART_CLK_SRC/2** 1: system clock = UART_CLK_SRC/4
1	AUTOBAUD_RATE_FIX	**0: system clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz)** 1: system clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depends on FREQ_SEL)

Bit(s)	Name	Description
0	RATE_FIX	**0: system clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz)** 1: system clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depends on FREQ_SEL)

11002038 AUTOBAUDSAMPLE Auto Baud Sample Register 0000000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											AUTOBAUDSAMPLE					
Type											RW					
Reset											0	0	1	1	0	1

Bit(s)	Name	Description
5:0	AUTOBAUDSAMPLE	**clk diveision for autobaud rate dectection.** for standard baud rate detection. system clk 52m :'d 27 system clk 26m :'d 13 system clk 13m :'d 6 for non-standard baud rate detection. :15.

1100203C GUARD Guard time added register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												GUARD_EN	GUARD_CNT			
Type												RW	RW			
Reset												0	1	1	1	1

Bit(s)	Name	Description
4	GUARD_EN	**Guard interval add enable signal.** 0: No guard interval added. 1: Add guard interval after stop bit.
3:0	GUARD_CNT	**Guard interval count value. Guard interval = (1/(system clock / div_step / div)) * GUARD_CNT.**

11002040 ESCAPE_DAT Escape character register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ESCAPE_DAT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	ESCAPE_DAT	**Escape character added before software flow control data and escape character, i.e. if tx data is xon (31h), with esc_en =1, uart transmits data as esc + CEh (~xon).**

11002044 ESCAPE_EN Escape enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ESC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	ESC_EN	**Add escape character in transmitter and remove escape character in receiver by UART.** 0: Do not deal with the escape character. 1: Add escape character in transmitter and remove escape character in receiver.

11002048 SLEEP_EN Sleep enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_EN	**For sleep mode issue** 0: Do not deal with sleep mode indicate signal 1: To activate hardware flow control or software control according to software initial setting when chip enters sleep mode. Releasing hardware flow when chip wakes up; but for software control, uart sends xon when awaken and when FIFO does not reach threshold level.

1100204C DMA_EN DMA enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FIFO_lsr_sel	TO_CNT_AUTORST	TX_DMA_EN	RX_DMA_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	FIFO_lsr_sel	**fifo lsr mode selection** 0: lsr will update automatically with read data from rx fifo.. 1: lsr will hold the first line status error state until you read the lsr register.
2	TO_CNT_AUTORST	**Timeout counter auto reset register** 0: After RX timeout happen, SW shall reset the interrupt by reading UART 0x4C. 1: The timeout counter will be auto reset. Set this register when Rain's new DMA is used.
1	TX_DMA_EN	**TX_DMA mechanism enable signal** 0: Do not use DMA in TX. 1: Use DMA in TX. When this reguster is enabled, the flow control is based on the DMA threshold, and generates a timeout interrupt for DMA.for DMA.
0	RX_DMA_EN	**RX_DMA mechanism enable signal** 0: Do not use DMA in RX 1: Use DMA in RX. When this reguster is enabled, the flow control is based on the DMA threshold, and generates a timeout interrupt

11002050 RXTRI_AD Rx Trigger Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RXTRIG			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RXTRIG	**When {rtm,rtl}=2'b11, The Rx FIFO threshold will be Rxtrig.** The value is suggested to be less than half of RX FIFO size, which is 32 Bytes.

11002054 FRACDIV_L Fractional Divider LSB Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FRACDIV_L							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FRACDIV_L	**Add sampling count (+1) from state data7 to data0, in order to contribute fractional divisor.only when high_speed==3.**

11002058 FRACDIV_M Fractional Divider MSB Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FRACDIV_M	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	FRACDIV_M	**Add sampling count when in state stop to parity, in order to contribute fractional divisor.only when high_speed==3.**

1100205C FCR_RD FIFO Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RFTL1_RFTL0		TFTL1_TFTL0			CLRT	CLRR	FIFOE
Type									RO		RO			RO	RO	RO
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:6	RFTL1_RFTL0	**RX FIFO trigger threshold. (RX FIFO contains total 32 bytes.)** 0: 1 1: 6 2: 12

Bit(s)	Name	Description
		3: RXTRIG
5:4	TFTL1_TFTL0	**TX FIFO trigger threshold (TX FIFO contains total 32 bytes.)** 0: 1 1: 4 2: 8 3: 14
2	CLRT	0: TX FIFO is not cleared 1: TX FIFO is cleared
1	CLRR	0: RX FIFO is not cleared 1: RX FIFOis cleared
0	FIFOE	**FIFO Enabled. This bit must be set to 1 for any of the other bits in the registers to have any effect.** 0: the RX and TX FIFOs are not enabled.. 1: RX and TX FIFOs are enabled.

1100209C FEATURE_SEL UART Feature Select Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**FEATURE_SEL**
Type																RW
Reset																0

Bit(s)	Name	Description
0	FEATURE_SEL	**For ap mcu side UART ,if use new UART register map feature_sel should keep 1.** 0: Disable new register map. 1: Enable new register map.

110020B0 USB_RX_SEL UART USB rx pin Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**USB_RX_SEL**
Type																RW
Reset																0

Bit(s)	Name	Description
0	USB_RX_SEL	0: uart rx pin is selected. 1: usb rx pin is selected.

Bit(s)	Name	Description

110020B4 SLEEP_REQ uart sleep request register. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_REQ
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_REQ	0: cancel sleep request to uart.(after wake up sent by cpu) 1: send sleep request to uart.(before sleep sent by cpu)

110020B8 SLEEP_ACK uart idle register. 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_ACK
Type																RU
Reset																1

Bit(s)	Name	Description
0	SLEEP_ACK	0: uart is not in idle state.(cpu can polling this register to get the uart state) 1: uart is in idle state.(cpu can polling this register to get the uart state)

110020BC SPM_SEL SPM interface selection register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SPM_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	SPM_SEL	0: SPM sleep interface will not be used. 1: SPM sleep interface will be used.

1.14 UART 3

1.14.1 Introduction

The UART provide full duplex serial communication channels between chip and external devices. The UART has M16C450 and M16550A modes of operation, which are compatible with a range of standard software drivers. The extensions have been designed to be broadly software compatible with 16550A variants, but certain areas offer no consensus.

In common with the M16550A, the UART supports word lengths from 5 to 8 bits, an optional parity bit and one or two stop bits, and is fully programmable by a CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided. The UART also includes two DMA handshake lines, used to indicate when the FIFOs are ready to transfer data to the CPU. Interrupts can be generated from any of the several sources.

After hardware reset, the UART is in M16C450 mode. Its FIFOs can be enabled and the UART can then enter M16550A mode. The UART adds further functionality beyond M16550A mode. Each of the extended functions can be selected individually under software control.

1.14.2 Features

- UART0 is 2 pin (tx, rx) UART channel
- Support both M16C450 and M16550A modes of operation
  - Compatible with standard software drivers
- Transfer system Asynchronuos
- Data length 5 to 8 bits
- Software flow control Use special character Xon/Xoff to do software flow control
- Baud rate Baud rate is programmable form 300bps to 3Mbps.
- Interrupt request Received interrupt/Transmit interrupt
- Data transfer DMA (Transmit/Received) transfer supported.

1.14.3 Register Definition

Module name: uart3 Base address: (+11005000h)

Address	Name	Width	Register Function
11002000	RBR_THR	8	RX Buffer Register / TX Holding Register
11002004	IER	8	Interrupt Enable Register By storing a '1' to a specific bit position, the interrupt associated with that bit is enabled. Otherwise, the interrupt is disabled. IER[7:4] are modified when EFR[4] = 1.
11002008	IIR_FCR	8	Interrupt Identification Register / FIFO Control Register priority is from high to low as following .IIR[5:0]==0X1: no interrupt pending .IIR[5:0]==0X6:line status interrup(Under IER[2]=1). IIR[5:0]==0Xc:rx data timeout interrup(Under IER[0]=1). IIR[5:0]==0X4:RX Data is placed in the RX

Address	Name	Width	Register Function
			Buffer Register or the RX Trigger Level is reached.(Under IER[0]=1) . IIR[5:0]==0X2: TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level(Under IER[1]=1). IIR[5:0]==0X0: modem status change interrupt(Under IER[3]=1). IIR[5:0]==0X10: XOFF character recieved (Under IER[5]=1,EFR[4] = 1). IIR[5:0]==0X20: CTS or RTS Rising edge (Under IER[7]=1,IER[6]=1,EFR[4] = 1).
1100200C	LCR	8	Line Control Register Line Control Register. Determines characteristics of serial communication signals.
11002010	MCR	8	Modem Control Register Modem Control Register. Control interface signals of the UART. MCR[7] can be read when EFR[4] = 1.
11002014	LSR	8	Line Status Register Line Status Register.
11002018	MSR	8	Modem Status Register Note: After a reset, D4-D7 are inputs. A modem status interrupt can be cleared by writing '0' to D0-D3or reading this register. And can be set by writing '1' to D0-D3 or input has changed. D0-D3 can be Modified when != BFh.
1100201C	SCR	8	Scratch Register A general purpose read/write register. After reset, its value is un-defined.
11002090	DLL	8	Divisor Latch (LS) uesd to divid the bclk frequency .
11002094	DLM	8	Divisor Latch (MS) uesd to divid the bclk frequency .
11002098	EFR	8	Enhanced Feature Register
110020A0	XON1	8	XON1 Char Register
110020A4	XON2	8	XON2 Char Register
110020A8	XOFF1	8	XOFF1 Char Register
110020AC	XOFF2	8	XOFF2 Char Register
11002020	AUTOBAUD_EN	8	Auto Baud Detect Enable Register
11002024	HIGHSPEED	8	High Speed Mode Register
11002028	SAMPLE_COUNT	8	Sample Counter Register When HIGHSPEED=3, the sample_count is the threshold value for UART sample counter (sample_num). Count from 0 to sample_count.
1100202C	SAMPLE_POINT	8	Sample Point Register When HIGHSPEED=3, UART gets the input data when sample_count=sample_num. e.g. system clock = 13MHz, 921600 = 13000000 / 14 sample_count = 13 and sample point = 6 (sample the central point to decrease the inaccuracy) The SAMPLE_POINT is usually (SAMPLE_COUNT-1)/2 and remove the decimal.
11002030	AUTOBAUD_REG	8	Auto Baud Monitor Register the autobaud detection state ,it will not change until enable the autobaud_en again.

Address	Name	Width	Register Function
11002034	RATEFIX_AD	8	Clock Rate Fix Register
11002038	AUTOBAUDSAMPLE	8	Auto Baud Sample Register Since the system clock may change, autobaud sample duration should change as system clock changes. When system clock = 13MHz, autobaudsample = 6; when system clock = 26MHz, autobaudsample = 13; When system clock = 52MHz, autobaudsample = 27.
1100203C	GUARD	8	Guard time added register
11002040	ESCAPE_DAT	8	Escape character register
11002044	ESCAPE_EN	8	Escape enable register
11002048	SLEEP_EN	8	Sleep enable register
1100204C	DMA_EN	8	DMA enable register
11002050	RXTRI_AD	8	Rx Trigger Address
11002054	FRACDIV_L	8	Fractional Divider LSB Address
11002058	FRACDIV_M	8	Fractional Divider MSB Address
1100205C	FCR_RD	8	FIFO Control Register
1100209C	FEATURE_SEL	8	UART Feature Select Register For ap mcu side UART ,if use new UART register map feature_sel should keep 1.
110020B0	USB_RX_SEL	8	UART USB rx pin Selection Register
110020B4	SLEEP_REQ	8	uart sleep request register.
110020B8	SLEEP_ACK	8	uart idle register.
110020BC	SPM_SEL	8	SPM interface selection register

11002000 RBR_THR RX Buffer Register / TX Holding Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RBR_THR**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RBR_THR	**For read : The received data can be read by accessing this register.** For write : The data to be transmitted is written to this register, and then sent to the PC via serial communication.

11002004 IER Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CTSI	RTSI	XOFFI		EDSSI	ELSI	ETBEI	ERBFI
Type									RW	RW	RW		RW	RW	RW	RW
Reset									0	0	0		0	0	0	0

Bit(s)	Name	Description
7	CTSI	**Masks an interrupt that is generated when a rising edge is detected on the CTS modem control line.** Note: This interrupt is only enabled when hardware flow control is enabled. 0: Mask an interrupt that is generated when a rising edge is detected on the CTS modem control line. 1: Unmask an interrupt that is generated when a rising edge is detected on the CTS modem control line.
6	RTSI	**Masks an interrupt that is generated when a rising edge is detected on the RTS modem control line.** Note: This interrupt is only enabled when hardware flow control is enabled. 0: Mask an interrupt that is generated when a rising edge is detected on the RTS modem control line. 1: Unmask an interrupt that is generated when a rising edge is detected on the RTS modem control line.
5	XOFFI	**Masks an interrupt that is generated when an XOFF character is received.** Note: This interrupt is only enabled when software flow control is enabled. 0: Mask an interrupt that is generated when an XOFF character is received. 1: Unmask an interrupt that is generated when an XOFF character is received.
3	EDSSI	**When set ("1"), an interrupt is generated if DCTS (MSR[0]) becomes set.** 0: No interrupt is generated if DCTS (MSR[0]) becomes set. 1: An interrupt is generated if DCTS (MSR[0]) becomes set.
2	ELSI	**When set ("1"), an interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.** 0: No interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set. 1: An interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.
1	ETBEI	**When set ("1"), an interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level.** 0: No interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level. 1: An interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level
0	ERBFI	**When set ("1"), an interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached.** 0: No interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. 1: An interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached.

11002008 IIR_FCR Interrupt Identification Register / FIFO Control Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOE_or_RFTL1_RFTL0		ID_or_FIFO_ctrl					
Type									RW		RW					
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:6	FIFOE_or_RFTL1_RFTL0	**RX FIFO trigger threshold. (RX FIFO contains total 32 bytes.)** 0: 1 1: 6 2: 12 3: RXTRIG
5:0	ID_or_FIFO_ctrl	**IIR_FCR[5:0] for read** Priority Level Interrupt Source 000001 - No interrupt pending 000110 1 Line Status Interrupt: BI, FE, PE or OE set in LSR. (Under IER[2]=1) 001100 2 RX Data Timeout: Timeout on character in RX FIFO. (Under IER[0]=1) 000100 3 RX Data Received: RX Data received or RX Trigger Level reached. (Under IER[0]=1) 000010 4 TX Holding Register Empty: TX Holding Register empty or TX FIFO Trigger Level reached. (Under IER[1]=1) 000000 5 Modem Status change: DDCD, TERI, DDSR or DCTS set in MSR. (Under IER[3]=1) 010000 6 Software Flow Control: XOFF Character received. (Under IER[5]=1) 100000 7 Hardware Flow Control: CTS or RTS Rising Edge. (Under IER[7]=1 or IER[6]=1) Line Status Interrupt: A RX Line Status Interrupt (IIR[5:0] == 000110b) is generated if ELSI (IER[2]) is set and any of BI, FE, PE or OE (LSR[4:1]) becomes set. The interrupt is cleared by reading the Line Status Register. RX Data Timeout Interrupt:When virtual FIFO mode is disabled, RX Data Timeout Interrupt is generated if all of the following apply: 1. FIFO contains at least one character; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register, or on a CPU read from the RX FIFO. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading RX FIFO.

Bit(s)	Name	Description
		When virtual FIFO mode is enabled, RX Data Timeout Interrupt is generated if all of the following apply: 1. FIFO is empty; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register or reading DMA_EN register. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading DMA_EN register. RX Data Received Interrupt: A RX Received interrupt (IER[5:0] == 000100b) is generated if EFRBI (IER[0]) is set and either RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. The interrupt is cleared by reading the RX Buffer Register or the RX FIFO (if enabled). TX Holding Register Empty Interrupt: A TX Holding Register Empty Interrupt (IIR[5:0] = 000010b) is generated if ETRBI (IER[1]) is set and either the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level. The interrupt is cleared by writing to the TX Holding Register or TX FIFO if FIFO enabled. Modem Status Change Interrupt: A Modem Status Change Interrupt (IIR[5:0] = 000000b) is generated if EDSSI (IER[3]) is set and either DDCD, TERI, DDSR or DCTS (MSR[3:0]) becomes set. The interrupt is cleared by reading the Modem Status Register. Software Flow Control Interrupt: A Software Flow Control Interrupt (IIR[5:0] = 010000b) is generated if Software Flow Control is enabled and XOFFI (IER[5]) becomes set, indicating that an XOFF character has been received. The interrupt is cleared by reading the Interrupt Identification Register. Hardware Flow Control Interrupt: A Hardware Flow Control Interrupt (IER[5:0] = 100000b) is generated if Hardware Flow Control is enabled and either RTSI (IER[6]) or CTSI (IER[7]) becomes set indicating that a rising edge has been detected on either the RTS/CTS Modem Control line. The interrupt is cleared by reading the Interrupt Identification Register. ---------- IIR_FCR [5:0] for write IIR_FCR [5:4] TX FIFO trigger threshold (TX FIFO contains total 32 bytes.) 0: 1 1: 6 2: 12 3: RXTRIG IIR_FCR [2] control bit to clear tx fifo

Bit(s)	Name	Description
		0: no effect 1: clear RX FIFO IIR_FCR [1] control bit to clear rx fifo 0: no effect 1: clear RX FIFO IIR_FCR [0] FIFO Enabled. This bit must be set to 1 for any of the other bits in the registers to have any effect. 0: Disable both the RX and TX FIFOs. 1: Enable both the RX and TX FIFOs.

1100200C LCR Line Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLAB	SB	SP	EPS	PEN	STB	WLS1_WLS0	
Type									RW	RW	RW	RW	RW	RW	RW	
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	DLAB	**Divisor Latch Access Bit.** 0: The RX and TX Registers are read/written at Address 0 and the IER register is read/written at Address 4. 1: The Divisor Latch LS is read/written at Address 0 and the Divisor Latch MS is read/written at Address 4.
6	SB	**Set Break** 0: No effect 1: SOUT signal is forced into the "0" state.
5	SP	**Stick Parity** 0: No effect. 1: The Parity bit is forced into a defined state, depending on the states of EPS and PEN: If EPS=1 & PEN=1, the Parity bit is set and checked = 0. If EPS=0 & PEN=1, the Parity bit is set and checked = 1.
4	EPS	**Even Parity Select** 0: When EPS=0, an odd number of ones is sent and checked. 1: When EPS=1, an even number of ones is sent and checked.
3	PEN	**Parity Enable** 0: The Parity is neither transmitted nor checked. 1: The Parity is transmitted and checked.
2	STB	**Number of STOP bits** 0: One STOP bit is always added. 1: Two STOP bits are added after each character is sent; unless the character length is 5 when 1 STOP bit is added.
1:0	WLS1_WLS0	**Word Length Select.** 0: 5 bits 1: 6 bits

Bit(s)	Name	Description
		2: 7 bits 3: 8 bits

11002010 MCR Modem Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF_STATUS			Loop			RTS	
Type									RU			RW			RW	
Reset									0			0			0	

Bit(s)	Name	Description
7	XOFF_STATUS	**This is a read-only bit.** 0: When an XON character is received. 1: When an XOFF character is received.
4	Loop	**Loop-back control bit.** 0: No loop-back is enabled. 1: Loop-back mode is enabled.
1	RTS	**Controls the state of the output NRTS, even in loop mode.** 0: RTS will always output 1. 1: RTS's output will be controled by flow control condition.

11002014 LSR Line Status Register 00000060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOERR	TEMT	THRE	BI	FE	PE	OE	DR
Type									RU	RU	RU	RU	RU	RU	RU	RU
Reset									0	1	1	0	0	0	0	0

Bit(s)	Name	Description
7	FIFOERR	**RX FIFO Error Indicator.** 0: No PE, FE, BI set in the RX FIFO. 1: Set to 1 when there is at least one PE, FE or BI in the RX FIFO.
6	TEMT	**TX Holding Register (or TX FIFO) and the TX Shift Register are empty.** 0: Empty conditions below are not met. 1: If FIFOs are enabled, the bit is set whenever the TX FIFO and the TX Shift Register are empty. If FIFOs are disabled, the bit is set whenever TX Holding Register and TX Shift Register are empty.

Bit(s)	Name	Description
5	THRE	**Indicates if there is room for TX Holding Register or TX FIFO is reduced to its Trigger Level.** 0: Reset whenever the contents of the TX FIFO are more than its Trigger Level (FIFOs are enabled), or whenever TX Holding Register is not empty(FIFOs are disabled). 1: Set whenever the contents of the TX FIFO are reduced to its Trigger Level (FIFOs are enabled), or whenever TX Holding Register is empty and ready to accept new data (FIFOs are disabled).
4	BI	**Break Interrupt.** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit is set whenever the SIN is held in the 0 state for more than one transmission time (START bit + DATA bits + PARITY + STOP bits). If the FIFOs are enabled, this error is associated with a corresponding character in the FIFO and is flagged when this byte is at the top of the FIFO. When a break occurs, only one zero character is loaded into the FIFO: the next character transfer is enabled when SIN goes into the marking state and receives the next valid start bit.
3	FE	**Framing Error.** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit is set if the received data did not have a valid STOP bit. If the FIFOs are enabled, the state of this bit is revealed when the byte it refers to is the next to be read.
2	PE	**Parity Error** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit is set if the received data did not have a valid parity bit. If the FIFOs are enabled, the state of this bit is revealed when the referred byte is the next to be read.
1	OE	**Overrun Error.** 0: Reset by the CPU reading this register. 1: If the FIFOs are disabled, this bit is set if the RX Buffer was not read by the CPU before new data from the RX Shift Register overwrote the previous contents. If the FIFOs are enabled, an overrun error occurs when the RX FIFO is full and the RX Shift Register becomes full. OE is set as soon as this happens. The character in the Shift Register is then overwritten, but not transferred to the FIFO.
0	DR	**Data Ready.** 0: Cleared by the CPU reading the RX Buffer or by reading all the FIFO bytes. 1: Set by the RX Buffer becoming full or by the FIFO becoming no empty.

11002018 MSR Modem Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**CTS**				**DCTS**
Type												RU				RW

Reset												0				0

Bit(s)	Name	Description
4	CTS	**Clear To Send.** When Loop = "0", this value is the complement of the NCTS input signal. When Loop = "1", this value is equal to the RTS bit in the Modem Control Register.
0	DCTS	**Delta Clear To Send** 0: Cleared if the state of CTS has not changed since this register was last read. 1: Set if the state of CTS has changed since this register was last read.

1100201C SCR Scratch Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SCR**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SCR	**A general purpose read/write register. After reset, its value is un-defined.**

11002090 DLL Divisor Latch (LS) 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**DLL**							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:0	DLL	**divisor Latch low 8bit data.**

11002094 DLM Divisor Latch (MS) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLM							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DLM	**divisor Latch high 8bit data.** Note: Division by 1 generates a BAUD signal that is constantly high. Note: DLL & DLM setting formula is {DLH,DLL}=(system clock frequency/baud_pulse/baud_rate). When RATE_FIX(RATEFIX_AD[0])=0, system clock frequency = 52MHz. When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=0, system clock frequency = 26MHz. When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=1, system clock frequency = 13MHz. For baud_pulse value refer to HIGH_SPEED(offset=24H) register. e.g. When 52MHz,default speed mode and 115200 baud rate, the {DLH,DLL}=52MHz/16/115200=28.

11002098 EFR Enhanced Feature Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AUTO_CTS	AUTO_RTS		ENABLE_E	SW_FLOW_CONT			
Type									RW	RW		RW	RW			
Reset									0	0		0	0	0	0	0

Bit(s)	Name	Description
7	AUTO_CTS	**Enables hardware transmission flow control** 0: Disabled. 1: Enabled.
6	AUTO_RTS	**Enables hardware reception flow control** 0: Disabled. 1: Enabled.
4	ENABLE_E	**Enables enhancement feature** 0: Disabled. 1: Enabled.
3:0	SW_FLOW_CONT	**Software flow control bits.** 00xx: No TX Flow Control 10xx: Transmit XON1/XOFF1 as flow control bytes 01xx: Transmit XON2/XOFF2 as flow control bytes xx00: No RX Flow Control xx10: Receive XON1/XOFF1 as flow control bytes xx01: Receive XON2/XOFF2 as flow control bytes

110020A0 XON1 XON1 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON1	**XON1 character for software flow control.**

110020A4 XON2 XON2 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON2	**XON2 character for software flow control.**

110020A8 XOFF1 XOFF1 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF1	**XOFF1 character for software flow control.**

110020AC XOFF2 XOFF2 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF2	**XOFF2 character for software flow control.**

11002020 AUTOBAUD_EN Auto Baud Detect Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														sleep_ack_sel	AUTOBAUD_SEL	AUTOBAUD_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	sleep_ack_sel	0: can send sleep_ack when autobaud_en is enalbed and autobaud state machine and rx is in idle . 1: can not send sleep_ack when autobaud_en is enabled .
1	AUTOBAUD_SEL	**Auto-baud select** 0: support standard baud rate detection . 1: support non_standard baud rate detection(Just support baud from 300 to 115200, it is recommend to use 52MHZ to auto fix) .
0	AUTOBAUD_EN	**Auto-baud enable signal** 0: Auto-baud function disable 1: Auto-baud function enable (UARTn+0024h SPEED should be set 0) Note: when AUTOBAUD_EN is active, there should not A*/a* char before the auto baud char AT/at, if the A*/a* is Inevitable, the autobaud will fail and please disable the AUTOBAUD_EN to reset the autobaud feature and autobaud_en again.

11002024 HIGHSPEED High Speed Mode Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SPEED	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	SPEED	**UART sample counter base** 0: based on 16*baud_pulse, baud_rate = system clock frequency/16/{DLH, DLL} 1: based on 8*baud_pulse, baud_rate = system clock frequency/8/{DLH, DLL} 2: based on 4*baud_pulse, baud_rate = system clock frequency/4/{DLH, DLL} 3: based on sampe_count * baud_pulse, baud_rate = system clock frequency / (sampe_count+1) / {DLM, DLL}

11002028 SAMPLE_COUNT Sample Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLECOUNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SAMPLECOUNT	**Just be useful when HIGHSPEED mode = 3.**

1100202C SAMPLE_POINT Sample Point Register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLEPOINT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SAMPLEPOINT	**The SAMPLE_POINT is usually (SAMPLE_COUNT-1)/2 and remove the decimal.** sample point , is effective only When HIGHSPEED=3

11002030 AUTOBAUD_REG Auto Baud Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BAUD_STAT				BAUD_RATE			
Type									RU				RU			

Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:4	BAUD_STAT	**Autobaud format** 0: Autobaud is detecting 1: AT_7N1 2: AT_7O1 3: AT_7E1 4:AT_8N1 5: AT_8O1 6: AT_8E1 7: at_7N1 8: at_7E1 9: at_7O1 10: at_8N1 11: at_8E1 12: at_8O1 13: Autobaud detection fails
3:0	BAUD_RATE	**Autobaud baud rate** 0: 115200 1: 57600 2: 38400 3: 19200 4: 9600 5: 4800 6: 2400 7: 1200 8: 300 9: 110

11002034 RATEFIX_AD Clock Rate Fix Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**FREQ_SEL**	**AUTOBAUD_RATE_FIX**	**RATE_FIX**
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FREQ_SEL	**0: system clock = UART_CLK_SRC/2** 1: system clock = UART_CLK_SRC/4
1	AUTOBAUD_RATE_FIX	**0: system clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz)** 1: system clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depends on FREQ_SEL)

Bit(s)	Name	Description
0	RATE_FIX	**0: system clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz)** 1: system clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depends on FREQ_SEL)

11002038 AUTOBAUDSAMPLE Auto Baud Sample Register 0000000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											AUTOBAUDSAMPLE					
Type											RW					
Reset											0	0	1	1	0	1

Bit(s)	Name	Description
5:0	AUTOBAUDSAMPLE	**clk diveision for autobaud rate dectection.** for standard baud rate detection. system clk 52m :'d 27 system clk 26m :'d 13 system clk 13m :'d 6 for non-standard baud rate detection. :15.

1100203C GUARD Guard time added register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												GUARD_EN	GUARD_CNT			
Type												RW	RW			
Reset												0	1	1	1	1

Bit(s)	Name	Description
4	GUARD_EN	**Guard interval add enable signal.** 0: No guard interval added. 1: Add guard interval after stop bit.
3:0	GUARD_CNT	**Guard interval count value. Guard interval = (1/(system clock / div_step / div)) * GUARD_CNT.**

11002040 ESCAPE_DAT Escape character register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ESCAPE_DAT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	ESCAPE_DAT	**Escape character added before software flow control data and escape character, i.e. if tx data is xon (31h), with esc_en =1, uart transmits data as esc + CEh (~xon).**

11002044 ESCAPE_EN Escape enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ESC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	ESC_EN	**Add escape character in transmitter and remove escape character in receiver by UART.** 0: Do not deal with the escape character. 1: Add escape character in transmitter and remove escape character in receiver.

11002048 SLEEP_EN Sleep enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_EN	**For sleep mode issue** 0: Do not deal with sleep mode indicate signal 1: To activate hardware flow control or software control according to software initial setting when chip enters sleep mode. Releasing hardware flow when chip wakes up; but for software control, uart sends xon when awaken and when FIFO does not reach threshold level.

1100204C DMA_EN DMA enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FIFO_lsr_sel	TO_CNT_AUTORST	TX_DMA_EN	RX_DMA_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	FIFO_lsr_sel	**fifo lsr mode selection** 0: lsr will update automatically with read data from rx fifo.. 1: lsr will hold the first line status error state until you read the lsr register.
2	TO_CNT_AUTORST	**Timeout counter auto reset register** 0: After RX timeout happen, SW shall reset the interrupt by reading UART 0x4C. 1: The timeout counter will be auto reset. Set this register when Rain's new DMA is used.
1	TX_DMA_EN	**TX_DMA mechanism enable signal** 0: Do not use DMA in TX. 1: Use DMA in TX. When this reguster is enabled, the flow control is based on the DMA threshold, and generates a timeout interrupt for DMA.for DMA.
0	RX_DMA_EN	**RX_DMA mechanism enable signal** 0: Do not use DMA in RX 1: Use DMA in RX. When this reguster is enabled, the flow control is based on the DMA threshold, and generates a timeout interrupt

11002050 RXTRI_AD Rx Trigger Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RXTRIG			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RXTRIG	**When {rtm,rtl}=2'b11, The Rx FIFO threshold will be Rxtrig.** The value is suggested to be less than half of RX FIFO size, which is 32 Bytes.

11002054 FRACDIV_L Fractional Divider LSB Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FRACDIV_L							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FRACDIV_L	**Add sampling count (+1) from state data7 to data0, in order to contribute fractional divisor.only when high_speed==3.**

11002058 FRACDIV_M Fractional Divider MSB Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FRACDIV_M	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	FRACDIV_M	**Add sampling count when in state stop to parity, in order to contribute fractional divisor.only when high_speed==3.**

1100205C FCR_RD FIFO Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RFTL1_RFTL0		TFTL1_TFTL0			CLRT	CLRR	FIFOE
Type									RO		RO			RO	RO	RO
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:6	RFTL1_RFTL0	**RX FIFO trigger threshold. (RX FIFO contains total 32 bytes.)** 0: 1 1: 6 2: 12

Bit(s)	Name	Description
		3: RXTRIG
5:4	TFTL1_TFTL0	**TX FIFO trigger threshold (TX FIFO contains total 32 bytes.)** 0: 1 1: 4 2: 8 3: 14
2	CLRT	0: TX FIFO is not cleared 1: TX FIFO is cleared
1	CLRR	0: RX FIFO is not cleared 1: RX FIFOis cleared
0	FIFOE	**FIFO Enabled. This bit must be set to 1 for any of the other bits in the registers to have any effect.** 0: the RX and TX FIFOs are not enabled.. 1: RX and TX FIFOs are enabled.

1100209C FEATURE_SEL UART Feature Select Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**FEATURE_SEL**
Type																RW
Reset																0

Bit(s)	Name	Description
0	FEATURE_SEL	**For ap mcu side UART ,if use new UART register map feature_sel should keep 1.** 0: Disable new register map. 1: Enable new register map.

110020B0 USB_RX_SEL UART USB rx pin Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**USB_RX_SEL**
Type																RW
Reset																0

Bit(s)	Name	Description
0	USB_RX_SEL	0: uart rx pin is selected. 1: usb rx pin is selected.

Bit(s)	Name	Description

110020B4 SLEEP_REQ uart sleep request register. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_REQ
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_REQ	0: cancel sleep request to uart.(after wake up sent by cpu) 1: send sleep request to uart.(before sleep sent by cpu)

110020B8 SLEEP_ACK uart idle register. 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_ACK
Type																RU
Reset																1

Bit(s)	Name	Description
0	SLEEP_ACK	0: uart is not in idle state.(cpu can polling this register to get the uart state) 1: uart is in idle state.(cpu can polling this register to get the uart state)

110020BC SPM_SEL SPM interface selection register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SPM_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	SPM_SEL	0: SPM sleep interface will not be used. 1: SPM sleep interface will be used.

1.15 Pulse-Width Modulation

1.15.1 Introduction

Seven generic pulse-width modulators are implemented to generate pulse sequences with programmable frequency and duration for LCD backlight, charging or other purposes. Before enabling PWM, the pulse sequences must be prepared in the memory or registers. Then PWM will read the pulse sequences to generate random waveform to meet all kinds of applications.

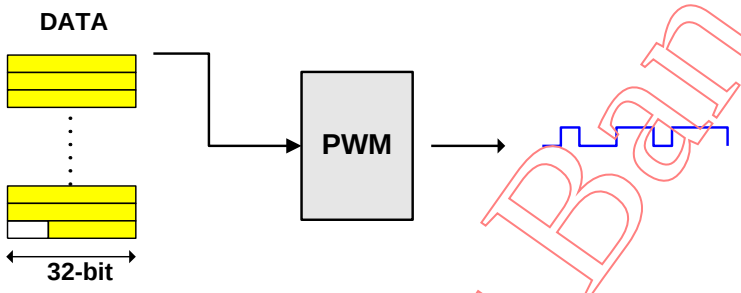
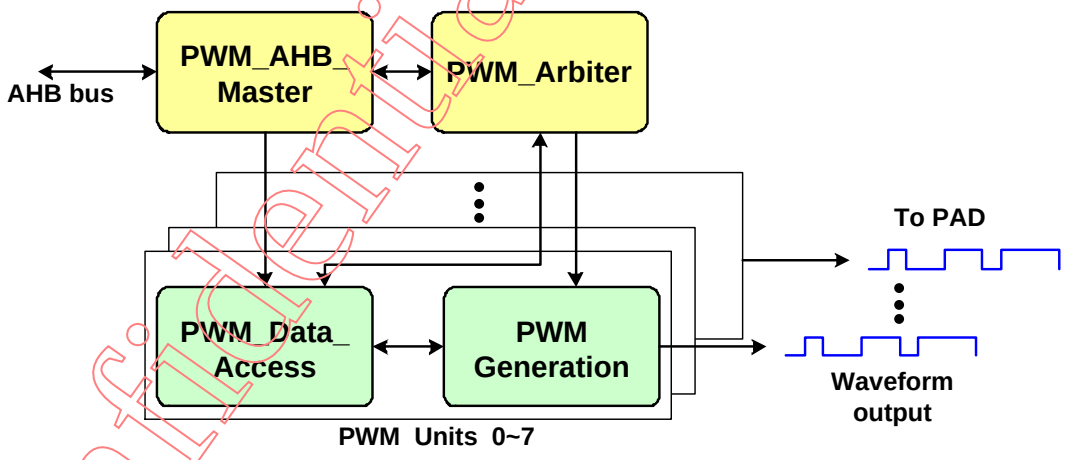


Figure 1-9. Generation procedure of PWM

1.15.2 Features

- Old mode, FIFO mode
- Periodical memory and random mode
- Sequential output mode and 3DLCM mode

1.15.3 Block Diagram



1.15.4 Register Definition

Module name: PWM Base address: (+11006000h)

Address	Name	Width	Register Function
11006000	PWM_ENABLE	32	PWM Enable Register

Address	Name	Width	Register Function
11006004	PWM3_DELAY	32	PWM3 Delay Duration Register
11006008	PWM4_DELAY	32	PWM4 Delay Duration Register
11006010	PWM0_CON	32	PWM0 Control Register
11006014	PWM0_HDURATION	32	PWM0 High Duration Register
11006018	PWM0_LDURATION	32	PWM0 Low Duration Register
1100601C	PWM0_GDURATION	32	PWM0 Guard Duration Register
11006020	PWM0_BUF0_BASE_ADDR	32	
11006024	PWM0_BUF0_SIZE	32	PWM0 Buffer0 Size Register
11006028	PWM0_BUF1_BASE_ADDR	32	PWM0 Buffer1 Base Address register
1100602C	PWM0_BUF1_SIZE	32	PWM0 Buffer1 Size Register
11006030	PWM0_SEND_DATA0	32	PWM0 Send Data0 Register
11006034	PWM0_SEND_DATA1	32	PWM0 Send Data1 Register
11006038	PWM0_WAVE_NUM	32	PWM0 Wave Number Register
1100603C	PWM0_DATA_WIDTH	32	PWM0 Data Width Register
11006040	PWM0_THRESH	32	PWM0 Thresh Register
11006044	PWM0_SEND_WAVE_NUM	32	PWM0 Send Wave Number register
11006048	PWM0_VALID	32	PWM0 Valid Register
11006050	PWM1_CON	32	PWM1 Control Register
11006054	PWM1_HDURATION	32	PWM1 High Duration Register
11006058	PWM1_LDURATION	32	PWM1 Low Duration Register
1100605C	PWM1_GDURATION	32	PWM1 Guard Duration Register
11006060	PWM1_BUF0_BASE_ADDR	32	PWM1 Buffer0 Base Address register
11006064	PWM1_BUF0_SIZE	32	PWM1 Buffer0 Size Register
11006068	PWM1_BUF1_BASE_ADDR	32	PWM1 Buffer1 Base Address register
1100606C	PWM1_BUF1_SIZE	32	PWM1 Buffer1 Size Register
11006070	PWM1_SEND_DATA0	32	PWM1 Send Data0 Register
11006074	PWM1_SEND_DATA1	32	PWM1 Send Data1 Register
11006078	PWM1_WAVE_NUM	32	PWM1 Wave Number Register
1100607C	PWM1_DATA_WIDTH	32	PWM1 Data Width Register
11006080	PWM1_THRESH	32	PWM1 Thresh Register
11006084	PWM1_SEND_WAVENUM	32	PWM1 Send Wave Number register
11006088	PWM1_VALID	32	PWM1 Valid Register
11006090	PWM2_CON	32	PWM2 Control Register
11006094	PWM2_HDURATION	32	PWM2 High Duration Register
11006098	PWM2_LDURATION	32	PWM2 Low Duration Register
1100609C	PWM2_GDURATION	32	PWM2 Guard Duration Register
110060A0	PWM2_BUF0_BASE_ADDR	32	PWM2 Buffer0 Base Address register
110060A4	PWM2_BUF0_SIZE	32	PWM2 Buffer0 Size Register
110060A8	PWM2_BUF1_BASE_ADDR	32	PWM2 Buffer1 Base Address register

Address	Name	Width	Register Function
110060AC	PWM2_BUF1_SIZE	32	PWM2 Buffer1 Size Register
110060B0	PWM2_SEND_DATA0	32	PWM2 Send Data0 Register
110060B4	PWM2_SEND_DATA1	32	PWM2 Send Data1 Register
110060B8	PWM2_WAVE_NUM	32	PWM2 Wave Number Register
110060BC	PWM2_DATA_WIDTH	32	PWM2 Data Width Register
110060C0	PWM2_THRESH	32	PWM2 Thresh Register
110060C4	PWM2_SEND_WAVENUM	32	PWM2 Send Wave Number register
110060C8	PWM2_VALID	32	PWM2 Valid Register
110060D0	PWM3_CON	32	PWM3 Control Register
110060D4	PWM3_HDURATION	32	PWM3 High Duration Register
110060D8	PWM3_LDURATION	32	PWM3 Low Duration Register
110060DC	PWM3_GDURATION	32	PWM3 Guard Duration Register
110060E0	PWM3_BUF0_BASE_ADDR	32	PWM3 Buffer0 Base Address register
110060E4	PWM3_BUF0_SIZE	32	PWM3 Buffer0 Size Register
110060E8	PWM3_BUF1_BASE_ADDR	32	PWM3 Buffer1 Base Address register
110060EC	PWM3_BUF1_SIZE	32	PWM3 Buffer1 Size Register
110060F0	PWM3_SEND_DATA0	32	PWM3 Send Data0 Register
110060F4	PWM3_SEND_DATA1	32	PWM3 Send Data1 Register
110060F8	PWM3_WAVE_NUM	32	PWM3 Wave Number Register
11006104	PWM3_SEND_WAVENUM	32	PWM3 Send Wave Number register
110060FC	PWM3_DATA_WIDTH	32	PWM3 Data Width Register
11006100	PWM3_THRESH	32	PWM3 Thresh Register
11006108	PWM3_VALID	32	PWM3 Valid Register
11006110	PWM4_CON	32	PWM4 Control Register
11006114	PWM4_HDURATION	32	PWM4 High Duration Register
11006118	PWM4_LDURATION	32	PWM4 Low Duration Register
1100611C	PWM4_GDURATION	32	PWM4 Guard Duration Register
11006120	PWM4_BUF0_BASE_ADDR	32	
11006124	PWM4_BUF0_SIZE	32	PWM4 Buffer0 Size Register
11006128	PWM4_BUF1_BASE_ADDR	32	PWM4 Buffer1 Base Address register
1100612C	PWM4_BUF1_SIZE	32	PWM4 Buffer1 Size Register
11006130	PWM4_SEND_DATA0	32	PWM4 Send Data0 Register
11006134	PWM4_SEND_DATA1	32	PWM4 Send Data1 Register
11006138	PWM4_WAVE_NUM	32	PWM4 Wave Number Register
11006144	PWM4_SEND_WAVENUM	32	PWM4 Send Wave Number Register
1100613C	PWM4_DATA_WIDTH	32	PWM4 Data Width Register
11006140	PWM4_THRESH	32	PWM4 Thresh Register
11006148	PWM4_VALID	32	PWM4 Valid Register
110061CC	PWM_LOOP_BACK_TEST	32	PWM Loop Back Test

Address	Name	Width	Register Function
110061D0	PWM_3DLCM	32	PWM Support For 3D LCM
11006200	PWM_INT_ENABLE	32	PWM Interrupt Enable Register
11006204	PWM_INT_STATUS	32	PWM Interrupt Status Register
11006208	PWM_INT_ACK	32	PWM Interrupt Acknowledge Register
1100620C	PWM_EN_STATUS	32	PWM Enable Status Register
11006210	PWM_CK_26M_SEL	32	PWM BCLK Selection

11006000 PWM_ENABLE PWM Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PWM_SEQ_MODE
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PWM4_EN	PWM3_EN	PWM2_EN	PWM1_EN	PWM0_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
16	PWM_SEQ_MODE	**Set to 1 to enable PWM2, PWM3, PWM4 ,PWM5 sequential delay mode. In this mode, PWM2 starts first and then after PWM3_DELAY_TIME, PWM3 will start. After PWM3 starts, PWM4 will start after PWM4_DELAY_TIME.After PWM4 starts, PWM5 will start after PWM5_DELAY_TIME** Note: The output of PWM_SEQ_MODE is started after PWM2 is enabled. And PWM_SEQ_MODE should be set before PWM3, PWM4 ,PWM5 are enabled or at the same time. Also this mode doesn't work when PWM2 is set at OLD_PWM_MODE and CLKSEL=1.
4	PWM4_EN	0: Disabe PWM4 1: Enable PWM4
3	PWM3_EN	0: Disabe PWM3 1: Enable PWM3
2	PWM2_EN	0: Disabe PWM2 1: Enable PWM2
1	PWM1_EN	0: Disabe PWM1 1: Enable PWM1
0	PWM0_EN	0: Disabe PWM0 1: Enable PWM0

11006004 PWM3_DELAY PWM3 Delay Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																DELAY_CLKSEL
Type																RW

Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PWM3_DELAY_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	DELAY_CLKSEL	**Clock unit of PWM3_DELAY_DURATION** 0: CLK=CLKSRC (32k is not allowed.) 1: CLK=CLKSRC/1625
15:0	PWM3_DELAY_DURATION	**Duration between PWM2 and PWM3 start point.**

11006008 PWM4_DELAY PWM4 Delay Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																DELAY_CLKSEL
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PWM4_DELAY_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	DELAY_CLKSEL	**Clock unit of PWM4_DELAY_DURATION** 0: CLK=CLKSRC (32k is not allowed.) 1: CLK=CLKSRC/1625
15:0	PWM4_DELAY_DURATION	**Duration between PWM3 and PWM4 start point**

11006010 PWM0_CON PWM0 Control Register 00007E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	OLD_PWM_MODE	**Uses old PWM mode** Note: Using old PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock however cannot work in system sleep mode. 0: New PWM mode

Bit(s)	Name	Description
		1: Old PWM mode
14:9	STOP_BITPOS	**Stop bit position for source data in periodical mode** In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	**PWMo output value during guard time**
7	IDLE_VALUE	**PWMo output value in idle state**
6	MODE	**Selects random generator mode** 0: Periodical PWM mode 1: Random PWM mode
5	SRCSEL	**Selects PWMo data source** 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K; CLK is not used. 1: CLK=32K; CLK can be used.
3	CLKSEL	**Selects PWMo clock** 0: CLK=CLKSRC 1: CLK=CLKSRC/1625
2:0	CLKDIV	**Selects PWMo clock scale** 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

11006014 PWMo_HDURATION PWMo High Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	**PWMo pulse duration based on the current clock when PWM output is high** If duration =N, program N-1 in this register. Note: The duration of PWM must not be 0.

11006018 PWMo_LDURATION PWMo Low Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	LDURATION	**PWM0 pulse duration based on the current clock when PWM output is low** If duration =N, program N-1 in this register. Note: The duration of PWM must not be 0.

1100601C PWM0_GDURATION PWM0 Guard Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2: The guard duration of old mode is set by PWM_DATA_WIDTH.

11006020 PWM0_BUF0_BASE_ADDR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	**Base address of memory buffer0 for PWM0's waveform data**

11006024 PWM0_BUF0_SIZE PWM0 Buffer0 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in memory buffer0 PWM0 should generate** If it equals N, program N-1 in this register. Note: The size is in unit of 32-bit data.

11006028 PWM0_BUF1_BASE_ADDR PWM0 Buffer1 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of memory buffer1 for PWM0's waveform data** Note: The memory buffer1 is useless in periodical mode.

1100602C PWM0_BUF1_SIZE PWM0 Buffer1 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in memory buffer1 PWM0 should generate** If it equals N, program N-1 in this register.

11006030 PWM0_SEND_DATA0 PWM0 Send Data0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM0 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

11006034 PWM0_SEND_DATA1 PWM0 Send Data1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM0 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

11006038 PWM0_WAVE_NUM PWM0 Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM0 will generate from pulse data repeatedly** Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.

1100603C PWM0_DATA_WIDTH PWM0 Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	**PWM0 pulse data width in old PWM mode**

11006040 PWM0_THRESH PWM0 Thresh Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	**PWM0 pulse data high/low switching threshold in old PWM mode**

11006044 PWM0_SEND_WAVENUM PWM0 Send Wave Number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SEND_WAVENUM	**Number by which PWM0 has already generated from specified data source in periodical mode**

11006048 PWM0_VALID PWM0 Valid Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	0: Memory1 is empty. 1: Memory1 is not empty. When finishing writing data to memory1, write 1 to inform PWM the data in memory1 are ready.
0	BUF0_VALID	0: Memory0 is empty. 1: Memory0 is not empty. When finishing writing data to memory0, write 1 to inform PWM the data in memory0 are ready.

11006050 PWM1_CON PWM1 Control Register 00007E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	OLD_PWM_MODE	**Uses old PWM mode** Note: Using old PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock however cannot work in system sleep mode. 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	**Note: Using old PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock however cannot work in system sleep mode.**
8	GUARD_VALUE	**PWM1 output value during guard time**
7	IDLE_VALUE	**PWM1 output value in idle state**
6	MODE	**Selects random generator mode** 0: Periodical PWM mode 1: Random PWM mode
5	SRCSEL	**Selects PWM1 data source** 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K; CLK is not used. 1: CLK=32K; CLK can be used.
3	CLKSEL	**Selects PWM0 clock** 0: CLK=CLKSRC 1: CLK=CLKSRC/1625
2:0	CLKDIV	**Selects PWM1 clock scale** 000b: CLK Hz

Bit(s)	Name	Description
		001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

11006054 PWM1_HDURATION PWM1 High Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	**PWM1 pulse duration based on the current clock when PWM output is high** If duration =N, program N-1 in this register. Note: The duration of PWM must not be 0.

11006058 PWM1_LDURATION PWM1 Low Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	LDURATION	**PWM1 pulse duration based on the current clock when PWM output is low** If duration =N, program N-1 in this register. Note: The duration of PWM must not be 0.

1100605C PWM1_GDURATION PWM1 Guard Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2: The guard duration of old mode is set by PWM_DATA_WIDTH.

11006060 PWM1_BUF0_BASE_ADDR PWM1 Buffer0 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	**Base address of memory buffer0 for PWM1's waveform data**

11006064 PWM1_BUF0_SIZE PWM1 Buffer0 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in memory buffer0 PWM1 should generate** If it equals N, program N-1 in this register. Note: The size is in unit of 32-bit data.

11006068 PWM1_BUF1_BASE_ADDR PWM1 Buffer1 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of memory buffer1 for PWM10's waveform data** Note: The memory buffer1 is useless in periodical mode.

1100606C PWM1_BUF1_SIZE PWM1 Buffer1 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in memory buffer1 PWM1 should generate** If it equals N, program N-1 in this register.

11006070 PWM1_SEND_DATA0 PWM1 Send Data0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM1 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

11006074 PWM1_SEND_DATA1 PWM1 Send Data1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM1 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

11006078 PWM1_WAVE_NUM PWM1 Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM1 will generate from pulse data repeatedly** Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.

1100607C PWM1_DATA_WIDTH PWM1 Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	**PWM1 pulse data width in old PWM mode**

11006080 PWM1_THRESH PWM1 Thresh Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	**PWM1 pulse data high/low switching threshold in old PWM mode**

11006084 PWM1_SEND_WAVENUM PWM1 Send Wave Number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SEND_WAVENUM	**Number by which PWM1 has already generated from specified data source in periodical mode**

11006088 PWM1_VALID PWM1 Valid Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	0: Memory1 is empty. 1: Memory1 is not empty. When finishing writing data to memory1, write 1 to inform PWM the data in memory1 are ready.
0	BUF0_VALID	0: Memory0 is empty. 1: Memory0 is not empty. When finishing writing data to memory0, write 1 to inform PWM the data in memory0 are ready.

11006090 PWM2_CON PWM2 Control Register 00007E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	OLD_PWM_MODE	**Uses old PWM mode** Note: Using old PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock source however cannot work in system sleep mode. 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	**Stop bit position for source data in periodical mode** In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	**PWM2 output value during guard time**
7	IDLE_VALUE	**PWM2 output value in idle state**
6	MODE	**Selects random generator mode** 0: Periodical PWM mode 1: Random PWM mode
5	SRCSEL	**Selects PWM2 data source** 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K; CLK is not used. 1: CLK=32K; CLK can be used.
3	CLKSEL	**Selects PWM0 clock** 0: CLK=CLKSRC 1: CLK=CLKSRC/1625
2:0	CLKDIV	**Selects PWM2 clock scale** 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

11006094 PWM2_HDURATION PWM2 High Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	**PWM2 pulse duration based on the current clock when PWM output is high** If duration =N, program N-1 in this register. Note: The duration of PWM must not be 0.

11006098 PWM2_LDURATION PWM2 Low Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	LDURATION	**PWM2 pulse duration based on the current clock when PWM output is low** If duration =N, program N-1 in this register. Note: The duration of PWM must not be 0.

1100609C PWM2_GDURATION PWM2 Guard Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2: The guard duration of old mode is set by PWM_DATA_WIDTH.

110060A0 PWM2_BUF0_BASE_ADDR PWM2 Buffer0 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	**Base address of memory buffer0 for PWM2's waveform data**

110060A4 PWM2_BUF0_SIZE PWM2 Buffer0 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in memory buffer0 PWM2 should generate** If it equals N, program N-1 in this register.

110060A8 PWM2_BUF1_BASE_ADDR PWM2 Buffer1 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of memory buffer1 for PWM2's waveform data** Note: The memory buffer1 is useless in periodical mode.

110060AC PWM2_BUF1_SIZE PWM2 Buffer1 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in memory buffer1 PWM2 should generate** If it equals N, program N-1 in this register.

110060B0 PWM2_SEND_DATA0 PWM2 Send Data0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM2 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

110060B4 PWM2_SEND_DATA1 PWM2 Send Data1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM2 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

110060B8 PWM2_WAVE_NUM PWM2 Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM2 will generate from pulse data repeatedly** Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.

110060BC PWM2_DATA_WIDTH PWM2 Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	**PWM2 pulse data width in old PWM mode**

110060C0 PWM2_THRESH PWM2 Thresh Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	**PWM2 pulse data high/low switching threshold in old PWM mode**

110060C4 PWM2_SEND_WAVENUM PWM2 Send Wave Number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SEND_WAVENUM	**Number by which PWM2 has already generated from specified data source in periodical mode**

110060C8 PWM2_VALID PWM2 Valid Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	0: Memory1 is empty. 1: Memory1 is not empty. When finishing writing data to memory1, write 1 to inform PWM the data in memory1 are ready.
0	BUF0_VALID	0: Memory0 is empty. 1: Memory0 is not empty. When finishing writing data to memory0, write 1 to inform PWM the data in memory0 are ready.

110060D0 PWM3_CON PWM3 Control Register 00007E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	OLD_PWM_MODE	**Uses old PWM mode** Note: Using old PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock source however cannot work in system sleep mode. 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	**Stop bit position for source data in periodical mode** In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	**PWM3 output value during guard time**
7	IDLE_VALUE	**PWM3 output value in idle state**
6	MODE	**Selects random generator mode**

Bit(s)	Name	Description
		0: Periodical PWM mode 1: Random PWM mode
5	SRCSEL	**Selects PWM3 data source** 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K; CLK is not used. 1: CLK=32K; CLK can be used.
3	CLKSEL	**Selects PWM0 clock** 0: CLK=CLKSRC 1: CLK=CLKSRC/1625
2:0	CLKDIV	**Selects PWM3 clock scale** 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

110060D4 PWM3_HDURATION PWM3 High Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	**PWM3 pulse duration based on the current clock when PWM output is high** If duration =N, program N-1 in this register. Note: The duration of PWM must not be 0.

110060D8 PWM3_LDURATION PWM3 Low Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	LDURATION	**PWM3 pulse duration based on the current clock when PWM output is low** If duration =N, program N-1 in this register. Note: The duration of PWM must not be 0.

110060DC PWM3_GDURATION PWM3 Guard Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2: The guard duration of old mode is set by PWM_DATA_WIDTH.

110060E0 PWM3_BUF0_BASE_ADDR PWM3 Buffer0 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	**Base address of memory buffer0 for PWM3's waveform data**

110060E4 PWM3_BUF0_SIZE PWM3 Buffer0 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in memory buffer0 PWM3 should generate** If it equals N, program N-1 in this register.

110060E8 PWM3_BUF1_BASE_ADDR PWM3 Buffer1 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of memory buffer1 for PWM3's waveform data** Note: The memory buffer1 is useless in periodical mode.

110060EC PWM3_BUF1_SIZE PWM3 Buffer1 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in memory buffer1 PWM3 should generate** If it equals N, program N-1 in this register.

110060F0 PWM3_SEND_DATA0 PWM3 Send Data0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM3 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

110060F4 PWM3_SEND_DATA1 PWM3 Send Data1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM3 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

110060F8 PWM3_WAVE_NUM PWM3 Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM3 will generate from pulse data repeatedly** Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.

11006104 PWM3_SEND_WAVENUM PWM3 Send Wave Number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SEND_WAVENUM	**Number by which PWM3 has already generated from specified data source in periodical mode**

110060FC PWM3_DATA_WIDTH PWM3 Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	**PWM3 pulse data width in old PWM mode**

11006100 PWM3_THRESH PWM3 Thresh Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	**PWM3 pulse data high/low switching threshold in old PWM mode**

11006108 PWM3_VALID PWM3 Valid Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUFo_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	0: Memory1 is empty.

Bit(s)	Name	Description
0	BUF0_VALID	1: Memory1 is not empty. When finishing writing data to memory1, write 1 to inform PWM the data in memory1 are ready. 0: Memory0 is empty. 1: Memory0 is not empty. When finishing writing data to memory0, write 1 to inform PWM the data in memory0 are ready.

11006110 PWM4_CON PWM4 Control Register 00007E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	OLD_PWM_MODE	**Uses old PWM mode** Note: Using old PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. Only old PWM mode with 32kHz clock source however cannont work in system sleep mode. 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	**Stop bit position for source data in periodical mode** In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	**PWM4 output value during guard time**
7	IDLE_VALUE	**PWM4 output value in idle state**
6	MODE	**Selects random generator mode** 0: Periodical PWM mode. 1: Random PWM mode
5	SRCSEL	**Selects PWM4 data source** 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K CLK IS NOT USED 1: CLK=32K CLK CAN BE USED
3	CLKSEL	**Selects PWM4 clock** 0: CLK=CLKSRC 1: CLK=CLKSRC/1625
2:0	CLKDIV	**Selects PWM4 clock scale** 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

Bit(s)	Name	Description

11006114 PWM4_HDURATION PWM4 High Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	**PWM4 pulse duration based on the current clock when PWM output is high** If duration =N, program N-1 in this register. Note: The duration of PWM must not be 0.

11006118 PWM4_LDURATION PWM4 Low Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	LDURATION	**PWM4 pulse duration based on the current clock when PWM output is low** If duration =N, program N-1 in this register. Note: The duration of PWM must not be 0.

1100611C PWM4_GDURATION PWM4 Guard Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE**

Bit(s)	Name	Description
		If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2: The guard duration of old mode is set by PWM_DATA_WIDTH.

11006120 PWM4_BUF0_BASE_ADDR **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	**Base address of memory buffer0 for PWM4's waveform data**

11006124 PWM4_BUF0_SIZE PWM4 Buffer0 Size Register **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in memory buffer0 PWM4 should generate** If it equals N, program N-1 in this register.

11006128 PWM4_BUF1_BASE_ADDR PWM4 Buffer1 Base Address register **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of memory buffer1 for PWM4's waveform data** Note: The memory buffer1 is useless in periodical mode.

1100612C PWM4_BUF1_SIZE PWM4 Buffer1 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in memory buffer1 PWM4 should generate** If it equals N, program N-1 in this register.

11006130 PWM4_SEND_DATA0 PWM4 Send Data0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM4 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

11006134 PWM4_SEND_DATA1 PWM4 Send Data1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM4 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

11006138 PWM4_WAVE_NUM PWM4 Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM4 will generate from pulse data repeatedly** Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.

11006144 PWM4_SEND_WAVENUM PWM4 Send Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SEND_WAVENUM	**Number by which PWM4 has already generated from specified data source in periodical mode**

1100613C PWM4_DATA_WIDTH PWM4 Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	**PWM4 pulse data width in old PWM mode**

11006140 PWM4_THRESH PWM4 Thresh Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	**PWM4 pulse data high/low switching threshold in old PWM mode**

11006148 PWM4_VALID PWM4 Valid Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	0: Memory1 is empty. 1: Memory1 is not empty. When finishing writing data to memory1, write 1 to inform PWM the data in memory1 are ready.
0	BUF0_VALID	0: Memory0 is empty. 1: Memory0 is not empty. When finishing writing data to memory0, write 1 to inform PWM the data in memory0 are ready.

110061CC PWM_LOOP_BACK_TEST PWM Loop Back Test 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PWM4_STATUS	PWM3_STATUS	PWM2_STATUS	PWM1_STATUS	PWM0_STATUS
Type												RU	RU	RU	RU	RU

Reset												0	0	0	0	0

Bit(s)	Name	Description
4	PWM4_STATUS	0: PWM4 output is low. 1: PWM4 output is high.
3	PWM3_STATUS	0: PWM3 output is low. 1: PWM3 output is high.
2	PWM2_STATUS	0: PWM2 output is low. 1: PWM2 output is high.
1	PWM1_STATUS	0: PWM1 output is low. 1: PWM1 output is high.
0	PWM0_STATUS	0: PWM0 output is low. 1: PWM0 output is high.

110061D0 PWM_3DLCM PWM Support For 3D LCM 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												PWM_3DLCM_5	PWM_3DLCM_4	PWM_3DLCM_3	PWM_3DLCM_2	PWM_3DLCM_1
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PWM_3DLCM_SYNC			PWM_3DLCM_5_base	PWM_3DLCM_4_base	PWM_3DLCM_3_base	PWM_3DLCM_2_base	PWM_3DLCM_1_base			PWM_3DLCM_5_INV	PWM_3DLCM_4_INV	PWM_3DLCM_3_INV	PWM_3DLCM_2_INV	PWM_3DLCM_1_INV	PWM_3DLCM_EN
Type	RW			RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW
Reset	0			0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
20	PWM_3DLCM_5	**Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.** 0: PWM4 is not selected as PWM auxiliary channel. 1: PWM4 is selected as PWM auxiliary channel.
19	PWM_3DLCM_4	**Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.** 0: PWM3 is not selected as PWM auxiliary channel. 1: PWM3 is selected as PWM auxiliary channel.
18	PWM_3DLCM_3	**Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.** 0: PWM2 is not selected as PWM auxiliary channel. 1: PWM2 is selected as PWM auxiliary channel.
17	PWM_3DLCM_2	**Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.** 0: PWM1 is not selected as PWM auxiliary channel. 1: PWM1 is selected as PWM auxiliary channel.
16	PWM_3DLCM_1	**Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.** 0: PWM0 is not selected as PWM auxiliary channel. 1: PWM0 is selected as PWM auxiliary channel.
15	PWM_3DLCM_SYNC	0: PWM auxiliary channel does not keep low when PWM base channel is disabled. 1: PWM auxiliary channel keeps low when PWM base channel is disabled.

Bit(s)	Name	Description
12	PWM_3DLCM_5_base	**Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.** 0: PWM4 is not selected as PWM base channel. 1: PWM4 is selected as PWM base channel.
11	PWM_3DLCM_4_base	**Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.** 0: PWM3 is not selected as PWM base channel. 1: PWM3 is selected as PWM base channel.
10	PWM_3DLCM_3_base	**Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.** 0: PWM2 is not selected as PWM base channel. 1: PWM2 is selected as PWM base channel.
9	PWM_3DLCM_2_base	**Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.** 0: PWM1 is not selected as PWM base channel. 1: PWM1 is selected as PWM base channel.
8	PWM_3DLCM_1_base	**Note: The PWM channel number should not be selected as base channel and auxiliary channel at the same time.** 0: PWM0 is not selected as PWM base channel. 1: PWM0 is selected as PWM base channel.
5	PWM_3DLCM_5_INV	0: PWM4 is the same as PWM base channel when PWM4 is selected as auxiliary channel. 1: PWM4 is inversion of PWM base channel when PWM4 is selected as auxiliary channel.
4	PWM_3DLCM_4_INV	0: PWM3 is the same as PWM base channel when PWM3 is selected as auxiliary channel. 1: PWM3 is inversion of PWM base channel when PWM3 is selected as auxiliary channel.
3	PWM_3DLCM_3_INV	0: PWM2 is the same as PWM base channel when PWM2 is selected as auxiliary channel. 1: PWM2 is inversion of PWM base channel when PWM2 is selected as auxiliary channel.
2	PWM_3DLCM_2_INV	0: PWM1 is the same as PWM base channel when PWM1 is selected as auxiliary channel. 1: PWM1 is inversion of PWM base channel when PWM1 is selected as auxiliary channel.
1	PWM_3DLCM_1_INV	0: PWM0 is the same as PWM base channel when PWM0 is selected as auxiliary channel. 1: PWM0 is inversion of PWM base channel when PWM0 is selected as auxiliary channel.
0	PWM_3DLCM_EN	0: Disable 3D_LCM for PWM 1: Enable 3D_LCM for PWM

11006200 PWM_INT_ENABLE PWM Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							PWM4_INT_UNDERFLOW_EN	PWM4_INT_FINISH_EN	PWM3_INT_UNDERFLOW_EN	PWM3_INT_FINISH_EN	PWM2_INT_UNDERFLOW_EN	PWM2_INT_FINISH_EN	PWM1_INT_UNDERFLOW_EN	PWM1_INT_FINISH_EN	PWM0_INT_UNDERFLOW_EN	PWM0_INT_FINISH_EN

Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	PWM4_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM4 1: Enable underflow interrupt for PWM4
8	PWM4_INT_FINISH_EN	0: Disable finished interrupt for PWM4 1: Enable finished interrupt for PWM4
7	PWM3_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM3 1: Enable underflow interrupt for PWM3
6	PWM3_INT_FINISH_EN	0: Disable finished interrupt for PWM3 1: Enable finished interrupt for PWM3
5	PWM2_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM2 1: Enable underflow interrupt for PWM2
4	PWM2_INT_FINISH_EN	0: Disable finished interrupt for PWM2 1: Enable finished interrupt for PWM2
3	PWM1_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM1 1: Enable underflow interrupt for PWM1
2	PWM1_INT_FINISH_EN	0: Disable finished interrupt for PWM1 1: Enable finished interrupt for PWM1
1	PWM0_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM0 1: Enable underflow interrupt for PWM0
0	PWM0_INT_FINISH_EN	0: Disable finished interrupt for PWM0 1: Enable finished interrupt for PWM0

11006204 PWM_INT_STATUS PWM Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							PWM4_INT_UNDERFLOW_ST	PWM4_INT_FINISH_ST	PWM3_INT_UNDERFLOW_ST	PWM3_INT_FINISH_ST	PWM2_INT_UNDERFLOW_ST	PWM2_INT_FINISH_ST	PWM1_INT_UNDERFLOW_ST	PWM1_INT_FINISH_ST	PWM0_INT_UNDERFLOW_ST	PWM0_INT_FINISH_ST
Type							RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	PWM4_INT_UNDERFLOW_ST	0: PWM4 underflow interrupt has not come. 1: PWM4 underflow interrupt has come.
8	PWM4_INT_FINISH_ST	0: PWM4 finished interrupt has not come. 1: PWM4 finished interrupt has come.
7	PWM3_INT_UNDERFLOW_ST	0: PWM3 underflow interrupt has not come. 1: PWM3 underflow interrupt has come.
6	PWM3_INT_FINISH_ST	0: PWM3 finished interrupt has not come. 1: PWM3 finished interrupt has come.
5	PWM2_INT_UNDERFLOW_ST	0: PWM2 underflow interrupt has not come. 1: PWM2 underflow interrupt has come.
4	PWM2_INT_FINISH_ST	0: PWM2 finished interrupt has not come. 1: PWM2 finished interrupt has come.

Bit(s)	Name	Description
3	PWM1_INT_UNDERFLOW_ST	0: PWM1 underflow interrupt has not come. 1: PWM1 underflow interrupt has come.
2	PWM1_INT_FINISH_ST	0: PWM1 finished interrupt has not come. 1: PWM1 finished interrupt has come.
1	PWM0_INT_UNDERFLOW_ST	0: PWM0 underflow interrupt has not come. 1: PWM0 underflow interrupt has come.
0	PWM0_INT_FINISH_ST	0: PWM0 finished interrupt has not come. 1: PWM0 finished interrupt has come.

11006208 PWM_INT_ACK PWM Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							PWM4_INT_UNDERFLOW_ACK	PWM4_INT_FINISH_ACK	PWM3_INT_UNDERFLOW_ACK	PWM3_INT_FINISH_ACK	PWM2_INT_UNDERFLOW_ACK	PWM2_INT_FINISH_ACK	PWM1_INT_UNDERFLOW_ACK	PWM1_INT_FINISH_ACK	PWM0_INT_UNDERFLOW_ACK	PWM0_INT_FINISH_ACK
Type							WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	PWM4_INT_UNDERFLOW_ACK	0: Does not clear PWM4 underflow interrupt 1: Clear PWM4 underflow interrupt
8	PWM4_INT_FINISH_ACK	0: Does not clear PWM4 finished interrupt 1: Clear PWM4 finished interrupt
7	PWM3_INT_UNDERFLOW_ACK	0: Does not clear PWM3 underflow interrupt 1: Clear PWM3 underflow interrupt
6	PWM3_INT_FINISH_ACK	0: Does not clear PWM3 finished interrupt 1: Clear PWM3 finished interrupt
5	PWM2_INT_UNDERFLOW_ACK	0: Does not clear PWM2 underflow interrupt 1: Clear PWM2 underflow interrupt
4	PWM2_INT_FINISH_ACK	0: Does not clear PWM2 finished interrupt 1: Clear PWM2 finished interrupt
3	PWM1_INT_UNDERFLOW_ACK	0: Does not clear PWM1 underflow interrupt 1: Clear PWM1 underflow interrupt
2	PWM1_INT_FINISH_ACK	0: Does not clear PWM1 finished interrupt 1: Clear PWM1 finished interrupt
1	PWM0_INT_UNDERFLOW_ACK	0: Does not clear PWM0 underflow interrupt 1: Clear PWM0 underflow interrupt
0	PWM0_INT_FINISH_ACK	0: Does not clear PWM0 finished interrupt 1: Clear PWM0 finished interrupt

1100620C PWM_EN_STATUS PWM Enable Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PWM4_EN_ST	PWM3_EN_ST	PWM2_EN_ST	PWM1_EN_ST	PWM0_EN_ST
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	PWM4_EN_ST	**PWM4 enabling status**
3	PWM3_EN_ST	**PWM3 enabling status**
2	PWM2_EN_ST	**PWM2 enabling status**
1	PWM1_EN_ST	**PWM1 enabling status**
0	PWM0_EN_ST	**PWM0 enabling status**

11006210 PWM_CK_26M_SEL PWM BCLK Selection 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PWM_26M_SEL
Type																RW
Reset																1

Bit(s)	Name	Description
0	PWM_26M_SEL	0: Select bus CLK as BCLK 1: Select 26M fix CLK as BCLK

1.16 I2C/SCCB Controller (I2C 0)

1.16.1 Introduction

I2C (Inter-IC)/SCCB (Serial Camera Control Bus) is a two-wire serial interface. The two signals are SCL and SDA. SCL is a clock signal that is driven by the master. SDA is a bi-directional data signal that can be driven by either the master or the slave. This generic controller supports the master role and conforms to the I2C specification.

1.16.2 Features

- I2C compliant master mode operation
- Adjustable clock speed for LS/FS mode operation
- Supports 7-bit/10-bit addressing
- Supports high-speed mode
- Supports slave clock extension
- START/STOP/REPEATED START condition
- Manual transfer mode
- Multi-write per transfer
- Multi-read per transfer
- Multi-transfer per transaction
- Combined format transfer with length change capability.-
- Active drive/wired-and I/O configuration

1.16.2.1 Manual Transfer Mode

The controller offers manual mode.

When the manual mode is selected, in addition to the slave address register, the controller has a built-in 8-byte deep FIFO which allows MCU to prepare up to 8 bytes of data for a write transfer, or read up to 8 bytes of data for a read transfer.

1.16.3 Block Diagram

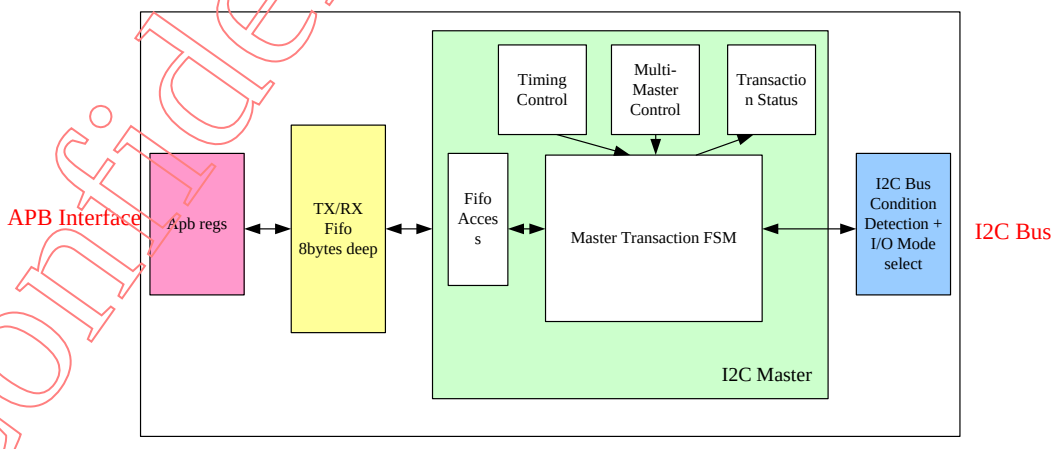


Figure 1-10. Block diagram of I2C

1.16.4 Register Definition

Module name: I2C Base address: (+11007000h)

Address	Name	Width	Register Function
11007000	DATA_PORT	16	Data Port Register
11007004	SLAVE_ADDR	16	Slave Address Register
11007008	INTR_MASK	16	**Interrupt Mask Register** This register provides masks for the corresponding interrupt sources as indicated in intr_stat register. 1 = Allow interrupt 0 = Disable interrupt *Note: While disabled, the corresponding interrupt will not be asserted, however the intr_stat will still be updated with the status, i.e. mask does not affect intr_stat register values.*
1100700C	INTR_STAT	16	**Interrupt Status Register** When an interrupt is issued by I2C controller, this register will need to be read by MCU to determine the cause for the interrupt. After this status has been read and appropriate actions are taken, the corresponding interrupt source will need to be written 1 to clear.
11007010	CONTROL	16	Control Register
11007014	TRANSFER_LEN	16	Transfer Length Register (Number of Bytes per Transfer)
11007018	TRANSAC_LEN	16	Transaction Length Register (Number of Transfers per Transaction)
1100701C	DELAY_LEN	16	Inter Delay Length Register
11007020	TIMING	16	**Timing Control Register** LS/FS only. This register is used to control the output waveform timing.
11007024	START	16	Start Register
11007028	EXT_CONF	16	Extension Configuration Register
11007030	FIFO_STAT	16	FIFO Status Register
11007034	FIFO_THRESH	16	**FIFO Thresh Register** (For debugging only) By default, these values do not need to be adjusted. *Note: For RX, no time-out mechanism is implemented. Therefore, RX_trig_thresh must be left at 0, or there would be data left in FIFO that is not fetched by the DMA controller.*
11007038	FIFO_ADDR_CLR	16	FIFO Address Clear Register
11007040	IO_CONFIG	16	**IO Config Register**

Address	Name	Width	Register Function
			This register is used to configure the I/O for the SDA and SCL lines to select between normal I/O mode, or open-drain mode to support wired-and bus.
11007044	**MULTIMAS**	16	**Multiple I2C Masters** This registers contains options for supporting multi-master features.
11007048	**HS**	16	**High Speed Mode Register** This register contains options for supporting high speed operation features.
11007050	**SOFTRESET**	16	Soft Reset Register
11007054	**HW_DCM_EN**	16	HW DCM Enable
11007064	**DEBUGSTAT**	16	Debug Status Register
11007068	**DEBUGCTRL**	16	Debug Control Register
1100706C	**TRANSFER_LEN_AUX**	16	Transfer Length Register (Number of Bytes per Transfer)

11007000 DATA_PORT Data Port Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA_PORT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DATA_PORT**	DATA_PORT	**FIFO access port** During master write sequences (slave_addr[0] = 0), this port can be written by APB, and during master read sequences (slave_addr[0] = 1), this port can be read by APB. *Note: Slave_addr must be set correctly before accessing FIFO.* For debugging only: If the fifo_apb_debug bit is set, FIFO can be read and written by the APB.

11007004 SLAVE_ADDR Slave Address Register 00BF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SLAVE_ADDR							
Type									RW							
Reset									1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
7:0	**SLAVE_ADDR**	SLAVE_ADDR	**Specifies the slave address of the device to be accessed** Bit 0 is defined by the I2C protocol as a bit that indicates the direction of transfer.

Bit(s)	Mnemonic	Name	Description
			0: Master write 1: Master read

11007008 INTR_MASK Interrupt Mask Register 00FF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SPARE			MASK_RS_TRANSFER	MASK_ARB_LOST	MASK_HS_NACKERR	MASK_ACKERR	MASK_TRANSAC_COMP
Type									RW			RW	RW	RW	RW	RW
Reset									1	1	1	1	1	1	1	1

Overview: This register provides masks for the corresponding interrupt sources as indicated in intr_stat register. 1 = allow interrupt; 0 = disable interrupt. Note that while disabled, the corresponding interrupt will not be asserted. However, intr_stat will still be updated with the status, i.e. mask does not affect intr_stat register values.

Bit(s)	Mnemonic	Name	Description
7:5	SPAR	SPAR	Reserved
4	MASK_RS_TRANSFER	MASK_RS_TRANSFER	Setting this value to 0 will mask RS_TRANSFER interrupt signal.
3	MASK_ARB_LOST	MASK_ARB_LOST	Setting this value to 0 will mask ARB_LOST interrupt signal.
2	MASK_HS_NACKERR	MASK_HS_NACKERR	Setting this value to 0 will mask HS_NACKERR interrupt signal.
1	MASK_ACKERR	MASK_ACKERR	Setting this value to 0 will mask ACK_ERR interrupt signal.
0	MASK_TRANSAC_COMP	MASK_TRANSAC_COMP	Setting this value to 0 will mask TRANSAC_COMP interrupt signal.

1100700C INTR_STAT Interrupt Status Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RS_TRANSFER	ARB_LOST	HS_NACKERR	ACKERR	TRANSAC_COMP

1100700C INTR_STAT Interrupt Status Register 0000

Type												W1C	W1C	W1C	W1C	W1C
Reset												0	0	0	0	0

Overview: When an interrupt is issued by the I2C controller, this register will need to be read by MCU to determine the cause for the interrupt. After this status has been read and appropriate actions are taken, the corresponding interrupt source will need to be written 1 to clear.

Bit(s)	Mnemonic	Name	Description
4	**RS_TRANSFER**	RS_TRANSFER	This status is asserted if the end of every re-start transfer.
3	**ARB_LOST**	ARB_LOST	This status is asserted if the I2C controller loses arbitration.
2	**HS_NACKERR**	HS_NACKERR	This status is asserted if HS master code NACK error detection is enabled. If enabled, HS master code NACK err will cause transaction to end, and stop will be issued.
1	**ACKERR**	ACKERR	This status is asserted if ACK error detection is enabled. If enabled, ACKERR will cause transaction to end, and stop will be issued.
0	**TRANSAC_COMP**	TRANSAC_COMP	This status is asserted when a transaction is completed successfully.

11007010 CONTROL Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**TRANSFER_LEN_CHANGE**	**ACKERR_DET_EN**	**DIR_CHANGE**	**CLK_EXT_EN**	**DMA_EN**	**RS_STOP**	
Type										RW	RW	RW	RW	RW	RW	
Reset										0	0	0	0	0	0	

Bit(s)	Mnemonic	Name	Description
6	**TRANSFER_LEN_CHANGE**	TRANSFER_LEN_CHANGE	**Specifies whether or not to change the transfer length after the fist transfer is completed** If enabled, the transfers after the first transfer will use the transfer_len_aux parameter.
5	**ACKERR_DET_EN**	ACKERR_DET_EN	**Enables slave ACK error detection** When enabled, if slave ACK error is detected, the master shall terminate the transaction by issuing a STOP condition and then asserts the ACKERR interrupt. MCU handles this case appropriately and then resets the FIFO address before reissuing transaction again. If this option is disabled, the controller will ignore slave ACK error and keep on scheduled transaction. 0: Disable 1: Enable

Bit(s)	Mnemonic	Name	Description
4	**DIR_CHANGE**	DIR_CHANGE	**Combined transfer format, where the direction of transfer is to be changed from write to read after the FIRST RS condition** *Note: When set to 1, the transfers after the direction change will be based on the transfer_len_aux parameter.* 0: Disable 1: Enable
3	**CLK_EXT_EN**	CLK_EXT_EN	**I2C spec allows slaves to hold the SCL line low if it is not yet ready for further processing.** Therefore, if this bit is set to 1, the master controller will enter a high wait state until the slave releases the SCL line.
2	**DMA_EN**	DMA_EN	**By default, this is disabled, and the FIFO data shall be manually prepared by MCU.** This default setting should be used for transfer sizes of smaller than 8 data bytes and no multiple transfer is configured. When enabled, DMA requests are turned on, and the FIFO data should be prepared in memory.
1	**RS_STOP**	RS_STOP	**In LS/FS mode, this bit affects multi-transfer transaction only.** It controls whether or not the REPEATED-START condition is used between transfers. The last ending transfer always ends with a STOP. In HS mode, this bit must be set to 1. 0: Use STOP 1: Use REPEATED-START

11007014 **TRANSFER_LEN** **Transfer Length Register (Number of Bytes per Transfer)** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
15:0	**TRANSFER_LEN**	TRANSFER_LEN	**Indicates the number of data bytes to be transferred in 1 transfer unit (excluding slave address byte)** *Note: The value must be set to be bigger than 1; otherwise no transfer will take place.*

11007018 **TRANSAC_LEN** **Transaction Length Register (Number of Transfers per Transaction)** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TRANSAC_LEN							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
7:0	**TRANSAC_LEN**	TRANSAC_LEN	**Indicates the number of transfers to be transferred in 1 transaction** *Note: The value must be set to be bigger than 1; otherwise no transfer will take place.*

1100701C DELAY_LEN Inter Delay Length Register 0002

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DELAY_LEN							
Type									RW							
Reset									0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0	**DELAY_LEN**	DELAY_LEN	**Sets up wait delay between consecutive transfers when RS_STOP bit is set to 0** Unit: Half the pulse width

11007020 TIMING Timing Control Register 1303

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_READ_ADJ	DATA_READ_TIME				SAMPLE_CNT_DIV					STEP_CNT_DIV					
Type	RW	RW				RW					RW					
Reset	0	0	0	1		0	1	1			0	0	0	0	1	1

Overview: LS/FS only. This register is used to control the output waveform timing. Each half pulse width, i.e. each high or low pulse, is equal to (step_cnt_div+1)*(sample_cnt_div+1)*1/4*BASE_CLOCK_PERIOD.

Bit(s)	Mnemonic	Name	Description
15	**DATA_READ_ADJ**	DATA_READ_ADJ	When set to 1, data latch in sampling time during master reads are adjusted according to the DATA_READ_TIME value. Otherwise, by default, the data are latched in at half of the high pulse width point. This value must be set to be smaller than or equal to half the high pulse width.
14:12	**DATA_READ_TIME**	DATA_READ_TIME	This value is valid only when DATA_READ_ADJ is set to 1. This can be used to adjust so that the data are latched in at earlier sampling points (assuming data are settled by then)
10:8	**SAMPLE_CNT_DIV**	SAMPLE_CNT_DIV	Used for LS/FS only. This adjusts the width of each sample. (sample width = sample_cnt_div*1/4 BASE_CLOCK_PERIOD)
5:0	**STEP_CNT_DIV**	STEP_CNT_DIV	Specifies the number of samples per half pulse width, i.e. each high or low pulse

11007024 START Start Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RS_MUL_CNFG	RS_MUL_TRIG	RS_MUL_CLR													START
Type	RW	RW	RO													RW
Reset	0	0	0													0

Bit(s)	Mnemonic	Name	Description
15	RS_MUL_CNFG	RS_MUL_CNFG	**Configuration of re-start multi-transfer**
14	RS_MUL_TRIG	RS_MUL_TRIG	**Start bit of re-start multi-transfer**
13	RS_MUL_CLR	RS_MUL_CLR	**Clear bit of re-start multi-transfer**
0	START	START	**Starts the transaction on the bus** It is auto de-asserted at the end of the transaction.

11007028 EXT_CONF Extension Configuration Register 1800

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_TIME															EXT_EN
Type	RW															RW
Reset	0	0	0	1	1	0	0	0								0

Bit(s)	Mnemonic	Name	Description
15:8	EXT_TIME	EXT_TIME	**Configurable extension time of start condition** Time unit: 1/4*BASE_CLOCK_PERIOD *Note: The max. value is {oxFF - SAMPLE_CNT_DIV}.*
0	EXT_EN	EXT_EN	**Used for standard mode only (baud rate is up to 100kHz)** This option decides to perform the extension of start /stop condition. If enabled, perform the extension; otherwise not. 0: Disable 1: Enable

11007030 FIFO_STAT FIFO Status Register 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RD_ADDR				WR_ADDR				FIFO_OFFSET						WR_FULL	RD_EMPTY
Type	RU				RU				RU						RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	1

Bit(s)	Mnemonic	Name	Description
15:12	**RD_ADDR**	RD_ADDR	**Current RD address pointer** Only bit [2:0] has physical meaning.
11:8	**WR_ADDR**	WR_ADDR	**Current WR address pointer** Only bit [2:0] has physical meaning.
7:4	**FIFO_OFFSET**	FIFO_OFFSET	**wr_addr[3:0] - rd_addr[3:0]**
1	**WR_FULL**	WR_FULL	**Indicates FIFO is full**
0	**RD_EMPTY**	RD_EMPTY	**Indicates FIFO is empty**

11007034 **FIFO_THRESH** **FIFO Thresh Register** **0700**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						TX_TRIG_THRESH								RX_TRIG_THRESH		
Type						RW								RW		
Reset						1	1	1						0	0	0

Overview: For debugging only. By default, these values do not need to be adjusted. Note that for RX, no time-out mechanism is implemented. Therefore, RX_trig_thresh must be left at 0, or there will be data left in FIFO that is not fetched by the DMA controller.

Bit(s)	Mnemonic	Name	Description
10:8	**TX_TRIG_THRESH**	TX_TRIG_THRESH	When Tx FIFO level is below this value, Tx DMA request is asserted.
2:0	**RX_TRIG_THRESH**	RX_TRIG_THRESH	When Rx FIFO level is above this value, Rx DMA request is asserted.

11007038 **FIFO_ADDR_CLR** **FIFO Address Clear Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FIFO_ADDR_CLR
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**FIFO_ADDR_CLR**	FIFO_ADDR_CLR	When written with 1'b1, a 1 pulse fifo_addr_clr is generated to clear the FIFO address to back to 0.

11007040 IO_CONFIG IO Config Register 0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													IDLE_OE_EN	IO_SYNC_EN	SDA_IO_CONFIG	SCL_IO_CONFIG
Type													RW	RW	RW	RW
Reset													0	0	1	1

Overview: This register is used to configure the I/O for the SDA and SCL lines to select between normal I/O mode, or open-drain mode to support wired-and bus.

Bit(s)	Mnemonic	Name	Description
3	**IDLE_OE_EN**	IDLE_OE_EN	0: Does not drive bus in idle state 1: Drive bus in idle state
2	**IO_SYNC_EN**	IO_SYNC_EN	**For debugging only** When set to 1, SCL and SDA inputs will be first dual synced by bclk_ck. This should not be needed. Only reserved for debugging.
1	**SDA_IO_CONFIG**	SDA_IO_CONFIG	0: Normal tristate I/O mode 1: Open-drain mode
0	**SCL_IO_CONFIG**	SCL_IO_CONFIG	0: Normal tristate I/O mode 1: Open-drain mode

11007044 MULTIMAS Multiple I2C Masters 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														BUS_DET_EN	CLK_SYNC_EN	ARB_EN
Type														RW	RW	RW
Reset														0	0	0

Overview: This registers contains options for supporting multi-master features.

Bit(s)	Mnemonic	Name	Description
2	**BUS_DET_EN**	BUS_DET_EN	When enabled, the bus status is monitored, and if the bus is currently busy, no new transaction can proceed.
1	**CLK_SYNC_EN**	CLK_SYNC_EN	When enabled, clk synchronization will be performed.
0	**ARB_EN**	ARB_EN	When enabled, multi-master arbitration will be performed.

11007048 HS High Speed Mode Register 0102

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		HS_SAMPLE_CNT_DIV				HS_STEP_CNT_DIV				MASTER_CODE					HS_NACKERR_DET_EN	HS_EN
Type		RW				RW				RW					RW	RW
Reset		0	0	0		0	0	1		0	0	0			1	0

Overview: This register contains options for supporting high speed operation features. Each HS half-pulse width, i.e. each high or low pulse, is equal to (step_cnt_div+1)*(sample_cnt_div+1)*1/4*BASE_CLOCK_PERIOD .

Bit(s)	Mnemonic	Name	Description
14:12	**HS_SAMPLE_CNT_DIV**	HS_SAMPLE_CNT_DIV	When the high-speed mode is entered after the master code transfer is completed, the sample width will become dependent on this parameter.
10:8	**HS_STEP_CNT_DIV**	HS_STEP_CNT_DIV	When the high-speed mode is entered after the master code transfer is completed, the number of samples per half pulse width will become dependent on this value.
6:4	**MASTER_CODE**	MASTER_CODE	This is the 3-bit programmable value for the master code to be transmitted.
1	**HS_NACKERR_DET_EN**	HS_NACKERR_DET_EN	**Enables NACKERR detection during the master code transmission** When enabled, if NACK is not received after the master code is transmitted, the transaction will be terminated with a STOP condition.
0	**HS_EN**	HS_EN	**Enables high-speed transaction** *Note: rs_stop must be set to 1.*

11007050 SOFTRESET Soft Reset Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SOFT_RESET
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**SOFT_RESET**	SOFT_RESET	When written with 1'b1, a 1 pulse soft reset is used as synchronous reset to reset the I2C internal hardware circuits.

11007054 **HW_DCM_EN** **HW DCM Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DCM_EN
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0	DCM_EN	DCM_EN	**Enables HW DCM function** Default is enable. 0: Disable 1: Enable

11007064 **DEBUGSTAT** **Debug Status Register** **0020**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BUS_BUSY	MASTER_WRITE	MASTER_READ	MASTER_STATE				
Type									RU	RU	RU	RU				
Reset									0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7	BUS_BUSY	BUS_BUSY	**For debugging only** Valid when bus_detect_en is 1. bus_busy = 1 indicates a start transaction has been detected and no stop condition has been detected yet.
6	MASTER_WRITE	MASTER_WRITE	**For debugging only** 1: Current transfer is in the master write dir
5	MASTER_READ	MASTER_READ	**For debugging only** 1: Current transfer is in the master read dir
4:0	MASTER_STATE	MASTER_STATE	**For debugging only. Reads back the current master_state.** 0: Idle state 1: I2C master is preparing sending out the start bit, SCL=1, SDA=1. 2: I2C master is sending out the start bit, SCL=1, SDA=0. 3: I2C master/slave is preparing transmitting data bit, SCL=0, DA=data bit (data bit can be changed when SCL=0). 4: I2C master/slave is transmitting data bit, SCL=1, SDA=data bit (data bit is stable when SCL=1). 5: I2C master/slave is preparing transmitting the ACK bit, SCL=0, SDA=ack (The ACK bit can be changed when SCL=0) 6: I2C master/slave is transmitting the ACK bit, SCL=1, SDA=0 (ack bit is stable when SCL=1) 7: I2C master is preparing sending out stop bit or repeated-start bit, SCL=0, SDA=0/1 (0: Stop bit; 1: Repeated-start bit).

Bit(s)	Mnemonic	Name	Description
			8: I2C master is sending out stop bit or repeated-start bit, SCL=1, SDA=1/0 (1: Stop bit; 0: Repeated-start bit). 9: I2C master is in delay start between two transfers, SCL=1, SDA=1. 10: I2C master is in FIFO wait state; For writing transaction, it means FIFO is empty and I2Cc master is waiting for DMA controller writing data into FIFO; For reading transaction, it means FIFOo is full and I2C master is waiting for DMA controller reading data from FIFO, SCL=0, SDA=don't care. 12: I2C master is preparing sending out data bit of master code. This state is used only in high-speed transaction, SCL=0, SDA=data bit of master code (data bit of master code can be changed when SCL=0). 13: I2C master is sending out data bit of master code. This state is used only in high-speed transaction, SCL=1, SDA=data bit of master code (data bit of master code is stable when SCL=1) 14: I2C master/slave is preparing transmitting the NACK bit, SCL=0, SDA=nack bit (The NACK bit can be changed when SCL=0). This state is used only in high-speed transaction. 15: I2C master/slave is transmitting the NACK bit, SCL=1, SDA=1; This state is used only in high-speed transaction. 16: I2C master is waiting for other master to release bus, SCL=1, SDA=0. 17: I2C master is waiting for the next restart of transfer during the multi-transfer, SCL=0, SDA=don't care.

11007068 DEBUGCTRL Debug Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															APB_DEBUG_RD	FIFO_APB_DEBUG
Type															WO	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	APB_DEBUG_RD	APB_DEBUG_RD	**Only valid when fifo_apb_debug is set to 1** Writing to this register will generate a 1 pulsed FIFO APB RD signal for reading the FIFO data.
0	FIFO_APB_DEBUG	FIFO_APB_DEBUG	**Used for trace 32 debugging purposes** When using trace 32, and the memory map is shown, turning this bit on will block the normal APB read access. The APB read access to the FIFO is then enabled by writing to apb_debug_rd. 0: Disable 1: Enable

Module name: I2C_SCCB_Controller base address : (+11007000h)

Address	Name	Width	Register Function
11007000	DATA_PORT	16	Data Port Register
11007004	SLAVE_ADDR	16	Slave Address Register
11007008	INTR_MASK	16	**Interrupt Mask Register** This register provides masks for the corresponding interrupt sources as indicated in the intr_stat register. 1 = Allow interrupt 0 = Disable interrupt *Note: While disabled, the corresponding interrupt will not be asserted. However the intr_stat will still be updated with the status, i.e. mask does not affect intr_stat register values.*
1100700C	INTR_STAT	16	**Interrupt Status Register** When an interrupt is issued by I2C controller, this register will need to be read by MCU to determine the cause for the interrupt. After this status has been read and appropriate actions are taken, the corresponding interrupt source will need to be written 1 to clear.
11007010	CONTROL	16	Control Register
11007014	TRANSFER_LEN	16	Transfer Length Register (Number of Bytes PerTransfer)
11007018	TRANSAC_LEN	16	Transaction Length Register (Number of Transfers per Transaction)
1100701C	DELAY_LEN	16	Inter Delay Length Register
11007020	TIMING	16	**Timing Control Register** LS/FS only. This register is used to control the output waveform timing. Each half pulse width, i.e. each high or low pulse, is equal to (step_cnt_div+1)*(sample_cnt_div+1)*1/4*BASE_CLOCK_PERIOD
11007024	START	16	Start Register
11007028	EXT_CONF	16	Extension Configuration Register
11007030	FIFO_STAT	16	FIFO Status Register
11007034	FIFO_THRESH	16	**FIFO Thresh Register** For debugging only. By default, these values do not need to be adjusted. *Note: For RX, no time-out mechanism is implemented. Therefore, RX_trig_thresh must be left at 0, or there will be data left in the FIFO that is not fetched by the DMA controller.*
11007038	FIFO_ADDR_CLR	16	FIFO Address Clear Register
11007040	IO_CONFIG	16	**IO Config Register**

Address	Name	Width	Register Function
			This register is used to configure the I/O for the SDA and SCL lines to select between normal I/O mode, or open-drain mode to support wired-and bus.
11007044	**MULTIMAS**	16	**Multiple I2C Masters** This registers contains options for supporting multi-master features.
11007048	**HS**	16	**High Speed Mode Register** This register contains options for supporting high speed operation features. Each HS half pulse width, i.e. each high or low pulse, is equal to (hs_step_cnt_div+1)*(hs_sample_cnt_div+1)*1/4 *BASE_CLOCK_PERIOD
11007050	**SOFTRESET**	16	Soft Reset Register
11007054	**HW_DCM_EN**	16	HW DCM Enable
11007064	**DEBUGSTAT**	16	Debug Status Register
11007068	**DEBUGCTRL**	16	Debug Control Register

11007000 DATA_PORT Data Port Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA_PORT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DATA_PORT**	DATA_PORT	**FIFO access port** During master write sequences (slave_addr[0] = 0), this port can be written by APB, and during master read sequences (slave_addr[0] = 1), this port can be read by APB. *Note: Slave_addr must be set correctly before accessing FIFO.* For debugging only: If the fifo_apb_debug bit is set, FIFO can be read and written by the APB.

11007004 SLAVE_ADDR Slave Address Register 00BF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SLAVE_ADDR							
Type									RW							
Reset									1	0	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
7:0	**SLAVE_ADDR**	SLAVE_ADDR	**Specifies the slave address of the device to be accessed** Bit 0 is defined by the I2C protocol as a bit that indicates the direction of transfer.

Bit(s)	Mnemonic	Name	Description
			0: Master writer 1: Master read

11007008 INTR_MASK Interrupt Mask Register 00FF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SPARE				MASK_ARB_LOST	MASK_HS_NACKERR	MASK_ACKERR	MASK_TRANSAC_COMP
Type									RW				RW	RW	RW	RW
Reset									1	1	1	1	1	1	1	1

Overview: This register provides masks for the corresponding interrupt sources as indicated in intr_stat register. 1 = allow interrupt; 0 = disable interrupt Note that while disabled, the corresponding interrupt will not be asserted. However, intr_stat will still be updated with the status, i.e. mask does not affect intr_stat register values.

Bit(s)	Mnemonic	Name	Description
7:4	**SPARE**	SPARE	Reserved
3	**MASK_ARB_LOST**	MASK_ARB_LOST	Setting this value to 0 will mask ARB_LOST interrupt signal.
2	**MASK_HS_NACKERR**	MASK_HS_NACKERR	Setting this value to 0 will mask HS_NACKERR interrupt signal.
1	**MASK_ACKERR**	MASK_ACKERR	Setting this value to 0 will mask ACK_ERR interrupt signal.
0	**MASK_TRANSAC_COMP**	MASK_TRANSAC_COMP	Setting this value to 0 will mask TRANSAC_COMP interrupt signal.

1100700C INTR_STAT Interrupt Status Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													ARB_LOST	HS_NACKERR	ACKERR	TRANSAC_COMP
Type													W1C	W1C	W1C	W1C
Reset													0	0	0	0

Overview: When an interrupt is issued by the I2C controller, this register will need to be read by MCU to determine the cause for the interrupt. After this status has been read and appropriate actions are taken, the corresponding interrupt source will need to be written 1 to clear.

Bit(s)	Mnemonic	Name	Description
3	**ARB_LOST**	ARB_LOST	This status is asserted if the I2C controller loses arbitration.
2	**HS_NACKERR**	HS_NACKERR	This status is asserted if HS master code NACK error detection is enabled. If enabled, HS master code NACK err will cause transaction to end and stop will be issued.
1	**ACKERR**	ACKERR	This status is asserted if ACK error detection is enabled. If enabled, ACKERR will cause transaction to end and stop will be issued.
0	**TRANSAC_COMP**	TRANSAC_COMP	This status is asserted when a transaction is completed successfully.

11007010 CONTROL Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**TRANSFER_LEN_CHANGE**	**ACKERR_DET_EN**	**DIR_CHANGE**	**CLK_EXT_EN**	**DMA_EN**	**RS_STOP**	
Type										RW	RW	RW	RW	RW	RW	
Reset										0	0	0	0	0	0	

Bit(s)	Mnemonic	Name	Description
6	**TRANSFER_LEN_CHANGE**	TRANSFER_LEN_CHANGE	**Specifies whether or not to change the transfer length after the fist transfer is completed** If enabled, the transfers after the first transfer will use the transfer_len_aux parameter.
5	**ACKERR_DET_EN**	ACKERR_DET_EN	**Enables slave ACK error detection** When enabled, if slave ACK error is detected, the master shall terminate the transaction by issuing a STOP condition and then asserts the ACKERR interrupt. MCU handles this case appropriately and then resets the FIFO address before reissuing transaction. If this option is disabled, the controller will ignore slave ACK error and keep on scheduled transaction. 0: Disable 1: Enable
4	**DIR_CHANGE**	DIR_CHANGE	**Combined transfer format, where the direction of transfer is to be changed from write to read after the FIRST RS condition** *Note: When set to 1, the transfers after the direction change will be based on the transfer_len_aux parameter.* 0: Disable 1: Enable
3	**CLK_EXT_EN**	CLK_EXT_EN	**I2C spec allows slaves to hold the SCL line low if it is not yet ready for further processing.** Therefore, if this bit is set to 1, the master controller will enter a high wait state until the slave releases the SCL line.
2	**DMA_EN**	DMA_EN	**By default, this is disabled, and the FIFO data shall be manually prepared by MCU.**

Bit(s)	Mnemonic	Name	Description
			This default setting should be used for transfer sizes of smaller than 8 data bytes and no multiple transfer is configured. When enabled, DMA requests are turned on, and the FIFO data should be prepared in memory.
1	**RS_STOP**	RS_STOP	**In LS/FS mode, this bit affects multi-transfer transaction only.** It controls whether or not the REPEATED-START condition is used between transfers. The last ending transfer always ends with a STOP. In HS mode, this bit must be set to 1. 0: Use STOP 1: Use REPEATED-START

11007014 **TRANSFER_LEN** **Transfer Length Register (Number of Bytes per Transfer)** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
15:0	**TRANSFER_LEN**	TRANSFER_LEN	**Indicates the number of data bytes to be transferred in 1 transfer unit (excluding slave address byte)** *Note: The value must be set to be bigger than 1; otherwise no transfer will take place.*

11007018 **TRANSAC_LEN** **Transaction Length Register (Number of Transfers per Transaction)** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TRANSAC_LEN							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
7:0	**TRANSAC_LEN**	TRANSAC_LEN	**Indicates the number of transfers to be transferred in 1 transaction** *Note: The value must be set to be bigger than 1; otherwise no transfer will take place.*

1100701C **DELAY_LEN** **Inter Delay Length Register** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

1100701C DELAY_LEN Inter Delay Length Register 0002

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DELAY_LEN							
Type									RW							
Reset									0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
7:0	**DELAY_LEN**	DELAY_LEN	**Sets up wait delay between consecutive transfers when RS_STOP bit is set to 0** Unit: Half the pulse width)

11007020 TIMING Timing Control Register 1303

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_READ_ADJ	DATA_READ_TIME				SAMPLE_CNT_DIV					STEP_CNT_DIV					
Type	RW	RW				RW					RW					
Reset	0	0	0	1		0	1	1			0	0	0	0	1	1

Overview: LS/FS only. This register is used to control the output waveform timing. Each half pulse width, i.e. each high or low pulse, is equal to (step_cnt_div+1)*(sample_cnt_div+1)*1/4*BASE_CLOCK_PERIOD.

Bit(s)	Mnemonic	Name	Description
15	**DATA_READ_ADJ**	DATA_READ_ADJ	When set to 1, data latch in sampling time during master reads are adjusted according to the DATA_READ_TIME value. Otherwise, by default, the data are latched in at half of the high pulse width point. This value must be set to be smaller than or equal to half the high pulse width.
14:12	**DATA_READ_TIME**	DATA_READ_TIME	This value is valid only when DATA_READ_ADJ is set to 1. This can be used to adjust so that the data are latched in at earlier sampling points (assuming data are settled by then)
10:8	**SAMPLE_CNT_DIV**	SAMPLE_CNT_DIV	Used for LS/FS only. This adjusts the width of each sample. (sample width = sample_cnt_div*1/4 BASE_CLOCK_PERIOD)
5:0	**STEP_CNT_DIV**	STEP_CNT_DIV	Specifies the number of samples per half pulse width, i.e. each high or low pulse

11007024 START Start Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RS_MUL_CNFG	RS_MUL_TRIG	RS_MUL_CLR													START
Type	RW	RW	RO													RW
Reset	0	0	0													0

Bit(s)	Mnemonic	Name	Description
15	**RS_MUL_CNFG**	RS_MUL_CNFG	**Configuration of re-start multi-transfer**
14	**RS_MUL_TRIG**	RS_MUL_TRIG	**Start bit of re-start multi-transfer**
13	**RS_MUL_CLR**	RS_MUL_CLR	**Clear bit of re-start multi-transfer**
0	**START**	START	**Starts the transaction on the bus** It is auto de-asserted at the end of the transaction.

11007028 EXT_CONF Extension Configuration Register 1800

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_TIME															EXT_EN
Type	RW															RW
Reset	0	0	0	1	1	0	0	0								0

Bit(s)	Mnemonic	Name	Description
15:8	**EXT_TIME**	EXT_TIME	**Configurable extension time of start condition** Time unit: 1/4 BASE_CLOCK_PERIOD *Note: The max. value is {0xFF - SAMPLE_CNT_DIV}.*
0	**EXT_EN**	EXT_EN	**Used for standard mode only (baud rate is up to 100kHz)** This option decides to perform the extension of start /stop condition. If enabled, perform the extension; otherwise not. 0: Disable 1: Enable

11007030 FIFO_STAT FIFO Status Register 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RD_ADDR				WR_ADDR				FIFO_OFFSET						WR_FULL	RD_EMPTY
Type	RU				RU				RU						RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	1

Bit(s)	Mnemonic	Name	Description
15:12	**RD_ADDR**	RD_ADDR	**Current RD address pointer** Only bit [2:0] has physical meaning.
11:8	**WR_ADDR**	WR_ADDR	**Current WR address pointer** Only bit [2:0] has physical meaning.

Bit(s)	Mnemonic	Name	Description
7:4	**FIFO_OFFSET**	FIFO_OFFSET	**wr_addr[3:0] - rd_addr[3:0]**
1	**WR_FULL**	WR_FULL	**Indicates FIFO is full**
0	**RD_EMPTY**	RD_EMPTY	**Indicates FIFO is empty**

11007034 FIFO_THRESH FIFO Thresh Register 0700

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						TX_TRIG_THRESH								RX_TRIG_THRESH		
Type						RW								RW		
Reset						1	1	1						0	0	0

Overview: For debugging only. By default, these values do not need to be adjusted. Note that for RX, no time-out mechanism is implemented. Therefore, RX_trig_thresh must be left at 0, or there will be data left in FIFO that is not fetched by the DMA controller.

Bit(s)	Mnemonic	Name	Description
10:8	**TX_TRIG_THRESH**	TX_TRIG_THRESH	When Tx FIFO level is below this value, Tx DMA request is asserted.
2:0	**RX_TRIG_THRESH**	RX_TRIG_THRESH	When Rx FIFO level is above this value, Rx DMA request is asserted.

11007038 FIFO_ADDR_CLR FIFO Address Clear Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FIFO_ADDR_CLR
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**FIFO_ADDR_CLR**	FIFO_ADDR_CLR	When written with 1'b1, a 1 pulse fifo_addr_clr is generated to clear the FIFO address to back to 0.

11007040 IO_CONFIG IO Config Register 0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

11007040 IO_CONFIG IO Config Register 0003

Name													IDLE_OE_EN	IO_SYNC_EN	SDA_IO_CONFIG	SCL_IO_CONFIG
Type													RW	RW	RW	RW
Reset													0	0	1	1

Overview: This register is used to configure the I/O for the SDA and SCL lines to select between normal I/O mode, or open-drain mode to support wired-and bus.

Bit(s)	Mnemonic	Name	Description
3	**IDLE_OE_EN**	IDLE_OE_EN	0: Does not drive bus in idle state 1: Drive bus in idle state
2	**IO_SYNC_EN**	IO_SYNC_EN	**For debugging only** When set to 1, SCL and SDA inputs will be first dual synced by bclk_ck. This should not be needed. Only reserved for debugging.
1	**SDA_IO_CONFIG**	SDA_IO_CONFIG	0: Normal tristate I/O mode 1: Open-drain mode
0	**SCL_IO_CONFIG**	SCL_IO_CONFIG	0: Normal tristate I/O mode 1: Open-drain mode

11007044 MULTIMAS Multiple I2C Masters 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														BUS_DET_EN	CLK_SYNC_EN	ARB_EN
Type														RW	RW	RW
Reset														0	0	0

Overview: This registers contains options for supporting multi-master features.

Bit(s)	Mnemonic	Name	Description
2	**BUS_DET_EN**	BUS_DET_EN	When enabled, bus status is monitored and if bus is currently busy, no new transaction can proceed.
1	**CLK_SYNC_EN**	CLK_SYNC_EN	When enabled, clk synchronization will be performed.
0	**ARB_EN**	ARB_EN	When enabled, multi-master arbitration will be performed.

11007048 HS High Speed Mode Register 0102

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		HS_SAMPLE_CNT_DIV				HS_STEP_CNT_DIV				MASTER_CODE					HS_NACKERR_D	HS_EN

11007048 HS High Speed Mode Register 0102

															ET_EN	
Type		RW				RW				RW					RW	RW
Reset		0	0	0		0	0	1		0	0	0			1	0

Overview: This register contains options for supporting high speed operation features Each HS half pulse width, i.e. each high or low pulse, is equal to (step_cnt_div+1)*(sample_cnt_div+1)*1/4*BASE_CLOCK_PERIOD.

Bit(s)	Mnemonic	Name	Description
14:12	**HS_SAMPLE_CNT_DIV**	HS_SAMPLE_CNT_DIV	When the high-speed mode is entered after the master code transfer is completed, the sample width will become dependent on this parameter.
10:8	**HS_STEP_CNT_DIV**	HS_STEP_CNT_DIV	When the high-speed mode is entered after the master code transfer is completed, the number of samples per half pulse width will become dependent on this value.
6:4	**MASTER_CODE**	MASTER_CODE	This is the 3-bit programmable value for the master code to be transmitted.
1	**HS_NACKERR_DET_EN**	HS_NACKERR_DET_EN	**Enables NACKERR detection during the master code transmission** When enabled, if NACK is not received after master code is transmitted, the transaction will be terminated with a STOP condition.
0	**HS_EN**	HS_EN	**Enables high-speed transaction** *Note: rs_stop must be set to 1.*

11007050 SOFTRESET Soft Reset Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SOFT_RESET
Type																WO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**SOFT_RESET**	SOFT_RESET	When written with 1'b1, a 1 pulse soft reset is used as synchronous reset to reset the I2C internal hardware circuits.

11007054 HW_DCM_EN HW DCM Enable 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DCM_EN
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0	**DCM_EN**	DCM_EN	**Enables HW DCM function** Default is enable. 0: Disable 1: Enable

11007064 DEBUGSTAT Debug Status Register 0020

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BUS_BUSY	MASTER_WRITE	MASTER_READ	MASTER_STATE				
Type									RU	RU	RU	RU				
Reset									0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7	**BUS_BUSY**	BUS_BUSY	**For debugging only** Valid when bus_detect_en is 1. bus_busy = 1 indicates a start transaction has been detected and no stop condition has been detected yet.
6	**MASTER_WRITE**	MASTER_WRITE	**For debugging only** 1: Current transfer is in the master write dir.
5	**MASTER_READ**	MASTER_READ	**For debugging only** 1: Current transfer is in the master read dir.
4:0	**MASTER_STATE**	MASTER_STATE	**For debugging only: Reads back the current master_state.** 0: Idle state 1: I2C master is preparing sending out the start bit, SCL=1, SDA=1. 2: I2C master is sending out the start bit, SCL=1, SDA=0. 3: I2C master/slave is preparing transmitting data bit, SCL=0, SDA=data bit (data bit can be changed when SCL=0). 4: I2C master/slave is transmitting data bit, SCL=1, SDA=data bit (data bit is stable when SCL=1). 5: I2C master/slave is preparing transmitting the ACK bit, SCL=0, SDA=ack (The ACK bit can be changed when SCL=0). 6: I2C master/slave is transmitting the ACK bit, SCL=1, SDA=0 (ack bit is stable when SCL=1). 7: I2C master is preparing sending out stop bit or repeated-start bit, SCL=0, SDA=0/1 (0: Stop bit; 1: Repeated-start bit). 8: I2C master is sending out stop bit or repeated-start bit, SCL=1, SDA=1/0 (1: Stop bit; 0: Repeated-start bit). 9: I2C master is in delay start between two transfers, SCL=1, SDA=1. 10: I2C master is in FIFO wait state; For writing transaction, it means FIFO is empty and I2C master is waiting for DMA controller writing data into FIFO; For reading transaction, it means FIFO is full and I2C master is waiting for DMA controller reading data from FIFO, SCL=0, SDA=don't care.

Bit(s)	Mnemonic	Name	Description
			12: I2C master is preparing sending out data bit of master code. This state is used only in high-speed transaction, SCL=0, SDA=data bit of master code (data bit of master code can be changed when SCL=0). 13: I2C master is sending out data bit of master code. This state is used only in high-speed transaction, SCL=1, SDA=data bit of master code (data bit of master code is stable when SCL=1). 14: I2C master/slave is preparing transmitting the NACK bit, SCL=0, SDA=nack bit (The NACK bit can be changed when SCL=0); This state is used only in high-speed transaction. 15: I2C master/slave is transmitting the NACK bit, SCL=1, SDA=1; This state is used only in high-speed transaction. 16: I2C master is waiting for other master to release bus, SCL=1, SDA=0. 17: I2C master is waiting for the next restart of transfer during the multi-transfer, SCL=0, SDA=don't care.

11007068 DEBUGCTRL Debug Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															APB_DEBUG_RD	FIFO_APB_DEBUG
Type															WO	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	APB_DEBUG_RD	APB_DEBUG_RD	**Only valid when fifo_apb_debug is set to 1** Writing to this register will generate a 1 pulsed FIFO APB RD signal for reading the FIFO data.
0	FIFO_APB_DEBUG	FIFO_APB_DEBUG	**Used for trace 32 debug purposes** When using trace 32, and the memory map is shown, turning this bit on will block the normal APB read access. The APB read access to the FIFO will then be enabled by writing to apb_debug_rd. 0: Disable 1: Enable

1100706C TRANSFER_LEN_AUX Transfer Length Register (Number of Bytes per Transfer) 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN_AUX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description

15:0	**TRANSFER_LEN_AUX**	TRANSFER_LEN_AUX	**This field is valid only when dir_change is set to 1.** Indicates the number of data bytes to be transferred in 1 transfer unit (excluding slave address byte) for the transfers following the direction change. That is, if dir_change =1, then the first write transfer length will depend on transfer_len, while the second read transfer length depend on transfer_len_aux. Dir change is always after the first transfer. *Note: The value must be set to be bigger than 1; otherwise no transfer will take place.*

1.17 I2C/SCCB Controller (I2C 1)

1.17.1 Introduction

I2C (Inter-IC)/SCCB (Serial Camera Control Bus) is a two-wire serial interface. The two signals are SCL and SDA. SCL is a clock signal that is driven by the master. SDA is a bi-directional data signal that can be driven by either the master or the slave. This generic controller supports the master role and conforms to the I2C specification.

1.17.2 Features

- I2C compliant master mode operation
- Adjustable clock speed for LS/FS mode operation
- Supports 7-bit/10-bit addressing
- Supports high-speed mode
- Supports slave clock extension
- START/STOP/REPEATED START condition
- Manual transfer mode
- Multi-write per transfer
- Multi-read per transfer
- Multi-transfer per transaction
- Combined format transfer with length change capability.-
- Active drive/wired-and I/O configuration

1.17.3 Block Diagram

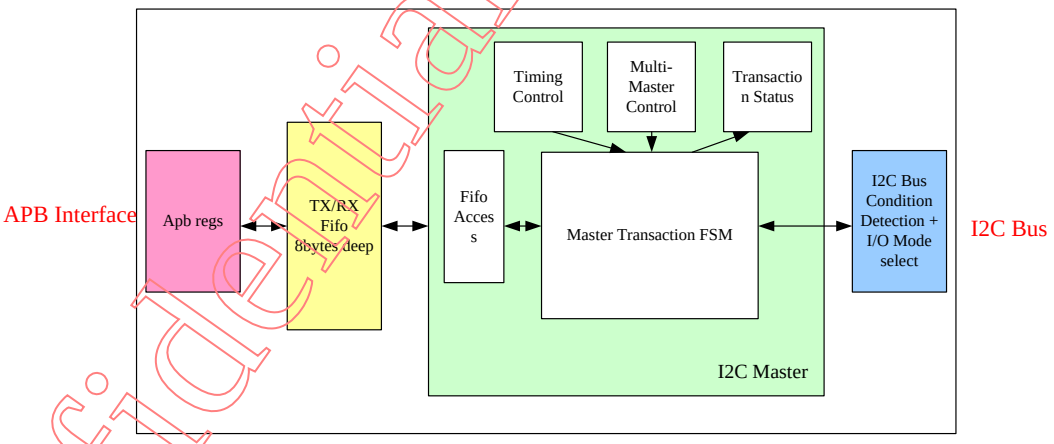


Figure 1-11. Block diagram of I2C

1.17.4 Register Definition

Module name: i2c1 Base address: (+11008000h)

Address	Name	Width	Register Function
11008000	DATA_PORT	16	Data Port Register

Address	Name	Width	Register Function
11008004	SLAVE_ADDR	16	Slave Address Register
11008008	INTR_MASK	16	Interrupt Mask Register
1100800C	INTR_STAT	16	Interrupt Status Register
11008010	CONTROL	16	Control Register
11008018	TRANSAC_LEN	16	Transaction Length Register (Number of Transfers per Transaction)
1100801C	DELAY_LEN	16	Inter Delay Length Register
11008020	TIMING	16	Timing Control Register LS/FS only. This register is used to control the output waveform timing.
11008024	START	16	Start Register
11008028	EXT_CONF	16	Extension Configuration Register
11008030	FIFO_STAT	16	FIFO Status Register
11008034	FIFO_THRESH	16	FIFO Thresh Register (DEBUG ONLY) By default, these values do not need to be adjusted. Note! for RX, no timeout mechanism is implemented. Therefore, RX_trig_thresh must be left at 0, or there would be data left in the fifo that is not fetched by DMA controller.
11008038	FIFO_ADDR_CLR	16	FIFO Address Clear Register
11008040	IO_CONFIG	16	IO Config Register This register is used to configure the I/O for the sda and scl lines to select between normal i/o mode, or open-drain mode to support wired-and bus.
11008044	DEBUG	16	RESERVED DEBUG Register NOTE: This register is for DEBUG ONLY. The bits are R/W, do not change the values from the default value.
11008048	HS	16	High Speed Mode Register This register contains options for supporting high speed operation features
11008050	SOFTRESET	16	Soft Reset Register
11008054	I2C0_I2CREG_HW_CG_EN	16	HW DCM Enable
11008064	DEBUGSTAT	16	Debug Status Register
11008068	DEBUGCTRL	16	Debug Control Register
1100806C	TRANSFER_LEN_AUX	16	Transfer Length Register (Number of Bytes per Transfer)

11008000 DATA_PORT Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**DATA_PORT**							
Type									RW							

Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DATA_PORT	**This is the FIFO access port. During master write sequences (slave_addr[0] = 0), this port can be written by APB, and during master read sequences (slave_addr[0] = 1), this port can be read by APB.** (NOTE) Slave_addr must be set correctly before accessing the fifo. (DEBUG ONLY) If the fifo_apb_debug bit is set, then the FIFO can be read and write by the APB

11008004 SLAVE_ADDR Slave Address Register 000000BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SLAVE_ADDR**							
Type									RW							
Reset									1	0	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SLAVE_ADDR	**This specifies the slave address of the device to be accessed. Bit 0 is defined by the I2C protocol as a bit that indicates the direction of transfer. 1 = master read, 0 = master write.**

11008008 INTR_MASK Interrupt Mask Register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SPARE**				**MAS_ARB_LOST**	**MAS_HS_NACKER**	**MAS_ACKERR**	**MAS_TRANSAC_COMP**
Type									RW				RW	RW	RW	RW
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:4	SPARE	**Reserved**
3	MAS_ARB_LOST	**Setting this value to 0 will mask ARB_LOST interrupt signal.**
2	MAS_HS_NACKER	**Setting this value to 0 will mask HS_NACKERR interrupt signal.**
1	MAS_ACKERR	**Setting this value to 0 will mask ACK_ERR interrupt signal.**
0	MAS_TRANSAC_COMP	**Setting this value to 0 will mask TRANSAC_COMP interrupt signal.**

Bit(s)	Name	Description

1100800C INTR_STAT Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RS_MULTIPLE	ARB_LOST	HS_NACKERR	ACKERR	TRANSAC_COMP
Type												W1C	W1C	W1C	W1C	W1C
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	RS_MULTIPLE	
3	ARB_LOST	**This status is asserted if the I2C controller loses arbition.**
2	HS_NACKERR	**This status is asserted if hs master code nack error detection is enabled. If enabled, hs master code nack err will cause transaction to end and stop will be issued.**
1	ACKERR	**This status is asserted if ACK error detection is enabled. If enabled, ackerr will cause transaction to end and stop will be issued.**
0	TRANSAC_COMP	**This status is asserted when a transaction has completed successfully.**

11008010 CONTROL Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TRANSFER_LEN_CHANGE	ACKERR_DET_EN	DIR_CHANGE	CLK_EXT_EN	DMA_EN	RS_STOP	
Type										RW	RW	RW	RW	RW	RW	
Reset										0	0	0	0	0	0	

Bit(s)	Name	Description
6	TRANSFER_LEN_CHANGE	**This options specifies whether or not to change the transfer length after the fist transfer completes. If enabled, the transfers after the first transfer will use the transfer_len_aux parameter.**
5	ACKERR_DET_EN	**This option enables slave ack error detection. When enabled, if slave ack error is detected, the master shall terminate the transaction by issuing a STOP condition and then asserts ackerr interrupt. Mcu shall handle this case appropriately and then resets the fifo address before reissuing transaction again. If this option is disabled, the**

Bit(s)	Name	Description
		controller will ignore slave ack error and keep on scheduled transaction. 0: disable 1: enable
4	DIR_CHANGE	**This option is used for combined transfer format, where the direction of transfer is to be changed from write to read after the FIRST RS condition. Note: when set to 1, the transfers after the direction change will be based on the transfer_len_aux parameter.** 0: disable 1: enable
3	CLK_EXT_EN	**I2C spec allows slaves to hold the SCL line low if it is not yet ready for further processing. Therefore, if this bit is set to 1, master controller will enter a high wait state until the slave releases the SCL line.**
2	DMA_EN	**By default, this is disabled, and fifo data shall be manually prepared by mcu. This default setting should be used for transfer sizes of less than 8 data bytes and no multiple transfer is configured. When enabled, dma requests are turned on, and the fifo data should be prepared in memory.**
1	RS_STOP	**In LS/FS mode, this bit affects multi-transfer transaction only. It controls whether or not REPEATED-START condition is used between transfers. The last ending transfer always ends with a STOP.** In HS mode, this bit must be set to 1. 0: use STOP 1: use REPEATED-START

11008018 TRANSAC_LEN Transaction Length Register (Number of Transfers per Transaction) 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TRANSFER_LEN							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:0	TRANSFER_LEN	**This indicates the number of TRANSFERS to be transferred in 1 transaction** (NOTE) The value must be set greater than 1, otherwise no transfer will take place.

1100801C DELAY_LEN Inter Delay Length Register 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DELAY_LEN							
Type									RW							
Reset									0	0	0	0	0	0	1	0

Bit(s)	Name	Description
7:0	DELAY_LEN	This sets the wait delay between consecutive transfers when RS_STOP bit is set to 0. (the unit is same as the half pulse width)

11008020 TIMING Timing Control Register 00001303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_READ_ADJ	DATA_READ_TIME				SAMPLE_CNT_DIV					STEP_CNT_DIV					
Type	RW	RW				RW					RW					
Reset	0	0	0	1		0	1	1			0	0	0	0	1	1

Bit(s)	Name	Description
15	DATA_READ_ADJ	When set to 1, data latch in sampling time during master reads are adjusted according to DATA_READ_TIME value. Otherwise, by default, data is latched in at half of the high pulse width point. This value must be set to less or equal to half the high pulse width.
14:12	DATA_READ_TIME	This value is valid only when DATA_READ_ADJ is set to 1. This can be used to adjust so that data is latched in at earlier sampling points (assuming data is settled by then)
10:8	SAMPLE_CNT_DIV	Used for LS/FS only. This adjusts the width of each sample. (sample width = sample_cnt_div * 1/13Mhz)
5:0	STEP_CNT_DIV	This specifies the number of samples per half pulse width (ie. each high or low pulse)

11008024 START Start Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RS_STOP_MULTIPLE_CONFIG	RS_STOP_MULTIPLE_TRIG	RS_STOP_MULTIPLE_TRIG_CLR													START
Type	RW	RW	RO													RW
Reset	0	0	0													0

Bit(s)	Name	Description
15	RS_STOP_MULTIPLE_CONFIG	**Enable multiple r/w & length & slave address with rs_stop transfer**
14	RS_STOP_MULTIPLE_TRIG	**Trigger next transfer when enable multiple r/w & length & slave address with rs_stop transfer**
13	RS_STOP_MULTIPLE_TRIG_CLR	**Clear the rs_stop_mul_trig for** next transfer
0	START	**This register starts the transaction on the bus. It is auto deasserted at the end of the transaction.**

11008028 EXT_CONF Extension Configuration Register 00001800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_TIME															EXT_EN
Type	RW															RW
Reset	0	0	0	1	1	0	0	0								0

Bit(s)	Name	Description
15:8	EXT_TIME	**Configurable extension time of start condition.** Time unit: 1/4*BASE_CLOCK_PERIOD Note: The max. value is {0xFF-SAMPLE_CNT_DIV}.
0	EXT_EN	**Used for standard mode only (baud rate is up to 100kHz).** This option decides to perform the extension of start/stop condion.If enbale, perform the extension; otherse not. 0: Disable 1: Enable

11008030 FIFO_STAT FIFO Status Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RD_ADDR				WR_ADDR				FIFO_OFFSET						WR_FULL	RD_EMPTY
Type	RO				RO				RO						RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	1

Bit(s)	Name	Description
15:12	RD_ADDR	**The current rd address pointer. (only bit [2:0] has physical meaning)**
11:8	WR_ADDR	**The current wr address pointer. (only bit [2:0] has physical meaning)**
7:4	FIFO_OFFSET	**wr_addr[3:0] - rd_addr[3:0]**
1	WR_FULL	**This indicates that the fifo is full.**

Bit(s)	Name	Description
0	RD_EMPTY	**This indicates that the fifo is empty.**

11008034 FIFO_THRESH FIFO Thresh Register 00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						TX_TRIG_THRESH								RX_TRIG_THRESH		
Type						RW								RW		
Reset						1	1	1						0	0	0

Bit(s)	Name	Description
10:8	TX_TRIG_THRESH	**When tx fifo level is below this value, tx dma request is asserted.**
2:0	RX_TRIG_THRESH	**When rx fifo level is above this value, rx dma request is asserted.**

11008038 FIFO_ADDR_CLR FIFO Address Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FIFO_ADDR_CLR
Type																WO
Reset																0

Bit(s)	Name	Description
0	FIFO_ADDR_CLR	**When written with a 1, a 1 pulse fifo_addr_clr is generated to clear the fifo address to back to 0.**

11008040 IO_CONFIG IO Config Register 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													IDLE_OE_EN	IO_SYNC_EN	SDA_IO_CONFIG	SCL_IO_CONFIG
Type													RW	RW	RW	RW

Reset													0	0	1	1

Bit(s)	Name	Description
3	IDLE_OE_EN	0: do not drive bus in idle state 1: drive bus in idle state
2	IO_SYNC_EN	**DEBUG ONLY: When set to 1, scl and sda inputs will be first dual synced by bclk_ck. This should not be needed. Only reserved for debugging.**
1	SDA_IO_CONFIG	0: normal tristate io mode 1: open-drain mode
0	SCL_IO_CONFIG	0: normal tristate io mode 1: open-drain mode

11008044 DEBUG RESERVED DEBUG Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**DEBUG**		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	DEBUG	

11008048 HS High Speed Mode Register 00000102

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**HS_SAMPLE_CNT_DIV**				**HS_STEP_CNT_DIV**				**MASTER_CODE**					**HS_NACKERR_DET_EN**	**HS_EN**
Type		RW				RW				RW					RW	RW
Reset		0	0	0		0	0	1		0	0	0			1	0

Bit(s)	Name	Description
14:12	HS_SAMPLE_CNT_DIV	**When high speed mode is entered after the master code transfer has been completed, the sample width becomes dependent on this parameter.**
10:8	HS_STEP_CNT_DIV	**When high speed mode is entered after the master code transfer has been completed, the number of samples per half pulse width becomes dependent on this value.**
6:4	MASTER_CODE	**This is the 3 bit programmable value for the master code to be transmitted.**

Bit(s)	Name	Description
1	HS_NACKERR_DET_EN	**This enables NACKERR detection during the master code transmission. When enabled, if NACK is not received after master code has been transmitted, the transaction will terminated with a STOP condition.**
0	HS_EN	**This enables the high speed transaction. (note: rs_stop must be set to 1 as well)**

11008050 SOFTRESET Soft Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SOFT_RESET
Type																WO
Reset																0

Bit(s)	Name	Description
0	SOFT_RESET	**When written with a 1, a 1 pulse soft reset is used as synchronous reset to reset the I2C internal hardware circuits.**

11008054 I2C0_I2CREG_HW_CG_EN HW DCM Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DCM_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	DCM_EN	**Enable HW DCM function.** Default is disable. 0: Disable 1: Enable

11008064 DEBUGSTAT Debug Status Register 00000020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BUS_BUSY	MASTER_WRITE	MASTER_READ	MASTER_STATE				
Type									RU	RU	RU	RU				
Reset									0	0	1	0	0	0	0	0

Bit(s)	Name	Description
7	BUS_BUSY	**DEBUG ONLY: valid when bus_detect_en is 1. bus_busy = 1 indicates a start transaction has been detected and no stop condition has been detected yet.**
6	MASTER_WRITE	**DEBUG ONLY: 1 = current transfer is in the master write dir**
5	MASTER_READ	**DEBUG ONLY: 1 = current transfer is in the master read dir**
4:0	MASTER_STATE	**DEBUG ONLY: reads back the current master_state.** 0: idle state; 1: i2c master is preparing sending out the start bit, SCL=1, SDA=1; 2: i2c master is sending out the start bit, SCL=1, SDA=0; 3: i2c master/slave is preparing transmitting data bit, SCL=0, SDA=data bit (data bit can be changed when SCL=0); 4: i2c master/slave is transmitting data bit, SCL=1, SDA=data bit (data bit is stable when SCL=1); 5: i2c master/slave is preparing transmitting ack bit, SCL=0, SDA=ack (ack bit can be changed when SCL=0); 6: i2c master/slave is transmitting ack bit, SCL=1, SDA=0 (ack bit is stable when SCL=1); 7: i2c master is preparing sending out stop bit or repeated-start bit, SCL=0, SDA=0/1 (0: means stop bit; 1: means repeated-start bit); 8: i2c master is sending out stop bit or repeated-start bit, SCL=1, SDA=1/0 (1: means stop bit; 0: means repeated-start bit); 9: i2c master is in delay start between two transfers, SCL=1, SDA=1; 10: i2c master is in fifo wait state; For writing transaction, it means fifo is empty and i2c master is waiting for dma controller writing data into fifo; For reading transaction, it means fifo is full and i2c master is waiting for dma controller reading data from fifo, SCL=0, SDA=do not care; 12: i2c master is preparing sending out data bit of master code. This state is used only in high-speed transaction, SCL=0, SDA=data bit of master code (data bit of master code can be changed when SCL=0); 13: i2c master is sending out data bit of master code. This state is used only in high-speed transaction, SCL=1, SDA=data bit of master code (data bit of master code is stable when SCL=1); 14: i2c master/slave is preparing transmitting nack bit, SCL=0, SDA=nack bit (nack bit can be changed when SCL=0); This state is used only in high-speed transaction; 15: i2c master/slave is transmitting nack bit, SCL=1, SDA=1; This state is used only in high-speed transaction;

11008068 DEBUGCTRL Debug Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															APB_DEBUG_RD	FIFO_APB_DEBUG
Type															WO	RW
Reset															0	0

Bit(s)	Name	Description
1	APB_DEBUG_RD	**This bit is only valid when fifo_apb_debug is set to 1. Writing to this register will generate a 1 pulsed fifo apb rd signal for reading the fifo data.**
0	FIFO_APB_DEBUG	**This is used for trace32 debug purposes. When using trace32, and the memory map is shown, turning this bit on will block the normal apb read access. Apb read access to the fifo is then enabled by writing to apb_debug_rd.** 0: disable 1: enable

1100806C TRANSFER_LEN_AUX Transfer Length Register (Number of Bytes per Transfer) 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TRANSFER_LEN_AUX**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	TRANSFER_LEN_AUX	**This field is valid only when dir_change or transfer_len_change is set to 1.** Indicates the number of data bytes to be transferred in 1 transfer unit (excluding slave address byte) for the transfers following the direction change. That is, if dir_change =1, then the first write transfer length will depend on transfer_len, while the second read transfer length depend on transfer_len_aux. Dir change is always after the first transfer. Note: The value must be set to be bigger than 1; otherwise no transfer will take place.

1.18 I2C/SCCB Controller (I2C 2)

1.18.1 Introduction

I2C (Inter-IC)/SCCB (Serial Camera Control Bus) is a two-wire serial interface. The two signals are SCL and SDA. SCL is a clock signal that is driven by the master. SDA is a bi-directional data signal that can be driven by either the master or the slave. This generic controller supports the master role and conforms to the I2C specification.

1.18.2 Features

- I2C compliant master mode operation
- Adjustable clock speed for LS/FS mode operation
- Supports 7-bit/10-bit addressing
- Supports high-speed mode
- Supports slave clock extension
- START/STOP/REPEATED START condition
- Manual transfer mode
- Multi-write per transfer
- Multi-read per transfer
- Multi-transfer per transaction
- Combined format transfer with length change capability.-
- Active drive/wired-and I/O configuration

1.18.3 Block Diagram

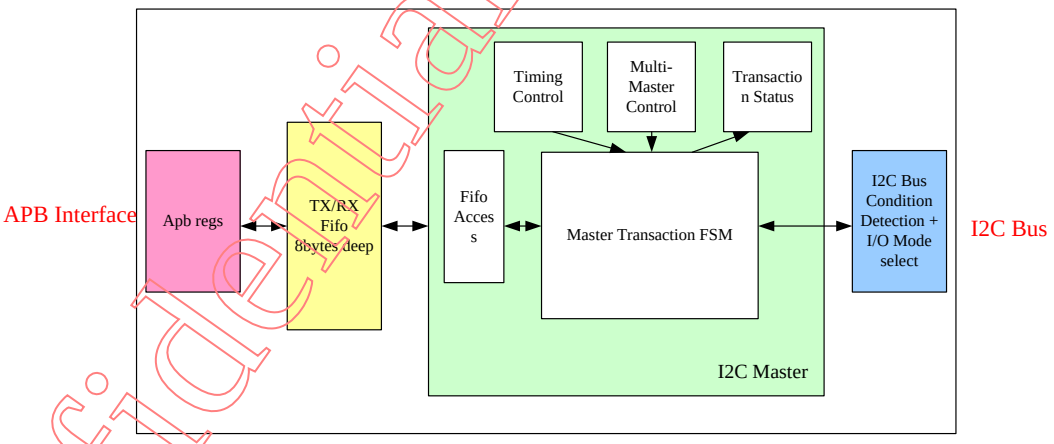


Figure 1-12. Block diagram of I2C

1.18.4 Register Definition

Module name: i2c2 Base address: (+11009000h)

Address	Name	Width	Register Function
11009000	DATA_PORT	16	Data Port Register

Address	Name	Width	Register Function
11009004	SLAVE_ADDR	16	Slave Address Register
11009008	INTR_MASK	16	Interrupt Mask Register
1100900C	INTR_STAT	16	Interrupt Status Register
11009010	CONTROL	16	Control Register
11009018	TRANSAC_LEN	16	Transaction Length Register (Number of Transfers per Transaction)
1100901C	DELAY_LEN	16	Inter Delay Length Register
11009020	TIMING	16	Timing Control Register LS/FS only. This register is used to control the output waveform timing.
11009024	START	16	Start Register
11009028	EXT_CONF	16	Extension Configuration Register
11009030	FIFO_STAT	16	FIFO Status Register
11009034	FIFO_THRESH	16	FIFO Thresh Register (DEBUG ONLY) By default, these values do not need to be adjusted. Note! for RX, no timeout mechanism is implemented. Therefore, RX_trig_thresh must be left at 0, or there would be data left in the fifo that is not fetched by DMA controller.
11009038	FIFO_ADDR_CLR	16	FIFO Address Clear Register
11009040	IO_CONFIG	16	IO Config Register This register is used to configure the I/O for the sda and scl lines to select between normal i/o mode, or open-drain mode to support wired-and bus.
11009044	DEBUG	16	RESERVED DEBUG Register NOTE: This register is for DEBUG ONLY. The bits are R/W, do not change the values from the default value.
11009048	HS	16	High Speed Mode Register This register contains options for supporting high speed operation features
11009050	SOFTRESET	16	Soft Reset Register
11009054	I2C0_I2CREG_HW_CG_EN	16	HW DCM Enable
11009064	DEBUGSTAT	16	Debug Status Register
11009068	DEBUGCTRL	16	Debug Control Register
1100906C	TRANSFER_LEN_AUX	16	Transfer Length Register (Number of Bytes per Transfer)

11009000 DATA_PORT Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name									**DATA_PORT**							
Type									RW							

Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DATA_PORT	**This is the FIFO access port. During master write sequences (slave_addr[0] = 0), this port can be written by APB, and during master read sequences (slave_addr[0] = 1), this port can be read by APB.** (NOTE) Slave_addr must be set correctly before accessing the fifo. (DEBUG ONLY) If the fifo_apb_debug bit is set, then the FIFO can be read and write by the APB

11009004 SLAVE_ADDR Slave Address Register 000000BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SLAVE_ADDR**							
Type									RW							
Reset									1	0	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SLAVE_ADDR	**This specifies the slave address of the device to be accessed. Bit 0 is defined by the I2C protocol as a bit that indicates the direction of transfer. 1 = master read, 0 = master write.**

11009008 INTR_MASK Interrupt Mask Register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SPARE**				**MAS_ARB_LOST**	**MAS_HS_NACKER**	**MAS_ACKERR**	**MAS_TRANSAC_COMP**
Type									RW				RW	RW	RW	RW
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:4	SPARE	**Reserved**
3	MAS_ARB_LOST	**Setting this value to 0 will mask ARB_LOST interrupt signal.**
2	MAS_HS_NACKER	**Setting this value to 0 will mask HS_NACKERR interrupt signal.**
1	MAS_ACKERR	**Setting this value to 0 will mask ACK_ERR interrupt signal.**
0	MAS_TRANSAC_COMP	**Setting this value to 0 will mask TRANSAC_COMP interrupt signal.**

Bit(s)	Name	Description

1100900C INTR_STAT Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RS_MULTIPLE	ARB_LOST	HS_NACKERR	ACKERR	TRANSAC_COMP
Type												W1C	W1C	W1C	W1C	W1C
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	RS_MULTIPLE	
3	ARB_LOST	This status is asserted if the I2C controller loses arbition.
2	HS_NACKERR	This status is asserted if hs master code nack error detection is enabled. If enabled, hs master code nack err will cause transaction to end and stop will be issued.
1	ACKERR	This status is asserted if ACK error detection is enabled. If enabled, ackerr will cause transaction to end and stop will be issued.
0	TRANSAC_COMP	This status is asserted when a transaction has completed successfully.

11009010 CONTROL Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TRANSFER_LEN_CHANGE	ACKERR_DET_EN	DIR_CHANGE	CLK_EXT_EN	DMA_EN	RS_STOP	
Type										RW	RW	RW	RW	RW	RW	
Reset										0	0	0	0	0	0	

Bit(s)	Name	Description
6	TRANSFER_LEN_CHANGE	This options specifies whether or not to change the transfer length after the fist transfer completes. If enabled, the transfers after the first transfer will use the transfer_len_aux parameter.
5	ACKERR_DET_EN	This option enables slave ack error detection. When enabled, if slave ack error is detected, the master shall terminate the transaction by issuing a STOP condition and then asserts ackerr interrupt. Mcu shall handle this case appropriately and then resets the fifo address before reissuing transaction again. If this option is disabled, the

Bit(s)	Name	Description
		controller will ignore slave ack error and keep on scheduled transaction. 0: disable 1: enable
4	DIR_CHANGE	**This option is used for combined transfer format, where the direction of transfer is to be changed from write to read after the FIRST RS condition. Note: when set to 1, the transfers after the direction change will be based on the transfer_len_aux parameter.** 0: disable 1: enable
3	CLK_EXT_EN	**I2C spec allows slaves to hold the SCL line low if it is not yet ready for further processing. Therefore, if this bit is set to 1, master controller will enter a high wait state until the slave releases the SCL line.**
2	DMA_EN	**By default, this is disabled, and fifo data shall be manually prepared by mcu. This default setting should be used for transfer sizes of less than 8 data bytes and no multiple transfer is configured. When enabled, dma requests are turned on, and the fifo data should be prepared in memory.**
1	RS_STOP	**In LS/FS mode, this bit affects multi-transfer transaction only. It controls whether or not REPEATED-START condition is used between transfers. The last ending transfer always ends with a STOP.** In HS mode, this bit must be set to 1. 0: use STOP 1: use REPEATED-START

11009018 TRANSAC_LEN Transaction Length Register (Number of Transfers per Transaction) 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**TRANSFER_LEN**							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:0	TRANSFER_LEN	**This indicates the number of TRANSFERS to be transferred in 1 transaction** (NOTE) The value must be set greater than 1, otherwise no transfer will take place.

1100901C DELAY_LEN Inter Delay Length Register 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DELAY_LEN							
Type									RW							
Reset									0	0	0	0	0	0	1	0

Bit(s)	Name	Description
7:0	DELAY_LEN	This sets the wait delay between consecutive transfers when RS_STOP bit is set to 0. (the unit is same as the half pulse width)

11009020 TIMING Timing Control Register 00001303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_READ_ADJ	DATA_READ_TIME				SAMPLE_CNT_DIV					STEP_CNT_DIV					
Type	RW	RW				RW					RW					
Reset	0	0	0	1		0	1	1			0	0	0	0	1	1

Bit(s)	Name	Description
15	DATA_READ_ADJ	When set to 1, data latch in sampling time during master reads are adjusted according to DATA_READ_TIME value. Otherwise, by default, data is latched in at half of the high pulse width point. This value must be set to less or equal to half the high pulse width.
14:12	DATA_READ_TIME	This value is valid only when DATA_READ_ADJ is set to 1. This can be used to adjust so that data is latched in at earlier sampling points (assuming data is settled by then)
10:8	SAMPLE_CNT_DIV	Used for LS/FS only. This adjusts the width of each sample. (sample width = sample_cnt_div * 1/13Mhz)
5:0	STEP_CNT_DIV	This specifies the number of samples per half pulse width (ie. each high or low pulse)

11009024 START Start Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RS_STOP_MULTIPLE_CONFIG	RS_STOP_MULTIPLE_TRIG	RS_STOP_MULTIPLE_TRIG_CLR													START
Type	RW	RW	RO													RW
Reset	0	0	0													0

Bit(s)	Name	Description
15	RS_STOP_MULTIPLE_CONFIG	**Enable multiple r/w & length & slave address with rs_stop transfer**
14	RS_STOP_MULTIPLE_TRIG	**Trigger next transfer when enable multiple r/w & length & slave address with rs_stop transfer**
13	RS_STOP_MULTIPLE_TRIG_CLR	**Clear the rs_stop_mul_trig for** next transfer
0	START	**This register starts the transaction on the bus. It is auto deasserted at the end of the transaction.**

11009028 EXT_CONF Extension Configuration Register 00001800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_TIME															EXT_EN
Type	RW															RW
Reset	0	0	0	1	1	0	0	0								0

Bit(s)	Name	Description
15:8	EXT_TIME	**Configurable extension time of start condition.** Time unit: 1/4*BASE_CLOCK_PERIOD Note: The max. value is {0xFF-SAMPLE_CNT_DIV}.
0	EXT_EN	**Used for standard mode only (baud rate is up to 100kHz).** This option decides to perform the extension of start/stop condion.If enbale, perform the extension; otherse not. 0: Disable 1: Enable

11009030 FIFO_STAT FIFO Status Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RD_ADDR				WR_ADDR				FIFO_OFFSET						WR_FULL	RD_EMPTY
Type	RO				RO				RO						RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	1

Bit(s)	Name	Description
15:12	RD_ADDR	**The current rd address pointer. (only bit [2:0] has physical meaning)**
11:8	WR_ADDR	**The current wr address pointer. (only bit [2:0] has physical meaning)**
7:4	FIFO_OFFSET	**wr_addr[3:0] - rd_addr[3:0]**
1	WR_FULL	**This indicates that the fifo is full.**

Bit(s)	Name	Description
0	RD_EMPTY	This indicates that the fifo is empty.

11009034 FIFO_THRESH FIFO Thresh Register 00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						TX_TRIG_THRESH								RX_TRIG_THRESH		
Type						RW								RW		
Reset						1	1	1						0	0	0

Bit(s)	Name	Description
10:8	TX_TRIG_THRESH	When tx fifo level is below this value, tx dma request is asserted.
2:0	RX_TRIG_THRESH	When rx fifo level is above this value, rx dma request is asserted.

11009038 FIFO_ADDR_CLR FIFO Address Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FIFO_ADDR_CLR
Type																WO
Reset																0

Bit(s)	Name	Description
0	FIFO_ADDR_CLR	When written with a 1, a 1 pulse fifo_addr_clr is generated to clear the fifo address to back to 0.

11009040 IO_CONFIG IO Config Register 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													IDLE_OE_EN	IO_SYNC_EN	SDA_IO_CONFIG	SCL_IO_CONFIG
Type													RW	RW	RW	RW

Reset													0	0	1	1

Bit(s)	Name	Description
3	IDLE_OE_EN	0: do not drive bus in idle state 1: drive bus in idle state
2	IO_SYNC_EN	**DEBUG ONLY: When set to 1, scl and sda inputs will be first dual synced by bclk_ck. This should not be needed. Only reserved for debugging.**
1	SDA_IO_CONFIG	0: normal tristate io mode 1: open-drain mode
0	SCL_IO_CONFIG	0: normal tristate io mode 1: open-drain mode

11009044 DEBUG RESERVED DEBUG Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**DEBUG**		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	DEBUG	

11009048 HS High Speed Mode Register 00000102

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**HS_SAMPLE_CNT_DIV**				**HS_STEP_CNT_DIV**				**MASTER_CODE**					**HS_NACKERR_DET_EN**	**HS_EN**
Type		RW				RW				RW					RW	RW
Reset		0	0	0		0	0	1		0	0	0			1	0

Bit(s)	Name	Description
14:12	HS_SAMPLE_CNT_DIV	**When high speed mode is entered after the master code transfer has been completed, the sample width becomes dependent on this parameter.**
10:8	HS_STEP_CNT_DIV	**When high speed mode is entered after the master code transfer has been completed, the number of samples per half pulse width becomes dependent on this value.**
6:4	MASTER_CODE	**This is the 3 bit programmable value for the master code to be transmitted.**

Bit(s)	Name	Description
1	HS_NACKERR_DET_EN	**This enables NACKERR detection during the master code transmission. When enabled, if NACK is not received after master code has been transmitted, the transaction will terminated with a STOP condition.**
0	HS_EN	**This enables the high speed transaction. (note: rs_stop must be set to 1 as well)**

11009050 SOFTRESET Soft Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SOFT_RESET
Type																WO
Reset																0

Bit(s)	Name	Description
0	SOFT_RESET	**When written with a 1, a 1 pulse soft reset is used as synchronous reset to reset the I2C internal hardware circuits.**

11009054 I2C0_I2CREG_HW_CG_EN HW DCM Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DCM_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	DCM_EN	**Enable HW DCM function.** Default is disable. 0: Disable 1: Enable

11009064 DEBUGSTAT Debug Status Register 00000020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BUS_BUSY	MASTER_WRITE	MASTER_READ	MASTER_STATE				
Type									RU	RU	RU	RU				
Reset									0	0	1	0	0	0	0	0

Bit(s)	Name	Description
7	BUS_BUSY	**DEBUG ONLY: valid when bus_detect_en is 1. bus_busy = 1 indicates a start transaction has been detected and no stop condition has been detected yet.**
6	MASTER_WRITE	**DEBUG ONLY: 1 = current transfer is in the master write dir**
5	MASTER_READ	**DEBUG ONLY: 1 = current transfer is in the master read dir**
4:0	MASTER_STATE	**DEBUG ONLY: reads back the current master_state.** 0: idle state; 1: i2c master is preparing sending out the start bit, SCL=1, SDA=1; 2: i2c master is sending out the start bit, SCL=1, SDA=0; 3: i2c master/slave is preparing transmitting data bit, SCL=0, SDA=data bit (data bit can be changed when SCL=0); 4: i2c master/slave is transmitting data bit, SCL=1, SDA=data bit (data bit is stable when SCL=1); 5: i2c master/slave is preparing transmitting ack bit, SCL=0, SDA=ack (ack bit can be changed when SCL=0); 6: i2c master/slave is transmitting ack bit, SCL=1, SDA=0 (ack bit is stable when SCL=1); 7: i2c master is preparing sending out stop bit or repeated-start bit, SCL=0, SDA=0/1 (0: means stop bit; 1: means repeated-start bit); 8: i2c master is sending out stop bit or repeated-start bit, SCL=1, SDA=1/0 (1: means stop bit; 0: means repeated-start bit); 9: i2c master is in delay start between two transfers, SCL=1, SDA=1; 10: i2c master is in fifo wait state; For writing transaction, it means fifo is empty and i2c master is waiting for dma controller writing data into fifo; For reading transaction, it means fifo is full and i2c master is waiting for dma controller reading data from fifo, SCL=0, SDA=do not care; 12: i2c master is preparing sending out data bit of master code. This state is used only in high-speed transaction, SCL=0, SDA=data bit of master code (data bit of master code can be changed when SCL=0); 13: i2c master is sending out data bit of master code. This state is used only in high-speed transaction, SCL=1, SDA=data bit of master code (data bit of master code is stable when SCL=1); 14: i2c master/slave is preparing transmitting nack bit, SCL=0, SDA=nack bit (nack bit can be changed when SCL=0); This state is used only in high-speed transaction; 15: i2c master/slave is transmitting nack bit, SCL=1, SDA=1; This state is used only in high-speed transaction;

11009068 DEBUGCTRL Debug Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															APB_DEBUG_RD	FIFO_APB_DEBUG
Type															WO	RW
Reset															0	0

Bit(s)	Name	Description
1	APB_DEBUG_RD	**This bit is only valid when fifo_apb_debug is set to 1. Writing to this register will generate a 1 pulsed fifo apb rd signal for reading the fifo data.**
0	FIFO_APB_DEBUG	**This is used for trace32 debug purposes. When using trace32, and the memory map is shown, turning this bit on will block the normal apb read access. Apb read access to the fifo is then enabled by writing to apb_debug_rd.** 0: disable 1: enable

1100906C TRANSFER_LEN_AUX Transfer Length Register (Number of Bytes per Transfer) 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TRANSFER_LEN_AUX**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	TRANSFER_LEN_AUX	**This field is valid only when dir_change or transfer_len_change is set to 1.** Indicates the number of data bytes to be transferred in 1 transfer unit (excluding slave address byte) for the transfers following the direction change. That is, if dir_change =1, then the first write transfer length will depend on transfer_len, while the second read transfer length depend on transfer_len_aux. Dir change is always after the first transfer. Note: The value must be set to be bigger than 1; otherwise no transfer will take place.

1.19 SPI 0

1.19.1 Introduction

The SPI interface is a bit-serial, four-pin transmission protocol. The figure is an example of the connection between the SPI master and SPI slave. The SPI controller interface is a master responsible of the data transmission with the slave.

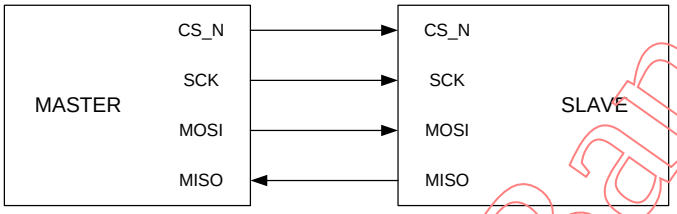


Figure 1-13. Pin connection between SPI master and SPI slave

1.19.1.1 Pin Description

Signal name	Type	Description
CS_N	O	Low active chip selection signal
SCK	O	The (bit) serial clock
MOSI	O	Data signal from master output to slave input
MISO	I	Data signal from slave output to master input

Table 1-7. SPI controller interface

1.19.1.2 Transmission Formats

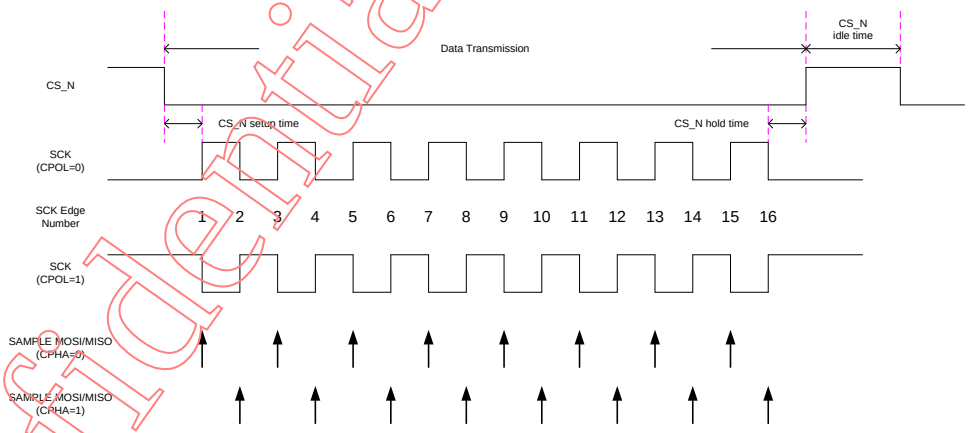


Figure 1-14. SPI transmission formats

The figure shows the waveform during the SPI transmission. The low active CS_N determines the start point and end point of one transaction. The CS_N setup time, hold time and idle time are also depicted. CPOL defines the clock polarity in the transmission. Two types of polarity can be adopted, i.e. polarity 0 and polarity 1.

CPHA defines the legal timing to sample MOSI and MISO. Two different methods can be adopted.

1.19.2 Features

The features of the SPI controller (master) are:
Configurable CS_N setup time, hold time and idle time

- Programmable SCK high time and low time
- Configurable transmitting and receiving bit order
- Two configurable modes for the source of the data to be transmitted.
  (1) In TX DMA mode, the SPI controller automatically fetches the transmitted data (to be put on the MOSI line) from memory;
  (2) In TX FIFO mode, the data to be transmitted on the MOSI line are written to FIFO before the start of the transaction.
- Two configurable modes for destination of the data to be received.
  (1) In RX DMA mode, the SPI controller automatically stores the received data (from MISO line) to memory;
  (2) In RX FIFO mode, the received data keep being in RX FIFO of the SPI controller. The processor must read back the data by itself.
- Adjustable endian order from/to memory system
- Programmable byte length for transmission
- Unlimited length for transmission. This is achieved by the operation of PAUSE mode. In PAUSE mode, the CS_N signal will keep being active (low) after the transmission. At this time, the SPI controller is in PAUSE_IDLE state, ready to receive the resume command. The state transition is shown in below figure.
- Configurable option to control CS_N de-assert between byte transfers. The controller supports a special transmission format called CS_N de-assert mode.

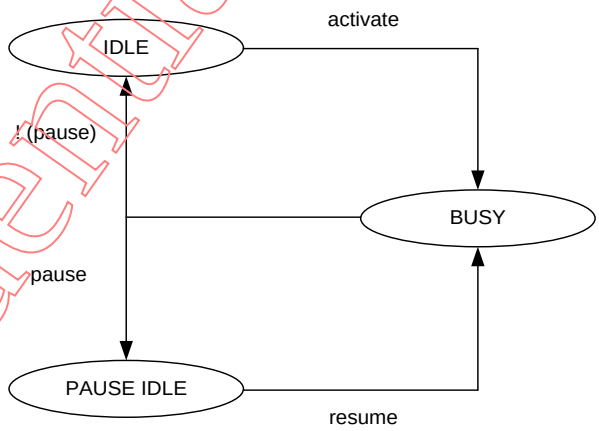


Figure 1-15. Operation flow with or without PAUSE mode

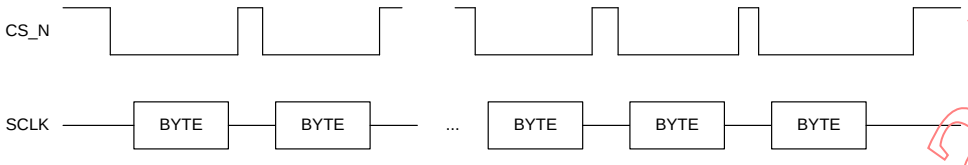


Figure 1-16. CS_N de-assert mode

1.19.3 Block Diagram

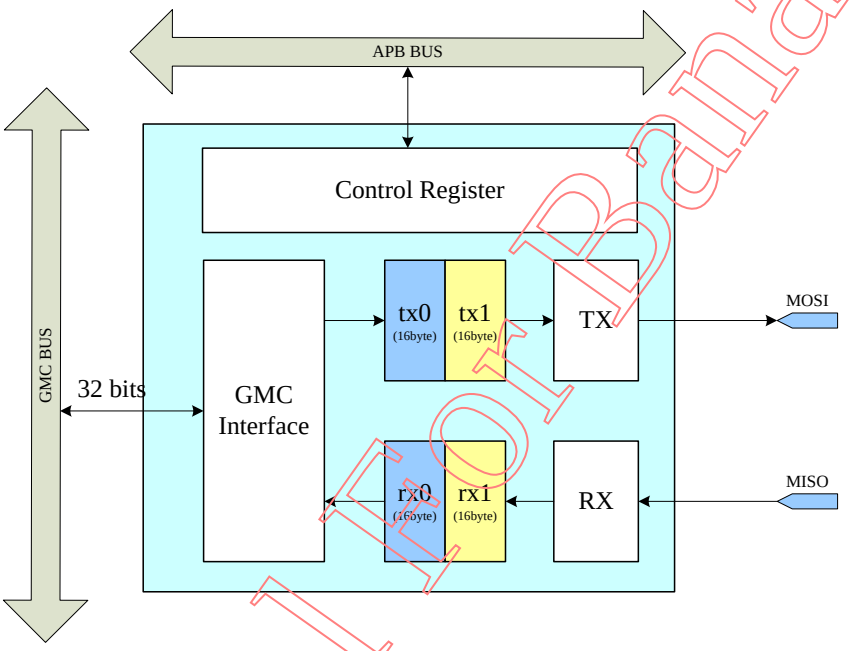


Figure 1-17. Block diagram of SPI

1.19.4 Register Definition

Module name: spio Base address: (+1100a000h)

Address	Name	Width	Register Function
1100A000	SPI_CFG0	32	SPI Configuration 0 Register
1100A004	SPI_CFG1	32	SPI Configuration 1 Register
1100A008	SPI_TX_SRC	32	SPI TX Source Address Register
1100A00C	SPI_RX_DST	32	SPI RX Destination Address Register
1100A010	SPI_TX_DATA	32	SPI TX Data FIFO
1100A014	SPI_RX_DATA	32	SPI RX Data FIFO
1100A018	SPI_CMD	32	SPI Command Register
1100A01C	SPI_STATUS0	32	SPI Status 0 Register
1100A020	SPI_STATUS1	32	SPI Status 1 Register
1100A024	SPI_PAD_MACRO_SEL	32	SPI pad_macro Selection Register
1100A028	SPI_CFG2	32	SPI Configuration 2 Register

1100A000 SPI_CFG0 SPI Configuration 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CS_SETUP_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CS_HOLD_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CS_SETUP_COUNT	**Chip select setup time = (CS_SETUP_COUNT + 1)*CLK_PERIOD; CLK_PERIOD is the cycle time of the clock SPI engine adopts.**
15:0	CS_HOLD_COUNT	**The chip select hold time = (CS_HOLD_COUNT+1) * CLK_PERIOD.**

1100A004 SPI_CFG1 SPI Configuration 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GET_TICK_DLY						PACKET_LENGTH									
Type	RW						RW									
Reset	0	0	0				0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PACKET_LOOP_CNT								CS_IDLE_COUNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:29	GET_TICK_DLY	**If the speed of SPI is not fast enough, these three bits can help tolerance get_tick timing. The timing range between get_tick is one cycle depending on the SPI system clock.**
25:16	PACKET_LENGTH	
15:8	PACKET_LOOP_CNT	**PACKET_LENGTH[9:0] defines the number of bytes in one packet, and PACKET_LOOP_CNT[7:0] defines the number of packets within one transaction. The number of bytes in one packet = PACKET_LENGTH + 1. The number of packets in one transaction = PACKET_LOOP_CNT + 1. Total bytes of one transaction = (PACKET_LENGTH + 1)*(PACKET_LOOP_CNT + 1).**
7:0	CS_IDLE_COUNT	**Chip select idle time between consecutive transaction = (CS_HOLD_COUNT + 1)*CLK_PERIOD**

1100A008 SPI_TX_SRC SPI TX Source Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_TX_SRC															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_TX_SRC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_TX_SRC	**If TX_DMA_EN is set, the data to be put on the MOSI line will be kept in memory in advance, and the SPI controller will automatically read the data from memory. SPI_TX_SRC defines the memory address from which SPI controller starts to read data.**

1100A00C SPI_RX_DST SPI RX Destination Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_RX_DST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_RX_DST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_RX_DST	**If RX_DMA_EN is set, the received data from the MISO line will be moved to memory automatically by the SPI controller. SPI_RX_DST defines the memory address to which the SPI controller starts to store the data.**

1100A010 SPI_TX_DATA SPI TX Data FIFO 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_TX_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_TX_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_TX_DATA	**The depth of the TX FIFO is 32 bytes.** Write to this register will write 4 bytes to TX FIFO. The TX FIFO pointer will automatically move towards the next four bytes. Read from this register will read 4 bytes from FIFO, and TX FIFO pointer will automatically move towards the next four bytes.

Bit(s)	Name	Description

1100A014 SPI_RX_DATA SPI RX Data FIFO 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_RX_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_RX_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_RX_DATA	**The depth of the RX FIFO is 32 bytes.** Read from this register will read 4 bytes from RX FIFO. The RX FIFO pointer will automatically move towards the next four bytes. Write to this register will write 4 bytes to FIFO, and the RX FIFO pointer will automatically move towards the next four bytes.

1100A018 SPI_CMD SPI Command Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															PAUSE_IE	FINISH_IE
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_ENDIAN	RX_ENDIAN	RXMSBF	TXMSBF	TX_DMA_EN	RX_DMA_EN	CPOL	CPHA	CS_POL	SAMPLE_SEL	CS_DEASSERT_EN	PAUSE_EN		RST	RESUME	CMD_ACT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
17	PAUSE_IE	**Interrupt enable bit of pause flag in SPI status register**
16	FINISH_IE	**Interrupt enable bit of finish flag in SPI status register**
15	TX_ENDIAN	**Defines whether to reverse the endian order of the data DMA from memory** 0: Does not reverse (default) Only supported in DMA mode.
14	RX_ENDIAN	**Defines whether to reverse the endian order of the data DMA to memory** 0: Does not reverse (default)
13	RXMSBF	**Indicates data received from MISO line is MSB first or not** Set RXMSBF to 1 for MSB first; otherwise set it to 0.

Bit(s)	Name	Description
12	TXMSBF	**Indicates data sent on MOSI line is MSB first or not** Set TXMSBF to 1 for MSB first; otherwise set it to 0.
11	TX_DMA_EN	**DMA mode enable bit of the data to be transmitted** 0: Not to enable (default)
10	RX_DMA_EN	**DMA mode enable bit of the data received** 0: Not to enable (default)
9	CPOL	**Control bit of SCK polarity** 0: CPOL = 0 1: CPOL = 1
8	CPHA	**Defines SPI Clock Format 0 or SPI Clock Format 1 during transmission** 0: CPHA = 0 1: CPHA = 1
7	CS_POL	**Control bit of chip select polarity** 0: Active low 1: Active high
6	SAMPLE_SEL	**Control bit of sample edge of MISO** 0: Postive edge 1: Negative edge
5	CS_DEASSERT_EN	**Enable bit of chip select de-assertion mode** Set to 1 to enable this mode.
4	PAUSE_EN	**Enable bit of pause mode** Set to 1 to enable this mode.
2	RST	**Software reset bit** When this bit is 1, software reset will be active high. Default: 0.
1	RESUME	**Used when controller is in PAUSE IDLE state** Write 1 to this bit to trigger the SPI controller to resume transfer from PAUSE IDLE state.
0	CMD_ACT	**Command activate bit** Write 1 to this bit to trigger the SPI controller to start the transaction.

1100A01C SPI_STATUS0 SPI Status 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**PAUSE**	**FINISH**
Type															RC	RC
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Interrupt status bit in pause mode** Will be set by the SPI controller when it completes the transaction, entering the PAUSE IDLE state.
0	FINISH	**Interrupt status bit in non-pause mode** Will be set by the SPI controller when it completes the transaction, entering the IDLE state.

1100A020 SPI_STATUS1 SPI Status 1 Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BUSY
Type																RO
Reset																1

Bit(s)	Name	Description
0	BUSY	**Status flag reflecting SPI controller is busy or not** This bit is low active; 0 means the SPI controller is busy now. 1'b1:idle 1'bo:busy

1100A024 SPI_PAD_MACRO_SEL SPI pad_macro Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PAD_MACRO_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	PAD_MACRO_SEL	**Selects which PAD group SPI will use**

1100A028 SPI_CFG2 SPI Configuration 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SCK_LOW_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCK_HIGH_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SCK_LOW_COUNT	**SCK clock low time = (SCK_LOW_COUNT + 1)*CLK_PERIOD**
15:0	SCK_HIGH_COUNT	**SCK clock high time = (SCK_HIGH_COUNT + 1)*CLK_PERIOD**

Bit(s)	Name	Description

1.20 Nand Flash Interface (NFI)

1.20.1 Introduction

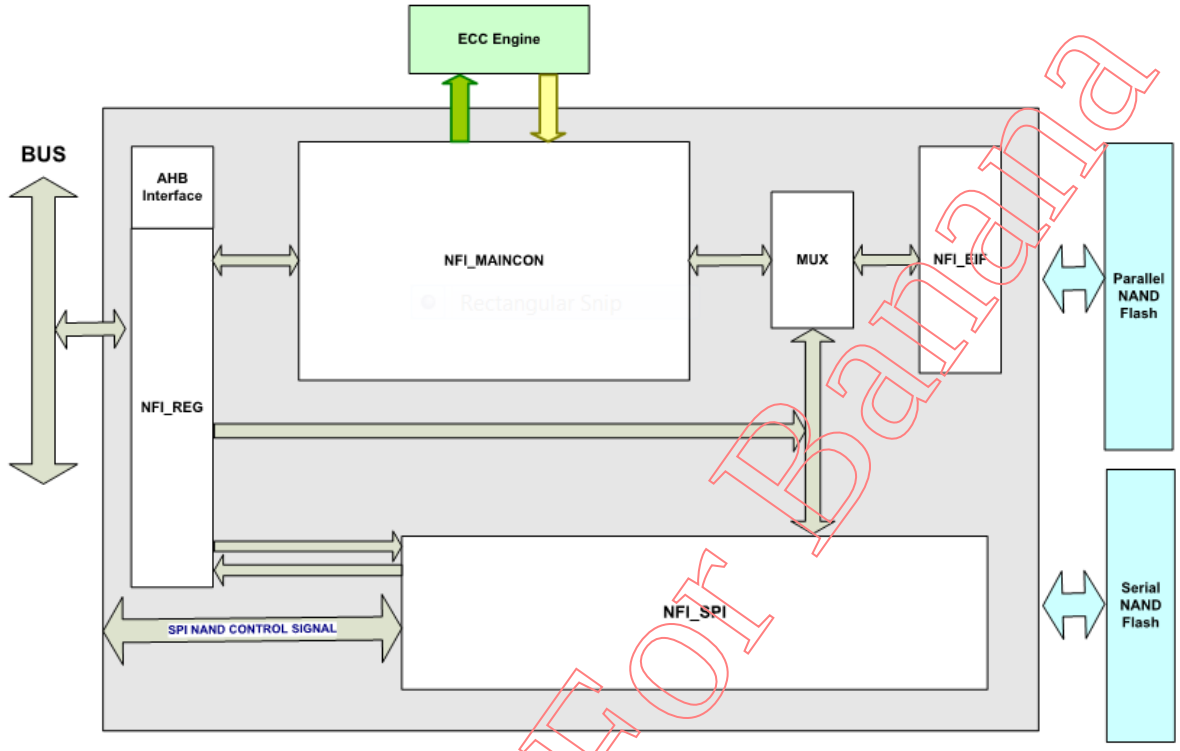
The NFI and ECC engine (in NFI mode) can automatically generate ECC syndrome bits when programming or reading the device. If the user approves the way it stores the syndrome bits in the spare area for each page, the HW_ECC mode can be used. Otherwise, the user can prepare the data (may contains operating system information or ECC syndrome bits) for the spare area with another arrangement. In former cases, the NFI and ECC engine (in NFI mode) checks the syndrome bits when reading from the device. The ECC module features BCH code, which is capable of correcting up to 16-bits errors within one sector.

Addtionaly, SPI NAND interface controller is added to NFI design.

1.20.2 Features

- ECC Engine: ECC (BCH code) acceleration capable of 16-bit error correction, and support encode and decode.
- APB: Word/byte access through APB bus(PIO Mode), and Register R/W
- AHB: DMA Mode for massive data transfer
- MUX: switch SPI/Parallel mode data path Function
- NFI MAINCON: Parallel NAND and SPI NAND common control circuit
- NFI_EIF: generate Parallel NAND Interface protocol and timing with state machine
- NFI_SPI: SPI NAND Main controller Supports 8 I/O interface

1.20.3 Block Diagram



1.20.4 Register Definition

Module name: NFI Base address: (+1100d000h)

Address	Name	Width	Register Function
1100D000	NFI_CNFG	16	NFI Configuration
1100D004	NFI_PAGEFMT	16	NFI Page Format Control Register
1100D008	NFI_CON	16	NFI Operation Control Register
1100D00C	NFI_ACCCON	32	NAND Flash Access Timing Control register
1100D010	NFI_INTR_EN	16	NFI Interrupt Enable Register
1100D014	NFI_INTR	16	NFI Interrupt Status Register
1100D020	NFI_CMD	16	NFI Command register
1100D030	NFI_ADDRNOB	16	NFI Address Length Register
1100D034	NFI_COLADDR	32	NFI Column Address Register
1100D038	NFI_ROWADDR	32	NFI Row Address Register
1100D040	NFI_STRDATA	16	NFI Data Transfer Start Trigger Register
1100D044	NFI_CNRNB	16	NFI Check NAND Ready/Busy Register
1100D050	NFI_DATAW	32	NFI Write Data Buffer
1100D054	NFI_DATAR	32	NFI Read Data Buffer
1100D058	NFI_PIO_DIRDY	16	PIO_mode Data Ready Register
1100D060	NFI_STA	32	NFI Status
1100D064	NFI_FIFOSTA	16	NFI FIFO Status
1100D070	NFI_ADDRCNTR	16	NFI Page Address Counter Register

Address	Name	Width	Register Function
1100D080	NFI_STRADDR	32	NFI AHB Start Address Register
1100D084	NFI_BYTELEN	16	NFI DMA Byte Length Register
1100D090	NFI_CSEL	16	NFI device select register
1100D094	NFI_IOCON	32	NFI IO Control register
1100D0A0	NFI_FDM0L	32	NFI Least FDM Data for Sector 0 Register
1100D0A4	NFI_FDM0M	32	NFI Most FDM Data for Sector 0 Register
1100D0A8	NFI_FDM1L	32	NFI Least FDM Data for Sector 1 Register
1100D0AC	NFI_FDM1M	32	NFI Most FDM Data for Sector 1 Register
1100D0B0	NFI_FDM2L	32	NFI Least FDM Data for Sector 2 Register
1100D0B4	NFI_FDM2M	32	NFI Most FDM Data for Sector 2 Register
1100D0B8	NFI_FDM3L	32	NFI Least FDM Data for Sector 3 Register
1100D0BC	NFI_FDM3M	32	NFI Most FDM Data for Sector 3 Register
1100D0C0	NFI_FDM4L	32	NFI Least FDM Data for Sector 4 Register
1100D0C4	NFI_FDM4M	32	NFI Most FDM Data for Sector 4 Register
1100D0C8	NFI_FDM5L	32	NFI Least FDM Data for Sector 5 Register
1100D0CC	NFI_FDM5M	32	NFI Most FDM Data for Sector 5 Register
1100D0D0	NFI_FDM6L	32	NFI Least FDM Data for Sector 6 Register
1100D0D4	NFI_FDM6M	32	NFI Most FDM Data for Sector 6 Register
1100D0D8	NFI_FDM07L	32	NFI Least FDM Data for Sector 7 Register
1100D0DC	NFI_FDM7M	32	NFI Most FDM Data for Sector 7 Register
1100D190	NFI_FIFODATA0	32	NFI FIFO Content Data 0
1100D194	NFI_FIFODATA1	32	NFI FIFO Content Data 1
1100D198	NFI_FIFODATA2	32	NFI FIFO Content Data 2
1100D19C	NFI_FIFODATA3	32	NFI FIFO Content Data 3
1100D200	NFI_MCON	16	NFI LCD Monitor Control Register
1100D204	NFI_TOTALCNT	32	NFI LCD Monitor Total Cycle Count
1100D208	NFI_RQCNT	32	NFI LCD Monitor Request Cycle Count
1100D20C	NFI_ACCNT	32	NFI LCD Monitor Access Cycle Count
1100D220	NFI_DEBUG_CON1	16	NFI Debug register
1100D224	NFI_MASTERSTA	16	NFI Master Status
1100D22C	NFI_SECCUS_SIZE	32	Enable bit for customized size for each sector
1100D230	NFI_SPIADDRCNTR	32	NFI AHB Start Address Register
1100D234	NFI_SPIBYTELEN	32	NFI DMA Byte Length Register
1100D500	SNF_MAC_CTL	32	Serial nand flash mac mode control
1100D504	SNF_MAC_OUTL	32	Serial nand flash mac mode output data length
1100D508	SNF_MAC_INL	32	Serial nand flash mac mode input data length
1100D50C	SNF_RD_CTL1	32	Serial nand flash read control 1
1100D510	SNF_RD_CTL2	32	Serial nand flash read control 2
1100D514	SNF_RD_CTL3	32	Serial nand flash read control 3
1100D518	SNF_GF_CTL1	32	Serial nand flash get feature control 1
1100D520	SNF_GF_CTL3	32	Serial nand flash mac mode control
1100D524	SNF_PG_CTL1	32	Serial nand flash program control1
1100D528	SNF_PG_CTL2	32	Serial nand flash program control2
1100D52C	SNF_PG_CTL3	32	Serial nand flash program control3
1100D530	SNF_ER_CTL	32	Serial nand flash erase control

Address	Name	Width	Register Function
1100D534	SNF_ER_CTL2	32	Serial nand flash erase control 2
1100D538	SNF_MISC_CTL	32	Serial nand flash MISC control
1100D53C	SNF_MISC_CTL2	32	Serial nand flash MISC control 2
1100D540	SNF_DLY_CTL1	32	Serial nand flash delay control setting 1
1100D544	SNF_DLY_CTL2	32	Serial nand flash delay control setting 2
1100D548	SNF_DLY_CTL3	32	Serial nand flash control setting 3
1100D54C	SNF_DLY_CTL4	32	Serial nand flash delay control setting 4
1100D550	SNF_STA_CTL1	32	
1100D554	SNF_STA_CTL2	32	
1100D558	SNF_STA_CTL3	32	
1100D55C	SNF_SNF_CNFG	32	SPI/Parallel NAND Selection
1100D560	SNF_DEBUG_SEL	32	DEBUG MUX Selection

1100D000 NFI_CNFG NFI Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**OP_MODE**					**AUTO_**	**HW_**		**BYTE_**				**DMA_**	**READ_**	**DMA_**
Type		RW					RW	RW		RW				RW	RW	RW
Reset		0	0	0			0	0		0				0	0	0

Bit(s)	Name	Description
14:12	OP_MODE	**The field control the operating process flow of FSM for NFI.** 000b: Idle state. 001b: Read Process. Recommend for basic read operation. 010b: Single Read Process. Recommend for read id and read status. 011b: Program Process. Recommend for basic program operation.

Bit(s)	Name	Description
		100b: Erase Process. Recommend for basic erase operation. 101b: Reset Process. Recommend for basic reset operation. 110b: Custom Process. Recommend for all advance operation. Others: Reserved
9	AUTO_FMT_EN	**Automatic HW ECC encode or decode enable.** If enabled, the ECC parity from HW ECC engine and FDM data from Register are written automatically to the spare area. If disable, the spare data all comes from PIO register, like DATAR, DATAW, (PIO Mode) or the memory(DMA Mode) as main area data.
8	HW_ECC_EN	**This field is used to enable encoding or decoding operation of HW ECC engine. If the bit is enabled, the data is transferring to ECC engine for encoding and decoding. The ECC Engine should be configured as nfi encoding mode, otherwise the NFI will hang.**
6	BYTE_RW	**Enable byte access. The valid bytes read from NFI_DATAR and NFI_DATAW is only DRo and DWo if BYTE_RW is enabled.**
2	DMA_BURST_EN	**When NFI is in DMA mode, single and burst(incremental) trans type are used. If start address is not alignment,single trans will auto be issued till address is alignment when DMA_BURST_EN is enabled in DMA mode** 0: DMA burst transaction disable 1: DMA burst transaction enable
1	READ_MODE	**This field is used to control the activity of read or write transfer.** 0: write operation of DMA or PIO. 1: read operation of DMA or PIO.
0	DMA_MODE	**This field is used to control the Operation mode.** 0: PIO mode. All data (include read or write) move by MCU through APB access. 1: DMA mode. All data (include read or write) move by HW automation through AHB bus.

1100D004 NFI_PAGEFMT NFI Page Format Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM_ECC_NUM				FDM_NUM						SPARE_SIZE		DBYTE_EN		PAGE_SIZE	
Type	RW				RW						RW		RW		RW	
Reset	0	0	0	0	0	0	0	0			0	0	0		0	0

Bit(s)	Name	Description
15:12	FDM_ECC_NUM	**The number of each FDM data for HW ECC protection. The valid number of bytes ranges are from 0 to 8.**
11:8	FDM_NUM	**The FDM data number for each spare area. The valid number of bytes are from 0 to 8.**
5:4	SPARE_SIZE	**The fields represents the spare size value .** 0: 16Bytes 1: 26Bytes 2: 27Bytes 3: 28Bytes
3	DBYTE_EN	**16 bits I/O bus interface enable.**
1:0	PAGE_SIZE	**Page Size. The field specifies the size of one page for the device. Some most widely used page size are supported.** 0: The page size is 512 bytes (including 512 bytes data area and (spare_size*1) bytes spare area). 1: The page size is 2k bytes (including 2048 bytes data area and (spare_size*4) bytes spare area). 2: The page size is 4k bytes (including 4096 bytes data area and (spare_size*8) bytes spare area). 3: Reserved.

1100D008 NFI_CON NFI Operation Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEC_NUM						BWR	BRD	NOB			SRD			NFI_	FIFO
Type	RW						RW	RW	RW			WO			WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Name	Description
15:12	SEC_NUM	**The field represents the sector number to be retrieved from the device or DMA Master. The valid number ranges from 1 to 8.**
9	BWR	**Burst write mode. Setting to be logic-1 enables the data burst write operation.**
8	BRD	**Burst read mode. Setting this field to be logic-1 enables the data read operation. The NFI core will issue read cycles to retrieve data from the device when the data FIFO is not full or the device is not in the busy state. The NFI core supports consecutive page reading.**
7:5	NOB	**The field represents the number of bytes to be retrieved from the device in single mode, and the number of bytes per APB transaction in both single and burst mode. If device is 16-bit IO, the read bytes number will double** 0: Read 8 bytes from the device. (16 byte for 16-bit IO) 1: Read 1 byte from the device. (2 byte for 16-bit IO) 2: Read 2 bytes from the device. (4 byte for 16-bit IO) 3: Read 3 bytes from the device. (6 byte for 16-bit IO) 4: Read 4 bytes from the device. (8 byte for 16-bit IO) 5: Read 5 byte from the device. (10 byte for 16-bit IO) 6: Read 6 bytes from the device. (12 byte for 16-bit IO) 7: Read 7 bytes from the device. (14 byte for 16-bit IO)
4	SRD	**Setting to be logic-1 initializes the one-shot data read operation. It's mainly used for read ID and read status command, which requires no more than 4 read**

Bit(s)	Name	Description
		cycles to retrieve data from the device. It used when FIFO is empty or after reset nficore
1	NFI_RST	**Reset the state machine, data FIFO (0x0000) and FDM data (0xffff)**
0	FIFO_FLUSH	**Flush the data FIFO.**

1100D00C NFI_ACCCON NAND Flash Access Timing Control register F3FFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	POECS				PRECS				C2R							
Type	RW				RW				RW							
Reset	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W2R				WH				WST				RLT			
Type	RW				RW				RW				RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:28	POECS	**The field represents the minimum required time for CS post-pulling down after the access to device.** Minimum required time = PRECS[1:0] + PRECS[2]*8 + PRECS[3]*64 (T)
27:22	PRECS	**The field represents the minimum required time for CS pre-pulling down before any access to device.** Minimum required time = PRECS[1:0] + PRECS[3:2]*8 + PRECS[5:4]*128 (T)
21:16	C2R	**The field represents the minimum required time from NCEB low to NREB low. It's in unit of 2T.** Minimum required time = C2R[5:0]*2 + 1 (T)
15:12	W2R	**The field represents the minimum required time from NWEB high to NREB low. It's in unit of 2T. So the actual time ranges from 0T to 30T in step of 2T.** Minimum required time = W2R[3:0]*2 + 1 (T)
11:8	WH	**Write-enable hold-time.** The field specifies the hold time of NALE, NCLE, NCEB signals relative to the rising edge of NWEB. This field is associated

Bit(s)	Name	Description
		with WST to expand the write cycle time, and is associated with RLT to expand the read cycle time.
7:4	WST	**Write Wait State** The field specifies the wait states to be inserted to meet the requirement of the pulse width of the NWEB signal. 00b: No wait state. 01b: 1T wait state. 10b: 2T wait state. 11b: 3T wait state.
3:0	RLT	**Read Latency Time** The field specifies how many wait states to be inserted to meet the requirement of the read access time for the device. 00b: No wait state. 01b: 1T wait state. 10b: 2T wait state. 11b: 3T wait state.

1100D010 NFI_INTR_EN NFI Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AUTO	AUTO	AUTO	CUST	CUST	AHB_	ACCE	BUSY	ERAS	RESE	WR_	RD_

					]			_]	]	]						
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	AUTO_BLKER_INTR_EN	**The done interrupt enable for spi auto block earase**
10	AUTO_READ_INTR_EN	**The done interrupt enable for spi auto read**
9	AUTO_PROGRAM_INTR_EN	**The done interrupt enable for spi auto program**
8	CUSTOM_READ_INTR_EN	**The done interrupt enable for spi custom read**
7	CUSTOM_PROGRAM_INTR_EN	**The done interrupt enable for spi custom program**
6	AHB_DONE_EN	**The done interrupt enable for DMA mode.**
5	ACCESS_LOCK_EN	
4	BUSY_RETURN_EN	**The busy return interrupt enable.**
3	ERASE_DONE_EN	**The erase completion interrupt enable.**
2	RESET_DONE_EN	**The reset completion interrupt enable.**
1	WR_DONE_EN	**The single page write completion interrupt enable.**
0	RD_DONE_EN	**The single page read completion interrupt enable.**

1100D014 NFI_INTR NFI Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**AUTO_**]	**AUTO_**]	**AUTO_**]	**CUST** ( ]	**CUST** ( ]	**AHB_**]	**ACCE** S]	**BUSY**]	**ERAS**]	**RESE**]	**WR_**]	**RD_**]

					]	]	]	]	]	]						
Type					RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	AUTO_BLKER_INTR	**Indicates that the spi auto erase is completed.**
10	AUTO_READ_INTR	**Indicates that the spi auto read is completed.**
9	AUTO_PROGRAM_INTR	**Indicates that the spi auto program is completed.**
8	CUSTOM_READ_INTR	**Indicates that the spi custom read is completed.**
7	CUSTOM_PROGRAM_INTR	**Indicates that the spi custom program is completed.**
6	AHB_DONE	**Indicates that the AHB operation is completed.**
5	ACCESS_LOCK	
4	BUSY_RETURN	**Indicates that the device state returns from busy by inspecting the R/B# pin.**
3	ERASE_DONE	**Indicates that the erase operation is completed.**
2	RESET_DONE	**Indicates that the reset operation is completed.**
1	WR_DONE	**Indicates that the write operation is completed.**
0	RD_DONE	**Indicates that the single page read operation is completed.**

1100D020 NFI_CMD NFI Command register 00000045

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**CMD**							
Type									RW							
Reset									0	1	0	0	0	1	0	1

Bit(s)	Name	Description
7:0	CMD	**Command word.**

1100D030 NFI_ADDRNOB NFI Address Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										ROW_ADDR_NOB				COL_ADDR_NOB		
Type										RW				RW		
Reset										0	0	0		0	0	0

Bit(s)	Name	Description
6:4	ROW_ADDR_NOB	**Number of bytes for the row address**
2:0	COL_ADDR_NOB	**Number of bytes for the column address**

1100D034 NFI_COLADDR NFI Column Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COL_ADDR3								COL_ADDR2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COL_ADDR1								COL_ADDR0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	COL_ADDR3	**The 3-th column address byte.**
23:16	COL_ADDR2	**The 2-th column address byte.**
15:8	COL_ADDR1	**The 1-th column address byte.**

Bit(s)	Name	Description
7:0	COL_ADDR0	**The 0-th column address byte.**

1100D038 NFI_ROWADDR NFI Row Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ROW_ADDR3								ROW_ADDR2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ROW_ADDR1								ROW_ADDR0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	ROW_ADDR3	**The 3-th row address byte.**
23:16	ROW_ADDR2	**The 2-th row address byte.**
15:8	ROW_ADDR1	**The 1-th row address byte.**
7:0	ROW_ADDR0	**The 0-th row address byte.**

1100D040 NFI_STRDATA NFI Data Transfer Start Trigger Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STR_
Type																WO
Reset																0

Bit(s)	Name	Description
0	STR_DATA	**This signal triggers the data transfer for read or write. It only takes effect as custom operation mode**

1100D044 NFI_CNRNB NFI Check NAND Ready/Busy Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CB2R_TIME							STR_
Type									RW							WO
Reset									0	0	0	0				0

Bit(s)	Name	Description
7:4	CB2R_TIME	**This time-out registers for polling the NAND busy/ready signal. The unit is 16T clock cycles. The clock rate is 61.44MHz in normal mode. It will be slow down after enable HW DCM mode.**
0	STR_CNRNB	**This signal triggers NFI to poll the status the NAND busy/ready signal after CB2R_TIME*16 cycles. This function is used to avoid the fail function of "BUSY2READY" status or "BUSY_RETURN" interrupt when NAND is operating at very low frequency(<7MHz). If NAND is operating in lower frequency, the sampling for the event, NAND busy/ready signal from low to high, may be failed and NFI will be hanged in busy state. This signal is a time-out register to check the NAND status. The results will be report to "BUSY2READY" status and "BUSY_RETURN" interrupt.**

1100D050 NFI_DATAW NFI Write Data Buffer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DW3								DW2							
Type	WO								WO							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW1								DW0							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DW3	**Write data byte 3.**
23:16	DW2	**Write data byte 2.**
15:8	DW1	**Write data byte 1.**
7:0	DW0	**Write data byte 0.**

1100D054 NFI_DATAR NFI Read Data Buffer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DR3								DR2							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DR1								DR0							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DR3	**Read data byte 3.**
23:16	DR2	**Read data byte 2.**
15:8	DR1	**Read data byte 1.**
7:0	DR0	**Read data byte 0.**

1100D058 NFI_PIO_DIRDY PIO_mode Data Ready Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PIO_
Type																RO
Reset																1

Bit(s)	Name	Description
0	PIO_DI_RDY	**indicates the PIO mode is ready for read data in read mode and ready for write data in write mode.** 0: NFI_DATAR and NFI_DATAW should not be read or write (not ready). 1: NFI is ready for reading data in ready mode and writing data in write mode.

1100D060 NFI_STA NFI Status 00001000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				NAND_FSM									NFI_FSM			
Type				RO									RO			
Reset				0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				READ			BUSY	BUSY				ACCES	DATA	DATA	ADD	CMD
Type				RO			RO	RO				RO	RO	RO	RO	RO
Reset				1			0	0				0	0	0	0	0

Bit(s)	Name	Description
28:24	NAND_FSM	**The field represents the state of NAND interface FSM.** 000000b: IDLE. idle. 111000b: PRE_CS. Pre CS state. 001001b: CMD_WRST. command write set up 001010b: CMD_WR. Command write enable. 001011b: CMD_WRHD. Command write hold. 001000b: CMD_WRRDY 010001b: ADDR_WRST. Address write set up 010010b: ADDR_WR. Address write enable 010011b: ADDR_WRHD. Address write hold 010000b: ADDR_WRRDY. 011000b: CA2DEXT. Command address write extension. 100001b: DATA_RDST. Data read set up. 100010b: DATA_RD. Data read enable. 100011b: DATA_RDHD. Data read hold. 110001b: DATA_WRST. Data write set up. 110010b: DATA_WR. Data write enable. 110011b: DATA_WRHD. Data write hold. Others: Reserved
19:16	NFI_FSM	**The field represents the state of NFI internal FSM.** 0000b: idle. 0001b: reset. Reset command to ready 0010b: read busy. 0011b: read data. 0100b: program busy 0101b: program data. Input data command to program command

Bit(s)	Name	Description
		1000b: erase busy. Erase command to ready 1001b: erase data. Erase command 1 to erase command 2 1111b: custom mode 1110b: custom mode for data access Others: Reserved
12	READ_EMPTY	**Empty page indication during read operation, include all data, FDM and parity for all sectors**
9	BUSY2READY	**It's read-only. This signal indicates NAND from busy to ready state and it will be reset after nfi_reset or write command/address.**
8	BUSY	**Synchronized busy signal from the NAND flash. It's read-only. This signal is sampled from NFI**
4	ACCESS_LOCK	**The access range is locked for erase or program .**
3	DATAW	**The NFI core is in data write mode.**
2	DATAR	**The NFI core is in data read mode.**
1	ADDR	**The NFI core is in address mode.**
0	CMD	**The NFI core is in command mode.**

1100D064 NFI_FIFOSTA NFI FIFO Status 00004040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WR_	WR_		WR_REMAIN					RD_F	RD_E		RD_REMAIN				
Type	RO	RO		RO					RO	RO		RO				
Reset	0	1		0	0	0	0	0	0	1		0	0	0	0	0

Bit(s)	Name	Description
15	WR_FULL	**Data FIFO full in burst write mode.**
14	WR_EMPTY	**Data FIFO empty in burst write mode.**
12:8	WR_REMAIN	**Data FIFO remaining byte number in burst write mode.**
7	RD_FULL	**Data FIFO full in burst read mode.**
6	RD_EMPTY	**Data FIFO empty in burst read mode.**
4:0	RD_REMAIN	**Data FIFO remaining byte number in burst read mode.**

1100D070 NFI_ADDRCNTR NFI Page Address Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEC_CNTR						SEC_ADDR									
Type	RO						RO									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	SEC_CNTR	**The sector count.**
9:0	SEC_ADDR	**The address count of 512 main data and spare data for each sector.**

1100D080 NFI_STRADDR NFI AHB Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STR_ADDR															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	STR_ADDR	**The start address of EMI for both read or write in DMA mode.** If start address of any sector data is not 4-byte aligned, the transfer will be automatically split into byte and word transaction by NFI DMA. Non 4-byte aligned data will be transferred in single-byte transaction. Non 16-byte aligned data will be transferred in single-word transaction. 16-byte aligned data will be transferred by 4 word incrementing bust if the NFI_CNFG->DMA_BURST_EN is enabled.

1100D084 NFI_BYTELEN NFI DMA Byte Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BUS_SEC_CNTR**						**BUS_SEC_ADDR**									
Type	RO						RO									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	BUS_SEC_CNTR	**The sector count.**
9:0	BUS_SEC_ADDR	**The address count of 512 main data and spare data for each sector.**

1100D090 NFI_CSEL NFI device select register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**CSEL**
Type																RW

Reset																0

Bit(s)	Name	Description
0	CSEL	**Chip select. The value defaults to 0.** 0: Device 1 is selected. 1: Device 2 is selected.

1100D094 NFI_IOCON NFI IO Control register 00000006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BRSTN					L2NW	L2NR	NLD_PD
Type									RW					RW	RW	RW
Reset									0	0	0	0		1	1	0

Bit(s)	Name	Description
7:4	BRSTN	**Maximum Burst Number for NAND read and writes. The unit is number of byte (8bits I/O) or double byte (16bits I/O)**
2	L2NW	**Enable 1T latency for the arbitration from LCD to NAND write operation, this is used to prevent bus contention between chip, NAND flash and LCD device.**
1	L2NR	**Enable 1T latency for the arbitration from LCD to NAND read operation, this is used to prevent bus contention between chip, NAND flash and LCD device.**
0	NLD_PD	**data bus pull down when no use.** 0: disable. 1: enable.

1100D0A0 NFI_FDM0L NFI Least FDM Data for Sector 0 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM0_3								FDM0_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM0_1								FDM0_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM0_3	**The 3-th FDM byte data for sector 0.**
23:16	FDM0_2	**The 2-th FDM byte data for sector 0.**
15:8	FDM0_1	**The 1-th FDM byte data for sector 0.**
7:0	FDM0_0	**The 0-th FDM byte data for sector 0.**

1100D0A4 NFI_FDM0M NFI Most FDM Data for Sector 0 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM0_7								FDM0_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM0_5								FDM0_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM0_7	**The 3-th FDM byte data for sector 0.**
23:16	FDM0_6	**The 2-th FDM byte data for sector 0.**
15:8	FDM0_5	**The 1-th FDM byte data for sector 0.**
7:0	FDM0_4	**The 0-th FDM byte data for sector 0.**

1100D0A8 NFI_FDM1L NFI Least FDM Data for Sector 1 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM1_3								FDM1_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM1_1								FDM1_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM1_3	**The 3-th FDM byte data for sector 1.**
23:16	FDM1_2	**The 2-th FDM byte data for sector 1.**
15:8	FDM1_1	**The 1-th FDM byte data for sector 1.**
7:0	FDM1_0	**The 0-th FDM byte data for sector 1.**

1100D0AC NFI_FDM1M NFI Most FDM Data for Sector 1 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM0_7								FDM0_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM0_5								FDM0_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM0_7	**The 7-th FDM byte data for sector 1.**
23:16	FDM0_6	**The 6-th FDM byte data for sector 1.**
15:8	FDM0_5	**The 5-th FDM byte data for sector 1.**
7:0	FDM0_4	**The 4-th FDM byte data for sector 1.**

Bit(s)	Name	Description

1100D0B0 NFI_FDM2L NFI Least FDM Data for Sector 2 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM0_3								FDM0_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM0_1								FDM0_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM0_3	**The 3-th FDM byte data for sector 2.**
23:16	FDM0_2	**The 2-th FDM byte data for sector 2.**
15:8	FDM0_1	**The 1-th FDM byte data for sector 2.**
7:0	FDM0_0	**The 0-th FDM byte data for sector 2.**

1100D0B4 NFI_FDM2M NFI Most FDM Data for Sector 2 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM0_7								FDM0_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM0_5								FDM0_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM0_7	**The 7-th FDM byte data for sector 2.**

Bit(s)	Name	Description
23:16	FDMo_6	**The 6-th FDM byte data for sector 2.**
15:8	FDMo_5	**The 5-th FDM byte data for sector 2.**
7:0	FDMo_4	**The 4-th FDM byte data for sector 2.**

1100D0B8 NFI_FDM3L NFI Least FDM Data for Sector 3 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMo_3								FDMo_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMo_1								FDMo_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMo_3	**The 3-th FDM byte data for sector 3.**
23:16	FDMo_2	**The 2-th FDM byte data for sector 3.**
15:8	FDMo_1	**The 1-th FDM byte data for sector 3.**
7:0	FDMo_0	**The 0-th FDM byte data for sector 3.**

1100D0BC NFI_FDM3M NFI Most FDM Data for Sector 3 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMo_7								FDMo_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMo_5								FDMo_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMo_7	**The 4-th FDM byte data for sector 3.**
23:16	FDMo_6	**The 6-th FDM byte data for sector 3.**
15:8	FDMo_5	**The 5-th FDM byte data for sector 3.**
7:0	FDMo_4	**The 4-th FDM byte data for sector 3.**

1100DoCo NFI_FDM4L NFI Least FDM Data for Sector 4 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMo_3								FDMo_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMo_1								FDMo_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMo_3	**The 3-th FDM byte data for sector 4.**
23:16	FDMo_2	**The 2-th FDM byte data for sector 4.**
15:8	FDMo_1	**The 1-th FDM byte data for sector 4.**
7:0	FDMo_0	**The 0-th FDM byte data for sector 4.**

1100DoC4 NFI_FDM4M NFI Most FDM Data for Sector 4 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMo_7								FDMo_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMo_5								FDMo_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMo_7	**The 7-th FDM byte data for sector 4.**
23:16	FDMo_6	**The 6-th FDM byte data for sector 4.**
15:8	FDMo_5	**The 5-th FDM byte data for sector 4.**
7:0	FDMo_4	**The 4-th FDM byte data for sector 4.**

1100D0C8 NFI_FDM5L NFI Least FDM Data for Sector 5 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMo_3								FDMo_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMo_1								FDMo_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMo_3	**The 3-th FDM byte data for sector 5.**
23:16	FDMo_2	**The 2-th FDM byte data for sector 5.**
15:8	FDMo_1	**The 1-th FDM byte data for sector 5.**
7:0	FDMo_0	**The 0-th FDM byte data for sector 5.**

1100D0CC NFI_FDM5M NFI Most FDM Data for Sector 5 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMo_7								FDMo_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMo_5								FDMo_4							
Type	RW								RW							

Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM0_7	**The 7-th FDM byte data for sector 5.**
23:16	FDM0_6	**The 6-th FDM byte data for sector 5.**
15:8	FDM0_5	**The 5-th FDM byte data for sector 5.**
7:0	FDM0_4	**The 4-th FDM byte data for sector 5.**

1100D0D0 NFI_FDM6L NFI Least FDM Data for Sector 6 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM0_3								FDM0_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM0_1								FDM0_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM0_3	**The 3-th FDM byte data for sector 6.**
23:16	FDM0_2	**The 2-th FDM byte data for sector 6.**
15:8	FDM0_1	**The 1-th FDM byte data for sector 6.**
7:0	FDM0_0	**The 0-th FDM byte data for sector 6.**

1100D0D4 NFI_FDM6M NFI Most FDM Data for Sector 6 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM0_7								FDM0_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM0_5								FDM0_4							

Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM0_7	**The 7-th FDM byte data for sector 6.**
23:16	FDM0_6	**The 6-th FDM byte data for sector 6.**
15:8	FDM0_5	**The 5-th FDM byte data for sector 6.**
7:0	FDM0_4	**The 4-th FDM byte data for sector 6.**

1100D0D8 NFI_FDM07L NFI Least FDM Data for Sector 7 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM7_3								FDM7_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM7_1								FDM7_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM7_3	**The 3-th FDM byte data for sector 7.**
23:16	FDM7_2	**The 2-th FDM byte data for sector 7.**
15:8	FDM7_1	**The 1-th FDM byte data for sector 7.**
7:0	FDM7_0	**The 0-th FDM byte data for sector 7.**

1100D0DC NFI_FDM7M NFI Most FDM Data for Sector 7 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM7_7								FDM7_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	FDM7_5								FDM7_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM7_7	**The 7-th FDM byte data for sector 7.**
23:16	FDM7_6	**The 6-th FDM byte data for sector 7.**
15:8	FDM7_5	**The 5-th FDM byte data for sector 7**
7:0	FDM7_4	**The 4-th FDM byte data for sector 7.**

1100D190 NFI_FIFODATA0 NFI FIFO Content Data 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA0	

1100D194 NFI_FIFODATA1 NFI FIFO Content Data 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA1	

1100D198 NFI_FIFODATA2 NFI FIFO Content Data 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA2	

1100D19C NFI_FIFODATA3 NFI FIFO Content Data 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA3	

1100D200 NFI_MCON NFI LCD Monitor Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BMCLR	BMSTR
Type															WO	RW
Reset															0	0

Bit(s)	Name	Description
1	BMCLR	**Clear NFI-LCD bandwidth monitor register counter**
0	BMSTR	**Enable NFI-LCD bandwidth monitor** 0: disable. 1: enable.

1100D204 NFI_TOTALCNT NFI LCD Monitor Total Cycle Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NFI_TOTALCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NFI_TOTALCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	NFI_TOTALCNT	**The total clock cycle count during enabling NFI-LCD bandwidth monitor**

1100D208 NFI_RQCNT NFI LCD Monitor Request Cycle Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NFI_RQCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NFI_RQCNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	NFI_RQCNT	**The request clock cycle count during enabling NFI-LCD bandwidth monitor**

1100D20C NFI_ACCNT NFI LCD Monitor Access Cycle Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NFI_ACCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NFI_ACCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	NFI_ACCNT	**The access clock cycle count during enabling NFI-LCD bandwidth monitor**

1100D220 NFI_DEBUG_CON1 NFI Debug register 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_CON													WBU	HWD	HWD
Type	RW													RW	RW	RW

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15:3	DEBUG_CON	
2	WBUF_EN	
1	HWDCM_SWCON_ON	**ECC clock gating control while nfiecc is idle and nand is busy** 1'b0: ECC clock gating disable, ECC clock will not be closed while NFI is working 1'b1: ECC clock gating enable, ECC clock will be closed while ECC is idle and nand is busy
0	HWDCM_SWCON_EN	**Hard ware DCM control enable,(this bit is not used in 6572)**

1100D224 NFI_MASTERSTA NFI Master Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**MAS_ADDR**			**MAS_RD**			**MAS_WR**			**MAS_RDDLY**		
Type					RO			RO			RO			RO		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:9	MAS_ADDR	**MAS_is in the Address phase of AHB protocol. In this phase, Bus gots the address data from Master.** 000b: There is no MAS in the Address phase of AHB protocol. 001b: NFI is in the Address pahse of AHB protocol. 010b: Auto-Correction is in the Address pahse of AHB protocol. 100b: ECC is in the Address pahse of AHB protocol.
8:6	MAS_RD	**MAS_is in the Read DATA phase of AHB protocol. In this phase, Bus returns the read data.**

Bit(s)	Name	Description
5:3	MAS_WR	**MAS_is in the Write DATA phase of AHB protocol. In this phase, Bus receives the write data.**
2:0	MAS_RDDLY	**MAS is in the Read DATA delay phase of AHB protocol. In this phase, NFI and ECC got the read back data**

1100D22C NFI_SECCUS_SIZE Enable bit for customized size for each sector 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SECCUS_SIZE_EN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CUS_SEC_SIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	SECCUS_SIZE_EN	**Enable Customized sector size. Note: The spare_size will be ignored if this feature Is enabled. Autofmt and ECC function will not work under this mode.**
12:0	CUS_SEC_SIZE	**The valid size range is 1 to 8187**

1100D230 NFI_SPIADDRCNTR NFI AHB Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													NF_TSF_SEC			
Type													RO			
Reset													0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				NF_TSF_ADDR												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:16	NF_TSF_SEC	**The register represents the start address for DMA to access EMI. These memory from the start address is used to put read data from NAND or write data to NAND in DMA mode**
12:0	NF_TSF_ADDR	

1100D234 NFI_SPIBYTELEN NFI DMA Byte Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BUS_TSF_SEC			
Type													RO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BUS_TSF_ADDR												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:16	BUS_TSF_SEC	**The register represents the current transfer length for DMA to access EMI.**
12:0	BUS_TSF_ADDR	

1100D500 SNF_MAC_CTL Serial nand flash mac mode control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												MAC_	SF_M	SF_T	WIP_	WIP

												]	_	]	A	
												(	]	(	]	
												-	]		Y	
												S				
												]				
												]				
Type												RW	RW	RW	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	MAC_XIO_SEL	**MAC mode for QPI/SPI setting** 0: SPI 1: QPI
3	SF_MAC_EN	**Switches the serial flash control to update the macro. Please set up this bit before triggering the update macro (It is suggested to run MAC mode in internal sysram code due to DIRECT/MAC cannot run at the same time. Another way to switch to hardware auto switch mode by setting up MAC_MASK_OP)** 0: MAC_MODE Disable 1: MAC MODE Enable (Direct read is forbidden when SF_MAC_EN = 1)
2	SF_TRIG	**Serial flash write macro trigger** 0: Disable 1: Enable (Fill command sequence I/O length before SF_TRIG)
1	WIP_READY	**WIP register status ready for access. WIP_READY exits due to asynchronous latency delay before flash responds to WIP** 0: WIP not ready for read 1: WIP ready for read (Check if WIP_READY = 1 before the next command sequence)
0	WIP	**Serial flash command write in process** 0: Flash update finished (Check if WIP = 0 before the next command sequence) 1: Not finished

1100D504 SNF_MAC_OUTL Serial nand flash mac mode output data length 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SNF_MAC_OUT_LENGTH							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SNF_MAC_OUT_LENGTH	**Serial flash write data length(unit: byte)**

1100D508 SNF_MAC_INL Serial nand flash mac mode input data length 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SNF_MAC_IN_LENGTH							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SNF_MAC_IN_LENGTH	**Serial flash read data length(unit: byte)**

1100D50C SNF_RD_CTL1 Serial nand flash read control 1 13000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PAGE_READ_CMD								PAGE_READ_ADDRESS							
Type	RW								RW							
Reset	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAGE_READ_ADDRESS															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	PAGE_READ_CMD	**Page read command setting**
23:0	PAGE_READ_ADDRESS	**Page Read Address**

1100D510 SNF_RD_CTL2 Serial nand flash read control 2 0000080B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DATA_READ_DUMMY				DATA_READ_CMD							
Type					RW				RW							
Reset					1	0	0	0	0	0	0	0	1	0	1	1

Bit(s)	Name	Description
11:8	DATA_READ_DUMMY	**Dummy Cycle;** when read from cache, setting the dummy cycles according to read command of datasheet.
7:0	DATA_READ_CMD	**Data Read command**

1100D514 SNF_RD_CTL3 Serial nand flash read control 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_READ_CMD_DUMMY_OUT				DATA_READ_ADDRESS											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	DATA_READ_CMD_DUMMY_OUT	**Data read command output in dummy cycle [3:0]**
11:0	DATA_READ_ADDRESS	**Data read address setting [11:0]**

1100D518 SNF_GF_CTL1 Serial nand flash get feature control 1 0FC00101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GF_CMD								GF_ADDR							
Type	RW								RW							
Reset	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GF_BUSY_MASK								GF_STATUS							
Type	RW								RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:24	GF_CMD	**Get Feature command setting**
23:16	GF_ADDR	**Get Feature address setting**

15:8	GF_BUSY_MASK	**Get Feature Status busy mask bits setting**
		Ex:
		flag[7:0] = get_feature_status[7:0] & get_feature_busy [7:0];
		If (flag[7:0] == 0) done;
		Else Continue;
		0: mask this bit. Do not check it
		1: check this bit

7:0	GF_STATUS	**Get Feature status result [7:0]**

1100D520 SNF_GF_CTL3 Serial nand flash mac mode control 000F0320

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LOOP_LIMIT			
Type													RW			

Reset													1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POOLING_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
19:16	LOOP_LIMIT	**Get Feature loop setting for status read and compare** NOTE: 4'b1111 for no limit setting
15:0	POOLING_CYCLE	**Polling cyce setting for standby period between issue Get Feature commands** Standby period = polling_cycle X base_time_slot Base_time_slot = spi-nand clock cycle X 128. Ex: spi-nand clock=100M, 1T=10ns, then base_time_slot = 1.28us. And the polling cycle value should be set to meet the Standby_period ~= spec time.

1100D524 SNF_PG_CTL1 Serial nand flash program control1 00100206

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PG_EXE_CMD							
Type									RW							
Reset									0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PG_LOAD_CMD								WRITE_EN_CMD							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
23:16	PG_EXE_CMD	**Program execute command [7:0]**
15:8	PG_LOAD_CMD	**Program load command [7:0]**
7:0	WRITE_EN_CMD	**Write Enable command [7:0]**

1100D528 SNF_PG_CTL2 Serial nand flash program control2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PG_LOAD_CMD_DUMMY_OUT								PG_LOAD_ADDR							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	PG_LOAD_CMD_DUMMY_OUT	**Program load command output in dummy cycle [3:0]**
7:0	PG_LOAD_ADDR	**Program load address [7:0]**

1100D52C SNF_PG_CTL3 Serial nand flash program control3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PG_EXE_ADDR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PG_EXE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	PG_EXE_ADDR	**Program execute address [23:0]**

1100D530 SNF_ER_CTL Serial nand flash erase control 0000D800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERASE_CMD															AUTO

Type	RW															RW
Reset	1	1	0	1	1	0	0	0								0

Bit(s)	Name	Description
15:8	ERASE_CMD	**Erase command setting [7:0]**
0	AUTO_ERASE_TRIGGER	**Auto Ease trigger bit**

1100D534 SNF_ER_CTL2 Serial nand flash erase control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERASE_ADDR	**Erase address setting [23:0]**

1100D538 SNF_MISC_CTL Serial nand flash MISC control 0400000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			MAC	SW_	SFIO	FIFO_RD_LTC		_4FIF	FBCL	SMPC	CLK_	PG_L		DATA_READ_MODE		

Type			RW	RW	RW	RW		RW	RW	RW	RW	RW		RW		
Reset			0	0	0	1	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SF2C	SF2C	SF2C			LATCH_LAT		PG_L	DATA		CS_DESELECT_CYC				
Type		RW	RW	RW			RW		RW	RW		RW				
Reset		0	0	0			0	0	0	0		0	1	0	1	0

Bit(s)	Name	Description
29	MACRO_RST_EN	**MACRO reset fifo enable**
28	SW_RST	**SW reset controller: 1 for reset on, 0 for reset off.**
27	SFIO_EN_SEL	**IO PAD Enable signal align with clock positive edge select**
26:25	FIFO_RD_LTC	**FIFO read latency**
24	_4FIFO_EN	**4Tap FIFO read enable**
23	FBCLK_SEL	**Feedback clock select**
22	SMPCK_INV	**Inner sample clock inverter select**
21	CLK_INV	**Output serial clock inverter select**
20	PG_LOAD_X4_EN	**Program load data x4 mode enable.**
18:16	DATA_READ_MODE	**Data Read mode select. Bit[1:0] for data mode, Bit[2] for IO mode.** 000:X1 data mode 001:X2 data mode

Bit(s)	Name	Description
		010:X4 data mode 011:Reserved 100:Reserved 101:Dual IO mode 110:Quad IO mode 111:Reserved
14	SF2CS_DUAL_EN	**Both CS1/CS2 enable/select for first/second SPI-nand device.**
13	SF2CS_SEL	**SF 2CS select for first/second SPI-nand device.**
12	SF2CS_EN	**SF 2CS enable for second SPI-nand device.**
9:8	LATCH_LAT	**Data read latch latency**
7	PG_LOAD_CUSTOM_EN	**Program load custom mode enable**
6	DATARD_CUSTOM_EN	**Data read custom mode enable**
4:0	CS_DESELECT_CYC	**CS deselect cycle setting**

1100D53C SNF_MISC_CTL2 Serial nand flash MISC control 2 02100210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					PROGRAM_LOAD_BYTE_NUM											
Type					RW											
Reset					0	0	1	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					READ_DATA_BYTE_NUM											
Type					RW											
Reset					0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
27:16	PROGRAM_LOAD_BYTE_NUM	**NOTE: Setting value should be sync with NFI Read/Write byte length.** if (NFI_SECCUS_SIZE.CUS_SEC_SIZE.SECCUS_SIZE_EN==0) {

Bit(s)	Name	Description
		(512 + PAGEFMT.spare_size) * NFI_CON.sec_num == Transfer Data Length == SNF_MISC_CTL2.PROGRAM_LOAD_BYTE_NUM == SNF_MISC_CTL2.READ_DATA_BYTE_NUM } else { (NFI_SECCUS_SIZE.CUS_SEC_SIZE) * NFI_CON.sec_num == Transfer Data Length == SNF_MISC_CTL2.PROGRAM_LOAD_BYTE_NUM == SNF_MISC_CTL2.READ_DATA_BYTE_NUM
11:0	READ_DATA_BYTE_NUM	

1100D540 SNF_DLY_CTL1 Serial nand flash delay control setting 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SFIO3_OUT_DLY								SFIO2_OUT_DLY					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			SFIO1_OUT_DLY										SFIO0_OUT_DLY			
Type			RW										RW			
Reset			0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
29:24	SFIO3_OUT_DLY	**Serial flash SFIO3 pin IO output delay setting**
21:16	SFIO2_OUT_DLY	**Serial flash SFIO2 pin IO output delay setting**
13:8	SFIO1_OUT_DLY	**Serial flash SFIO1 pin IO output delay setting**
3:0	SFIO0_OUT_DLY	**Serial flash SFIO3 pin IO output delay setting**

1100D544 SNF_DLY_CTL2 Serial nand flash delay control setting 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SFIO3_IN_DLY								SFIO2_IN_DLY					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			SFIO1_IN_DLY								SFIO0_IN_DLY					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
29:24	SFIO3_IN_DLY	**Serial flash SFIO3 pin IO input delay setting**
21:16	SFIO2_IN_DLY	**Serial flash SFIO2 pin IO input delay setting**
13:8	SFIO1_IN_DLY	**Serial flash SFIO1 pin IO input delay setting**
5:0	SFIO0_IN_DLY	**Serial flash SFIO3 pin IO input delay setting**

1100D548 SNF_DLY_CTL3 Serial nand flash control setting 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SFIFO_WR_EN_DLY_SEL										SFCS_DLY			
Type			RW										RW			
Reset			0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SFCK_OUT_DLY						SFCK_SAM_DLY					
Type					RW						RW					
Reset					0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
29:24	SFIFO_WR_EN_DLY_SEL	**Serial flash FIFO write enable delay select setting**
19:16	SFCS_DLY	**Serial flash SFCS pin IO output delay setting**
11:8	SFCK_OUT_DLY	**Serial flash CK pin IO output delay setting**
5:0	SFCK_SAM_DLY	**Serial flash sample clock delay setting**

1100D54C SNF_DLY_CTL4 Serial nand flash delay control setting 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SFCS2_DLY			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	SFCS2_DLY	**Serial flash SFCS2 pin IO output delay setting**

1100D550 SNF_STA_CTL1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			GF_L	CUS_	CUS_	AUTO	AUTO	AUTO		DATARD_STATE			PGREAD_STATE			PGEX
Type			RO	W1C	W1C	W1C	W1C	W1C		RO			RO			RO
Reset			0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PGEXE_STATE		PGLOAD_STATE			GF_STATE			BLKER_STATE			WRE	SPI_STATE			
Type	RO		RO			RO			RO			RO	RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	GF_LOOP_TIMEOUT	**Get Feature read status time out flag**
28	CUS_PG_DONE	**Custom program mode Clear setting and Status** Status read(R): Custom program mode done flag. Clear(W): Set 1 then Set 0 to clear this flag.
27	CUS_READ_DONE	**Custom read mode Clear setting and Status** Status read(R): Custom read mode done flag. Clear(W): Set 1 then Set 0 to clear this flag.
26	AUTO_PG_DONE	**Auto program mode Clear setting and Status** Status read(R): Auto program mode done flag. Clear(W): Set 1 then Set 0 to clear this flag.
25	AUTO_READ_DONE	**Auto read mode Clear setting and Status** Status read(R): Auto read mode done flag. Clear(W): Set 1 then Set 0 to clear this flag.
24	AUTO_BLRER_DONE	**Auto block erase mode Clear setting and Status** Status read(R): Auto block erase mode done flag. Clear(W): Set 1 then Set 0 to clear this flag.
22:20	DATARD_STATE	**State machine of custom read** 0: IDLE 1: CMD 2: ADDR1 3: ADDR2 4: DUMMY 5: DATA 6: BUFOUT 7: WAIT
19:17	PGREAD_STATE	**State machine of auto read** 0: IDLE

Bit(s)	Name	Description
		1: CMD 2: ADDR1 3: ADDR2 4: ADDR3
16:14	PGEXE_STATE	**State machine of program execution** 0: IDLE 1: CMD 2: ADDR1 3: ADDR2 4: ADDR3
13:11	PGLOAD_STATE	**State machine of program load** 0: IDLE 1: CMD 2: ADDR1 3: ADDR2 4: BUFIN 5: DATA
10:8	GF_STATE	**State machine of get feature** 0: IDLE 1: GF_CMD 2: GF_ADDR 3: GF_DATA 4: GF_CMP 5: GF_WAIT
7:5	BLKER_STATE	**State machine of auto block erase** 0: IDLE 1: CMD

Bit(s)	Name	Description
		2: ADDR1 3: ADDR2 4: ADDR3
4	WREN_STATE	**State machine of write enable** 0: IDLE 1: CMD
3:0	SPI_STATE	**State machine SPI main Controller** 0:IDLE 1: Write Enable 2: Block Erase 3: Get Feature 4: Program Load 5: Program Execution 6: Page Read 7: Custom Data Read

1100D554 SNF_STA_CTL2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DATARD_BYTE_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PGLOAD_BTTE_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DATARD_BYTE_CNT	**Data Read Transfer byte count**

Bit(s)	Name	Description
12:0	PGLOAD_BTTE_CNT	**Program Load Transfer byte count**

1100D558 SNF_STA_CTL3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										GF_BASE_CNT						
Type										RO						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GF_WAIT_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
22:16	GF_BASE_CNT	**Get feature base counter**
15:0	GF_WAIT_CNT	**Get feature wait counter** When GF_BASE_CNT==8'hff, GF_WAIT_CNT plus 1; When GF_WAIT_CNT= Polling_Cycle, issue get feature command.

1100D55C SNF_SNF_CNFG SPI/Parallel NAND Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SPI_
Type																RW
Reset																0

Bit(s)	Name	Description
0	SPI_MODE	**Switch for Parallel NAND or Serial NAND** 0: NFI 1: SPI NAND

1100D560 SNF_DEBUG_SEL DEBUG MUX Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_SEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DEBUG_SEL	

Module name: NFIECC Base address: (+1100e000h)

Address	Name	Width	Register Function
1100E000	NFIECC_ENCCON	16	NFIECC Encoder Control Register
1100E004	NFIECC_ENCCNFG	32	NFIECC Configure Register
1100E008	NFIECC_ENCDIADDR	32	NFIECC Encoder DI Memory Address Register
1100E00C	NFIECC_ENCIDLE	16	NFIECC Encoder Idle Status Register
1100E010	NFIECC_ENCPAR0	32	NFIECC Parity0 Register
1100E014	NFIECC_ENCPAR1	32	NFIECC Parity1 Register
1100E018	NFIECC_ENCPAR2	32	NFIECC Parity2 Register
1100E01C	NFIECC_ENCPAR3	32	NFIECC Parity3 Register
1100E020	NFIECC_ENCPAR4	32	NFIECC Parity4 Register
1100E024	NFIECC_ENCPAR5	32	NFIECC Parity5 Register
1100E028	NFIECC_ENCPAR6	32	NFIECC Parity6 Register
1100E02C	NFIECC_ENCSTA	32	NFIECC Encoder Status Register
1100E030	NFIECC_ENCIRQEN	16	NFIECC Encoder IRQ enable Register
1100E034	NFIECC_ENCIRQSTA	16	NFIECC Encoder IRQ status Register
1100E080	NFIECC_PIO_DIRDY	16	NFIECC PIO Data Ready Register
1100E084	NFIECC_PIO_DI	32	NFIECC PIO Data Register

Address	Name	Width	Register Function
1100E100	NFIECC_DECCON	16	NFIECC Decoder Control Register
1100E104	NFIECC_DECCNFG	32	NFIECC Decoder Configure Register
1100E108	NFIECC_DECDIADDR	32	NFIECC Decoder DI Memory Address Register
1100E10C	NFIECC_DECIDLE	16	NFIECC Decoder Idle Status Register
1100E110	NFIECC_DECFER	16	NFIECC Decoder Found Error Status Register
1100E114	NFIECC_DECENUM0	32	NFIECC Decode Error Number Register
1100E118	NFIECC_DECENUM1	32	
1100E11C	NFIECC_DECDONE	16	NFIECC Decoder Error Status Register
1100E120	NFIECC_DECEL0	32	NFIECC Decoder Error location0 Register
1100E124	NFIECC_DECEL1	32	NFIECC Decoder Error Location1 Register
1100E128	NFIECC_DECEL2	32	NFIECC Decoder Error Location2 Register
1100E12C	NFIECC_DECEL3	32	NFIECC Decoder Error Location3 Register
1100E130	NFIECC_DECEL4	32	NFIECC Decoder Error Location4 Register
1100E134	NFIECC_DECEL5	32	NFIECC Decoder Error Location5 Register
1100E138	NFIECC_DECEL6	32	NFIECC Decoder Error Location6 Register
1100E13C	NFIECC_DECEL7	32	NFIECC Decoder Error Location6 Register
1100E140	NFIECC_DECIRQEN	16	NFIECC Decoder IRQ enable Register
1100E144	NFIECC_DECIRQSTA	16	NFIECC Decoder IRQ status Register
1100E148	NFIECC_FDMADDR	32	NFIECC FDM Register Address
1100E14C	NFIECC_DECFSM	32	NFIECC Decoder FSM
1100E150	NFIECC_SYNSTA	32	NFIECC Syndrome Status Register
1100E154	NFIECC_NFIDIDECNFIDI	32	NFIECC NFI input dataNFI input data Register
1100E158	NFIECC_SYN0	32	NFIECC Syndrom Register

1100E000 NFIECC_ENCCON NFIECC Encoder Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ENC_
Type																RW
Reset																0

Bit(s)	Name	Description
0	ENC_EN	**indicates the enable in NFI mode and start to work in AHB mode. In AHB mode, parity bits is remained in the PAR0~PAR4 register field until the ENC_EN is deasserted to 0.**

Bit(s)	Name	Description
		0: means disable the Encode block. 1: means enable the Encode block. In AHB mode, the Encoder starts to fetch data when the register changes from 0 to 1. In NFI mode, the register enables the Encode block, and then the Encoder module waits start signal and data from NFI.

1100E004 NFIECC_ENCCNFG NFIECC Configure Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ENC_MS												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ENC_			ENC_MODE			ENC_TNUM		
Type								RW			RW			RW		
Reset								0			0	0		0	0	0

Bit(s)	Name	Description
28:19	ENC_MS	**indicates the total bit size of message block including main data and control(FDM) data in the NFI mode. The spare_ECC_num parameter in old version has been merged into the message block_size parameter. If the block_size is equal to zero, the NFIECC do nothing.** The acceptable coded block size, which includes data and parity bits size, is 1~8191bits. Different ENC_TNUM results in different parity bits, and also results in different maximum message block size.
8	ENC_BURST_EN	**indicates the burst enalbe.** 0: means DMA mode uses single read. 1: means DMA mode uses burst read.

Bit(s)	Name	Description
5:4	ENC_MODE	**indicates the data source from access through AHB bus or from NFI.** 00b: means source data from access through Bus. (DMA mode) 01b: means source data from NFI module. (NFI mode) 10b: means source data is written by MCU. (PIO mode) 11b: reserved mode.
2:0	ENC_TNUM	**indicates the correct capability in one block size. (Remove)** 0: means the NFIECC is capable of correct 4 bits in one block size. 1: means the NFIECC is capable of correct 6 bits in one block size. 2: means the NFIECC is capable of correct 8 bits in one block size. 3: means the NFIECC is capable of correct 10 bits in one block size. 4: means the NFIECC is capable of correct 12 bits in one block size. 5: means the NFIECC is capable of correct 14 bits in one block size. 6: means the NFIECC is capable of correct 16 bits in one block size.

1100E008 NFIECC_ENCDIADDR NFIECC Encoder DI Memory Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_DIADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_DIADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	ENC_DIADDR	**indicates the memory address of input data to Encoder block in AHB mode. (4-Byte align)**

1100E00C NFIECC_ENCIDLE NFIECC Encoder Idle Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ENC_
Type																RO
Reset																0

Bit(s)	Name	Description
0	ENC_IDLE	**indicates the Encode block in idle state and ready for new message block.** 0: means the Encode block is under working. 1: means the Encode block is in Idle state and available for new message block.

1100E010 NFIECC_ENCPAR0 NFIECC Parity0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR0	**indicates the highest order of output parity bits and the bit 0 is the highest order of parity bit. The PAR0~PAR4 register is remain the last message block parity bits until ENC_EN is deasserted. The parity bits should append after main data by order of {PAR0[31:0], PAR1[31:0], PAR2[31:0], PAR3[31:0], PAR4[31:4], 4'b0}, The redundant bit of parity bit will be padded by 0.**

1100E014 NFIECC_ENCPAR1 NFIECC Parity1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR1	**indicates the parity bits and the bit 0 is the highest order of parity bit.**

1100E018 NFIECC_ENCPAR2 NFIECC Parity2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR2	**indicates the parity bits and the bit 0 is the highest order of parity bit.**

Bit(s)	Name	Description

1100E01C NFIECC_ENCPAR3 NFIECC Parity3 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR3	**indicates the parity bits and the bit 0 is the highest order of parity bit.**

1100E020 NFIECC_ENCPAR4 NFIECC Parity4 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR4	**indicates the parity bits and the bit 0 is the highest order of parity bit.**

1100E024 NFIECC_ENCPAR5 NFIECC Parity5 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR5															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR5	**indicates the parity bits and the bit 0 is the highest order of parity bit.**

1100E028 NFIECC_ENCPAR6 NFIECC Parity6 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR6	**indicates the parity bits and the 31 is the highest order of parity bit.**

1100E02C NFIECC_ENCSTA NFIECC Encoder Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				COUNT_MS												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														ENC_FSM		
Type														RO		
Reset														0	0	0

Bit(s)	Name	Description
28:19	COUNT_MS	**indicates the remaining un-processing message bits.**
2:0	ENC_FSM	**indicates encoder finite state machine state** 3'd1: IDLE 3'd2: DATA 3'd4: DONE

1100E030 NFIECC_ENCIRQEN NFIECC Encoder IRQ enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ENC_
Type																RW
Reset																0

Bit(s)	Name	Description
0	ENC_IRQEN	**Encoder IRQ mask: triggered when Encoder operation is completed.** 0: Disable 1: Enable

1100E034 NFIECC_ENCIRQSTA NFIECC Encoder IRQ status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ENC_
Type																RC
Reset																0

Bit(s)	Name	Description
0	ENC_IRQSTA	**indicates interrupt status for Encoder processing.** 0: No interrupt is generated. 1: An interrupt is pending and waiting for service. Active when Encoder processing is done.

1100E080 NFIECC_PIO_DIRDY NFIECC PIO Data Ready Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**PIO_**
Type																RO
Reset																0

Bit(s)	Name	Description
0	PIO_DI_RDY	**indicates the PIO mode (Encoder/Decoder) is ready for input data.** 0: ECC is busy. During busy state, NFIECC_PIO_DI should not be over-write.

Bit(s)	Name	Description
		1: ECC is ready for input data. In PIO mode, write next PIO_DI when pio_di_rdy is equal to 1.

1100E084 NFIECC_PIO_DI NFIECC PIO Data Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_DI															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_DI															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PIO_DI	**indicates the PIO mode data input.**

1100E100 NFIECC_DECCON NFIECC Decoder Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DEC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	DEC_EN	**indicates the enable in NFI mode and start to work in AHB mode. In AHB mode, the decode-status FER and error number registers and error location registers will be reset to 0 when DEC_EN is deasserted.** 0: means disable the Decode block.

Bit(s)	Name	Description
		1: means enable the Decode block. In AHB mode, the Decoder starts to fetch data when the register changes from 0 to 1. In NFI mode, the register enables the Decode block, and then the Decoder module waits start signal and data from NFI.

1100E104 NFIECC_DECCNFG NFIECC Decoder Configure Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEC_EMPTY_EN			DEC_CS												
Type	RW			RW												
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEC_CON					DEC_CS			DEC_MODE			DEC_TNUM		
Type			RW					RW			RW			RW		
Reset			0	0				0			0	0		0	0	0

Bit(s)	Name	Description
31	DEC_EMPTY_EN	**indicates the Decoder automatically detects the empty source data and by pass the auto-correction block (data are all equal to 1). (ignore in AHB_mode)** 0: means disenable the detection of empty source data. 1: means enable the detection of empty source data.
28:16	DEC_CS	**indicates the total bit size of coded block including protected data and parity bits. The acceptable coded block size is 1~8191bits. If the coded block size is**

Bit(s)	Name	Description
		equal to zero, the decoder does nothing. The detail figure shows in Figure 2.
13:12	DEC_CON	**indicates the bypass configuration in decoding processor.** 0: is reserved 1: means only active syndrome calculator for error detecting purpose. ECC reports DONE and FER status after syndrome calculator is done. 2: means error-correction module is bypassed for being aware of error location purpose. ECC reports DONE, FER, EL and ERRNUM status after Chien search is done. 3: means the ECC processor decoded data and auto-correction error data. The data address is signaled by DEC_DIADDR register in AHB mode and NFI_DIADDR in NFI mode. ECC reports DONE, FER, EL and ERRNUM status after error-correction is done.
8	DEC_BURST_EN	**indicates the burst enalbe.** 0: means DMA mode uses single read. 1: means DMA mode uses burst read.
5:4	DEC_MODE	**indicates the data source from access AHB bus or from NFI.** 00b: means source data from access through Bus. (DMA mode) 01b: means source data from NFI module. (NFI mode) 10b: means source data is written by MCU. (PIO mode) 11b: Reserved mode.
2:0	DEC_TNUM	**indicates the correct capability in one block size.** 0: means the Decoder is capable of correct 4 bits in one block size. 1: means the Decoder is capable of correct 6 bits in one block size. 2: means the Decoder is capable of correct 8 bits in one block size. 3: means the NFIECC is capable of correct 10 bits in one block size. 4: means the NFIECC is capable of correct 12 bits in one block size.

Bit(s)	Name	Description

1100E108 NFIECC_DECDIADDR NFIECC Decoder DI Memory Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEC_DIADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEC_DIADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	DEC_DIADDR	**indicates the memory address of input data to the Decoder block in AHB mode. (4-Byte align).**

1100E10C NFIECC_DECIDLE NFIECC Decoder Idle Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DEC_
Type																RO
Reset																0

Bit(s)	Name	Description
0	DEC_IDLE	**indicates the Decode block is in idle state and ready for new coded block.** 0: means the Decode block is under working.

Bit(s)	Name	Description
		1: means the Decode block is in idle state and available for new coded block.

1100E110 NFIECC_DECFER NFIECC Decoder Found Error Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FER7	FER6	FER5	FER4	FER3	FER2	FER1	FER0
Type									RO	RO	RO	RO	RO	RO	RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	FER7	**indicates the error found or not in the coded block. The FER numbered by NFI sector number in NFI mode, otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode.** 0: means there is no error detected in the coded block. 1: means there is(are) error(s) detected in the coded block.
6	FER6	**indicates the error found or not in the coded block. The FER numbered by NFI sector number in NFI mode, otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode.** 0: means there is no error detected in the coded block. 1: means there is(are) error(s) detected in the coded block.
5	FER5	**indicates the error found or not in the coded block. The FER numbered by NFI sector number in NFI mode, otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode.** 0: means there is no error detected in the coded block. 1: means there is(are) error(s) detected in the coded block.

Bit(s)	Name	Description
4	FER4	**indicates the error found or not in the coded block. The FER numbered by NFI sector number in NFI mode, otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode.** 0: means there is no error detected in the coded block. 1: means there is(are) error(s) detected in the coded block.
3	FER3	**indicates the error found or not in the coded block. The FER numbered by NFI sector number in NFI mode, otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode.** 0: means there is no error detected in the coded block. 1: means there is(are) error(s) detected in the coded block.
2	FER2	**indicates the error found or not in the coded block. The FER numbered by NFI sector number in NFI mode, otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode.** 0: means there is no error detected in the coded block. 1: means there is(are) error(s) detected in the coded block.
1	FER1	**indicates the error found or not in the coded block. The FER numbered by NFI sector number in NFI mode, otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode.** 0: means there is no error detected in the coded block. 1: means there is(are) error(s) detected in the coded block.
0	FER0	**indicates the error found or not in the coded block. The FER numbered by NFI sector number in NFI mode, otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode.** 0: means there is no error detected in the coded block. 1: means there is(are) error(s) detected in the coded block.

1100E114 NFIECC_DECENUM0 NFIECC Decode Error Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name													ERRNUM3			
Type													RO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERRNUM7	ERRNUM2					ERRNUM1						ERRNUM0			
Type	RO	RO					RO						RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:15	ERRNUM3	**indicates the error numbers of coded block in one start signal. 4'hf means the error is uncorrectable.** But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
14:10	ERRNUM2	**indicates the error numbers of coded block in one start signal. 4'hf means the error is uncorrectable.** But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
9:5	ERRNUM1	**indicates the error numbers of coded block in one start signal. 4'hf means the error is uncorrectable.** But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
4:0	ERRNUM0	**indicates the error numbers of coded block in one start signal. 4'hf means the error is uncorrectable.** But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.

1100E118 NFIECC_DECENUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													ERRNUM7			
Type													RO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	ERR	ERRNUM6					ERRNUM5					ERRNUM4				
Type	RO	RO					RO					RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:15	ERRNUM7	**indicates the error numbers of coded block in one start signal. 4'hf means the error is uncorrectable.** But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
14:10	ERRNUM6	**indicates the error numbers of coded block in one start signal. 4'hf means the error is uncorrectable.** But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
9:5	ERRNUM5	**indicates the error numbers of coded block in one start signal. 4'hf means the error is uncorrectable.** But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
4:0	ERRNUM4	**indicates the error numbers of coded block in one start signal. 4'hf means the error is uncorrectable.** But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.

1100E11C NFIECC_DECDONE NFIECC Decoder Error Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DONE7	DONE6	DONE5	DONE4	DONE3	DONE2	DONE1	DONE0
Type									RO	RO	RO	RO	RO	RO	RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	DONE7	**indicates the Decoding procedure is done.** 0: means the Decode block is under working. 1: means the Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning. Detail of the definitions show in the Table.
6	DONE6	**indicates the Decoding procedure is done.** 0: means the Decode block is under working. 1: means the Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning. Detail of the definitions show in the Table.
5	DONE5	**indicates the Decoding procedure is done.** 0: means the Decode block is under working. 1: means the Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning. Detail of the definitions show in the Table.
4	DONE4	**indicates the Decoding procedure is done.** 0: means the Decode block is under working. 1: means the Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning. Detail of the definitions show in the Table.
3	DONE3	**indicates the Decoding procedure is done.** 0: means the Decode block is under working. 1: means the Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning. Detail of the definitions show in the Table.
2	DONE2	**indicates the Decoding procedure is done.** 0: means the Decode block is under working. 1: means the Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning. Detail of the definitions show in the Table.
1	DONE1	**indicates the Decoding procedure is done.**

Bit(s)	Name	Description
		0: means the Decode block is under working. 1: means the Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning. Detail of the definitions show in the Table.
0	DONE0	**indicates the Decoding procedure is done.** 0: means the Decode block is under working. 1: means the Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning. Detail of the definitions show in the Table.

1100E120 NFIECC_DECEL0 NFIECC Decoder Error location0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DEC_EL1												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DEC_EL0												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DEC_EL1	**indicates the error location 1 of the decoding result.**
12:0	DEC_EL0	**indicates the error location 0 of the decoding result. The EL remains until the DEC_EN is deasserted to 0 in both AHB and NFI mode. When the error number is less than 12, error location registers will be filled from DEC_EL0, and the redundant register fields remain 0.**

1100E124 NFIECC_DECEL1 NFIECC Decoder Error Location1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DEC_EL3												
Type				RO												

Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**DEC_EL2**												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DEC_EL3	**indicates the error location 3 of the decoding result.**
12:0	DEC_EL2	**indicates the error location 2 of the decoding result.**

1100E128 NFIECC_DECEL2 NFIECC Decoder Error Location2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**DEC_EL5**												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**DEC_EL4**												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DEC_EL5	**indicates the error location 5 of the decoding result.**
12:0	DEC_EL4	**indicates the error location 4 of the decoding result.**

1100E12C NFIECC_DECEL3 NFIECC Decoder Error Location3 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**DEC_EL7**												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**DEC_EL6**												
Type				RO												

Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DEC_EL7	**indicates the error location 7 of the decoding result.**
12:0	DEC_EL6	**indicates the error location 6 of the decoding result.**

1100E130 NFIECC_DECEL4 NFIECC Decoder Error Location4 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DEC_EL9												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DEC_EL8												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DEC_EL9	**indicates the error location 9 of the decoding result.**
12:0	DEC_EL8	**indicates the error location 8 of the decoding result.**

1100E134 NFIECC_DECEL5 NFIECC Decoder Error Location5 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DEC_EL11												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DEC_EL10												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DEC_EL11	**indicates the error location 11 of the decoding result.**
12:0	DEC_EL10	**indicates the error location 10 of the decoding result.**

1100E138 NFIECC_DECEL6 NFIECC Decoder Error Location6 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DEC_EL13												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DEC_EL12												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DEC_EL13	**indicates the error location 13 of the decoding result.**
12:0	DEC_EL12	**indicates the error location 12 of the decoding result.**

1100E13C NFIECC_DECEL7 NFIECC Decoder Error Location6 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DEC_EL15												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DEC_EL14												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DEC_EL15	**indicates the error location 15 of the decoding result.**

Bit(s)	Name	Description
12:0	DEC_EL14	**indicates the error location 14 of the decoding result.**

1100E140 NFIECC_DECIRQEN NFIECC Decoder IRQ enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DEC_
Type																RW
Reset																0

Bit(s)	Name	Description
0	DEC_IRQEN	**Decoder IRQ mask: triggered when Decoder operation is completed.** 0: Disable 1: Enable

1100E144 NFIECC_DECIRQSTA NFIECC Decoder IRQ status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DEC_

Type																RC
Reset																0

Bit(s)	Name	Description
0	DEC_IRQSTA	**indicates Interrupt status for Decoder processing.** 0: No interrupt is generated. 1: An interrupt is pending and waiting for service. Active when Decoder processing is done.

1100E148 NFIECC_FDMADDR NFIECC FDM Register Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**FDM_ADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FDM_ADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FDM_ADDR	**indicates the APB register address of FDM data in NFI module.**

1100E14C NFIECC_DECFSM NFIECC Decoder FSM 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		**AUTOC_FSM**											**CHIEN_FSM**			
Type		RW											RO			
Reset		0	0	0	0	0	0	1					0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**BMA_FSM**								**SYN_FSM**			
Type					RW								RO			
Reset					0	0	0	1					0	0	0	1

Bit(s)	Name	Description
30:24	AUTOC_FSM	**indicates the status of auto-correction stage.** 7'd1: IDLE 7'd2: COUNTE 7'd4: READ_PRE 7'd8: READ 7'd16: WRITE_PRE 7'd32: WRITE 7'd64: DONE
19:16	CHIEN_FSM	**indicates the status of Chien search stage.** 4'd1: IDLE 4'd2: BUSY 4'd4: DONE 4'd8: WAITAC
11:8	BMA_FSM	**indicates the status of BMA stage.** 4'd1: IDLE 4'd2: BUSY 4'd4: DONE
3:0	SYN_FSM	**indicates the status of syndrome stage.** 4'd1: IDLE 4'd2: BUSY 4'd4: DONE 4'd8: WAITIN

1100E150 NFIECC_SYNSTA NFIECC Syndrome Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYN_SNUM						DIBW							NFI_SEC_NUM		
Type	RO						RO							RO		

Reset	0	0	0				0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NFI_		SYN_COUNT_CS													
Type	RO		RO													
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:29	SYN_SNUM	**indicates the sector number recorded by syndrome.**
25:20	DIBW	**indicates input bandwidth.**
18:16	NFI_SEC_NUMNFI_SEC_NUM	**indicates the sector number from NFI.**
15	NFI_STR_SET	**indicates the NFI_STR signal from NFI.**
13:0	SYN_COUNT_CS	**indicates the remaining un-processing coded block bits.**

1100E154 NFIECC_NFIDIDECNFIDI NFIECC NFI input dataNFI input data 00000000
Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NFI_DINFI_DI															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NFI_DINFI_DI															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	NFI_DINFI_DI	**indicates the latest 4 byte input data from nfi.**

1100E158 NFIECC_SYN0 NFIECC Syndrom Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DEC_SYN3												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DEC_SYN1												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DEC_SYN3	**informs the syndrome 3 from syndrome calculator.**
12:0	DEC_SYN1	**informs the syndrome 1 from syndrome calculator.**

1.21 IR-TX

1.21.1 IR transmitter for 3D shutter glasses

1.21.1.1 Introduction

The infrared remote control transmitter module supports realD 3D shutter glasses of IR transmission protocol. This IR transmitter output both of the IR baseband and modulated signals. The IR signal's sync leading pulse, bit time, modulation carrier frequency, and modulation carrier duty cycle are all programmable. This hardware provides up to 32 bits with 1MHz ~ 1Hz bit rate in a transaction. There are independent 24-bit registers to set data high and data low period.
For realD 3D glasess IR protocol, the bit rate is 26.2kbps and the data definition as below figure shows. The datum '1' is purely logic high in a period; on the other hand, the datum '0' is purely logic low in a period. The unit of value in L0H/L0L/L1H/L1L registers is 27MHz (37.07ns). In this example, we should set L0L/L1H = 0x406 (27M/26.2) and set L0H/L1L = 0x0.

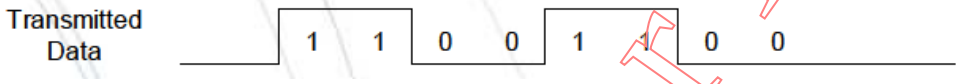


Figure 1-18 realD IR command

1.21.2 IR transmitter for general purpose

1.21.2.1 Introduction

The infrared remote control transmitter module supports NEC, REC-80, SONY pulse-coded signal and Philips RC5, RC6 IR transmission protocol. This IR transmitter output both of the IR baseband and modulated signals. The IR signal's sync leading pulse, bit time, modulation carrier frequency, and modulation carrier duty cycle are all programmable.

For NEC protocol, bit 0 is indicated as 1T high and 1T low, and bit 1 is indicated as 1T high and 3T low. The reference T value for NEC protocol is 0.562ms. For RC5 and RC6 protocol, bi-phase encoding is adopted, and bit time is 2T, but reference T = 1.778ms and 0.889ms respectively. For REC-80 protocol, bit 1 is indicated as 1T high and 2T low and bit 0 is indicated as 1T high and 3T low. For SONY pulse-coded signal, bit 1 is indicated as 1T high and 1T low and bit 0 is indicated as 2T high and 1T low.Except RC5 and RC6, the leading sync pulse can be defined by the registers SYNCH and SYNCL.

The default carrier frequency is 39KHz and carrier waveform duty cycle is 33%. Users can program the registers CWT and CDT to adjust the carrier frequency and carrier duty factor. For design flexibility, we create a user create mode. When this mode is set, after the leading sync pulse, the IRTX base-band signal output is only the contents of the shift registers IRTX_R0 ~ IRTX_R11. User can program these registers' value to constitute a suitable IR protocol signal. Below figure is the infrared remote control transmitter block diagram.

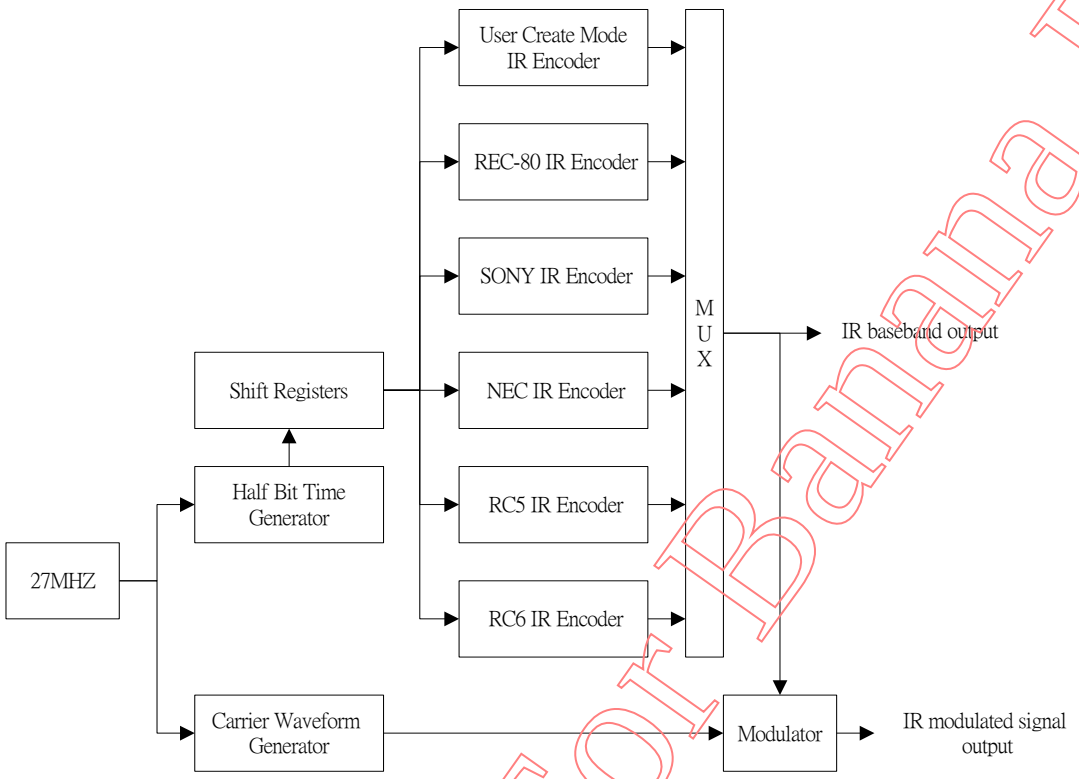


Figure 1-19 infrared remote control transmitter block diagram

1.21.3 Register Definition

Module name: irtx Base address: (+11011000h)

Address	*Name*	*Width*	*Register Function*
11011000	**IRTXCFG**	32	**IRTX CONFIGURATION REGISTER**
11011004	**IRTXD0**	32	**IRTX TRANSMISSION DATA 0 REGISTER)**
11011008	**IRTXD1**	32	**IRTX TRANSMISSION DATA 1 REGISTER**
1101100C	**IRTXD2**	32	**IRTX TRANSMISSION DATA 2 REGISTER**
11011010	**IRTX_L0H**	32	**IRTX LOGIC 0 HIGH PERIOD REGISTER**
11011014	**IRTX_L0L**	32	**IRTX LOGIC 0 LOW PERIOD REGISTER**
11011018	**IRTX_L1H**	32	**IRTX LOGIC 1 HIGH PERIOD REGISTER**
1101101C	**IRTX_L1L**	32	**IRTX LOGIC 1 LOW PERIOD REGISTER**
11011020	**IRTXSYNCH**	32	**IRTX SYNC HIGH PERIOD REGISTER**
11011024	**IRTXSYNCL**	32	**IRTX SYNC LOW PERIOD REGISTER**
11011028	**IRTXMT**	32	**IRTX MODULATION PARAMETER REGISTER**
1101102C	**IRTX_INT_CLR**	32	**IRTX INTERRUPT CLEAR REGISTER**
11011030	**IRTX_SWM_BP**	32	**IRTX SOFTWARE MODE BASE PERIOD REGISTER**
11011034	**IRTX_SWM_PW0**	32	**IRTX SOFTWARE MODE PULSE WIDTH 0 REGISTER**
11011038	**IRTX_SWM_PW1**	32	**IRTX SOFTWARE MODE PULSE WIDTH 1 REGISTER**

Address	Name	Width	Register Function
1101103C	IRTX_SWM_PW2	32	IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER
11011040	IRTX_SWM_PW3	32	IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER
11011044	IRTX_SWM_PW4	32	IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER
11011048	IRTX_SWM_PW5	32	IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER
1101104C	IRTX_SWM_PW6	32	IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER
11011050	IRTX_SWM_PW7	32	IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER
11011054	IRTX_SWM_PW8	32	IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER
11011058	IRTX_SWM_PW9	32	IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER
1101105C	IRTX_SWM_PW10	32	IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER
11011060	IRTX_SWM_PW11	32	IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER
11011064	IRTX_SWM_PW12	32	IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER
11011068	IRTX_SWM_PW13	32	IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER
1101106C	IRTX_SWM_PW14	32	IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER
11011070	IRTX_SWM_PW15	32	IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER
11011074	IRTX_SWM_PW16	32	IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER

11011000 IRTXCFG IRTX CONFIGURATION REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															IRTX_SWO	OPEN_DRAIN
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_INV	IRTX_BITNUM							IRTX_IRINV	IRTX_IROS	IRTX_RODR	IRTX_BODR	IRTX_MODE			IRTX_STRT
Type	RW	RW							RW	RW	RW	RW	RW			RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[931] Bit(s)	[932] Name	[933] Description
17	IRTX_SWO	**Software output bit** When the IRTX output protocol is set to software mode, the IR output is the same as SWO.
16	OPEN_DRAIN	**Reserved**

[931] Bit(s)	[932] Name	[933] Description
15	DATA_INV	**IR N inverter** Set this bit as '1' to invert IR data waveform only
14:8	IRTX_BITNUM	**Bit Number** Number of IR bits will be transmitted
7	IRTX_IRINV	**IR inverter** Set this bit as '1' to invert IR output
6	IRTX_IROS	**IR output select** 0: IR output is IRTX baseband signal 1: IR output is IRTX modulated signal
5	IRTX_RODR	**Register transmission order** 0: IRTX_R0 first, IRTX_R11 last (R0, R1 ~ R11) 1: IRTX_R11 first, IRTX_R0 last (R11, R10 ~R0)
4	IRTX_BODR	**Bit transmission order** 0: MSB first, LSB last (ex. R0[7], R0[6] ~ R0[0]) 1: LSB first, MSB last (ex. R0[0], R0[1] ~ R0[7])
3:1	IRTX_MODE	**IR output protocol** 0: pulse-width coded protocol 1: RC5 protocol 2: RC6 protocol 3: software mode 4: software pulse-width mode
0	IRTX_STRT	**IR trigger bit** 0: IR code transfer completed 1: Start to transfer IR code When IRTX output protocol is set to software mode, this bit is set as 0 to terminate IR transmission.

11011004 ***IRTXD0*** ***IRTX TRANSMISSION DATA 0 REGISTER)*** ***00000000***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_R3								IRTX_R2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_R1								IRTX_R0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[934] Bit(s)	[935] Name	[936] Description
31:24	IRTX_R3	**IRTX byte 3**
23:16	IRTX_R2	**IRTX byte 2**
15:8	IRTX_R1	**IRTX byte 1**
7:0	IRTX_R0	**IRTX byte 0**

11011008 ***IRTXD1*** ***IRTX TRANSMISSION DATA 1 REGISTER*** ***00000000***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_R7								IRTX_R6							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_R5								IRTX_R4							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[937] Bit(s)	[938] Name	[939] Description
31:24	IRTX_R7	**IRTX byte 7**
23:16	IRTX_R6	**IRTX byte 6**
15:8	IRTX_R5	**IRTX byte 5**
7:0	IRTX_R4	**IRTX byte 4**

1101100C ***IRTXD2*** ***IRTX TRANSMISSION DATA 2 REGISTER*** ***00000000***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_R11								IRTX_R10							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_R9								IRTX_R8							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[940] Bit(s)	[941] Name	[942] Description
31:24	IRTX_R11	**IRTX byte 11**
23:16	IRTX_R10	**IRTX byte 10**
15:8	IRTX_R9	**IRTX byte 9**
7:0	IRTX_R8	**IRTX byte 8**

11011010 ***IRTX_LoH*** ***IRTX LOGIC 0 HIGH PERIOD REGISTER*** ***00000000***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_LoH							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_LoH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[943] Bit(s)	[944] Name	[945] Description
23:0	IRTX_LoH	**Logic 0 pulse high period** The period is equal to LoH/27MHz. This register is also valid in RC5/RC6 protocol. RC5 T = 24000, so T = 24000/27MHz = 0.889ms

11011014 ***IRTX_LoL*** ***IRTX LOGIC 0 LOW PERIOD REGISTER*** ***00000000***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_LoL							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_LoL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[946] Bit(s)	[947] Name	[948] Description
23:0	IRTX_LoL	**Logic 0 pulse low period** The period is equal to LoL/27MHz. ***While in SWO, bit[2:0] indicates which PWM channel is selected.

11011018 ***IRTX_L1H*** ***IRTX LOGIC 1 HIGH PERIOD REGISTER*** ***00000000***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_L1H							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_L1H															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[949] Bit(s)	[950] Name	[951] Description
23:0	IRTX_L1H	**Logic 1 pulse high period** The period is equal to L1H/27MHz.

1101101C ***IRTX_L1L*** ***IRTX LOGIC 1 LOW PERIOD REGISTER*** ***00000000***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_L1L							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_L1L															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[952] Bit(s)	[953] Name	[954] Description
23:0	IRTX_L1L	**Logic 1 pulse low period** The period is equal to L1L/27MHz.

11011020 IRTXSYNCH IRTX SYNC HIGH PERIOD REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_SYNCH							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_SYNCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[955] Bit(s)	[956] Name	[957] Description
23:0	IRTX_SYNCH	**SYNCH leading pulse high period** The period is equal to SYNCH/27MHz. SYNCH will be ignored if RC5/RC6 protocol adopted.

11011024 IRTXSYNCL IRTX SYNC LOW PERIOD REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IRTX_SYNCL							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_SYNCL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[958] Bit(s)	[959] Name	[960] Description
23:0	IRTX_SYNCL	**SYNCL leading pulse low period** The period is equal to SYNCL/27MHz. SYNCL will be ignored if RC5/RC6 protocol adopted.

[958] Bit(s)	[959] Name	[960] Description

11011028 ***IRTXMT*** ***IRTX MODULATION PARAMETER REGISTER*** ***00110033***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_CDT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_CWT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1

[961] Bit(s)	[962] Name	[963] Description
31:16	IRTX_CDT	**Carrier waveform duty time** Duty cycle = CDT/CWT Default duty cycle = 230/690 =33%
15:0	IRTX_CWT	**Carrier waveform period**

1101102C ***IRTX_INT_CLR*** ***IRTX INTERRUPT CLEAR REGISTER*** ***00000000***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INT_CLR
Type																W1C
Reset																0

[964] Bit(s)	[965] Name	[966] Description
0	INT_CLR	**Interrupt Clear**

11011030 ***IRTX_SWM_BP*** ***IRTX SOFTWARE MODE BASE PERIOD REGISTER*** ***00000000***

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name									IRTX_SWM_BP							
Type									RW							
Reset									0	0	0	0	0	0	0	0

[967] Bit(s)	[968] Name	[969] Description
7:0	IRTX_SWM_BP	**Base Period in Software Pulse-Width Mode** Unit: 0.5 us (2 MHz operating clock)

11011034 IRTX_SWM_PW0 IRTX SOFTWARE MODE PULSE WIDTH 0 REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_SWM_PW3								IRTX_SWM_PW2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_SWM_PW1								IRTX_SWM_PW0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[970] Bit(s)	[971] Name	[972] Description
31:24	IRTX_SWM_PW3	**IRTX Pulse-Width in Software Pulse-Width Mode**
23:16	IRTX_SWM_PW2	**IRTX Pulse-Width in Software Pulse-Width Mode**
15:8	IRTX_SWM_PW1	**IRTX Pulse-Width in Software Pulse-Width Mode**
7:0	IRTX_SWM_PW0	**IRTX Pulse-Width in Software Pulse-Width Mode**

11011038 IRTX_SWM_PW1 IRTX SOFTWARE MODE PULSE WIDTH 1 REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_SWM_PW7								IRTX_SWM_PW6							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_SWM_PW5								IRTX_SWM_PW4							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[973] Bit(s)	[974] Name	[975] Description
31:24	IRTX_SWM_PW7	**IRTX Pulse-Width in Software Pulse-Width Mode**
23:16	IRTX_SWM_PW6	**IRTX Pulse-Width in Software Pulse-Width Mode**
15:8	IRTX_SWM_PW5	**IRTX Pulse-Width in Software Pulse-Width Mode**
7:0	IRTX_SWM_PW4	**IRTX Pulse-Width in Software Pulse-Width Mode**

1101103C IRTX_SWM_PW2 IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_SWM_PW11								IRTX_SWM_PW10							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_SWM_PW9								IRTX_SWM_PW8							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[976] Bit(s)	[977] Name	[978] Description
31:24	IRTX_SWM_PW11	**IRTX Pulse-Width in Software Pulse-Width Mode**
23:16	IRTX_SWM_PW10	**IRTX Pulse-Width in Software Pulse-Width Mode**
15:8	IRTX_SWM_PW9	**IRTX Pulse-Width in Software Pulse-Width Mode**
7:0	IRTX_SWM_PW8	**IRTX Pulse-Width in Software Pulse-Width Mode**

11011040 IRTX_SWM_PW3 IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_SWM_PW15								IRTX_SWM_PW14							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_SWM_PW13								IRTX_SWM_PW12							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[979] Bit(s)	[980] Name	[981] Description
31:24	IRTX_SWM_PW15	**IRTX Pulse-Width in Software Pulse-Width Mode**
23:16	IRTX_SWM_PW14	**IRTX Pulse-Width in Software Pulse-Width Mode**
15:8	IRTX_SWM_PW13	**IRTX Pulse-Width in Software Pulse-Width Mode**
7:0	IRTX_SWM_PW12	**IRTX Pulse-Width in Software Pulse-Width Mode**

11011044 IRTX_SWM_PW4 IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_SWM_PW19								IRTX_SWM_PW18							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_SWM_PW17								IRTX_SWM_PW16							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[982] Bit(s)	[983] Name	[984] Description
31:24	IRTX_SWM_PW19	**IRTX Pulse-Width in Software Pulse-Width Mode**
23:16	IRTX_SWM_PW18	**IRTX Pulse-Width in Software Pulse-Width Mode**
15:8	IRTX_SWM_PW17	**IRTX Pulse-Width in Software Pulse-Width Mode**
7:0	IRTX_SWM_PW16	**IRTX Pulse-Width in Software Pulse-Width Mode**

11011048 IRTX_SWM_PW5 IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRTX_SWM_PW23								IRTX_SWM_PW22							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRTX_SWM_PW21								IRTX_SWM_PW20							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[985] Bit(s)	[986] Name	[987] Description
31:24	IRTX_SWM_PW23	**IRTX Pulse-Width in Software Pulse-Width Mode**
23:16	IRTX_SWM_PW22	**IRTX Pulse-Width in Software Pulse-Width Mode**
15:8	IRTX_SWM_PW21	**IRTX Pulse-Width in Software Pulse-Width Mode**
7:0	IRTX_SWM_PW20	**IRTX Pulse-Width in Software Pulse-Width Mode**

1101104C IRTX_SWM_PW6 IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER 00000000

Bit	31	30	29	28	27
Name	IRTX_SWM_PW27				
Type	RW				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	IRTX_SWM_PW25				
Type	RW				
Reset	0	0	0	0	0

[988] Bit(s)	[989] Name	[990] Description
[991] 31:24	[992] IRTX_SWM_PW27	[993] **IRTX Pulse-Width in Software Pulse-Width Mode**
[994] 23:16	[995] IRTX_SWM_PW26	[996] **IRTX Pulse-Width in Software Pulse-Width Mode**
[997] 15:8	[998] IRTX_SWM_PW25	[999] **IRTX Pulse-Width in Software Pulse-Width Mode**

[988] Bit(s)	[989] Name	[990] Description
[1000] 7:0	[1001] IRTX_SWM_PW24	[1002] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1003]	[1004]	[1005]

11011050 IRTX_SWM_PW7 IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER 00000000

Bit	31	30	29	28	27
Name	IRTX_SWM_PW31				
Type	RW				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	IRTX_SWM_PW29				
Type	RW				
Reset	0	0	0	0	0

[1006] Bit(s)	[1007] Name	[1008] Description
[1009] 31:24	[1010] IRTX_SWM_PW31	[1011] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1012] 23:16	[1013] IRTX_SWM_PW30	[1014] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1015] 15:8	[1016] IRTX_SWM_PW29	[1017] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1018] 7:0	[1019] IRTX_SWM_PW28	[1020] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1021]	[1022]	[1023]

11011054 IRTX_SWM_PW8 IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER 00000000

Bit	31	30	29	28	27
Name	IRTX_SWM_PW35				
Type	RW				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	IRTX_SWM_PW33				
Type	RW				
Reset	0	0	0	0	0

[1024] Bit(s)	[1025] Name	[1026] Description
[1027] 31:24	[1028] IRTX_SWM_PW35	[1029] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1030] 23:16	[1031] IRTX_SWM_PW34	[1032] **IRTX Pulse-Width in Software Pulse-Width Mode**

[1024]Bit(s)	[1025]Name	[1026]Description
[1033]15:8	[1034]IRTX_SWM_PW33	[1035]IRTX Pulse-Width in Software Pulse-Width Mode
[1036]7:0	[1037]IRTX_SWM_PW32	[1038]IRTX Pulse-Width in Software Pulse-Width Mode

[1039]	[1040]	[1041]

11011058 IRTX_SWM_PW9 IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER 00000000

Bit	31	30	29	28	27
Name	IRTX_SWM_PW39				
Type	RW				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	IRTX_SWM_PW37				
Type	RW				
Reset	0	0	0	0	0

[1042]Bit(s)	[1043]Name	[1044]Description
[1045]31:24	[1046]IRTX_SWM_PW39	[1047]IRTX Pulse-Width in Software Pulse-Width Mode
[1048]23:16	[1049]IRTX_SWM_PW38	[1050]IRTX Pulse-Width in Software Pulse-Width Mode
[1051]15:8	[1052]IRTX_SWM_PW37	[1053]IRTX Pulse-Width in Software Pulse-Width Mode
[1054]7:0	[1055]IRTX_SWM_PW36	[1056]IRTX Pulse-Width in Software Pulse-Width Mode

[1057]	[1058]	[1059]

1101105C IRTX_SWM_PW10 IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER 00000000

Bit	31	30	29	28	27
Name	IRTX_SWM_PW43				
Type	RW				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	IRTX_SWM_PW41				
Type	RW				
Reset	0	0	0	0	0

[1060]Bit(s)	[1061]Name	[1062]Description
[1063]31:24	[1064]IRTX_SWM_PW43	[1065]IRTX Pulse-Width in Software Pulse-Width Mode

[1060]Bit(s)	[1061]Name	[1062]Description
[1066]23:16	[1067]IRTX_SWM_PW42	[1068]**IRTX Pulse-Width in Software Pulse-Width Mode**
[1069]15:8	[1070]IRTX_SWM_PW41	[1071]**IRTX Pulse-Width in Software Pulse-Width Mode**
[1072]7:0	[1073]IRTX_SWM_PW40	[1074]**IRTX Pulse-Width in Software Pulse-Width Mode**
[1075]	[1076]	[1077]

11011060 IRTX_SWM_PW11 IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER 00000000

Bit	31	30	29	28	27
Name	IRTX_SWM_PW47				
Type	RW				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	IRTX_SWM_PW45				
Type	RW				
Reset	0	0	0	0	0

[1078]Bit(s)	[1079]Name	[1080]Description
[1081]31:24	[1082]IRTX_SWM_PW47	[1083]**IRTX Pulse-Width in Software Pulse-Width Mode**
[1084]23:16	[1085]IRTX_SWM_PW46	[1086]**IRTX Pulse-Width in Software Pulse-Width Mode**
[1087]15:8	[1088]IRTX_SWM_PW45	[1089]**IRTX Pulse-Width in Software Pulse-Width Mode**
[1090]7:0	[1091]IRTX_SWM_PW44	[1092]**IRTX Pulse-Width in Software Pulse-Width Mode**
[1093]	[1094]	[1095]

11011064 IRTX_SWM_PW12 IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER 00000000

Bit	31	30	29	28	27
Name	IRTX_SWM_PW51				
Type	RW				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	IRTX_SWM_PW49				
Type	RW				
Reset	0	0	0	0	0

[1096] Bit(s)	[1097] Name	[1098] Description
[1099] 31:24	[1100] IRTX_SWM_PW51	[1101] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1102] 23:16	[1103] IRTX_SWM_PW50	[1104] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1105] 15:8	[1106] IRTX_SWM_PW49	[1107] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1108] 7:0	[1109] IRTX_SWM_PW48	[1110] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1111]	[1112]	[1113]

11011068 ***IRTX_SWM_PW13*** ***IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER*** ***00000000***

Bit	31	30	29	28	27
Name	IRTX_SWM_PW55				
Type	RW				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	IRTX_SWM_PW53				
Type	RW				
Reset	0	0	0	0	0

[1114] Bit(s)	[1115] Name	[1116] Description
[1117] 31:24	[1118] IRTX_SWM_PW55	[1119] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1120] 23:16	[1121] IRTX_SWM_PW54	[1122] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1123] 15:8	[1124] IRTX_SWM_PW53	[1125] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1126] 7:0	[1127] IRTX_SWM_PW52	[1128] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1129]	[1130]	[1131]

1101106C ***IRTX_SWM_PW14*** ***IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER*** ***00000000***

Bit	31	30	29	28	27
Name	IRTX_SWM_PW59				
Type	RW				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	IRTX_SWM_PW57				
Type	RW				
Reset	0	0	0	0	0

[1132] Bit(s)	[1133] Name	[1134] Description
[1135] 31:24	[1136] IRTX_SWM_PW59	[1137] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1138] 23:16	[1139] IRTX_SWM_PW58	[1140] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1141] 15:8	[1142] IRTX_SWM_PW57	[1143] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1144] 7:0	[1145] IRTX_SWM_PW56	[1146] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1147]	[1148]	[1149]

11011070 IRTX_SWM_PW15 IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER 00000000

Bit	31	30	29	28	27
Name	IRTX_SWM_PW63				
Type	RW				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	IRTX_SWM_PW61				
Type	RW				
Reset	0	0	0	0	0

[1150] Bit(s)	[1151] Name	[1152] Description
[1153] 31:24	[1154] IRTX_SWM_PW63	[1155] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1156] 23:16	[1157] IRTX_SWM_PW62	[1158] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1159] 15:8	[1160] IRTX_SWM_PW61	[1161] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1162] 7:0	[1163] IRTX_SWM_PW60	[1164] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1165]	[1166]	[1167]

11011074 IRTX_SWM_PW16 IRTX SOFTWARE MODE PULSE WIDTH 2 REGISTER 00000000

Bit	31	30	29	28	27
Name	IRTX_SWM_PW67				
Type	RW				
Reset	0	0	0	0	0
Bit	15	14	13	12	11
Name	IRTX_SWM_PW65				
Type	RW				
Reset	0	0	0	0	0

[1168] Bit(s)	[1169] Name	[1170] Description
[1171] 31:24	[1172] IRTX_SWM_PW67	[1173] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1174] 23:16	[1175] IRTX_SWM_PW66	[1176] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1177] 15:8	[1178] IRTX_SWM_PW65	[1179] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1180] 7:0	[1181] IRTX_SWM_PW64	[1182] **IRTX Pulse-Width in Software Pulse-Width Mode**
[1183]	[1184]	[1185]

1.22 SPI NOR Flash Controller

1.22.1 Introduction

The serial flash controller for convenient high-speed serial NOR flash device access. The controller supports standard SPI NOR flash device as well as high-performance dual and quad SPI NOR flash device. The speed of SPI clock could up to 50MHz for both single bit SPI mode and dual/quad SPI mode.

1.22.2 Features

The SPI NOR Flash Controller fully supports the following features:

- Data bit width x1/x2/x4
- Max Frequency up to 50MHz
- 512Byte r/w buffer
- 4byte address mode support, compatible 3byte address mode
- Support Direct-Read and PIO-Read
- DMA inside
- Boot availability

1.22.3 Block Diagram

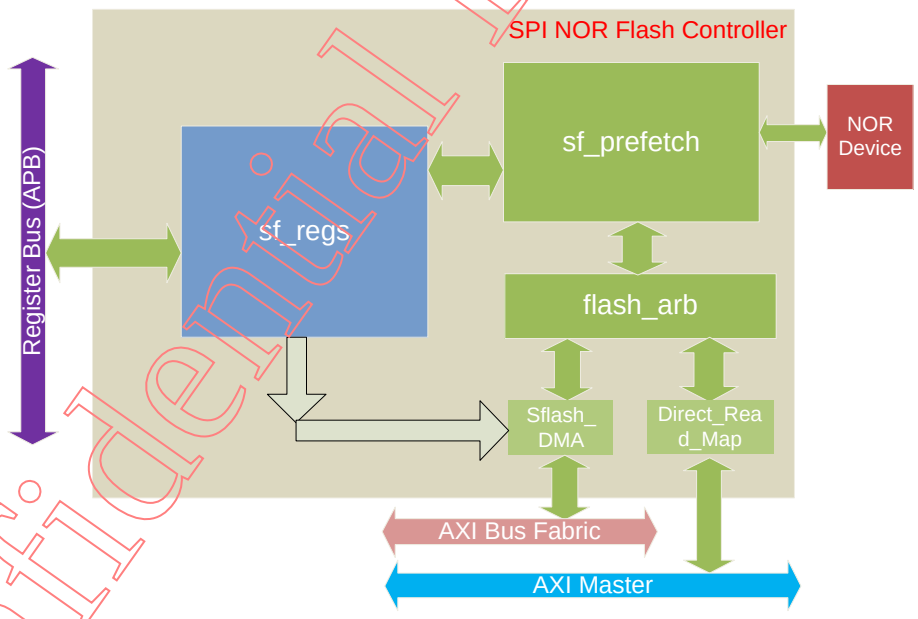


Figure 1-20. SPI NOR Flash Controller Block Diagram

1.22.4 Register Definition

Module name: Flashif Base address: (+11014000h)

Address	Name	Width	Register Function
11014000	REG_SF_CMD	8	serial flash command register
11014004	REG_SF_CNT	8	Bit count to transfer by PRG command
11014008	REG_SF_RDSR	8	Read back Status Register by RDSR command
1101400C	REG_SF_RDATA	8	Read back Flash Data by RD command
11014010	REG_SF_RADR0	8	Read or Write address for Read command or Write command
11014014	REG_SF_RADR1	8	Read or Write address for Read command or Write command
11014018	REG_SF_RADR2	8	Read or Write address for Read command or Write command
110140C8	REG_SF_RADR3	8	Read or Write address for Read command or Write command
1101401C	REG_SF_WDATA	8	The serial flash write data used by the Write Command
11014020	REG_SF_PRGDATA0	8	The serial flash program shift data used by the PRG Command.
11014024	REG_SF_PRGDATA1	8	The serial flash program shift data used by the PRG Command.
11014028	REG_SF_PRGDATA2	8	The serial flash program shift data used by the PRG Command.
1101402C	REG_SF_PRGDATA3	8	The serial flash program shift data used by the PRG Command.
11014030	REG_SF_PRGDATA4	8	The serial flash program shift data used by the PRG Command.
11014034	REG_SF_PRGDATA5	8	The serial flash program shift data used by the PRG Command.
11014038	REG_SF_SHREG0	8	The shift register of serial flash interface. For debug only.
1101403C	REG_SF_SHREG1	8	The shift register of serial flash interface. For debug only.
11014040	REG_SF_SHREG2	8	The shift register of serial flash interface. For debug only.
11014044	REG_SF_SHREG3	8	The shift register of serial flash interface. For debug only.
11014048	REG_SF_SHREG4	8	The shift register of serial flash interface. For debug only.
1101404C	REG_SF_SHREG5	8	The shift register of serial flash interface. For debug only.
11014050	REG_SF_SHREG6	8	The shift register of serial flash interface. For debug only.
11014054	REG_SF_SHREG7	8	The shift register of serial flash interface. For debug only.
11014058	REG_SF_SHREG8	8	The shift register of serial flash interface. For debug only.
1101405C	REG_SF_SHREG9	8	The shift register of serial flash interface. For debug only.
11014060	REG_SF_SHREG10	8	The shift register of serial flash interface. For debug only.
11014060	REG_SF_CFG1	8	module Configure register 1
11014064	REG_SF_CFG2	8	module Configure register 2
110140B4	REG_SF_CFG3	8	module Configure register 3
110140A0	REG_SF_DELSEL0	8	Serial flash interface port delay select register 0

Address	Name	Width	Register Function
110140A4	REG_SF_DELSEL1	8	Serial flash interface port delay select register 1
110140D0	REG_SF_DELSEL2	8	Serial flash interface port delay select register 2
110140D4	REG_SF_DELSEL3	8	Serial flash interface port delay select register 3
110140D8	REG_SF_DELSEL4	8	Serial flash interface port delay select register 4
110140A8	REG_SF_INTRSTUS	8	Interrupt register
110140AC	REG_SF_INTREN	8	Interrupt Enable register
110140C0	REG_SF_AAICMD	8	AAI programming command enable register
110140C4	REG_SF_WRPROT	8	Write command enable register
110140CC	REG_SF_DUAL	8	Serial flash dual mode configure register
11014080	RREG_FLASH_TIME	32	Serial flash access timing register. (RISC R/W only)
11014094	RREG_SFLASH_TIME	32	CS active or inactive clock cycle control register. (RISC R/W only)
11014098	REG_SF_PP_DW_DATA	32	Flash page program data register
1101409C	REG_DIFF_WHEN_WR	32	The difference between flash read address and cache data address
110140B8	REG_FL_CHKSUM_CTL	8	flash check sum control register
110140BC	REG_FL_CHKSUM	32	Check sum output register
11014070	REG_FL_STATUS0	32	Flash status register 0
11014710	REG_CFG1_BRI	32	DRAM2AXI config register1
11014714	REG_CFG2_BRI	32	DRAM2AXI config register2
11014718	REG_FDMA_CTL	32	sflash dma control register
1101471C	REG_FDMA_FADR	32	sflash dma read sflash start address
11014720	REG_FDMA_DADR	32	sflash dma writer dram start address
11014724	REG_FDMA_END_DADR	32	sflash dma writer dram end address
11014728	REG_CG_DIS	32	Clock gate disable register

11014000 REG_SF_CMD serial flash command register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**AUTO_INCR**		**WRSR_CMD**	**WR_CMD**	**ERASE_CMD**	**PRG_CMD**	**RDSR_CMD**	**RD**
Type									RW		A0	A0	A0	A0	A0	A0
Reset									0		0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7	**AINC**	AUTO_INCR	**The RADR will auto increase by 1 after trigger RD or WR command** 0: address not auto increase 1: address auto increase

Bit(s)	Mnemonic	Name	Description
5	**WRSR**	WRSR_CMD	**Write Status Register. This command works for ST, SST and compatible command-set flash, but not work for ATMEL** 0: no write serial flash status register command 1: write serial flash status register command
4	**WR**	WR_CMD	**Write 1 to trigger Single Byte Write. The write data must be prepared at WDATA and the write address must be prepared at RADR before trigger. This bit will be auto-cleared when done. This command works for ST, SST and compatible command-set flash, but not work for ATMEL.** Setting buf2wr_en (CFG2[0]), will enter page programming mode. In this mode, this bit is the trigger bit. 0: write data command is not triggered 1: trigger write data command
3	**ERASE**	ERASE_CMD	**This bit will be auto-cleared when done. This command works for ST and compatible command-set flash, but not work for SST and ATMEL.** 0: bulk erase is not triggered 1: trigger bulk erase command
2	**PRG**	PRG_CMD	**The program bit count must be prepared at REG_SF_CNT and the program data must be prepared at PRGDATA0~5 before trigger. This bit will be auto-cleared when done. This command works for all flash.** 0: program data is not triggered 1: trigger user program command
1	**RDSR**	RDSR_CMD	**This Status Register will be shown on RDSR Register . This command works for ST, SST, ATMEL and compatible command-set flash.** 0: read status register is not triggered 1: trigger read status register command
0	**RD**	RD	**The read address must be prepared at RADR before trigger. Read Data will be shown on RDATA Register. This command works for ST, SST, ATMEL and compatible command-set flash.**

Bit(s)	Mnemonic	Name	Description
			0: read data is not triggered 1: trigger read data command

11014004 REG_SF_CNT Bit count to transfer by PRG command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											SF_CNT					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0	**CNT**	SF_CNT	**bit count to transfer by PRG command. Maximum 48 bits**

11014008 REG_SF_RDSR Read back Status Register by RDSR command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RDSR_DATA							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**RDSRDAT**	RDSR_DATA	**Read back Status Register by RDSR command**

1101400C REG_SF_RDATA Read back Flash Data by RD command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SF_RDATA							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SFRDAT**	SF_RDATA	**Read back Flash Data by RD command**

11014010 REG_SF_RADR0 Read or Write address for Read command or Write command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SFP_ADR0							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SFPADR0**	SFP_ADR0	**Read or Write address for Read command or Write command**

11014014 REG_SF_RADR1 Read or Write address for Read command or Write command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SFP_ADR1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SFPADR1**	SFP_ADR1	**Read or Write address for Read command or Write command**

11014018 REG_SF_RADR2 Read or Write address for Read command or Write command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SFP_ADR2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SFPADR2**	SFP_ADR2	**Read or Write address for Read command or Write command**

110140C8 REG_SF_RADR3 Read or Write address for Read command or Write command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SFP_ADR3							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SFPADR3**	SFP_ADR3	**Read or Write address for Read command or Write command**

1101401C REG_SF_WDATA The serial flash write data used by the Write Command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SFP_WR_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SFWRDAT**	SFP_WR_DATA	**The serial flash write data used by the Write Command**

11014020 REG_SF_PRGDATA0 The serial flash program shift data used by the PRG Command. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SFP_PRGDATA0**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**PRGDATA0**	SFP_PRGDATA0	**The serial flash program shift data used by the PRG Command. The PRGDATA5 is shifted first, and the PRGDATA0 is shifted last. In each byte shift, MSB is shifted first.**

11014024 REG_SF_PRGDATA1 The serial flash program shift data used by the PRG Command. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SFP_PRGDATA1**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**PRGDATA1**	SFP_PRGDATA1	**The serial flash program shift data used by the PRG Command. The PRGDATA5 is shifted first, and the PRGDATA0 is shifted last. In each byte shift, MSB is shifted first.**

11014028 REG_SF_PRGDATA2 The serial flash program shift data used by the PRG Command. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SFP_PRGDATA2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**PRGDATA2**	SFP_PRGDATA2	**The serial flash program shift data used by the PRG Command. The PRGDATA5 is shifted first, and the PRGDATA0 is shifted last. In each byte shift, MSB is shifted first.**

1101402C REG_SF_PRGDATA3 The serial flash program shift data used by the PRG Command. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SFP_PRGDATA3							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**PRGDATA3**	SFP_PRGDATA3	**The serial flash program shift data used by the PRG Command. The PRGDATA5 is shifted first, and the PRGDATA0 is shifted last. In each byte shift, MSB is shifted first.**

11014030 REG_SF_PRGDATA4 The serial flash program shift data used by the PRG Command. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SFP_PRGDATA4							
Type									RW							

Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**PRGDATA4**	SFP_PRGDATA4	**The serial flash program shift data used by the PRG Command. The PRGDATA5 is shifted first, and the PRGDATA0 is shifted last. In each byte shift, MSB is shifted first.**

11014034 REG_SF_PRGDATA5 The serial flash program shift data used by the PRG Command. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SFP_PRGDATA5							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**PRGDATA5**	SFP_PRGDATA5	**The serial flash program shift data used by the PRG Command. The PRGDATA5 is shifted first, and the PRGDATA0 is shifted last. In each byte shift, MSB is shifted first.**

11014038 REG_SF_SHREG0 The shift register of serial flash interface. For debug only. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SHIFT_REG0							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SHREG0**	SHIFT_REG0	**The shift register of serial flash interface. For debug only.**

1101403C REG_SF_SHREG1 The shift register of serial flash interface. For debug only. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SHIFT_REG1							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SHREG1**	SHIFT_REG1	**The shift register of serial flash interface. For debug only.**

11014040 REG_SF_SHREG2 The shift register of serial flash interface. For debug only. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SHIFT_REG2							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SHREG2**	SHIFT_REG2	**The shift register of serial flash interface. For debug only.**

11014044 REG_SF_SHREG3 The shift register of serial flash interface. For debug only. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SHIFT_REG3							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SHREG3**	SHIFT_REG3	**The shift register of serial flash interface. For debug only.**

11014048 REG_SF_SHREG4 The shift register of serial flash interface. For debug only. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SHIFT_REG4**							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SHREG4**	SHIFT_REG4	**The shift register of serial flash interface. For debug only.**

1101404C REG_SF_SHREG5 The shift register of serial flash interface. For debug only. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SHIFT_REG5**							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SHREG5**	SHIFT_REG5	**The shift register of serial flash interface. For debug only.**

11014050 REG_SF_SHREG6 The shift register of serial flash interface. For debug only. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SHIFT_REG6							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SHREG6**	SHIFT_REG6	**The shift register of serial flash interface. For debug only.**

11014054 REG_SF_SHREG7 The shift register of serial flash interface. For debug only. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SHIFT_REG7							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SHREG7**	SHIFT_REG7	**The shift register of serial flash interface. For debug only.**

11014058 REG_SF_SHREG8 The shift register of serial flash interface. For debug only. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SHIFT_REG8							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SHREG8**	SHIFT_REG8	**The shift register of serial flash interface. For debug only.**

1101405C REG_SF_SHREG9 The shift register of serial flash interface. For debug only. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SHIFT_REG9							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SHREG9**	SHIFT_REG9	**The shift register of serial flash interface. For debug only.**

11014068 REG_SF_SHREG10 The shift register of serial flash interface. For debug only. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SHIFT_REG10							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SHREG9**	SHIFT_REG10	**The shift register of serial flash interface. For debug only.**

11014060 REG_SF_CFG1 module Configure register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FL_MON_SEL							FAST_READ
Type									RW							RW
Reset									0	0						0

Bit(s)	Mnemonic	Name	Description
7:6	**FL_MON_SEL**	FL_MON_SEL	**Nor flash controller monitor signal selection.** 00: nor flash controller status0 01: nor flash controller status1 10: nor flash controller status2 11: nor flash controller status3
0	**FR**	FAST_READ	**Fast read** 0: Normal read command 1: support ST fast read command (read command 0Bh, and 1 dummy bytes)

11014064 REG_SF_CFG2 module Configure register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**AAI_CFG**		**PRG_WR_OPCODE_EN**				**BUF2WR_EN_SET**
Type										RW		RW				RW
Reset										0		0				0

Bit(s)	Mnemonic	Name	Description
6	**AAICFG**	AAI_CFG	**Auto Address Increment command configure** 0: AAI command is 0xAD 1: AAI command is 0xAF
4	**PRGWREN**	PRG_WR_OPCODE_EN	**Program operation code enable** 0: Using 0x02 as the write Command Op Code 1: Using the PRGDATA0 as the Write Command Op Code
0	**BUF2WREN**	BUF2WR_EN_SET	**Let the pre-fetch buffer, designed for flash reading, used for Page Program. We promise**

Bit(s)	Mnemonic	Name	Description
			that the data path is not switched until the pre-fetch buffer is idle. 0: pre-fetch buffer use for reading 1: pre-fetch buffer use for Page program

110140B4 REG_SF_CFG3 module Configure register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									WREN_DIS	PRG_WREN_OPCODE_EN	POL_RDY_BIT_DIS	PRG_RD_OPCODE_EN	RDY_VLUE	STUS_POS		
Type									RW	RW	RW	RW	RW	RW		
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7	**WRDI**	WREN_DIS	**Serial flash write enable control bit** 0: Send write enable command 1: Skip the write enable state
6	**PRGWEOPEN**	PRG_WREN_OPCODE_EN	**Write Enable command op-code configure** 0: Using 0x06 as the Write Enable Command Op-code 1: Using the PRGDATA2 as the Write Enable Command Op-code
5	**POLRDYDIS**	POL_RDY_BIT_DIS	**Disable polling ready bit disable configure bit** 0: Polling status register 1: Skip the polling status state
4	**PRGRDOPEN**	PRG_RD_OPCODE_EN	**Configure Read Status Command Op-code** 0: Using 0x05 as the Read Status Command Op-code if flash brand is zero else 0xd7 1: Using the PRGDATA1 as the Read Status Command Op-code

Bit(s)	Mnemonic	Name	Description
3	**RDYVLUE**	RDY_VLUE	**Serial flash Output bit value when it is ready** 0: Wait the polled bit until it becomes logic zero 1: Wait the polled bit until it becomes logic one
2:0	**STUSPOS**	STUS_POS	**7~0 Which bit of status register is polled**

110140A0 REG_SF_DELSEL0 Serial flash interface port delay select register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FOE_DELAY_SEL				FWR_DELAY_SEL			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:4	**SOOUTDEL**	FOE_DELAY_SEL	**For SFCK pin delay. The unit delay is 0.8 ns. Total delay is FOE_DELAY_SEL * 0.8 ns.**
3:0	**SIOUTDEL**	FWR_DELAY_SEL	**For SFDI pin input delay. The unit delay is 0.8 ns. Total delay is FWR_DELAY_SEL * 0.8 ns.**

110140A4 REG_SF_DELSEL1 Serial flash interface port delay select register 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												SMPCK_INV	FA16_DELAY_SEL			
Type												RW	RW			
Reset												1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4	**SMPCKINV**	SMPCK_INV	**Pin input sampling clock inverter configure**

Bit(s)	Mnemonic	Name	Description
			0: posedge sample data 1: negedge sample data
3:0	**SCKDEL**	FA16_DELAY_SEL	**For SFDO pin output delay. The unit delay is 0.8 ns. Total delay is FA16_DELAY_SEL * 0.8 ns.**

110140D0 REG_SF_DELSEL2 Serial flash interface port delay select register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SF_Q_DELAY_SEL				SF_D_DELAY_SEL			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:4	**SOINDEL**	SF_Q_DELAY_SEL	**For SFDO pin input delay. The unit delay is 0.8 ns. Total delay is SF_Q_DELAY_SEL * 0.8 ns.**
3:0	**SIINDEL**	SF_D_DELAY_SEL	**For SFDI pin output delay. The unit delay is 0.8 ns. Total delay is SF_D_DELAY_SEL * 0.8 ns.**

110140D4 REG_SF_DELSEL3 Serial flash interface port delay select register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SF_D2_IN_DELAY_SEL				SF_D2_OUT_DELAY_SEL			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:4	**SFDIO2INDEL**	SF_D2_IN_DELAY_SEL	**For SFDIO2 pin input delay. The unit delay is 0.8 ns. Total delay is SF_Q_DELAY_SEL * 0.8 ns.**

Bit(s)	Mnemonic	Name	Description
3:0	**SFDIO2OUTDEL**	SF_D2_OUT_DELAY_SEL	**For SFDIO3 pin output delay. The unit delay is 0.8 ns. Total delay is SF_D_DELAY_SEL * 0.8 ns.**

110140D8 REG_SF_DELSEL4 Serial flash interface port delay select register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SF_D3_IN_DELAY_SEL				SF_D3_OUT_DELAY_SEL			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:4	**SFDIO3INDEL**	SF_D3_IN_DELAY_SEL	**For SFDIO3 pin input delay. The unit delay is 0.8 ns. Total delay is SF_Q_DELAY_SEL * 0.8 ns.**
3:0	**SFDIO3OUTDEL**	SF_D3_OUT_DELAY_SEL	**For SFDIO3 pin output delay. The unit delay is 0.8 ns. Total delay is SF_D_DELAY_SEL * 0.8 ns.**

110140A8 REG_SF_INTRSTUS Interrupt register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									sflash_dma_int	AAI_INT	WSR_INT	WR_INT	ERASE_INT	PRG_INT	RDSR_INT	RD_INT
Type									RO	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7	**DMAINT**	sflash_dma_int	**Interrupt for sflash dma completion. Cleared when write 1 to it.** 0: no sflash_dma interrupt

Bit(s)	Mnemonic	Name	Description
			1: sflash_dma interrupt occur
6	**AAIINT**	AAI_INT	**Interrupt for AAI programming completion. Cleared when write 1 to it.** 0: no AAI interrupt 1: AAI interrupt occur
5	**WSRINT**	WRSR_INT	**Interrupt for Write Status Register completion. Cleared when write 1 to it.** 0: no Write status register not interrupt 1: Write status register complete interrupt
4	**WRINT**	WR_INT	**Interrupt for Write/Page Program Completion. Cleared when write 1 to it.** 0: No write/program interrupt 1: Write/program completion interrupt
3	**ERSINT**	ERASE_INT	**Interrupt for Bulk Erase. Cleared when write 1 to it** 0: No Erase interrupt 1: Erase complete interrupt
2	**PRGINT**	PRG_INT	**Interrupt for Programmable op-code completion. Cleared when write 1 to it.** 0: No program op-code completion interrupt. 1: Programmable op-code completion interrupt.
1	**RSRINT**	RDSR_INT	**Interrupt for Read Status completion. Cleared when write 1 to it.** 0: No read status completion interrupt 1: Read status completion interrupt
0	**RDINT**	RD_INT	**Interrupt for Read Operation Completion. Cleared when write 1 to it.** 0: No read operation completion interrupt 1: Read operation completion interrupt

110140AC REG_SF_INTREN Interrupt Enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DMA_INTREN	AAI_INTREN	WSR_INTREN	WR_INTREN	ERASE_INTREN	PRG_INTREN	RDSR_INTREN	RD_INTREN
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7	**DMAINTEN**	DMA_INTREN	**sflash dma enable interrupt control bit** 0: sflash dma interrupt disable 1: sflash dma interrupt enable
6	**AAIINTEN**	AAI_INTREN	**AAI enable interrupt control bit** 0: AAI interrupt disable 1: AAI interrupt enable
5	**WSRINTEN**	WRSR_INTREN	**WRSR enable interrupt control bit** 0: WRSR interrupt disable 1: WRSR interrupt enable
4	**WRINTEN**	WR_INTREN	**WR enable interrupt control bit** 0: WR interrupt disable 1: WR interrupt enable
3	**ERSINTEN**	ERASE_INTREN	**ERASE enable interrupt control bit** 0: ERASE interrupt disable 1: ERASE interrupt enable
2	**PRGINTEN**	PRG_INTREN	**PRG enable interrupt control bit** 0: PRG interrupt disable 1: PRG interrupt enable
1	**RSRINTEN**	RDSR_INTREN	**RDSR enable interrupt control bit** 0: RDSR interrupt disable 1: RDSR interrupt enable
0	**RDINTEN**	RD_INTREN	**RD enable interrupt control bit** 0: RD interrupt disable

Bit(s)	Mnemonic	Name	Description
			1: RD interrupt enable

110140C0 REG_SF_AAICMD AAI programming command enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																AAI_WR_CMD
Type																A0
Reset																0

Bit(s)	Mnemonic	Name	Description
0	AAIWR	AAI_WR_CMD	**Write 1 to this register will enable AAI (Auto Address Increment) program procedure. The write address must be prepared at RADR (RADR3, RADR2, RADR1, RADR0) and set suitable AAI_CFG (CFG2[6]) before trigger. This bit will be auto-cleared when done. It must to set buf2wr_en(CFG2[0]) for AAI programming.** 0: AAI procedure not start 1: AAI procedure is triggered

110140C4 REG_SF_WRPROT Write command enable register 00000085

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									WRITE_PROTECT							
Type									RW							
Reset									1	0	0	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
7:0	WRPROT	WRITE_PROTECT	**Set this byte to 0x30 will turn off write protection and enable SF commands in CMD and AAI_CMD.**

Bit(s)	Mnemonic	Name	Description

110140CC REG_SF_DUAL Serial flash dual mode configure register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												LARGE_ADDR_EN	ADDR_QUAD	QUAD_READ_EN	ADDR_DUAL	DUAL_READ_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4	**LARGE_ADDR_EN**	LARGE_ADDR_EN	**Instruction will need 4 byte address to access the memory space larger than 16MB. Works for Erase/PP/Read commond** 0: 3 byte address mode(max 16MB) 1: 4 byte address mode(larger than 16MB)
3	**ADRQUAD**	ADDR_QUAD	**quad address mode** 0: quad address mode disable 1: quad address mode enable (for MXIC)
2	**DUALRDEN**	QUAD_READ_EN	**Quad read mode will be enable after previous read operation is finished. The quad read command must be write in PRGDATA4, and the read data can be obtained in RDATA.** 0: quad read mode disable 1: quad read mode enable
1	**ADRDUAL**	ADDR_DUAL	**Dual address mode** 0: dual address mode disable 1: dual address mode enable (for MXIC)
0	**DUALRDEN**	DUAL_READ_EN	**Dual read mode will be enable after previous read operation is finished. The dual read command must be write in PRGDATA3, and the read data can be obtained in RDATA.** 0: dual read mode disable

Bit(s)	Mnemonic	Name	Description
			1: dual read mode enable

11014080 RREG_FLASH_TIME Serial flash access timing register. (RISC R/W only) 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											LATE_LATCH	FLASH_ACC				
Type											RW	RW				
Reset											0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
5	**LLAT**	LATE_LATCH	**Flash controller later latch data from flash interface, so that gain 1T more setup time, but will have less hold time** 0: normal latch data 1: late latch data
4:0	**FACC**	FLASH_ACC	**Flash access AC timing is in cycles of BCLK periods of FACC+1**

11014094 RREG_SFLASH_TIME CS active or inactive clock cycle control register. (RISC R/W only) 00000522

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TCSHI_REG					TCSH_REG				TCSS_REG		
Type					RW					RW				RW		
Reset					0	1	0	1		0	1	0		0	1	0

Bit(s)	Mnemonic	Name	Description
11:8	**TCSHI**	TCSHI_REG	**CS_ high time = TCSHI for ATMEL flash. Others 5 T.**

Bit(s)	Mnemonic	Name	Description
6:4	**TCSH**	TCSH_REG	**CS_ hold time = TCSH + 1 T for ATMEL flash. Others 1 T.**
2:0	**TCSS**	TCSS_REG	**CS_ setup time = TCSS + 1.5T for ATMEL flash. Others 1.5T.**

11014098 REG_SF_PP_DW_DATA Flash page program data register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REG_SF_PP_DW_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REG_SF_PP_DW_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PP_DATA**	REG_SF_PP_DW_DATA	**Flash page program data register**

1101409C REG_DIFF_WHEN_WR The difference between flash read address and cache data address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RD_CACHE_ADR_DIFF					
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0	**RDCHEDFF**	RD_CACHE_ADR_DIFF	**The difference between flash read address and cache data address**

110140B8 REG_FL_CHKSUM_CTL flash check sum control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CHKSUM_CTL7	CHKSUM_CTL6						CHKSUM_CTL0
Type									RW	RW						RW
Reset									0	0						0

Bit(s)	Mnemonic	Name	Description
7	**CHKSUM7**	CHKSUM_CTL7	**BIM Flash dma check sum control register** 0: Flash dma read data check sum disable 1: Flash dma read data check sum enable
6	**CHKSUM6**	CHKSUM_CTL6	**BIM Read flash check sum control register** 0: datard read data check sum disable 1: datard read data check sum enable
0	**CHKSUM0**	CHKSUM_CTL0	**RISC0 read flash check sum control register** 0: Stop RISC check sum 1: RISC read flash data check sum enable

110140BC REG_FL_CHKSUM Check sum output register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHKSUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHKSUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CHKSUM**	CHKSUM	**Check sum output data.**

110140C0 REG_FL_STATUS0 Flash status register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																
Type																
Reset																

Bit(s)	Name	Description

11014710 REG_CFG1_BRI DRAM2AXI config register1 0000887F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AWHP	ARHP		STOP_AXI_READY	AWDOMAIN		ARDOMAIN	
Type									RW	RW		RW	RW		RW	
Reset									0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUTSTAND_W_NUM				OUTSTAND_R_NUM				IGNORE_TAG_FULL	CHECK_BVALID	WMERGE_EQUAL	WMERGE_PLUS1	WMERGE_EN	RMERGE_EQUAL	RMERGE_PLUS1	RMERGE_EN
Type	RW				RW				RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
23	**AWHP**	AWHP	**AXI awhp**
22	**ARHP**	ARHP	**AXI arhp**
20	**STOP_AXI_READY**	STOP_AXI_READY	**RISC force stop AXI wrapper ready** signal now
19:18	**AWDOMAIN**	AWDOMAIN	**AXI awdomain**
17:16	**ARDOMAIN**	ARDOMAIN	**AXI ardomain**
15:12	**OUTSTAND_W_NUM**	OUTSTAND_W_NUM	**AXI wrapper max write outstanding num**
11:8	**OUTSTAND_R_NUM**	OUTSTAND_R_NUM	**AXI wrapper max read outstanding num**
7	**IGNORE_TAG_FULL**	IGNORE_TAG_FULL	**DRAM request ignore write address tag** fifo full. (may cause read after write hazard if on)
6	**CHECK_BVALID**	CHECK_BVALID	**AXI wrapper return wdle after received** BVALID
5	**WMERGE_EQUAL**	WMERGE_EQUAL	**DRAM write request (equal address)** merge enable

Bit(s)	Mnemonic	Name	Description
4	**WMERGE_PLUS1**	WMERGE_PLUS1	**DRAM write request (address + 1)** merge enable
3	**WMERGE_EN**	WMERGE_EN	**DRAM write request merge enable**
2	**RMERGE_EQUAL**	RMERGE_EQUAL	**DRAM read request (equal address)** merge enable
1	**RMERGE_PLUS1**	RMERGE_PLUS1	**DRAM read request (address + 1) merge enable**
0	**RMERGE_EN**	RMERGE_EN	**DRAM read request merge enable**

11014714 REG_CFG2_BRI DRAM2AXI config register2 00020002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ARMMU	ARUSER	ARPREULTRA	ARFLUSH	ARULTRA	ARPROT		
Type									RW	RW	RW	RW	RW	RW		
Reset									0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AWMMU	AWUSER	AWPREULTRA	AWFLUSH	AWULTRA	AWPROT		
Type									RW	RW	RW	RW	RW	RW		
Reset									0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23	**ARMMU**	ARMMU	**AXI ARMMU**
22	**ARUSER**	ARUSER	**AXI ARUSER**
21	**ARPREULTRA**	ARPREULTRA	**AXI ARPREULTRA**
20	**ARFLUSH**	ARFLUSH	**AXI ARFLUSH**
19	**ARULTRA**	ARULTRA	**AXI ARULTRA**
18:16	**ARPROT**	ARPROT	**AXI ARPROT**
7	**AWMMU**	AWMMU	**AXI AWMMU**
6	**AWUSER**	AWUSER	**AXI AWUSER**
5	**AWPREULTRA**	AWPREULTRA	**AXI AWPREULTRA**
4	**AWFLUSH**	AWFLUSH	**AXI AWFLUSH**
3	**AWULTRA**	AWULTRA	**AXI AWULTRA**

Bit(s)	Mnemonic	Name	Description
2:0	**AWPROT**	AWPROT	**AXI AWPROT**

11014718 REG_FDMA_CTL sflash dma control register 00000F04

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					REQ_LEN									WDLE_EN	SW_RST	DMA_TRIG
Type					RW									RW	RW	RW
Reset					1	1	1	1						1	0	0

Bit(s)	Mnemonic	Name	Description
11:8	**REQ_LEN**	REQ_LEN	**Request length**
2	**WDLE_EN**	WDLE_EN	**When write this bit 1, use wdle signal to indicate a write dram transaction finish**
1	**SW_RST**	SW_RST	**software reset bit**
0	**DMA_TRIG**	DMA_TRIG	**sflash dma trigger bit, set 1 to start sflash dma, when dma complete, this bit auto clear by hw**

1101471C REG_FDMA_FADR sflash dma read sflash start address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SFLASH_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SFLASH_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SFLASH_ADDR**	SFLASH_ADDR	**sflash dma read sflash start address**

11014720 REG_FDMA_DADR sflash dma writer dram start address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	WDRAM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDRAM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4	**WDRAM_ADDR**	WDRAM_ADDR	**sflash dma write dram start address**

11014724 REG_FDMA_END_DADR sflash dma writer dram end address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDRAM_END_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDRAM_END_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4	**WDRAM_END_ADDR**	WDRAM_END_ADDR	**sflash dma write dram end address**

11014728 REG_CG_DIS Clock gate disable register 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								TOUT_EN	TOUT_CNT							
Type								WO	WO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FDATA_EN	CLK_DRAM_CG_DIS	CLK_AXI_CG_DIS
Type														WO	WO	WO
Reset														0	1	1

Bit(s)	Mnemonic	Name	Description
24	**TOUT_EN**	TOUT_EN	**bus timeout enable bit**

Bit(s)	Mnemonic	Name	Description
			0: tout disable 1: tout enable
23:16	**TOUT_CNT**	TOUT_CNT	**bus timeout counter**
2	**PIMP_EN**	FDATA_EN	**performance improve enable bit** 0: Performance improve disable 1: Performance improve enable
1	**CLK_DRAM_CG_DIS**	CLK_DRAM_CG_DIS	**CLK_DRAM GG disable bit** 0: CG enable 1: CG disable
0	**CLK_AXI_CG_DIS**	CLK_AXI_CG_DIS	**CLK_AXI GG disable bit** 0: CG enable 1: CG disable

1.23 SPI 1

1.23.1 Introduction

The SPI interface is a bit-serial, four-pin transmission protocol. Below figure is an example of the connection between the SPI master and SPI slave. The SPI controller interface is a master responsible of the data transmission with the slave.

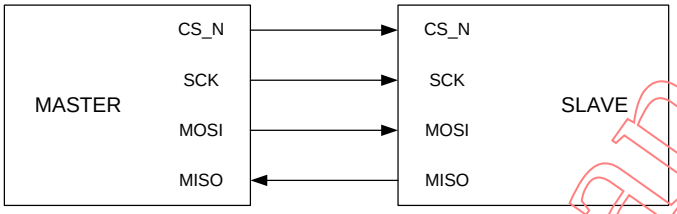


Figure 1-21. Pin connection between SPI master and SPI slave

1.23.1.1 Pin Description

Signal name	Type	Description
CS_N	O	Low active chip selection signal
SCK	O	The (bit) serial clock
MOSI	O	Data signal from master output to slave input
MISO	I	Data signal from slave output to master input

Table 1-8. SPI controller interface

1.23.1.2 Transmission Formats

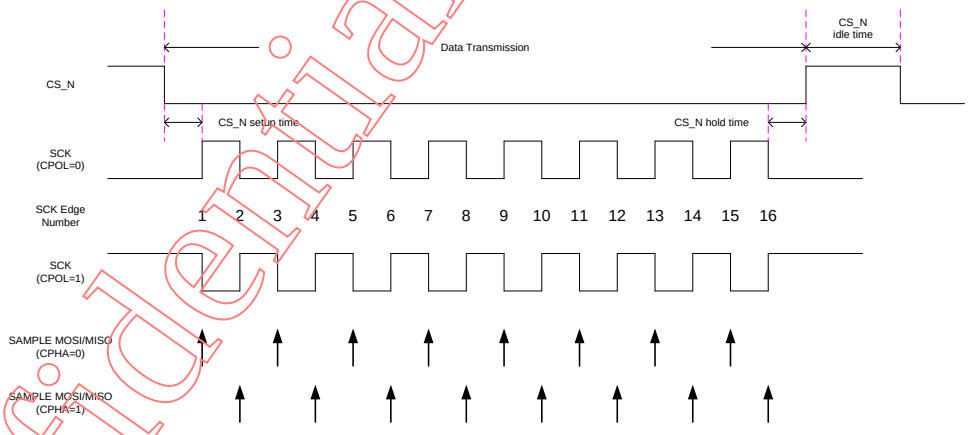


Figure 1-22. SPI transmission formats

The figure shows the waveform during the SPI transmission. The low active CS_N determines the start point and end point of one transaction. The CS_N setup time, hold time and idle time are also depicted.

CPOL defines the clock polarity in the transmission. Two types of polarity can be adopted, i.e. polarity 0 and polarity 1.

CPHA defines the legal timing to sample MOSI and MISO. Two different methods can be adopted.

1.23.2 Features

The features of the SPI controller (master) are:
Configurable CS_N setup time, hold time and idle time

- Programmable SCK high time and low time
- Configurable transmitting and receiving bit order
- Two configurable modes for the source of the data to be transmitted.
  (1) In TX DMA mode, the SPI controller automatically fetches the transmitted data (to be put on the MOSI line) from memory;
  (2) In TX FIFO mode, the data to be transmitted on the MOSI line are written to FIFO before the start of the transaction.
- Two configurable modes for destination of the data to be received.
  (1) In RX DMA mode, the SPI controller automatically stores the received data (from MISO line) to memory;
  (2) In RX FIFO mode, the received data keep being in RX FIFO of the SPI controller. The processor must read back the data by itself.
- Adjustable endian order from/to memory system
- Programmable byte length for transmission
- Unlimited length for transmission. This is achieved by the operation of PAUSE mode. In PAUSE mode, the CS_N signal will keep being active (low) after the transmission. At this time, the SPI controller is in PAUSE_IDLE state, ready to receive the resume command. The state transition is shown in below figure.
- Configurable option to control CS_N de-assert between byte transfers. The controller supports a special transmission format called CS_N de-assert mode.

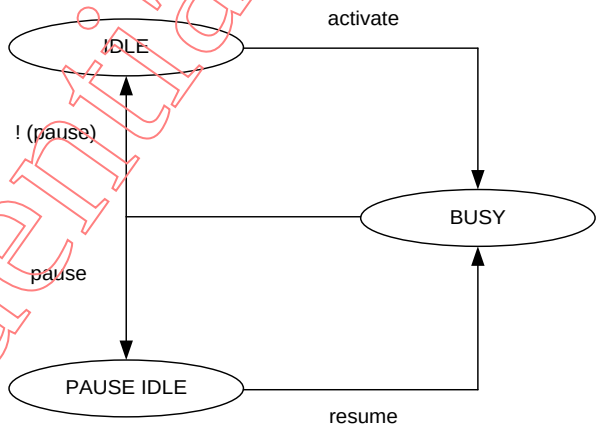


Figure 1-23. Operation flow with or without PAUSE mode

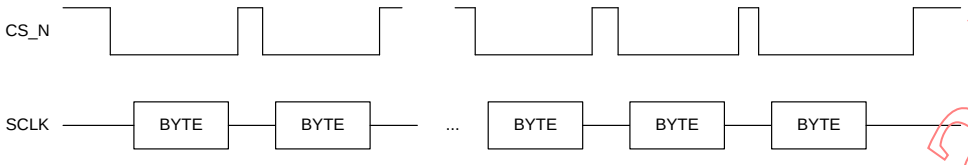


Figure 1-24. CS_N de-assert mode

1.23.3 Block Diagram

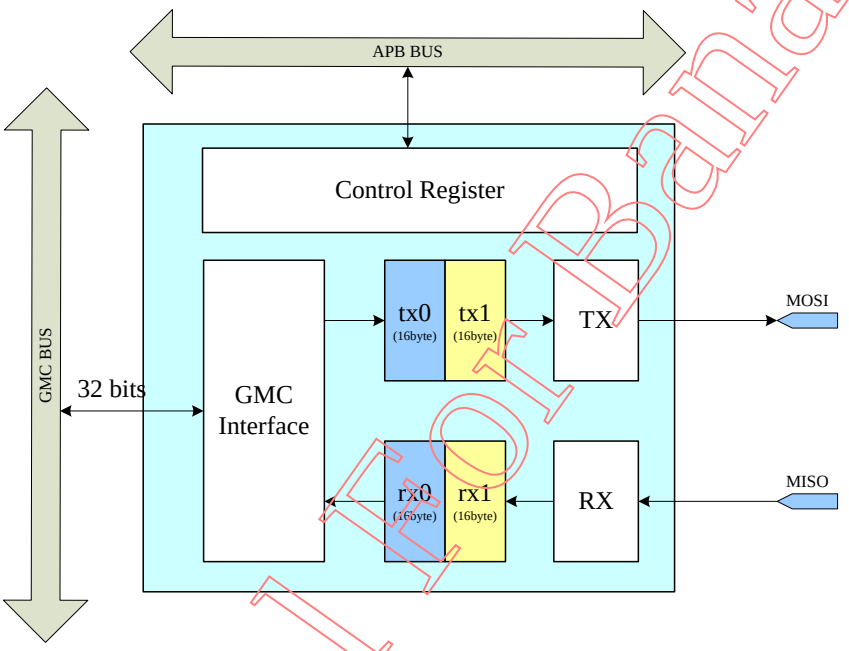


Figure 1-25. Block diagram of SPI

1.23.4 Register Definition

Module name: spi1 Base address: (+11016000h)

Address	Name	Width	Register Function
11016000	SPI_CFG0	32	SPI Configuration 0 Register
11016004	SPI_CFG1	32	SPI Configuration 1 Register
11016008	SPI_TX_SRC	32	SPI TX Source Address Register
1101600C	SPI_RX_DST	32	SPI RX Destination Address Register
11016010	SPI_TX_DATA	32	SPI TX Data FIFO
11016014	SPI_RX_DATA	32	SPI RX Data FIFO
11016018	SPI_CMD	32	SPI Command Register
1101601C	SPI_STATUS0	32	SPI Status 0 Register
11016020	SPI_STATUS1	32	SPI Status 1 Register
11016024	SPI_PAD_MACRO_SEL	32	SPI pad_macro Selection Register
11016028	SPI_CFG2	32	SPI Configuration 2 Register

11016000 SPI_CFG0 SPI Configuration 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CS_SETUP_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CS_HOLD_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CS_SETUP_COUNT	**Chip select setup time = (CS_SETUP_COUNT + 1)*CLK_PERIOD; CLK_PERIOD is the cycle time of the clock SPI engine adopts.**
15:0	CS_HOLD_COUNT	**The chip select hold time = (CS_HOLD_COUNT+1) * CLK_PERIOD.**

11016004 SPI_CFG1 SPI Configuration 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GET_TICK_DLY						PACKET_LENGTH									
Type	RW						RW									
Reset	0	0	0				0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PACKET_LOOP_CNT								CS_IDLE_COUNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:29	GET_TICK_DLY	**If the speed of SPI is not fast enough, these three bits can help tolerance get_tick timing. The timing range between get_tick is one cycle depending on the SPI system clock.**
25:16	PACKET_LENGTH	
15:8	PACKET_LOOP_CNT	**PACKET_LENGTH[9:0] defines the number of bytes in one packet, and PACKET_LOOP_CNT[7:0] defines the number of packets within one transaction. The number of bytes in one packet = PACKET_LENGTH + 1. The number of packets in one transaction = PACKET_LOOP_CNT + 1. Total bytes of one transaction = (PACKET_LENGTH + 1)*(PACKET_LOOP_CNT + 1).**
7:0	CS_IDLE_COUNT	**Chip select idle time between consecutive transaction = (CS_HOLD_COUNT + 1)*CLK_PERIOD**

11016008 SPI_TX_SRC SPI TX Source Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_TX_SRC															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_TX_SRC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_TX_SRC	**If TX_DMA_EN is set, the data to be put on the MOSI line will be kept in memory in advance, and the SPI controller will automatically read the data from memory. SPI_TX_SRC defines the memory address from which SPI controller starts to read data.**

1101600C SPI_RX_DST SPI RX Destination Address Register 00000000

Bit Name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SPI_RX_DST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_RX_DST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_RX_DST	**If RX_DMA_EN is set, the received data from the MISO line will be moved to memory automatically by the SPI controller. SPI_RX_DST defines the memory address to which the SPI controller starts to store the data.**

11016010 SPI_TX_DATA SPI TX Data FIFO 00000000

Bit Name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SPI_TX_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_TX_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_TX_DATA	**The depth of the TX FIFO is 32 bytes.** Write to this register will write 4 bytes to TX FIFO. The TX FIFO pointer will automatically move towards the next four bytes. Read from this register will read 4 bytes from FIFO, and TX FIFO pointer will automatically move towards the next four bytes.

Bit(s)	Name	Description

11016014 SPI_RX_DATA SPI RX Data FIFO 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_RX_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_RX_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_RX_DATA	**The depth of the RX FIFO is 32 bytes.** Read from this register will read 4 bytes from RX FIFO. The RX FIFO pointer will automatically move towards the next four bytes. Write to this register will write 4 bytes to FIFO, and the RX FIFO pointer will automatically move towards the next four bytes.

11016018 SPI_CMD SPI Command Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															PAUSE_IE	FINISH_IE
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_ENDIAN	RX_ENDIAN	RXMSBF	TXMSBF	TX_DMA_EN	RX_DMA_EN	CPOL	CPHA	CS_POL	SAMPLE_SEL	CS_DEASSERT_EN	PAUSE_EN		RST	RESUME	CMD_ACT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
17	PAUSE_IE	**Interrupt enable bit of pause flag in SPI status register**
16	FINISH_IE	**Interrupt enable bit of finish flag in SPI status register**
15	TX_ENDIAN	**Defines whether to reverse the endian order of the data DMA from memory** 0: Does not reverse (default) Only supported in DMA mode.
14	RX_ENDIAN	**Defines whether to reverse the endian order of the data DMA to memory** 0: Does not reverse (default)
13	RXMSBF	**Indicates data received from MISO line is MSB first or not** Set RXMSBF to 1 for MSB first; otherwise set it to 0.

Bit(s)	Name	Description
12	TXMSBF	**Indicates data sent on MOSI line is MSB first or not** Set TXMSBF to 1 for MSB first; otherwise set it to 0.
11	TX_DMA_EN	**DMA mode enable bit of the data to be transmitted** 0: Not to enable (default)
10	RX_DMA_EN	**DMA mode enable bit of the data received** 0: Not to enable (default)
9	CPOL	**Control bit of SCK polarity** 0: CPOL = 0 1: CPOL = 1
8	CPHA	**Defines SPI Clock Format 0 or SPI Clock Format 1 during transmission** 0: CPHA = 0 1: CPHA = 1
7	CS_POL	**Control bit of chip select polarity** 0: Active low 1: Active high
6	SAMPLE_SEL	**Control bit of sample edge of MISO** 0: Postive edge 1: Negative edge
5	CS_DEASSERT_EN	**Enable bit of chip select de-assertion mode** Set to 1 to enable this mode.
4	PAUSE_EN	**Enable bit of pause mode** Set to 1 to enable this mode.
2	RST	**Software reset bit** When this bit is 1, software reset will be active high. Default: 0.
1	RESUME	**Used when controller is in PAUSE IDLE state** Write 1 to this bit to trigger the SPI controller to resume transfer from PAUSE IDLE state.
0	CMD_ACT	**Command activate bit** Write 1 to this bit to trigger the SPI controller to start the transaction.

1101601C SPI_STATUS0 SPI Status 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**PAUSE**	**FINISH**
Type															RC	RC
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Interrupt status bit in pause mode** Will be set by the SPI controller when it completes the transaction, entering the PAUSE IDLE state.
0	FINISH	**Interrupt status bit in non-pause mode** Will be set by the SPI controller when it completes the transaction, entering the IDLE state.

11016020 SPI_STATUS1 SPI Status 1 Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BUSY
Type																RO
Reset																1

Bit(s)	Name	Description
0	BUSY	**Status flag reflecting SPI controller is busy or not** This bit is low active; 0 means the SPI controller is busy now. 1'b1:idle 1'bo:busy

11016024 SPI_PAD_MACRO_SEL SPI pad_macro Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PAD_MACRO_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	PAD_MACRO_SEL	**Selects which PAD group SPI will use**

11016028 SPI_CFG2 SPI Configuration 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SCK_LOW_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCK_HIGH_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SCK_LOW_COUNT	**SCK clock low time = (SCK_LOW_COUNT + 1)*CLK_PERIOD**
15:0	SCK_HIGH_COUNT	**SCK clock high time = (SCK_HIGH_COUNT + 1)*CLK_PERIOD**

Bit(s)	Name	Description

1.24 UART4

1.24.1 Introduction

The UART provide full duplex serial communication channels between chip and external devices. The UART has M16C450 and M16550A modes of operation, which are compatible with a range of standard software drivers. The extensions have been designed to be broadly software compatible with 16550A variants, but certain areas offer no consensus.

In common with the M16550A, the UART supports word lengths from 5 to 8 bits, an optional parity bit and one or two stop bits, and is fully programmable by a CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided. The UART also includes two DMA handshake lines, used to indicate when the FIFOs are ready to transfer data to the CPU. Interrupts can be generated from any of the several sources.

After hardware reset, the UART is in M16C450 mode. Its FIFOs can be enabled and the UART can then enter M16550A mode. The UART adds further functionality beyond M16550A mode. Each of the extended functions can be selected individually under software control.

1.24.2 Features

- UART4 is 4 pin (tx, rx,cts,rts) UART channel
- Support both M16C450 and M16550A modes of operation
  - Compatible with standard software drivers
- Transfer system — Asynchronuos
- Data length — 5 to 8 bits
- Hardware flow control — CTS/RTS-based automatic transmit received control
- Software flow control — Use special character Xon/Xoff to do software flow control
- Baud rate — Baud rate is programmable form 300bps to 3Mbps.
- Interrupt request — Received interrupt/Transmit interrupt
- Data transfer — DMA (Transmit/Received) transfer supported.

1.24.3 Register Definition

Module name: uart4 Base address: (+11019000h)

Address	Name	Width	Register Function
11002000	RBR_THR	8	RX Buffer Register / TX Holding Register
11002004	IER	8	Interrupt Enable Register By storing a '1' to a specific bit position, the interrupt associated with that bit is enabled. Otherwise, the interrupt is disabled. IER[7:4] are modified when EFR[4] = 1.
11002008	IIR_FCR	8	Interrupt Identification Register / FIFO Control Register priority is from high to low as following .IIR[5:0]==0X1: no interrupt pending .IIR[5:0]==0X6:line status interrup(Under IER[2]=1). IIR[5:0]==0Xc:rx

Address	Name	Width	Register Function
			data timeout interrup(Under IER[0]=1). IIR[5:0]==0X4:RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached.(Under IER[0]=1) . IIR[5:0]==0X2: TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level(Under IER[1]=1). IIR[5:0]==0X0: modem status change interrupt(Under IER[3]=1). IIR[5:0]==0X10: XOFF character recieved (Under IER[5]=1,EFR[4] = 1). IIR[5:0]==0X20: CTS or RTS Rising edge (Under IER[7]=1,IER[6]=1,EFR[4] = 1).
1100200C	LCR	8	Line Control Register Line Control Register. Determines characteristics of serial communication signals.
11002010	MCR	8	Modem Control Register Modem Control Register. Control interface signals of the UART. MCR[7] can be read when EFR[4] = 1.
11002014	LSR	8	Line Status Register Line Status Register.
11002018	MSR	8	Modem Status Register Note: After a reset, D4-D7 are inputs. A modem status interrupt can be cleared by writing '0' to D0-D3or reading this register. And can be set by writing '1' to D0-D3 or input has changed. D0-D3 can be Modified when != BFh.
1100201C	SCR	8	Scratch Register A general purpose read/write register. After reset, its value is un-defined.
11002090	DLL	8	Divisor Latch (LS) uesd to divid the bclk frequency .
11002094	DLM	8	Divisor Latch (MS) uesd to divid the bclk frequency .
11002098	EFR	8	Enhanced Feature Register
110020A0	XON1	8	XON1 Char Register
110020A4	XON2	8	XON2 Char Register
110020A8	XOFF1	8	XOFF1 Char Register
110020AC	XOFF2	8	XOFF2 Char Register
11002020	AUTOBAUD_EN	8	Auto Baud Detect Enable Register
11002024	HIGHSPEED	8	High Speed Mode Register
11002028	SAMPLE_COUNT	8	Sample Counter Register When HIGHSPEED=3, the sample_count is the threshold value for UART sample counter (sample_num). Count from 0 to sample_count.
1100202C	SAMPLE_POINT	8	Sample Point Register When HIGHSPEED=3, UART gets the input data when sample_count=sample_num. e.g. system clock = 13MHz, 921600 = 13000000 / 14 sample_count = 13 and sample point = 6 (sample the central point to decrease the inaccuracy) The SAMPLE_POINT is usually (SAMPLE_COUNT-1)/2 and remove the decimal.

Address	Name	Width	Register Function
11002030	AUTOBAUD_REG	8	Auto Baud Monitor Register the autobaud detection state ,it will not change until enable the autobaud_en again.
11002034	RATEFIX_AD	8	Clock Rate Fix Register
11002038	AUTOBAUDSAMPLE	8	Auto Baud Sample Register Since the system clock may change, autobaud sample duration should change as system clock changes. When system clock = 13MHz, autobaudsample = 6; when system clock = 26MHz, autobaudsample = 13;When system clock = 52MHz, autobaudsample = 27.
1100203C	GUARD	8	Guard time added register
11002040	ESCAPE_DAT	8	Escape character register
11002044	ESCAPE_EN	8	Escape enable register
11002048	SLEEP_EN	8	Sleep enable register
1100204C	DMA_EN	8	DMA enable register
11002050	RXTRI_AD	8	Rx Trigger Address
11002054	FRACDIV_L	8	Fractional Divider LSB Address
11002058	FRACDIV_M	8	Fractional Divider MSB Address
1100205C	FCR_RD	8	FIFO Control Register
1100209C	FEATURE_SEL	8	UART Feature Select Register For ap mcu side UART ,if use new UART register map feature_sel should keep 1.
110020B0	USB_RX_SEL	8	UART USB rx pin Selection Register
110020B4	SLEEP_REQ	8	uart sleep request register.
110020B8	SLEEP_ACK	8	uart idle register.
110020BC	SPM_SEL	8	SPM interface selection register

11002000 RBR_THR RX Buffer Register / TX Holding Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RBR_THR**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

• Bit(s)	• Name	• Description
• 7:0	• RBR_THR	• **For read : The received data can be read by accessing this register.** • For write : The data to be transmitted is written to this register, and then sent to the PC via serial communication.
•	•	•

11002004 IER Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CTSI	RTSI	XOFFI		EDSSI	ELSI	ETBEI	ERBFI
Type									RW	RW	RW		RW	RW	RW	RW
Reset									0	0	0		0	0	0	0

Bit(s)	Name	Description
7	CTSI	**Masks an interrupt that is generated when a rising edge is detected on the CTS modem control line.** Note: This interrupt is only enabled when hardware flow control is enabled. 0: Mask an interrupt that is generated when a rising edge is detected on the CTS modem control line. 1: Unmask an interrupt that is generated when a rising edge is detected on the CTS modem control line.
6	RTSI	**Masks an interrupt that is generated when a rising edge is detected on the RTS modem control line.** Note: This interrupt is only enabled when hardware flow control is enabled. 0: Mask an interrupt that is generated when a rising edge is detected on the RTS modem control line. 1: Unmask an interrupt that is generated when a rising edge is detected on the RTS modem control line.
5	XOFFI	**Masks an interrupt that is generated when an XOFF character is received.** Note: This interrupt is only enabled when software flow control is enabled. 0: Mask an interrupt that is generated when an XOFF character is received. 1: Unmask an interrupt that is generated when an XOFF character is received.
3	EDSSI	**When set ("1"), an interrupt is generated if DCTS (MSR[0]) becomes set.** 0: No interrupt is generated if DCTS (MSR[0]) becomes set. 1: An interrupt is generated if DCTS (MSR[0]) becomes set.
2	ELSI	**When set ("1"), an interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.** 0: No interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set. 1: An interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.
1	ETBEI	**When set ("1"), an interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level.** 0: No interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level. 1: An interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level

Bit(s)	Name	Description
0	ERBFI	**When set ("1"), an interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached.** 0: No interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. 1: An interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached.

11002008 IIR_FCR Interrupt Identification Register / FIFO Control Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**FIFOE_or_RFTL1_RFTL0**		**ID_or_FIFO_ctrl**					
Type									RW		RW					
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:6	FIFOE_or_RFTL1_RFTL0	**RX FIFO trigger threshold. (RX FIFO contains total 32 bytes.)** 0: 1 1: 6 2: 12 3: RXTRIG
5:0	ID_or_FIFO_ctrl	**IIR_FCR[5:0] for read** Priority Level Interrupt Source 000001 - No interrupt pending 000110 1 Line Status Interrupt: BI, FE, PE or OE set in LSR. (Under IER[2]=1) 001100 2 RX Data Timeout: Timeout on character in RX FIFO. (Under IER[0]=1) 000100 3 RX Data Received: RX Data received or RX Trigger Level reached. (Under IER[0]=1) 000010 4 TX Holding Register Empty: TX Holding Register empty or TX FIFO Trigger Level reached. (Under IER[1]=1) 000000 5 Modem Status change: DDCD, TERI, DDSR or DCTS set in MSR. (Under IER[3]=1) 010000 6 Software Flow Control: XOFF Character received. (Under IER[5]=1) 100000 7 Hardware Flow Control:

Bit(s)	Name	Description
		CTS or RTS Rising Edge. (Under IER[7]=1 or IER[6]=1) Line Status Interrupt: A RX Line Status Interrupt (IIR[5:0] == 000110b) is generated if ELSI (IER[2]) is set and any of BI, FE, PE or OE (LSR[4:1]) becomes set. The interrupt is cleared by reading the Line Status Register. RX Data Timeout Interrupt:When virtual FIFO mode is disabled, RX Data Timeout Interrupt is generated if all of the following apply: 1. FIFO contains at least one character; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register, or on a CPU read from the RX FIFO. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading RX FIFO. When virtual FIFO mode is enabled, RX Data Timeout Interrupt is generated if all of the following apply: 1. FIFO is empty; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register or reading DMA_EN register. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading DMA_EN register. RX Data Received Interrupt: A RX Received interrupt (IER[5:0] == 000100b) is generated if EFRBI (IER[0]) is set and either RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. The interrupt is cleared by reading the RX Buffer Register or the RX FIFO (if enabled). TX Holding Register Empty Interrupt: A TX Holding Register Empty Interrupt (IIR[5:0] = 000010b) is generated if ETRBI (IER[1]) is set and either the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level. The interrupt is cleared by writing to the TX Holding Register or TX FIFO if FIFO enabled. Modem Status Change Interrupt: A Modem Status Change Interrupt (IIR[5:0] = 000000b) is generated if EDSSI (IER[3]) is set and either DDCD, TERI, DDSR or DCTS (MSR[3:0]) becomes set. The interrupt is cleared by reading the Modem Status Register. Software Flow Control Interrupt: A Software Flow Control Interrupt (IIR[5:0] = 010000b) is generated if Software Flow Control is enabled and XOFFI (IER[5]) becomes set, indicating

Bit(s)	Name	Description
		that an XOFF character has been received. The interrupt is cleared by reading the Interrupt Identification Register. Hardware Flow Control Interrupt: A Hardware Flow Control Interrupt (IER[5:0] = 100000b) is generated if Hardware Flow Control is enabled and either RTSI (IER[6]) or CTSI (IER[7]) becomes set indicating that a rising edge has been detected on either the RTS/CTS Modem Control line. The interrupt is cleared by reading the Interrupt Identification Register. ---------- IIR_FCR [5:0] for write IIR_FCR [5:4] TX FIFO trigger threshold (TX FIFO contains total 32 bytes.) 0: 1 1: 6 2: 12 3: RXTRIG IIR_FCR [2] control bit to clear tx fifo 0: no effect 1: clear RX FIFO IIR_FCR [1] control bit to clear rx fifo 0: no effect 1: clear RX FIFO IIR_FCR [0] FIFO Enabled. This bit must be set to 1 for any of the other bits in the registers to have any effect. 0: Disable both the RX and TX FIFOs. 1: Enable both the RX and TX FIFOs.

1100200C LCR Line Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLAB	SB	SP	EPS	PEN	STB	WLS1_WLS0	
Type									RW	RW	RW	RW	RW	RW	RW	
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	DLAB	**Divisor Latch Access Bit.** 0: The RX and TX Registers are read/written at Address 0 and the IER register is read/written at Address 4. 1: The Divisor Latch LS is read/written at Address 0 and the Divisor Latch MS is read/written at Address 4.
6	SB	**Set Break** 0: No effect 1: SOUT signal is forced into the "0" state.
5	SP	**Stick Parity** 0: No effect. 1: The Parity bit is forced into a defined state, depending on the states of EPS and PEN: If EPS=1 & PEN=1, the Parity bit is set and checked = 0. If EPS=0 & PEN=1, the Parity bit is set and checked = 1.
4	EPS	**Even Parity Select** 0: When EPS=0, an odd number of ones is sent and checked. 1: When EPS=1, an even number of ones is sent and checked.
3	PEN	**Parity Enable** 0: The Parity is neither transmitted nor checked. 1: The Parity is transmitted and checked.
2	STB	**Number of STOP bits** 0: One STOP bit is always added. 1: Two STOP bits are added after each character is sent; unless the character length is 5 when 1 STOP bit is added.
1:0	WLS1_WLS0	**Word Length Select.** 0: 5 bits 1: 6 bits 2: 7 bits 3: 8 bits

11002010 MCR Modem Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**XOFF_STATUS**			**Loop**			**RTS**	
Type									RU			RW			RW	
Reset									0			0			0	

Bit(s)	Name	Description
7	XOFF_STATUS	**This is a read-only bit.** 0: When an XON character is received. 1: When an XOFF character is received.
4	Loop	**Loop-back control bit.**

Bit(s)	Name	Description
		0: No loop-back is enabled.
		1: Loop-back mode is enabled.
1	RTS	**Controls the state of the output NRTS, even in loop mode.**
		0: RTS will always output 1.
		1: RTS's output will be controled by flow control condition.

11002014 LSR Line Status Register 00000060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**FIFOERR**	**TEMT**	**THRE**	**BI**	**FE**	**PE**	**OE**	**DR**
Type									RU	RU	RU	RU	RU	RU	RU	RU
Reset									0	1	1	0	0	0	0	0

Bit(s)	Name	Description
7	FIFOERR	**RX FIFO Error Indicator.**
		0: No PE, FE, BI set in the RX FIFO.
		1: Set to 1 when there is at least one PE, FE or BI in the RX FIFO.
6	TEMT	**TX Holding Register (or TX FIFO) and the TX Shift Register are empty.**
		0: Empty conditions below are not met.
		1: If FIFOs are enabled, the bit is set whenever the TX FIFO and the TX Shift Register are empty. If FIFOs are disabled, the bit is set whenever TX Holding Register and TX Shift Register are empty.
5	THRE	**Indicates if there is room for TX Holding Register or TX FIFO is reduced to its Trigger Level.**
		0: Reset whenever the contents of the TX FIFO are more than its Trigger Level (FIFOs are enabled), or whenever TX Holding Register is not empty(FIFOs are disabled).
		1: Set whenever the contents of the TX FIFO are reduced to its Trigger Level (FIFOs are enabled), or whenever TX Holding Register is empty and ready to accept new data (FIFOs are disabled).
4	BI	**Break Interrupt.**
		0: Reset by the CPU reading this register
		1: If the FIFOs are disabled, this bit is set whenever the SIN is held in the 0 state for more than one transmission time (START bit + DATA bits + PARITY + STOP bits).
		If the FIFOs are enabled, this error is associated with a corresponding character in the FIFO and is flagged when this byte is at the top of the FIFO. When a break occurs, only one zero character is loaded into the FIFO: the next character

Bit(s)	Name	Description
		transfer is enabled when SIN goes into the marking state and receives the next valid start bit.
3	FE	**Framing Error.** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit is set if the received data did not have a valid STOP bit. If the FIFOs are enabled, the state of this bit is revealed when the byte it refers to is the next to be read.
2	PE	**Parity Error** 0: Reset by the CPU reading this register 1: If the FIFOs are disabled, this bit is set if the received data did not have a valid parity bit. If the FIFOs are enabled, the state of this bit is revealed when the referred byte is the next to be read.
1	OE	**Overrun Error.** 0: Reset by the CPU reading this register. 1: If the FIFOs are disabled, this bit is set if the RX Buffer was not read by the CPU before new data from the RX Shift Register overwrote the previous contents. If the FIFOs are enabled, an overrun error occurs when the RX FIFO is full and the RX Shift Register becomes full. OE is set as soon as this happens. The character in the Shift Register is then overwritten, but not transferred to the FIFO.
0	DR	**Data Ready.** 0: Cleared by the CPU reading the RX Buffer or by reading all the FIFO bytes. 1: Set by the RX Buffer becoming full or by the FIFO becoming no empty.

11002018 MSR Modem Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**CTS**				**DCTS**
Type												RU				RW
Reset												0				0

Bit(s)	Name	Description
4	CTS	**Clear To Send.** When Loop = "0", this value is the complement of the NCTS input signal. When Loop = "1", this value is equal to the RTS bit in the Modem Control Register.
0	DCTS	**Delta Clear To Send** 0: Cleared if the state of CTS has not changed since this register was last read.

Bit(s)	Name	Description
		1: Set if the state of CTS has changed since this register was last read.

1100201C SCR Scratch Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SCR**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SCR	**A general purpose read/write register. After reset, its value is un-defined.**

11002090 DLL Divisor Latch (LS) 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**DLL**							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:0	DLL	**divisor Latch low 8bit data.**

11002094 DLM Divisor Latch (MS) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**DLM**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DLM	**divisor Latch high 8bit data.** Note: Division by 1 generates a BAUD signal that is constantly high. Note: DLL & DLM setting formula is {DLH,DLL}=(system clock frequency/baud_pulse/baud_rate). When RATE_FIX(RATEFIX_AD[0])=0, system clock frequency = 52MHz. When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=0, system clock frequency = 26MHz. When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=1, system clock frequency = 13MHz. For baud_pulse value refer to HIGH_SPEED(offset=24H) register. e.g. When 52MHz,default speed mode and 115200 baud rate, the {DLH,DLL}=52MHz/16/115200=28.

11002098 EFR Enhanced Feature Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**AUTO_CTS**	**AUTO_RTS**		**ENABLE_E**	**SW_FLOW_CONT**			
Type									RW	RW		RW	RW			
Reset									0	0		0	0	0	0	0

Bit(s)	Name	Description
7	AUTO_CTS	**Enables hardware transmission flow control** 0: Disabled. 1: Enabled.
6	AUTO_RTS	**Enables hardware reception flow control** 0: Disabled. 1: Enabled.
4	ENABLE_E	**Enables enhancement feature** 0: Disabled. 1: Enabled.
3:0	SW_FLOW_CONT	**Software flow control bits.** 00xx: No TX Flow Control 10xx: Transmit XON1/XOFF1 as flow control bytes 01xx: Transmit XON2/XOFF2 as flow control bytes xx00: No RX Flow Control xx10: Receive XON1/XOFF1 as flow control bytes xx01: Receive XON2/XOFF2 as flow control bytes

110020A0 XON1 XON1 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON1	**XON1 character for software flow control.**

110020A4 XON2 XON2 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON2	**XON2 character for software flow control.**

110020A8 XOFF1 XOFF1 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF1	**XOFF1 character for software flow control.**

110020AC XOFF2 XOFF2 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF2	**XOFF2 character for software flow control.**

11002020 AUTOBAUD_EN Auto Baud Detect Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														sleep_ack_sel	AUTOBAUD_SEL	AUTOBAUD_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	sleep_ack_sel	0: can send sleep_ack when autobaud_en is enalbed and autobaud state machine and rx is in idle . 1: can not send sleep_ack when autobaud_en is enabled .
1	AUTOBAUD_SEL	**Auto-baud select** 0: support standard baud rate detection . 1: support non_standard baud rate detection(Just support baud from 300 to 115200, it is recommend to use 52MHZ to auto fix) .
0	AUTOBAUD_EN	**Auto-baud enable signal** 0: Auto-baud function disable 1: Auto-baud function enable (UARTn+0024h SPEED should be set 0) Note: when AUTOBAUD_EN is active, there should not A*/a* char before the auto baud char AT/at, if the A*/a* is Inevitable, the autobaud will fail and please disable the AUTOBAUD_EN to reset the autobaud feature and autobaud_en again.

11002024 HIGHSPEED High Speed Mode Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SPEED	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	SPEED	**UART sample counter base** 0: based on 16*baud_pulse, baud_rate = system clock frequency/16/{DLH, DLL} 1: based on 8*baud_pulse, baud_rate = system clock frequency/8/{DLH, DLL} 2: based on 4*baud_pulse, baud_rate = system clock frequency/4/{DLH, DLL} 3: based on sampe_count * baud_pulse, baud_rate = system clock frequency / (sampe_count+1) / {DLM, DLL}

11002028 SAMPLE_COUNT Sample Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLECOUNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SAMPLECOUNT	**Just be useful when HIGHSPEED mode = 3.**

1100202C SAMPLE_POINT Sample Point Register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLEPOINT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SAMPLEPOINT	**The SAMPLE_POINT is usually (SAMPLE_COUNT-1)/2 and remove the decimal.** sample point , is effective only When HIGHSPEED=3

11002030 AUTOBAUD_REG Auto Baud Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BAUD_STAT				BAUD_RATE			
Type									RU				RU			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:4	BAUD_STAT	**Autobaud format** 0: Autobaud is detecting 1: AT_7N1 2: AT_7O1 3: AT_7E1 4:AT_8N1 5: AT_8O1 6: AT_8E1 7: at_7N1 8: at_7E1 9: at_7O1 10: at_8N1 11: at_8E1 12: at_8O1 13: Autobaud detection fails
3:0	BAUD_RATE	**Autobaud baud rate** 0: 115200 1: 57600 2: 38400 3: 19200 4: 9600 5: 4800 6: 2400 7: 1200 8: 300 9: 110

11002034 RATEFIX_AD Clock Rate Fix Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FREQ_SEL	AUTOBAUD_RATE_FIX	RATE_FIX
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FREQ_SEL	**0: system clock = UART_CLK_SRC/2** 1: system clock = UART_CLK_SRC/4
1	AUTOBAUD_RATE_FIX	**0: system clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz)** 1: system clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depends on FREQ_SEL)
0	RATE_FIX	**0: system clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz)** 1: system clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depends on FREQ_SEL)

11002038 AUTOBAUDSAMPLE Auto Baud Sample Register 0000000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											AUTOBAUDSAMPLE					
Type											RW					
Reset											0	0	1	1	0	1

Bit(s)	Name	Description
5:0	AUTOBAUDSAMPLE	**clk diveision for autobaud rate dectection.** for standard baud rate detection. system clk 52m :'d 27 system clk 26m :'d 13 system clk 13m :'d 6 for non-standard baud rate detection. :15.

1100203C GUARD Guard time added register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												GUARD_EN	GUARD_CNT			
Type												RW	RW			
Reset												0	1	1	1	1

Bit(s)	Name	Description
4	GUARD_EN	**Guard interval add enable signal.** 0: No guard interval added. 1: Add guard interval after stop bit.
3:0	GUARD_CNT	**Guard interval count value. Guard interval = (1/(system clock / div_step / div)) * GUARD_CNT.**

11002040 ESCAPE_DAT Escape character register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ESCAPE_DAT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	ESCAPE_DAT	**Escape character added before software flow control data and escape character, i.e. if tx data is xon (31h), with esc_en =1, uart transmits data as esc + CEh (~xon).**

11002044 ESCAPE_EN Escape enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ESC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	ESC_EN	**Add escape character in transmitter and remove escape character in receiver by UART.** 0: Do not deal with the escape character. 1: Add escape character in transmitter and remove escape character in receiver.

11002048 SLEEP_EN Sleep enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SLEEP_EN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_EN	**For sleep mode issue** 0: Do not deal with sleep mode indicate signal 1: To activate hardware flow control or software control according to software initial setting when chip enters sleep mode. Releasing hardware flow when chip wakes up; but for software control, uart sends xon when awaken and when FIFO does not reach threshold level.

1100204C DMA_EN DMA enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**FIFO_lsr_sel**	**TO_CNT_AUTORST**	**TX_DMA_EN**	**RX_DMA_EN**
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	FIFO_lsr_sel	**fifo lsr mode selection** 0: lsr will update automatically with read data from rx fifo.. 1: lsr will hold the first line status error state until you read the lsr register.

Bit(s)	Name	Description
2	TO_CNT_AUTORST	**Timeout counter auto reset register** 0: After RX timeout happen, SW shall reset the interrupt by reading UART 0x4C. 1: The timeout counter will be auto reset. Set this register when Rain's new DMA is used.
1	TX_DMA_EN	**TX_DMA mechanism enable signal** 0: Do not use DMA in TX. 1: Use DMA in TX. When this reguster is enabled, the flow control is based on the DMA threshold, and generates a timeout interrupt for DMA.for DMA.
0	RX_DMA_EN	**RX_DMA mechanism enable signal** 0: Do not use DMA in RX 1: Use DMA in RX. When this reguster is enabled, the flow control is based on the DMA threshold, and generates a timeout interrupt

11002050 RXTRI_AD Rx Trigger Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RXTRIG			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RXTRIG	**When {rtm,rtl}=2'b11, The Rx FIFO threshold will be Rxtrig.** The value is suggested to be less than half of RX FIFO size, which is 32 Bytes.

11002054 FRACDIV_L Fractional Divider LSB Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FRACDIV_L							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FRACDIV_L	**Add sampling count (+1) from state data7 to data0, in order to contribute fractional divisor.only when high_speed==3.**

11002058 FRACDIV_M Fractional Divider MSB Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**FRACDIV_M**	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	FRACDIV_M	**Add sampling count when in state stop to parity, in order to contribute fractional divisor.only when high_speed==3.**

1100205C FCR_RD FIFO Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RFTL1_RFTL0**		**TFTL1_TFTL0**			**CLRT**	**CLRR**	**FIFOE**
Type									RO		RO			RO	RO	RO
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:6	RFTL1_RFTL0	**RX FIFO trigger threshold. (RX FIFO contains total 32 bytes.)** 0: 1 1: 6 2: 12 3: RXTRIG
5:4	TFTL1_TFTL0	**TX FIFO trigger threshold (TX FIFO contains total 32 bytes.)** 0: 1 1: 4 2: 8 3: 14

Bit(s)	Name	Description
2	CLRT	0: TX FIFO is not cleared 1: TX FIFO is cleared
1	CLRR	0: RX FIFO is not cleared 1: RX FIFOis cleared
0	FIFOE	**FIFO Enabled. This bit must be set to 1 for any of the other bits in the registers to have any effect.** 0: the RX and TX FIFOs are not enabled.. 1: RX and TX FIFOs are enabled.

1100209C FEATURE_SEL UART Feature Select Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FEATURE_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	FEATURE_SEL	**For ap mcu side UART ,if use new UART register map feature_sel should keep 1.** 0: Disable new register map. 1: Enable new register map.

110020B0 USB_RX_SEL UART USB rx pin Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																USB_RX_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	USB_RX_SEL	0: uart rx pin is selected. 1: usb rx pin is selected.

110020B4 SLEEP_REQ uart sleep request register. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_REQ
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_REQ	0: cancel sleep request to uart.(after wake up sent by cpu) 1: send sleep request to uart.(before sleep sent by cpu)

110020B8 SLEEP_ACK uart idle register. 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_ACK
Type																RU
Reset																1

Bit(s)	Name	Description
0	SLEEP_ACK	0: uart is not in idle state.(cpu can polling this register to get the uart state) 1: uart is in idle state.(cpu can polling this register to get the uart state)

110020BC SPM_SEL SPM interface selection register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SPM_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	SPM_SEL	0: SPM sleep interface will not be used. 1: SPM sleep interface will be used.

1.25 AUDIO

1.25.1 Introduction

The audio system provides the audio data exchange ability. The interfaces are list as follows:

- Master/Slave I2S input interface with SRC x 4
- Master/Slave I2S output interface with SRC x 4
- DIR(SPDIF-Input) x1
- SPDIF-Output x1
- Master TDM TX x1
- Master TDM RX x1

1.25.2 Features

The audio system is responsible for generating the following clock signals:

- **I2S**
  - Supports master/slave input mode
  - Supports master/slave output mode
  - Supports 32-bit stereo data
  - Supports 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, 176.4, and 192kHz sampling rate in both master and slave mode
  - Supports LJ/I2S/RJ format
  - Supports I2S input/output with the same sampling rate at the same time
  - Supports MCLK frequency range is 2.304~24.576MHz

- **DIR (SPDIF-In)**
  - supports SPDIF input decode
  - supports 32, 44.1, 48, 88.2, and 96KHz sample rate
- **SPDIF-Out**
  - supports SPDIF output encode
  - supports 32, 44.1, 48, 88.2, and 96KHz sample rate
- **TDM TX**
  - supports Time Division Multiplexer I2S output (master mode only)
  - supports eight, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, and 192KHz sample rate
  - supports channel number up to 2/4/8/12/16 in configuration by 1 data pins
  - dedicated pin for TDM TX (not share clock pins with TDM RX)
- **TDM RX**
  - supports Time Division Multiplexer I2S intput (master mode only)
  - supports 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, and 192KHz sample rate
  - supports channel number up to 2/4/8/12/16 in 1 serial data pin
  - dedicated pin for TDM RX (not share clock pins with TDM TX)
  - Can share clock pin with TDM TX.

1.25.3 Register Definitions

Module name: AFE Base address: (+11220000h)

Address	Name	Width	Register Function
11220000	AUDIO_TOP_CON0	32	Audio Top Control Register 0
11220004	AUDIO_TOP_CON1	32	Audio Top Control Register 1
11220008	AUDIO_TOP_CON2	32	Audio Top Control Register 2
1122000C	AUDIO_TOP_CON3	32	Audio Top Control Register 3
11220010	AUDIO_TOP_CON4	32	Audio Top Control Register 4
11220014	AUDIO_TOP_CON5	32	Audio Top Control Register 5
11220400	AUDIO_TOP_STA0	32	Audio Top Status 0
11220404	AUDIO_TOP_STA1	32	Audio Top Status 1
1122001C	AFE_DAIBT_CON0	32	AFE DAI/BT CONTROL REGISTER0
11220100	ASMI_TIMING_CON1	32	ASM_IN_TIMING_SEL
11220104	ASMO_TIMING_CON1	32	ASM_OUT_TIMING_SEL
11220108	PWR1_ASM_CON1	32	PWR1_ASM_CALI_CK_SEL
112201F0	AFE_SINEGEN_CON0	32	AFE Sine-wave Gen Config 0
11220320	AFE_BT_SECURITY0	16	daibt data array control
11220324	AFE_BT_SECURITY1	8	daibt data array control
11220360	AFE_SPDIF2_OUT_CON0	8	AFE SPDIF2 Ouput Control Register
11220364	AFE_SPDIF2_BASE	32	AFE SPDIF2 Base Address Register
11220368	AFE_SPDIF2_CUR	32	AFE SPDIF2 Cursor Register
1122036C	AFE_SPDIF2_END	32	AFE_SPDIF2_END
11220370	AFE_TDM_OUT_CON0	32	AFE HDMI_OUT Control Register 0
11220374	AFE_TDM_OUT_BASE	32	AFE HDMI_OUT Base Address Register
11220378	AFE_TDM_OUT_CUR	32	AFE HDMI_OUT Cursor Register
1122037C	AFE_TDM_OUT_END	32	AFE_TDM_OUT_END
11220380	AFE_SPDIF_OUT_CON0	8	AFE SPDIF Ouput Control Register
11220384	AFE_SPDIF_BASE	32	AFE SPDIF Base Address Register
11220388	AFE_SPDIF_CUR	32	AFE SPDIF Cursor Register
1122038C	AFE_SPDIF_END	32	AFE_SPDIF_END
11220390	AFE_HDMI_CONN0	32	AFE HDMI Output Connection Control Register 0
11220394	AFE_8CH_I2S_OUT_CON	32	AFE HDMI 8CH I2S out Control Register 0
11220398	AFE_HDMI_CONN1	32	AFE HDMI Output Connection Control Register 1
1122039C	AFE_HDMI_CONN2	32	AFE HDMI Output Connection Control Register 2
112203A0	AFE_IRQ_MCU_CON	32	AFE IRQ MCU Control Register
112203A4	AFE_IRQ_MCU_STATUS	32	AFE IRQ MCU Status Register
112203A8	AFE_IRQ_CLR	32	AFE IRQ Clear Register
112203AC	AFE_IRQ_MCU_CNT1	32	AFE IRQ1 MCU Counter Register
112203B0	AFE_IRQ_MCU_CNT2	32	AFE IRQ2 MCU Counter Register
112203B8	AFE_IRQ_MCU_MON2	32	AFE IRQ MCU MON2 Register
112203BC	AFE_IRQ_MCU_CNT5	32	AFE IRQ5 MCU Counter Register
112203C0	AFE_IRQ1_MCU_CNT_MON	32	AFE IRQ1 MCU Count Monitor Register

Address	Name	Width	Register Function
112203C4	AFE_IRQ2_MCU_CNT_MON	32	AFE IRQ2 MCU Count Monitor Register
112203C8	AFE_IRQ1_MCU_EN_CNT_MON	32	AFE IRQ1 MCU Enable Count Monitor Register
112203CC	AFE_IRQ5_MCU_CNT_MON	32	AFE IRQ5 MCU Count Monitor Register
112203D0	AFE_IRQ_MCU_EN	16	AFE IRQ MCU Enable Register
11220410	AFE_GAIN1_CON0	32	AFE Gain1 Control Register 0
11220414	AFE_GAIN1_CON1	32	AFE Gain1 Control Register 1
11220418	AFE_GAIN1_CON2	32	AFE Gain1 Control Register 2
1122041C	AFE_GAIN1_CON3	32	AFE Gain1 Control Register 3
11220424	AFE_GAIN1_CUR	32	AFE Gain1 Cursor Register
11220428	AFE_GAIN2_CON0	32	AFE Gain2 Control Register 0
1122042C	AFE_GAIN2_CON1	32	AFE Gain2 Control Register 1
11220430	AFE_GAIN2_CON2	32	AFE Gain2 Control Register 2
11220434	AFE_GAIN2_CON3	32	AFE Gain2 Control Register 3
1122043C	AFE_GAIN2_CUR	32	AFE Gain2 Cursor Register
11220480	AFE_IEC_CFG	32	AFE IEC958 Config
11220484	AFE_IEC_NSNUM	32	AFE IEC958 Next Interrupt Number
11220488	AFE_IEC_BURST_INFO	24	AFE IEC958 Register Lock Status
1122048C	AFE_IEC_BURST_LEN	24	AFE IEC958 Burst Length
11220490	AFE_IEC_NSADR	32	AFE IEC958 Next Source Address
112204A0	AFE_IEC_CHL_STAT0	32	AFE IEC958 L-Channel Status Register 0
112204A4	AFE_IEC_CHL_STAT1	16	AFE IEC958 L-Channel Status Register 1
112204A8	AFE_IEC_CHR_STAT0	32	AFE IEC958 R-Channel Status Register 0
112204AC	AFE_IEC_CHR_STAT1	16	AFE IEC958 R-Channel Status Register 1
112204B0	AFE_IEC2_CFG	32	AFE IEC958-2 Config
112204B4	AFE_IEC2_NSNUM	32	AFE IEC958-2 Next Interrupt Number
112204B8	AFE_IEC2_BURST_INFO	24	AFE IEC958-2 Register Lock Status
112204BC	AFE_IEC2_BURST_LEN	24	AFE IEC958-2 Burst Length
112204C0	AFE_IEC2_NSADR	32	AFE IEC958-2 Next Source Address
112204D0	AFE_IEC2_CHL_STAT0	32	AFE IEC958-2 L-Channel Status Register 0
112204D4	AFE_IEC2_CHL_STAT1	16	AFE IEC958-2 L-Channel Status Register 1
112204D8	AFE_IEC2_CHR_STAT0	32	AFE IEC958-2 R-Channel Status Register 0
112204DC	AFE_IEC2_CHR_STAT1	16	AFE IEC958-2 R-Channel Status Register 1
11220500	AFE_SPDIFIN_CFG0	32	AFE SPDIFIN Control Register0
11220504	AFE_SPDIFIN_CFG1	32	AFE SPDIFIN Control Register1
11220508	AFE_SPDIFIN_CHSTS1	32	SPDIFIN channel status 1
1122050C	AFE_SPDIFIN_CHSTS2	32	SPDIFIN channel status 2
11220510	AFE_SPDIFIN_CHSTS3	32	SPDIFIN channel status 3
11220514	AFE_SPDIFIN_CHSTS4	32	SPDIFIN channel status 4
11220518	AFE_SPDIFIN_CHSTS5	32	SPDIFIN channel status 5
1122051C	AFE_SPDIFIN_CHSTS6	32	SPDIFIN channel status 6
11220520	AFE_SPDIFIN_DEBUG1	32	SPDIFIN DEBUG status 1
11220524	AFE_SPDIFIN_DEBUG2	32	SPDIFIN DEBUG status 2
11220528	AFE_SPDIFIN_DEBUG3	32	SPDIFIN DEBUG status 3

Address	Name	Width	Register Function
1122052C	AFE_SPDIFIN_DEBUG4	32	SPDIFIN DEBUG status 4
11220530	AFE_SPDIFIN_EC	32	SPDIFIN edge Clear
11220534	AFE_SPDIFIN_CKLOCK_CFG	32	SPDIFIN Clock Lock Configuration
1122053C	AFE_SPDIFIN_BR	32	SPDIFIN bitclk recovery Configuration
11220540	AFE_SPDIFIN_BR_DBG1	32	SPDIFIN bitclk recovery debug information 1
11220544	AFE_SPDIFIN_CKFBDIV	32	SPDIFIN CKFBDIV
11220548	AFE_SPDIFIN_INT_EXT	32	
1122054C	AFE_SPDIFIN_INT_EXT2	32	
11220550	SPDIFIN_FREQ_INFO	32	SPDIFIN rough frequency detection information setup
11220554	SPDIFIN_FREQ_INFO_2	32	SPDIFIN rough frequency detection information setup2
11220558	SPDIFIN_FREQ_INFO_3	32	SPDIFIN rough frequency detection information setup 3
1122055C	SPDIFIN_FREQ_STATUS	32	SPDIFIN rough frequency detection status
11220560	SPDIFIN_USERCODE1	32	SPDIFIN Usercode 1
11220564	SPDIFIN_USERCODE2	32	SPDIFIN Usercode 2
11220568	SPDIFIN_USERCODE3	32	SPDIFIN Usercode 3
1122056C	SPDIFIN_USERCODE4	32	SPDIFIN Usercode 4
11220570	SPDIFIN_USERCODE5	32	SPDIFIN Usercode 5
11220574	SPDIFIN_USERCODE6	32	SPDIFIN Usercode 6
11220578	SPDIFIN_USERCODE7	32	SPDIFIN Usercode 7
1122057C	SPDIFIN_USERCODE8	32	SPDIFIN Usercode 8
11220580	SPDIFIN_USERCODE9	32	SPDIFIN Usercode 9
11220584	SPDIFIN_USERCODE10	32	SPDIFIN Usercode 10
11220588	SPDIFIN_USERCODE11	32	SPDIFIN Usercode 11
1122058C	SPDIFIN_USERCODE12	32	SPDIFIN Usercode 12
11220590	AFE_HADDS2_CON	32	HADDS2 PCW
11220594	AFE_SPDIFIN_APLL_TUNER_CFG	32	SPDIFIN APLL tuner config
11220598	AFE_SPDIFIN_APLL_TUNER_CFG1	32	SPDIFIN APLL tuner config1
112205F0	I2SIN_BCOUNT_MON	32	I2S in bcount monitor
112205F4	I2SO_BCOUNT_MON	32	I2S out bcount monitor
112205F8	I2S_UNUSED_BCOUNT_MON	32	I2S 5,6 bcount monitor
11220600	ASYS_TOP_CON	32	PCM Interface Config 1
11220604	ASYS_I2SIN1_CON	32	I2S in1 Control Register
11220608	ASYS_I2SIN2_CON	32	I2S in2 Control Register
1122060C	ASYS_I2SIN3_CON	32	I2S in3 Control Register
11220610	ASYS_I2SIN4_CON	32	I2S in4 Control Register
11220614	ASYS_I2SIN5_CON	32	I2S in5 Control Register
11220618	ASYS_I2SIN6_CON	32	I2S in6 Control Register
1122061C	ASYS_I2SO1_CON	32	I2S out1 Control Register
11220620	ASYS_I2SO2_CON	32	I2S out2 Control Register

Address	Name	Width	Register Function
11220624	ASYS_I2SO3_CON	32	I2S out3 Control Register
11220628	ASYS_I2SO4_CON	32	I2S out4 Control Register
1122062C	ASYS_I2SO5_CON	32	I2S out5 Control Register
11220630	ASYS_I2SO6_CON	32	I2S out6 Control Register
11220634	PWR2_TOP_CON	32	PWR2_TOP_CON
1122063C	PCM_INTF_CON1	32	PCM Interface Config 1
11220640	PCM_INTF_CON2	32	PCM Interface Config 2
11220648	DSD1_FADER_CON0	32	dsd1 fader control
1122064C	DSD2_FADER_CON0	32	dsd2 fader control
11220650	DSD_FADER_MON	32	dsd fader moniter
112206C0	AFE_CONN0	32	AFE Connection Register 0
112206C4	AFE_CONN1	32	AFE Connection Register 1
112206C8	AFE_CONN2	32	AFE Connection Register 2
112206CC	AFE_CONN3	32	AFE Connection Register 3
112206D0	AFE_CONN4	32	AFE Connection Register 4
112206D4	AFE_CONN5	32	AFE Connection Register 5
112206D8	AFE_CONN6	32	AFE Connection Register 6
112206DC	AFE_CONN7	32	AFE Connection Register 7
112206E0	AFE_CONN8	32	AFE Connection Register 8
112206E4	AFE_CONN9	32	AFE Connection Register 9
112206E8	AFE_CONN10	32	AFE Connection Register 10
112206EC	AFE_CONN11	32	AFE Connection Register 11
112206F0	AFE_CONN12	32	AFE Connection Register 12
112206F4	AFE_CONN13	32	AFE Connection Register 13
112206F8	AFE_CONN14	32	AFE Connection Register 14
112206FC	AFE_CONN15	32	AFE Connection Register 15
11220700	AFE_CONN16	32	AFE Connection Register 16
11220704	AFE_CONN17	32	AFE Connection Register 17
11220708	AFE_CONN18	32	AFE Connection Register 18
1122070C	AFE_CONN19	32	AFE Connection Register 19
11220710	AFE_CONN20	32	AFE Connection Register 20
11220714	AFE_CONN21	32	AFE Connection Register 21
11220718	AFE_CONN22	32	AFE Connection Register 22
1122071C	AFE_CONN23	32	AFE Connection Register 23
11220720	AFE_CONN24	32	AFE Connection Register 24
11220724	AFE_CONN25	32	AFE Connection Register 25
11220728	AFE_CONN26	32	AFE Connection Register 26
1122072C	AFE_CONN27	32	AFE Connection Register 27
11220730	AFE_CONN28	32	AFE Connection Register 28
11220734	AFE_CONN29	32	AFE Connection Register 29
11220738	AFE_CONN30	32	AFE Connection Register 30
1122073C	AFE_CONN31	32	AFE Connection Register 31
11220740	AFE_CONN32	32	AFE Connection Register 32
11220744	AFE_CONN33	32	AFE Connection Register 33
11220748	AFE_CONN34	32	AFE Connection Register 34

Address	Name	Width	Register Function
1122074C	AFE_CONN35	32	AFE Connection Register 35
11220750	AFE_CONN36	32	AFE Connection Register 36
11220754	AFE_CONN37	32	AFE Connection Register 37
11220758	AFE_CONN38	32	AFE Connection Register 38
1122075C	AFE_CONN39	32	AFE Connection Register 39
11220760	AFE_CONN40	32	AFE Connection Register 40
11220764	AFE_CONN41	32	AFE Connection Register 41
11220768	AFE_CONN_24BIT	32	AFE CONNECTION 24BIT REGISTER
1122076C	AFE_CONN_16BIT	32	AFE CONNECTION 16BIT REGISTER
1122077C	ASYS_IRQ_CONFIG	32	IRQ MON sel
11220780	ASYS_IRQ1_CON	32	ASYS IRQ1 CONTROL
11220784	ASYS_IRQ2_CON	32	ASYS IRQ2 CONTROL
11220788	ASYS_IRQ3_CON	32	ASYS IRQ3 CONTROL
1122078C	ASYS_IRQ4_CON	32	ASYS IRQ4 CONTROL
11220790	ASYS_IRQ5_CON	32	ASYS IRQ5 CONTROL
11220794	ASYS_IRQ6_CON	32	ASYS IRQ6 CONTROL
11220798	ASYS_IRQ7_CON	32	ASYS IRQ7 CONTROL
1122079C	ASYS_IRQ8_CON	32	ASYS IRQ8 CONTROL
112207A0	ASYS_IRQ9_CON	32	ASYS IRQ9 CONTROL
112207A4	ASYS_IRQ10_CON	32	ASYS IRQ10 CONTROL
112207A8	ASYS_IRQ11_CON	32	ASYS IRQ11 CONTROL
112207AC	ASYS_IRQ12_CON	32	ASYS IRQ12 CONTROL
112207B0	ASYS_IRQ13_CON	32	ASYS IRQ13 CONTROL
112207B4	ASYS_IRQ14_CON	32	ASYS IRQ14 CONTROL
112207B8	ASYS_IRQ15_CON	32	ASYS IRQ15 CONTROL
112207BC	ASYS_IRQ16_CON	32	ASYS IRQ16 CONTROL
112207C0	ASYS_IRQ_CLR	32	ASYS IRQ CLEAR
112207C4	ASYS_IRQ_STATUS	32	ASYS IRQ STATUS
112207C8	ASYS_IRQ_MON1	32	ASYS IRQ MON1
112207CC	ASYS_IRQ_MON2	32	ASYS IRQ MON2
11221180	DMIC_TOP_CON	32	Digital mic control
11221184	DMIC_ULCF_CON1	32	DMIC fir filter coef
11221188	DMIC_ULCF_CON2	32	DMIC fir filter coef
1122118C	DMIC_ULCF_CON3	32	DMIC fir filter coef
11221190	DMIC_ULCF_CON4	32	DMIC fir filter coef
11221194	DMIC_ULCF_CON5	32	DMIC fir filter coef
11221198	DMIC_ULCF_CON6	32	DMIC fir filter coef
1122119C	DMIC_ULCF_CON7	32	DMIC fir filter coef
112211A0	DMIC_ULCF_CON8	32	DMIC fir filter coef
112211A4	DMIC_ULCF_CON9	32	DMIC fir filter coef
112211A8	DMIC_ULCF_CON10	32	DMIC fir filter coef
112211AC	DMIC_ULCF_CON11	32	DMIC fir filter coef
112211B0	DMIC_ULCF_CON12	32	DMIC fir filter coef
112211B4	DMIC_ULCF_CON13	32	DMIC fir filter coef
112211B8	DMIC_ULCF_CON14	32	DMIC fir filter coef

Address	Name	Width	Register Function
112211BC	DMIC_ULCF_CON15	32	DMIC fir filter coef
11221030	DMIC2_TOP_CON	32	Digital mic control
11221034	DMIC2_ULCF_CON1	32	DMIC fir filter coef
11221038	DMIC2_ULCF_CON2	32	DMIC fir filter coef
1122103C	DMIC2_ULCF_CON3	32	DMIC fir filter coef
11221040	DMIC2_ULCF_CON4	32	DMIC fir filter coef
11221044	DMIC2_ULCF_CON5	32	DMIC fir filter coef
11221048	DMIC2_ULCF_CON6	32	DMIC fir filter coef
1122104C	DMIC2_ULCF_CON7	32	DMIC fir filter coef
11221050	DMIC2_ULCF_CON8	32	DMIC fir filter coef
11221054	DMIC2_ULCF_CON9	32	DMIC fir filter coef
11221058	DMIC2_ULCF_CON10	32	DMIC fir filter coef
1122105C	DMIC2_ULCF_CON11	32	DMIC fir filter coef
11221060	DMIC2_ULCF_CON12	32	DMIC fir filter coef
11221064	DMIC2_ULCF_CON13	32	DMIC fir filter coef
11221068	DMIC2_ULCF_CON14	32	DMIC fir filter coef
1122106C	DMIC2_ULCF_CON15	32	DMIC fir filter coef
11221070	PWR2_ASM_CON1	32	sample base ASRC clock selection
11221074	PWR2_ASM_CON2	32	mem base ASRC clock selection
11221078	PWR2_ASM_CON3	32	ASM BRIDGE control
1122107C	PWR2_ASM_CON4	32	ASM BRIDGE control
11221080	PWR2_ASM_MON0	32	ASM BRIDGE control
11221084	PWR2_ASM_MON1	32	ASM BRIDGE control
11221088	AFE_LRCK_CNT	32	lrck number count and read control
1122108C	MASM_TRAC_CON1	32	asrc cali lrck sel
11220800	AFE_ASRC_NEW_CON0	32	ASRC Config 0
11220804	AFE_ASRC_NEW_CON1	32	ASRC Config 1
11220808	AFE_ASRC_NEW_CON2	32	ASRC Config 2
1122080C	AFE_ASRC_NEW_CON3	32	ASRC Config 3
11220810	AFE_ASRC_NEW_CON4	32	ASRC Config 4
11220814	AFE_ASRC_NEW_CON5	32	ASRC Config 5
11220818	AFE_ASRC_NEW_CON6	32	ASRC Config 6
1122081C	AFE_ASRC_NEW_CON7	32	ASRC Config 7
11220820	AFE_ASRC_NEW_CON8	32	ASRC Config 8
11220824	AFE_ASRC_NEW_CON9	32	ASRC Config 9
11220828	AFE_ASRC_NEW_CON10	32	ASRC Config 10
1122082C	AFE_ASRC_NEW_CON11	32	ASRC Config 11
11220834	AFE_ASRC_NEW_CON13	32	ASRC Config 13
11220838	AFE_ASRC_NEW_CON14	32	ASRC Config 14
11220840	AFE_ASRCI2_NEW_CON0	32	ASRC Config 0
11220844	AFE_ASRCI2_NEW_CON1	32	ASRC Config 1
11220848	AFE_ASRCI2_NEW_CON2	32	ASRC Config 2

Address	Name	Width	Register Function
1122084C	AFE_ASRCI2_NEW_CON3	32	ASRC Config 3
11220850	AFE_ASRCI2_NEW_CON4	32	ASRC Config 4
11220854	AFE_ASRCI2_NEW_CON5	32	ASRC Config 5
11220858	AFE_ASRCI2_NEW_CON6	32	ASRC Config 6
1122085C	AFE_ASRCI2_NEW_CON7	32	ASRC Config 7
11220860	AFE_ASRCI2_NEW_CON8	32	ASRC Config 8
11220864	AFE_ASRCI2_NEW_CON9	32	ASRC Config 9
11220868	AFE_ASRCI2_NEW_CON10	32	ASRC Config 10
1122086C	AFE_ASRCI2_NEW_CON11	32	ASRC Config 11
11220874	AFE_ASRCI2_NEW_CON13	32	ASRC Config 13
11220878	AFE_ASRCI2_NEW_CON14	32	ASRC Config 14
11220880	AFE_ASRCI3_NEW_CON0	32	ASRC Config 0
11220884	AFE_ASRCI3_NEW_CON1	32	ASRC Config 1
11220888	AFE_ASRCI3_NEW_CON2	32	ASRC Config 2
1122088C	AFE_ASRCI3_NEW_CON3	32	ASRC Config 3
11220890	AFE_ASRCI3_NEW_CON4	32	ASRC Config 4
11220894	AFE_ASRCI3_NEW_CON5	32	ASRC Config 5
11220898	AFE_ASRCI3_NEW_CON6	32	ASRC Config 6
1122089C	AFE_ASRCI3_NEW_CON7	32	ASRC Config 7
112208A0	AFE_ASRCI3_NEW_CON8	32	ASRC Config 8
112208A4	AFE_ASRCI3_NEW_CON9	32	ASRC Config 9
112208A8	AFE_ASRCI3_NEW_CON10	32	ASRC Config 10
112208AC	AFE_ASRCI3_NEW_CON11	32	ASRC Config 11
112208B4	AFE_ASRCI3_NEW_CON13	32	ASRC Config 13
112208B8	AFE_ASRCI3_NEW_CON14	32	ASRC Config 14
112208C0	AFE_ASRCI4_NEW_CON0	32	ASRC Config 0

Address	Name	Width	Register Function
112208C4	AFE_ASRCI4_NEW_CON1	32	ASRC Config 1
112208C8	AFE_ASRCI4_NEW_CON2	32	ASRC Config 2
112208CC	AFE_ASRCI4_NEW_CON3	32	ASRC Config 3
112208D0	AFE_ASRCI4_NEW_CON4	32	ASRC Config 4
112208D4	AFE_ASRCI4_NEW_CON5	32	ASRC Config 5
112208D8	AFE_ASRCI4_NEW_CON6	32	ASRC Config 6
112208DC	AFE_ASRCI4_NEW_CON7	32	ASRC Config 7
112208E0	AFE_ASRCI4_NEW_CON8	32	ASRC Config 8
112208E4	AFE_ASRCI4_NEW_CON9	32	ASRC Config 9
112208E8	AFE_ASRCI4_NEW_CON10	32	ASRC Config 10
112208EC	AFE_ASRCI4_NEW_CON11	32	ASRC Config 11
112208F4	AFE_ASRCI4_NEW_CON13	32	ASRC Config 13
112208F8	AFE_ASRCI4_NEW_CON14	32	ASRC Config 14
11220940	AFE_ASRCO1_NEW_CON0	32	ASRC Config 0
11220944	AFE_ASRCO1_NEW_CON1	32	ASRC Config 1
11220948	AFE_ASRCO1_NEW_CON2	32	ASRC Config 2
1122094C	AFE_ASRCO1_NEW_CON3	32	ASRC Config 3
11220950	AFE_ASRCO1_NEW_CON4	32	ASRC Config 4
11220954	AFE_ASRCO1_NEW_CON5	32	ASRC Config 5
11220958	AFE_ASRCO1_NEW_CON6	32	ASRC Config 6
1122095C	AFE_ASRCO1_NEW_CON7	32	ASRC Config 7
11220960	AFE_ASRCO1_NEW_CON8	32	ASRC Config 8
11220964	AFE_ASRCO1_NEW_CON9	32	ASRC Config 9
11220968	AFE_ASRCO1_NEW_CON10	32	ASRC Config 10
1122096C	AFE_ASRCO1_NEW_CON11	32	ASRC Config 11
11220974	AFE_ASRCO1_NEW_CON13	32	ASRC Config 13

Address	Name	Width	Register Function
11220978	AFE_ASRCO1_NEW_CON14	32	ASRC Config 14
11220980	AFE_ASRCO2_NEW_CON0	32	ASRC Config 0
11220984	AFE_ASRCO2_NEW_CON1	32	ASRC Config 1
11220988	AFE_ASRCO2_NEW_CON2	32	ASRC Config 2
1122098C	AFE_ASRCO2_NEW_CON3	32	ASRC Config 3
11220990	AFE_ASRCO2_NEW_CON4	32	ASRC Config 4
11220994	AFE_ASRCO2_NEW_CON5	32	ASRC Config 5
11220998	AFE_ASRCO2_NEW_CON6	32	ASRC Config 6
1122099C	AFE_ASRCO2_NEW_CON7	32	ASRC Config 7
112209A0	AFE_ASRCO2_NEW_CON8	32	ASRC Config 8
112209A4	AFE_ASRCO2_NEW_CON9	32	ASRC Config 9
112209A8	AFE_ASRCO2_NEW_CON10	32	ASRC Config 10
112209AC	AFE_ASRCO2_NEW_CON11	32	ASRC Config 11
112209B4	AFE_ASRCO2_NEW_CON13	32	ASRC Config 13
112209B8	AFE_ASRCO2_NEW_CON14	32	ASRC Config 14
112209C0	AFE_ASRCO3_NEW_CON0	32	ASRC Config 0
112209C4	AFE_ASRCO3_NEW_CON1	32	ASRC Config 1
112209C8	AFE_ASRCO3_NEW_CON2	32	ASRC Config 2
112209CC	AFE_ASRCO3_NEW_CON3	32	ASRC Config 3
112209D0	AFE_ASRCO3_NEW_CON4	32	ASRC Config 4
112209D4	AFE_ASRCO3_NEW_CON5	32	ASRC Config 5
112209D8	AFE_ASRCO3_NEW_CON6	32	ASRC Config 6
112209DC	AFE_ASRCO3_NEW_CON7	32	ASRC Config 7
112209E0	AFE_ASRCO3_NEW_CON8	32	ASRC Config 8
112209E4	AFE_ASRCO3_NEW_CON9	32	ASRC Config 9
112209E8	AFE_ASRCO3_NEW_CON10	32	ASRC Config 10

Address	Name	Width	Register Function
112209EC	AFE_ASRC03_NEW_CON11	32	ASRC Config 11
112209F4	AFE_ASRC03_NEW_CON13	32	ASRC Config 13
112209F8	AFE_ASRC03_NEW_CON14	32	ASRC Config 14
11220A00	AFE_ASRC04_NEW_CON0	32	ASRC Config 0
11220A04	AFE_ASRC04_NEW_CON1	32	ASRC Config 1
11220A08	AFE_ASRC04_NEW_CON2	32	ASRC Config 2
11220A0C	AFE_ASRC04_NEW_CON3	32	ASRC Config 3
11220A10	AFE_ASRC04_NEW_CON4	32	ASRC Config 4
11220A14	AFE_ASRC04_NEW_CON5	32	ASRC Config 5
11220A18	AFE_ASRC04_NEW_CON6	32	ASRC Config 6
11220A1C	AFE_ASRC04_NEW_CON7	32	ASRC Config 7
11220A20	AFE_ASRC04_NEW_CON8	32	ASRC Config 8
11220A24	AFE_ASRC04_NEW_CON9	32	ASRC Config 9
11220A28	AFE_ASRC04_NEW_CON10	32	ASRC Config 10
11220A2C	AFE_ASRC04_NEW_CON11	32	ASRC Config 11
11220A34	AFE_ASRC04_NEW_CON13	32	ASRC Config 13
11220A38	AFE_ASRC04_NEW_CON14	32	ASRC Config 14
11220B00	ASRC_GEN_CONF	32	ASRC_GEN_CONF
11220B04	ASRC_IER	32	ASRC_IER
11220B08	ASRC_IFR	32	ASRC_IFR
11220B10	ASRC_CH01_CNFG	32	ASRC_CH01_CNFG
11220B20	ASRC_FREQUENCY_0	32	ASRC_FREQUENCY_0
11220B24	ASRC_FREQUENCY_1	32	ASRC_FREQUENCY_1
11220B28	ASRC_FREQUENCY_2	32	ASRC_FREQUENCY_2
11220B2C	ASRC_FREQUENCY_3	32	ASRC_FREQUENCY_3
11220B30	ASRC_IBUF_SADR	32	ASRC_IBUF_SADR
11220B34	ASRC_IBUF_SIZE	32	ASRC_IBUF_SIZE
11220B38	ASRC_OBUF_SADR	32	ASRC_OBUF_SADR
11220B3C	ASRC_OBUF_SIZE	32	ASRC_OBUF_SIZE
11220B40	ASRC_CH01_IBUF_RDPNT	32	ASRC_CH01_IBUF_RDPNT
11220B50	ASRC_CH01_IBUF_WRPNT	32	ASRC_CH01_IBUF_WRPNT

Address	Name	Width	Register Function
11220B60	ASRC_CH01_OBUF_WRPNT	32	ASRC_CH01_OBUF_WRPNT
11220B70	ASRC_CH01_OBUF_RDPNT	32	ASRC_CH01_OBUF_RDPNT
11220B80	ASRC_IBUF_INTR_CNT0	32	ASRC_IBUF_INTR_CNT0
11220B88	ASRC_OBUF_INTR_CNT0	32	ASRC_OBUF_INTR_CNT0
11220B90	ASRC_BAK_REG	32	ASRC_BAK_REG
11220B94	ASRC_FREQ_CALI_CTRL	32	ASRC_FREQ_CALI_CTRL
11220B98	ASRC_FREQ_CALI_CYC	32	ASRC_FREQ_CALI_CYC
11220B9C	ASRC_PRD_CALI_RESULT	32	ASRC_PRD_CALI_RESULT
11220BA0	ASRC_FREQ_CALI_RESULT	32	ASRC_FREQ_CALI_RESULT
11220BD8	ASRC_CALI_DENOMINATOR	32	ASRC_CALI_DENOMINATOR
11220BE0	ASRC_MAX_OUT_PER_IN0	32	ASRC_MAX_OUT_PER_IN0
11220BE8	ASRC_IN_BUF_MON0	32	ASRC_IN_BUF_MON0
11220BEC	ASRC_IN_BUF_MON1	32	ASRC_IN_BUF_MON1
11220BF0	ASRC_IIR_CRAM_ADDR	32	ASRC_IIR_CRAM_ADDR
11220BF4	ASRC_IIR_CRAM_DATA	32	ASRC_IIR_CRAM_DATA
11220BF8	ASRC_OUT_BUF_MON0	32	ASRC_OUT_BUF_MON0
11220BFC	ASRC_OUT_BUF_MON1	32	ASRC_OUT_BUF_MON1
11220C00	ASRC2_GEN_CONF	32	ASRC_GEN_CONF
11220C04	ASRC2_IER	32	ASRC_IER
11220C08	ASRC2_IFR	32	ASRC_IFR
11220C10	ASRC2_CH01_CNFG	32	ASRC_CH01_CNFG
11220C20	ASRC2_FREQUENCY_0	32	ASRC_FREQUENCY_0
11220C24	ASRC2_FREQUENCY_1	32	ASRC_FREQUENCY_1
11220C28	ASRC2_FREQUENCY_2	32	ASRC_FREQUENCY_2
11220C2C	ASRC2_FREQUENCY_3	32	ASRC_FREQUENCY_3
11220C30	ASRC2_IBUF_SADR	32	ASRC_IBUF_SADR
11220C34	ASRC2_IBUF_SIZE	32	ASRC_IBUF_SIZE
11220C38	ASRC2_OBUF_SADR	32	ASRC_OBUF_SADR
11220C3C	ASRC2_OBUF_SIZE	32	ASRC_OBUF_SIZE
11220C40	ASRC2_CH01_IBUF_RDPNT	32	ASRC_CH01_IBUF_RDPNT
11220C50	ASRC2_CH01_IBUF_WRPNT	32	ASRC_CH01_IBUF_WRPNT
11220C60	ASRC2_CH01_OBUF_WRPNT	32	ASRC_CH01_OBUF_WRPNT
11220C70	ASRC2_CH01_OBUF_RDPNT	32	ASRC_CH01_OBUF_RDPNT
11220C80	ASRC2_IBUF_INTR_CNT0	32	ASRC_IBUF_INTR_CNT0
11220C88	ASRC2_OBUF_INTR_CNT0	32	ASRC_OBUF_INTR_CNT0
11220C90	ASRC2_BAK_REG	32	ASRC_BAK_REG

Address	Name	Width	Register Function
11220C94	ASRC2_FREQ_CALI_CTRL	32	ASRC_FREQ_CALI_CTRL
11220C98	ASRC2_FREQ_CALI_CYC	32	ASRC_FREQ_CALI_CYC
11220C9C	ASRC2_PRD_CALI_RESULT	32	ASRC_PRD_CALI_RESULT
11220CA0	ASRC2_FREQ_CALI_RESULT	32	ASRC_FREQ_CALI_RESULT
11220CD8	ASRC2_CALI_DENOMINATOR	32	ASRC_CALI_DENOMINATOR
11220CE0	ASRC2_MAX_OUT_PER_IN0	32	ASRC_MAX_OUT_PER_IN0
11220CF0	ASRC2_IIR_CRAM_ADDR	32	ASRC_IIR_CRAM_ADDR
11220CF4	ASRC2_IIR_CRAM_DATA	32	ASRC_IIR_CRAM_DATA
11220CF8	ASRC2_OUT_BUF_MON0	32	ASRC_OUT_BUF_MON0
11220CFC	ASRC2_OUT_BUF_MON1	32	ASRC_OUT_BUF_MON1
11220D00	ASRC3_GEN_CONF	32	ASRC_GEN_CONF
11220D04	ASRC3_IER	32	ASRC_IER
11220D08	ASRC3_IFR	32	ASRC_IFR
11220D10	ASRC3_CH01_CNFG	32	ASRC_CH01_CNFG
11220D20	ASRC3_FREQUENCY_0	32	ASRC_FREQUENCY_0
11220D24	ASRC3_FREQUENCY_1	32	ASRC_FREQUENCY_1
11220D28	ASRC3_FREQUENCY_2	32	ASRC_FREQUENCY_2
11220D2C	ASRC3_FREQUENCY_3	32	ASRC_FREQUENCY_3
11220D30	ASRC3_IBUF_SADR	32	ASRC_IBUF_SADR
11220D34	ASRC3_IBUF_SIZE	32	ASRC_IBUF_SIZE
11220D38	ASRC3_OBUF_SADR	32	ASRC_OBUF_SADR
11220D3C	ASRC3_OBUF_SIZE	32	ASRC_OBUF_SIZE
11220D40	ASRC3_CH01_IBUF_RDPNT	32	ASRC_CH01_IBUF_RDPNT
11220D50	ASRC3_CH01_IBUF_WRPNT	32	ASRC_CH01_IBUF_WRPNT
11220D60	ASRC3_CH01_OBUF_WRPNT	32	ASRC_CH01_OBUF_WRPNT
11220D70	ASRC3_CH01_OBUF_RDPNT	32	ASRC_CH01_OBUF_RDPNT
11220D80	ASRC3_IBUF_INTR_CNT0	32	ASRC_IBUF_INTR_CNT0
11220D88	ASRC3_OBUF_INTR_CNT0	32	ASRC_OBUF_INTR_CNT0
11220D90	ASRC3_BAK_REG	32	ASRC_BAK_REG
11220D94	ASRC3_FREQ_CALI_CTRL	32	ASRC_FREQ_CALI_CTRL
11220D98	ASRC3_FREQ_CALI_CYC	32	ASRC_FREQ_CALI_CYC
11220D9C	ASRC3_PRD_CALI_RESULT	32	ASRC_PRD_CALI_RESULT
11220DA0	ASRC3_FREQ_CALI_RESULT	32	ASRC_FREQ_CALI_RESULT

Address	Name	Width	Register Function
11220DD8	ASRC3_CALI_DENOMINATOR	32	ASRC_CALI_DENOMINATOR
11220DE0	ASRC3_MAX_OUT_PER_IN0	32	ASRC_MAX_OUT_PER_IN0
11220DF0	ASRC3_IIR_CRAM_ADDR	32	ASRC_IIR_CRAM_ADDR
11220DF4	ASRC3_IIR_CRAM_DATA	32	ASRC_IIR_CRAM_DATA
11220DF8	ASRC3_OUT_BUF_MON0	32	ASRC_OUT_BUF_MON0
11220DFC	ASRC3_OUT_BUF_MON1	32	ASRC_OUT_BUF_MON1
11220E00	ASRC4_GEN_CONF	32	ASRC_GEN_CONF
11220E04	ASRC4_IER	32	ASRC_IER
11220E08	ASRC4_IFR	32	ASRC_IFR
11220E10	ASRC4_CH01_CNFG	32	ASRC_CH01_CNFG
11220E20	ASRC4_FREQUENCY_0	32	ASRC_FREQUENCY_0
11220E24	ASRC4_FREQUENCY_1	32	ASRC_FREQUENCY_1
11220E28	ASRC4_FREQUENCY_2	32	ASRC_FREQUENCY_2
11220E2C	ASRC4_FREQUENCY_3	32	ASRC_FREQUENCY_3
11220E30	ASRC4_IBUF_SADR	32	ASRC_IBUF_SADR
11220E34	ASRC4_IBUF_SIZE	32	ASRC_IBUF_SIZE
11220E38	ASRC4_OBUF_SADR	32	ASRC_OBUF_SADR
11220E3C	ASRC4_OBUF_SIZE	32	ASRC_OBUF_SIZE
11220E40	ASRC4_CH01_IBUF_RDPNT	32	ASRC_CH01_IBUF_RDPNT
11220E50	ASRC4_CH01_IBUF_WRPNT	32	ASRC_CH01_IBUF_WRPNT
11220E60	ASRC4_CH01_OBUF_WRPNT	32	ASRC_CH01_OBUF_WRPNT
11220E70	ASRC4_CH01_OBUF_RDPNT	32	ASRC_CH01_OBUF_RDPNT
11220E80	ASRC4_IBUF_INTR_CNT0	32	ASRC_IBUF_INTR_CNT0
11220E88	ASRC4_OBUF_INTR_CNT0	32	ASRC_OBUF_INTR_CNT0
11220E90	ASRC4_BAK_REG	32	ASRC_BAK_REG
11220E94	ASRC4_FREQ_CALI_CTRL	32	ASRC_FREQ_CALI_CTRL
11220E98	ASRC4_FREQ_CALI_CYC	32	ASRC_FREQ_CALI_CYC
11220E9C	ASRC4_PRD_CALI_RESULT	32	ASRC_PRD_CALI_RESULT
11220EA0	ASRC4_FREQ_CALI_RESULT	32	ASRC_FREQ_CALI_RESULT
11220ED8	ASRC4_CALI_DENOMINATOR	32	ASRC_CALI_DENOMINATOR
11220EE0	ASRC4_MAX_OUT_PER_IN0	32	ASRC_MAX_OUT_PER_IN0
11220EF0	ASRC4_IIR_CRAM_ADDR	32	ASRC_IIR_CRAM_ADDR
11220EF4	ASRC4_IIR_CRAM_DATA	32	ASRC_IIR_CRAM_DATA

Address	Name	Width	Register Function
11220EF8	ASRC4_OUT_BUF_MON0	32	ASRC_OUT_BUF_MON0
11220EFC	ASRC4_OUT_BUF_MON1	32	ASRC_OUT_BUF_MON1
11220F00	ASRC5_GEN_CONF	32	ASRC_GEN_CONF
11220F04	ASRC5_IER	32	ASRC_IER
11220F08	ASRC5_IFR	32	ASRC_IFR
11220F10	ASRC5_CH01_CNFG	32	ASRC_CH01_CNFG
11220F20	ASRC5_FREQUENCY_0	32	ASRC_FREQUENCY_0
11220F24	ASRC5_FREQUENCY_1	32	ASRC_FREQUENCY_1
11220F28	ASRC5_FREQUENCY_2	32	ASRC_FREQUENCY_2
11220F2C	ASRC5_FREQUENCY_3	32	ASRC_FREQUENCY_3
11220F30	ASRC5_IBUF_SADR	32	ASRC_IBUF_SADR
11220F34	ASRC5_IBUF_SIZE	32	ASRC_IBUF_SIZE
11220F38	ASRC5_OBUF_SADR	32	ASRC_OBUF_SADR
11220F3C	ASRC5_OBUF_SIZE	32	ASRC_OBUF_SIZE
11220F40	ASRC5_CH01_IBUF_RDPNT	32	ASRC_CH01_IBUF_RDPNT
11220F50	ASRC5_CH01_IBUF_WRPNT	32	ASRC_CH01_IBUF_WRPNT
11220F60	ASRC5_CH01_OBUF_WRPNT	32	ASRC_CH01_OBUF_WRPNT
11220F70	ASRC5_CH01_OBUF_RDPNT	32	ASRC_CH01_OBUF_RDPNT
11220F80	ASRC5_IBUF_INTR_CNT0	32	ASRC_IBUF_INTR_CNT0
11220F88	ASRC5_OBUF_INTR_CNT0	32	ASRC_OBUF_INTR_CNT0
11220F90	ASRC5_BAK_REG	32	ASRC_BAK_REG
11220F94	ASRC5_FREQ_CALI_CTRL	32	ASRC_FREQ_CALI_CTRL
11220F98	ASRC5_FREQ_CALI_CYC	32	ASRC_FREQ_CALI_CYC
11220F9C	ASRC5_PRD_CALI_RESULT	32	ASRC_PRD_CALI_RESULT
11220FA0	ASRC5_FREQ_CALI_RESULT	32	ASRC_FREQ_CALI_RESULT
11220FD8	ASRC5_CALI_DENOMINATOR	32	ASRC_CALI_DENOMINATOR
11220FE0	ASRC5_MAX_OUT_PER_IN0	32	ASRC_MAX_OUT_PER_IN0
11220FF0	ASRC5_IIR_CRAM_ADDR	32	ASRC_IIR_CRAM_ADDR
11220FF4	ASRC5_IIR_CRAM_DATA	32	ASRC_IIR_CRAM_DATA
11220FF8	ASRC5_OUT_BUF_MON0	32	ASRC_OUT_BUF_MON0
11220FFC	ASRC5_OUT_BUF_MON1	32	ASRC_OUT_BUF_MON1
112211C0	DSD_ENC_CON0	32	DSD ENC Control Register 0
112211C4	DSD_ENC_CON1	32	DSD ENC Control Register 1
112211C8	DSD_ENC_CON2	32	DSD ENC Control Register 2
112211D0	DSD_ENC_STATUS	32	DSD ENC STATUS

Address	Name	Width	Register Function
112211D4	DSD_UPDATE_POS	32	AFE Control Register 0
11221200	AFE_DAC_CON0	32	AFE Control Register 0
11221204	AFE_DAC_CON1	32	AFE Control Register 1
11221208	AFE_DAC_CON2	32	AFE Control Register 2
1122120C	AFE_DAC_CON3	32	AFE Control Register 3
11221210	AFE_DAC_CON4	32	AFE Control Register 4
11221214	AFE_DAC_CON5	32	AFE Control Register 5
11221218	AFE_DAC_MON0	32	AFE Control Monitor 0
11221220	AFE_MEMIF_MINLEN0	32	AFE Memif Min BLength Register 0
11221224	AFE_MEMIF_MINLEN1	32	AFE Memif Min BLength Register 1
11221228	AFE_MEMIF_MINLEN2	32	AFE Memif Min BLength Register 2
1122122C	AFE_MEMIF_MAXLEN0	32	AFE Memif Max BLength Register 0
11221230	AFE_MEMIF_MAXLEN1	32	AFE Memif Max BLength Register 1
11221234	AFE_MEMIF_MAXLEN2	32	AFE Memif Max BLength Register 2
11221238	AFE_MEMIF_PBUF_SIZE	32	AFE Memif prefecth buffer size
1122123C	AFE_MEMIF_HD_CON0	32	AFE Memif HD Audio Control Register 0
1122121C	AFE_MEMIF_HD_CON1	32	AFE Memif HD Audio Control Register 1
11221240	AFE_DL1_BASE	32	AFE DL1 Base Address Register
11221244	AFE_DL1_CUR	32	AFE DL1 Cursor Register
11221248	AFE_DL1_END	32	AFE DL1 End Address Register
11221250	AFE_DL2_BASE	32	AFE DL2 Base Address Register
11221254	AFE_DL2_CUR	32	AFE DL2 Cursor Register
11221258	AFE_DL2_END	32	AFE DL2 End Address Register
11221260	AFE_DL3_BASE	32	AFE DL3 Base Address Register
11221264	AFE_DL3_CUR	32	AFE DL3 Cursor Register
11221268	AFE_DL3_END	32	AFE DL3 End Address Register
11221270	AFE_DL4_BASE	32	AFE DL4 Base Address Register
11221274	AFE_DL4_CUR	32	AFE DL4 Cursor Register
11221278	AFE_DL4_END	32	AFE DL4 End Address Register
11221280	AFE_DL5_BASE	32	AFE DL5 Base Address Register
11221284	AFE_DL5_CUR	32	AFE DL5 Cursor Register
11221288	AFE_DL5_END	32	AFE DL5 End Address Register
11221290	AFE_DL6_BASE	32	AFE DL6 Base Address Register
11221294	AFE_DL6_CUR	32	AFE DL6 Cursor Register
11221298	AFE_DL6_END	32	AFE DL6 End Address Register
112212A0	AFE_DLMCH_BASE	32	AFE DLMCH Base Address Register
112212A4	AFE_DLMCH_CUR	32	AFE DLMCH Cursor Register
112212A8	AFE_DLMCH_END	32	AFE DLMCH End Address Register
112212B0	AFE_ARB1_BASE	32	AFE ARB1 Base Address Register
112212B4	AFE_ARB1_CUR	32	AFE ARB1 Cursor Register
112212B8	AFE_ARB1_END	32	AFE ARB1 End Address Register
112212C0	AFE_DSDR_BASE	32	AFE DSDR Base Address Register
112212C4	AFE_DSDR_CUR	32	AFE DSDR Cursor Register
112212C8	AFE_DSDR_END	32	AFE DSDR End Address Register

Address	Name	Width	Register Function
112212D0	AFE_AWB_BASE	32	AFE AWB Base Address Register
112212D8	AFE_AWB_END	32	AFE AWB End Address Register
112212DC	AFE_AWB_CUR	32	AFE AWB Cursor Register
112212E0	AFE_AWB2_BASE	32	AFE AWB2 Base Address Register
112212E8	AFE_AWB2_END	32	AFE AWB2 End Address Register
112212EC	AFE_AWB2_CUR	32	AFE AWB2 Cursor Register
112212F0	AFE_DSDW_BASE	32	AFE DSDW Base Address Register
112212F8	AFE_DSDW_END	32	AFE DSDW End Address Register
112212FC	AFE_DSDW_CUR	32	AFE DSDW Cursor Register
11221300	AFE_VUL_BASE	32	AFE VUL Base Address Register
11221308	AFE_VUL_END	32	AFE VUL End Address Register
1122130C	AFE_VUL_CUR	32	AFE VUL Cursor Register
11221310	AFE_UL2_BASE	32	AFE UL2 Base Address Register
11221318	AFE_UL2_END	32	AFE UL2 End Address Register
1122131C	AFE_UL2_CUR	32	AFE UL2 Cursor Register
11221320	AFE_UL3_BASE	32	AFE UL3 Base Address Register
11221328	AFE_UL3_END	32	AFE UL3 End Address Register
1122132C	AFE_UL3_CUR	32	AFE UL3 Cursor Register
11221330	AFE_UL4_BASE	32	AFE UL4 Base Address Register
11221338	AFE_UL4_END	32	AFE UL4 End Address Register
1122133C	AFE_UL4_CUR	32	AFE UL4 Cursor Register
11221340	AFE_UL5_BASE	32	AFE UL5 Base Address Register
11221348	AFE_UL5_END	32	AFE UL5 End Address Register
1122134C	AFE_UL5_CUR	32	AFE UL5 Cursor Register
11221350	AFE_UL6_BASE	32	AFE UL6 Base Address Register
11221358	AFE_UL6_END	32	AFE UL6 End Address Register
1122135C	AFE_UL6_CUR	32	AFE UL6 Cursor Register
11221360	AFE_ULMCH_BASE	32	AFE ULMCH Base Address Register
11221368	AFE_ULMCH_END	32	AFE ULMCH End Address Register
1122136C	AFE_ULMCH_CUR	32	AFE ULMCH Cursor Register
11221370	AFE_DAI_BASE	32	AFE DAI Base Address Register
11221378	AFE_DAI_END	32	AFE_DAI_END
1122137C	AFE_DAI_CUR	32	AFE DAI Cursor Register
11221380	AFE_MOD_DAI_BASE	32	AFE MOD_DAI Base Address Register
11221388	AFE_MOD_DAI_END	32	AFE_MOD_DAI_END
1122138C	AFE_MOD_DAI_CUR	32	AFE MOD_DAI Cursor Register
112213A0	AFE_DMA_BASE	32	AFE DMA Base Address Register
112213A4	AFE_DMA_CUR	32	AFE DMA Read Cursor Register
112213A8	AFE_DMA_END	32	AFE_DMA_END
112213AC	AFE_DMA_WR_CUR	32	AFE DMA Write Cursor Register
112213B0	AFE_DMA_CON0	32	AFE DMA Control Register 0
112213B4	AFE_DMA_THRESHOLD	32	AFE DMA Threshold amount for downlink output
112213B8	AFE_DMA_INTR_SIZE	32	AFE DMA Interrupt size for DMA
112213BC	AFE_DMA_NEXT_INTR	32	AFE_DMA Next Interrupt Size for DMA
112213C0	AFE_DMA_NEXT_BASE	32	AFE DMA Next Base Address Register

Address	Name	Width	Register Function
112213C8	AFE_DMA_NEXT_END	32	AFE_DMA_NEXT_END
112213D0	AFE_TDM_IN_BASE	32	AFE TDM IN Base Address Register
112213D4	AFE_TDM_IN_CUR	32	AFE TDM IN Cursor Register
112213D8	AFE_TDM_IN_END	32	AFE TDM IN End Address Register
11221400	AFE_AWB_CHK_SUM1	32	AFE_AWB_CHK_SUM1
11221404	AFE_AWB_CHK_SUM2	32	AFE_AWB_CHK_SUM2
11221418	AFE_AWB2_CHK_SUM1	32	AFE_AWB2_CHK_SUM1
1122141C	AFE_AWB2_CHK_SUM2	32	AFE_AWB2_CHK_SUM2
11221430	AFE_DSDW_CHK_SUM1	32	AFE_DSDW_CHK_SUM1
11221434	AFE_DSDW_CHK_SUM2	32	AFE_DSDW_CHK_SUM2
11221450	AFE_VUL_CHK_SUM1	32	AFE_VUL_CHK_SUM1
11221454	AFE_VUL_CHK_SUM2	32	AFE_VUL_CHK_SUM2
11221458	AFE_UL2_CHK_SUM1	32	AFE_UL2_CHK_SUM1
1122145C	AFE_UL2_CHK_SUM2	32	AFE_UL2_CHK_SUM2
11221460	AFE_UL3_CHK_SUM1	32	AFE_UL3_CHK_SUM1
11221464	AFE_UL3_CHK_SUM2	32	AFE_UL3_CHK_SUM2
11221468	AFE_UL4_CHK_SUM1	32	AFE_UL4_CHK_SUM1
1122146C	AFE_UL4_CHK_SUM2	32	AFE_UL4_CHK_SUM2
11221470	AFE_UL5_CHK_SUM1	32	AFE_UL5_CHK_SUM1
11221474	AFE_UL5_CHK_SUM2	32	AFE_UL5_CHK_SUM2
11221478	AFE_UL6_CHK_SUM1	32	AFE_UL6_CHK_SUM1
1122147C	AFE_UL6_CHK_SUM2	32	AFE_UL6_CHK_SUM2
11221480	AFE_ULM_CHK_SUM1	32	AFE_ULM_CHK_SUM1
11221484	AFE_ULM_CHK_SUM2	32	AFE_ULM_CHK_SUM2
11221490	AFE_DL1_CHK_SUM1	32	AFE_DL1_CHK_SUM1
11221494	AFE_DL1_CHK_SUM2	32	AFE_DL1_CHK_SUM2
11221498	AFE_DL1_CHK_SUM3	32	AFE_DL1_CHK_SUM3
1122149C	AFE_DL1_CHK_SUM4	32	AFE_DL1_CHK_SUM4
112214A0	AFE_DL2_CHK_SUM1	32	AFE_DL2_CHK_SUM1
112214A4	AFE_DL2_CHK_SUM2	32	AFE_DL2_CHK_SUM2
112214B0	AFE_DL3_CHK_SUM1	32	AFE_DL3_CHK_SUM1
112214B4	AFE_DL3_CHK_SUM2	32	AFE_DL3_CHK_SUM2
112214C0	AFE_DL4_CHK_SUM1	32	AFE_DL4_CHK_SUM1
112214C4	AFE_DL4_CHK_SUM2	32	AFE_DL4_CHK_SUM2
112214D0	AFE_DL5_CHK_SUM1	32	AFE_DL5_CHK_SUM1
112214D4	AFE_DL5_CHK_SUM2	32	AFE_DL5_CHK_SUM2
112214E0	AFE_DL6_CHK_SUM1	32	AFE_DL6_CHK_SUM1
112214E4	AFE_DL6_CHK_SUM2	32	AFE_DL6_CHK_SUM2
112214F0	AFE_ARB1_CHK_SUM1	32	AFE_ARB1_CHK_SUM1
112214F4	AFE_ARB1_CHK_SUM2	32	AFE_ARB1_CHK_SUM2
11221500	AFE_DSDR_CHK_SUM1	32	AFE_DSDR_CHK_SUM1
11221504	AFE_DSDR_CHK_SUM2	32	AFE_DSDR_CHK_SUM2
11221510	AFE_DLMCH_CHK_SUM1	32	AFE_DLMCH_CHK_SUM1

Address	Name	Width	Register Function
11221514	AFE_DLMCH_CHK_SUM2	32	AFE_DLMCH_CHK_SUM2
11221518	AFE_DLMCH_CHK_SUM3	32	AFE_DLMCH_CHK_SUM3
1122151C	AFE_DLMCH_CHK_SUM4	32	AFE_DLMCH_CHK_SUM4
11221520	AFE_TDM_OUT_CHK_SUM1	32	AFE_TDM_CHK_SUM1
11221524	AFE_TDM_OUT_CHK_SUM2	32	AFE_TDM_CHK_SUM2
11221528	AFE_TDM_OUT_CHK_SUM3	32	AFE_TDM_CHK_SUM3
1122152C	AFE_TDM_OUT_CHK_SUM4	32	AFE_TDM_CHK_SUM4
11221530	AFE_SPDIF_CHK_SUM1	32	AFE_SPDIF_CHK_SUM1
11221538	AFE_SPDIF2_CHK_SUM1	32	AFE_SPDIF2_CHK_SUM1
11221544	AFE_DL_COUNTER_CON	32	AFE_DL_COUNTER_CON
11221550	AFE_TDM_IN_CHK_SUM1	32	AFE_TDM_IN_CHK_SUM1
11221554	AFE_TDM_IN_CHK_SUM2	32	AFE_TDM_IN_CHK_SUM2
11221558	AFE_TDM_IN_CHK_SUM3	32	AFE_TDM_IN_CHK_SUM3
1122155C	AFE_TDM_IN_CHK_SUM4	32	AFE_TDM_IN_CHK_SUM4
11221560	AFE_TDM_IN_CHK_SUM5	32	AFE_TDM_IN_CHK_SUM5
11221564	AFE_TDM_IN_CHK_SUM6	32	AFE_TDM_IN_CHK_SUM6
11221568	AFE_DL1_RD_COUNTER	32	AFE_DL1_RD_COUNTER
1122156C	AFE_DL2_RD_COUNTER	32	AFE_DL2_RD_COUNTER
11221570	AFE_DL3_RD_COUNTER	32	AFE_DL3_RD_COUNTER
11221574	AFE_DL4_RD_COUNTER	32	AFE_DL4_RD_COUNTER
11221578	AFE_DL5_RD_COUNTER	32	AFE_DL5_RD_COUNTER
1122157C	AFE_DL6_RD_COUNTER	32	AFE_DL6_RD_COUNTER
112215D0	AFE_MEMIF_MON0	32	AFE Memory Interface Monitor Register 0
112215D4	AFE_MEMIF_MON1	32	AFE Memory Interface Monitor Register 1
112215D8	AFE_MEMIF_MON2	32	AFE Memory Interface Monitor Register 2
112215DC	AFE_MEMIF_MON3	32	AFE Memory Interface Monitor Register 3
112215E0	AFE_MEMIF_MON4	32	AFE Memory Interface Monitor Register 4
11220054	AFE_TDM_CON1	32	TDM Config 1
11220058	AFE_TDM_CON2	32	
1122005C	AFE_SINEGNE_CON_TDM	32	
11220074	AFE_SINEGNE_CON_TDM_IN	32	
11220078	TDMOUT_CLKDIV_CFG	32	TDM OUT CLK DVI Control Register
11220060	AFE_TDM_IN_CON1	32	AFE TDM IN Control Register 0
11220064	AFE_TDM_IN_CON2	32	AFE TDM IN Control Register 1

Address	Name	Width	Register Function
11220068	AFE_TDM_IN_MON1	32	AFE TDM IN MON Register 0
1122006C	AFE_TDM_IN_MON2	32	AFE TDM IN MON Register 1
11220070	AFE_TDM_IN_MON3	32	AFE TDM IN MON Register 2
1122007C	TDMIN_CLKDIV_CFG	32	TDM IN CLK DVI Control Register
11221700	AFE_IRQ_ACC1_CNT	32	AFE IRQ ACC1 Counter Register
11221704	AFE_IRQ_ACC2_CNT	32	AFE IRQ ACC2 Counter Register
11221708	AFE_IRQ_ACC1_CNT_MON1	32	AFE IRQ ACC1 Counter MON1 Register
1122170C	AFE_IRQ_ACC1_CNT_MON2	32	AFE IRQ ACC1 Counter MON2 Register
11221710	AFE_TSF_CON	32	WiFi TSF control registers
11221714	AFE_TSF_MON	32	WiFi TSF read out registers
11221718	AFE_IRQ_ACC2_CNT_MON	32	AFE IRQ ACC2 Counter MON Register
1122171C	AFE_IRQ_MCU_CNT11	32	AFE IRQ11 MCU Counter Register
11221720	AFE_IRQ_MCU_CNT12	32	AFE IRQ12 MCU Counter Register
11221724	AFE_IRQ11_MCU_CNT_MON	32	AFE IRQ11 MCU Count Monitor Register
11221728	AFE_IRQ12_MCU_CNT_MON	32	AFE IRQ12 MCU Count Monitor Register
1122172C	AFE_I2S_UL1_REORDER	8	AFE I2S UL1 REORDER

11220000 AUDIO_TOP_CON0 Audio Top Control Register 0 80794038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		ahb_idle_en	ahb_idle_en_ext		pdn_tml			pdn_apll2_ck	pdn_apll_ck	pdn_spdf2_ck	pdn_spdf_ck	pdn_hdmi_ck				
Type		RW	RW		RW			RW	RW	RW	RW	RW				
Reset		0	0		0			0	0	1	1	1				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		APB3_SEL	APB_R2T	APB_W2T								PDN_LRCK_CNT		PDN_AFE		
Type		RW	RW	RW								RW		RW		
Reset		1	0	0								1		0		

Bit(s)	Mnemonic	Name	Description
30		ahb_idle_en	**Enable AHB idle for internal bus clock** 0: Disable 1: Enable
29		ahb_idle_en_ext	**Enable AHB idle for external bus clock** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
27		pdn_tml	**Powers (test model) clock** 0: Does not Power down 1: Power down
24		pdn_apll2_ck	**Powers down apll2_ck clock** 0: Does not Power down 1: Power down
23		pdn_apll_ck	**Powers down apll_ck clock** 0: Does not Power down 1: Power down
22		pdn_spdf2_ck	**Power down spdf2 clock** 0: Does not Power down 1: Power down
21		pdn_spdf_ck	**Power down spdf clock** 0: Does not Power down 1: Power down
20		pdn_hdmi_ck	**Power down hdmi clock** 0: Does not Power down 1: Power down
14		APB3_SEL	**Uses APB 3.0 protocol** 0: Does not use APB 3p0 1: Use APB 3p0
13		APB_R2T	**Read cycle for APB write** 0: 1T 1: 2T
12		APB_W2T	**Read cycle for APB read** 0: 1T 1: 2T

Bit(s)	Mnemonic	Name	Description
4		PDN_LRCK_CNT	
2		PDN_AFE	**Power down AFE clock** 0: Does not Power down 1: Power down

11220004 AUDIO_TOP_CON1 Audio Top Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11220008 AUDIO_TOP_CON2 Audio Top Control Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved_31_24								spdf2_ck_div							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved_15_8								spdf_ck_div							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		Reserved_31_24	**Reserved**
23:16		spdf2_ck_div	**Divider setting of spdf2_ck, n = [7:0]** spdf2_ck = clock source * (1 / n+1)
15:8		Reserved_15_8	**Reserved**

Bit(s)	Mnemonic	Name	Description
7:0		spdf_ck_div	**Divider setting of spdf_ck, n = [7:0]** spdf_ck = clock source * (1 / n+1)

1122000C AUDIO_TOP_CON3 Audio Top Control Register 3 60000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUSY	OS_DISABLE	CG_DISABLE			i2s6_in_ck_align	i2s5_in_ck_align	i2s4_in_ck_align	i2s3_in_ck_align	i2s2_in_ck_align					spdif_out_sel	
Type	RW	RW	RW			RW	RW	RW	RW	RW					RW	
Reset	0	1	1			0	0	0	0	0					0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			hdmi_bck_div						speaker_out_hdmi_sel		speaker_out_hdmi	hdmi_out_speaker				CLEAR_FLAG
Type			RW						RW		RW	RW				RW
Reset			0	0	0	0	0	0	0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
31		BUSY	**Reserved**
30		OS_DISABLE	**Reserved**
29		CG_DISABLE	**Reserved**
26		i2s6_in_ck_align	**i2s6 in_ck, in_ws align to i2s1** 1 : i2s6 in_ck, in_ws align to i2s1
25		i2s5_in_ck_align	**i2s5 in_ck, in_ws align to i2s1** 1 : i2s5 in_ck, in_ws align to i2s1
24		i2s4_in_ck_align	**i2s4 in_ck, in_ws align to i2s1** 1 : i2s4 in_ck, in_ws align to i2s1
23		i2s3_in_ck_align	**i2s3 in_ck, in_ws align to i2s1** 1 : i2s3 in_ck, in_ws align to i2s1
22		i2s2_in_ck_align	**i2s2 in_ck, in_ws align to i2s1** 1 : i2s2 in_ck, in_ws align to i2s1

Bit(s)	Mnemonic	Name	Description
17:16		spdif_out_sel	**SPDIF output selection** [0]: 0: SPDIF for HDMI, 1: SPDIF2 for HDMI [1]: 0: SPDIF2 for PAD, 1: SPDIF for PAD
13:8		hdmi_bck_div	**Divider setting of hdmi_bck, n = [5:0]** hdmi_bck = clock source / (2 * (n+1))
7:6		speaker_out_hdmi_sel	**Decide the HDMI 2ch should be which sdata.** 2'b00: hdmi_sdata0 2'b01: hdmi_sdata1 2'b10: hdmi_sdata2 2'b11: hdmi_sdata3
5		speaker_out_hdmi	**Control if the speaker should output HDMI 2ch content.** 0: speaker clock and sdata will be oringinal one. 1: speaker clock and sdata will the 2ch HDMI output.
4		hdmi_out_speaker	**Control if the HDMI should output speaker content.** 0: HDMI clock and sdata0 will be oringinal one. 1: HDMI clock and sdata0 will the DAC_I2S output.
0		CLEAR_FLAG	**Clears slave bus decoding error flag**

11220010 AUDIO_TOP_CON4 Audio Top Control Register 4 0FFBFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					pdn_mp3_ultra_low	pdn_mp3_low	pdn_mrgif	pdn_pcmif	pdn_afe_conn	pdn_a2sys	pdn_a1sys	pdn_intdir	pdn_multi_in		pdn_asrc12	pdn_asrc11
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset					1	1	1	1	1	1	1	1	1		1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_asrco2	pdn_asrco1	pdn_asrci2	pdn_asrci1			pdn_i2so4	pdn_i2so3	pdn_i2so2	pdn_i2so1			pdn_i2sin4	pdn_i2sin3	pdn_i2sin2	pdn_i2sin1
Type	RW	RW	RW	RW			RW	RW	RW	RW			RW	RW	RW	RW
Reset	1	1	1	1			1	1	1	1			1	1	1	1

Bit(s)	Mnemonic	Name	Description
27		pdn_mp3_ultra_low	**Power down merge interface** 0: Normal 1: Power down
26		pdn_mp3_low	**Power down pcm interface** 0: Normal 1: Power down
25		pdn_mrgif	**Power down merge interface** 0: Normal 1: Power down
24		pdn_pcmif	**Power down pcm interface** 0: Normal 1: Power down
23		pdn_afe_conn	**Power down afe connector** 0: Normal 1: Power down
22		pdn_a2sys	**Power down a1sys clk (48k domain)** 0: Normal 1: Power down
21		pdn_a1sys	**Power down a2sys clk (44.1k domain)** 0: Normal 1: Power down
20		pdn_intdir	**Power down int dir clock** 0: Normal 1: Power down
19		pdn_multi_in	**Power down multi in clk** 0: Normal 1: Power down

Bit(s)	Mnemonic	Name	Description
17		pdn_asrc12	**Power down pcm in asrc clk** 0: Normal 1: Power down
16		pdn_asrc11	**Power down pcm out asrc clk** 0: Normal 1: Power down
15		pdn_asrc02	**Power down i2s out 2 asrc clk** 0: Normal 1: Power down
14		pdn_asrc01	**Power down i2s out 1 asrc clk** 0: Normal 1: Power down
13		pdn_asrci2	**Power down i2s in 2 asrc clk** 0: Normal 1: Power down
12		pdn_asrci1	**Power down i2s in 1 asrc clk** 0: Normal 1: Power down
9		pdn_i2so4	**Power down i2s out 4 clk** 0: Normal 1: Power down
8		pdn_i2so3	**Power down i2s out 3 clk** 0: Normal 1: Power down
7		pdn_i2so2	**Power down i2s out 2 clk** 0: Normal 1: Power down
6		pdn_i2so1	**Power down i2s out 1 clk**

Bit(s)	Mnemonic	Name	Description
			0: Normal
			1: Power down
3		pdn_i2sin4	**Power down i2s in 4 clk**
			0: Normal
			1: Power down
2		pdn_i2sin3	**Power down i2s in 3 clk**
			0: Normal
			1: Power down
1		pdn_i2sin2	**Power down i2s in 2 clk**
			0: Normal
			1: Power down
0		pdn_i2sin1	**Power down i2s in 1 clk**
			0: Normal
			1: Power down

11220014 AUDIO_TOP_CON5 Audio Top Control Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															pdn_memif_mod	pdn_memif_dai
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_memif_awb2	pdn_memif_awb	pdn_memif_arb1	pdn_memif_dlmch	pdn_memif_dl6	pdn_memif_dl5	pdn_memif_dl4	pdn_memif_dl3	pdn_memif_dl2	pdn_memif_dl1	pdn_memif_ul6	pdn_memif_ul5	pdn_memif_ul4	pdn_memif_ul3	pdn_memif_ul2	pdn_memif_ul1
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17		pdn_memif_mod	**Power down bt in channel memory agent**

Bit(s)	Mnemonic	Name	Description
			0: Normal
			1: Power down
16		pdn_memif_dai	**Power down pcminterface in memory agent**
			0: Normal
			1: Power down
15		pdn_memif_awb2	**Power down audio write back2 memory agent**
			0: Normal
			1: Power down
14		pdn_memif_awb	**Power down audio write back memory agent**
			0: Normal
			1: Power down
13		pdn_memif_arb1	**Power down audio read back memory agent**
			0: Normal
			1: Power down
12		pdn_memif_dlmch	**Power down downlink multi channel memory agent**
			0: Normal
			1: Power down
11		pdn_memif_dl6	**Power down downlink 6 memory agent**
			0: Normal
			1: Power down
10		pdn_memif_dl5	**Power down downlink 5 memory agent**
			0: Normal
			1: Power down
9		pdn_memif_dl4	**Power down downlink 4 memory agent**
			0: Normal
			1: Power down
8		pdn_memif_dl3	**Power down downlink 3 memory agent**

Bit(s)	Mnemonic	Name	Description
			0: Normal
			1: Power down
7		pdn_memif_dl2	**Power down downlink 2 memory agent**
			0: Normal
			1: Power down
6		pdn_memif_dl1	**Power down downlink 1 memory agent**
			0: Normal
			1: Power down
5		pdn_memif_ul6	**Power down up link 6 memory agent**
			0: Normal
			1: Power down
4		pdn_memif_ul5	**Power down up link 5 memory agent**
			0: Normal
			1: Power down
3		pdn_memif_ul4	**Power down up link 4 memory agent**
			0: Normal
			1: Power down
2		pdn_memif_ul3	**Power down up link 3 memory agent**
			0: Normal
			1: Power down
1		pdn_memif_ul2	**Power down up link 2 memory agent**
			0: Normal
			1: Power down
0		pdn_memif_ul1	**Power down up link 1 memory agent**
			0: Normal
			1: Power down

11220400 AUDIO_TOP_STA0 Audio Top Status 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11220404 AUDIO_TOP_STA1 Audio Top Status 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1122001C AFE_DAIBT_CON0 AFE DAI/BT CONTROL REGISTER0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11220100 ASMI_TIMING_CON1 ASM_IN_TIMING_SEL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			asmi6_mode					asmi5_mode					asmi4_mode			
Type			RW					RW					RW			
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asmi4_mode	asmi3_mode					asmi2_mode					asmi1_mode				
Type	RW	RW					RW					RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:25		asmi6_mode	**control for i2sin6 sample base asrc output en selection** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2sin1_1x_en 5'b01010: ext_i2sin2_1x_en 5'b01011: ext_i2sin3_1x_en 5'b01100: ext_i2sin4_1x_en 5'b01101: ext_i2sin5_1x_en 5'b01110: ext_i2sin6_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k

Bit(s)	Mnemonic	Name	Description
			5'b10011: 22.05k
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4kk
			5'b11000: 352.8k
24:20		asmi5_mode	**control for i2sin5 sample base asrc output en selection** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2sin1_1x_en 5'b01010: ext_i2sin2_1x_en 5'b01011: ext_i2sin3_1x_en 5'b01100: ext_i2sin4_1x_en 5'b01101: ext_i2sin5_1x_en 5'b01110: ext_i2sin6_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k

Bit(s)	Mnemonic	Name	Description
			5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
19:15		asmi4_mode	**control for i2sin4 sample base asrc output en selection** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2sin1_1x_en 5'b01010: ext_i2sin2_1x_en 5'b01011: ext_i2sin3_1x_en 5'b01100: ext_i2sin4_1x_en 5'b01101: ext_i2sin5_1x_en 5'b01110: ext_i2sin6_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k

Bit(s)	Mnemonic	Name	Description
			5'b10111: 176.4kk
			5'b11000: 352.8k
14:10		asmi3_mode	**control for i2sin3 sample base asrc output en selection**
			5'b00000: 8k
			5'b00001: 12k
			5'b00010: 16k
			5'b00011: 24k
			5'b00100: 32k
			5'b00101: 48k
			5'b00110: 96k
			5'b00111: 192kk
			5'b01000: 384k
			5'b01001: ext_i2sin1_1x_en
			5'b01010: ext_i2sin2_1x_en
			5'b01011: ext_i2sin3_1x_en
			5'b01100: ext_i2sin4_1x_en
			5'b01101: ext_i2sin5_1x_en
			5'b01110: ext_i2sin6_1x_en
			5'b10000: 7.35k
			5'b10001: 11.025k
			5'b10010: 14.7k
			5'b10011: 22.05k
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4kk
			5'b11000: 352.8k

Bit(s)	Mnemonic	Name	Description
9:5		asmi2_mode	**control for i2sin2 sample base asrc output en selection** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2sin1_1x_en 5'b01010: ext_i2sin2_1x_en 5'b01011: ext_i2sin3_1x_en 5'b01100: ext_i2sin4_1x_en 5'b01101: ext_i2sin5_1x_en 5'b01110: ext_i2sin6_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
4:0		asmi1_mode	**control for i2sin1 sample base asrc output en selection** 5'b00000: 8k

Bit(s)	Mnemonic	Name	Description
			5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2s01_1x_en 5'b01010: 5'bext_i2s02_1x_en 5'b01011: ext_i2s03_1x_en 5'b01100: ext_i2s04_1x_en 5'b01101: ext_i2s05_1x_en 5'b01110: ext_i2s06_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k

11220104 ASMO_TIMING_CON1 ASM_OUT_TIMING_SEL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			asmo6_mode					asmo5_mode					asmo4_mode			
Type			RW					RW					RW			

Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asmo4_mode	asmi3_mode					asmi2_mode					asmi1_mode				
Type	RW	RW					RW					RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:25		asmo6_mode	**control for i2sout6 sample base asrc input en selection** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2so1_1x_en 5'b01010: 5'bext_i2so2_1x_en 5'b01011: ext_i2so3_1x_en 5'b01100: ext_i2so4_1x_en 5'b01101: ext_i2so5_1x_en 5'b01110: ext_i2so6_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k

Bit(s)	Mnemonic	Name	Description
			5'b10110: 88.2k
			5'b10111: 176.4kk
			5'b11000: 352.8k
24:20		asmo5_mode	**control for i2sout5 sample base asrc input en selection**
			5'b00000: 8k
			5'b00001: 12k
			5'b00010: 16k
			5'b00011: 24k
			5'b00100: 32k
			5'b00101: 48k
			5'b00110: 96k
			5'b00111: 192kk
			5'b01000: 384k
			5'b01001: ext_i2so1_1x_en
			5'b01010: 5'bext_i2so2_1x_en
			5'b01011: ext_i2so3_1x_en
			5'b01100: ext_i2so4_1x_en
			5'b01101: ext_i2so5_1x_en
			5'b01110: ext_i2so6_1x_en
			5'b10000: 7.35k
			5'b10001: 11.025k
			5'b10010: 14.7k
			5'b10011: 22.05k
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4kk

Bit(s)	Mnemonic	Name	Description
			5'b11000: 352.8k
19:15		asmo4_mode	**control for i2sout4 sample base asrc input en selection** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2so1_1x_en 5'b01010: 5'bext_i2so2_1x_en 5'b01011: ext_i2so3_1x_en 5'b01100: ext_i2so4_1x_en 5'b01101: ext_i2so5_1x_en 5'b01110: ext_i2so6_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
14:10		asmi3_mode	**control for i2sout3 sample base asrc input en selection**

Bit(s)	Mnemonic	Name	Description
			5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2so1_1x_en 5'b01010: 5'bext_i2so2_1x_en 5'b01011: ext_i2so3_1x_en 5'b01100: ext_i2so4_1x_en 5'b01101: ext_i2so5_1x_en 5'b01110: ext_i2so6_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
9:5		asmi2_mode	**control for i2sout2 sample base asrc input en selection** 5'b00000: 8k 5'b00001: 12k

Bit(s)	Mnemonic	Name	Description
			5'b00010: 16k
			5'b00011: 24k
			5'b00100: 32k
			5'b00101: 48k
			5'b00110: 96k
			5'b00111: 192kk
			5'b01000: 384k
			5'b01001: ext_i2s01_1x_en
			5'b01010: 5'bext_i2s02_1x_en
			5'b01011: ext_i2s03_1x_en
			5'b01100: ext_i2s04_1x_en
			5'b01101: ext_i2s05_1x_en
			5'b01110: ext_i2s06_1x_en
			5'b10000: 7.35k
			5'b10001: 11.025k
			5'b10010: 14.7k
			5'b10011: 22.05k
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4kk
			5'b11000: 352.8k
4:0		asmi1_mode	**control for i2sout1 sample base asrc input en selection**
			5'b00000: 8k
			5'b00001: 12k
			5'b00010: 16k
			5'b00011: 24k

Bit(s)	Mnemonic	Name	Description
			5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2s01_1x_en 5'b01010: 5'bext_i2s02_1x_en 5'b01011: ext_i2s03_1x_en 5'b01100: ext_i2s04_1x_en 5'b01101: ext_i2s05_1x_en 5'b01110: ext_i2s06_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k

11220108 PWR1_ASM_CON1 PWR1_ASM_CALI_CK_SEL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															pcm_out_asrc_cali_ck_sel	pcm_out_asrc_process_ck_sel
Type															RW	RW
Reset															0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcm_out_asrc_process_ck_sel	pcm_in_asrc_cali_ck_sel	pcm_in_asrc_process_ck_sel		i2s_out2_asrc_cali_ck_sel	i2s_out2_asrc_process_ck_sel		i2s_out1_asrc_cali_ck_sel	i2s_out1_asrc_process_ck_sel		i2s_in2_asrc_cali_ck_sel	i2s_in2_asrc_process_ck_sel		i2s_in1_asrc_cali_ck_sel	i2s_in1_asrc_process_ck_sel	
Type	RW	RW	RW		RW	RW		RW	RW		RW	RW		RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17		pcm_out_asrc_cali_ck_sel	**control for i2sout6 sample base asrc input en selection** 0:49.152M 1:45.1584M
16:15		pcm_out_asrc_process_ck_sel	**control for i2sout5 sample base asrc input en selection**
14		pcm_in_asrc_cali_ck_sel	**control for i2sout4 sample base asrc input en selection** 0:49.152M 1:45.1584M
13:12		pcm_in_asrc_process_ck_sel	**control for i2sout3 sample base asrc input en selection**
11		i2s_out2_asrc_cali_ck_sel	**control for i2sout2 sample base asrc input en selection** 0:49.152M 1:45.1584M
10:9		i2s_out2_asrc_process_ck_sel	**control for i2sout1 sample base asrc input en selection**
8		i2s_out1_asrc_cali_ck_sel	**control for i2sout2 sample base asrc input en selection** 0:49.152M 1:45.1584M
7:6		i2s_out1_asrc_process_ck_sel	**control for i2sout1 sample base asrc input en selection**
5		i2s_in2_asrc_cali_ck_sel	**control for i2sout2 sample base asrc input en selection** 0:49.152M

Bit(s)	Mnemonic	Name	Description
			1:45.1584M
4:3		i2s_in2_asrc_process_ck_sel	**control for i2sout1 sample base asrc input en selection**
2		i2s_in1_asrc_cali_ck_sel	**control for i2sout2 sample base asrc input en selection** 0:49.152M 1:45.1584M
1:0		i2s_in1_asrc_process_ck_sel	**control for i2sout1 sample base asrc input en selection**

112201F0 AFE_SINEGEN_CON0 AFE Sine-wave Gen Config 0 F0000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INNER_LOOP_BACK_MODE					dac_en	mute_sw_ch2	mute_sw_ch1	sine_mode_ch2				amp_div_ch2			freq_div_ch2
Type	RW					RW	RW	RW	RW				RW			RW
Reset	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	freq_div_ch2				sine_mode_ch1				amp_div_ch1			freq_div_ch1				
Type	RW				RW				RW			RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:27		INNER_LOOP_BACK_MODE	**Loopback mode testing for audio_conn.** Valid if SINE_MODE_CH1 > 8 for sinewave gen ch1 and SINE_MODE_CH2 > 8 for sinewave gen ch2. 0 : in_en[00], i_00, i_01 use sin_ch1 and sin_ch2 as input source 1 : in_en[02], i_02 use sin_ch1 input source 2 : in_en[03], i_03,i_04 use sin_ch1 and sin_ch2 as input source 3 : in_en[05], i_05, i_06 use sin_ch1 and sin_ch2 as input source (if 0x1d0[19]=0) 4 : in_en[07], i_07, i_08 use sin_ch1 and sin_ch2 as input source 5 : in_en[09], i_09 use sin_ch1, and i_14 use sin_ch1 as input source

Bit(s)	Mnemonic	Name	Description
			6 : in_en[11], i_11, i_12 use sin_ch1 and sin_ch2 as input source 7 : out_en[00], o_00, o_01 use sin_ch1 and sin_ch2 as input source 8 : out_en[02], o_02 use sin_ch1 as input source 9 : out_en[03], o_03, o_04 use sin_ch1 and sin_ch2 as input source 10 : out_en[05], o_05, o_06 use sin_ch1 and sin_ch2 as input source 11 : out_en[07], o_07, o_08 use sin_ch1 and sin_ch2, and o17,o_18 use sin_ch1 and sin_ch2 as input source, too 12 : out_en[09], o_09, o_10 use sin_ch1 and sin_ch2 as input source 13 : out_en[11], o_11 use sin_ch1 as input source 14 : out_en[12], o_12 use sin_ch1 as input source 15 : out_en[14]
26		dac_en	**Enables sinewave generator** 0: Disable sigen 1: Enable sigen
25		mute_sw_ch2	**Sinewave generator mute for ch2** 0: Unmute sigen 1: Mute sigen
24		mute_sw_ch1	**Sinewave generator mute for ch1** 0: Unmute sigen 1: Mute sigen
23:20		sine_mode_ch2	**Enables sinewave generator timing selection for ch2** 0 : 8k 1 : 11.025k 2 : 12k 3 : 16k

Bit(s)	Mnemonic	Name	Description
			4 : 22.05k 5 : 24k 6 : 32k 7 : 44.1k 8 : 48k 9~15 : Depending on bit[31:28] INNER_LOOP_BACK_MODE
19:17		amp_div_ch2	**Selects sinewave generator amplitude for ch2** 0 : sinewave_out/128 1 : sinewave_out/64 2 : sinewave_out/32 3 : sinewave_out/16 4 : sinewave_out/8 5 : sinewave_out/4 6 : sinewave_out/2 7 : sinewave_out/1
16:12		freq_div_ch2	**sinewave generator frequency selection for ch2 sampled by signal timing generator selection bit[23:20] (or bit[31:28]) for ch2** 0 : DC output 1 : 64/1 samples/period 2 : 64/2 samples/period 3 : 64/3 samples/period 4 : 64/4 samples/period 5 : 64/5 samples/period 6 : 64/6 samples/period x : 64/x samples/period 31 : 64/31 samples/period
11:8		sine_mode_ch1	**Enables sinewave generator timing selection for ch1**

Bit(s)	Mnemonic	Name	Description
			0 : 8k 1 : 11.025k 2 : 12k 3 : 16k 4 : 22.05k 5 : 24k 6 : 32k 7 : 44.1k 8 : 48k 9~15 : Depending on bit[31:28] INNER_LOOP_BACK_MODE
7:5		amp_div_ch1	**Selects sinewave generator amplitude for ch1** 0 : sinewave_out/128 1 : sinewave_out/64 2 : sinewave_out/32 3 : sinewave_out/16 4 : sinewave_out/8 5 : sinewave_out/4 6 : sinewave_out/2 7 : sinewave_out/1
4:0		freq_div_ch1	**sinewave generator frequency selection for ch2 sampled by signal timing generator selection bit[23:20] (or bit[31:28]) for ch1** 0 : DC output 1 : 64/1 samples/period 2 : 64/2 samples/period 3 : 64/3 samples/period 4 : 64/4 samples/period 5 : 64/5 samples/period

Bit(s)	Mnemonic	Name	Description
			6 : 64/6 samples/period x : 64/x samples/period 31 : 64/31 samples/period

11220320 AFE_BT_SECURITY0 daibt data array control 00000770

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11220324 AFE_BT_SECURITY1 daibt data array control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11220360 AFE_SPDIF2_OUT_CON0 AFE SPDIF2 Ouput Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11220364 AFE_SPDIF2_BASE AFE SPDIF2 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11220368 AFE_SPDIF2_CUR AFE SPDIF2 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1122036C AFE_SPDIF2_END AFE_SPDIF2_END 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11220370 AFE_TDM_OUT_CON0 AFE HDMI_OUT Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								HDMI_OUT_CH_NUM							HDMI_OUT_BIT_WIDTH	HDMI_OUT_ON
Type								RW							RW	RW
Reset								0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
8:4		HDMI_OUT_CH_NUM	**HDMI out channel number assignement.** 0: No HDMI out channel 1: 1-ch 2: 2-ch 3: 3-ch 4: 4-ch 5: 5-ch 6: 6-ch 7: 7-ch 8: 8-ch
1		HDMI_OUT_BIT_WIDTH	**This bit control the input data bit-width.**

Bit(s)	Mnemonic	Name	Description
			0: 16-bit 1: 32-bit
0		HDMI_OUT_ON	**Set this bit to 1 to enable HDMI out.** 0: no operation 1: enable HDMI out

11220374 AFE_TDM_OUT_BASE AFE HDMI_OUT Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_TDM_OUT_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_OUT_BASE													AFE_TDM_OUT_BASE_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:3		AFE_TDM_OUT_BASE	**Base address of the TDM input at master mode. Please always set AFE_TDM_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.**
2:0		AFE_TDM_OUT_BASE_LSB	

11220378 AFE_TDM_OUT_CUR AFE HDMI_OUT Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_TDM_OUT_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_OUT_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_TDM_OUT_CUR	**Indicates current address of the TDM input buffer.**

1122037C AFE_TDM_OUT_END AFE_TDM_OUT_END 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_TDM_OUT_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_OUT_END													AFE_TDM_OUT_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3		AFE_TDM_OUT_END	**Ending address of the TDM input at master mode. Please always set AFE_TDM_OUT_END[2:0] = 3'h7 for the convenience of the hardware implementation.**
2:0		AFE_TDM_OUT_END_LSB	

11220380 AFE_SPDIF_OUT_CON0 AFE SPDIF Ouput Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															AFE_SPDIF_OUT_CON1	AFE_SPDIF_OUT_CON0
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1		AFE_SPDIF_OUT_CON1	**PDN signal for SPDIF memif** 0: off 1: on
0		AFE_SPDIF_OUT_CON0	**PDN signal for SPDIF clock** 0: off 1: on

11220384 AFE_SPDIF_BASE AFE SPDIF Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_SPDIF_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_SPDIF_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_SPDIF_BASE	**Base address of the SPDIF input at master mode. Please always set AFE_SPDIF_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.**

11220388 AFE_SPDIF_CUR AFE SPDIF Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_SPDIF_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_SPDIF_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_SPDIF_CUR	**Indicates current address of the SPDIF input buffer.**

1122038C AFE_SPDIF_END AFE_SPDIF_END 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_SPDIF_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_SPDIF_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_SPDIF_END	**Ending address of the SPDIF input at master mode. Please always set AFE_SPDIF_END[2:0] = 3'h7 for the convenience of the hardware implementation.**

11220390 AFE_HDMI_CONN0 AFE HDMI Output Connection Control Register 0 76543210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	O_7_CFG				O_6_CFG				O_5_CFG				O_4_CFG			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	O_3_CFG				O_2_CFG				O_1_CFG				O_0_CFG			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		O_7_CFG	**These bits control the o_7 data.** 0: I_0 1: I_1 2: I_2

Bit(s)	Mnemonic	Name	Description
			3: I_3
			4: I_4
			5: I_5
			6: I_6
			7: I_7
			8: I_8
			9: I_9
			10: I_10
			11: I_11
			12: I_12
			13: I_13
			14: I_14
			15: I_15
27:24		O_6_CFG	**These bits control the o_6 data.**
			0: I_0
			1: I_1
			2: I_2
			3: I_3
			4: I_4
			5: I_5
			6: I_6
			7: I_7
			8: I_8
			9: I_9
			10: I_10
			11: I_11
			12: I_12
			13: I_13

Bit(s)	Mnemonic	Name	Description
			14: I_14
			15: I_15
23:20		O_5_CFG	**These bits control the o_5 data.**
			0: I_0
			1: I_1
			2: I_2
			3: I_3
			4: I_4
			5: I_5
			6: I_6
			7: I_7
			8: I_8
			9: I_9
			10: I_10
			11: I_11
			12: I_12
			13: I_13
			14: I_14
			15: I_16
19:16		O_4_CFG	**These bits control the o_4 data.**
			0: I_0
			1: I_1
			2: I_2
			3: I_3
			4: I_4
			5: I_5
			6: I_6
			7: I_7

Bit(s)	Mnemonic	Name	Description
			8: I_8
			9: I_9
			10: I_10
			11: I_11
			12: I_12
			13: I_13
			14: I_14
			15: I_17
15:12		O_3_CFG	**These bits control the o_3 data.**
			0: I_0
			1: I_1
			2: I_2
			3: I_3
			4: I_4
			5: I_5
			6: I_6
			7: I_7
			8: I_8
			9: I_9
			10: I_10
			11: I_11
			12: I_12
			13: I_13
			14: I_14
			15: I_18
11:8		O_2_CFG	**These bits control the o_2 data.**
			0: I_0
			1: I_1

Bit(s)	Mnemonic	Name	Description
			2: I_2
			3: I_3
			4: I_4
			5: I_5
			6: I_6
			7: I_7
			8: I_8
			9: I_9
			10: I_10
			11: I_11
			12: I_12
			13: I_13
			14: I_14
			15: I_19
7:4		O_1_CFG	**These bits control the o_1 data.**
			0: I_0
			1: I_1
			2: I_2
			3: I_3
			4: I_4
			5: I_5
			6: I_6
			7: I_7
			8: I_8
			9: I_9
			10: I_10
			11: I_11
			12: I_12

Bit(s)	Mnemonic	Name	Description
			13: I_13
			14: I_14
			15: I_20
3:0		O_0_CFG	**These bits control the o_0 data.**
			0: I_0
			1: I_1
			2: I_2
			3: I_3
			4: I_4
			5: I_5
			6: I_6
			7: I_7
			8: I_8
			9: I_9
			10: I_10
			11: I_11
			12: I_12
			13: I_13
			14: I_14
			15: I_21

11220394 AFE_8CH_I2S_OUT_CON AFE HDMI 8CH I2S out Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											I2S_WLEN		I2S_DELA	I2S_LRCK_INV	I2S_BCLK_INV	I2S_EN_PRE

													Y_DATA			
Type											RW		RW	RW	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:4		I2S_WLEN	**These bits control the HDMI I2S out bit-width.** 0: 8-bit 1: 16-bit 2: 24-bit 3: 32-bit
3		I2S_DELAY_DATA	**This bit controls the input delay data.** 0: not delay 1: first bit 1T delay
2		I2S_LRCK_INV	**This bit controls the inverse LRCK.** 0: not inverse LRCK. 1: Inverse LRCK.
1		I2S_BCLK_INV	**This bit controls the inverse BCLK.** 0: not inverse BCLK 1: inverse BCLK
0		I2S_EN_PRE	**This bit controls the enable for HDMI I2S out.** 0: off 1: on

11220398 AFE_HDMI_CONN1 AFE HDMI Output Connection Control Register 1 FEDCBA98

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	O_15_CFG				O_14_CFG				O_13_CFG				O_12_CFG			
Type	RW				RW				RW				RW			
Reset	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	O_11_CFG				O_10_CFG				O_9_CFG				O_8_CFG			
Type	RW				RW				RW				RW			

Reset	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		O_15_CFG	**These bits control the o_15 data.** 0: I_0 1: I_1 2: I_2 3: I_3 4: I_4 5: I_5 6: I_6 7: I_7 8: I_8 9: I_9 10: I_10 11: I_11 12: I_12 13: I_13 14: I_14 15: I_15
27:24		O_14_CFG	**These bits control the o_14 data.** 0: I_0 1: I_1 2: I_2 3: I_3 4: I_4 5: I_5 6: I_6 7: I_7

Bit(s)	Mnemonic	Name	Description
			8: I_8
			9: I_9
			10: I_10
			11: I_11
			12: I_12
			13: I_13
			14: I_14
			15: I_16
23:20		O_13_CFG	**These bits control the o_13 data.**
			0: I_0
			1: I_1
			2: I_2
			3: I_3
			4: I_4
			5: I_5
			6: I_6
			7: I_7
			8: I_8
			9: I_9
			10: I_10
			11: I_11
			12: I_12
			13: I_13
			14: I_14
			15: I_17
19:16		O_12_CFG	**These bits control the o_12 data.**
			0: I_0
			1: I_1

Bit(s)	Mnemonic	Name	Description
			2: I_2
			3: I_3
			4: I_4
			5: I_5
			6: I_6
			7: I_7
			8: I_8
			9: I_9
			10: I_10
			11: I_11
			12: I_12
			13: I_13
			14: I_14
			15: I_18
15:12		O_11_CFG	**These bits control the o_11 data.**
			0: I_0
			1: I_1
			2: I_2
			3: I_3
			4: I_4
			5: I_5
			6: I_6
			7: I_7
			8: I_8
			9: I_9
			10: I_10
			11: I_11
			12: I_12

Bit(s)	Mnemonic	Name	Description
			13: I_13
			14: I_14
			15: I_19
11:8		O_10_CFG	**These bits control the o_10 data.**
			0: I_0
			1: I_1
			2: I_2
			3: I_3
			4: I_4
			5: I_5
			6: I_6
			7: I_7
			8: I_8
			9: I_9
			10: I_10
			11: I_11
			12: I_12
			13: I_13
			14: I_14
			15: I_20
7:4		O_9_CFG	**These bits control the o_9 data.**
			0: I_0
			1: I_1
			2: I_2
			3: I_3
			4: I_4
			5: I_5
			6: I_6

Bit(s)	Mnemonic	Name	Description
			7: I_7
			8: I_8
			9: I_9
			10: I_10
			11: I_11
			12: I_12
			13: I_13
			14: I_14
			15: I_21
3:0		O_8_CFG	**These bits control the o_8 data.**
			0: I_0
			1: I_1
			2: I_2
			3: I_3
			4: I_4
			5: I_5
			6: I_6
			7: I_7
			8: I_8
			9: I_9
			10: I_10
			11: I_11
			12: I_12
			13: I_13
			14: I_14
			15: I_22

1122039C AFE_HDMI_CONN2 AFE HDMI Output Connection Control Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPDF2_USE_HDMI_LRCK	SPDF_USE_HDMI_LRCK														
Type	RW	RW														
Reset	0	0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
31		SPDF2_USE_HDMI_LRCK	**These bits control the SPDIF2 LRCK source** 0: SPDIF LRCK 1: USE HDMI LRCK
30		SPDF_USE_HDMI_LRCK	**These bits control the SPDIF LRCK source** 0: SPDIF LRCK 1: USE HDMI LRCK

112203A0 AFE_IRQ_MCU_CON AFE IRQ MCU Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ11_MCU_MODE				IRQ_ACC2_MCU_MODE				IRQ_ACC1_MCU_MODE				IRQ12_MCU_ON	IRQ11_MCU_ON	IRQ_ACC2_ON	IRQ_ACC1_ON
Type	RW				RW				RW				RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IRQ6_MCU_ON	IRQ5_MCU_ON	IRQ2_MCU_MODE				IRQ1_MCU_MODE						IRQ2_MCU_ON	IRQ1_MCU_ON
Type			RW	RW	RW				RW						RW	RW
Reset			0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		IRQ11_MCU_MODE	**Controls the IRQ11_MCU count unit** 4'h0: 8k 4'h1: 12k 4'h2: 16k 4'h3: 24k 4'h4: 32k 4'h5: 48k 4'h6: 96k 4'h7: 192k 4'h9: 11.025k 4'hb: 22.05k 4'hd: 44.1 4'he: 88.2 4'hf: 176.4
27:24		IRQ_ACC2_MCU_MODE	**Controls the IRQ_ACC2_MCU count unit** 4'h0: 8k 4'h1: 12k 4'h2: 16k 4'h3: 24k 4'h4: 32k 4'h5: 48k 4'h6: 96k 4'h7: 192k 4'h9: 11.025k 4'hb: 22.05k 4'hd: 44.1 4'he: 88.2

Bit(s)	Mnemonic	Name	Description
			4'hf: 176.4
23:20		IRQ_ACC1_MCU_MODE	**Controls the IRQ_ACC1_MCU count unit** 4'h0: 8k 4'h1: 12k 4'h2: 16k 4'h3: 24k 4'h4: 32k 4'h5: 48k 4'h6: 96k 4'h7: 192k 4'h9: 11.025k 4'hb: 22.05k 4'hd: 44.1 4'he: 88.2 4'hf: 176.4
19		IRQ12_MCU_ON	**This bit controls the enable for IRQ11_MCU, which is specialized for TDMOUT** 0: off 1: on
18		IRQ11_MCU_ON	**This bit controls the enable for IRQ11_MCU, which is specialized for TSF or common usage like IRQ1,2 when TSF is not used.** 0: off 1: on
17		IRQ_ACC2_ON	**This bit controls the enable for IRQ_ACC2_MCU, which is specialized for WIFI TSF** 0: off 1: on

Bit(s)	Mnemonic	Name	Description
16		IRQ_ACC1_ON	**This bit controls the enable for IRQ_ACC1_MCU, which is specialized for WIFI TSF** 0: off 1: on
13		IRQ6_MCU_ON	**This bit controls the enable for IRQ6_MCU, which is specialized for SPDIF.** 0: off 1: on
12		IRQ5_MCU_ON	**This bit controls the enable for IRQ5_MCU, which is specialized for HDMI 8ch I2S.** 0: off 1: on
11:8		IRQ2_MCU_MODE	**Controls the IRQ2_MCU count unit** 4'h0: 8k 4'h1: 12k 4'h2: 16k 4'h3: 24k 4'h4: 32k 4'h5: 48k 4'h6: 96k 4'h7: 192k 4'h9: 11.025k 4'hb: 22.05k 4'hd: 44.1 4'he: 88.2 4'hf: 176.4
7:4		IRQ1_MCU_MODE	**Controls the IRQ1_MCU count unit** 4'h0: 8k 4'h1: 12k

Bit(s)	Mnemonic	Name	Description
			4'h2: 16k
			4'h3: 24k
			4'h4: 32k
			4'h5: 48k
			4'h6: 96k
			4'h7: 192k
			4'h9: 11.025k
			4'hb: 22.05k
			4'hd: 44.1
			4'he: 88.2
			4'hf: 176.4
1		IRQ2_MCU_ON	**Controls the enbling of IRQ2_MCU** 0: Off 1: On
0		IRQ1_MCU_ON	**Controls the enbling of IRQ1_MCU** 0: Off 1: On

112203A4 AFE_IRQ_MCU_STATUS AFE IRQ MCU Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	spdif_miss_flag	afe_irq_miss_flag														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					IRQ12_MCU	IRQ11_MCU	IRQ_ACC2_MCU	IRQ_ACC1_MCU	afe_dam_intr_status	IRQ7_MCU	IRQ6_MCU	IRQ5_MCU	IRQ4_MCU	IRQ3_MCU	IRQ2_MCU	IRQ1_MCU
Type					RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		spdif_miss_flag	
30:16		afe_irq_miss_flag	
11		IRQ12_MCU	**This bit read the status for IRQ12_MCU** 0: No interrupt 1: IRQ12 interrupt
10		IRQ11_MCU	**This bit read the status for IRQ11_MCU** 0: No interrupt 1: IRQ11 interrupt
9		IRQ_ACC2_MCU	**This bit read the status for IRQ_ACC2_MCU** 0: No interrupt 1: IRQ_ACC2 interrupt
8		IRQ_ACC1_MCU	**This bit read the status for IRQ_ACC1_MCU** 0: No interrupt 1: IRQ_ACC1 interrupt
7		afe_dam_intr_status	
6		IRQ7_MCU	**This bit read the status for IRQ7_MCU** 0: No interrupt 1: IRQ7 interrupt
5		IRQ6_MCU	**This bit read the status for IRQ6_MCU** 0: No interrupt 1: IRQ6 interrupt
4		IRQ5_MCU	**This bit read the status for IRQ5_MCU** 0: No interrupt 1: IRQ5 interrupt
3		IRQ4_MCU	**This bit read the status for IRQ4_MCU** 0: No interrupt 1: IRQ4 interrupt

Bit(s)	Mnemonic	Name	Description
2		IRQ3_MCU	**This bit read the status for IRQ3_MCU** 0: No interrupt 1: IRQ3 interrupt
1		IRQ2_MCU	**This bit read the status for IRQ2_MCU (I2S)** 0: No interrupt 1: IRQ2 interrupt
0		IRQ1_MCU	**This bit read the status for IRQ1_MCU (VUL/DL1/DL2/AWB)** 0: No interrupt 1: IRQ1 interrupt

112203A8 AFE_IRQ_CLR AFE IRQ Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		IRQ_ACC2_MCU_MISS_CLR	IRQ_ACC1_MCU_MISS_CLR		IRQ12_MCU_MISS_CLR	IRQ11_MCU_MISS_CLR						IRQ5_MCU_MISS_CLR		IRQ3_MCU_MISS_CLR	IRQ2_MCU_MISS_CLR	IRQ1_MCU_MISS_CLR
Type		WO	WO		WO	WO						WO		WO	WO	WO
Reset		0	0		0	0						0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		IRQ_ACC2_MCU_CLR	IRQ_ACC1_MCU_CLR		IRQ12_MCU_CLR	IRQ11_MCU_CLR				IRQ_MCU_CLR	IRQ6_MCU_CLR	IRQ5_MCU_CLR		IRQ3_MCU_CLR	IRQ2_MCU_CLR	IRQ1_MCU_CLR
Type		WO	WO		WO	WO				WO	WO	WO		WO	WO	WO
Reset		0	0		0	0				0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
30		IRQ_ACC2_MCU_MISS_CLR	**This bit clears the status of IRQ_ACC2 miss flag.** 0: no operation 1: clear IRQ_ACC2 miss flag.

Bit(s)	Mnemonic	Name	Description
29		IRQ_ACC1_MCU_MISS_CLR	**This bit clears the status of IRQ_ACC1 miss flag.** 0: no operation 1: clear IRQ_ACC1 miss flag.
27		IRQ12_MCU_MISS_CLR	**This bit clears the status of IRQ12 miss flag.** 0: no operation 1: clear IRQ12 miss flag.
26		IRQ11_MCU_MISS_CLR	**This bit clears the status of IRQ11 miss flag.** 0: no operation 1: clear IRQ11 miss flag.
20		IRQ5_MCU_MISS_CLR	**This bit clears the status of IRQ5 miss flag.** 0: no operation 1: clear IRQ5 miss flag.
18		IRQ3_MCU_MISS_CLR	**This bit clears the status of IRQ3 miss flag.** 0: no operation 1: clear IRQ3 miss flag.
17		IRQ2_MCU_MISS_CLR	**This bit clears the status of IRQ2 miss flag.** 0: no operation 1: clear IRQ2 miss flag.
16		IRQ1_MCU_MISS_CLR	**This bit clears the status of IRQ1 miss flag.** 0: no operation 1: clear IRQ1 miss flag.
14		IRQ_ACC2_MCU_CLR	**This bit clears the status for IRQ_ACC2_MCU.** 0: no operation 1: clear IRQ_ACC2 interrupt.
13		IRQ_ACC1_MCU_CLR	**This bit clears the status for IRQ_ACC1_MCU.** 0: no operation 1: clear IRQ_ACC1 interrupt.

Bit(s)	Mnemonic	Name	Description
11		IRQ12_MCU_CLR	**This bit clears the status for IRQ12_MCU.** 0: no operation 1: clear IRQ12 interrupt.
10		IRQ11_MCU_CLR	**This bit clears the status for IRQ11_MCU.** 0: no operation 1: clear IRQ11 interrupt.
6		IRQ_MCU_CLR	**This bit clears the intDIR IRQ** 0: no operation 1: clear internal DIR Interrupt
5		IRQ6_MCU_CLR	**This bit clears the status for IRQ6_MCU.** 0: no operation 1: clear IRQ6 interrupt.
4		IRQ5_MCU_CLR	**This bit clears the status for IRQ5_MCU.** 0: no operation 1: clear IRQ5 interrupt.
2		IRQ3_MCU_CLR	**Clears the status for IRQ3_MCU.** 0: No operation 1: Clear MULTI IN interrupt
1		IRQ2_MCU_CLR	**Clears the status for IRQ2_MCU.** 0: No operation 1: Clear IRQ2 interrupt
0		IRQ1_MCU_CLR	**Clears the status for IRQ1_MCU.** 0: No operation 1: Clear IRQ1 interrupt

112203AC AFE_IRQ_MCU_CNT1 AFE IRQ1 MCU Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ_MCU_CNT1	

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_MCU_CNT1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:0		AFE_IRQ_MCU_CNT1	**Sets up the counter value for IRQ1 according to IRQ1_MODE. The IRQ1 counter in AFE will count down from AFE_IRQ_MCU_CNT1 and set up IRQ1 while IRQ1 counter reaches 1. Therefore, the maximum IRQ time for IRQ1 at 48kHz mode is 5s.**

112203B0 AFE_IRQ_MCU_CNT2 AFE IRQ2 MCU Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ_MCU_CNT2	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_MCU_CNT2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:0		AFE_IRQ_MCU_CNT2	**Sets up the counter value for IRQ2 according to IRQ2_MODE. The IRQ2 counter in AFE will count down from AFE_IRQ_MCU_CNT2 and set up IRQ2 while IRQ2 counter reaches 1. Therefore, the maximum IRQ time for IRQ2 at 48kHz mode is 5s.**

112203B8 AFE_IRQ_MCU_MON2 AFE IRQ MCU MON2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													IRQ6_MISS_CNT			
Type													RO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name			IRQ6_MISS_FLAG	IRQ5_MISS_FLAG	IRQ4_MISS_FLAG	MULTI_IN_IRQ2_MISS_FLAG	IRQ2_MISS_FLAG	IRQ1_MISS_FLAG								AFE_IRQ_MCU_CLR_PHASE
Type			RO	RO	RO	RO	RO	RO								RO
Reset			0	0	0	0	0	0								0

Bit(s)	Mnemonic	Name	Description
19:16		IRQ6_MISS_CNT	**Shows how many IRQ6 missed since this register is last cleared. Write 0x3a8[16] with 1 will clear this register.**
13		IRQ6_MISS_FLAG	**This bit shows if there is any miss of the IRQ6. Write 0x3a8[13] with 1 will clear this bit.** 0: no miss 1: miss had happened.
12		IRQ5_MISS_FLAG	**This bit shows if there is any miss of the IRQ5. Write 0x3a8[11] with 1 will clear this bit.** 0: no miss 1: miss had happened.
11		IRQ4_MISS_FLAG	**This bit shows if there is any miss of the IRQ4. Write 0x3a8[10] with 1 will clear this bit.** 0: no miss 1: miss had happened.
10		MULTI_IN_IRQ2_MISS_FLAG	**This bit shows if there is any miss of the IRQ2. Write 0x3a8[9] with 1 will clear this bit.** 0: no miss 1: miss had happened.
9		IRQ2_MISS_FLAG	**This bit shows if there is any miss of the IRQ2. Write 0x3a8[8] with 1 will clear this bit.** 0: no miss 1: miss had happened.
8		IRQ1_MISS_FLAG	**This bit shows if there is any miss of the IRQ1. Write 0x3a8[7] with 1 will clear this bit.** 0: no miss 1: miss had happened.

Bit(s)	Mnemonic	Name	Description
0		AFE_IRQ_MCU_CLR_PHASE	**For debuggingAFE_IRQ_MCU_CLR.**

112203BC AFE_IRQ_MCU_CNT5 AFE IRQ5 MCU Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112203C0 AFE_IRQ1_MCU_CNT_MON AFE IRQ1 MCU Count Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ1_CNT_MON	
Type															RO	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ1_CNT_MON															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:0		AFE_IRQ1_CNT_MON	**Monitors the counter value for IRQ1 according toIRQ1_MODE. The IRQ1 counter in AFE will count down from AFE_IRQ_MCU_CNT1.**

112203C4 AFE_IRQ2_MCU_CNT_MON AFE IRQ2 MCU Count Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name															AFE_IRQ2_CNT_MON	
Type															RO	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ2_CNT_MON															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:0		AFE_IRQ2_CNT_MON	**Monitors the counter value for IRQ2 according toI2S_MODE. The IRQ1 counter in AFE will count down from AFE_IRQ_MCU_CNT2.**

112203C8 AFE_IRQ1_MCU_EN_CNT_MON AFE IRQ1 MCU Enable Count Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_IRQ1_MCU_EN_CNT_MON															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ1_MCU_EN_CNT_MON															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_IRQ1_MCU_EN_CNT_MON	**Monitors the enable count number of IRQ1 enabling signal.**

112203CC AFE_IRQ5_MCU_CNT_MON AFE IRQ5 MCU Count Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ5_CNT_MON	
Type															RO	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ5_CNT_MON															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:0		AFE_IRQ5_CNT_MON	**Monitors the counter value for IRQ5 according to the HDMI Fs. The IRQ5 counter in AFE will count down from AFE_IRQ_MCU_CNT5.**

112203D0 AFE_IRQ_MCU_EN AFE IRQ MCU Enable Register 0000FFF3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_MCU_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1

Bit(s)	Mnemonic	Name	Description
15:0		AFE_IRQ_MCU_EN	

11220410 AFE_GAIN1_CON0 AFE Gain1 Control Register 0 0000C800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN1_SAMPLE_PER_STEP								GAIN1_MODE							GAIN1_ON
Type	RW								RW							RW
Reset	1	1	0	0	1	0	0	0	0	0	0	0	0			0

Bit(s)	Mnemonic	Name	Description
15:8		GAIN1_SAMPLE_PER_STEP	**gain1 sample per step**
7:3		GAIN1_MODE	**gain1 mode** 5'b00000: 8k 5'b00001: 12k

Bit(s)	Mnemonic	Name	Description
			5'b00010: 16k
			5'b00011: 24k
			5'b00100: 32k
			5'b00101: 48k
			5'b00110: 96k
			5'b00111: 192kk
			5'b01000: 384k
			5'b10000: 7.35k
			5'b10001: 11.025k
			5'b10010: 14.7k
			5'b10011: 22.05k
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4kk
			5'b11000: 352.8k
0		GAIN1_ON	**gain1 on** 0: Off 1: On

11220414 AFE_GAIN1_CON1 AFE Gain1 Control Register 1 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN1_TARGET			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN1_TARGET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0		GAIN1_TARGET	**gain1 target**

11220418 AFE_GAIN1_CON2 AFE Gain1 Control Register 2 0007C5E5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN1_DOWN_STEP			
Type													RW			
Reset													0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN1_DOWN_STEP															
Type	RW															
Reset	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
19:0		GAIN1_DOWN_STEP	**gain1 down step**

1122041C AFE_GAIN1_CON3 AFE Gain1 Control Register 3 00083BCD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN1_UP_STEP			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN1_UP_STEP															
Type	RW															
Reset	0	0	1	1	1	0	1	1	1	1	0	0	1	1	0	1

Bit(s)	Mnemonic	Name	Description
19:0		GAIN1_UP_STEP	**gain1 up step**

11220424 AFE_GAIN1_CUR AFE Gain1 Cursor Register 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													AFE_GAIN1_CUR			
Type													RW			
Reset													1	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_GAIN1_CUR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0		AFE_GAIN1_CUR	**Indicates the current gain 1.**

11220428 AFE_GAIN2_CON0 AFE Gain2 Control Register 0 0000C800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN2_SAMPLE_PER_STEP								GAIN2_MODE							GAIN2_ON
Type	RW								RW							RW
Reset	1	1	0	0	1	0	0	0	0	0	0	0	0			0

Bit(s)	Mnemonic	Name	Description
15:8		GAIN2_SAMPLE_PER_STEP	**GAIN2 sample per step**
7:3		GAIN2_MODE	**GAIN2 mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b10000: 7.35k 5'b10001: 11.025k

Bit(s)	Mnemonic	Name	Description
			5'b10010: 14.7k
			5'b10011: 22.05k
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4kk
			5'b11000: 352.8k
0		GAIN2_ON	**GAIN2 on** 0: Off 1: On

1122042C AFE_GAIN2_CON1 AFE Gain2 Control Register 1 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN2_TARGET			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN2_TARGET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0		GAIN2_TARGET	**GAIN2 target**

11220430 AFE_GAIN2_CON2 AFE Gain2 Control Register 2 0007C5E5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN2_DOWN_STEP			
Type													RW			
Reset													0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN2_DOWN_STEP															
Type	RW															

Reset	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
19:0		GAIN2_DOWN_STEP	**GAIN2 down step**

11220434 AFE_GAIN2_CON3 AFE Gain2 Control Register 3 00083BCD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GAIN2_UP_STEP			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GAIN2_UP_STEP															
Type	RW															
Reset	0	0	1	1	1	0	1	1	1	1	0	0	1	1	0	1

Bit(s)	Mnemonic	Name	Description
19:0		GAIN2_UP_STEP	**GAIN2 up step**

1122043C AFE_GAIN2_CUR AFE Gain2 Cursor Register 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													AFE_GAIN2_CUR			
Type													RW			
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_GAIN2_CUR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
19:0		AFE_GAIN2_CUR	**Indicates the current gain 2.**

11220480 AFE_IEC_CFG AFE IEC958 Config 01900000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	IEC_FORCE_UPDATE_SIZE								IEC_SW_RST	IEC_REG_LOCK_EN	IEC_MUTE	IEC_FORCE_UPDATE	IEC_DOWN_SAMPLE		RISC_SWAP_IEC_BYTE	IEC_EN
Type	RW								RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							IEC_DST_BIT_REV	IEC_MAT_CRC_EN	IEC_MAT_LEN	IEC_RAW_24BIT_SWITCH	IEC_RAW_24BIT	VALID_DATA	IEC_MUTE_DATA		IEC_PCM_SEL	IEC_RAW_SEL
Type							RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset							0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
31:24		IEC_FORCE_UPDATE_SIZE	**The time to force update when how many samples remain for this burst**
23		IEC_SW_RST	
22		IEC_REG_LOCK_EN	**When enable, the IEC register including IEC_NX_SAM_NUM, IEC_BURST_LEN, IEC_NSADR and IEC_NXBURST_RDY. These registers will only be written during IEC interrupt and force update or next burst start if there is no force update.** 0: disable register lock 1: enable register lock
21		IEC_MUTE	
20		IEC_FORCE_UPDATE	**force IEC958 HW update burst information**
19:18		IEC_DOWN_SAMPLE	**IEC958 downsample rate** 0: No downsample 1: downsample by 2 3: downsample by 4
17		RISC_SWAP_IEC_BYTE	
16		IEC_EN	**IEC958 enable control** 0: disable 1: enable

Bit(s)	Mnemonic	Name	Description
9		IEC_DST_BIT_REV	**IEC958 DST bit reverse**
8		IEC_MAT_CRC_EN	**IEC958 output CRC result for MAT** 0: disable 1: enable
7		IEC_MAT_LEN	**PD output REG_IEC958_NEXT_LENGTH[18:3]**
6		IEC_RAW_24BIT_SWITCH	**IEC958 24bit raw data bytes switch mode**
5		IEC_RAW_24BIT	**IEC958 raw data 24bit mode**
4		VALID_DATA	**IEC958 valid data**
3		IEC_MUTE_DATA	
1		IEC_PCM_SEL	**IEC958 PCM select** 0: PCM data 1: encoded data
0		IEC_RAW_SEL	**IEC958 data source** 0: cooked data 1: raw data (from DRAM)

11220484 AFE_IEC_NSNUM AFE IEC958 Next Interrupt Number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IEC_NX_INTR_NUM													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			IEC_NX_SAM_NUM													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:16		IEC_NX_INTR_NUM	**The time to generate interrupt when how many samples remain for this burst**

Bit(s)	Mnemonic	Name	Description
13:0		IEC_NX_SAM_NUM	**The next sample number represented by next burst data**

11220488 AFE_IEC_BURST_INFO AFE IEC958 Register Lock Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IEC_REG_LOCK_STA							IEC_NXBURST_RDY
Type									RO							RW
Reset									0							0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IEC_BURST_INFO															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23		IEC_REG_LOCK_STA	**Register lock status for IEC958** 0: Not locked 1: Locked
16		IEC_NXBURST_RDY	**Ready status for next burst information** 0: Ready for next burst information 1: Not ready
15:0		IEC_BURST_INFO	**IEC958 burst information**

1122048C AFE_IEC_BURST_LEN AFE IEC958 Burst Length 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														IEC_BURST_LEN		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IEC_BURST_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
18:0		IEC_BURST_LEN	**number of bits for next burst**

11220490 AFE_IEC_NSADR AFE IEC958 Next Source Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IEC_NSADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IEC_NSADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		IEC_NSADR	**Next start address for next sample data**

112204A0 AFE_IEC_CHL_STAT0 AFE IEC958 L-Channel Status Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_IEC_CHL_STAT0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IEC_CHL_STAT0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_IEC_CHL_STAT0	**LSB of IEC958 L-Channel status**

112204A4 AFE_IEC_CHL_STAT1 AFE IEC958 L-Channel Status Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	AFE_IEC_CHL_STAT1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		AFE_IEC_CHL_STAT1	**MSB of IEC958 L-Channel status**

112204A8 AFE_IEC_CHR_STAT0 AFE IEC958 R-Channel Status Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_IEC_CHR_STAT0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IEC_CHR_STAT0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_IEC_CHR_STAT0	**LSB of IEC958 R-Channel status**

112204AC AFE_IEC_CHR_STAT1 AFE IEC958 R-Channel Status Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IEC_CHR_STAT1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		AFE_IEC_CHR_STAT1	**MSB of IEC958 R-Channel status**

112204B0 AFE_IEC2_CFG AFE IEC958-2 Config 01900000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112204B4 AFE_IEC2_NSNUM AFE IEC958-2 Next Interrupt Number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112204B8 AFE_IEC2_BURST_INFO AFE IEC958-2 Register Lock Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112204BC AFE_IEC2_BURST_LEN AFE IEC958-2 Burst Length 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112204C0 AFE_IEC2_NSADR AFE IEC958-2 Next Source Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112204D0 AFE_IEC2_CHL_STAT0 AFE IEC958-2 L-Channel Status Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112204D4 AFE_IEC2_CHL_STAT1 AFE IEC958-2 L-Channel Status Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112204D8 AFE_IEC2_CHR_STAT0 AFE IEC958-2 R-Channel Status Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112204DC AFE_IEC2_CHR_STAT1 AFE IEC958-2 R-Channel Status Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11220500 AFE_SPDIFIN_CFG0 AFE SPDIFIN Control Register0 008C6400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INV_LRCK	OFF_IECCLK	INV_IECCLK	chstslr	OFF_BITCLK	INV_BITCLK	GMAT_BITCELL_NUM_SEL		MAX_LEN_NUM							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPGLITCH	DE_SEL		DE_CNT					TimeOut2IDLE_EN	SPDIFRX_INTEN	DERR2IDLE_EN		DPER2IDLE_EN	PARITY	SPDIFRX_FLIP	SPDIFRX_EN
Type	RW	RW		RW					RW	RW	RW		RW	RW	RW	RW
Reset	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		INV_LRCK	**inverse recovery LRCK** 0: not inverted 1: inverted
30		OFF_IECCLK	**off (zero) recovery IECCLK which be the input to the APLL** 0: normal mode 1: disabled clock output
29		INV_IECCLK	**inverse recovery IECCLK which be the input to the APLL** 0: not inverted 1: inverted
28		chstslr	**capture Left/Right channel status informations** 0 : Left (default) 1 : Right
27		OFF_BITCLK	**off (zero) recovery BITCLK which be the input to the APLL** 0: normal mode 1: disabled clock output
26		INV_BITCLK	**inverse recovery BITCLK which be the input to the APLL**

Bit(s)	Mnemonic	Name	Description
			0: not inverted 1: inverted
25:24		GMAT_BITCELL_NUM_SEL	**How many number of bitcell cycle to take during getmini and training phase before the SPDIFIN receiver begin to decode.** 2'b00: 32 cycles. 2'b01: 64 cycles. 2'b10: 128 cycles. 2'b11: 256 cycles.
23:16		MAX_LEN_NUM	**max number sampled by spdifin_clk. The input bitcell will be sampled by spdifin_clk. The output will be invalid If the value is larger than the max number, and the state machine will go to the idle state to restart the initial process.** Take 32k input sample rate and 432Mhz spdifin_clk for example: half of bitcell 1 would be the shortest interval and will be the rate of 32k*128=4.096Mhz. spdifin_clk/4.096 = 105. and the longest interval will be the preamble with length around 3*105 = 315 sample counts. Consider the 3% input frequency variation ; then we use 315*1.03 = 324 plus 4 (and a few margin for i/o clock skew) = 328 = 2*MAX_LEN_NUM[7:0]. We need to use MAX_LEN_NUM[7:0] = 164 (0xA4) for 432MHZ and 224 (0xE0) for 594MHZ spdifin_clk
15		BPGLITCH	**bypass the input de-glitch function** 0: de-glitch function enabled 1: de-glitch function bypass
14:13		DE_SEL	**de-glitch function : input threshold used to be recognized as non-glitch signal.** 0: 3 sample counts 1: 14 sample counts 2: 30 sample counts 3: decided by DE_CNT[4:0]
12:8		DE_CNT	**de-glitch function : input threshold counter.** User defines threshold value

Bit(s)	Mnemonic	Name	Description
7		TimeOut2IDLE_EN	**TimeOut Error flag return to IDLE state enabled bit.** 0: soft reset (default) 1: enabled
6		SPDIFRX_INTEN	**SPDIFRX interrupt enabled. (Interrupt here just pass the interrupt flag to RISC/DSP only)** 0: disabled 1: enabled
5:4		DERR2IDLE_EN	**decoding error type 1 return to IDLE state enable bit** 01: sample count error (the valid count is counted from 1~28, the sample count will be error if count up beyond 28) 10: parity check error / subframe
3		DPERR2IDLE_EN	**decoding error type 2** Sync signal preamble error return to IDLE state enable bit
2		PARITY	**parity polarity** 0: even parity 1: odd parity
1		SPDIFRX_FLIP	**decoded data flip** 0: no flip. 1: flip 24-bit data
0		SPDIFRX_EN	**SPDIFRX enabled (soft reset). PS : The effective enabled bit =SPDIFRX_EN | SPDIFRX_EN2** 0: soft reset (default) 1: enabled

11220504 AFE_SPDIFIN_CFG1 AFE SPDIFIN Control Register1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	spdifin_int_en												use_iecclk_spdi	use_iecclk_spdi	pinmux_se	apllin_sel_bitclk

													f_as_audclk2	f_as_audclk	l_bitcli	_spdifin
Type	RW												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	loopback_spdf2_real	loopback_spdf_real	spdifin_iecclk_sel	spdifin_bitclk_sel	bypass_spdfin_spdf2_real	bypass_spdfin_spdf_real	seliecclk2_fromspdif	seliecclk1_fromspdif		FIFOSTARTPOINT			DEC2_SEL_SPDFIN_CLK	DEC2_SEL_SPDIFIN	SEL_SPDIFIN_CLK	SEL_SPDIFIN
Type	RW	RW	RW	RW	RW	RW	RW	RW		RW			RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:20		spdifin_int_en	**spdifin interrupt enable bit group, every corresponding bit = 1 means turned on, and 0 means turned off:** [11] : channel status collection interrupt [10] : when intDIR enters decoding stage and found that chansts bit[1] (audiobit) = 0 that means bitstream is PCM type. Then intDIR will check whether the parity bit has consecutive errors up to 9 times. If so, the intDIR will interrupt RISC to tell RISC should do the mute. [9] : audiobit (chansts[1]) or pre-amphasis field (chansts[5:3]) change interrupt. [8] : Time out interrupt (plug-in state to plug-out detection used) [7:6] : spdifin input fifo error interrupt (overrun/underrun detection) [5] : decoding error @ parity check failed [4] : decoding error @ invalid bitcnt (invalid subframe structure) [3] : preamble error @ symbol W [2] : preamble error @ symbol M [1] : preamble error @ symbol B [0]: preamble error no matter what the symbol is
19		use_iecclk_spdif_as_audclk2	**use recovery clock (iecclk) as aud_clk2 (audio master clock for DEC1)** 0 : normal mode

Bit(s)	Mnemonic	Name	Description
			1 : choose recovery clock (iecclk)
18		use_iecclk_spdif_as_audclk	**use recovery clock (iecclk) as aud_clk (audio master clock for DECo)** 0 : normal mode 1 : choose recovery clock (iecclk)
17		pinmux_sel_bitcell	**pin mux selection of spmclk or spbck for spdifin input.** 0 : spmclk 1 : spbck
16		apllin_sel_bitclk_spdifin	**apll input select bit.** 0 : normal mode (apll input original path) 1 : bitclk recovery mode (choose spdifin recovery bitclk)
15		loopback_spdf2_real	**loop back (spdif-out to spdifin), engineer test only.** 0 : normal mode. 1 : loop back mode (choose spdf2_real).
14		loopback_spdf_real	**loop back (spdif-out to spdifin), engineer test only.** 0 : normal mode. 1 : loop back mode (choose spdf_real if bit[15] = 0).
13		spdifin_iecclk_sel	**select iecclk or bitclk as aud_clk (audio master clock) input.** 0 : choose bitclk 1 : choose iecclk
12		spdifin_bitclk_sel	**select iecclk or bitclk as APLL clock input (the bit field 16 of SPDIFIN_CFG1 should be set to 1 as well to make it effective)** 0 : choose bitclk 1 : choose iecclk
11		bypass_spdfin_spdf2_real	**bypass spdifin input to spdf2 output.** 0 : normal mode.

Bit(s)	Mnemonic	Name	Description
			1 : bypass mode.
10		bypass_spdfin_spdf_real	**bypass spdifin input to spdf output.** 0 : normal mode. 1 : bypass mode.
9		selіecclk2_fromspdif	**choose spdifin recovery iecclk for spdf2_real.** 0 : disabled 1 : enabled
8		selіecclk1_fromspdif	**choose spdifin recovery iecclk for spdf_real.** 0 : disabled 1 : enabled
6:4		FIFOSTARTPOINT	**FIFO read start pointer: the input sample count will store into FIFO, the read start pointer is programmable.** 0: 3 (default) 1: 5 2: 6 3: 7 4: 8 5: 10 6: 11 7: 12
3		DEC2_SEL_SPDIFIN_CLK	**select SPDIFIN recovery BITCLK and LRCK as LINE-IN source for decoder 1.** 0: disabled 1: enabled
2		DEC2_SEL_SPDIFIN	**select SPDIFIN decoded data into LINE-IN buffer for decoder 1.** 0: disabled 1: enabled
1		SEL_SPDIFIN_CLK	**select SPDIFIN recovery BITCLK and LRCK as LINE-IN source for decoder 0.**

Bit(s)	Mnemonic	Name	Description
			0: disabled 1: enabled
0		SEL_SPDIFIN	**select SPDIFIN decoded data into LINE-IN buffer for decoder 0.** 0: disabled 1: enabled

11220508 AFE_SPDIFIN_CHSTS1 SPDIFIN channel status 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHANNEL_STS1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHANNEL_STS1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CHANNEL_STS1	**CHANNEL_STS[31:0]** IEC958 channel status registers. It updates itself every blocks (192 frames)

1122050C AFE_SPDIFIN_CHSTS2 SPDIFIN channel status 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHANNEL_STS2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHANNEL_STS2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CHANNEL_STS2	**CHANNEL_STS[63:32]**

Bit(s)	Mnemonic	Name	Description

11220510 AFE_SPDIFIN_CHSTS3 SPDIFIN channel status 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHANNEL_STS3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHANNEL_STS3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CHANNEL_STS3	**CHANNEL_STS[95:64]**

11220514 AFE_SPDIFIN_CHSTS4 SPDIFIN channel status 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHANNEL_STS4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHANNEL_STS4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CHANNEL_STS4	**CHANNEL_STS[127:96]**

11220518 AFE_SPDIFIN_CHSTS5 SPDIFIN channel status 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHANNEL_STS5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHANNEL_STS5															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CHANNEL_STS5	**CHANNEL_STS[159:128]**

1122051C AFE_SPDIFIN_CHSTS6 SPDIFIN channel status 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHANNEL_STS6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHANNEL_STS6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CHANNEL_STS6	**CHANNEL_STS[191:160]**

11220520 AFE_SPDIFIN_DEBUG1 SPDIFIN DEBUG status 1 001FF018

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	spdifin_int2risc			CS								MINBLENCNTMEM				
Type	RO			RO								RO				
Reset	0			0	0	0	0	0				1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MINBLENCNTMEM					dlerr		AVBLENCNTMEM								
Type	RO					RO		RO								
Reset	1	1	1	1		0		0	0	0	0	1	1	0	0	0

Bit(s)	Mnemonic	Name	Description
31		spdifin_int2risc	**spdifin error handling interrupt flag, it is the "OR" result of all exception handling flag (10 cases).**
28:24		CS	**current state of decoding state machine** 5'b00000: IDLE (no input)

Bit(s)	Mnemonic	Name	Description
			5'b00001: Get minimum bitcell length 5'b00010: Training average bitcell length 5'b00100: Tracking left channel preamble B/M 5'b01000: Locking block head preamble B
20:12		MINBLENCNTMEM	**Minimum bit length counts sampled by MCLK**
10		dlerr	**Data latch error flag when inner status error by bitclk polarity abnormal change; Setup 0x52D8[17]=1 will give a interrupt to RISC. Use 0x52B0[17]=1 to write clear this bit.** 0 : no data latch error happen 1 : data latch error
8:0		AVBLENCNTMEM	**Average bit length counts sampled by MCLK**

11220524 AFE_SPDIFIN_DEBUG2 SPDIFIN DEBUG status 2 01FF1003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	fifoerr		rd_prempty	wr_prefull	splin_lrck	chanstsIntFlag	perr9timesFlag	SFC								
Type	RO		RO	RO	RO	RO	RO	RO								
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPDIFIN_EN	STARTRD	FIRSTPCSHOW	BITCLK_POLARITY	TimeOut	TimeOuterr	bitclk_spdif	BITCNT					drb		DECBIT	
Type	RO	RO	RO	RO	RO	RO	RO	RO					RO		RO	
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:30		fifoerr	**fifo error flag:** [0] wirte full [1] read empty
29		rd_prempty	**spdifin input buffer read pre-empty signal (next read address equals write address after startrd)**

Bit(s)	Mnemonic	Name	Description
28		wr_prefull	**spdifin input buffer write pre-full signal (next write address equals read address after startrd)**
27		splin_lrck	**Subframe counter** default = -1. normal = 0 ~ 383.
26		chanstsIntFlag	**Channel status interrupt flag**
25		perr9timesFlag	**Parity bit consecutive errors up to 9 times interrupt flag when audioBit (chasts[1]) = 0.**
24:16		SFC	**Subframe counter** default = -1. normal = 0 ~ 383.
15		SPDIFIN_EN	**SPDIFRX softreset for decoder 0**
14		STARTRD	**FIFO start read flag** It means the re-build bitcell waveform starts.
13		FIRSTPCSHOW	**The input signal shows(phase changes)**
12		BITCLK_POLARITY	**Bit clock recovery phase polarity** 0: not inverted. 1: inverted.
11		TimeOut	**Time Out pre-error flag.(advanced phase of TimeOuterr)**
10		TimeOuterr	**Time Out error flag.**
9		bitclk_spdif	**Bit clock recovery phase polarity.**
8:4		BITCNT	**Decoded bit counter** 5'b00000: reset value 5'b11111: idle state 5'b00000: preamble state other valid value 1~28.
3:2		drb	**Decision result buffer** 2'b00: no defined idle state. 2'b01: input length < 1.5 bitcell unit

Bit(s)	Mnemonic	Name	Description
			2'b10: 1.5 bitcell unit <= input length < 2.5 bitcell unit 2'b11: input length >= 2.5 bitcell unit
1:0		DECBIT	**Decoded data bit** 2'b00: decoded bit = 0 2'b01: decoded bit = 1 2'b10: undefined state 2'b11: Invalid state

11220528 AFE_SPDIFIN_DEBUG3 SPDIFIN DEBUG status 3 0001FF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RBIN				RBCNT								LRC_spdif	derr_new	bitclk	RDATA
Type	RO				RO								RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDATA								audioBit_preamphsisBit_change	TimeOuterr	DERR		DPERR			
Type	RO								RO	RO	RO		RO			
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		RBIN	**FIFO read address port**
27:20		RBCNT	**Re-build waveform counter** it will start counting from 0 to rdata[9:0] for each bitcell
19		LRC_spdif	**recovery word clock signal.**
18		derr_new	**Additional decoding error flag status. When this bit = 1; it represents any invalid BMC such as preamble 3N pulse showing on the valid data bit field range (0~28). Enable 0x52D8[18]=1 will give a interrupt to RISC. Write 0x52B0[18]=1 will clear this bit.** 0 : no new data error happen

Bit(s)	Mnemonic	Name	Description
			1 : data error error
17		bitclk	**recovery pre-bitclk signal (advance 1T phase)**
16:8		RDATA	**FIFO read data port**
7		audioBit_preamphsisBit_change	**audiobit (chansts[1]) or pre-amphasis field (chansts[5:3]) change if ECO is OK**
6		TimeOuterr	**Time Out error flag.**
5:4		DERR	**Decoding error** 2'b01: sample counter error. 2'b10: parity check error.
3:0		DPERR	**Decoding preamble error** 4'b0000: no error 4'b0001: preamble error 4'b0010: preamble B error 4'b0100: preamble M error 4'b1000: preamble W error

1122052C AFE_SPDIFIN_DEBUG4 SPDIFIN DEBUG status 4 000001FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPDIFIN_INT2RISC_BCK								SPDIFIN_EN	SPDIFIN2_EN	RBIN					WBIN
Type	RO								RO	RO	RO					RO
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WBIN				bitcell	bitcell_rebuild	bitclk_spdif	WDATA								
Type	RO				RO	RO	RO	RO								
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31		SPDIFIN_INT2RISC_BCK	**Interrupt to RISC flag.**

Bit(s)	Mnemonic	Name	Description
23		SPDIFIN_EN	**The same as SPDIFIN_DEBUG2 [15]**
22		SPDIFIN2_EN	**SPDIFRX softreset for decoder 1**
21:17		RBIN	**5-bit FIFO read address port (including 1 MSB direction bit)**
16:12		WBIN	**5-bit FIFO write address port (including 1 MSB direction bit)**
11		bitcell	**input bitcell polarity.**
10		bitcell_rebuild	**rebuild bitcell polarity**
9		bitclk_spdif	**recovery bitclk signal.**
8:0		WDATA	**FIFO write data port**

11220530 AFE_SPDIFIN_EC SPDIFIN edge Clear 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														derr_clear_new	clr_dataLatchError	clr_lrc_change
Type														W1C	W1C	W1C
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	edge_flag_clear				spdifin_error_clear											
Type	W1C				W1C											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
18		derr_clear_new	**clear preamble 3N pulse range error.Write bit = 1 means do write clear, and will do auto clear in the next cycle**
17		clr_dataLatchError	**clear data latch error.Write bit = 1 means do write clear, and will do auto clear in the next cycle**
16		clr_lrc_change	**spdifin LRCK (sample rate) change interrupt clear bit. Write bit = 1 means do write clear, and will do auto clear in the next cycle.**
15:12		edge_flag_clear	**spdifin edge interrupt clear bit group, every corresponding bit = 1 means do write clear, and will do auto clear in the next cycle:**

Bit(s)	Mnemonic	Name	Description
			[3] : reserved [2] : clear ARC channel [1] : clear coaxial channel [0] : clear optical channel
11:0		spdifin_error_clear	**spdifin interrupt clear bit group, every corresponding bit = 1 means do write clear, and will do auto clear in the next cycle:** [11] : channel status collection interrupt clear. [10] : userCode collection interrupt clear. [9] : word clock (timer lrck) input change interrupt clear. [8] : Time out interrupt (plug-in state to plug-out detection used) clear [7:6] : spdifin input fifo error interrupt (overrun/underrun detection) clear [5] : decoding error @ parity check failed clear [4] : decoding error @ invalid bitcnt (invalid subframe structure) clear [3] : preamble error @ symbol W clear [2] : preamble error @ symbol M clear [1] : preamble error @ symbol B clear [0] : preamble error clear (no matter the symbol is)

11220534 AFE_SPDIFIN_CKLOCK_CFG SPDIFIN Clock Lock Configuration 00010600

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								spdifin_locked	spdifin_clkrecover_cfg							
Type								W1C	RW							
Reset								0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spdifin_clkrecover_cfg															
Type	RW															
Reset	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24		spdifin_locked	**SPDIFIN Clock Lock Triggle Status**
23:0		spdifin_clkrecover_cfg	**SPDIFIN Clock Recovery Configuration**

1122053C AFE_SPDIFIN_BR SPDIFIN bitclk recovery Configuration 00018000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	iec_parcheck_err_num						coaxial_sig_sel	arc_sig_sel	indicator_fine_tune			auto_fix_mode_en		tune_mode		bitcell_lowerbound
Type	RW						RW	RW	RW			RW		RW		RW
Reset	0	0	0	0			0	0	0	0	0	0		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bitcell_lowerbound				subframe_number					howManyFs						BRE
Type	RW				RW					RW						RW
Reset	1	0	0	0	0	0	0	0		0	0	0				0

Bit(s)	Mnemonic	Name	Description
31:28		iec_parcheck_err_num	**Emu ESD short attacks iec signal in data field (parity bit error on purpose) to check intDIR interrupt happen :** 0 : all parity bit send by iec is OK 1 : 1 errors 2 : 2 consecutive errors 9 : 3 consecutive errors Note : The number decides how many consecutive subframe parity bit error and each time software update the value different from last update will activate the new error happen.
25		coaxial_sig_sel	**Coaxial signal selection reserved bit :** 0 : from coaxial analog buffer 1 : tied low
24		arc_sig_sel	**ARC signal selection reserved bit :** 0 : from ARC analog buffer 1 : tied low

Bit(s)	Mnemonic	Name	Description
23:21		indicator_fine_tune	**Long term frequency indicator (0x52C4) initial value :** 0 : 0 1 : 1 2 : 2 3 : 3 4 : -1 5 : -2 6 : -3 7 : -4
20		auto_fix_mode_en	**HBR input lock ability auto-fixed threshold mode : whenever enable this bit, it will preview the input frequency roughly during initialization stage of the INTDIR. The output is previewed in the bit field [31:28] of the register 0x52EC** 1'b0 : disabled 1'b1 : enabled
18:17		tune_mode	**HBR input lock ability tuning mode :** 2'b00 : mode0 (disable duty_tuner/lowerbound enabled/instant threshold) 2'b01 : mode1 (disable duty_tuner/lowerbound enabled/half-sample threshold) 2'b10 : mode2 (enable duty_tuner/lowerbound enabled/half-sample threshold) 2'b11 : mode1 (enable duty_tuner/lowerbound enabled/instant threshold)
16:12		bitcell_lowerbound	**number of bitcell (128fs) lower bound counted by spdifin sys_clk, where fs = 192KHZ counted by spdifin sys_clk which is 594MHZ at most.** 594MHZ/(192K*128) = 24.169, default = 5'd24 for 192KHZ input.
11:8		subframe_number	**Bitclk recovery update timing:** 0 : 1 subframe 1 : 2 subframes 2 : 4 subframes

Bit(s)	Mnemonic	Name	Description
			3 : 8 subframes 4 : 16 subframes ... x : 2^x subframes ... 15 : 2^15 subframes
6:4		howManyFs	**Bitclk recovery Fs type to APLL input** 0 : 32fs 1 : 64fs 2 : 128fs 3 : 256fs 4 : 512fs 5 : 1024fs 6 : 2048fs 7 : 4096fs
0		BRE	**Bitclk recovery enable bit** 0 : disable 1 : enable

11220540 AFE_SPDIFIN_BR_DBG1 SPDIFIN bitclk recovery debug information 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				amplitude												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	amplitude															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:0		amplitude	**Bitclk recovery debug information 1**

Bit(s)	Mnemonic	Name	Description
			: amplitude[28:0] calculated by constant clock rate (432M/594M)

11220544 AFE_SPDIFIN_CKFBDIV SPDIFIN CKFBDIV 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		apll_fbdiv														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	apll_fbdiv															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		apll_fbdiv	**SPDIFIN Clock Locked fbdiv for APLL**

11220548 AFE_SPDIFIN_INT_EXT 00000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	edge_flag_int				bitcell_deg				bitcell_raw			auto_thr_en	derr_new_reten	derr_new_det_en	dataLatchError_det_en	
Type	RO				RO				RO			RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	input_sel				edge_det_en				edge_cnt							
Type	RW				RW				RW							
Reset	0	0			0	0	0	0	0	0	0	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		edge_flag_int	**Multi-input detection status after interrupt happened :** bit[0] = optical bit[1] = coaxial

Bit(s)	Mnemonic	Name	Description
			bit[2] = coaxial ARC
			bit[3] = 0 (reserved)
27:24		bitcell_deg	**Multi-input signals after deglitching**
			bit[0] = optical
			bit[1] = coaxial
			bit[2] = coaxial ARC
			bit[3] = 0 (reserved)
23:21		bitcell_raw	**Multi-input signals:**
			bit[2] = optical
			bit[1] = coaxial
			bit[0] = coaxial ARC
20		auto_thr_en	**This bit will turn on variable TIMEOUT auto threhsold value (upper bound) for different input sample rate.**
19		derr_new_reten	**Adding additional one decoding error when valid decoding interval (data bit field 0~28) shows the invalid BMC (preamble 3N long pulse); Enable this bit will restart INTDIR without bothering RISC when set to 1.**
18		derr_new_det_en	**Adding additional one decoding error when valid decoding interval (data bit field 0~28) shows the invalid BMC (preamble 3N long pulse); Enable this bit will give a interrupt to RISC when set to 1.**
17		dataLatchError_det_en	**When machine inner status error such as bitclk polarity error by instant abnormal input after INTDIR locking, the detection flag will give a interrutpt to RISC when this bit set to 1.**
15:14		input_sel	**Multi-input selection :**
			2'b00 : optical input
			2'b01 : coaxial input
			2'b10 : coaxial ARC input
			2'b11 : tied low
11:8		edge_det_en	**Multi-input edge detection enable :**
			4"b0001 : optical input
			4'b0010 : coaxial input

Bit(s)	Mnemonic	Name	Description
			4'b0100 : coaxial ARC input 4'b1000 and others : reserved for none
7:0		edge_cnt	**Multi-input edge detection valid window size :** programmable 8bit edge transition window, for example, default number 8 means valid consecutive 0->1 or 1->0 transitions happen 8 times; whenever the number of transition meet the edge_cnt, the edge detector will be active to interrupt the RISC.

1122054C AFE_SPDIFIN_INT_EXT2 00000174

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rough_freq				lrck_change_int										Mode_594M	Mode_432M
Type	RO				RO										RW	RW
Reset	0	0	0	0	0										0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lrc_change_int_en	lrc_compare														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	1	0	1	1	1	0	1	0	0

Bit(s)	Mnemonic	Name	Description
31:28		rough_freq	**The rough frequency index :** 4'd0 : NOT defined. 4'd1 : 32K. 4'd2 : 44.1K. 4'd3 : 48K. 4'd4 : 64K. 4'd5 : 88.2K. 4'd6 : 96K. 4'd7 : 128K. 4'd8 : 144K. 4'd9 : 176.4K.

Bit(s)	Mnemonic	Name	Description
			4'd10 : 192K. 4'd11 : 216K (experiment)
27		lrck_change_int	**The interrupt flag which is active whenever the lrck changed threshold by lrc_compare.**
17		Mode_594M	**The rough frequency detection bit in sys_clk = 594MHZ mode** 0 : disabled 1 : enable
16		Mode_432M	**The rough frequency detection bit in sys_clk = 432MHZ mode** 0 : disabled 1 : enable
15		lrc_change_int_en	**The interrupt enable bit for lrck change :** 0 : disabled 1 : enable
14:0		lrc_compare	**The interrupt threshold tolerance range counted by spdifin sys_clk (594M/432M). The default value is calculated by range between 48K*(1-3%) ~48K*(1+3%) by sys_clk 594MHZ.**

11220550 SPDIFIN_FREQ_INFO SPDIFIN rough frequency detection information setup 0080F910

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									m594m_2x144kfs							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	m594m_2x144kfs				m594m_2x128kfs											
Type	RW				RW											
Reset	1	1	1	1	1	0	0	1	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:12		m594m_2x144kfs	**The rough frequency detection information setup bit in 594MHZ mode counted by** 594M/(2*144K) = 2063

Bit(s)	Mnemonic	Name	Description
11:0		m594m_2x128kfs	**The rough frequency detection information setup bit in 594MHZ mode counted by** 594M/(2*128K) = 2320

11220554 SPDIFIN_FREQ_INFO_2 SPDIFIN rough frequency detection information setup2 0060B694

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									m594m_2x192kfs							
Type									RW							
Reset									0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	m594m_2x192kfs				m594m_2x176kfs											
Type	RW				RW											
Reset	1	0	1	1	0	1	1	0	1	0	0	1	0	1	0	0

Bit(s)	Mnemonic	Name	Description
23:12		m594m_2x192kfs	**The rough frequency detection information setup bit in 594MHZ mode counted by** 594M/(2*192K) = 1547
11:0		m594m_2x176kfs	**The rough frequency detection information setup bit in 594MHZ mode counted by** 594M/(2*176K) = 1684

11220558 SPDIFIN_FREQ_INFO_3 SPDIFIN rough frequency detection information setup 3 0000055F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					m594m_2x216kfs											
Type					RW											
Reset					0	1	0	1	0	1	0	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
11:0		m594m_2x216kfs	**The rough frequency detection information setup bit in 594MHZ mode counted by** 594M/(2*216K) = 1375

1122055C SPDIFIN_FREQ_STATUS SPDIFIN rough frequency detection status 0000FF18

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Rough_freq_preview_idx							MAXBLENCNTMEM								
Type	RO							RO								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MINBLENCNTMEM								AVBLENCNTMEM							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	0	0	0	1	1	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		Rough_freq_preview_idx	**The rough frequency preview index :** 4'd0 : NOT defined. 4'd1 : 32K. 4'd2 : 44.1K. 4'd3 : 48K. 4'd4 : 64K. 4'd5 : 88.2K. 4'd6 : 96K. 4'd7 : 128K. 4'd8 : 144K. 4'd9 : 176.4K. 4'd10 : 192K. 4'd11 : 216K (experiment)
24:16		MAXBLENCNTMEM	**The maximum input length counter by 594MHZ. 0 default value represnets the initial stage (not training completed yet)**

Bit(s)	Mnemonic	Name	Description
15:8		MINBLENCNTMEM	**The minimum input length counter by 594MHZ. 255 default value represnets the initial stage (not training completed yet)**
7:0		AVBLENCNTMEM	**The average input length counter by 594MHZ in default.**

11220560 SPDIFIN_USERCODE1 SPDIFIN Usercode 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	userCode															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	userCode															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		userCode	**Re-build usercode[31:0]**

11220564 SPDIFIN_USERCODE2 SPDIFIN Usercode 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	userCode															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	userCode															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		userCode	**Re-build usercode[63:32]**

11220568 SPDIFIN_USERCODE3 SPDIFIN Usercode 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	userCode															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**userCode**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		userCode	**Re-build usercode[95:64]**

1122056C SPDIFIN_USERCODE4 SPDIFIN Usercode 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**userCode**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**userCode**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		userCode	**Re-build usercode[127:96]**

11220570 SPDIFIN_USERCODE5 SPDIFIN Usercode 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**userCode**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**userCode**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		userCode	**Re-build usercode[159:128]**

11220574 SPDIFIN_USERCODE6 SPDIFIN Usercode 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	userCode															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	userCode															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		userCode	**Re-build usercode[191:160]**

11220578 SPDIFIN_USERCODE7 SPDIFIN Usercode 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	userCode															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	userCode															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		userCode	**Re-build usercode[223:192]**

1122057C SPDIFIN_USERCODE8 SPDIFIN Usercode 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	userCode															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	userCode															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		userCode	**Re-build usercode[255:224]**

11220580 SPDIFIN_USERCODE9 SPDIFIN Usercode 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**userCode**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**userCode**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		userCode	**Re-build usercode[287:256]**

11220584 SPDIFIN_USERCODE10 SPDIFIN Usercode 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**userCode**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**userCode**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		userCode	**Re-build usercode[319:288]**

11220588 SPDIFIN_USERCODE11 SPDIFIN Usercode 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**userCode**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	userCode															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		userCode	**Re-build usercode[351:320]**

1122058C SPDIFIN_USERCODE12 SPDIFIN Usercode 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	userCode															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	userCode															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		userCode	**Re-build usercode[383:352]**

11220590 AFE_HADDS2_CON HADDS2 PCW 073126EA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pcw_ncpo_chg	pcw														
Type	RW	RW														
Reset	0	0	0	0	0	1	1	1	0	0	1	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcw															
Type	RW															
Reset	0	0	1	0	0	1	1	0	1	1	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
31		pcw_ncpo_chg	
30:0		pcw	

11220594 AFE_SPDIFIN_APLL_TUNER_CFG SPDIFIN APLL tuner config 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			spdifin_apll_freq_diff										spdifin_apll_freq_tuner_cfg			
Type			RO										RW			
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spdifin_apll_freq_tuner_cfg															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:20		spdifin_apll_freq_diff	
19:0		spdifin_apll_freq_tuner_cfg	[19:12] upper_bound [9:4] apll_div [0]freq_tuner_en

11220598 AFE_SPDIFIN_APLL_TUNER_CFG1 SPDIFIN APLL tuner config1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									spdifin_apll_freq_iec_div							spdifin_apll_tuner_sel
Type									RW							RW
Reset									0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
7:4		spdifin_apll_freq_iec_div	
0		spdifin_apll_tuner_sel	

112205F0 I2SIN_BCOUNT_MON I2S in bcount monitor 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	i2sin4_bcount								i2sin3_bcount							
Type	RU								RU							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	i2sin2_bcount								i2sin1_bcount							
Type	RU								RU							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:24		i2sin4_bcount	
23:16		i2sin3_bcount	
15:8		i2sin2_bcount	
7:0		i2sin1_bcount	

112205F4 I2SO_BCOUNT_MON I2S out bcount monitor 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	i2so4_bcount								i2so3_bcount							
Type	RU								RU							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	i2so2_bcount								i2so1_bcount							
Type	RU								RU							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:24		i2so4_bcount	
23:16		i2so3_bcount	
15:8		i2so2_bcount	
7:0		i2so1_bcount	

112205F8 I2S_UNUSED_BCOUNT_MON I2S 5,6 bcount monitor 01010101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11220600 ASYS_TOP_CON PCM Interface Config 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**i2s2_dsd_use_sony_ip**	**i2s1_dsd_use_sony_ip**	**dl1_bypass_conn**	**A2SYS_TIMING_ON**	**A1SYS_TIMING_ON**
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		i2s2_dsd_use_sony_ip	**i2s2 dsd out use sony ip** 0: normal dsd out 1: sony ip dsd out
3		i2s1_dsd_use_sony_ip	**i2s1 dsd out use sony ip** 0: normal dsd out 1: sony ip dsd out
2		dl1_bypass_conn	**dl1_bypass connector** 0: normal 1: byps

Bit(s)	Mnemonic	Name	Description
1		A2SYS_TIMING_ON	**enable this bit will genrate 44.1k domain timing signals** 0: disable timing 1: enable timing
0		A1SYS_TIMING_ON	**enable this bit will genrate 44.1k domain timing signals** 0: disable timing 1: enable timing

11220604 ASYS_I2SIN1_CON I2S in1 Control Register 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	phase_shift_fix	i2s_soft_reset				in_ws_inverse			I2Sin1_fpga_test_loop_bit		I2Sin1_fpga_test_loop_bit1	I2Sin1_fpga_test_loop_bit2	i2s_in_asrc_select	dsd_mode	I2S_couple_mode	
Type	RW	RW				RW			RW		RW	RW	RW	RW	RW	
Reset	0	0				0			0		0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	low_fill_zero	right_adjust	valid_24_16	I2S_mode_sel							I2S_ws_invert		I2S_FMT	I2S_slave_mode_sel	I2S_WLEN	I2S_enable
Type	RW	RW	RW	RW							RW		RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		phase_shift_fix	
30		i2s_soft_reset	**i2s in soft reset** 0: disable 1: enable
26		in_ws_inverse	
23		I2Sin1_fpga_test_loop_bit	**i2s in1 wst from i2s out1 ws** 0: disable

Bit(s)	Mnemonic	Name	Description
			1: enable
21		I2Sin1_fpga_test_loop_bit1	**i2s in1 s_dat from i2s out1 s_dat** 0: disable 1: enable
20		I2Sin1_fpga_test_loop_bit2	**2is in1 s_dat/lrck/bck from out2 s_dat/lrck/bck** 0: disable 1: enable
19		i2s_in_asrc_select	
18		dsd_mode	
17		I2S_couple_mode	**i2s in couple mode** share same timing 0: self timing 1: use i2s out timing
15		low_fill_zero	**when lrck 32 cycle number and the 24/16 bit valid,the low 16/24bit is zero** 0:high bit fill zero(32) 1:low bit fill zero(32)
14		right_adjust	**when I2S_FMT = 0, the bit=1, right adjust;** when I2S_FMT = 0, the bit=0, left adjust; 0:left adjust 1:Right adjust
13		valid_24_16	**when I2S_WLEN =1, the valid data is 24bit or 16bit** 0:input 16bit mode 1:input 24bit mode
12:8		I2S_mode_sel	**i2s in timing mode select** 5'b00000: 8k 5'b00001: 12k

Bit(s)	Mnemonic	Name	Description
			5'b00010: 16k
			5'b00011: 24k
			5'b00100: 32k
			5'b00101: 48k
			5'b00110: 96k
			5'b00111: 192k
			5'b01000: 384k
			5'b10000: 7.25k
			5'b10001: 11.025k
			5'b10010: 14.7k
			5'b10011: 22.05k
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4k
			5'b11000: 352.8k
5		I2S_ws_invert	
3		I2S_FMT	**EIAJ: right adjust**
			0: EIAJ
			1: I2S
2		I2S_slave_mode_sel	**master slave mode control**
			0: master mode
			1: slave mode
1		I2S_WLEN	**Controls the word length of I2S.**
			0: 16 bits
			1: 32 bits
0		I2S_enable	**Controls the I2S on.**
			0: disable

Bit(s)	Mnemonic	Name	Description
			1: enable

11220608 ASYS_I2SIN2_CON I2S in2 Control Register 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	phase_shift_fix	i2s_soft_reset				in_ws_inverse			I2Sin2_fpga_test_loop_bit		I2Sin2_fpga_test_loop_bit1	I2Sin2_fpga_test_loop_bit2	i2s_in_asrc_select	dsd_mode	I2S_couple_mode	
Type	RW	RW				RW			RW		RW	RW	RW	RW	RW	
Reset	0	0				0			0		0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	low_fill_zero	right_adjust	valid_24_16	I2S_mode_sel							I2S_ws_invert		I2S_FMT	I2S_slave_mode_sel	I2S_WLEN	I2S_enable
Type	RW	RW	RW	RW							RW		RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		phase_shift_fix	
30		i2s_soft_reset	**i2s in soft reset**
			0: disable
			1: enable
26		in_ws_inverse	
23		I2Sin2_fpga_test_loop_bit	**i2s2 in wst from i2s out2 ws**
			0: disable
			1: enable
21		I2Sin2_fpga_test_loop_bit1	**i2s in2 s_dat from i2s out2 s_dat**
			0: disable
			1: enable
20		I2Sin2_fpga_test_loop_bit2	**2is in2 s_dat/lrck/bck from out3 s_dat/lrck/bck**

Bit(s)	Mnemonic	Name	Description
			0: disable
			1: enable
19		i2s_in_asrc_select	
18		dsd_mode	
17		I2S_couple_mode	**i2s in couple mode**
			share same timing
			0: self timing
			1: use i2s out timing
15		low_fill_zero	**when lrck 32 cycle number and the 24/16 bit valid,the low 16/24bit is zero**
			0:high bit fill zero(32)
			1:low bit fill zero(32)
14		right_adjust	**when I2S_FMT = 0, the bit=1, right adjust;**
			when I2S_FMT = 0, the bit=0, left adjust;
			0:left adjust
			1:Right adjust
13		valid_24_16	**when I2S_WLEN =1, the valid data is 24bit or 16bit**
			0:input 16bit mode
			1:input 24bit mode
12:8		I2S_mode_sel	**i2s in timing mode select**
			5'b00000: 8k
			5'b00001: 12k
			5'b00010: 16k
			5'b00011: 24k
			5'b00100: 32k
			5'b00101: 48k
			5'b00110: 96k
			5'b00111: 192k

Bit(s)	Mnemonic	Name	Description
			5'b01000: 384k 5'b10000: 7.25k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4k 5'b11000: 352.8k
5		I2S_ws_invert	
3		I2S_FMT	**EIAJ: right adjust** 0: EIAJ 1: I2S
2		I2S_slave_mode_sel	**master slave mode control** 0: master mode 1: slave mode
1		I2S_WLEN	**Controls the word length of I2S.** 0: 16 bits 1: 32 bits
0		I2S_enable	**Controls the I2S on.** 0: disable 1: enable

1122060C ASYS_I2SIN3_CON I2S in3 Control Register 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	phase_shift_fix	i2s_soft_reset				in_ws_inverse			I2Sin3_fpga_test		I2Sin3_fpga_test	I2Sin3_fpga_test	i2s_in_asr	dsd_mode	I2S_couple	

									_loop_bit		_loop_bit1	_loop_bit2	c_select		_mode	
Type	RW	RW				RW			RW		RW	RW	RW	RW	RW	
Reset	0	0				0			0		0	0	0	0	0	

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**low_fill_zero**	**right_adjust**	**valid_24_16**	**I2S_mode_sel**							**I2S_ws_invert**		**I2S_FMT**	**I2S_slave_mode_sel**	**I2S_WLEN**	**I2S_enable**
Type	RW	RW	RW	RW							RW		RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0			0		0	0	0	0

Bit(s)	**Mnemonic**	**Name**	**Description**
31		phase_shift_fix	
30		i2s_soft_reset	**i2s in soft reset** 0: disable 1: enable
26		in_ws_inverse	
23		I2Sin3_fpga_test_loop_bit	**i2s3 in wst from i2s out3 ws** 0: disable 1: enable
21		I2Sin3_fpga_test_loop_bit1	**i2s in3 s_dat from i2s out3 s_dat** 0: disable 1: enable
20		I2Sin3_fpga_test_loop_bit2	**2is in3 s_dat/lrck/bck from out4 s_dat/lrck/bck** 0: disable 1: enable
19		i2s_in_asrc_select	
18		dsd_mode	
17		I2S_couple_mode	**i2s in couple mode** share same timing 0: self timing

Bit(s)	Mnemonic	Name	Description
			1: use i2s out timing
15		low_fill_zero	**when lrck 32 cycle number and the 24/16 bit valid,the low 16/24bit is zero** 0:high bit fill zero(32) 1:low bit fill zero(32)
14		right_adjust	**when I2S_FMT = 0, the bit=1, right adjust;** when I2S_FMT = 0, the bit=0, left adjust; 0:left adjust 1:Right adjust
13		valid_24_16	**when I2S_WLEN =1, the valid data is 24bit or 16bit** 0:input 16bit mode 1:input 24bit mode
12:8		I2S_mode_sel	**i2s in timing mode select** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192k 5'b01000: 384k 5'b10000: 7.25k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k

Bit(s)	Mnemonic	Name	Description
			5'b10110: 88.2k
			5'b10111: 176.4k
			5'b11000: 352.8k
5		I2S_ws_invert	
3		I2S_FMT	**EIAJ: right adjust**
			0: EIAJ
			1: I2S
2		I2S_slave_mode_sel	**master slave mode control**
			0: master mode
			1: slave mode
1		I2S_WLEN	**Controls the word length of I2S.**
			0: 16 bits
			1: 32 bits
0		I2S_enable	**Controls the I2S on.**
			0: disable
			1: enable

11220610 ASYS_I2SIN4_CON I2S in4 Control Register 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	phase_shift_fix	i2s_soft_reset				in_ws_inverse			I2Sin4_fpga_test_loop_bit		I2Sin4_fpga_test_loop_bit1	I2Sin4_fpga_test_loop_bit2	i2s_in_asrc_select	dsd_mode	I2S_couple_mode	
Type	RW	RW				RW			RW		RW	RW	RW	RW	RW	
Reset	0	0				0			0		0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	low_fili_zero	right_adjust	valid24_16	I2S_mode_sel							I2S_ws_invert		I2S_FMT	I2S_slave_mode_sel	I2S_WLEN	I2S_enable
Type	RW	RW	RW	RW							RW		RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		phase_shift_fix	
30		i2s_soft_reset	**i2s in soft reset** 0: disable 1: enable
26		in_ws_inverse	
23		I2Sin4_fpga_test_loop_bit	**i2s4 in wst from i2s out4 ws** 0: disable 1: enable
21		I2Sin4_fpga_test_loop_bit1	**i2s in4 s_dat from i2s out4 s_dat** 0: disable 1: enable
20		I2Sin4_fpga_test_loop_bit2	**2is in4 s_dat/lrck/bck from out5 s_dat/lrck/bck** 0: disable 1: enable
19		i2s_in_asrc_select	
18		dsd_mode	
17		I2S_couple_mode	**i2s in couple mode** share same timing 0: self timing 1: use i2s out timing
15		low_fill_zero	**when lrck 32 cycle number and the 24/16 bit valid,the low 16/24bit is zero** 0:high bit fill zero(32) 1:low bit fill zero(32)
14		right_adjust	**when I2S_FMT = 0, the bit=1, right adjust;** when I2S_FMT = 0, the bit=0, left adjust; 0:left adjust

Bit(s)	Mnemonic	Name	Description
			1:Right adjust
13		valid_24_16	**when I2S_WLEN =1, the valid data is 24bit or 16bit** 0:input 16bit mode 1:input 24bit mode
12:8		I2S_mode_sel	**i2s in timing mode select** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192k 5'b01000: 384k 5'b10000: 7.25k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4k 5'b11000: 352.8k
5		I2S_ws_invert	
3		I2S_FMT	**EIAJ: right adjust** 0: EIAJ 1: I2S

Bit(s)	Mnemonic	Name	Description
2		I2S_slave_mode_sel	**master slave mode control** 0: master mode 1: slave mode
1		I2S_WLEN	**Controls the word length of I2S.** 0: 16 bits 1: 32 bits
0		I2S_enable	**Controls the I2S on.** 0: disable 1: enable

11220614 ASYS_I2SIN5_CON I2S in5 Control Register 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	phase_shift_fix	i2s_soft_reset				in_ws_inverse			I2Sin5_fpga_test_loop_bit		I2Sin1_fpga_test_loop_bit1	I2Sin1_fpga_test_loop_bit2	i2s_in_asrc_select	dsd_mode	I2S_couple_mode	
Type	RW	RW				RW			RW		RW	RW	RW	RW	RW	
Reset	0	0				0			0		0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	low_fill_zero	right_adjust	valid_24_16	I2S_mode_sel							I2S_ws_invert		I2S_FMT	I2S_slave_mode_sel	I2S_WLEN	I2S_enable
Type	RW	RW	RW	RW							RW		RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		phase_shift_fix	
30		i2s_soft_reset	**i2s in soft reset** 0: disable 1: enable
26		in_ws_inverse	

Bit(s)	Mnemonic	Name	Description
23		I2Sin5_fpga_test_loop_bit	**i2s5 in wst from i2s out5 ws** 0: disable 1: enable
21		I2Sin1_fpga_test_loop_bit1	**i2s in5 s_dat from i2s out5 s_dat** 0: disable 1: enable
20		I2Sin1_fpga_test_loop_bit2	**2is in5 s_dat/lrck/bck from out6 s_dat/lrck/bck** 0: disable 1: enable
19		i2s_in_asrc_select	
18		dsd_mode	
17		I2S_couple_mode	**i2s in couple mode** share same timing 0: self timing 1: use i2s out timing
15		low_fill_zero	**when lrck 32 cycle number and the 24/16 bit valid,the low 16/24bit is zero** 0:high bit fill zero(32) 1:low bit fill zero(32)
14		right_adjust	**when I2S_FMT = 0, the bit=1, right adjust;** when I2S_FMT = 0, the bit=0, left adjust; 0:left adjust 1:Right adjust
13		valid_24_16	**when I2S_WLEN =1, the valid data is 24bit or 16bit** 0:input 16bit mode 1:input 24bit mode
12:8		I2S_mode_sel	**i2s in timing mode select**

Bit(s)	Mnemonic	Name	Description
			5'b00000: 8k
			5'b00001: 12k
			5'b00010: 16k
			5'b00011: 24k
			5'b00100: 32k
			5'b00101: 48k
			5'b00110: 96k
			5'b00111: 192k
			5'b01000: 384k
			5'b10000: 7.25k
			5'b10001: 11.025k
			5'b10010: 14.7k
			5'b10011: 22.05k
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4k
			5'b11000: 352.8k
5		I2S_ws_invert	
3		I2S_FMT	**EIAJ: right adjust**
			0: EIAJ
			1: I2S
2		I2S_slave_mode_sel	**master slave mode control**
			0: master mode
			1: slave mode
1		I2S_WLEN	**Controls the word length of I2S.**
			0: 16 bits
			1: 32 bits

Bit(s)	Mnemonic	Name	Description
0		I2S_enable	**Controls the I2S on.** 0: disable 1: enable

11220618 ASYS_I2SIN6_CON I2S in6 Control Register 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	phase_shift_fix	i2s_soft_reset				in_ws_inverse			I2Sin6_fpga_test_loop_bit		I2Sin1_fpga_test_loop_bit1	I2Sin1_fpga_test_loop_bit2	i2s_in_asrc_select	dsd_mode	I2S_couple_mode	
Type	RW	RW				RW			RW		RW	RW	RW	RW	RW	
Reset	0	0				0			0		0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	low_fill_zero	right_adjust	valid_24_16	I2S_mode_sel							I2S_ws_invert		I2S_FMT	I2S_slave_mode_sel	I2S_WLEN	I2S_enable
Type	RW	RW	RW	RW							RW		RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		phase_shift_fix	
30		i2s_soft_reset	**i2s in soft reset** 0: disable 1: enable
26		in_ws_inverse	
23		I2Sin6_fpga_test_loop_bit	**i2s6 in wst from i2s out6 ws** 0: disable 1: enable
21		I2Sin1_fpga_test_loop_bit1	**i2s in6 s_dat from i2s out6 s_dat** 0: disable

Bit(s)	Mnemonic	Name	Description
			1: enable
20		I2Sin1_fpga_test_loop_bit2	**2is in6 s_dat/lrck/bck from out1 s_dat/lrck/bck** 0: disable 1: enable
19		i2s_in_asrc_select	
18		dsd_mode	
17		I2S_couple_mode	**i2s in couple mode** share same timing 0: self timing 1: use i2s out timing
15		low_fill_zero	**when lrck 32 cycle number and the 24/16 bit valid,the low 16/24bit is zero** 0:high bit fill zero(32) 1:low bit fill zero(32)
14		right_adjust	**when I2S_FMT = 0, the bit=1, right adjust;** when I2S_FMT = 0, the bit=0, left adjust; 0:left adjust 1:Right adjust
13		valid_24_16	**when I2S_WLEN =1, the valid data is 24bit or 16bit** 0:input 16bit mode 1:input 24bit mode
12:8		I2S_mode_sel	**i2s in timing mode select** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k

Bit(s)	Mnemonic	Name	Description
			5'b00110: 96k
			5'b00111: 192k
			5'b01000: 384k
			5'b10000: 7.25k
			5'b10001: 11.025k
			5'b10010: 14.7k
			5'b10011: 22.05k
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4k
			5'b11000: 352.8k
5		I2S_ws_invert	
3		I2S_FMT	**EIAJ: right adjust**
			0: EIAJ
			1: I2S
2		I2S_slave_mode_sel	**master slave mode control**
			0: master mode
			1: slave mode
1		I2S_WLEN	**Controls the word length of I2S.**
			0: 16 bits
			1: 32 bits
0		I2S_enable	**Controls the I2S on.**
			0: disable
			1: enable

1122061C ASYS_I2SO1_CON I2S out1 Control Register 00020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	i2s_lr_swap	i2s_soft_reset					I2S_data_from_sine_select1				I2S_fpga_test_loop_bit			dsd_mode	i2s_in_out_couple_mode	i2s_out_one_heart
Type	RW	RW					RW				RW			RW	RW	RW
Reset	0	0					0				0			0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		right_adjust	valid_24_16	I2S_mode_sel							I2S_ws_invert		I2S_FMT	I2S_slave_mode_sel	I2S_WLEN	I2S_enable
Type		RW	RW	RW							RW		RW	RW	RW	RW
Reset		0	0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		i2s_lr_swap	**Swap l/r channel data** 0 : not swap l/r channel
30		i2s_soft_reset	**i2s out soft reset** 0: disable 1: enable
25		I2S_data_from_sine_select1	**I2S p_data from sine select:** l_ch from sine_ch1; r_ch from sine_ch2 0: Disable 1: Enable
21		I2S_fpga_test_loop_bit	**i2s out1 lrck/bck from i2s out2** 0: disable 1: enable
18		dsd_mode	
17		i2s_in_out_couple_mode	
16		i2s_out_one_heart	
14		right_adjust	**when I2S_FMT = 0, the bit=1, right adjust;** when I2S_FMT = 0, the bit=0, left adjust;

Bit(s)	Mnemonic	Name	Description
			0:left adjust
			1:Right adjust
13		valid_24_16	**when I2S_WLEN =1, the valid data is 24bit or 16bit**
			0:input 16bit mode
			1:input 24bit mode
12:8		I2S_mode_sel	**i2s in timing mode select**
			5'b00000: 8k
			5'b00001: 12k
			5'b00010: 16k
			5'b00011: 24k
			5'b00100: 32k
			5'b00101: 48k
			5'b00110: 96k
			5'b00111: 192k
			5'b01000: 384k
			5'b10000: 7.25k
			5'b10001: 11.025k
			5'b10010: 14.7k
			5'b10011: 22.05k
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4k
			5'b11000: 352.8k
5		I2S_ws_invert	
3		I2S_FMT	
2		I2S_slave_mode_sel	**master slave mode control**

Bit(s)	Mnemonic	Name	Description
			0: master mode
			1: slave mode
1		I2S_WLEN	**Controls the word length of I2S.**
			0: 16 bits
			1: 32 bits
0		I2S_enable	**Controls the I2S on.**
			0: disable
			1: enable

11220620 ASYS_I2SO2_CON I2S out2 Control Register 00020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	i2s_lr_swap	i2s_soft_reset					I2S_data_from_sine_select1				I2S_fpga_test_loop_bit			dsd_mode	i2s_in_out_couple_mode	i2s_out_one_heart
Type	RW	RW					RW				RW			RW	RW	RW
Reset	0	0					0				0			0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		right_adjust	valid_24_16	I2S_mode_sel							I2S_ws_invert		I2S_FMT	I2S_slave_mode_sel	I2S_WLEN	I2S_enable
Type		RW	RW	RW							RW		RW	RW	RW	RW
Reset		0	0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		i2s_lr_swap	**Swap l/r channel data**
			0 : not swap l/r channel
30		i2s_soft_reset	**i2s out soft reset**
			0: disable
			1: enable

Bit(s)	Mnemonic	Name	Description
25		I2S_data_from_sine_select1	**I2S p_data from sine select:** l_ch from sine_ch1; r_ch from sine_ch2 0: Disable 1: Enable
21		I2S_fpga_test_loop_bit	**i2s out2 lrck/bck from i2s out3** 0: disable 1: enable
18		dsd_mode	
17		i2s_in_out_couple_mode	
16		i2s_out_one_heart	
14		right_adjust	**when I2S_FMT = 0, the bit=1, right adjust;** when I2S_FMT = 0, the bit=0, left adjust; 0:left adjust 1:Right adjust
13		valid_24_16	**when I2S_WLEN =1, the valid data is 24bit or 16bit** 0:input 16bit mode 1:input 24bit mode
12:8		I2S_mode_sel	**i2s in timing mode select** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192k

Bit(s)	Mnemonic	Name	Description
			5'b01000: 384k 5'b10000: 7.25k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4k 5'b11000: 352.8k
5		I2S_ws_invert	
3		I2S_FMT	
2		I2S_slave_mode_sel	**master slave mode control** 0: master mode 1: slave mode
1		I2S_WLEN	**Controls the word length of I2S.** 0: 16 bits 1: 32 bits
0		I2S_enable	**Controls the I2S on.** 0: disable 1: enable

11220624 ASYS_I2SO3_CON I2S out3 Control Register 00020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	i2s_ir_swap	i2s_soft_reset					I2S_data_from_sine_select1				I2S_fpga_test_loop_bit			dsd_mode	i2s_in_out_couple_mode	i2s_out_one_heart
Type	RW	RW					RW				RW			RW	RW	RW

Reset	0	0					0				0			0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		right_adjust	valid_24_16	I2S_mode_sel							I2S_ws_invert		I2S_FMT	I2S_slave_mode_sel	I2S_WLEN	I2S_enable
Type		RW	RW	RW							RW		RW	RW	RW	RW
Reset		0	0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		i2s_lr_swap	**Swap l/r channel data** 0 : not swap l/r channel
30		i2s_soft_reset	**i2s out soft reset** 0: disable 1: enable
25		I2S_data_from_sine_select1	**I2S p_data from sine select:** l_ch from sine_ch1; r_ch from sine_ch2 0: Disable 1: Enable
21		I2S_fpga_test_loop_bit	**i2s out3 lrck/bck from i2s out4** 0: disable 1: enable
18		dsd_mode	
17		i2s_in_out_couple_mode	
16		i2s_out_one_heart	
14		right_adjust	**when I2S_FMT = 0, the bit=1, right adjust;** when I2S_FMT = 0, the bit=0, left adjust; 0:left adjust 1:Right adjust
13		valid_24_16	**when I2S_WLEN =1, the valid data is 24bit or 16bit**

Bit(s)	Mnemonic	Name	Description
			0:input 16bit mode
			1:input 24bit mode
12:8		I2S_mode_sel	**i2s in timing mode select**
			5'b00000: 8k
			5'b00001: 12k
			5'b00010: 16k
			5'b00011: 24k
			5'b00100: 32k
			5'b00101: 48k
			5'b00110: 96k
			5'b00111: 192k
			5'b01000: 384k
			5'b10000: 7.25k
			5'b10001: 11.025k
			5'b10010: 14.7k
			5'b10011: 22.05k
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4k
			5'b11000: 352.8k
5		I2S_ws_invert	
3		I2S_FMT	
2		I2S_slave_mode_sel	**master slave mode control**
			0: master mode
			1: slave mode
1		I2S_WLEN	**Controls the word length of I2S.**
			0: 16 bits

Bit(s)	Mnemonic	Name	Description
			1: 32 bits
0		I2S_enable	**Controls the I2S on.** 0: disable 1: enable

11220628 ASYS_I2SO4_CON I2S out4 Control Register 00020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	i2s_lr_swap	i2s_soft_reset					I2S_data_from_sine_select1				I2S_fpga_test_loop_bit			dsd_mode	i2s_in_out_couple_mode	i2s_out_one_heart
Type	RW	RW					RW				RW			RW	RW	RW
Reset	0	0					0				0			0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		right_adjust	valid_24_16	I2S_mode_sel							I2S_ws_invert		I2S_FMT	I2S_slave_mode_sel	I2S_WLEN	I2S_enable
Type		RW	RW	RW							RW		RW	RW	RW	RW
Reset		0	0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		i2s_lr_swap	**Swap l/r channel data** 0 : not swap l/r channel
30		i2s_soft_reset	**i2s out soft reset** 0: disable 1: enable
25		I2S_data_from_sine_select1	**I2S p_data from sine select:** l_ch from sine_ch1; r_ch from sine_ch2 0: Disable 1: Enable

Bit(s)	Mnemonic	Name	Description
21		I2S_fpga_test_loop_bit	**i2s out4 lrck/bck from i2s out5** 0: disable 1: enable
18		dsd_mode	
17		i2s_in_out_couple_mode	
16		i2s_out_one_heart	
14		right_adjust	**when I2S_FMT = 0, the bit=1, right adjust;** when I2S_FMT = 0, the bit=0, left adjust; 0:left adjust 1:Right adjust
13		valid_24_16	**when I2S_WLEN =1, the valid data is 24bit or 16bit** 0:input 16bit mode 1:input 24bit mode
12:8		I2S_mode_sel	**i2s in timing mode select** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192k 5'b01000: 384k 5'b10000: 7.25k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k

Bit(s)	Mnemonic	Name	Description
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4k
			5'b11000: 352.8k
5		I2S_ws_invert	
3		I2S_FMT	
2		I2S_slave_mode_sel	**master slave mode control**
			0: master mode
			1: slave mode
1		I2S_WLEN	**Controls the word length of I2S.**
			0: 16 bits
			1: 32 bits
0		I2S_enable	**Controls the I2S on.**
			0: disable
			1: enable

1122062C ASYS_I2SO5_CON I2S out5 Control Register 00020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	i2s_lr_swap	i2s_soft_reset					I2S_data_from_sine_select1				I2S_fpga_test_loop_bit			dsd_mode	i2s_in_out_couple_mode	i2s_out_one_heart
Type	RW	RW					RW				RW			RW	RW	RW
Reset	0	0					0				0			0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		right_adjust	valid_24_16	I2S_mode_sel							I2S_ws_invert		I2S_FMT	I2S_slave_mode_sel	I2S_WLEN	I2S_enable
Type		RW	RW	RW							RW		RW	RW	RW	RW

Reset		0	0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		i2s_lr_swap	**Swap l/r channel data** 0 : not swap l/r channel
30		i2s_soft_reset	**i2s out soft reset** 0: disable 1: enable
25		I2S_data_from_sine_select1	**I2S p_data from sine select:** l_ch from sine_ch1; r_ch from sine_ch2 0: Disable 1: Enable
21		I2S_fpga_test_loop_bit	**i2s out5 lrck/bck from i2s out6** 0: disable 1: enable
18		dsd_mode	
17		i2s_in_out_couple_mode	
16		i2s_out_one_heart	
14		right_adjust	**when I2S_FMT = 0, the bit=1, right adjust;** when I2S_FMT = 0, the bit=0, left adjust; 0:left adjust 1:Right adjust
13		valid_24_16	**when I2S_WLEN =1, the valid data is 24bit or 16bit** 0:input 16bit mode 1:input 24bit mode
12:8		I2S_mode_sel	**i2s in timing mode select** 5'b00000: 8k 5'b00001: 12k

Bit(s)	Mnemonic	Name	Description
			5'b00010: 16k
			5'b00011: 24k
			5'b00100: 32k
			5'b00101: 48k
			5'b00110: 96k
			5'b00111: 192k
			5'b01000: 384k
			5'b10000: 7.25k
			5'b10001: 11.025k
			5'b10010: 14.7k
			5'b10011: 22.05k
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4k
			5'b11000: 352.8k
5		I2S_ws_invert	
3		I2S_FMT	
2		I2S_slave_mode_sel	**master slave mode control**
			0: master mode
			1: slave mode
1		I2S_WLEN	**Controls the word length of I2S.**
			0: 16 bits
			1: 32 bits
0		I2S_enable	**Controls the I2S on.**
			0: disable
			1: enable

Bit(s)	Mnemonic	Name	Description

11220630 ASYS_I2SO6_CON I2S out6 Control Register 00020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	i2s_lr_swap	i2s_soft_reset					I2S_data_from_sine_select			I2SOUT6_share_timing_select	I2S_fpga_test_loop_bit			dsd_mode	i2s_in_out_couple_mode	i2s_out_one_heart
Type	RW	RW					RW			RW	RW			RW	RW	RW
Reset	0	0					0			0	0			0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		right_adjust	valid_24_16	I2S_mode_sel							I2S_ws_invert		I2S_FMT	I2S_slave_mode_sel	I2S_WLEN	I2S_enable
Type		RW	RW	RW							RW		RW	RW	RW	RW
Reset		0	0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		i2s_lr_swap	**Swap l/r channel data** 0 : not swap l/r channel
30		i2s_soft_reset	**i2s out soft reset** 0: disable 1: enable
25		I2S_data_from_sine_select	**I2S p_data from sine select:** l_ch from sine_ch1; r_ch from sine_ch2 0: Disable 1: Enable
22		I2SOUT6_share_timing_select	**i2s out6 lrck/bck to i2s out1/2/3/4/5;** i2s out6 lrck/bck to i2s in1/2/3/4/5 0: disable 1: enable

Bit(s)	Mnemonic	Name	Description
21		I2S_fpga_test_loop_bit	**i2s out6 lrck/bck from i2s out1** 0: disable 1: enable
18		dsd_mode	
17		i2s_in_out_couple_mode	
16		i2s_out_one_heart	
14		right_adjust	**when I2S_FMT = 0, the bit=1, right adjust;** when I2S_FMT = 0, the bit=0, left adjust; 0:left adjust 1:Right adjust
13		valid_24_16	**when I2S_WLEN =1, the valid data is 24bit or 16bit** 0:input 16bit mode 1:input 24bit mode
12:8		I2S_mode_sel	**i2s in timing mode select** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192k 5'b01000: 384k 5'b10000: 7.25k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k

Bit(s)	Mnemonic	Name	Description
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4k
			5'b11000: 352.8k
5		I2S_ws_invert	
3		I2S_FMT	
2		I2S_slave_mode_sel	**master slave mode control**
			0: master mode
			1: slave mode
1		I2S_WLEN	**Controls the word length of I2S.**
			0: 16 bits
			1: 32 bits
0		I2S_enable	**Controls the I2S on.**
			0: disable
			1: enable

11220634 PWR2_TOP_CON PWR2_TOP_CON 0001FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																pdn_asrc_brg
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_dsd_enc	pdn_mem_asrc5	pdn_mem_asrc4	pdn_mem_asrc3	pdn_mem_asrc2	pdn_mem_asrc1	pdn_asrco6	pdn_asrco5	pdn_asrco4	pdn_asrco3	pdn_asrci6	pdn_asrci5	pdn_asrci4	pdn_asrci3	pdn_dmic2	pdn_dmic1
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
16		pdn_asrc_brg	**power down dsd_enc clock** 0: normal 1: power down
15		pdn_dsd_enc	**power down dsd_enc clock** 0: normal 1: power down
14		pdn_mem_asrc5	**power down memory base asrc5** 0: normal 1: power down
13		pdn_mem_asrc4	**power down memory base asrc4** 0: normal 1: power down
12		pdn_mem_asrc3	**power down memory base asrc3** 0: normal 1: power down
11		pdn_mem_asrc2	**power down memory base asrc2** 0: normal 1: power down
10		pdn_mem_asrc1	**power down memory base asrc1** 0: normal 1: power down
9		pdn_asrco6	**power down out6 asrc** 0: normal 1: power down
8		pdn_asrco5	**power down out5 asrc** 0: normal 1: power down
7		pdn_asrco4	**power down out4 asrc**

Bit(s)	Mnemonic	Name	Description
			0: normal
			1: power down
6		pdn_asrco3	**power down out3 asrc**
			0: normal
			1: power down
5		pdn_asrci6	**power down in6 asrc**
			0: normal
			1: power down
4		pdn_asrci5	**power down in5 asrc**
			0: normal
			1: power down
3		pdn_asrci4	**power down in4 asrc**
			0: normal
			1: power down
2		pdn_asrci3	**power down in3 asrc**
			0: normal
			1: power down
1		pdn_dmic2	**power down digital mic 2**
			0: normal
			1: power down
0		pdn_dmic1	**power down digital mic 1**
			0: normal
			1: power down

1122063C PCM_INTF_CON1 PCM Interface Config 1 00000006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11220640 PCM_INTF_CON2 PCM Interface Config 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11220648 DSD1_FADER_CON0 dsd1 fader control 20000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			dsd1_fatt													
Type			RW													
Reset			1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fader_byps	bck_in_inv	mon_dsd2_sel	mon_rch_sel	ercpr h	en64	test	xzdflg msk	chmu te_r	chmu te_l	dsw			smute		
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Mnemonic	Name	Description
29:16		dsd1_fatt	**Attenuate Value 1.0 : 0x2000**
15		fader_byps	**bypass fader**
14		bck_in_inv	**input bck invert**

Bit(s)	Mnemonic	Name	Description
13		mon_dsd2_sel	**dsd2 fader mon select**
12		mon_rch_sel	**r channel mon select**
11		ercprh	**Error Clear Prohibit**
10		en64	**64FS cycle Enable sininal**
9		test	**Test mode**
8		xzdflgmsk	**Mute Data Detect flag Mask 0 Mask**
7		chmute_r	**channel r mute** 0: normal 1: mute
6		chmute_l	**channel l mute** 0: normal 1: mute
5:3		dsw	**Direct Switch** 0: org 1: mute 2: DS
2		smute	**soft mute** 0: normal 1: mute

1122064C DSD2_FADER_CON0 dsd2 fader control 20000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			dsd2_fatt													
Type			RW													
Reset			1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fader_bypsn_inv	bck_i		mon_rch_sel	ercpr h	en64	test	xzdflg msk	chmu te_r	chmu te_l	dsw			smute		
Type	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW			RW		
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Mnemonic	Name	Description
29:16		dsd2_fatt	**Attenuate Value 1.0 : 0x2000**
15		fader_byps	**bypass fader**
14		bck_in_inv	**input bck invert**
12		mon_rch_sel	**r channel mon select**
11		ercprh	**Error Clear Prohibit**
10		en64	**64FS cycle Enable sininal**
9		test	**Test mode**
8		xzdflgmsk	**Mute Data Detect flag Mask 0 Mask**
7		chmute_r	**channel r mute** 0: normal 1: mute
6		chmute_l	**channel l mute** 0: normal 1: mute
5:3		dsw	**Direct Switch** 0: org 1: mute 2: DS
2		smute	**soft mute** 0: normal 1: mute

11220650 DSD_FADER_MON dsd fader moniter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						zdflg	nsswm	volume_arrive								
Type						RO	RO	RO								
Reset						0	0	0								

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
26		zdflg	**mute data detect**
25		nsswm	**Switch moninoer** 0: Orignal data side 1: delta sigma side
24		volume_arrive	**arrive Attenuation level**

112206C0 AFE_CONN0 AFE Connection Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_Ooo_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_Ooo_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_Ooo_S	**Controls the path from {I31,...,I00} to Ooo,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

112206C4 AFE_CONN1 AFE Connection Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_Oo1_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	Ixx_O01_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O01_S	**Controls the path from {I31,...,I00} to O01,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

112206C8 AFE_CONN2 AFE Connection Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O02_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O02_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O02_S	**Controls the path from {I31,...,I00} to O02,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

112206CC AFE_CONN3 AFE Connection Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O03_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O03_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O03_S	**Controls the path from {I31,...,I00} to O03,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

112206D0 AFE_CONN4 AFE Connection Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O04_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O04_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O04_S	**Controls the path from {I31,...,I00} to O04,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

112206D4 AFE_CONN5 AFE Connection Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O05_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O05_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O05_S	**Controls the path from {I31,...,I00} to O05,**

Bit(s)	Mnemonic	Name	Description
			bit0 is I00, ... , bit31 is I31 0: Off 1: On

112206D8 AFE_CONN6 AFE Connection Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O06_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O06_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O06_S	**Controls the path from {I31,...,I00} to O06,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

112206DC AFE_CONN7 AFE Connection Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O07_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O07_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O07_S	**Controls the path from {I31,...,I00} to O07,** bit0 is I00, ... , bit31 is I31

Bit(s)	Mnemonic	Name	Description
			0: Off 1: On

112206E0 AFE_CONN8 AFE Connection Register 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O08_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O08_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O08_S	**Controls the path from {I31,...,I00} to O08,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

112206E4 AFE_CONN9 AFE Connection Register 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O09_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O09_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O09_S	**Controls the path from {I31,...,I00} to O09,** bit0 is I00, ... , bit31 is I31 0: Off

Bit(s)	Mnemonic	Name	Description
			1: On

112206E8 AFE_CONN10 AFE Connection Register 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O10_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O10_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O10_S	**Controls the path from {I31,...,I00} to O10,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

112206EC AFE_CONN11 AFE Connection Register 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O11_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O11_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O11_S	**Controls the path from {I31,...,I00} to O11,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

Bit(s)	Mnemonic	Name	Description

112206F0 AFE_CONN12 AFE Connection Register 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O12_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O12_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O12_S	**Controls the path from {I31,...,I00} to O12,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

112206F4 AFE_CONN13 AFE Connection Register 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O13_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O13_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O13_S	**Controls the path from {I31,...,I00} to O13,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

112206F8 AFE_CONN14 AFE Connection Register 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O14_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O14_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O14_S	**Controls the path from {I31,...,I00} to O14,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

112206FC AFE_CONN15 AFE Connection Register 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O15_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O15_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O15_S	**Controls the path from {I31,...,I00} to O15,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

11220700 AFE_CONN16 AFE Connection Register 16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	Ixx_O16_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O16_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O16_S	**Controls the path from {I31,...,I00} to O16,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

11220704 AFE_CONN17 AFE Connection Register 17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O17_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O17_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O17_S	**Controls the path from {I31,...,I00} to O17,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

11220708 AFE_CONN18 AFE Connection Register 18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O18_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O18_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O18_S	**Controls the path from {I31,...,I00} to O18,** bito is I00, ... , bit31 is I31 0: Off 1: On

1122070C AFE_CONN19 AFE Connection Register 19 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O19_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O19_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O19_S	**Controls the path from {I31,...,I00} to O19,** bito is I00, ... , bit31 is I31 0: Off 1: On

11220710 AFE_CONN20 AFE Connection Register 20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O20_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O20_S															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O20_S	**Controls the path from {I31,...,I00} to O20,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

11220714 AFE_CONN21 AFE Connection Register 21 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**Ixx_O21_S**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**Ixx_O21_S**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O21_S	**Controls the path from {I31,...,I00} to O21,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

11220718 AFE_CONN22 AFE Connection Register 22 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**Ixx_O22_S**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**Ixx_O22_S**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O22_S	**Controls the path from {I31,...,I00} to O22,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

1122071C AFE_CONN23 AFE Connection Register 23 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**Ixx_O23_S**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**Ixx_O23_S**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O23_S	**Controls the path from {I31,...,I00} to O23,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

11220720 AFE_CONN24 AFE Connection Register 24 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**Ixx_O24_S**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**Ixx_O24_S**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O24_S	**Controls the path from {I31,...,I00} to O24,**

Bit(s)	Mnemonic	Name	Description
			bit0 is I00, ... , bit31 is I31 0: Off 1: On

11220724 AFE_CONN25 AFE Connection Register 25 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O25_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O25_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O25_S	**Controls the path from {I31,...,I00} to O25,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

11220728 AFE_CONN26 AFE Connection Register 26 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O26_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O26_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O26_S	**Controls the path from {I31,...,I00} to O26,** bit0 is I00, ... , bit31 is I31

Bit(s)	Mnemonic	Name	Description
			0: Off 1: On

1122072C AFE_CONN27 AFE Connection Register 27 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O27_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O27_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O27_S	**Controls the path from {I31,...,I00} to O27,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

11220730 AFE_CONN28 AFE Connection Register 28 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O28_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O28_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O28_S	**Controls the path from {I31,...,I00} to O28,** bit0 is I00, ... , bit31 is I31 0: Off

Bit(s)	Mnemonic	Name	Description
			1: On

11220734 AFE_CONN29 AFE Connection Register 29 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O29_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O29_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O29_S	**Controls the path from {I31,...,I00} to O29,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

11220738 AFE_CONN30 AFE Connection Register 30 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O30_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O30_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O30_S	**Controls the path from {I31,...,I00} to O30,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

Bit(s)	Mnemonic	Name	Description

1122073C AFE_CONN31 AFE Connection Register 31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O31_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O31_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O31_S	**Controls the path from {I31,...,I00} to O31,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

11220740 AFE_CONN32 AFE Connection Register 32 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O32_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O32_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O32_S	**Controls the path from {I31,...,I00} to O32,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

11220744 AFE_CONN33 AFE Connection Register 33 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Ixx_O33_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O33_S															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Ixx_O33_S	**Controls the path from {I31,...,I00} to O33,** bit0 is I00, ... , bit31 is I31 0: Off 1: On

11220748 AFE_CONN34 AFE Connection Register 34 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OXX_R															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OXX_R															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		OXX_R	**Controls the enabling of right shift 1 bit from OXX,** Bit0 is O00 ,...,, Bit31 is O31 0: No shift 1: Right shift 1 bit

1122074C AFE_CONN35 AFE Connection Register 35 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	i26_pcm_rx_sel	o31_pcm_tx_sel	Ixx_O04_S_H						Ixx_O03_S_H						Ixx_O02_S_H	
Type	RW	RW	RW						RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O02_S_H				Ixx_O01_S_H				Ixx_O00_S_H							
Type	RW				RW				RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		i26_pcm_rx_sel	**I26 select pcm rx** 0: daibt 1: pcm rx
30		o31_pcm_tx_sel	**O31 select pcm tx** 0: daibt 1: pcm tx
29:24		Ixx_O04_S_H	**Controls the path from {I36,...,I32} to O04,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
23:18		Ixx_O03_S_H	**Controls the path from {I36,...,I32} to O03,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
17:12		Ixx_O02_S_H	**Controls the path from {I36,...,I32} to O02,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
11:6		Ixx_O01_S_H	**Controls the path from {I36,...,I32} to O01,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On

Bit(s)	Mnemonic	Name	Description
5:0		Ixx_O00_S_H	**Controls the path from {I36,...,I32} to O00,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On

11220750 AFE_CONN36 AFE Connection Register 36 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	O31_SGEN_EN	O3233_SGEN_EN	Ixx_O09_S_H						Ixx_O08_S_H						Ixx_O07_S_H	
Type	RW	RW	RW						RW						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O07_S_H				Ixx_O06_S_H						Ixx_O05_S_H					
Type	RW				RW						RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		O31_SGEN_EN	**O31 SGEN enable** 0: O31 1: SGEN
30		O3233_SGEN_EN	**O32/O33 SGEN enable** 0: O32/33 1: SGEN
29:24		Ixx_O09_S_H	**Controls the path from {I36,...,I32} to O09,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
23:18		Ixx_O08_S_H	**Controls the path from {I36,...,I32} to O08,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off

Bit(s)	Mnemonic	Name	Description
			1: On
17:12		Ixx_O07_S_H	**Controls the path from {I36,...,I32} to O07,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
11:6		Ixx_O06_S_H	**Controls the path from {I36,...,I32} to O06,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
5:0		Ixx_O05_S_H	**Controls the path from {I36,...,I32} to O05,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On

11220754 AFE_CONN37 AFE Connection Register 37 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			Ixx_O14_S_H						Ixx_O13_S_H						Ixx_O12_S_H	
Type			RW						RW						RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O12_S_H				Ixx_O11_S_H						Ixx_O10_S_H					
Type	RW				RW						RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:24		Ixx_O14_S_H	**Controls the path from {I36,...,I32} to O14,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
23:18		Ixx_O13_S_H	**Controls the path from {I36,...,I32} to O13,**

Bit(s)	Mnemonic	Name	Description
			bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
17:12		Ixx_O12_S_H	**Controls the path from {I36,...,I32} to O12,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
11:6		Ixx_O11_S_H	**Controls the path from {I36,...,I32} to O11,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
5:0		Ixx_O10_S_H	**Controls the path from {I36,...,I32} to O10,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On

11220758 AFE_CONN38 AFE Connection Register 38 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			Ixx_O19_S_H						Ixx_O18_S_H						Ixx_O17_S_H	
Type			RW						RW						RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O17_S_H				Ixx_O16_S_H						Ixx_O15_S_H					
Type	RW				RW						RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:24		Ixx_O19_S_H	**Controls the path from {I36,...,I32} to O19,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off

Bit(s)	Mnemonic	Name	Description
			1: On
23:18		Ixx_O18_S_H	**Controls the path from {I36,...,I32} to O18,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
17:12		Ixx_O17_S_H	**Controls the path from {I36,...,I32} to O17,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
11:6		Ixx_O16_S_H	**Controls the path from {I36,...,I32} to O16,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
5:0		Ixx_O15_S_H	**Controls the path from {I36,...,I32} to O15,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On

1122075C AFE_CONN39 AFE Connection Register 39 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			Ixx_O24_S_H						Ixx_O23_S_H						Ixx_O22_S_H	
Type			RW						RW						RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O22_S_H				Ixx_O21_S_H				Ixx_O20_S_H							
Type	RW				RW				RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:24		Ixx_O24_S_H	**Controls the path from {I36,...,I32} to O24,**

Bit(s)	Mnemonic	Name	Description
			bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
23:18		Ixx_O23_S_H	**Controls the path from {I36,...,I32} to O23,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
17:12		Ixx_O22_S_H	**Controls the path from {I36,...,I32} to O22,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
11:6		Ixx_O21_S_H	**Controls the path from {I36,...,I32} to O21,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
5:0		Ixx_O20_S_H	**Controls the path from {I36,...,I32} to O20,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On

11220760 AFE_CONN40 AFE Connection Register 40 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			Ixx_O29_S_H						Ixx_O28_S_H						Ixx_O27_S_H	
Type			RW						RW						RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O27_S_H				Ixx_O26_S_H						Ixx_O25_S_H					
Type	RW				RW						RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:24		Ixx_O29_S_H	**Controls the path from {I36,...,I32} to O29,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
23:18		Ixx_O28_S_H	**Controls the path from {I36,...,I32} to O28,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
17:12		Ixx_O27_S_H	**Controls the path from {I36,...,I32} to O27,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
11:6		Ixx_O26_S_H	**Controls the path from {I36,...,I32} to O26,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
5:0		Ixx_O25_S_H	**Controls the path from {I36,...,I32} to O25,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On

11220764 AFE_CONN41 AFE Connection Register 41 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			O33_24BIT_SEL	O32_24BIT_SEL	O33_16BIT_SEL	O32_16BIT_SEL	O33_R	O32_R	Ixx_O33_S_H						Ixx_O32_S_H	
Type			RW	RW	RW	RW	RW	RW	RW						RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Ixx_O32_S_H				Ixx_O31_S_H						Ixx_O30_S_H					
Type	RW				RW						RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29		O33_24BIT_SEL	**Controls output data format of O33,** 0: 32-bit 1: 24-bit
28		O32_24BIT_SEL	**Controls output data format of O32,** 0: 32-bit 1: 24-bit
27		O33_16BIT_SEL	**Controls output data format of O33,** 0: 32-bit 1: 16-bit
26		O32_16BIT_SEL	**Controls output data format of O32,** 0: 32-bit 1: 16-bit
25		O33_R	**Controls the enabling of right shift 1 bit from O33** 0: No shift 1: Right shift 1 bit
24		O32_R	**Controls the enabling of right shift 1 bit from O32** 0: No shift 1: Right shift 1 bit
23:18		Ixx_O33_S_H	**Controls the path from {I36,...,I32} to O33,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
17:12		Ixx_O32_S_H	**Controls the path from {I36,...,I32} to O32,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
11:6		Ixx_O31_S_H	**Controls the path from {I36,...,I32} to O31,**

Bit(s)	Mnemonic	Name	Description
			bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On
5:0		Ixx_O30_S_H	**Controls the path from {I36,...,I32} to O30,** bit0 is I32, ... , bit4 is I36, bit5 reserved 0: Off 1: On

11220768 AFE_CONN_24BIT AFE CONNECTION 24BIT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OXX_24BIT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OXX_24BIT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		OXX_24BIT	**Controls output data 24bit format of OXX,** Bit0 is O00 ,..., Bit31 is O31 0: 32-bit 1: 24-bit

1122076C AFE_CONN_16BIT AFE CONNECTION 16BIT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OXX_16BIT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OXX_16BIT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		OXX_16BIT	**Controls output data 16bit format of OXX,** Bit0 is O00 ,..., Bit31 is O31 0: 32-bit 1: 16-bit

1122077C ASYS_IRQ_CONFIG IRQ MON sel 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**asys_irq_mon**			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		asys_irq_mon	**information with: read from ASYS_IRQ_MON2** irq_miss_flag irq_blk irq_cnt[23:0] 4'h0: irq1 info 4'h1: irq2 info 4'h2: irq3 info 4'h3: irq4 info 4'h4: irq5 info 4'h5: irq6 info 4'h6: irq7 info 4'h7: irq8 info 4'h8: irq9 info 4'h9: irq10 info

Bit(s)	Mnemonic	Name	Description
			4'ha: irq11 info
			4'hb: irq12 info
			4'hc: irq13 info
			4'hd: irq14 info
			4'he: irq15 info
			4'hf: irq16 info

11220780 ASYS_IRQ1_CON ASYS IRQ1 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							
Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal**
			0: irq disable
			1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag**
			0: pingpang mode
			1: normal mode
28:24		asys_irq_mode	**irq count frequency mode**
			5'b00000: 8k
			5'b00001: 12k
			5'b00010: 16k
			5'b00011: 24k

Bit(s)	Mnemonic	Name	Description
			5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2so1_1x_en 5'b01010: ext_i2so2_1x_en 5'b01011: ext_i2so3_1x_en 5'b01100: ext_i2so4_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

11220784 ASYS_IRQ2_CON ASYS IRQ2 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							

Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal** 0: irq disable 1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag** 0: pingpang mode 1: normal mode
28:24		asys_irq_mode	**irq count frequency mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2s01_1x_en 5'b01010: ext_i2s02_1x_en 5'b01011: ext_i2s03_1x_en 5'b01100: ext_i2s04_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k

Bit(s)	Mnemonic	Name	Description
			5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

11220788 ASYS_IRQ3_CON ASYS IRQ3 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							
Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal** 0: irq disable 1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag** 0: pingpang mode 1: normal mode

Bit(s)	Mnemonic	Name	Description
28:24		asys_irq_mode	**irq count frequency mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2s01_1x_en 5'b01010: ext_i2s02_1x_en 5'b01011: ext_i2s03_1x_en 5'b01100: ext_i2s04_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

Bit(s)	Mnemonic	Name	Description

1122078C ASYS_IRQ4_CON ASYS IRQ4 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							
Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal** 0: irq disable 1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag** 0: pingpang mode 1: normal mode
28:24		asys_irq_mode	**irq count frequency mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2s01_1x_en

Bit(s)	Mnemonic	Name	Description
			5'b01010: ext_i2s02_1x_en 5'b01011: ext_i2s03_1x_en 5'b01100: ext_i2s04_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

11220790 ASYS_IRQ5_CON ASYS IRQ5 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							
Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal** 0: irq disable 1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag** 0: pingpang mode 1: normal mode
28:24		asys_irq_mode	**irq count frequency mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2s01_1x_en 5'b01010: ext_i2s02_1x_en 5'b01011: ext_i2s03_1x_en 5'b01100: ext_i2s04_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k

Bit(s)	Mnemonic	Name	Description
			5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

11220794 ASYS_IRQ6_CON ASYS IRQ6 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							
Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal** 0: irq disable 1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag** 0: pingpang mode 1: normal mode
28:24		asys_irq_mode	**irq count frequency mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k

Bit(s)	Mnemonic	Name	Description
			5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2so1_1x_en 5'b01010: ext_i2so2_1x_en 5'b01011: ext_i2so3_1x_en 5'b01100: ext_i2so4_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

11220798 ASYS_IRQ7_CON ASYS IRQ7 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							

Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal** 0: irq disable 1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag** 0: pingpang mode 1: normal mode
28:24		asys_irq_mode	**irq count frequency mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2s01_1x_en 5'b01010: ext_i2s02_1x_en 5'b01011: ext_i2s03_1x_en 5'b01100: ext_i2s04_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k

Bit(s)	Mnemonic	Name	Description
			5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

1122079C ASYS_IRQ8_CON ASYS IRQ8 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							
Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal** 0: irq disable 1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag** 0: pingpang mode 1: normal mode

Bit(s)	Mnemonic	Name	Description
28:24		asys_irq_mode	**irq count frequency mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2s01_1x_en 5'b01010: ext_i2s02_1x_en 5'b01011: ext_i2s03_1x_en 5'b01100: ext_i2s04_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

Bit(s)	Mnemonic	Name	Description

112207A0 ASYS_IRQ9_CON ASYS IRQ9 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							
Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal** 0: irq disable 1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag** 0: pingpang mode 1: normal mode
28:24		asys_irq_mode	**irq count frequency mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2s01_1x_en

Bit(s)	Mnemonic	Name	Description
			5'b01010: ext_i2s02_1x_en 5'b01011: ext_i2s03_1x_en 5'b01100: ext_i2s04_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

112207A4 ASYS_IRQ10_CON ASYS IRQ10 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							
Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal** 0: irq disable 1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag** 0: pingpang mode 1: normal mode
28:24		asys_irq_mode	**irq count frequency mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2s01_1x_en 5'b01010: ext_i2s02_1x_en 5'b01011: ext_i2s03_1x_en 5'b01100: ext_i2s04_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k

Bit(s)	Mnemonic	Name	Description
			5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

112207A8 ASYS_IRQ11_CON ASYS IRQ11 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							
Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal** 0: irq disable 1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag** 0: pingpang mode 1: normal mode
28:24		asys_irq_mode	**irq count frequency mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k

Bit(s)	Mnemonic	Name	Description
			5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2so1_1x_en 5'b01010: ext_i2so2_1x_en 5'b01011: ext_i2so3_1x_en 5'b01100: ext_i2so4_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

112207AC ASYS_IRQ12_CON ASYS IRQ12 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							

Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal** 0: irq disable 1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag** 0: pingpang mode 1: normal mode
28:24		asys_irq_mode	**irq count frequency mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2so1_1x_en 5'b01010: ext_i2so2_1x_en 5'b01011: ext_i2so3_1x_en 5'b01100: ext_i2so4_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k

Bit(s)	Mnemonic	Name	Description
			5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

112207B0 ASYS_IRQ13_CON ASYS IRQ13 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							
Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal** 0: irq disable 1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag** 0: pingpang mode 1: normal mode

Bit(s)	Mnemonic	Name	Description
28:24		asys_irq_mode	**irq count frequency mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2s01_1x_en 5'b01010: ext_i2s02_1x_en 5'b01011: ext_i2s03_1x_en 5'b01100: ext_i2s04_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

Bit(s)	Mnemonic	Name	Description

112207B4 ASYS_IRQ14_CON ASYS IRQ14 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							
Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal** 0: irq disable 1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag** 0: pingpang mode 1: normal mode
28:24		asys_irq_mode	**irq count frequency mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2s01_1x_en

Bit(s)	Mnemonic	Name	Description
			5'b01010: ext_i2s02_1x_en 5'b01011: ext_i2s03_1x_en 5'b01100: ext_i2s04_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

112207B8 ASYS_IRQ15_CON ASYS IRQ15 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							
Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal** 0: irq disable 1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag** 0: pingpang mode 1: normal mode
28:24		asys_irq_mode	**irq count frequency mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2s01_1x_en 5'b01010: ext_i2s02_1x_en 5'b01011: ext_i2s03_1x_en 5'b01100: ext_i2s04_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k

Bit(s)	Mnemonic	Name	Description
			5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

112207BC ASYS_IRQ16_CON ASYS IRQ16 CONTROL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_on	asys_irq_blk_mode		asys_irq_mode					asys_irq_cnt_ini							
Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asys_irq_cnt_ini															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		asys_irq_on	**local irq enabal** 0: irq disable 1: irq on
30		asys_irq_blk_mode	**0: 2 irq not responss will set miss flag** 0: pingpang mode 1: normal mode
28:24		asys_irq_mode	**irq count frequency mode** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k

Bit(s)	Mnemonic	Name	Description
			5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192kk 5'b01000: 384k 5'b01001: ext_i2so1_1x_en 5'b01010: ext_i2so2_1x_en 5'b01011: ext_i2so3_1x_en 5'b01100: ext_i2so4_1x_en 5'b01101: tdm_out_1x_en 5'b01110: tdm_in_1x_en 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4kk 5'b11000: 352.8k
23:0		asys_irq_cnt_ini	**irq count initial value** after irq on, it will decrease from this value when reach 0 then trigge irq

112207C0 ASYS_IRQ_CLR ASYS IRQ CLEAR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	asys_irq_clear															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	asys_miss_flag_clear															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		asys_irq_clear	**missing flag clear** bit[31] --> miss_flag_16 clear ... bit[16] --> miss_flag_1 clear
15:0		asys_miss_flag_clear	**IRQ clear** bit[15] --> irq16 clear ... bit[0] --> irq1 clear

112207C4 ASYS_IRQ_STATUS ASYS IRQ STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	miss_flag_status															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	irq_status															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		miss_flag_status	**missing flag** bit[31] --> miss_flag_16 ... bit[16] --> miss_flag_1
15:0		irq_status	**IRQ status** bit[15] --> irq16 ... bit[0] --> irq1

112207C8 ASYS_IRQ_MON1 ASYS IRQ MON1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112207CC ASYS_IRQ_MON2 ASYS IRQ MON2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							miss_flag_status	irq_status	irq_cnt_status							
Type							RO	RO	RO							
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	irq_cnt_status															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25		miss_flag_status	**debug**
24		irq_status	**debug**
23:0		irq_cnt_status	**debug (selected from ASYS_IRQ_CONFIG)**

11221180 DMIC_TOP_CON Digital mic control 02000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																

Type																
Reset																

Bit(s)	Name	Description

11221184 DMIC_ULCF_CON1 DMIC fir filter coef 002C0117

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221188 DMIC_ULCF_CON2 DMIC fir filter coef FFF2FEA9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1122118C DMIC_ULCF_CON3 DMIC fir filter coef 004A01D7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																
Type																
Reset																

Bit(s)	Name	Description

11221190 DMIC_ULCF_CON4 DMIC fir filter coef FFB6FD29

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221194 DMIC_ULCF_CON5 DMIC fir filter coef 009603D6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221198 DMIC_ULCF_CON6 DMIC fir filter coef FF3EFAA6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1122119C DMIC_ULCF_CON7 DMIC fir filter coef 013D070A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112211A0 DMIC_ULCF_CON8 DMIC fir filter coef FE3DF6A4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112211A4 DMIC_ULCF_CON9 DMIC fir filter coef 02C20C21

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112211A8 DMIC_ULCF_CON10 DMIC fir filter coef FBCCF029

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112211AC DMIC_ULCF_CON11 DMIC fir filter coef 06DE1494

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112211B0 DMIC_ULCF_CON12 DMIC fir filter coef F439E4D6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112211B4 DMIC_ULCF_CON13 DMIC fir filter coef 1688244E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112211B8 DMIC_ULCF_CON14 DMIC fir filter coef CE44CF0A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112211BC DMIC_ULCF_CON15 DMIC fir filter coef 7FD03927

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221030 DMIC2_TOP_CON Digital mic control 02000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221034 DMIC2_ULCF_CON1 DMIC fir filter coef 002C0117

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221038 DMIC2_ULCF_CON2 DMIC fir filter coef FFF2FEA9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1122103C DMIC2_ULCF_CON3 DMIC fir filter coef 004A01D7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221040 DMIC2_ULCF_CON4 DMIC fir filter coef FFB6FD29

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221044 DMIC2_ULCF_CON5 DMIC fir filter coef 009603D6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221048 DMIC2_ULCF_CON6 DMIC fir filter coef FF3EFAA6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1122104C DMIC2_ULCF_CON7 DMIC fir filter coef 013D070A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221050 DMIC2_ULCF_CON8 DMIC fir filter coef FE3DF6A4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221054 DMIC2_ULCF_CON9 DMIC fir filter coef 02C20C21

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221058 DMIC2_ULCF_CON10 DMIC fir filter coef FBCCF029

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1122105C DMIC2_ULCF_CON11 DMIC fir filter coef 06DE1494

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221060 DMIC2_ULCF_CON12 DMIC fir filter coef F439E4D6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221064 DMIC2_ULCF_CON13 DMIC fir filter coef 1688244E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221068 DMIC2_ULCF_CON14 DMIC fir filter coef CE44CF0A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1122106C DMIC2_ULCF_CON15 DMIC fir filter coef 7FD03927

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221070 PWR2_ASM_CON1 sample base ASRC clock selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									i2s_out6_asrc_cali_ck_sel	i2s_out6_asrc_process_clk_sel		i2s_out5_asrc_cali_ck_sel	i2s_out5_asrc_process_clk_sel		i2s_out4_asrc_cali_ck_sel	i2s_out4_asrc_process_clk_sel
Type									RW	RW		RW	RW		RW	RW

Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	i2s_out4_asrc_process_clk_sel	i2s_out3_asrc_cali_ck_sel	i2s_out3_asrc_process_clk_sel		i2s_in6_asrc_cali_ck_sel	i2s_in6_asrc_process_clk_sel		i2s_in5_asrc_cali_ck_sel	i2s_in5_asrc_process_clk_sel		i2s_in4_asrc_cali_ck_sel	i2s_in4_asrc_process_clk_sel		i2s_in3_asrc_cali_ck_sel	i2s_in3_asrc_process_clk_sel	
Type	RW	RW	RW		RW	RW		RW	RW		RW	RW		RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23		i2s_out6_asrc_cali_ck_sel	**caliculation clock select** 0: a1sys_hoping_ck 1: a2sys_hoping_ck
22:21		i2s_out6_asrc_process_clk_sel	**pocessing clock select** 2'b00: low freq clock 2'b01: middle freq clock 2'b10: high req clock
20		i2s_out5_asrc_cali_ck_sel	**caliculation clock select** 0: a1sys_hoping_ck 1: a2sys_hoping_ck
19:18		i2s_out5_asrc_process_clk_sel	**pocessing clock select** 2'b00: low freq clock 2'b01: middle freq clock 2'b10: high req clock
17		i2s_out4_asrc_cali_ck_sel	**caliculation clock select** 0: a1sys_hoping_ck 1: a2sys_hoping_ck
16:15		i2s_out4_asrc_process_clk_sel	**pocessing clock select** 2'b00: low freq clock

Bit(s)	Mnemonic	Name	Description
			2'b01: middle freq clock
			2'b10: high req clock
14		i2s_out3_asrc_cali_ck_sel	**caliculation clock select**
			0: a1sys_hoping_ck
			1: a2sys_hoping_ck
13:12		i2s_out3_asrc_process_clk_sel	**pocessing clock select**
			2'b00: low freq clock
			2'b01: middle freq clock
			2'b10: high req clock
11		i2s_in6_asrc_cali_ck_sel	**caliculation clock select**
			0: a1sys_hoping_ck
			1: a2sys_hoping_ck
10:9		i2s_in6_asrc_process_clk_sel	**pocessing clock select**
			2'b00: low freq clock
			2'b01: middle freq clock
			2'b10: high req clock
8		i2s_in5_asrc_cali_ck_sel	**caliculation clock select**
			0: a1sys_hoping_ck
			1: a2sys_hoping_ck
7:6		i2s_in5_asrc_process_clk_sel	**pocessing clock select**
			2'b00: low freq clock
			2'b01: middle freq clock
			2'b10: high req clock
5		i2s_in4_asrc_cali_ck_sel	**caliculation clock select**
			0: a1sys_hoping_ck

Bit(s)	Mnemonic	Name	Description
			1: a2sys_hoping_ck
4:3		i2s_in4_asrc_process_clk_sel	**pocessing clock select** 2'b00: low freq clock 2'b01: middle freq clock 2'b10: high req clock
2		i2s_in3_asrc_cali_ck_sel	**caliculation clock select** 0: a1sys_hoping_ck 1: a2sys_hoping_ck
1:0		i2s_in3_asrc_process_clk_sel	**pocessing clock select** 2'b00: low freq clock 2'b01: middle freq clock 2'b10: high req clock

11221074 PWR2_ASM_CON2 mem base ASRC clock selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								masm5_sft_rst	masm4_sft_rst	masm3_sft_rst	masm2_sft_rst	masm1_sft_rst				
Type								RW	RW	RW	RW	RW				
Reset								0	0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		mem_asrc5_cali_ck_sel	mem_asrc5_asrc_process_clk_sel		mem_asrc4_cali_ck_sel	mem_asrc4_asrc_process_clk_sel		mem_asrc3_cali_ck_sel	mem_asrc3_asrc_process_clk_sel		mem_asrc2_cali_ck_sel	mem_asrc2_asrc_process_clk_sel		mem_asrc1_cali_ck_sel	mem_asrc1_asrc_process_clk_sel	
Type		RW	RW		RW	RW		RW	RW		RW	RW		RW	RW	
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24		masm5_sft_rst	**mem asrc5 soft reset** 0: normal

Bit(s)	Mnemonic	Name	Description
			1: reset
23		masm4_sft_rst	**mem asrc4 soft reset** 0: normal 1: reset
22		masm3_sft_rst	**mem asrc3 soft reset** 0: normal 1: reset
21		masm2_sft_rst	**mem asrc2 soft reset** 0: normal 1: reset
20		masm1_sft_rst	**mem asrc1 soft reset** 0: normal 1: reset
14		mem_asrc5_cali_ck_sel	**caliculation clock select** 0: a1sys_hoping_ck 1: a2sys_hoping_ck
13:12		mem_asrc5_asrc_process_clk_sel	**pocessing clock select** 2'b00: low freq clock 2'b01: middle freq clock 2'b10: high req clock
11		mem_asrc4_cali_ck_sel	**caliculation clock select** 0: a1sys_hoping_ck 1: a2sys_hoping_ck
10:9		mem_asrc4_asrc_process_clk_sel	**pocessing clock select** 2'b00: low freq clock 2'b01: middle freq clock 2'b10: high req clock

Bit(s)	Mnemonic	Name	Description
8		mem_asrc3_cali_ck_sel	**caliculation clock select** 0: a1sys_hoping_ck 1: a2sys_hoping_ck
7:6		mem_asrc3_asrc_process_clk_sel	**pocessing clock select** 2'b00: low freq clock 2'b01: middle freq clock 2'b10: high req clock
5		mem_asrc2_cali_ck_sel	**caliculation clock select** 0: a1sys_hoping_ck 1: a2sys_hoping_ck
4:3		mem_asrc2_asrc_process_clk_sel	**pocessing clock select** 2'b00: low freq clock 2'b01: middle freq clock 2'b10: high req clock
2		mem_asrc1_cali_ck_sel	**caliculation clock select** 0: a1sys_hoping_ck 1: a2sys_hoping_ck
1:0		mem_asrc1_asrc_process_clk_sel	**pocessing clock select** 2'b00: low freq clock 2'b01: middle freq clock 2'b10: high req clock

11221078 PWR2_ASM_CON3 ASM BRIDGE control 00004440

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pwr2_asm_con3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	pwr2_asm_con3															
Type	RW															
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		pwr2_asm_con3	**asm bridge control**

1122107C PWR2_ASM_CON4 ASM BRIDGE control 00020002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pwr2_asm_con4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pwr2_asm_con4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:0		pwr2_asm_con4	**asm bridge control**

11221080 PWR2_ASM_MON0 ASM BRIDGE control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pwr2_asm_mono															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pwr2_asm_mono															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		pwr2_asm_mono	

11221084 PWR2_ASM_MON1 ASM BRIDGE control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	pwr2_asm_mon1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pwr2_asm_mon1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		pwr2_asm_mon1	

11221088 AFE_LRCK_CNT lrck number count and read control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_lrck_cnt												lrck_counting_status			
Type	RO												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													slave_lrck_select			lrck_count_enable
Type													RW			RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:20		afe_lrck_cnt	**lrck counter number in the lrck cycle**
19		lrck_counting_status	
3:1		slave_lrck_select	**i2s out6 lrck/bck from i2s out1** 3'b000: i2sin1 slave lrck 3'b001: i2sin2 slave lrck 3'b010: i2sin3 slave lrck 3'b011: i2sin4 slave lrck 3'b100: i2sin5 slave lrck

Bit(s)	Mnemonic	Name	Description
			3'b101: i2sin6 slave lrck
			3'b110: pcm_sync_in
			3'b111: hdmi_rx_lrck
0		lrck_count_enable	**lrck count enable** 0: Disable 1: Enable

1122108C MASM_TRAC_CON1 asrc cali lrck sel 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		masrc5_calc_lrck_selector			masrc4_calc_lrck_selector			masrc3_calc_lrck_selector			masrc2_calc_lrck_selector			masrc1_calc_lrck_selector		
Type		RW			RW			RW			RW			RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
14:12		masrc5_calc_lrck_selector	**masrc5 calc lrck selector** 3'b000: 0 3'b001: i2s1 slave lrck 3'b010: i2s2 slave lrck 3'b011: i2s3 slave lrck 3'b100: i2s4 slave lrck 3'b101: i2s5 slave lrck 3'b110: i2s6 slave lrck 3'b111: pcm_sync_in_ext
11:9		masrc4_calc_lrck_selector	**masrc4 calc lrck selector** 3'b000: 0

Bit(s)	Mnemonic	Name	Description
			3'b001: i2s1 slave lrck 3'b010: i2s2 slave lrck 3'b011: i2s3 slave lrck 3'b100: i2s4 slave lrck 3'b101: i2s5 slave lrck 3'b110: i2s6 slave lrck 3'b111: pcm_sync_in_ext
8:6		masrc3_calc_lrck_selector	**masrc3 calc lrck selector** 3'b000: 0 3'b001: i2s1 slave lrck 3'b010: i2s2 slave lrck 3'b011: i2s3 slave lrck 3'b100: i2s4 slave lrck 3'b101: i2s5 slave lrck 3'b110: i2s6 slave lrck 3'b111: pcm_sync_in_ext
5:3		masrc2_calc_lrck_selector	**masrc2 calc lrck selector** 3'b000: 0 3'b001: i2s1 slave lrck 3'b010: i2s2 slave lrck 3'b011: i2s3 slave lrck 3'b100: i2s4 slave lrck 3'b101: i2s5 slave lrck 3'b110: i2s6 slave lrck 3'b111: pcm_sync_in_ext
2:0		masrc1_calc_lrck_selector	**masrc1 calc lrck selector** 3'b000: 0

Bit(s)	Mnemonic	Name	Description
			3'b001: i2s1 slave lrck 3'b010: i2s2 slave lrck 3'b011: i2s3 slave lrck 3'b100: i2s4 slave lrck 3'b101: i2s5 slave lrck 3'b110: i2s6 slave lrck 3'b111: pcm_sync_in_ext

11220800 AFE_ASRC_NEW_CON0 ASRC Config 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CHSET0_O16BIT		CHSET0_CLR_IIR_HISTORY	CHSET0_IS_MONO
Type													RW		RW	RW
Reset													0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHSET0_OFS_SEL		CHSET0_IFS_SEL		CHSET0_IIR_EN	CHSET0_IIR_STAGE						CHSET_STR_CLR		CHSET_ON	COEF_SRAM_CTRL	ASM_ON
Type	RW		RW		RW	RW						RW		RU	RW	RW
Reset	0	0	0	0	0	0	0	0				0		0	0	0

Bit(s)	Mnemonic	Name	Description
19		CHSET0_O16BIT	**Selects 16-bit/32-bit output** 0: 32-bit 1: 16-bit
17		CHSET0_CLR_IIR_HISTORY	**Set to 1 to clear current IIR output history buffer for TX. This register will auto-clear once the histories are cleared.**
16		CHSET0_IS_MONO	**Mono/Stereo selection register**
15:14		CHSET0_OFS_SEL	**Selects output sample rate.**

Bit(s)	Mnemonic	Name	Description
			TX: Set to 00 for OFS fix value. RX: Set to 01 for OFS fix value. 2'b00: I2S slave out 2'b01: I2S slave in
13:12		CHSET0_IFS_SEL	**Selects input sample rate selection.** TX: Set to 11 for period tracking mode. RX: Set to 10 for frequency tracking mode. 2'b11: I2S slave out 2'b10: I2S slave in
11		CHSET0_IIR_EN	**Enables anti-alias IIR filter for TX.** Set 1 to Turns on anti-alias IIR filter.
10:8		CHSET0_IIR_STAGE	**Anti-alias IIR filter stage for TX.** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
4		CHSET_STR_CLR	**Each channel set clear signal** Set bit 0 to 1 to clear the TX history. Set bit 1 to 1 to clear the RX history. Set bit 2 to 1 to clear the I2S history.
2		CHSET_ON	**Indicates channel set is on currently.**
1		COEFF_SRAM_CTRL	**Controls coefficient SRAM access** 0: Disable access 1: Enable access
0		ASM_ON	**ASRC enabling signal** Turn it on after all configurations are set. 0: Disable ASRC 1: Enable ASRC

11220804 AFE_ASRC_NEW_CON1 ASRC Config 1 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name									ASM_FREQ_0							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_0															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_0	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX OFS.

11220808 AFE_ASRC_NEW_CON2 ASRC Config 2 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_1							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_1	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX OFS.

1122080C AFE_ASRC_NEW_CON3 ASRC Config 3 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_2							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	ASM_FREQ_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_2	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX IFS.

11220810 AFE_ASRC_NEW_CON4 ASRC Config 4 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_3							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_3															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_3	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX IFS.

11220814 AFE_ASRC_NEW_CON5 ASRC Config 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RESULT_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		RESULT_SEL	**Selects output** 3'b000: ASRC output 3'b001: Data input 3'b010: CMPF output 3'b011: HBF1 output 3'b100: HBF2 output 3'b101: HBF3 output 3'b110: HBF4 output 3'b111: Each IIR stage output in order

11220818 AFE_ASRC_NEW_CON6 ASRC Config 6 00010800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FREQ_CALI_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_EN		FREQ_CALC_RUNNING	AUTO_TUNE_FREQ3	COMP_FREQ_RES_EN		FREQ_CALI_SEL		FREQ_CALI_BP_DGL	FREQ_CALI_MAX_GWIDTH			AUTO_TUNE_FREQ2	FREQ_CALI_AUTO_RESTART	CALI_USE_FREQ_OUT	CALI_EN
Type	RW		RU	RW	RW		RW		RW	RW			RW	RW	RW	RU
Reset	0		0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		FREQ_CALI_CYCLE	**Frequency calibrating cycle register.** Defines how many input signal cycles the calibrator calibrates are in one round. This register is updated into calibrator once the calibrator enable [0] is turned on.
15		FREQ_CALI_AUTORST_EN	**Enables period calibration auto-reset** Period calibration being larger than FREQ_CALI_AUTORST_TH_HIGH or smaller than FREQ_CALI_AUTORST_TH_LOW will trigger ASRC reset.

Bit(s)	Mnemonic	Name	Description
13		FREQ_CALC_RUNNING	**Shows if frequency calculation is running.** For one round running case, wait for this bit and the CALI_EN bit to become low before frequency result is ready.
12		AUTO_TUNE_FREQ3	**Enables asm_freq_3 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave out.** 0: Disable auto update 1: Enable auto update
11		COMP_FREQ_RES_EN	**Frequency compensation enabling register.** 0: Disable compensation 1: Enable compensation
9:8		FREQ_CALI_SEL	**Calibrator input source selection register. Before modifying this register, make sure the calibrator is turned off.** 2'b00: Use PCM SYNC word 2'b01: Not connected 2'b10: Not connected 2'b11: Not connected
7		FREQ_CALI_BP_DGL	**Bypasses deglitch circuit for calibrator input** 0: No bypass 1: Bypass
6:4		FREQ_CALI_MAX_GWIDTH	**Defines the maximum glitch width of the calibrator input signal. Unit: Calibrator reference clock cycles.**
3		AUTO_TUNE_FREQ2	**Enables asm_freq_2 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave in.** 0: Disable auto update 1: Enable auto update
2		FREQ_CALI_AUTO_RESTART	**Enables calibrator auto restart new calibration while one run is completed. This value will be updated into calibrator once the enabling signal is turned on from off state.** 0: Disable auto restart

Bit(s)	Mnemonic	Name	Description
			1: Enable auto restart
1		CALI_USE_FREQ_OUT	**Selects frequency or period calibration mode** 0: Use period calibration result to update asm_freq_2. Use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2. Use period calibration result to update asm_freq_3
0		CALI_EN	**Enables frequency calibrator** If auto restart is 0, this bit will be cleared while one calibration run is completed. If this bit is set to 0, wait until this bit becomes 0 to make the next run start safely. 0: Disable calibrator 1: Enable calibrator

1122081C AFE_ASRC_NEW_CON7 ASRC Config 7 00000659

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALC_DENOMINATOR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALC_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALC_DENOMINATOR	**Determines the denominator for performing period-to-frequency calibration result translation.**

11220820 AFE_ASRC_NEW_CON8 ASRC Config 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PRD_CALI_RESULT_RECORD							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	PRD_CALI_RESULT_RECORD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		PRD_CALI_RESULT_RECORD	**Period calibration result.** Records the calibration result of the previous round. Writing any value to this register will clear the result.

11220824 AFE_ASRC_NEW_CON9 ASRC Config 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_RESULT							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_RESULT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_RESULT	**Frequency calibrator result.** Records the calibration result of previous round. This value is got from the quotient of (FREQ_CALC_DENOMINATOR / PRD_CALI_RESULT) in 1.23 format.

11220828 AFE_ASRC_NEW_CON10 ASRC Config 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									COEFF_SRAM_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COEFF_SRAM_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		COEFF_SRAM_DATA	**Read/Write data port of coefficient SRAM.** Read data have one cycle delay. The coefficients are filled stage by stage: each stage has 6 coefficients. For the 2nd-order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2/1 + (2^shift)*b1*Z^ -1 + (2^shift)*b2*Z^-2" The coefficient should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

1122082C AFE_ASRC_NEW_CON11 ASRC Config 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**COEFF_SRAM_ADR**						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6:0		COEFF_SRAM_ADR	**Determines the rd/wr address of IIR coefficient SRAM.** Read/Write COEFF_SRAM_DATA will make this register increase by 1.

11220834 AFE_ASRC_NEW_CON13 ASRC Config 13 00001B00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**FREQ_CALI_AUTORST_TH_HIGH**							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FREQ_CALI_AUTORST_TH_HIGH**															
Type	RW															

Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_HIGH	**High period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

11220838 AFE_ASRC_NEW_CON14 ASRC Config 14 00001800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_LOW							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_LOW															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_LOW	**Low period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

11220840 AFE_ASRCI2_NEW_CON0 ASRC Config 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CHSETo_O16BIT		CHSETo_CLR_IIR_HISTORY	CHSETo_IS_MONO
Type													RW		RW	RW
Reset													0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHSETo_OFS_SEL		CHSETo_IFS_SEL		CHSETo_IIR_EN	CHSETo_IIR_STAGE						CHSET_STR_CLR		CHSET_ON	COEFF_SRAM_CTRL	ASM_ON
Type	RW		RW		RW	RW						RW		RU	RW	RW

Reset	0	0	0	0	0	0	0	0				0		0	0	0

Bit(s)	Mnemonic	Name	Description
19		CHSETo_O16BIT	**Selects 16-bit/32-bit output** 0: 32-bit 1: 16-bit
17		CHSETo_CLR_IIR_HISTORY	**Set to 1 to clear current IIR output history buffer for TX. This register will auto-clear once the histories are cleared.**
16		CHSETo_IS_MONO	**Mono/Stereo selection register**
15:14		CHSETo_OFS_SEL	**Selects output sample rate.** TX: Set to 00 for OFS fix value. RX: Set to 01 for OFS fix value. 2'b00: I2S slave out 2'b01: I2S slave in
13:12		CHSETo_IFS_SEL	**Selects input sample rate selection.** TX: Set to 11 for period tracking mode. RX: Set to 10 for frequency tracking mode. 11: I2S slave out 10: I2S slave in
11		CHSETo_IIR_EN	**Enables anti-alias IIR filter for TX.** Set 1 to Turns on anti-alias IIR filter.
10:8		CHSETo_IIR_STAGE	**Anti-alias IIR filter stage for TX.** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
4		CHSET_STR_CLR	**Each channel set clear signal** Set bit 0 to 1 to clear the TX history. Set bit 1 to 1 to clear the RX history. Set bit 2 to 1 to clear the I2S history.
2		CHSET_ON	**Indicates channel set is on currently.**
1		COEFF_SRAM_CTRL	**Controls coefficient SRAM access** 0: Disable access

Bit(s)	Mnemonic	Name	Description
			1: Enable access
0		ASM_ON	**ASRC enabling signal** Turn it on after all configurations are set. 0: Disable ASRC 1: Enable ASRC

11220844 AFE_ASRCI2_NEW_CON1 ASRC Config 1 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_0							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_0															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_0	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX OFS.

11220848 AFE_ASRCI2_NEW_CON2 ASRC Config 2 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_1							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_1	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX OFS.

1122084C AFE_ASRCI2_NEW_CON3 ASRC Config 3 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_2							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_2	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX IFS.

11220850 AFE_ASRCI2_NEW_CON4 ASRC Config 4 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_3							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_3															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_3	**Frequency palette.**

Bit(s)	Mnemonic	Name	Description
			The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX IFS.

11220854 AFE_ASRCI2_NEW_CON5 ASRC Config 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RESULT_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		RESULT_SEL	**Selects output** 3'b000: ASRC output 3'bv001: Data input 3'b010: CMPF output 3'b011: HBF1 output 3'b100: HBF2 output 3'b101: HBF3 output 3'b110: HBF4 output 3'b111: Each IIR stage output in order

11220858 AFE_ASRCI2_NEW_CON6 ASRC Config 6 00010800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FREQ_CALI_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	FREQ_CALI_AUTORST_EN		FREQ_CALC_RUNNING	AUTO_TUNE_FREQ3	COMP_FREQ_RES_EN		FREQ_CALI_SEL		FREQ_CALI_BP_DGL	FREQ_CALI_MAX_GWIDTH			AUTO_TUNE_FREQ2	FREQ_CALI_AUTO_RESTART	CALI_USE_FREQ_OUT	CALI_EN
Type	RW		RU	RW	RW		RW		RW	RW			RW	RW	RW	RU
Reset	0		0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		FREQ_CALI_CYCLE	**Frequency calibrating cycle register.** Defines how many input signal cycles the calibrator calibrates are in one round. This register is updated into calibrator once the calibrator enable [0] is turned on.
15		FREQ_CALI_AUTORST_EN	**Enables period calibration auto-reset** Period calibration being larger than FREQ_CALI_AUTORST_TH_HIGH or smaller than FREQ_CALI_AUTORST_TH_LOW will trigger ASRC reset.
13		FREQ_CALC_RUNNING	**Shows if frequency calculation is running.** For one round running case, wait for this bit and the CALI_EN bit to become low before frequency result is ready.
12		AUTO_TUNE_FREQ3	**Enables asm_freq_3 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave out.** 0: Disable auto update 1: Enable auto update
11		COMP_FREQ_RES_EN	**Frequency compensation enabling register.** 0: Disable compensation 1: Enable compensation
9:8		FREQ_CALI_SEL	**Calibrator input source selection register. Before modifying this register, make sure the calibrator is turned off.** 2'b00: Use PCM SYNC word 2'b01: Not connected 2'b10: Not connected 2'b11: Not connected

Bit(s)	Mnemonic	Name	Description
7		FREQ_CALI_BP_DGL	**Bypasses deglitch circuit for calibrator input** 0: No bypass 1: Bypass
6:4		FREQ_CALI_MAX_GWIDTH	**Defines the maximum glitch width of the calibrator input signal. Unit: Calibrator reference clock cycles.**
3		AUTO_TUNE_FREQ2	**Enables asm_freq_2 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave in.** 0: Disable auto update 1: Enable auto update
2		FREQ_CALI_AUTO_RESTART	**Enables calibrator auto restart new calibration while one run is completed. This value will be updated into calibrator once the enabling signal is turned on from off state.** 0: Disable auto restart 1: Enable auto restart
1		CALI_USE_FREQ_OUT	**Selects frequency or period calibration mode** 0: Use period calibration result to update asm_freq_2. Use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2. Use period calibration result to update asm_freq_3
0		CALI_EN	**Enables frequency calibrator** If auto restart is 0, this bit will be cleared while one calibration run is completed. If this bit is set to 0, wait until this bit becomes 0 to make the next run start safely. 0: Disable calibrator 1: Enable calibrator

1122085C AFE_ASRCI2_NEW_CON7 ASRC Config 7 00000659

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALC_DENOMINATOR							
Type									RW							

Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALC_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALC_DENOMINATOR	**Determines the denominator for performing period-to-frequency calibration result translation.**

11220860 AFE_ASRCI2_NEW_CON8 ASRC Config 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PRD_CALI_RESULT_RECORD							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRD_CALI_RESULT_RECORD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		PRD_CALI_RESULT_RECORD	**Period calibration result.** Records the calibration result of the previous round. Writing any value to this register will clear the result.

11220864 AFE_ASRCI2_NEW_CON9 ASRC Config 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_RESULT							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_RESULT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_RESULT	**Frequency calibrator result.** Records the calibration result of previous round. This value is got from the quotient of (FREQ_CALC_DENOMINATOR / PRD_CALI_RESULT) in 1.23 format.

11220868 AFE_ASRCI2_NEW_CON10 ASRC Config 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									COEFF_SRAM_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COEFF_SRAM_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		COEFF_SRAM_DATA	**Read/Write data port of coefficient SRAM.** Read data have one cycle delay. The coefficients are filled stage by stage: each stage has 6 coefficients. For the 2nd-order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2/1 + (2^shift)*b1*Z^ -1 + (2^shift)*b2*Z^-2" The coefficient should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

1122086C AFE_ASRCI2_NEW_CON11 ASRC Config 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name										COEFF_SRAM_ADR						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6:0		COEFF_SRAM_ADR	**Determines the rd/wr address of IIR coefficient SRAM.** Read/Write COEFF_SRAM_DATA will make this register increase by 1.

11220874 AFE_ASRCI2_NEW_CON13 ASRC Config 13 00001B00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_HIGH							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_HIGH															
Type	RW															
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_HIGH	**High period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

11220878 AFE_ASRCI2_NEW_CON14 ASRC Config 14 00001800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_LOW							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_LOW															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_LOW	**Low period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

11220880 AFE_ASRCI3_NEW_CON0 ASRC Config 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CHSETo_O16BIT		CHSETo_CLR_IIR_HISTORY	CHSETo_IS_MONO
Type													RW		RW	RW
Reset													0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHSETo_OFS_SEL		CHSETo_IFS_SEL		CHSETo_IIR_EN	CHSETo_IIR_STAGE						CHSET_STR_CLR		CHSET_ON	COEFF_SRAM_CTRL	ASM_ON
Type	RW		RW		RW	RW						RW		RU	RW	RW
Reset	0	0	0	0	0	0	0	0				0		0	0	0

Bit(s)	Mnemonic	Name	Description
19		CHSETo_O16BIT	**Selects 16-bit/32-bit output** 0: 32-bit 1: 16-bit
17		CHSETo_CLR_IIR_HISTORY	**Set to 1 to clear current IIR output history buffer for TX. This register will auto-clear once the histories are cleared.**
16		CHSETo_IS_MONO	**Mono/Stereo selection register**
15:14		CHSETo_OFS_SEL	**Selects output sample rate.** TX: Set to 00 for OFS fix value. RX: Set to 01 for OFS fix value. 00: I2S slave out 01: I2S slave in

Bit(s)	Mnemonic	Name	Description
13:12		CHSETo_IFS_SEL	**Selects input sample rate selection.** TX: Set to 11 for period tracking mode. RX: Set to 10 for frequency tracking mode. 11: I2S slave out 10: I2S slave in
11		CHSETo_IIR_EN	**Enables anti-alias IIR filter for TX.** Set 1 to Turns on anti-alias IIR filter.
10:8		CHSETo_IIR_STAGE	**Anti-alias IIR filter stage for TX.** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
4		CHSET_STR_CLR	**Each channel set clear signal** Set bit 0 to 1 to clear the TX history. Set bit 1 to 1 to clear the RX history. Set bit 2 to 1 to clear the I2S history.
2		CHSET_ON	**Indicates channel set is on currently.**
1		COEFF_SRAM_CTRL	**Controls coefficient SRAM access** 0: Disable access 1: Enable access
0		ASM_ON	**ASRC enabling signal** Turn it on after all configurations are set. 0: Disable ASRC 1: Enable ASRC

11220884 AFE_ASRCI3_NEW_CON1 ASRC Config 1 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_0							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_0															

Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_0	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX OFS.

11220888 AFE_ASRCI3_NEW_CON2 ASRC Config 2 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_1							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_1	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX OFS.

1122088C AFE_ASRCI3_NEW_CON3 ASRC Config 3 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_2							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_2	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX IFS.

11220890 AFE_ASRCI3_NEW_CON4 ASRC Config 4 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_3							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_3															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_3	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX IFS.

11220894 AFE_ASRCI3_NEW_CON5 ASRC Config 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RESULT_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		RESULT_SEL	**Selects output** 3'b000: ASRC output 3'b001: Data input 3'b010: CMPF output 3'b011: HBF1 output 3'b100: HBF2 output 3'b101: HBF3 output 3'b110: HBF4 output 3'b111: Each IIR stage output in order

11220898 AFE_ASRCI3_NEW_CON6 ASRC Config 6 00010800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FREQ_CALI_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_EN		FREQ_CALC_RUNNING	AUTO_TUNE_FREQ3	COMP_FREQ_RES_EN		FREQ_CALI_SEL		FREQ_CALI_BP_DGL	FREQ_CALI_MAX_GWIDTH			AUTO_TUNE_FREQ2	FREQ_CALI_AUTO_RESTART	CALI_USE_FREQ_OUT	CALI_EN
Type	RW		RU	RW	RW		RW		RW	RW			RW	RW	RW	RU
Reset	0		0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		FREQ_CALI_CYCLE	**Frequency calibrating cycle register.** Defines how many input signal cycles the calibrator calibrates are in one round. This register is updated into calibrator once the calibrator enable [0] is turned on.
15		FREQ_CALI_AUTORST_EN	**Enables period calibration auto-reset** Period calibration being larger than FREQ_CALI_AUTORST_TH_HIGH or smaller than

Bit(s)	Mnemonic	Name	Description
			FREQ_CALI_AUTORST_TH_LOW will trigger ASRC reset.
13		FREQ_CALC_RUNNING	**Shows if frequency calculation is running.** For one round running case, wait for this bit and the CALI_EN bit to become low before frequency result is ready.
12		AUTO_TUNE_FREQ3	**Enables asm_freq_3 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave out.** 0: Disable auto update 1: Enable auto update
11		COMP_FREQ_RES_EN	**Frequency compensation enabling register.** 0: Disable compensation 1: Enable compensation
9:8		FREQ_CALI_SEL	**Calibrator input source selection register. Before modifying this register, make sure the calibrator is turned off.** 2'b00: Use PCM SYNC word 2'b01: Not connected 2'b10: Not connected 2'b11: Not connected
7		FREQ_CALI_BP_DGL	**Bypasses deglitch circuit for calibrator input** 0: No bypass 1: Bypass
6:4		FREQ_CALI_MAX_GWIDTH	**Defines the maximum glitch width of the calibrator input signal. Unit: Calibrator reference clock cycles.**
3		AUTO_TUNE_FREQ2	**Enables asm_freq_2 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave in.** 0: Disable auto update 1: Enable auto update
2		FREQ_CALI_AUTO_RESTART	**Enables calibrator auto restart new calibration while one run is completed. This value will be updated into calibrator once the enabling signal is turned on from off state.**

Bit(s)	Mnemonic	Name	Description
			0: Disable auto restart 1: Enable auto restart
1		CALI_USE_FREQ_OUT	**Selects frequency or period calibration mode** 0: Use period calibration result to update asm_freq_2. Use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2. Use period calibration result to update asm_freq_3
0		CALI_EN	**Enables frequency calibrator** If auto restart is 0, this bit will be cleared while one calibration run is completed. If this bit is set to 0, wait until this bit becomes 0 to make the next run start safely. 0: Disable calibrator 1: Enable calibrator

1122089C AFE_ASRCI3_NEW_CON7 ASRC Config 7 00000659

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALC_DENOMINATOR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALC_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALC_DENOMINATOR	**Determines the denominator for performing period-to-frequency calibration result translation.**

1122208A0 AFE_ASRCI3_NEW_CON8 ASRC Config 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PRD_CALI_RESULT_RECORD							

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRD_CALI_RESULT_RECORD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		PRD_CALI_RESULT_RECORD	**Period calibration result.** Records the calibration result of the previous round. Writing any value to this register will clear the result.

112208A4 AFE_ASRCI3_NEW_CON9 ASRC Config 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_RESULT							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_RESULT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_RESULT	**Frequency calibrator result.** Records the calibration result of previous round. This value is got from the quotient of (FREQ_CALC_DENOMINATOR / PRD_CALI_RESULT) in 1.23 format.

112208A8 AFE_ASRCI3_NEW_CON10 ASRC Config 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									COEFF_SRAM_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COEFF_SRAM_DATA															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		COEFF_SRAM_DATA	**Read/Write data port of coefficient SRAM.** Read data have one cycle delay. The coefficients are filled stage by stage: each stage has 6 coefficients. For the 2nd-order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2/1 + (2^shift)*b1*Z^-1 + (2^shift)*b2*Z^-2" The coefficient should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

112208AC AFE_ASRCI3_NEW_CON11 ASRC Config 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										COEFF_SRAM_ADR						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6:0		COEFF_SRAM_ADR	**Determines the rd/wr address of IIR coefficient SRAM.** Read/Write COEFF_SRAM_DATA will make this register increase by 1.

112208B4 AFE_ASRCI3_NEW_CON13 ASRC Config 13 00001B00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_HIGH							
Type									RW							

Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_HIGH															
Type	RW															
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_HIGH	**High period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

112208B8 AFE_ASRCI3_NEW_CON14 ASRC Config 14 00001800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_LOW							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_LOW															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_LOW	**Low period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

112208C0 AFE_ASRCI4_NEW_CON0 ASRC Config 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CHSETo_O16BIT		CHSETo_CLR_IIR_HISTORY	CHSETo_IS_MONO
Type													RW		RW	RW
Reset													0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CHSETo_OFS_SEL		CHSETo_IFS_SEL		CHSETo_IIR_EN	CHSETo_IIR_STAGE						CHSET_STR_CLR		CHSET_ON	COEFF_SRAM_CTRL	ASM_ON
Type	RW		RW		RW	RW						RW		RU	RW	RW
Reset	0	0	0	0	0	0	0	0				0		0	0	0

Bit(s)	Mnemonic	Name	Description
19		CHSETo_O16BIT	**Selects 16-bit/32-bit output** 0: 32-bit 1: 16-bit
17		CHSETo_CLR_IIR_HISTORY	**Set to 1 to clear current IIR output history buffer for TX. This register will auto-clear once the histories are cleared.**
16		CHSETo_IS_MONO	**Mono/Stereo selection register**
15:14		CHSETo_OFS_SEL	**Selects output sample rate.** TX: Set to 00 for OFS fix value. RX: Set to 01 for OFS fix value. 2'b00: I2S slave out 2'b01: I2S slave in
13:12		CHSETo_IFS_SEL	**Selects input sample rate selection.** TX: Set to 11 for period tracking mode. RX: Set to 10 for frequency tracking mode. 2'b11: I2S slave out 2'b10: I2S slave in
11		CHSETo_IIR_EN	**Enables anti-alias IIR filter for TX.** Set 1 to Turns on anti-alias IIR filter.
10:8		CHSETo_IIR_STAGE	**Anti-alias IIR filter stage for TX.** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
4		CHSET_STR_CLR	**Each channel set clear signal** Set bit 0 to 1 to clear the TX history. Set bit 1 to 1 to clear the RX history. Set bit 2 to 1 to clear the I2S history.

Bit(s)	Mnemonic	Name	Description
2		CHSET_ON	**Indicates channel set is on currently.**
1		COEFF_SRAM_CTRL	**Controls coefficient SRAM access** 0: Disable access 1: Enable access
0		ASM_ON	**ASRC enabling signal** Turn it on after all configurations are set. 0: Disable ASRC 1: Enable ASRC

112208C4 AFE_ASRCI4_NEW_CON1 ASRC Config 1 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_0							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_0															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_0	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX OFS.

112208C8 AFE_ASRCI4_NEW_CON2 ASRC Config 2 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_1							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	ASM_FREQ_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_1	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX OFS.

112208CC AFE_ASRCI4_NEW_CON3 ASRC Config 3 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_2							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_2	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX IFS.

112208D0 AFE_ASRCI4_NEW_CON4 ASRC Config 4 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_3							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_3															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_3	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX IFS.

112208D4 AFE_ASRCI4_NEW_CON5 ASRC Config 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**RESULT_SEL**		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		RESULT_SEL	**Selects output** 3'b000: ASRC output 3'b001: Data input 3'b010: CMPF output 3'b011: HBF1 output 3'b100: HBF2 output 3'b101: HBF3 output 3'b110: HBF4 output 3'b111: Each IIR stage output in order

112208D8 AFE_ASRCI4_NEW_CON6 ASRC Config 6 00010800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**FREQ_CALI_CYCLE**															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_EN		FREQ_CALC_RUNNING	AUTO_TUNE_FREQ3	COMP_FREQ_RES_EN		FREQ_CALI_SEL		FREQ_CALI_BP_DGL	FREQ_CALI_MAX_GWIDTH			AUTO_TUNE_FREQ2	FREQ_CALI_AUTO_RESTART	CALI_USE_FREQ_OUT	CALI_EN
Type	RW		RU	RW	RW		RW		RW	RW			RW	RW	RW	RU
Reset	0		0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		FREQ_CALI_CYCLE	**Frequency calibrating cycle register.** Defines how many input signal cycles the calibrator calibrates are in one round. This register is updated into calibrator once the calibrator enable [0] is turned on.
15		FREQ_CALI_AUTORST_EN	**Enables period calibration auto-reset** Period calibration being larger than FREQ_CALI_AUTORST_TH_HIGH or smaller than FREQ_CALI_AUTORST_TH_LOW will trigger ASRC reset.
13		FREQ_CALC_RUNNING	**Shows if frequency calculation is running.** For one round running case, wait for this bit and the CALI_EN bit to become low before frequency result is ready.
12		AUTO_TUNE_FREQ3	**Enables asm_freq_3 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave out.** 0: Disable auto update 1: Enable auto update
11		COMP_FREQ_RES_EN	**Frequency compensation enabling register.** 0: Disable compensation 1: Enable compensation
9:8		FREQ_CALI_SEL	**Calibrator input source selection register. Before modifying this register, make sure the calibrator is turned off.** 2'b00: Use PCM SYNC word 2'b01: Not connected

Bit(s)	Mnemonic	Name	Description
			2'b10: Not connected 2'b11: Not connected
7		FREQ_CALI_BP_DGL	**Bypasses deglitch circuit for calibrator input** 0: No bypass 1: Bypass
6:4		FREQ_CALI_MAX_GWIDTH	**Defines the maximum glitch width of the calibrator input signal. Unit: Calibrator reference clock cycles.**
3		AUTO_TUNE_FREQ2	**Enables asm_freq_2 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave in.** 0: Disable auto update 1: Enable auto update
2		FREQ_CALI_AUTO_RESTART	**Enables calibrator auto restart new calibration while one run is completed. This value will be updated into calibrator once the enabling signal is turned on from off state.** 0: Disable auto restart 1: Enable auto restart
1		CALI_USE_FREQ_OUT	**Selects frequency or period calibration mode** 0: Use period calibration result to update asm_freq_2. Use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2. Use period calibration result to update asm_freq_3
0		CALI_EN	**Enables frequency calibrator** If auto restart is 0, this bit will be cleared while one calibration run is completed. If this bit is set to 0, wait until this bit becomes 0 to make the next run start safely. 0: Disable calibrator 1: Enable calibrator

112208DC AFE_ASRCI4_NEW_CON7 ASRC Config 7 00000659

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALC_DENOMINATOR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALC_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALC_DENOMINATOR	**Determines the denominator for performing period-to-frequency calibration result translation.**

112208E0 AFE_ASRCI4_NEW_CON8 ASRC Config 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PRD_CALI_RESULT_RECORD							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRD_CALI_RESULT_RECORD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		PRD_CALI_RESULT_RECORD	**Period calibration result.** Records the calibration result of the previous round. Writing any value to this register will clear the result.

112208E4 AFE_ASRCI4_NEW_CON9 ASRC Config 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_RESULT							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_RESULT															

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_RESULT	**Frequency calibrator result.** Records the calibration result of previous round. This value is got from the quotient of (FREQ_CALC_DENOMINATOR / PRD_CALI_RESULT) in 1.23 format.

112208E8 AFE_ASRCI4_NEW_CON10 ASRC Config 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									COEFF_SRAM_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COEFF_SRAM_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		COEFF_SRAM_DATA	**Read/Write data port of coefficient SRAM.** Read data have one cycle delay. The coefficients are filled stage by stage: each stage has 6 coefficients. For the 2nd-order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2/1 + (2^shift)*b1*Z^ -1 + (2^shift)*b2*Z^-2" The coefficient should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

112208EC AFE_ASRCI4_NEW_CON11 ASRC Config 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										COEFF_SRAM_ADR						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6:0		COEFF_SRAM_ADR	**Determines the rd/wr address of IIR coefficient SRAM.** Read/Write COEFF_SRAM_DATA will make this register increase by 1.

112208F4 AFE_ASRCI4_NEW_CON13 ASRC Config 13 00001B00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_HIGH							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_HIGH															
Type	RW															
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_HIGH	**High period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

112208F8 AFE_ASRCI4_NEW_CON14 ASRC Config 14 00001800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_LOW							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_LOW															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_LOW	**Low period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

11220940 AFE_ASRCO1_NEW_CON0 ASRC Config 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CHSETo_O16BIT		CHSETo_CLR_IIR_HISTORY	CHSETo_IS_MONO
Type													RW		RW	RW
Reset													0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHSETo_OFS_SEL		CHSETo_IFS_SEL		CHSETo_IIR_EN	CHSETo_IIR_STAGE						CHSET_STR_CLR		CHSET_ON	COEFF_SRAM_CTRL	ASM_ON
Type	RW		RW		RW	RW						RW		RU	RW	RW
Reset	0	0	0	0	0	0	0	0				0		0	0	0

Bit(s)	Mnemonic	Name	Description
19		CHSETo_O16BIT	**Selects 16-bit/32-bit output** 0: 32-bit 1: 16-bit
17		CHSETo_CLR_IIR_HISTORY	**Set to 1 to clear current IIR output history buffer for TX. This register will auto-clear once the histories are cleared.**
16		CHSETo_IS_MONO	**Mono/Stereo selection register**
15:14		CHSETo_OFS_SEL	**Selects output sample rate.** TX: Set to 00 for OFS fix value. RX: Set to 01 for OFS fix value. 2'b00: I2S slave out 2'b01: I2S slave in

Bit(s)	Mnemonic	Name	Description
13:12		CHSETo_IFS_SEL	**Selects input sample rate selection.** TX: Set to 11 for period tracking mode. RX: Set to 10 for frequency tracking mode. 11: I2S slave out 10: I2S slave in
11		CHSETo_IIR_EN	**Enables anti-alias IIR filter for TX.** Set 1 to Turns on anti-alias IIR filter.
10:8		CHSETo_IIR_STAGE	**Anti-alias IIR filter stage for TX.** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
4		CHSET_STR_CLR	**Each channel set clear signal** Set bit 0 to 1 to clear the TX history. Set bit 1 to 1 to clear the RX history. Set bit 2 to 1 to clear the I2S history.
2		CHSET_ON	**Indicates channel set is on currently.**
1		COEFF_SRAM_CTRL	**Controls coefficient SRAM access** 0: Disable access 1: Enable access
0		ASM_ON	**ASRC enabling signal** Turn it on after all configurations are set. 0: Disable ASRC 1: Enable ASRC

11220944 AFE_ASRCO1_NEW_CON ASRC Config 1 00000CB2
1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_o							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_o															

Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_0	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX OFS.

11220948 AFE_ASRCO1_NEW_CON2 ASRC Config 2 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_1							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_1	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX OFS.

1122094C AFE_ASRCO1_NEW_CON3 ASRC Config 3 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_2							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_2	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX IFS.

11220950 AFE_ASRCO1_NEW_CON4 ASRC Config 4 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_3							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_3															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_3	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX IFS.

11220954 AFE_ASRCO1_NEW_CON5 ASRC Config 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RESULT_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		RESULT_SEL	**Selects output** 3'b000: ASRC output 3'b001: Data input 3'b010: CMPF output 3'b011: HBF1 output 3'b100: HBF2 output 3'b101: HBF3 output 3'b110: HBF4 output 3'b111: Each IIR stage output in order

11220958 AFE_ASRCO1_NEW_CON6 ASRC Config 6 00010800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FREQ_CALI_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_EN		FREQ_CALC_RUNNING	AUTO_TUNE_FREQ3	COMP_FREQ_RES_EN		FREQ_CALI_SEL		FREQ_CALI_BP_DGL	FREQ_CALI_MAX_GWIDTH			AUTO_TUNE_FREQ2	FREQ_CALI_AUTO_RESTART	CALI_USE_FREQ_OUT	CALI_EN
Type	RW		RU	RW	RW		RW		RW	RW			RW	RW	RW	RU
Reset	0		0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		FREQ_CALI_CYCLE	**Frequency calibrating cycle register.** Defines how many input signal cycles the calibrator calibrates are in one round. This register is updated into calibrator once the calibrator enable [0] is turned on.
15		FREQ_CALI_AUTORST_EN	**Enables period calibration auto-reset** Period calibration being larger than FREQ_CALI_AUTORST_TH_HIGH or smaller than

Bit(s)	Mnemonic	Name	Description
			FREQ_CALI_AUTORST_TH_LOW will trigger ASRC reset.
13		FREQ_CALC_RUNNING	**Shows if frequency calculation is running.** For one round running case, wait for this bit and the CALI_EN bit to become low before frequency result is ready.
12		AUTO_TUNE_FREQ3	**Enables asm_freq_3 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave out.** 0: Disable auto update 1: Enable auto update
11		COMP_FREQ_RES_EN	**Frequency compensation enabling register.** 0: Disable compensation 1: Enable compensation
9:8		FREQ_CALI_SEL	**Calibrator input source selection register. Before modifying this register, make sure the calibrator is turned off.** 2'b00: Use PCM SYNC word 2'b01: Not connected 2'b10: Not connected 2'b11: Not connected
7		FREQ_CALI_BP_DGL	**Bypasses deglitch circuit for calibrator input** 0: No bypass 1: Bypass
6:4		FREQ_CALI_MAX_GWIDTH	**Defines the maximum glitch width of the calibrator input signal. Unit: Calibrator reference clock cycles.**
3		AUTO_TUNE_FREQ2	**Enables asm_freq_2 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave in.** 0: Disable auto update 1: Enable auto update
2		FREQ_CALI_AUTO_RESTART	**Enables calibrator auto restart new calibration while one run is completed. This value will be updated into calibrator once the enabling signal is turned on from off state.**

Bit(s)	Mnemonic	Name	Description
			0: Disable auto restart 1: Enable auto restart
1		CALI_USE_FREQ_OUT	**Selects frequency or period calibration mode** 0: Use period calibration result to update asm_freq_2. Use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2. Use period calibration result to update asm_freq_3
0		CALI_EN	**Enables frequency calibrator** If auto restart is 0, this bit will be cleared while one calibration run is completed. If this bit is set to 0, wait until this bit becomes 0 to make the next run start safely. 0: Disable calibrator 1: Enable calibrator

1122095C AFE_ASRCO1_NEW_CON7 ASRC Config 7 00000659

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALC_DENOMINATOR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALC_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALC_DENOMINATOR	**Determines the denominator for performing period-to-frequency calibration result translation.**

11220960 AFE_ASRCO1_NEW_CON8 ASRC Config 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PRD_CALI_RESULT_RECORD							

Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRD_CALI_RESULT_RECORD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		PRD_CALI_RESULT_RECORD	**Period calibration result.** Records the calibration result of the previous round. Writing any value to this register will clear the result.

11220964 AFE_ASRCO1_NEW_CON9 ASRC Config 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_RESULT							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_RESULT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_RESULT	**Frequency calibrator result.** Records the calibration result of previous round. This value is got from the quotient of (FREQ_CALC_DENOMINATOR / PRD_CALI_RESULT) in 1.23 format.

11220968 AFE_ASRCO1_NEW_CON10 ASRC Config 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									COEFF_SRAM_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COEFF_SRAM_DATA															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		COEFF_SRAM_DATA	**Read/Write data port of coefficient SRAM.** Read data have one cycle delay. The coefficients are filled stage by stage: each stage has 6 coefficients. For the 2nd-order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2/1 + (2^shift)*b1*Z^-1 + (2^shift)*b2*Z^-2" The coefficient should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

1122096C AFE_ASRCO1_NEW_CON11 ASRC Config 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**COEFF_SRAM_ADR**						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6:0		COEFF_SRAM_ADR	**Determines the rd/wr address of IIR coefficient SRAM.** Read/Write COEFF_SRAM_DATA will make this register increase by 1.

11220974 AFE_ASRCO1_NEW_CON13 ASRC Config 13 00001B00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**FREQ_CALI_AUTORST_TH_HIGH**							
Type									RW							

Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_HIGH															
Type	RW															
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_HIGH	**High period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

11220978 AFE_ASRCO1_NEW_CON14 ASRC Config 14 00001800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_LOW							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_LOW															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_LOW	**Low period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

11220980 AFE_ASRCO2_NEW_CON0 ASRC Config 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CHSETo_O16BIT		CHSETo_CLR_IIR_HISTORY	CHSETo_IS_MONO
Type													RW		RW	RW
Reset													0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CHSETo_OFS_SEL		CHSETo_IFS_SEL		CHSETo_IIR_EN	CHSETo_IIR_STAGE						CHSET_STR_CLR		CHSET_ON	COEFF_SRAM_CTRL	ASM_ON
Type	RW		RW		RW	RW						RW		RU	RW	RW
Reset	0	0	0	0	0	0	0	0				0		0	0	0

Bit(s)	Mnemonic	Name	Description
19		CHSETo_O16BIT	**Selects 16-bit/32-bit output** 0: 32-bit 1: 16-bit
17		CHSETo_CLR_IIR_HISTORY	**Set to 1 to clear current IIR output history buffer for TX. This register will auto-clear once the histories are cleared.**
16		CHSETo_IS_MONO	**Mono/Stereo selection register**
15:14		CHSETo_OFS_SEL	**Selects output sample rate.** TX: Set to 00 for OFS fix value. RX: Set to 01 for OFS fix value. 2'b00: I2S slave out 2'b01: I2S slave in
13:12		CHSETo_IFS_SEL	**Selects input sample rate selection.** TX: Set to 11 for period tracking mode. RX: Set to 10 for frequency tracking mode. 2'b11: I2S slave out 2'b10: I2S slave in
11		CHSETo_IIR_EN	**Enables anti-alias IIR filter for TX.** Set 1 to Turns on anti-alias IIR filter.
10:8		CHSETo_IIR_STAGE	**Anti-alias IIR filter stage for TX.** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
4		CHSET_STR_CLR	**Each channel set clear signal** Set bit 0 to 1 to clear the TX history. Set bit 1 to 1 to clear the RX history. Set bit 2 to 1 to clear the I2S history.

Bit(s)	Mnemonic	Name	Description
2		CHSET_ON	**Indicates channel set is on currently.**
1		COEFF_SRAM_CTRL	**Controls coefficient SRAM access** 0: Disable access 1: Enable access
0		ASM_ON	**ASRC enabling signal** Turn it on after all configurations are set. 0: Disable ASRC 1: Enable ASRC

11220984 AFE_ASRCO2_NEW_CON1 ASRC Config 1 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_0							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_0															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_0	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX OFS.

11220988 AFE_ASRCO2_NEW_CON2 ASRC Config 2 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_1							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	ASM_FREQ_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_1	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX OFS.

1122098C AFE_ASRCO2_NEW_CON3 ASRC Config 3 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_2							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_2	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX IFS.

11220990 AFE_ASRCO2_NEW_CON4 ASRC Config 4 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_3							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_3															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_3	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX IFS.

11220994 AFE_ASRCO2_NEW_CON5 ASRC Config 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**RESULT_SEL**		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		RESULT_SEL	**Selects output** 3'b000: ASRC output 3'b001: Data input 3'b010: CMPF output 3'b011: HBF1 output 3'b100: HBF2 output 3'b101: HBF3 output 3'b110: HBF4 output 3'b111: Each IIR stage output in order

11220998 AFE_ASRCO2_NEW_CON6 ASRC Config 6 00010800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**FREQ_CALI_CYCLE**															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_EN		FREQ_CALC_RUNNING	AUTO_TUNE_FREQ3	COMP_FREQ_RES_EN		FREQ_CALI_SEL		FREQ_CALI_BP_DGL	FREQ_CALI_MAX_GWIDTH			AUTO_TUNE_FREQ2	FREQ_CALI_AUTO_RESTART	CALI_USE_FREQ_OUT	CALI_EN
Type	RW		RU	RW	RW		RW		RW	RW			RW	RW	RW	RU
Reset	0		0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		FREQ_CALI_CYCLE	**Frequency calibrating cycle register.** Defines how many input signal cycles the calibrator calibrates are in one round. This register is updated into calibrator once the calibrator enable [0] is turned on.
15		FREQ_CALI_AUTORST_EN	**Enables period calibration auto-reset** Period calibration being larger than FREQ_CALI_AUTORST_TH_HIGH or smaller than FREQ_CALI_AUTORST_TH_LOW will trigger ASRC reset.
13		FREQ_CALC_RUNNING	**Shows if frequency calculation is running.** For one round running case, wait for this bit and the CALI_EN bit to become low before frequency result is ready.
12		AUTO_TUNE_FREQ3	**Enables asm_freq_3 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave out.** 0: Disable auto update 1: Enable auto update
11		COMP_FREQ_RES_EN	**Frequency compensation enabling register.** 0: Disable compensation 1: Enable compensation
9:8		FREQ_CALI_SEL	**Calibrator input source selection register. Before modifying this register, make sure the calibrator is turned off.** 2'b00: Use PCM SYNC word 2'b01: Not connected

Bit(s)	Mnemonic	Name	Description
			2'b10: Not connected 2'b11: Not connected
7		FREQ_CALI_BP_DGL	**Bypasses deglitch circuit for calibrator input** 0: No bypass 1: Bypass
6:4		FREQ_CALI_MAX_GWIDTH	**Defines the maximum glitch width of the calibrator input signal. Unit: Calibrator reference clock cycles.**
3		AUTO_TUNE_FREQ2	**Enables asm_freq_2 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave in.** 0: Disable auto update 1: Enable auto update
2		FREQ_CALI_AUTO_RESTART	**Enables calibrator auto restart new calibration while one run is completed. This value will be updated into calibrator once the enabling signal is turned on from off state.** 0: Disable auto restart 1: Enable auto restart
1		CALI_USE_FREQ_OUT	**Selects frequency or period calibration mode** 0: Use period calibration result to update asm_freq_2. Use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2. Use period calibration result to update asm_freq_3
0		CALI_EN	**Enables frequency calibrator** If auto restart is 0, this bit will be cleared while one calibration run is completed. If this bit is set to 0, wait until this bit becomes 0 to make the next run start safely. 0: Disable calibrator 1: Enable calibrator

1122099C	AFE_ASRCO2_NEW_CON7	ASRC Config 7	00000659

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALC_DENOMINATOR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALC_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALC_DENOMINATOR	**Determines the denominator for performing period-to-frequency calibration result translation.**

112209A0 AFE_ASRCO2_NEW_CON8 ASRC Config 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PRD_CALI_RESULT_RECORD							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRD_CALI_RESULT_RECORD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		PRD_CALI_RESULT_RECORD	**Period calibration result.** Records the calibration result of the previous round. Writing any value to this register will clear the result.

112209A4 AFE_ASRCO2_NEW_CON9 ASRC Config 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_RESULT							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_RESULT															

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_RESULT	**Frequency calibrator result.** Records the calibration result of previous round. This value is got from the quotient of (FREQ_CALC_DENOMINATOR / PRD_CALI_RESULT) in 1.23 format.

112209A8 AFE_ASRCO2_NEW_CON10 ASRC Config 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									COEFF_SRAM_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COEFF_SRAM_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		COEFF_SRAM_DATA	**Read/Write data port of coefficient SRAM.** Read data have one cycle delay. The coefficients are filled stage by stage: each stage has 6 coefficients. For the 2nd-order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2/1 + (2^shift)*b1*Z^ -1 + (2^shift)*b2*Z^-2" The coefficient should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

112209AC AFE_ASRCO2_NEW_CON11 ASRC Config 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										COEFF_SRAM_ADR						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6:0		COEFF_SRAM_ADR	**Determines the rd/wr address of IIR coefficient SRAM.** Read/Write COEFF_SRAM_DATA will make this register increase by 1.

112209B4 AFE_ASRCO2_NEW_CON13 ASRC Config 13 00001B00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_HIGH							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_HIGH															
Type	RW															
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_HIGH	**High period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

112209B8 AFE_ASRCO2_NEW_CON14 ASRC Config 14 00001800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_LOW							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_LOW															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_LOW	**Low period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

112209C0 AFE_ASRCO3_NEW_CON0 ASRC Config 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CHSETo_O16BIT		CHSETo_CLR_IIR_HISTORY	CHSETo_IS_MONO
Type													RW		RW	RW
Reset													0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHSETo_OFS_SEL		CHSETo_IFS_SEL		CHSETo_IIR_EN	CHSETo_IIR_STAGE						CHSET_STR_CLR		CHSET_ON	COEFF_SRAM_CTRL	ASM_ON
Type	RW		RW		RW	RW						RW		RU	RW	RW
Reset	0	0	0	0	0	0	0	0				0		0	0	0

Bit(s)	Mnemonic	Name	Description
19		CHSETo_O16BIT	**Selects 16-bit/32-bit output** 0: 32-bit 1: 16-bit
17		CHSETo_CLR_IIR_HISTORY	**Set to 1 to clear current IIR output history buffer for TX. This register will auto-clear once the histories are cleared.**
16		CHSETo_IS_MONO	**Mono/Stereo selection register**
15:14		CHSETo_OFS_SEL	**Selects output sample rate.** TX: Set to 00 for OFS fix value. RX: Set to 01 for OFS fix value. 2'b00: I2S slave out 2'b01: I2S slave in

Bit(s)	Mnemonic	Name	Description
13:12		CHSETo_IFS_SEL	**Selects input sample rate selection.** TX: Set to 11 for period tracking mode. RX: Set to 10 for frequency tracking mode. 2'b11: I2S slave out 2'b10: I2S slave in
11		CHSETo_IIR_EN	**Enables anti-alias IIR filter for TX.** Set 1 to Turns on anti-alias IIR filter.
10:8		CHSETo_IIR_STAGE	**Anti-alias IIR filter stage for TX.** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
4		CHSET_STR_CLR	**Each channel set clear signal** Set bit 0 to 1 to clear the TX history. Set bit 1 to 1 to clear the RX history. Set bit 2 to 1 to clear the I2S history.
2		CHSET_ON	**Indicates channel set is on currently.**
1		COEFF_SRAM_CTRL	**Controls coefficient SRAM access** 0: Disable access 1: Enable access
0		ASM_ON	**ASRC enabling signal** Turn it on after all configurations are set. 0: Disable ASRC 1: Enable ASRC

112209C4 AFE_ASRCO3_NEW_CON ASRC Config 1 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_0							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_0															

Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_0	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX OFS.

112209C8 AFE_ASRCO3_NEW_CON2 ASRC Config 2 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_1							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_1	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX OFS.

112209CC AFE_ASRCO3_NEW_CON3 ASRC Config 3 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_2							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_2	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX IFS.

112209D0 AFE_ASRCO3_NEW_CON4 ASRC Config 4 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_3							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_3															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_3	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX IFS.

112209D4 AFE_ASRCO3_NEW_CON5 ASRC Config 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RESULT_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		RESULT_SEL	**Selects output** 3'b000: ASRC output 3'b001: Data input 3'b010: CMPF output 3'b011: HBF1 output 3'b100: HBF2 output 3'b101: HBF3 output 3'b110: HBF4 output 3'b111: Each IIR stage output in order

112209D8 AFE_ASRCO3_NEW_CON6 ASRC Config 6 00010800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FREQ_CALI_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_EN		FREQ_CALC_RUNNING	AUTO_TUNE_FREQ3	COMP_FREQ_RES_EN		FREQ_CALI_SEL		FREQ_CALI_BP_DGL	FREQ_CALI_MAX_GWIDTH			AUTO_TUNE_FREQ2	FREQ_CALI_AUTO_RESTART	CALI_USE_FREQ_OUT	CALI_EN
Type	RW		RU	RW	RW		RW		RW	RW			RW	RW	RW	RU
Reset	0		0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		FREQ_CALI_CYCLE	**Frequency calibrating cycle register.** Defines how many input signal cycles the calibrator calibrates are in one round. This register is updated into calibrator once the calibrator enable [0] is turned on.
15		FREQ_CALI_AUTORST_EN	**Enables period calibration auto-reset** Period calibration being larger than FREQ_CALI_AUTORST_TH_HIGH or smaller than

Bit(s)	Mnemonic	Name	Description
			FREQ_CALI_AUTORST_TH_LOW will trigger ASRC reset.
13		FREQ_CALC_RUNNING	**Shows if frequency calculation is running.** For one round running case, wait for this bit and the CALI_EN bit to become low before frequency result is ready.
12		AUTO_TUNE_FREQ3	**Enables asm_freq_3 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave out.** 0: Disable auto update 1: Enable auto update
11		COMP_FREQ_RES_EN	**Frequency compensation enabling register.** 0: Disable compensation 1: Enable compensation
9:8		FREQ_CALI_SEL	**Calibrator input source selection register. Before modifying this register, make sure the calibrator is turned off.** 2'b00: Use PCM SYNC word 2'b01: Not connected 2'b10: Not connected 2'b11: Not connected
7		FREQ_CALI_BP_DGL	**Bypasses deglitch circuit for calibrator input** 0: No bypass 1: Bypass
6:4		FREQ_CALI_MAX_GWIDTH	**Defines the maximum glitch width of the calibrator input signal. Unit: Calibrator reference clock cycles.**
3		AUTO_TUNE_FREQ2	**Enables asm_freq_2 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave in.** 0: Disable auto update 1: Enable auto update
2		FREQ_CALI_AUTO_RESTART	**Enables calibrator auto restart new calibration while one run is completed. This value will be updated into calibrator once the enabling signal is turned on from off state.**

Bit(s)	Mnemonic	Name	Description
			0: Disable auto restart 1: Enable auto restart
1		CALI_USE_FREQ_OUT	**Selects frequency or period calibration mode** 0: Use period calibration result to update asm_freq_2. Use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2. Use period calibration result to update asm_freq_3
0		CALI_EN	**Enables frequency calibrator** If auto restart is 0, this bit will be cleared while one calibration run is completed. If this bit is set to 0, wait until this bit becomes 0 to make the next run start safely. 0: Disable calibrator 1: Enable calibrator

112209DC AFE_ASRCO3_NEW_CON7 ASRC Config 7 00000659

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALC_DENOMINATOR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALC_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALC_DENOMINATOR	**Determines the denominator for performing period-to-frequency calibration result translation.**

112209E0 AFE_ASRCO3_NEW_CON8 ASRC Config 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PRD_CALI_RESULT_RECORD							

Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRD_CALI_RESULT_RECORD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		PRD_CALI_RESULT_RECORD	**Period calibration result.** Records the calibration result of the previous round. Writing any value to this register will clear the result.

112209E4 AFE_ASRCO3_NEW_CON9 ASRC Config 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_RESULT							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_RESULT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_RESULT	**Frequency calibrator result.** Records the calibration result of previous round. This value is got from the quotient of (FREQ_CALC_DENOMINATOR / PRD_CALI_RESULT) in 1.23 format.

112209E8 AFE_ASRCO3_NEW_CON10 ASRC Config 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									COEFF_SRAM_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COEFF_SRAM_DATA															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		COEFF_SRAM_DATA	**Read/Write data port of coefficient SRAM.** Read data have one cycle delay. The coefficients are filled stage by stage: each stage has 6 coefficients. For the 2nd-order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2/1 + (2^shift)*b1*Z^-1 + (2^shift)*b2*Z^-2" The coefficient should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

112209EC AFE_ASRCO3_NEW_CON11 ASRC Config 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**COEFF_SRAM_ADR**						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6:0		COEFF_SRAM_ADR	**Determines the rd/wr address of IIR coefficient SRAM.** Read/Write COEFF_SRAM_DATA will make this register increase by 1.

112209F4 AFE_ASRCO3_NEW_CON13 ASRC Config 13 00001B00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**FREQ_CALI_AUTORST_TH_HIGH**							
Type									RW							

Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_HIGH															
Type	RW															
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_HIGH	**High period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

112209F8 AFE_ASRCO3_NEW_CON14 ASRC Config 14 00001800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_LOW							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_LOW															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_LOW	**Low period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

11220A00 AFE_ASRCO4_NEW_CON0 ASRC Config 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CHSETo_O16BIT		CHSETo_CLR_IIR_HISTORY	CHSETo_IS_MONO
Type													RW		RW	RW
Reset													0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CHSETo_OFS_SEL		CHSETo_IFS_SEL		CHSETo_IIR_EN	CHSETo_IIR_STAGE						CHSET_STR_CLR		CHSET_ON	COEFF_SRAM_CTRL	ASM_ON
Type	RW		RW		RW	RW						RW		RU	RW	RW
Reset	0	0	0	0	0	0	0	0				0		0	0	0

Bit(s)	Mnemonic	Name	Description
19		CHSETo_O16BIT	**Selects 16-bit/32-bit output** 0: 32-bit 1: 16-bit
17		CHSETo_CLR_IIR_HISTORY	**Set to 1 to clear current IIR output history buffer for TX. This register will auto-clear once the histories are cleared.**
16		CHSETo_IS_MONO	**Mono/Stereo selection register**
15:14		CHSETo_OFS_SEL	**Selects output sample rate.** TX: Set to 00 for OFS fix value. RX: Set to 01 for OFS fix value. 2'b00: I2S slave out 2'b01: I2S slave in
13:12		CHSETo_IFS_SEL	**Selects input sample rate selection.** TX: Set to 11 for period tracking mode. RX: Set to 10 for frequency tracking mode. 2'b11: I2S slave out 2'b10: I2S slave in
11		CHSETo_IIR_EN	**Enables anti-alias IIR filter for TX.** Set 1 to Turns on anti-alias IIR filter.
10:8		CHSETo_IIR_STAGE	**Anti-alias IIR filter stage for TX.** Defines how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 orders are supported.
4		CHSET_STR_CLR	**Each channel set clear signal** Set bit 0 to 1 to clear the TX history. Set bit 1 to 1 to clear the RX history. Set bit 2 to 1 to clear the I2S history.

Bit(s)	Mnemonic	Name	Description
2		CHSET_ON	**Indicates channel set is on currently.**
1		COEFF_SRAM_CTRL	**Controls coefficient SRAM access** 0: Disable access 1: Enable access
0		ASM_ON	**ASRC enabling signal** Turn it on after all configurations are set. 0: Disable ASRC 1: Enable ASRC

11220A04 AFE_ASRCO4_NEW_CON1 ASRC Config 1 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_0							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_0															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_0	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX OFS.

11220A08 AFE_ASRCO4_NEW_CON2 ASRC Config 2 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_1							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	ASM_FREQ_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_1	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX OFS.

11220A0C AFE_ASRCO4_NEW_CON3 ASRC Config 3 00400000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_2							
Type									RW							
Reset									0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_2	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for RX IFS.

11220A10 AFE_ASRCO4_NEW_CON4 ASRC Config 4 00000CB2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASM_FREQ_3							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASM_FREQ_3															
Type	RW															
Reset	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
23:0		ASM_FREQ_3	**Frequency palette.** The frequency palette for each channel set to define its input frequency and output frequency. Default is set for TX IFS.

11220A14 AFE_ASRCO4_NEW_CON5 ASRC Config 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**RESULT_SEL**		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		RESULT_SEL	**Selects output** 3'b000: ASRC output 3'b001: Data input 3'b010: CMPF output 3'b011: HBF1 output 3'b100: HBF2 output 3'b101: HBF3 output 3'b110: HBF4 output 3'b111: Each IIR stage output in order

11220A18 AFE_ASRCO4_NEW_CON6 ASRC Config 6 00010800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**FREQ_CALI_CYCLE**															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_EN		FREQ_CALC_RUNNING	AUTO_TUNE_FREQ3	COMP_FREQ_RES_EN		FREQ_CALI_SEL		FREQ_CALI_BP_DGL	FREQ_CALI_MAX_GWIDTH			AUTO_TUNE_FREQ2	FREQ_CALI_AUTO_RESTART	CALI_USE_FREQ_OUT	CALI_EN
Type	RW		RU	RW	RW		RW		RW	RW			RW	RW	RW	RU
Reset	0		0	0	1		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		FREQ_CALI_CYCLE	**Frequency calibrating cycle register.** Defines how many input signal cycles the calibrator calibrates are in one round. This register is updated into calibrator once the calibrator enable [0] is turned on.
15		FREQ_CALI_AUTORST_EN	**Enables period calibration auto-reset** Period calibration being larger than FREQ_CALI_AUTORST_TH_HIGH or smaller than FREQ_CALI_AUTORST_TH_LOW will trigger ASRC reset.
13		FREQ_CALC_RUNNING	**Shows if frequency calculation is running.** For one round running case, wait for this bit and the CALI_EN bit to become low before frequency result is ready.
12		AUTO_TUNE_FREQ3	**Enables asm_freq_3 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave out.** 0: Disable auto update 1: Enable auto update
11		COMP_FREQ_RES_EN	**Frequency compensation enabling register.** 0: Disable compensation 1: Enable compensation
9:8		FREQ_CALI_SEL	**Calibrator input source selection register. Before modifying this register, make sure the calibrator is turned off.** 2'b00: Use PCM SYNC word 2'b01: Not connected

Bit(s)	Mnemonic	Name	Description
			2'b10: Not connected 2'b11: Not connected
7		FREQ_CALI_BP_DGL	**Bypasses deglitch circuit for calibrator input** 0: No bypass 1: Bypass
6:4		FREQ_CALI_MAX_GWIDTH	**Defines the maximum glitch width of the calibrator input signal. Unit: Calibrator reference clock cycles.**
3		AUTO_TUNE_FREQ2	**Enables asm_freq_2 auto update with the calibrator result once the calibrator completes one round. Set to 1 for I2S slave in.** 0: Disable auto update 1: Enable auto update
2		FREQ_CALI_AUTO_RESTART	**Enables calibrator auto restart new calibration while one run is completed. This value will be updated into calibrator once the enabling signal is turned on from off state.** 0: Disable auto restart 1: Enable auto restart
1		CALI_USE_FREQ_OUT	**Selects frequency or period calibration mode** 0: Use period calibration result to update asm_freq_2. Use frequency calibration result to update asm_freq_3 1: Use frequency calibration result to update asm_freq_2. Use period calibration result to update asm_freq_3
0		CALI_EN	**Enables frequency calibrator** If auto restart is 0, this bit will be cleared while one calibration run is completed. If this bit is set to 0, wait until this bit becomes 0 to make the next run start safely. 0: Disable calibrator 1: Enable calibrator

11220A1C	AFE_ASRCO4_NEW_CON7	ASRC Config 7	00000659

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALC_DENOMINATOR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALC_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALC_DENOMINATOR	**Determines the denominator for performing period-to-frequency calibration result translation.**

11220A20 AFE_ASRCO4_NEW_CON8 ASRC Config 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PRD_CALI_RESULT_RECORD							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRD_CALI_RESULT_RECORD															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		PRD_CALI_RESULT_RECORD	**Period calibration result.** Records the calibration result of the previous round. Writing any value to this register will clear the result.

11220A24 AFE_ASRCO4_NEW_CON9 ASRC Config 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_RESULT							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_RESULT															

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_RESULT	**Frequency calibrator result.** Records the calibration result of previous round. This value is got from the quotient of (FREQ_CALC_DENOMINATOR / PRD_CALI_RESULT) in 1.23 format.

11220A28 AFE_ASRCO4_NEW_CON10 ASRC Config 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									COEFF_SRAM_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COEFF_SRAM_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		COEFF_SRAM_DATA	**Read/Write data port of coefficient SRAM.** Read data have one cycle delay. The coefficients are filled stage by stage: each stage has 6 coefficients. For the 2nd-order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2/1 + (2^shift)*b1*Z^ -1 + (2^shift)*b2*Z^-2" The coefficient should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

11220A2C AFE_ASRCO4_NEW_CON11 ASRC Config 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										COEFF_SRAM_ADR						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6:0		COEFF_SRAM_ADR	**Determines the rd/wr address of IIR coefficient SRAM.** Read/Write COEFF_SRAM_DATA will make this register increase by 1.

11220A34 AFE_ASRCO4_NEW_CON13 ASRC Config 13 00001B00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_HIGH							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_HIGH															
Type	RW															
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_HIGH	**High period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

11220A38 AFE_ASRCO4_NEW_CON14 ASRC Config 14 00001800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FREQ_CALI_AUTORST_TH_LOW							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FREQ_CALI_AUTORST_TH_LOW															
Type	RW															
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		FREQ_CALI_AUTORST_TH_LOW	**Low period calibration threshold to trigger autoreset** Enabling FREQ_CALI_AUTORST_EN is required.

11220B00 ASRC_GEN_CONF ASRC_GEN_CONF 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					USE_OUT_MAY_FULL							CH_CNTX_SWEN				CH_CLEAR
Type					RW							RW				RW
Reset					0							0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CH_EN	DSP_CTRL_COEFF_SRAM		ASRC_BUSY	ASRC_EN								
Type				RW	RW		RO	RW								
Reset				0	0		0	0								

Bit(s)	Mnemonic	Name	Description
27		USE_OUT_MAY_FULL	**Setting 1 makes ASM update status when output is going to be full.** 0: Don't use out_may_full 1.: Use out_may_full
20		CH_CNTX_SWEN	**Context switch disabler for CH-set 0.** Disable context switch of each CH-set, remember to stop each CH-set first by set related enable before using this registers.
16		CH_CLEAR	**CH-set clear signal for CH-set 0,** set to 1 means the chset will clear history at next run.
12		CH_EN	**CH-set enable signal for CH-set 0,** This register controls which CH-set should be execute.

Bit(s)	Mnemonic	Name	Description
11		DSP_CTRL_COEFF_SRAM	**Setting 1 makes RISC can access coefficient SRAM through ASRC_IIR_CRAM_ADDR and ASRC_IIR_CRAM_DATA.**
9		ASRC_BUSY	**asrc busy flag.** 1 means chseto is running.
8		ASRC_EN	**asrc enable.** The central enable signal, should be turned on after all configration are set.

11220B04 ASRC_IER ASRC_IER 00101000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												IBUF_EMPTY_INTEN				IBUF_AMOUNT_INTEN
Type												RW				RW
Reset												1				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBUF_OV_INTEN				OBUF_AMOUNT_INTEN								
Type				RW				RW								
Reset				1				0								

Bit(s)	Mnemonic	Name	Description
20		IBUF_EMPTY_INTEN	**input buffer empty interrupt enable for CH-set 0.**
16		IBUF_AMOUNT_INTEN	**input buffer amount interrupt enable for CH-set 0.**
12		OBUF_OV_INTEN	**output buffer overflow interupt enable for CH-set 0.**
8		OBUF_AMOUNT_INTEN	**output buffer amount interupt enable for CH-set 0.**

11220B08 ASRC_IFR ASRC_IFR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												IBUF_EMPTY_INT				IBUF_AMOUNT_INT
Type												RW				RW
Reset												0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBUF_OV_INT				OBUF_AMOUNT_INT								
Type				RW				RW								
Reset				0				0								

Bit(s)	Mnemonic	Name	Description
20		IBUF_EMPTY_INT	**Input Buffer Empty Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related input buffer is empty. Write 1 to the related bit will clear it.
16		IBUF_AMOUNT_INT	**Input left amount reached Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related input buffer left amount reached the dedicated value. Write 1 to the related bit will clear it.
12		OBUF_OV_INT	**Output Buffer Full Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related output buffer is full. Write buffer full will make the whole system hang, please resolve it as soon as possible. Write 1 to the related bit will clear it.
8		OBUF_AMOUNT_INT	**Output Amount Reached Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related channel pair output amount meets requirement. Write 1 to the related bit will clear it.

11220B10 ASRC_CH01_CNFG ASRC_CH01_CNFG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CLR_IIR_BUF	OBIT_WIDTH	IBIT_WIDTH	MONO	OFS		IFS	
Type									RW	RW	RW	RW	RW		RW	
Reset									0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLAC_AMOUNT								IIR_EN	IIR_STAGE						
Type	RW								RW	RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
23		CLR_IIR_BUF	**Set 1 to clear current IIR output history buffer. This register will auto-clear once the histories are cleared.**
22		OBIT_WIDTH	**Bit-width Selection for Output** 0: 32-bit 1: 16-bit
21		IBIT_WIDTH	**Bit-width Selection for Input** 0: 32-bit 1: 16-bit
20		MONO	**Mono/Stereo Selection Regsiter** 0: This channel pair is stereo. 1: This channel pair is mono.
19:18		OFS	**Output Sample Rate Selection.** set 0, 1, 2 to choose the realted frequency on palette.
17:16		IFS	**Input Sample Rate Selection.** set 0, 1, 2 to choose the realted frequency on palette.
15:8		CLAC_AMOUNT	**Calculation amount.** Define how many 128-bit output the related channel pair should calculate at each turn.
7		IIR_EN	**Anti-alias IIR filter enable.** Set 1 to turn on the anti-alias IIR filter.
6:4		IIR_STAGE	**Anti-alias IIR filter stage.** Define how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 order is supported.

11220B20 ASRC_FREQUENCY_0 ASRC_FREQUENCY_0 00F00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_0							
Type									RW							
Reset									1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_0	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220B24 ASRC_FREQUENCY_1 ASRC_FREQUENCY_1 00DC8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_1							
Type									RW							
Reset									1	1	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_1															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_1	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220B28 ASRC_FREQUENCY_2 ASRC_FREQUENCY_2 00A00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_2							
Type									RW							
Reset									1	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_2															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_2	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220B2C ASRC_FREQUENCY_3 ASRC_FREQUENCY_3 00DC8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_3							
Type									RW							
Reset									1	1	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_3															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_3	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220B30 ASRC_IBUF_SADR ASRC_IBUF_SADR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		IBUF_SADR	**Input Buffer Start Address.** The start address of input buffer, in byte unit and128-bit alignment.

Bit(s)	Mnemonic	Name	Description

11220B34 ASRC_IBUF_SIZE ASRC_IBUF_SIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CH_IBUF_SIZE			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH_IBUF_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
19:4		CH_IBUF_SIZE	**Input Channel Size.** The input buffer size for each channel, in byte unit and 128-bit alignment. Each channel uses the same size an is circular.

11220B38 ASRC_OBUF_SADR ASRC_OBUF_SADR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		OBUF_SADR	**Output Buffer Start Address.** The start address of output buffer, in byte unit and128-bit alignment.

11220B3C ASRC_OBUF_SIZE ASRC_OBUF_SIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name													CH_OBUF_SIZE			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH_OBUF_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
19:4		CH_OBUF_SIZE	**Output Channel Size.** The output buffer size per channel, in byte unit and128-bit alignment. Each channel uses the same size an is circular.

11220B40 ASRC_CH01_IBUF_RDPNT ASRC_CH01_IBUF_RDPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_IBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_IBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_IBUF_RDPNT	**IBUF Read Address Register. In byte unit and128-bit alignment.** Current input buffer read address for each channel pair. For stereo channe, this value is related to first channel.

11220B50 ASRC_CH01_IBUF_WRPNT ASRC_CH01_IBUF_WRPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_IBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_IBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_IBUF_WRPNT	**IBUF Write Address Register. In byte unit and128-bit alignment.** Current input buffer write address for each channel pair, this register is used to prevent ASRC read the invalid data. For stereo channel, this value is related to first channel.

11220B60 ASRC_CH01_OBUF_WRPNT ASRC_CH01_OBUF_WRPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_OBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_OBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_OBUF_WRPNT	**OBUF Write Address Register. In byte unit and 32-bit alignment.** Current output buffer write address for each channel pair. For stereo channe, this value is related to first channel.

11220B70 ASRC_CH01_OBUF_RDPNT ASRC_CH01_OBUF_RDPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_OBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_OBUF_RDPNT															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_OBUF_RDPNT	**OBUF Read Address Register. In byte unit and128-bit alignment.** Current output buffer read address for each channel pair, this register is used to prevent ASRC write the un-read output. For stereo channe, this value is related to first channel.

11220B80 ASRC_IBUF_INTR_CNT0 ASRC_IBUF_INTR_CNT0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH01_IBUF_INTR_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		CH01_IBUF_INTR_CNT	**Channel Pair01 Iutput Buffer Amount Interrupt Register** When the related input buffer left less than this amount (in 512-bit unit) of input data. It will rise the input buffer amount flag.

11220B88 ASRC_OBUF_INTR_CNT0 ASRC_OBUF_INTR_CNT0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH01_OBUF_INTR_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		CH01_OBUF_INTR_CNT	**Channel Pair01 Output Buffer Amount Interrupt Register** When the related onput buffer contain more than this amount (in 512-bit unit) of output data. It will rise the output buffer amount flag.

11220B90 ASRC_BAK_REG ASRC_BAK_REG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**RESULT_SEL**		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		RESULT_SEL	**Output Selection** 000: ASRC output 001: Data input 010: CMPF output 011: HBF1 output 100: HBF2 output 101: HBF3 output 110: HBF4 output 111: Each stage IIR output in order.

11220B94 ASRC_FREQ_CALI_CTRL ASRC_FREQ_CALI_CTRL 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												**FREQ_CALC_BUSY**	**COMP_FREQ_RES_EN**		**SRC_SEL**	

Type												RW	RW		RW	
Reset												0	1		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYPASS_DEGLITCH	MAX_GWIDTH			AUTO_FS2_UPDATE	AUTO_RESTART	FREQ_UPDATE_FS2	CALI_EN								
Type	RW	RW			RW	RW	RW	RW								
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
20		FREQ_CALC_BUSY	**This bit shows if the frequency calculation is running. For one round running case, user should wait this bit and CALI_EN bit become low and then the frequency result will be ready.**
19		COMP_FREQ_RES_EN	**Frequency compenstation enabling register.**
17:16		SRC_SEL	**The calibrator input source selection register. Before modifying this register, please make sure the calibrator is turned off.**
15		BYPASS_DEGLITCH	**Set 1 to bypass the deglitch circuit for calibrator input.**
14:12		MAX_GWIDTH	**Define the maximum glitchwidth of the calibrator input signal, in unit of calibrator reference clock cycle.**
11		AUTO_FS2_UPDATE	**set 1 to enalbe ASRC_FREQUENCY_2 auto update with the calibrator result once the calibrator complete one round.**
10		AUTO_RESTART	**Auto restart. set 1 make the calibrator auto restart new calibration while one run completes.** This value will be updated into calibrator once the enable signal is turned on from off state.
9		FREQ_UPDATE_FS2	**0: Use period calibration result to update FS2.** 1: Use frequency calibration result to update FS2.
8		CALI_EN	**Set 1 to enable frequency clibrator. If auto restart is 0, this bit will be cleared while one clibration run is completed.** If you set 0 to close calibrator, please wait until this bit become 0 to make next run can be started safely.

11220B98 ASRC_FREQ_CALI_CYC ASRC_FREQ_CALI_CYC 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQ_CALI_CYC							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQ_CALI_CYC															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
23:8		ASRC_FREQ_CALI_CYC	**ASRC Frequency Calibrating Cycle Register** Define how many input signal cycles the calibrator calibrates in one round. This register is updated into calibrator once the calibrator enbale CALI_EN(ASRC_FREQ_CALI_CTRL[8]) is turned on from off state.

11220B9C ASRC_PRD_CALI_RESULT ASRC_PRD_CALI_RESULT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_PRD_CALI_RESULT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_PRD_CALI_RESULT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_PRD_CALI_RESULT	**ASRC Period Calibrator Result** Record the calibration result of previous round. Write any value to this register will clear the result.

11220BA0 ASRC_FREQ_CALI_RESULT ASRC_FREQ_CALI_RESULT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name									ASRC_FREQ_CALI_RESULT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQ_CALI_RESULT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQ_CALI_RESULT	**ASRC Frequency Calibrator Result** Record the calibration result of previous round. This value is got from the quotient of (ASRC_FCALC_DENOMINATOR / ASRC_PRD_CALI_RESULT), in 1.23 format. Write any value to this register will clear the result.

11220BD8 ASRC_CALI_DENOMINATOR ASRC_CALI_DENOMINATOR 00800000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_CALI_DENOMINATOR							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CALI_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_CALI_DENOMINATOR	**Determine the denominator for performing period-to-frequency calibration result translation.**

11220BE0 ASRC_MAX_OUT_PER_IN0 ASRC_MAX_OUT_PER_IN0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CH01_MAX_OUT_PER_IN											
Type					RW											
Reset					0	0	0	0								

Bit(s)	Mnemonic	Name	Description
11:8		CH01_MAX_OUT_PER_IN	**CH01 Maximum output amount per input.** Tell ASRC each CH-set translation information to prevent output full. This value should be "ceil(OFs / IFs)". The ASRC support up to 8x up-sample and ~16x down-sample.

11220BE8 ASRC_IN_BUF_MON0 ASRC_IN_BUF_MON0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_IN_BUF_MON0															
Type	RO															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		ASRC_IN_BUF_MON0	**mon**

11220BEC ASRC_IN_BUF_MON1 ASRC_IN_BUF_MON1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_IN_BUF_MON1															
Type	RO															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		ASRC_IN_BUF_MON1	**mon**

11220BF0 ASRC_IIR_CRAM_ADDR ASRC_IIR_CRAM_ADDR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_IIR_CRAM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		ASRC_IIR_CRAM_ADDR	**Determine the read/write address of IIR coefficient SRAM. Read/Write ASRC_IIR_CRAM_DATA will make this register increase by 1.**

11220BF4 ASRC_IIR_CRAM_DATA ASRC_IIR_CRAM_DATA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_IIR_CRAM_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_IIR_CRAM_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_IIR_CRAM_DATA	**Read/Write data port of the coefficient SRAM. Read data have one cycle delay.** The coefficients are filled stage by stage, each stage has 6 coefficient. For the 2nd order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2 /

Bit(s)	Mnemonic	Name	Description
			1 + (2^shift)*b1*Z^-1 + (2^shift)*b2*Z^-2" The coefficent should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

11220BF8 ASRC_OUT_BUF_MON0 ASRC_OUT_BUF_MON0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WDLE_CNT**															**ASRC_WRITE_DONE**
Type	RO															RO
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Mnemonic	Name	Description
15:8		WDLE_CNT	**Inticate number of not-finished 128-bit ASRC DRAM write data.**
0		ASRC_WRITE_DONE	**Inticate all ASRC write data to DRAM are done.**

11220BFC ASRC_OUT_BUF_MON1 ASRC_OUT_BUF_MON1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ASRC_WR_ADR**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ASRC_WR_ADR**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_WR_ADR	**ASRC DRAM write address.**

Bit(s)	Mnemonic	Name	Description

11220C00 ASRC2_GEN_CONF ASRC_GEN_CONF 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					USE_OUT_MAY_FULL							CH_CNTX_SWEN				CH_CLEAR
Type					RW							RW				RW
Reset					0							0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CH_EN	DSP_CTRL_COEFF_SRAM		ASRC_BUSY	ASRC_EN								
Type				RW	RW		RO	RW								
Reset				0	0		0	0								

Bit(s)	Mnemonic	Name	Description
27		USE_OUT_MAY_FULL	**Setting 1 makes ASM update status when output is going to be full.** 0: Don't use out_may_full 1.: Use out_may_full
20		CH_CNTX_SWEN	**Context switch disabler for CH-set 0.** Disable context switch of each CH-set, remember to stop each CH-set first by set related enable before using this registers.
16		CH_CLEAR	**CH-set clear signal for CH-set 0,** set to 1 means the chset will clear history at next run.
12		CH_EN	**CH-set enable signal for CH-set 0,** This register controls which CH-set should be execute.
11		DSP_CTRL_COEFF_SRAM	**Setting 1 makes RISC can access coefficient SRAM through ASRC_IIR_CRAM_ADDR and ASRC_IIR_CRAM_DATA.**
9		ASRC_BUSY	**asrc busy flag.** 1 means chset0 is running.

Bit(s)	Mnemonic	Name	Description
8		ASRC_EN	**asrc enable.** The central enable signal, should be turned on after all configration are set.

11220C04 ASRC2_IER ASRC_IER 00101000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												IBUF_EMPTY_INTEN				IBUF_AMOUNT_INTEN
Type												RW				RW
Reset												1				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBUF_OV_INTEN				OBUF_AMOUNT_INTEN								
Type				RW				RW								
Reset				1				0								

Bit(s)	Mnemonic	Name	Description
20		IBUF_EMPTY_INTEN	**input buffer empty interrupt enable for CH-set 0.**
16		IBUF_AMOUNT_INTEN	**input buffer amount interrupt enable for CH-set 0.**
12		OBUF_OV_INTEN	**output buffer overflow interupt enable for CH-set 0.**
8		OBUF_AMOUNT_INTEN	**output buffer amount interupt enable for CH-set 0.**

11220C08 ASRC2_IFR ASRC_IFR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												IBUF_EMPTY_INT				IBUF_AMOUNT_INT

Type												RW				RW
Reset												0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBUF_OV_INT				OBUF_AMOUNT_INT								
Type				RW				RW								
Reset				0				0								

Bit(s)	Mnemonic	Name	Description
20		IBUF_EMPTY_INT	**Input Buffer Empty Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related input buffer is empty. Write 1 to the related bit will clear it.
16		IBUF_AMOUNT_INT	**Input left amount reached Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related input buffer left amount reached the dedicated value. Write 1 to the related bit will clear it.
12		OBUF_OV_INT	**Output Buffer Full Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related output buffer is full. Write buffer full will make the whole system hang, please resolve it as soon as possible. Write 1 to the related bit will clear it.
8		OBUF_AMOUNT_INT	**Output Amount Reached Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related channel pair output amount meets requirement. Write 1 to the related bit will clear it.

11220C10 ASRC2_CH01_CNFG ASRC_CH01_CNFG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CLR_IIR_BUF	OBIT_WIDTH	IBIT_WIDTH	MONO	OFS		IFS	
Type									RW	RW	RW	RW	RW		RW	
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLAC_AMOUNT								IIR_EN	IIR_STAGE						
Type	RW								RW	RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
23		CLR_IIR_BUF	**Set 1 to clear current IIR output history buffer. This register will auto-clear once the histories are cleared.**
22		OBIT_WIDTH	**Bit-width Selection for Output** 0: 32-bit 1: 16-bit
21		IBIT_WIDTH	**Bit-width Selection for Input** 0: 32-bit 1: 16-bit
20		MONO	**Mono/Stereo Selection Regsiter** 0: This channel pair is stereo. 1: This channel pair is mono.
19:18		OFS	**Output Sample Rate Selection.** set 0, 1, 2 to choose the realted frequency on palette.
17:16		IFS	**Input Sample Rate Selection.** set 0, 1, 2 to choose the realted frequency on palette.
15:8		CLAC_AMOUNT	**Calculation amount.** Define how many 128-bit output the related channel pair should calculate at each turn.
7		IIR_EN	**Anti-alias IIR filter enable.** Set 1 to turn on the anti-alias IIR filter.
6:4		IIR_STAGE	**Anti-alias IIR filter stage.** Define how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 order is supported.

11220C20 ASRC2_FREQUENCY_0 ASRC_FREQUENCY_0 00F00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_0							
Type									RW							
Reset									1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_0															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_0	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220C24 ASRC2_FREQUENCY_1 ASRC_FREQUENCY_1 00DC8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_1							
Type									RW							
Reset									1	1	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_1															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_1	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220C28 ASRC2_FREQUENCY_2 ASRC_FREQUENCY_2 00A00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_2							
Type									RW							
Reset									1	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_2	**Frequency Palette.**

Bit(s)	Mnemonic	Name	Description
			The frequency 'palette' for each channel set to define its input frequency & output frequency

11220C2C ASRC2_FREQUENCY_3 ASRC_FREQUENCY_3 00DC8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_3							
Type									RW							
Reset									1	1	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_3															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_3	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220C30 ASRC2_IBUF_SADR ASRC_IBUF_SADR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		IBUF_SADR	**Input Buffer Start Address.** The start address of input buffer, in byte unit and128-bit alignment.

11220C34 ASRC2_IBUF_SIZE ASRC_IBUF_SIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CH_IBUF_SIZE			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH_IBUF_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
19:4		CH_IBUF_SIZE	**Input Channel Size.** The input buffer size for each channel, in byte unit and 128-bit alignment. Each channel uses the same size an is circular.

11220C38 ASRC2_OBUF_SADR ASRC_OBUF_SADR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		OBUF_SADR	**Output Buffer Start Address.** The start address of output buffer, in byte unit and128-bit alignment.

11220C3C ASRC2_OBUF_SIZE ASRC_OBUF_SIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CH_OBUF_SIZE			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH_OBUF_SIZE															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
19:4		CH_OBUF_SIZE	**Output Channel Size.** The output buffer size per channel, in byte unit and128-bit alignment. Each channel uses the same size an is circular.

11220C40 ASRC2_CH01_IBUF_RDPNT ASRC_CH01_IBUF_RDPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_IBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_IBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_IBUF_RDPNT	**IBUF Read Address Register. In byte unit and128-bit alignment.** Current input buffer read address for each channel pair. For stereo channe, this value is related to first channel.

11220C50 ASRC2_CH01_IBUF_WRPNT ASRC_CH01_IBUF_WRPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_IBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_IBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_IBUF_WRPNT	**IBUF Write Address Register. In byte unit and128-bit alignment.** Current input buffer write address for each channel pair, this register is used to prevent ASRC read the invalid data. For stereo channel, this value is related to first channel.

11220C60 ASRC2_CH01_OBUF_WRPNT ASRC_CH01_OBUF_WRPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_OBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_OBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Mnemonic	Name	Description
31:2		ASRC_CH01_OBUF_WRPNT	**OBUF Write Address Register. In byte unit and 32-bit alignment.** Current output buffer write address for each channel pair. For stereo channe, this value is related to first channel.

11220C70 ASRC2_CH01_OBUF_RDPNT ASRC_CH01_OBUF_RDPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_OBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_OBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_OBUF_RDPNT	**OBUF Read Address Register. In byte unit and128-bit alignment.** Current output buffer read address for each channel pair, this register is used to prevent ASRC write the un-read output. For stereo channe, this value is related to first channel.

11220C80 ASRC2_IBUF_INTR_CNT0 ASRC_IBUF_INTR_CNT0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH01_IBUF_INTR_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		CH01_IBUF_INTR_CNT	**Channel Pair01 Iutput Buffer Amount Interrupt Register** When the related input buffer left less than this amount (in 512-bit unit) of input data. It will rise the input buffer amount flag.

11220C88 ASRC2_OBUF_INTR_CNT0 ASRC_OBUF_INTR_CNT0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH01_OBUF_INTR_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		CH01_OBUF_INTR_CNT	**Channel Pair01 Output Buffer Amount Interrupt Register** When the related onput buffer contain more than this amount (in 512-bit unit) of output data. It will rise the output buffer amount flag.

11220C90 ASRC2_BAK_REG ASRC_BAK_REG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**RESULT_SEL**		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		RESULT_SEL	**Output Selection** 000: ASRC output 001: Data input 010: CMPF output 011: HBF1 output 100: HBF2 output 101: HBF3 output 110: HBF4 output 111: Each stage IIR output in order.

11220C94 ASRC2_FREQ_CALI_CTRL ASRC_FREQ_CALI_CTRL 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												**FREQ_CALC_BUSY**	**COMP_FREQ_RES_EN**		**SRC_SEL**	

Type												RW	RW		RW	
Reset												0	1		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYPASS_DEGLITCH	MAX_GWIDTH			AUTO_FS2_UPDATE	AUTO_RESTART	FREQ_UPDATE_FS2	CALI_EN								
Type	RW	RW			RW	RW	RW	RW								
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
20		FREQ_CALC_BUSY	**This bit shows if the frequency calculation is running. For one round running case, user should wait this bit and CALI_EN bit become low and then the frequency result will be ready.**
19		COMP_FREQ_RES_EN	**Frequency compenstation enabling register.**
17:16		SRC_SEL	**The calibrator input source selection register. Before modifying this register, please make sure the calibrator is turned off.**
15		BYPASS_DEGLITCH	**Set 1 to bypass the deglitch circuit for calibrator input.**
14:12		MAX_GWIDTH	**Define the maximum glitchwidth of the calibrator input signal, in unit of calibrator reference clock cycle.**
11		AUTO_FS2_UPDATE	**set 1 to enalbe ASRC_FREQUENCY_2 auto update with the calibrator result once the calibrator complete one round.**
10		AUTO_RESTART	**Auto restart. set 1 make the calibrator auto restart new calibration while one run completes.** This value will be updated into calibrator once the enable signal is turned on from off state.
9		FREQ_UPDATE_FS2	**0: Use period calibration result to update FS2.** 1: Use frequency calibration result to update FS2.
8		CALI_EN	**Set 1 to enable frequency clibrator. If auto restart is 0, this bit will be cleared while one clibration run is completed.** If you set 0 to close calibrator, please wait until this bit become 0 to make next run can be started safely.

11220C98 ASRC2_FREQ_CALI_CYC ASRC_FREQ_CALI_CYC 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQ_CALI_CYC							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQ_CALI_CYC															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
23:8		ASRC_FREQ_CALI_CYC	**ASRC Frequency Calibrating Cycle Register** Define how many input signal cycles the calibrator calibrates in one round. This register is updated into calibrator once the calibrator enbale CALI_EN(ASRC_FREQ_CALI_CTRL[8]) is turned on from off state.

11220C9C ASRC2_PRD_CALI_RESULT ASRC_PRD_CALI_RESULT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_PRD_CALI_RESULT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_PRD_CALI_RESULT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_PRD_CALI_RESULT	**ASRC Period Calibrator Result** Record the calibration result of previous round. Write any value to this register will clear the result.

11220CA0 ASRC2_FREQ_CALI_RESULT ASRC_FREQ_CALI_RESULT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name									ASRC_FREQ_CALI_RESULT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQ_CALI_RESULT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQ_CALI_RESULT	**ASRC Frequency Calibrator Result** Record the calibration result of previous round. This value is got from the quotient of (ASRC_FCALC_DENOMINATOR / ASRC_PRD_CALI_RESULT), in 1.23 format. Write any value to this register will clear the result.

11220CD8 ASRC2_CALI_DENOMINATOR ASRC_CALI_DENOMINATOR 00800000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_CALI_DENOMINATOR							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CALI_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_CALI_DENOMINATOR	**Determine the denominator for performing period-to-frequency calibration result translation.**

11220CE0 ASRC2_MAX_OUT_PER_IN0 ASRC_MAX_OUT_PER_IN0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CH01_MAX_OUT_PER_IN											
Type					RW											
Reset					0	0	0	0								

Bit(s)	Mnemonic	Name	Description
11:8		CH01_MAX_OUT_PER_IN	**CH01 Maximum output amount per input.** Tell ASRC each CH-set translation information to prevent output full. This value should be "ceil(OFs / IFs)". The ASRC support up to 8x up-sample and ~16x down-sample.

11220CF0 ASRC2_IIR_CRAM_ADDR ASRC_IIR_CRAM_ADDR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_IIR_CRAM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		ASRC_IIR_CRAM_ADDR	**Determine the read/write address of IIR coefficient SRAM. Read/Write ASRC_IIR_CRAM_DATA will make this register increase by 1.**

11220CF4 ASRC2_IIR_CRAM_DATA ASRC_IIR_CRAM_DATA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_IIR_CRAM_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_IIR_CRAM_DATA															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_IIR_CRAM_DATA	**Read/Write data port of the coefficient SRAM. Read data have one cycle delay.** The coefficients are filled stage by stage, each stage has 6 coefficient. For the 2nd order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2 / 1 + (2^shift)*b1*Z^-1 + (2^shift)*b2*Z^-2" The coefficent should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

11220CF8 ASRC2_OUT_BUF_MON0 ASRC_OUT_BUF_MON0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WDLE_CNT**															**ASRC_WRITE_DONE**
Type	RO															RO
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Mnemonic	Name	Description
15:8		WDLE_CNT	**Inticate number of not-finished 128-bit ASRC DRAM write data.**
0		ASRC_WRITE_DONE	**Inticate all ASRC write data to DRAM are done.**

11220CFC ASRC2_OUT_BUF_MON1 ASRC_OUT_BUF_MON1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ASRC_WR_ADR**															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_WR_ADR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_WR_ADR	**ASRC DRAM write address.**

11220D00 ASRC3_GEN_CONF ASRC_GEN_CONF 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					USE_OUT_MAY_FULL							CH_CNTX_SWEN				CH_CLEAR
Type					RW							RW				RW
Reset					0							0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CH_EN	DSP_CTRL_COEFF_SRAM		ASRC_BUSY	ASRC_EN								
Type				RW	RW		RO	RW								
Reset				0	0		0	0								

Bit(s)	Mnemonic	Name	Description
27		USE_OUT_MAY_FULL	**Setting 1 makes ASM update status when output is going to be full.** 0: Don't use out_may_full 1.: Use out_may_full
20		CH_CNTX_SWEN	**Context switch disabler for CH-set 0.** Disable context switch of each CH-set, remember to stop each CH-set first by set related enable before using this registers.
16		CH_CLEAR	**CH-set clear signal for CH-set 0,** set to 1 means the chset will clear history at next run.
12		CH_EN	**CH-set enable signal for CH-set 0,**

Bit(s)	Mnemonic	Name	Description
			This register controls which CH-set should be execute.
11		DSP_CTRL_COEFF_SRAM	**Setting 1 makes RISC can access coefficient SRAM through ASRC_IIR_CRAM_ADDR and ASRC_IIR_CRAM_DATA.**
9		ASRC_BUSY	**asrc busy flag.** 1 means chseto is running.
8		ASRC_EN	**asrc enable.** The central enable signal, should be turned on after all configration are set.

11220D04 ASRC3_IER ASRC_IER 00101000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												IBUF_EMPTY_INTEN				IBUF_AMOUNT_INTEN
Type												RW				RW
Reset												1				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBUF_OV_INTEN				OBUF_AMOUNT_INTEN								
Type				RW				RW								
Reset				1				0								

Bit(s)	Mnemonic	Name	Description
20		IBUF_EMPTY_INTEN	**input buffer empty interrupt enable for CH-set 0.**
16		IBUF_AMOUNT_INTEN	**input buffer amount interrupt enable for CH-set 0.**
12		OBUF_OV_INTEN	**output buffer overflow interupt enable for CH-set 0.**
8		OBUF_AMOUNT_INTEN	**output buffer amount interupt enable for CH-set 0.**

11220D08 ASRC3_IFR ASRC_IFR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												IBUF_EMPTY_INT				IBUF_AMOUNT_INT
Type												RW				RW
Reset												0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBUF_OV_INT				OBUF_AMOUNT_INT								
Type				RW				RW								
Reset				0				0								

Bit(s)	Mnemonic	Name	Description
20		IBUF_EMPTY_INT	**Input Buffer Empty Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related input buffer is empty. Write 1 to the related bit will clear it.
16		IBUF_AMOUNT_INT	**Input left amount reached Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related input buffer left amount reached the dedicated value. Write 1 to the related bit will clear it.
12		OBUF_OV_INT	**Output Buffer Full Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related output buffer is full. Write buffer full will make the whole system hang, please resolve it as soon as possible. Write 1 to the related bit will clear it.
8		OBUF_AMOUNT_INT	**Output Amount Reached Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related channel pair output amount meets requirement. Write 1 to the related bit will clear it.

11220D10 ASRC3_CH01_CNFG ASRC_CH01_CNFG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CLR_IIR_BUF	OBIT_WIDTH	IBIT_WIDTH	MONO	OFS		IFS	
Type									RW	RW	RW	RW	RW		RW	

Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLAC_AMOUNT								IIR_EN	IIR_STAGE						
Type	RW								RW	RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
23		CLR_IIR_BUF	**Set 1 to clear current IIR output history buffer. This register will auto-clear once the histories are cleared.**
22		OBIT_WIDTH	**Bit-width Selection for Output** 0: 32-bit 1: 16-bit
21		IBIT_WIDTH	**Bit-width Selection for Input** 0: 32-bit 1: 16-bit
20		MONO	**Mono/Stereo Selection Regsiter** 0: This channel pair is stereo. 1: This channel pair is mono.
19:18		OFS	**Output Sample Rate Selection.** set 0, 1, 2 to choose the realted frequency on palette.
17:16		IFS	**Input Sample Rate Selection.** set 0, 1, 2 to choose the realted frequency on palette.
15:8		CLAC_AMOUNT	**Calculation amount.** Define how many 128-bit output the related channel pair should calculate at each turn.
7		IIR_EN	**Anti-alias IIR filter enable.** Set 1 to turn on the anti-alias IIR filter.
6:4		IIR_STAGE	**Anti-alias IIR filter stage.** Define how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 order is supported.

11220D20 ASRC3_FREQUENCY_0 ASRC_FREQUENCY_0 00F00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_0							
Type									RW							
Reset									1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_0	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220D24 ASRC3_FREQUENCY_1 ASRC_FREQUENCY_1 00DC8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_1							
Type									RW							
Reset									1	1	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_1															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_1	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220D28 ASRC3_FREQUENCY_2 ASRC_FREQUENCY_2 00A00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_2							
Type									RW							
Reset									1	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_2															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_2	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220D2C ASRC3_FREQUENCY_3 ASRC_FREQUENCY_3 00DC8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_3							
Type									RW							
Reset									1	1	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_3															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_3	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220D30 ASRC3_IBUF_SADR ASRC_IBUF_SADR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		IBUF_SADR	**Input Buffer Start Address.**

Bit(s)	Mnemonic	Name	Description
			The start address of input buffer, in byte unit and128-bit alignment.

11220D34 ASRC3_IBUF_SIZE ASRC_IBUF_SIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CH_IBUF_SIZE			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH_IBUF_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
19:4		CH_IBUF_SIZE	**Input Channel Size.** The input buffer size for each channel, in byte unit and 128-bit alignment. Each channel uses the same size an is circular.

11220D38 ASRC3_OBUF_SADR ASRC_OBUF_SADR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		OBUF_SADR	**Output Buffer Start Address.** The start address of output buffer, in byte unit and128-bit alignment.

11220D3C ASRC3_OBUF_SIZE ASRC_OBUF_SIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CH_OBUF_SIZE			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH_OBUF_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
19:4		CH_OBUF_SIZE	**Output Channel Size.** The output buffer size per channel, in byte unit and128-bit alignment. Each channel uses the same size an is circular.

11220D40 ASRC3_CH01_IBUF_RDPNT ASRC_CH01_IBUF_RDPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_IBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_IBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_IBUF_RDPNT	**IBUF Read Address Register. In byte unit and128-bit alignment.** Current input buffer read address for each channel pair. For stereo channe, this value is related to first channel.

11220D50 ASRC3_CH01_IBUF_WRPNT ASRC_CH01_IBUF_WRPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_IBUF_WRPNT															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_IBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_IBUF_WRPNT	**IBUF Write Address Register. In byte unit and128-bit alignment.** Current input buffer write address for each channel pair, this register is used to prevent ASRC read the invalid data. For stereo channel, this value is related to first channel.

11220D60 ASRC3_CH01_OBUF_WRPNT ASRC_CH01_OBUF_WRPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_OBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_OBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Mnemonic	Name	Description
31:2		ASRC_CH01_OBUF_WRPNT	**OBUF Write Address Register. In byte unit and 32-bit alignment.** Current output buffer write address for each channel pair. For stereo channe, this value is related to first channel.

11220D70 ASRC3_CH01_OBUF_RDPNT ASRC_CH01_OBUF_RDPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_OBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_OBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_OBUF_RDPNT	**OBUF Read Address Register. In byte unit and128-bit alignment.** Current output buffer read address for each channel pair, this register is used to prevent ASRC write the un-read output. For stereo channe, this value is related to first channel.

11220D80 ASRC3_IBUF_INTR_CNT0 ASRC_IBUF_INTR_CNT0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH01_IBUF_INTR_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		CH01_IBUF_INTR_CNT	**Channel Pair01 Iutput Buffer Amount Interrupt Register** When the related input buffer left less than this amount (in 512-bit unit) of input data. It will rise the input buffer amount flag.

11220D88 ASRC3_OBUF_INTR_CNT0 ASRC_OBUF_INTR_CNT0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CH01_OBUF_INTR_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		CH01_OBUF_INTR_CNT	**Channel Pair01 Output Buffer Amount Interrupt Register** When the related onput buffer contain more than this amount (in 512-bit unit) of output data. It will rise the output buffer amount flag.

11220D90 ASRC3_BAK_REG ASRC_BAK_REG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RESULT_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		RESULT_SEL	**Output Selection** 000: ASRC output 001: Data input 010: CMPF output 011: HBF1 output 100: HBF2 output 101: HBF3 output 110: HBF4 output 111: Each stage IIR output in order.

11220D94 ASRC3_FREQ_CALI_CTRL ASRC_FREQ_CALI_CTRL 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name												FREQ_CALC_BUSY	COMP_FREQ_RES_EN		SRC_SEL	
Type												RW	RW		RW	
Reset												0	1		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYPASS_DEGLITCH	MAX_GWIDTH			AUTO_FS2_UPDATE	AUTO_RESTART	FREQ_UPDATE_FS2	CALI_EN								
Type	RW	RW			RW	RW	RW	RW								
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
20		FREQ_CALC_BUSY	**This bit shows if the frequency calculation is running. For one round running case, user should wait this bit and CALI_EN bit become low and then the frequency result will be ready.**
19		COMP_FREQ_RES_EN	**Frequency compenstation enabling register.**
17:16		SRC_SEL	**The calibrator input source selection register. Before modifying this register, please make sure the calibrator is turned off.**
15		BYPASS_DEGLITCH	**Set 1 to bypass the deglitch circuit for calibrator input.**
14:12		MAX_GWIDTH	**Define the maximum glitchwidth of the calibrator input signal, in unit of calibrator reference clock cycle.**
11		AUTO_FS2_UPDATE	**set 1 to enalbe ASRC_FREQUENCY_2 auto update with the calibrator result once the calibrator complete one round.**
10		AUTO_RESTART	**Auto restart. set 1 make the calibrator auto restart new calibration while one run completes.** This value will be updated into calibrator once the enable signal is turned on from off state.
9		FREQ_UPDATE_FS2	**0: Use period calibration result to update FS2.** 1: Use frequency calibration result to update FS2.
8		CALI_EN	**Set 1 to enable frequency clibrator. If auto restart is 0, this bit will be cleared while one clibration run is completed.** If you set 0 to close calibrator, please wait until this bit become 0 to make next run can be started safely.

Bit(s)	Mnemonic	Name	Description

11220D98 ASRC3_FREQ_CALI_CYC ASRC_FREQ_CALI_CYC 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQ_CALI_CYC							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQ_CALI_CYC															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
23:8		ASRC_FREQ_CALI_CYC	**ASRC Frequency Calibrating Cycle Register** Define how many input signal cycles the calibrator calibrates in one round. This register is updated into calibrator once the calibrator enbale CALI_EN(ASRC_FREQ_CALI_CTRL[8]) is turned on from off state.

11220D9C ASRC3_PRD_CALI_RESULT ASRC_PRD_CALI_RESULT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_PRD_CALI_RESULT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_PRD_CALI_RESULT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_PRD_CALI_RESULT	**ASRC Period Calibrator Result** Record the calibration result of previous round. Write any value to this register will clear the result.

Bit(s)	Mnemonic	Name	Description

11220DA0 ASRC3_FREQ_CALI_RESULT ASRC_FREQ_CALI_RESULT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQ_CALI_RESULT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQ_CALI_RESULT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQ_CALI_RESULT	**ASRC Frequency Calibrator Result** Record the calibration result of previous round. This value is got from the quotient of (ASRC_FCALC_DENOMINATOR / ASRC_PRD_CALI_RESULT), in 1.23 format. Write any value to this register will clear the result.

11220DD8 ASRC3_CALI_DENOMINATOR ASRC_CALI_DENOMINATOR 00800000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_CALI_DENOMINATOR							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CALI_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_CALI_DENOMINATOR	**Determine the denominator for performing period-to-frequency calibration result translation.**

Bit(s)	Mnemonic	Name	Description

11220DE0 ASRC3_MAX_OUT_PER_IN0 ASRC_MAX_OUT_PER_IN0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CH01_MAX_OUT_PER_IN											
Type					RW											
Reset					0	0	0	0								

Bit(s)	Mnemonic	Name	Description
11:8		CH01_MAX_OUT_PER_IN	**CH01 Maximum output amount per input.** Tell ASRC each CH-set translation information to prevent output full. This value should be "ceil(OFs / iFs)". The ASRC support up to 8x up-sample and ~16x down-sample.

11220DF0 ASRC3_IIR_CRAM_ADDR ASRC_IIR_CRAM_ADDR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_IIR_CRAM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		ASRC_IIR_CRAM_ADDR	**Determine the read/write address of IIR coefficient SRAM. Read/Write ASRC_IIR_CRAM_DATA will make this register increase by 1.**

Bit(s)	Mnemonic	Name	Description

11220DF4 ASRC3_IIR_CRAM_DATA ASRC_IIR_CRAM_DATA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_IIR_CRAM_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_IIR_CRAM_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_IIR_CRAM_DATA	**Read/Write data port of the coefficient SRAM. Read data have one cycle delay.** The coefficients are filled stage by stage, each stage has 6 coefficient. For the 2nd order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2 / 1 + (2^shift)*b1*Z^-1 + (2^shift)*b2*Z^-2" The coefficent should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

11220DF8 ASRC3_OUT_BUF_MON0 ASRC_OUT_BUF_MON0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDLE_CNT															ASRC_WRITE_DONE
Type	RO															RO
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Mnemonic	Name	Description
15:8		WDLE_CNT	**Intication number of not-finished 128-bit ASRC DRAM write data.**
0		ASRC_WRITE_DONE	**Intication all ASRC write data to DRAM are done.**

11220DFC ASRC3_OUT_BUF_MON1 ASRC_OUT_BUF_MON1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_WR_ADR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_WR_ADR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_WR_ADR	**ASRC DRAM write address.**

11220E00 ASRC4_GEN_CONF ASRC_GEN_CONF 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					USE_OUT_MAY_FULL							CH_CNTX_SWEN				CH_CLEAR
Type					RW							RW				RW
Reset					0							0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CH_EN	DSP_CTRL_COEFF_SRAM		ASRC_BUSY	ASRC_EN								
Type				RW	RW		RO	RW								
Reset				0	0		0	0								

Bit(s)	Mnemonic	Name	Description
27		USE_OUT_MAY_FULL	**Setting 1 makes ASM update status when output is going to be full.** 0: Don't use out_may_full 1.: Use out_may_full
20		CH_CNTX_SWEN	**Context switch disabler for CH-set 0.** Disable context switch of each CH-set, remember to stop each CH-set first by set related enable before using this registers.
16		CH_CLEAR	**CH-set clear signal for CH-set 0,** set to 1 means the chset will clear history at next run.
12		CH_EN	**CH-set enable signal for CH-set 0,** This register controls which CH-set should be execute.
11		DSP_CTRL_COEFF_SRAM	**Setting 1 makes RISC can access coefficient SRAM through ASRC_IIR_CRAM_ADDR and ASRC_IIR_CRAM_DATA.**
9		ASRC_BUSY	**asrc busy flag.** 1 means chset0 is running.
8		ASRC_EN	**asrc enable.** The central enable signal, should be turned on after all configration are set.

11220E04 ASRC4_IER ASRC_IER 00101000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												IBUF_EMPTY_INTEN				IBUF_AMOUNT_INTEN
Type												RW				RW
Reset												1				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBUF_OV_INTEN				OBUF_AMOUNT_INTEN								
Type				RW				RW								
Reset				1				0								

Bit(s)	Mnemonic	Name	Description
20		IBUF_EMPTY_INTEN	**input buffer empty interrupt enable for CH-set 0.**
16		IBUF_AMOUNT_INTEN	**input buffer amount interrupt enable for CH-set 0.**
12		OBUF_OV_INTEN	**output buffer overflow interupt enable for CH-set 0.**
8		OBUF_AMOUNT_INTEN	**output buffer amount interupt enable for CH-set 0.**

11220E08 ASRC4_IFR ASRC_IFR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												IBUF_EMPTY_INT				IBUF_AMOUNT_INT
Type												RW				RW
Reset												0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBUF_OV_INT				OBUF_AMOUNT_INT								
Type				RW				RW								
Reset				0				0								

Bit(s)	Mnemonic	Name	Description
20		IBUF_EMPTY_INT	**Input Buffer Empty Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related input buffer is empty. Write 1 to the related bit will clear it.
16		IBUF_AMOUNT_INT	**Input left amount reached Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related input buffer left amount reached the dedicated value. Write 1 to the related bit will clear it.
12		OBUF_OV_INT	**Output Buffer Full Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related output buffer is full. Write buffer full will make

Bit(s)	Mnemonic	Name	Description
			the whole system hang, please resolve it as soon as possible. Write 1 to the related bit will clear it.
8		OBUF_AMOUNT_INT	**Output Amount Reached Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related channel pair output amount meets requirement. Write 1 to the related bit will clear it.

11220E10 ASRC4_CH01_CNFG ASRC_CH01_CNFG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CLR_IIR_BUF	OBIT_WIDTH	IBIT_WIDTH	MONO	OFS		IFS	
Type									RW	RW	RW	RW	RW		RW	
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLAC_AMOUNT								IIR_EN	IIR_STAGE						
Type	RW								RW	RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
23		CLR_IIR_BUF	**Set 1 to clear current IIR output history buffer. This register will auto-clear once the histories are cleared.**
22		OBIT_WIDTH	**Bit-width Selection for Output** 0: 32-bit 1: 16-bit
21		IBIT_WIDTH	**Bit-width Selection for Input** 0: 32-bit 1: 16-bit
20		MONO	**Mono/Stereo Selection Regsiter** 0: This channel pair is stereo. 1: This channel pair is mono.
19:18		OFS	**Output Sample Rate Selection.** set 0, 1, 2 to choose the realted frequency on palette.

Bit(s)	Mnemonic	Name	Description
17:16		IFS	**Input Sample Rate Selection.** set 0, 1, 2 to choose the realted frequency on palette.
15:8		CLAC_AMOUNT	**Calculation amount.** Define how many 128-bit output the related channel pair should calculate at each turn.
7		IIR_EN	**Anti-alias IIR filter enable.** Set 1 to turn on the anti-alias IIR filter.
6:4		IIR_STAGE	**Anti-alias IIR filter stage.** Define how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 order is supported.

11220E20 ASRC4_FREQUENCY_0 ASRC_FREQUENCY_0 00F00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_0							
Type									RW							
Reset									1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_0	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220E24 ASRC4_FREQUENCY_1 ASRC_FREQUENCY_1 00DC8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_1							
Type									RW							
Reset									1	1	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_1															

Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_1	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220E28 ASRC4_FREQUENCY_2 ASRC_FREQUENCY_2 00A00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_2							
Type									RW							
Reset									1	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_2	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220E2C ASRC4_FREQUENCY_3 ASRC_FREQUENCY_3 00DC8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_3							
Type									RW							
Reset									1	1	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_3															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_3	**Frequency Palette.**

Bit(s)	Mnemonic	Name	Description
			The frequency 'palette' for each channel set to define its input frequency & output frequency

11220E30 ASRC4_IBUF_SADR ASRC_IBUF_SADR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		IBUF_SADR	**Input Buffer Start Address.** The start address of input buffer, in byte unit and128-bit alignment.

11220E34 ASRC4_IBUF_SIZE ASRC_IBUF_SIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CH_IBUF_SIZE			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH_IBUF_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
19:4		CH_IBUF_SIZE	**Input Channel Size.** The input buffer size for each channel, in byte unit and 128-bit alignment. Each channel uses the same size an is circular.

11220E38 ASRC4_OBUF_SADR ASRC_OBUF_SADR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		OBUF_SADR	**Output Buffer Start Address.** The start address of output buffer, in byte unit and128-bit alignment.

11220E3C ASRC4_OBUF_SIZE ASRC_OBUF_SIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CH_OBUF_SIZE			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH_OBUF_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
19:4		CH_OBUF_SIZE	**Output Channel Size.** The output buffer size per channel, in byte unit and128-bit alignment. Each channel uses the same size an is circular.

11220E40 ASRC4_CH01_IBUF_RDPNT ASRC_CH01_IBUF_RDPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_IBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_IBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_IBUF_RDPNT	**IBUF Read Address Register. In byte unit and128-bit alignment.** Current input buffer read address for each channel pair. For stereo channe, this value is related to first channel.

11220E50 ASRC4_CH01_IBUF_WRPNT ASRC_CH01_IBUF_WRPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_IBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_IBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_IBUF_WRPNT	**IBUF Write Address Register. In byte unit and128-bit alignment.** Current input buffer write address for each channel pair, this register is used to prevent ASRC read the invalid data. For stereo channel, this value is related to first channel.

11220E60 ASRC4_CH01_OBUF_WRPNT ASRC_CH01_OBUF_WRPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_OBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_OBUF_WRPNT															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Mnemonic	Name	Description
31:2		ASRC_CH01_OBUF_WRPNT	**OBUF Write Address Register. In byte unit and 32-bit alignment.** Current output buffer write address for each channel pair. For stereo channe, this value is related to first channel.

11220E70 ASRC4_CH01_OBUF_RDPNT ASRC_CH01_OBUF_RDPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_OBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_OBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_OBUF_RDPNT	**OBUF Read Address Register. In byte unit and128-bit alignment.** Current output buffer read address for each channel pair, this register is used to prevent ASRC write the un-read output. For stereo channe, this value is related to first channel.

11220E80 ASRC4_IBUF_INTR_CNT ASRC_IBUF_INTR_CNT0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH01_IBUF_INTR_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		CH01_IBUF_INTR_CNT	**Channel Pair01 Iutput Buffer Amount Interrupt Register** When the related input buffer left less than this amount (in 512-bit unit) of input data. It will rise the input buffer amount flag.

11220E88 ASRC4_OBUF_INTR_CNTo ASRC_OBUF_INTR_CNTo 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH01_OBUF_INTR_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		CH01_OBUF_INTR_CNT	**Channel Pair01 Output Buffer Amount Interrupt Register** When the related onput buffer contain more than this amount (in 512-bit unit) of output data. It will rise the output buffer amount flag.

11220E90 ASRC4_BAK_REG ASRC_BAK_REG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RESULT_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		RESULT_SEL	**Output Selection** 000: ASRC output 001: Data input 010: CMPF output 011: HBF1 output 100: HBF2 output 101: HBF3 output 110: HBF4 output 111: Each stage IIR output in order.

11220E94 ASRC4_FREQ_CALI_CTRL ASRC_FREQ_CALI_CTRL 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												FREQ_CALC_BUSY	COMP_FREQ_RES_EN		SRC_SEL	
Type												RW	RW		RW	
Reset												0	1		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYPASS_DEGLITCH	MAX_GWIDTH			AUTO_FS2_UPDATE	AUTO_RESTART	FREQ_UPDATE_FS2	CALI_EN								
Type	RW	RW			RW	RW	RW	RW								
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
20		FREQ_CALC_BUSY	**This bit shows if the frequency calculation is running. For one round running case, user should wait this bit and CALI_EN bit become low and then the frequency result will be ready.**
19		COMP_FREQ_RES_EN	**Frequency compenstation enabling register.**
17:16		SRC_SEL	**The calibrator input source selection register. Before modifying this register, please make sure the calibrator is turned off.**

Bit(s)	Mnemonic	Name	Description
15		BYPASS_DEGLITCH	**Set 1 to bypass the deglitch circuit for calibrator input.**
14:12		MAX_GWIDTH	**Define the maximum glitchwidth of the calibrator input signal, in unit of calibrator reference clock cycle.**
11		AUTO_FS2_UPDATE	**set 1 to enalbe ASRC_FREQUENCY_2 auto update with the calibrator result once the calibrator complete one round.**
10		AUTO_RESTART	**Auto restart. set 1 make the calibrator auto restart new calibration while one run completes.** This value will be updated into calibrator once the enable signal is turned on from off state.
9		FREQ_UPDATE_FS2	**0: Use period calibration result to update FS2.** 1: Use frequency calibration result to update FS2.
8		CALI_EN	**Set 1 to enable frequency clibrator. If auto restart is 0, this bit will be cleared while one clibration run is completed.** If you set 0 to close calibrator, please wait until this bit become 0 to make next run can be started safely.

11220E98 ASRC4_FREQ_CALI_CYC ASRC_FREQ_CALI_CYC 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQ_CALI_CYC							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQ_CALI_CYC															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
23:8		ASRC_FREQ_CALI_CYC	**ASRC Frequency Calibrating Cycle Register** Define how many input signal cycles the calibrator calibrates in one round. This register is updated into calibrator once the calibrator enbale

Bit(s)	Mnemonic	Name	Description
			CALI_EN(ASRC_FREQ_CALI_CTRL[8]) is turned on from off state.

11220E9C ASRC4_PRD_CALI_RESULT ASRC_PRD_CALI_RESULT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_PRD_CALI_RESULT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_PRD_CALI_RESULT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_PRD_CALI_RESULT	**ASRC Period Calibrator Result** Record the calibration result of previous round. Write any value to this register will clear the result.

11220EA0 ASRC4_FREQ_CALI_RESULT ASRC_FREQ_CALI_RESULT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQ_CALI_RESULT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQ_CALI_RESULT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQ_CALI_RESULT	**ASRC Frequency Calibrator Result** Record the calibration result of previous round.

Bit(s)	Mnemonic	Name	Description
			This value is got from the quotient of (ASRC_FCALC_DENOMINATOR / ASRC_PRD_CALI_RESULT), in 1.23 format. Write any value to this register will clear the result.

11220ED8 ASRC4_CALI_DENOMINATOR ASRC_CALI_DENOMINATOR 00800000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_CALI_DENOMINATOR							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CALI_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_CALI_DENOMINATOR	**Determine the denominator for performing period-to-frequency calibration result translation.**

11220EE0 ASRC4_MAX_OUT_PER_IN0 ASRC_MAX_OUT_PER_IN0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CH01_MAX_OUT_PER_IN											
Type					RW											
Reset					0	0	0	0								

Bit(s)	Mnemonic	Name	Description
11:8		CH01_MAX_OUT_PER_IN	**CH01 Maximum output amount per input.**

Bit(s)	Mnemonic	Name	Description
			Tell ASRC each CH-set translation information to prevent output full. This value should be "ceil(OFs / IFs)". The ASRC support up to 8x up-sample and ~16x down-sample.

11220EF0 ASRC4_IIR_CRAM_ADDR ASRC_IIR_CRAM_ADDR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_IIR_CRAM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		ASRC_IIR_CRAM_ADDR	**Determine the read/write address of IIR coefficient SRAM. Read/Write ASRC_IIR_CRAM_DATA will make this register increase by 1.**

11220EF4 ASRC4_IIR_CRAM_DATA ASRC_IIR_CRAM_DATA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_IIR_CRAM_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_IIR_CRAM_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_IIR_CRAM_DATA	**Read/Write data port of the coefficient SRAM. Read data have one cycle delay.**

Bit(s)	Mnemonic	Name	Description
			The coefficients are filled stage by stage, each stage has 6 coefficient. For the 2nd order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2 / 1 + (2^shift)*b1*Z^-1 + (2^shift)*b2*Z^-2" The coefficent should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

11220EF8 ASRC4_OUT_BUF_MON0 ASRC_OUT_BUF_MON0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WDLE_CNT**															**ASRC_WRITE_DONE**
Type	RO															RO
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Mnemonic	Name	Description
15:8		WDLE_CNT	**Inticate number of not-finished 128-bit ASRC DRAM write data.**
0		ASRC_WRITE_DONE	**Inticate all ASRC write data to DRAM are done.**

11220EFC ASRC4_OUT_BUF_MON1 ASRC_OUT_BUF_MON1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ASRC_WR_ADR**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ASRC_WR_ADR**															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_WR_ADR	**ASRC DRAM write address.**

11220F00 ASRC5_GEN_CONF ASRC_GEN_CONF 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					USE_OUT_MAY_FULL							CH_CNTX_SWEN				CH_CLEAR
Type					RW							RW				RW
Reset					0							0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CH_EN	DSP_CTRL_COEFF_SRAM		ASRC_BUSY	ASRC_EN								
Type				RW	RW		RO	RW								
Reset				0	0		0	0								

Bit(s)	Mnemonic	Name	Description
27		USE_OUT_MAY_FULL	**Setting 1 makes ASM update status when output is going to be full.** 0: Don't use out_may_full 1.: Use out_may_full
20		CH_CNTX_SWEN	**Context switch disabler for CH-set 0.** Disable context switch of each CH-set, remember to stop each CH-set first by set related enable before using this registers.
16		CH_CLEAR	**CH-set clear signal for CH-set 0,** set to 1 means the chset will clear history at next run.
12		CH_EN	**CH-set enable signal for CH-set 0,** This register controls which CH-set should be execute.
11		DSP_CTRL_COEFF_SRAM	**Setting 1 makes RISC can access coefficient SRAM through ASRC_IIR_CRAM_ADDR and ASRC_IIR_CRAM_DATA.**

Bit(s)	Mnemonic	Name	Description
9		ASRC_BUSY	**asrc busy flag.** 1 means chseto is running.
8		ASRC_EN	**asrc enable.** The central enable signal, should be turned on after all configration are set.

11220F04 ASRC5_IER ASRC_IER 00101000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												IBUF_EMPTY_INTEN				IBUF_AMOUNT_INTEN
Type												RW				RW
Reset												1				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBUF_OV_INTEN				OBUF_AMOUNT_INTEN								
Type				RW				RW								
Reset				1				0								

Bit(s)	Mnemonic	Name	Description
20		IBUF_EMPTY_INTEN	**input buffer empty interrupt enable for CH-set 0.**
16		IBUF_AMOUNT_INTEN	**input buffer amount interrupt enable for CH-set 0.**
12		OBUF_OV_INTEN	**output buffer overflow interupt enable for CH-set 0.**
8		OBUF_AMOUNT_INTEN	**output buffer amount interupt enable for CH-set 0.**

11220F08 ASRC5_IFR ASRC_IFR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												IBUF_EMP				IBUF_AM

												TY_INT				OUNT_INT
Type												RW				RW
Reset												0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				OBUF_OV_INT				OBUF_AMOUNT_INT								
Type				RW				RW								
Reset				0				0								

Bit(s)	Mnemonic	Name	Description
20		IBUF_EMPTY_INT	**Input Buffer Empty Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related input buffer is empty. Write 1 to the related bit will clear it.
16		IBUF_AMOUNT_INT	**Input left amount reached Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related input buffer left amount reached the dedicated value. Write 1 to the related bit will clear it.
12		OBUF_OV_INT	**Output Buffer Full Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related output buffer is full. Write buffer full will make the whole system hang, please resolve it as soon as possible. Write 1 to the related bit will clear it.
8		OBUF_AMOUNT_INT	**Output Amount Reached Flag for CH-set 0.** Each bit related to one channel pair, 1 means the related channel pair output amount meets requirement. Write 1 to the related bit will clear it.

11220F10 ASRC5_CH01_CNFG ASRC_CH01_CNFG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CLR_IIR_BUF	OBIT_WIDTH	IBIT_WIDTH	MONO	OFS		IFS	
Type									RW	RW	RW	RW	RW		RW	
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLAC_AMOUNT								IIR_EN	IIR_STAGE						

Type	RW								RW	RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
23		CLR_IIR_BUF	**Set 1 to clear current IIR output history buffer. This register will auto-clear once the histories are cleared.**
22		OBIT_WIDTH	**Bit-width Selection for Output** 0: 32-bit 1: 16-bit
21		IBIT_WIDTH	**Bit-width Selection for Input** 0: 32-bit 1: 16-bit
20		MONO	**Mono/Stereo Selection Regsiter** 0: This channel pair is stereo. 1: This channel pair is mono.
19:18		OFS	**Output Sample Rate Selection.** set 0, 1, 2 to choose the realted frequency on palette.
17:16		IFS	**Input Sample Rate Selection.** set 0, 1, 2 to choose the realted frequency on palette.
15:8		CLAC_AMOUNT	**Calculation amount.** Define how many 128-bit output the related channel pair should calculate at each turn.
7		IIR_EN	**Anti-alias IIR filter enable.** Set 1 to turn on the anti-alias IIR filter.
6:4		IIR_STAGE	**Anti-alias IIR filter stage.** Define how many 2-order IIR stages are cascaded for the anti-alias filter. This value should be "real stage amount" minus 1, which means up to 8 stages and 16 order is supported.

11220F20 ASRC5_FREQUENCY_0 ASRC_FREQUENCY_0 00F00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_0							

Type									RW							
Reset									1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_0	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220F24 ASRC5_FREQUENCY_1 ASRC_FREQUENCY_1 00DC8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_1							
Type									RW							
Reset									1	1	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_1															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_1	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220F28 ASRC5_FREQUENCY_2 ASRC_FREQUENCY_2 00A00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_2							
Type									RW							
Reset									1	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_2	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220F2C ASRC5_FREQUENCY_3 ASRC_FREQUENCY_3 00DC8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQUENCY_3							
Type									RW							
Reset									1	1	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQUENCY_3															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQUENCY_3	**Frequency Palette.** The frequency 'palette' for each channel set to define its input frequency & output frequency

11220F30 ASRC5_IBUF_SADR ASRC_IBUF_SADR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		IBUF_SADR	**Input Buffer Start Address.** The start address of input buffer, in byte unit and128-bit alignment.

11220F34 ASRC5_IBUF_SIZE ASRC_IBUF_SIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CH_IBUF_SIZE			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH_IBUF_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
19:4		CH_IBUF_SIZE	**Input Channel Size.** The input buffer size for each channel, in byte unit and 128-bit alignment. Each channel uses the same size an is circular.

11220F38 ASRC5_OBUF_SADR ASRC_OBUF_SADR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OBUF_SADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		OBUF_SADR	**Output Buffer Start Address.** The start address of output buffer, in byte unit and128-bit alignment.

11220F3C ASRC5_OBUF_SIZE ASRC_OBUF_SIZE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													CH_OBUF_SIZE			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	CH_OBUF_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
19:4		CH_OBUF_SIZE	**Output Channel Size.** The output buffer size per channel, in byte unit and128-bit alignment. Each channel uses the same size an is circular.

11220F40 ASRC5_CH01_IBUF_RDPNT ASRC_CH01_IBUF_RDPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_IBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_IBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_IBUF_RDPNT	**IBUF Read Address Register. In byte unit and128-bit alignment.** Current input buffer read address for each channel pair. For stereo channe, this value is related to first channel.

11220F50 ASRC5_CH01_IBUF_WRPNT ASRC_CH01_IBUF_WRPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_IBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_IBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_IBUF_WRPNT	**IBUF Write Address Register. In byte unit and128-bit alignment.** Current input buffer write address for each channel pair, this register is used to prevent ASRC read the invalid data. For stereo channel, this value is related to first channel.

11220F60 ASRC5_CH01_OBUF_WRPNT ASRC_CH01_OBUF_WRPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_OBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_OBUF_WRPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Mnemonic	Name	Description
31:2		ASRC_CH01_OBUF_WRPNT	**OBUF Write Address Register. In byte unit and 32-bit alignment.** Current output buffer write address for each channel pair. For stereo channe, this value is related to first channel.

11220F70 ASRC5_CH01_OBUF_RDPNT ASRC_CH01_OBUF_RDPNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ASRC_CH01_OBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CH01_OBUF_RDPNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_CH01_OBUF_RDPNT	**OBUF Read Address Register. In byte unit and128-bit alignment.** Current output buffer read address for each channel pair, this register is used to prevent ASRC write the un-read output. For stereo channe, this value is related to first channel.

11220F80 ASRC5_IBUF_INTR_CNT0 ASRC_IBUF_INTR_CNT0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH01_IBUF_INTR_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		CH01_IBUF_INTR_CNT	**Channel Pair01 Iutput Buffer Amount Interrupt Register** When the related input buffer left less than this amount (in 512-bit unit) of input data. It will rise the input buffer amount flag.

11220F88 ASRC5_OBUF_INTR_CNT0 ASRC_OBUF_INTR_CNT0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH01_OBUF_INTR_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		CH01_OBUF_INTR_CNT	**Channel Pair01 Output Buffer Amount Interrupt Register** When the related onput buffer contain more than this amount (in 512-bit unit) of output data. It will rise the output buffer amount flag.

11220F90 ASRC5_BAK_REG ASRC_BAK_REG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**RESULT_SEL**		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		RESULT_SEL	**Output Selection** 000: ASRC output 001: Data input 010: CMPF output 011: HBF1 output 100: HBF2 output 101: HBF3 output 110: HBF4 output 111: Each stage IIR output in order.

11220F94 ASRC5_FREQ_CALI_CTRL ASRC_FREQ_CALI_CTRL 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												**FREQ_CALC_BUSY**	**COMP_FREQ_RES_EN**		**SRC_SEL**	

Type												RW	RW		RW	
Reset												0	1		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYPASS_DEGLITCH	MAX_GWIDTH			AUTO_FS2_UPDATE	AUTO_RESTART	FREQ_UPDATE_FS2	CALI_EN								
Type	RW	RW			RW	RW	RW	RW								
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
20		FREQ_CALC_BUSY	**This bit shows if the frequency calculation is running. For one round running case, user should wait this bit and CALI_EN bit become low and then the frequency result will be ready.**
19		COMP_FREQ_RES_EN	**Frequency compenstation enabling register.**
17:16		SRC_SEL	**The calibrator input source selection register. Before modifying this register, please make sure the calibrator is turned off.**
15		BYPASS_DEGLITCH	**Set 1 to bypass the deglitch circuit for calibrator input.**
14:12		MAX_GWIDTH	**Define the maximum glitchwidth of the calibrator input signal, in unit of calibrator reference clock cycle.**
11		AUTO_FS2_UPDATE	**set 1 to enalbe ASRC_FREQUENCY_2 auto update with the calibrator result once the calibrator complete one round.**
10		AUTO_RESTART	**Auto restart. set 1 make the calibrator auto restart new calibration while one run completes.** This value will be updated into calibrator once the enable signal is turned on from off state.
9		FREQ_UPDATE_FS2	**0: Use period calibration result to update FS2.** 1: Use frequency calibration result to update FS2.
8		CALI_EN	**Set 1 to enable frequency clibrator. If auto restart is 0, this bit will be cleared while one clibration run is completed.** If you set 0 to close calibrator, please wait until this bit become 0 to make next run can be started safely.

11220F98 ASRC5_FREQ_CALI_CYC ASRC_FREQ_CALI_CYC 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_FREQ_CALI_CYC							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQ_CALI_CYC															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
23:8		ASRC_FREQ_CALI_CYC	**ASRC Frequency Calibrating Cycle Register** Define how many input signal cycles the calibrator calibrates in one round. This register is updated into calibrator once the calibrator enbale CALI_EN(ASRC_FREQ_CALI_CTRL[8]) is turned on from off state.

11220F9C ASRC5_PRD_CALI_RESULT ASRC_PRD_CALI_RESULT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_PRD_CALI_RESULT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_PRD_CALI_RESULT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_PRD_CALI_RESULT	**ASRC Period Calibrator Result** Record the calibration result of previous round. Write any value to this register will clear the result.

11220FA0 ASRC5_FREQ_CALI_RESULT ASRC_FREQ_CALI_RESULT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name									ASRC_FREQ_CALI_RESULT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_FREQ_CALI_RESULT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_FREQ_CALI_RESULT	**ASRC Frequency Calibrator Result** Record the calibration result of previous round. This value is got from the quotient of (ASRC_FCALC_DENOMINATOR / ASRC_PRD_CALI_RESULT), in 1.23 format. Write any value to this register will clear the result.

11220FD8 ASRC5_CALI_DENOMINATOR ASRC_CALI_DENOMINATOR 00800000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_CALI_DENOMINATOR							
Type									RW							
Reset									1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_CALI_DENOMINATOR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_CALI_DENOMINATOR	**Determine the denominator for performing period-to-frequency calibration result translation.**

11220FE0 ASRC5_MAX_OUT_PER_IN0 ASRC_MAX_OUT_PER_IN0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CH01_MAX_OUT_PER_IN											
Type					RW											
Reset					0	0	0	0								

Bit(s)	Mnemonic	Name	Description
11:8		CH01_MAX_OUT_PER_IN	**CH01 Maximum output amount per input.** Tell ASRC each CH-set translation information to prevent output full. This value should be "ceil(OFs / IFs)". The ASRC support up to 8x up-sample and ~16x down-sample.

11220FF0 ASRC5_IIR_CRAM_ADDR ASRC_IIR_CRAM_ADDR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_IIR_CRAM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15:8		ASRC_IIR_CRAM_ADDR	**Determine the read/write address of IIR coefficient SRAM. Read/Write ASRC_IIR_CRAM_DATA will make this register increase by 1.**

11220FF4 ASRC5_IIR_CRAM_DATA ASRC_IIR_CRAM_DATA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									ASRC_IIR_CRAM_DATA							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_IIR_CRAM_DATA															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:0		ASRC_IIR_CRAM_DATA	**Read/Write data port of the coefficient SRAM. Read data have one cycle delay.** The coefficients are filled stage by stage, each stage has 6 coefficient. For the 2nd order IIR filter with transfer function of one stage as: "(2^shift)*a0 + (2^shift)*a1*Z^-1 + (2^shift)*a2*Z^-2 / 1 + (2^shift)*b1*Z^-1 + (2^shift)*b2*Z^-2" The coefficent should be filled as (from low address to high address) a2 a1 a0 -b1 -b2 shift

11220FF8 ASRC5_OUT_BUF_MON0 ASRC_OUT_BUF_MON0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WDLE_CNT**															**ASRC_WRITE_DONE**
Type	RO															RO
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Mnemonic	Name	Description
15:8		WDLE_CNT	**Inticate number of not-finished 128-bit ASRC DRAM write data.**
0		ASRC_WRITE_DONE	**Inticate all ASRC write data to DRAM are done.**

11220FFC ASRC5_OUT_BUF_MON1 ASRC_OUT_BUF_MON1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ASRC_WR_ADR**															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ASRC_WR_ADR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ASRC_WR_ADR	**ASRC DRAM write address.**

112211C0 DSD_ENC_CON0 DSD ENC Control Register 0 00020003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112211C4 DSD_ENC_CON1 DSD ENC Control Register 1 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112211C8 DSD_ENC_CON2 DSD ENC Control Register 2 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112211D0 DSD_ENC_STATUS DSD ENC STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

112211D4 DSD_UPDATE_POS AFE Control Register 0 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221200 AFE_DAC_CON0 AFE Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							TDM_IN_ON	DMA_ON	SIGMADSP_ON	DSDW_ON	AWB2_ON	AWB_ON	Reserved	MOD_PCM_ON	DAI_ON	ULMCH_ON
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UL6_ON	UL5_ON	UL4_ON	UL3_ON	UL2_ON	VUL_ON	DSDR_ON	ARB1_ON	DLMCH_ON	DL6_ON	DL5_ON	DL4_ON	DL3_ON	DL2_ON	DL1_ON	AFE_ON
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
25		TDM_IN_ON	**Controls the enabling of audio dma read memory interface path** 0: Off 1: On
24		DMA_ON	**Controls the enabling of audio dma read memory interface path** 0: Off 1: On
23		SIGMADSP_ON	
22		DSDW_ON	**Controls the enabling of dsd encoder write memory interface path** 0: Off 1: On
21		AWB2_ON	**Controls the enabling of AWB 2 memory interface path** 0: Off 1: On
20		AWB_ON	**Controls the enabling of AWB 1 memory interface path** 0: Off 1: On

Bit(s)	Mnemonic	Name	Description
19		Reserved	**Controls the enabling of I2S memory interface path** 0: Off 1: On
18		MOD_PCM_ON	**Controls the enabling of modem PCM memory interface path** 0: Off 1: On
17		DAI_ON	**Controls the enabling of DAI memory interface path** 0: Off 1: On
16		ULMCH_ON	**Controls the enabling of uplink multi-channel memory interface path** 0: Off 1: On
15		UL6_ON	**Controls the enabling of uplink 6 memory interface path** 0: Off 1: On
14		UL5_ON	**Controls the enabling of uplink 5 memory interface path** 0: Off 1: On
13		UL4_ON	**Controls the enabling of uplink 4 memory interface path** 0: Off 1: On
12		UL3_ON	**Controls the enabling of uplink 3 memory interface path** 0: Off 1: On

Bit(s)	Mnemonic	Name	Description
11		UL2_ON	**Controls the enabling of uplink 2 memory interface path** 0: Off 1: On
10		VUL_ON	**Controls the enabling of uplink 1 memory interface path** 0: Off 1: On
9		DSDR_ON	**Controls the enabling of dsd encoder read memory interface path** 0: Off 1: On
8		ARB1_ON	**Controls the enabling of ARB 1 memory interface path** 0: Off 1: On
7		DLMCH_ON	**Controls the enabling of downlink multi-channel memory interface path** 0: Off 1: On
6		DL6_ON	**Controls the enabling of downlink 6 memory interface path** 0: Off 1: On
5		DL5_ON	**Controls the enabling of downlink 5 memory interface path** 0: Off 1: On
4		DL4_ON	**Controls the enabling of downlink 4 memory interface path** 0: Off 1: On

Bit(s)	Mnemonic	Name	Description
3		DL3_ON	**Controls the enabling of downlink 3 memory interface path** 0: Off 1: On
2		DL2_ON	**Controls the enabling of downlink 2 memory interface path** 0: Off 1: On
1		DL1_ON	**Controls the enabling of downlink 1 memory interface path** 0: Off 1: On
0		AFE_ON	**Controls the enabling of the whole AFE module** 0: Off 1: On

11221204 AFE_DAC_CON1 AFE Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DL6_MODE					DL5_MODE					DL4_MODE			
Type			RW					RW					RW			
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL4_MODE		DL3_MODE					DL2_MODE					DL1_MODE			
Type	RW		RW					RW					RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:25		DL6_MODE	**Controls the sampling frequency for downlink 6 path.** 5'b00000: 8k 5'b00001: 12k

Bit(s)	Mnemonic	Name	Description
			5'b00010: 16k
			5'b00011: 24k
			5'b00100: 32k
			5'b00101: 48k
			5'b00110: 96k
			5'b00111: 192k
			5'b01000: 384k
			5'b01001: i2s1 salve fs
			5'b01010: i2s2 salve fs
			5'b01011: i2s3 salve fs
			5'b01100: i2s4 salve fs
			5'b01101: i2s5 salve fs
			5'b01110: i2s6 salve fs
			5'b10000: 7.35k
			5'b10001: 11.025k
			5'b10010: 14.7k
			5'b10011: 22.05k
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4k
			5'b11000: 352.8k
24:20		DL5_MODE	**Controls the sampling frequency for downlink 5 path.**
			5'b00000: 8k
			5'b00001: 12k
			5'b00010: 16k
			5'b00011: 24k

Bit(s)	Mnemonic	Name	Description
			5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192k 5'b01000: 384k 5'b01001: i2s1 salve fs 5'b01010: i2s2 salve fs 5'b01011: i2s3 salve fs 5'b01100: i2s4 salve fs 5'b01101: i2s5 salve fs 5'b01110: i2s6 salve fs 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4k 5'b11000: 352.8k
19:15		DL4_MODE	**Controls the sampling frequency for downlink 4 path.** 00000b: 8k 00001b: 12k 00010b: 16k 00011b: 24k 00100b: 32k 00101b: 48k

Bit(s)	Mnemonic	Name	Description
			00110b: 96k 00111b: 192k 01000b: 384k 01001b: i2s1 salve fs 01010b: i2s2 salve fs 01011b: i2s3 salve fs 01100b: i2s4 salve fs 01101b: i2s5 salve fs 01110b: i2s6 salve fs 10000b: 7.35k 10001b: 11.025k 10010b: 14.7k 10011b: 22.05k 10100b: 29.4k 10101b: 44.1k 10110b: 88.2k 10111b: 176.4k 11000b: 352.8k
14:10		DL3_MODE	**Controls the sampling frequency for downlink 3 path.** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192k

Bit(s)	Mnemonic	Name	Description
			5'b01000: 384k 5'b01001: i2s1 salve fs 5'b01010: i2s2 salve fs 5'b01011: i2s3 salve fs 5'b01100: i2s4 salve fs 5'b01101: i2s5 salve fs 5'b01110: i2s6 salve fs 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4k 5'b11000: 352.8k
9:5		DL2_MODE	**Controls the sampling frequency for downlink 2 path.** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192k 5'b01000: 384k 5'b01001: i2s1 salve fs

Bit(s)	Mnemonic	Name	Description
			5'b01010: i2s2 salve fs
			5'b01011: i2s3 salve fs
			5'b01100: i2s4 salve fs
			5'b01101: i2s5 salve fs
			5'b01110: i2s6 salve fs
			5'b10000: 7.35k
			5'b10001: 11.025k
			5'b10010: 14.7k
			5'b10011: 22.05k
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4k
			5'b11000: 352.8k
4:0		DL1_MODE	**Controls the sampling frequency for downlink 1 path.**
			00000b: 8k
			00001b: 12k
			00010b: 16k
			00011b: 24k
			00100b: 32k
			00101b: 48k
			00110b: 96k
			00111b: 192k
			01000b: 384k
			01001b: i2s1 salve fs
			01010b: i2s2 salve fs
			01011b: i2s3 salve fs

Bit(s)	Mnemonic	Name	Description
			01100b: i2s4 salve fs 01101b: i2s5 salve fs 01110b: i2s6 salve fs 10000b: 7.35k 10001b: 11.025k 10010b: 14.7k 10011b: 22.05k 10100b: 29.4k 10101b: 44.1k 10110b: 88.2k 10111b: 176.4k 11000b: 352.8k

11221208 AFE_DAC_CON2 AFE Control Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MOD_PCM_MODE	DAI_MODE	UL6_MODE					UL5_MODE					UL4_MODE			
Type	RW	RW	RW					RW					RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UL4_MODE	UL3_MODE					UL2_MODE					VUL_MODE				
Type	RW	RW					RW					RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		MOD_PCM_MODE	**Controls the sampling frequency for MOD_PCM path.** 0: 8k 1: 16k

Bit(s)	Mnemonic	Name	Description
30		DAI_MODE	**Controls the sampling frequency for DAI path.** 0: 8k 1: 16k
29:25		UL6_MODE	**Controls the sampling frequency for uplink 6 path.** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192k 5'b01000: 384k 5'b01001: i2s1 salve fs 5'b01010: i2s2 salve fs 5'b01011: i2s3 salve fs 5'b01100: i2s4 salve fs 5'b01101: i2s5 salve fs 5'b01110: i2s6 salve fs 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4k

Bit(s)	Mnemonic	Name	Description
			5'b11000: 352.8k
24:20		UL5_MODE	**Controls the sampling frequency for uplink 5 path.** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192k 5'b01000: 384k 5'b01001: i2s1 salve fs 5'b01010: i2s2 salve fs 5'b01011: i2s3 salve fs 5'b01100: i2s4 salve fs 5'b01101: i2s5 salve fs 5'b01110: i2s6 salve fs 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4k 5'b11000: 352.8k
19:15		UL4_MODE	**Controls the sampling frequency for uplink 4 path.**

Bit(s)	Mnemonic	Name	Description
			5'b00000: 8k
			5'b00001: 12k
			5'b00010: 16k
			5'b00011: 24k
			5'b00100: 32k
			5'b00101: 48k
			5'b00110: 96k
			5'b00111: 192k
			5'b01000: 384k
			5'b01001: i2s1 salve fs
			5'b01010: i2s2 salve fs
			5'b01011: i2s3 salve fs
			5'b01100: i2s4 salve fs
			5'b01101: i2s5 salve fs
			5'b01110: i2s6 salve fs
			5'b10000: 7.35k
			5'b10001: 11.025k
			5'b10010: 14.7k
			5'b10011: 22.05k
			5'b10100: 29.4k
			5'b10101: 44.1k
			5'b10110: 88.2k
			5'b10111: 176.4k
			5'b11000: 352.8k
14:10		UL3_MODE	**Controls the sampling frequency for uplink 3 path.**
			00000b: 8k
			00001b: 12k

Bit(s)	Mnemonic	Name	Description
			00010b: 16k
			00011b: 24k
			00100b: 32k
			00101b: 48k
			00110b: 96k
			00111b: 192k
			01000b: 384k
			01001b: i2s1 salve fs
			01010b: i2s2 salve fs
			01011b: i2s3 salve fs
			01100b: i2s4 salve fs
			01101b: i2s5 salve fs
			01110b: i2s6 salve fs
			10000b: 7.35k
			10001b: 11.025k
			10010b: 14.7k
			10011b: 22.05k
			10100b: 29.4k
			10101b: 44.1k
			10110b: 88.2k
			10111b: 176.4k
			11000b: 352.8k
9:5		UL2_MODE	**Controls the sampling frequency for uplink 2 path.**
			5'b00000: 8k
			5'b00001: 12k
			5'b00010: 16k
			5'b00011: 24k

Bit(s)	Mnemonic	Name	Description
			5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192k 5'b01000: 384k 5'b01001: i2s1 salve fs 5'b01010: i2s2 salve fs 5'b01011: i2s3 salve fs 5'b01100: i2s4 salve fs 5'b01101: i2s5 salve fs 5'b01110: i2s6 salve fs 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4k 5'b11000: 352.8k
4:0		VUL_MODE	**Controls the sampling frequency for uplink 1 path.** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k

Bit(s)	Mnemonic	Name	Description
			5'b00110: 96k 5'b00111: 192k 5'b01000: 384k 5'b01001: i2s1 salve fs 5'b01010: i2s2 salve fs 5'b01011: i2s3 salve fs 5'b01100: i2s4 salve fs 5'b01101: i2s5 salve fs 5'b01110: i2s6 salve fs 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4k 5'b11000: 352.8k

1122120C AFE_DAC_CON3 AFE Control Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSDW_LSB_MODE	DSDR_LSB_MODE	DL6_LSB_MDOE	DL5_LSB_MODE	DL4_LSB_MODE	DL3_LSB_MODE	DL2_LSB_MODE	DL1_LSB_MODE	DSDR_DATA	ARB1_DATA	DL6_DATA	DL5_DATA	DL4_DATA	DL3_DATA	DL2_DATA	DL1_DATA
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARB1_LSB_MODE	ARB1_MODE					AWB2_MODE					AWB_MODE				
Type	RW	RW					RW					RW				

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		DSDW_LSB_MODE	**DSD encoder write DSD bit format.** 0: MSB mode 1: LSB mode
30		DSDR_LSB_MODE	**DSD encoder read DSD bit format.** 0: MSB mode 1: LSB mode
29		DL6_LSB_MDOE	**Downlink 6 read DSD bit format.** 0: MSB mode 1: LSB mode
28		DL5_LSB_MODE	**Downlink 5 read DSD bit format.** 0: MSB mode 1: LSB mode
27		DL4_LSB_MODE	**Downlink 4 read DSD bit format.** 0: MSB mode 1: LSB mode
26		DL3_LSB_MODE	**Downlink 3 read DSD bit format.** 0: MSB mode 1: LSB mode
25		DL2_LSB_MODE	**Downlink 2 read DSD bit format.** 0: MSB mode 1: LSB mode
24		DL1_LSB_MODE	**Downlink 1 read DSD bit format.** 0: MSB mode 1: LSB mode
23		DSDR_DATA	**Controls the data mode for dsd encoder read memory interface path.** 0: Stereo

Bit(s)	Mnemonic	Name	Description
			1: Mono
22		ARB1_DATA	**Controls the data mode for audio read back 1 memory interface path.** 0: Stereo 1: Mono
21		DL6_DATA	**Controls the data mode for downlink 6 memory interface path.** 0: Stereo 1: Mono
20		DL5_DATA	**Controls the data mode for downlink 5 memory interface path.** 0: Stereo 1: Mono
19		DL4_DATA	**Controls the data mode for downlink 4 memory interface path.** 0: Stereo 1: Mono
18		DL3_DATA	**Controls the data mode for downlink 3 memory interface path.** 0: Stereo 1: Mono
17		DL2_DATA	**Controls the data mode for downlink 2 memory interface path.** 0: Stereo 1: Mono
16		DL1_DATA	**Controls the data mode for downlink 1 memory interface path.** 0: Stereo 1: Mono
15		ARB1_LSB_MODE	**Audio read back DSD bit format.** 0: MSB mode 1: LSB mode

Bit(s)	Mnemonic	Name	Description
14:10		ARB1_MODE	**Controls the sampling frequency for audio read back 1 path.** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192k 5'b01000: 384k 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4k 5'b11000: 352.8k
9:5		AWB2_MODE	**Controls the sampling frequency for audio write back 2 path.** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k

Bit(s)	Mnemonic	Name	Description
			5'b00111: 192k 5'b01000: 384k 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k 5'b10110: 88.2k 5'b10111: 176.4k 5'b11000: 352.8k
4:0		AWB_MODE	**Controls the sampling frequency for audio write back 1 path.** 5'b00000: 8k 5'b00001: 12k 5'b00010: 16k 5'b00011: 24k 5'b00100: 32k 5'b00101: 48k 5'b00110: 96k 5'b00111: 192k 5'b01000: 384k 5'b10000: 7.35k 5'b10001: 11.025k 5'b10010: 14.7k 5'b10011: 22.05k 5'b10100: 29.4k 5'b10101: 44.1k

Bit(s)	Mnemonic	Name	Description
			5'b10110: 88.2k 5'b10111: 176.4k 5'b11000: 352.8k

11221210 AFE_DAC_CON4 AFE Control Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AWB2_LSB_MODE	AWB_LSB_MODE	UL6_LSB_MODE	UL5_LSB_MODE	UL4_LSB_MODE	UL3_LSB_MODE	UL2_LSB_MODE	VUL_LSB_MODE	DSDW_DSD_WIDTH		DSDW_RMONO	DSDW_DATA	AWB2_R_MONO	AWB2_DATA	AWB_R_MONO	AWB_DATA
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MOD_PCM_DUP_WR	DAI_DUP_WR	ULMCH_R_MONO	ULMCH_DATA	UL6_R_MONO	UL6_DATA	UL5_R_MONO	UL5_DATA	UL4_R_MONO	UL4_DATA	UL3_R_MONO	UL3_DATA	UL2_R_MONO	UL2_DATA	VUL_R_MONO	VUL_DATA
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		AWB2_LSB_MODE	**Audio write back 2 DSD bit format.** 0: MSB mode 1: LSB mode
30		AWB_LSB_MODE	**Audio write back 1 DSD bit format.** 0: MSB mode 1: LSB mode
29		UL6_LSB_MODE	**Uplink 6 write DSD bit format.** 0: MSB mode 1: LSB mode
28		UL5_LSB_MODE	**Uplink 5 write DSD bit format.** 0: MSB mode 1: LSB mode

Bit(s)	Mnemonic	Name	Description
27		UL4_LSB_MODE	**Uplink 4 write DSD bit format.** 0: MSB mode 1: LSB mode
26		UL3_LSB_MODE	**Uplink 3 write DSD bit format.** 0: MSB mode 1: LSB mode
25		UL2_LSB_MODE	**Uplink 2 write DSD bit format.** 0: MSB mode 1: LSB mode
24		VUL_LSB_MODE	**Uplink 1 write DSD bit format.** 0: MSB mode 1: LSB mode
23:22		DSDW_DSD_WIDTH	**Controls the bit width for each dsd channel for dsd encoder write memory interface path.** 00b: 32bit 01b: 16bit 10b: 8bit
21		DSDW_R_MONO	**Controls the data mono type for dsd encoder write memory interface path.** 0: Mono use L channel 1: Mono use R channel
20		DSDW_DATA	**Controls the data mode for dsd encoder write memory interface path.** 0: Stereo 1: Mono
19		AWB2_R_MONO	**Controls the data mono type for audio write back 2 memory interface path.** 0: Mono use L channel 1: Mono use R channel
18		AWB2_DATA	**Controls the data mode for audio write back 2 memory interface path.**

Bit(s)	Mnemonic	Name	Description
			0: Stereo 1: Mono
17		AWB_R_MONO	**Controls the data mono type for audio write back memory interface path.** 0: Mono use L channel 1: Mono use R channel
16		AWB_DATA	**Controls the data mode for audio write back memory interface path.** 0: Stereo 1: Mono
15		MOD_PCM_DUP_WR	**Controls the data write mode for modem PCM memory interface path.** 0: Normal write 1: Duplicated write
14		DAI_DUP_WR	**Controls the data write mode for DAI memory interface path.** 0: Normal write 1: Duplicated write
13		ULMCH_R_MONO	**Controls the data mono type for uplink multi-channel memory interface path.** 0: Mono use L channel 1: Mono use R channel
12		ULMCH_DATA	**Controls the data mode for uplink multi-channel memory interface path.** 0: Stereo 1: Mono
11		UL6_R_MONO	**Controls the data mono type for uplink 6 memory interface path.** 0: Mono use L channel 1: Mono use R channel
10		UL6_DATA	**Controls the data mode for uplink 6 memory interface path.**

Bit(s)	Mnemonic	Name	Description
			0: Stereo 1: Mono
9		UL5_R_MONO	**Controls the data mono type for uplink 5 memory interface path.** 0: Mono use L channel 1: Mono use R channel
8		UL5_DATA	**Controls the data mode for uplink5 memory interface path.** 0: Stereo 1: Mono
7		UL4_R_MONO	**Controls the data mono type for uplink 4 memory interface path.** 0: Mono use L channel 1: Mono use R channel
6		UL4_DATA	**Controls the data mode for uplink 4 memory interface path.** 0: Stereo 1: Mono
5		UL3_R_MONO	**Controls the data mono type for uplink 3 memory interface path.** 0: Mono use L channel 1: Mono use R channel
4		UL3_DATA	**Controls the data mode for uplink 3 memory interface path.** 0: Stereo 1: Mono
3		UL2_R_MONO	**Controls the data mono type for uplink 2 memory interface path.** 0: Mono use L channel 1: Mono use R channel
2		UL2_DATA	**Controls the data mode for uplink 2 memory interface path.**

Bit(s)	Mnemonic	Name	Description
			0: Stereo 1: Mono
1		VUL_R_MONO	**Controls the data mono type for uplink 1 memory interface path.** 0: Mono use L channel 1: Mono use R channel
0		VUL_DATA	**Controls the data mode for uplink 1 memory interface path.** 0: Stereo 1: Mono

11221214 AFE_DAC_CON5 AFE Control Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AWB2_DSD_WIDTH		AWB_DSD_WIDTH		UL6_DSD_WIDTH		UL5_DSD_WIDTH		UL4_DSD_WIDTH		UL3_DSD_WIDTH		UL2_DSD_WIDTH		VUL_DSD_WIDTH	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DSDR_DSD_WIDTH		ARB1_DSD_WIDTH		DL6_DSD_WIDTH		DL5_DSD_WIDTH		DL4_DSD_WIDTH		DL3_DSD_WIDTH		DL2_DSD_WIDTH		DL1_DSD_WIDTH	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:30		AWB2_DSD_WIDTH	**Controls the bit width for each dsd channel for audio write back 2 memory interface path.** 2'b00: 32bit 2'b01: 16bit 2'b10: 8bit
29:28		AWB_DSD_WIDTH	**Controls the bit width for each dsd channel for audio write back 1 memory interface path.** 2'b00: 32bit 2'b01: 16bit 2'b10: 8bit

Bit(s)	Mnemonic	Name	Description
27:26		UL6_DSD_WIDTH	**Controls the bit width for each dsd channel for uplink 6 memory interface path.** 2'b00: 32bit 2'b01: 16bit 2'b10: 8bit
25:24		UL5_DSD_WIDTH	**Controls the bit width for each dsd channel for uplink 5 memory interface path.** 2'b00: 32bit 2'b01: 16bit 2'b10: 8bit
23:22		UL4_DSD_WIDTH	**Controls the bit width for each dsd channel for uplink 4 memory interface path.** 2'b00: 32bit 2'b01: 16bit 2'b10: 8bit
21:20		UL3_DSD_WIDTH	**Controls the bit width for each dsd channel for uplink 3 memory interface path.** 2'b00: 32bit 2'b01: 16bit 2'b10: 8bit
19:18		UL2_DSD_WIDTH	**Controls the bit width for each dsd channel for uplink 2 memory interface path.** 2'b00: 32bit 2'b01: 16bit 2'b10: 8bit
17:16		VUL_DSD_WIDTH	**Controls the bit width for each dsd channel for uplink 1 memory interface path.** 2'b00: 32bit 2'b01: 16bit 2'b10: 8bit
15:14		DSDR_DSD_WIDTH	**Controls the bit width for each dsd channel for dsd encoder read memory interface path.**

Bit(s)	Mnemonic	Name	Description
			2'b00: 32bit 2'b01: 16bit 2'b10: 8bit
13:12		ARB1_DSD_WIDTH	**Controls the bit width for each dsd channel for audio read back 1 memory interface path.** 2'b00: 32bit 2'b01: 16bit 2'b10: 8bit
11:10		DL6_DSD_WIDTH	**Controls the bit width for each dsd channel for downlink 6 memory interface path.** 2'b00: 32bit 2'b01: 16bit 2'b10: 8bit
9:8		DL5_DSD_WIDTH	**Controls the bit width for each dsd channel for downlink 5 memory interface path.** 2'b00: 32bit 2'b01: 16bit 2'b10: 8bit
7:6		DL4_DSD_WIDTH	**Controls the bit width for each dsd channel for downlink 4 memory interface path.** 2'b00: 32bit 2'b01: 16bit 2'b10: 8bit
5:4		DL3_DSD_WIDTH	**Controls the bit width for each dsd channel for downlink 3 memory interface path.** 2'b00: 32bit 2'b01: 16bit 2'b10: 8bit
3:2		DL2_DSD_WIDTH	**Controls the bit width for each dsd channel for downlink 2 memory interface path.** 2'b00: 32bit

Bit(s)	Mnemonic	Name	Description
			2'b01: 16bit 2'b10: 8bit
1:0		DL1_DSD_WIDTH	**Controls the bit width for each dsd channel for downlink 1 memory interface path.** 2'b00: 32bit 2'b01: 16bit 2'b10: 8bit

11221218 AFE_DAC_MON0 AFE Control Monitor 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						AFE_DMA_RETM	TDM_IN_ON_RETM	IEC2_OUT_RETM	IEC_OUT_RETM	HDMI_OUT_RETM	MOD_DAI_RETM	AFE_DSDW_RETM	AFE_AWB2_RETM	AFE_AWB_RETM	AFE_DAI_RETM	AFE_ULMCH_RETM
Type						RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL6_RETM	AFE_UL5_RETM	AFE_UL4_RETM	AFE_UL3_RETM	AFE_UL2_RETM	AFE_VUL_RETM	AFE_DSDR_RETM	AFE_ARB1_RETM	AFE_DLMCH_RETM	AFE_DL6_RETM	AFE_DL5_RETM	AFE_DL4_RETM	AFE_DL3_RETM	AFE_DL2_RETM	AFE_DL1_RETM	AFE_ON_RETM
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
26		AFE_DMA_RETM	**Monitor signal for retiming of DMA_ON**
25		TDM_IN_ON_RETM	**Monitor signal for retiming of TDM_IN_ON**
24		IEC2_OUT_RETM	**Monitor signal for retiming of IEC2_OUT_ON**
23		IEC_OUT_RETM	**Monitor signal for retiming of IEC_OUT_ON**
22		HDMI_OUT_RETM	**Monitor signal for retiming of HDMI_OUT_ON**
21		MOD_DAI_RETM	**Monitor signal for retiming of MOD_DAI_ON**
20		AFE_DSDW_RETM	**Monitor signal for retiming of DSDW_ON**
19		AFE_AWB2_RETM	**Monitor signal for retiming of AWB2_ON**

Bit(s)	Mnemonic	Name	Description
18		AFE_AWB_RETM	**Monitor signal for retiming of AWB_ON**
17		AFE_DAI_RETM	**Monitor signal for retiming of DAI_ON**
16		AFE_ULMCH_RETM	**Monitor signal for retiming of ULMCH_ON**
15		AFE_UL6_RETM	**Monitor signal for retiming of UL6_ON**
14		AFE_UL5_RETM	**Monitor signal for retiming of UL5_ON**
13		AFE_UL4_RETM	**Monitor signal for retiming of UL4_ON**
12		AFE_UL3_RETM	**Monitor signal for retiming of UL3_ON**
11		AFE_UL2_RETM	**Monitor signal for retiming of UL2_ON**
10		AFE_VUL_RETM	**Monitor signal for retiming of VUL_ON**
9		AFE_DSDR_RETM	**Monitor signal for retiming of DSDR_ON**
8		AFE_ARB1_RETM	**Monitor signal for retiming of ARB1_ON**
7		AFE_DLMCH_RETM	**Monitor signal for retiming of DLMCH_ON**
6		AFE_DL6_RETM	**Monitor signal for retiming of DL6_ON**
5		AFE_DL5_RETM	**Monitor signal for retiming of DL5_ON**
4		AFE_DL4_RETM	**Monitor signal for retiming of DL4_ON**
3		AFE_DL3_RETM	**Monitor signal for retiming of DL3_ON**
2		AFE_DL2_RETM	**Monitor signal for retiming of DL2_ON**
1		AFE_DL1_RETM	**Monitor signal for retiming of DL1_ON**
0		AFE_ON_RETM	**Monitor signal for retiming of AFE_ON**

11221220 AFE_MEMIF_MINLEN0 AFE Memif Min BLength Register 0 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARB1_MINLEN				DLMCH_MINLEN				DL6_MINLEN				DL5_MINLEN			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL4_MINLEN				DL3_MINLEN				DL2_MINLEN				DL1_MINLEN			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:28		ARB1_MINLEN	**0: not support** 1: 16 byte burst
27:24		DLMCH_MINLEN	**0: not support** 1: 16 byte burst
23:20		DL6_MINLEN	**0: not support** 1: 16 byte burst
19:16		DL5_MINLEN	**0: not support** 1: 16 byte burst
15:12		DL4_MINLEN	**0: not support** 1: 16 byte burst
11:8		DL3_MINLEN	**0: not support** 1: 16 byte burst
7:4		DL2_MINLEN	**0: not support** 1: 16 byte burst
3:0		DL1_MINLEN	**0: not support** 1: 16 byte burst

11221224 AFE_MEMIF_MINLEN1 AFE Memif Min BLength Register 1 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MOD_DAI_MINLEN				DSDW_MINLEN				AWB2_MINLEN				AWB_MINLEN			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_IN_MINLEN				IEC_OUT_MINLEN				HDMI_OUT_MINLEN				DSDR_MINLEN			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:28		MOD_DAI_MINLEN	**0: not support** 1: 16 byte burst
27:24		DSDW_MINLEN	**0: not support**

Bit(s)	Mnemonic	Name	Description
			1: 16 byte burst
23:20		AWB2_MINLEN	**0: not support**
			1: 16 byte burst
19:16		AWB_MINLEN	**0: not support**
			1: 16 byte burst
15:12		TDM_IN_MINLEN	**0: not support**
			1: 16 byte burst
11:8		IEC_OUT_MINLEN	**0: not support**
			1: 16 byte burst
7:4		HDMI_OUT_MINLEN	**0: not support**
			1: 16 byte burst
3:0		DSDR_MINLEN	**0: not support**
			1: 16 byte burst

11221228 AFE_MEMIF_MINLEN2 AFE Memif Min BLength Register 2 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAI_MINLEN				ULMCH_MINLEN				UL6_MINLEN				UL5_MINLEN			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UL4_MINLEN				UL3_MINLEN				UL2_MINLEN				VUL_MINLEN			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:28		DAI_MINLEN	**0: not support**
			1: 16 byte burst
27:24		ULMCH_MINLEN	**0: not support**
			1: 16 byte burst
23:20		UL6_MINLEN	**0: not support**
			1: 16 byte burst

Bit(s)	Mnemonic	Name	Description
19:16		UL5_MINLEN	**0: not support** 1: 16 byte burst
15:12		UL4_MINLEN	**0: not support** 1: 16 byte burst
11:8		UL3_MINLEN	**0: not support** 1: 16 byte burst
7:4		UL2_MINLEN	**0: not support** 1: 16 byte burst
3:0		VUL_MINLEN	**0: not support** 1: 16 byte burst

1122122C AFE_MEMIF_MAXLEN0 AFE Memif Max BLength Register 0 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARB1_MAXLEN				DLMCH_MAXLEN				DL6_MAXLEN				DL5_MAXLEN			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL4_MAXLEN				DL3_MAXLEN				DL2_MAXLEN				DL1_MAXLEN			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:28		ARB1_MAXLEN	**0: not support** 1: 16 byte burst
27:24		DLMCH_MAXLEN	**0: not support** 1: 16 byte burst
23:20		DL6_MAXLEN	**0: not support** 1: 16 byte burst
19:16		DL5_MAXLEN	**0: not support** 1: 16 byte burst
15:12		DL4_MAXLEN	**0: not support**

Bit(s)	Mnemonic	Name	Description
			1: 16 byte burst
11:8		DL3_MAXLEN	**0: not support**
			1: 16 byte burst
7:4		DL2_MAXLEN	**0: not support**
			1: 16 byte burst
3:0		DL1_MAXLEN	**0: not support**
			1: 16 byte burst

11221230 AFE_MEMIF_MAXLEN1 AFE Memif Max BLength Register 1 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MOD_DAI_MAXLEN				DSDW_MAXLEN				AWB2_MAXLEN				AWB_MAXLEN			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_IN_MAXLEN				IEC_OUT_MAXLEN				HDMI_OUT_MAXLEN				DSDR_MAXLEN			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:28		MOD_DAI_MAXLEN	**0: not support**
			1: 16 byte burst
27:24		DSDW_MAXLEN	**0: not support**
			1: 16 byte burst
23:20		AWB2_MAXLEN	**0: not support**
			1: 16 byte burst
19:16		AWB_MAXLEN	**0: not support**
			1: 16 byte burst
15:12		TDM_IN_MAXLEN	**0: not support**
			1: 16 byte burst
11:8		IEC_OUT_MAXLEN	**0: not support**
			1: 16 byte burst

Bit(s)	Mnemonic	Name	Description
7:4		HDMI_OUT_MAXLEN	**0: not support** 1: 16 byte burst
3:0		DSDR_MAXLEN	**0: not support** 1: 16 byte burst

11221234 AFE_MEMIF_MAXLEN2 AFE Memif Max BLength Register 2 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAI_MAXLEN				ULMCH_MAXLEN				UL6_MAXLEN				UL5_MAXLEN			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UL4_MAXLEN				UL3_MAXLEN				UL2_MAXLEN				VUL_MAXLEN			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:28		DAI_MAXLEN	**0: not support** 1: 16 byte burst
27:24		ULMCH_MAXLEN	**0: not support** 1: 16 byte burst
23:20		UL6_MAXLEN	**0: not support** 1: 16 byte burst
19:16		UL5_MAXLEN	**0: not support** 1: 16 byte burst
15:12		UL4_MAXLEN	**0: not support** 1: 16 byte burst
11:8		UL3_MAXLEN	**0: not support** 1: 16 byte burst
7:4		UL2_MAXLEN	**0: not support** 1: 16 byte burst
3:0		VUL_MAXLEN	**0: not support**

Bit(s)	Mnemonic	Name	Description
			1: 16 byte burst

11221238 AFE_MEMIF_PBUF_SIZE AFE Memif prefecth buffer size 00FFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DLMCH_BIT_WIDTH	DLMCH_CH_NUM				Reserved		IEC_PBUF_SIZE		HDMI_PBUF_SIZE		DSDR_PBUF_SIZE	
Type				RW	RW				RW		RW		RW		RW	
Reset				0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARB1_PBUF_SIZE		DLMCH_PBUF_SIZE		DL6_PBUF_SIZE		DL5_PBUF_SIZE		DL4_PBUF_SIZE		DL3_PBUF_SIZE		DL2_PBUF_SIZE		DL1_PBUF_SIZE	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
28		DLMCH_BIT_WIDTH	**This bit control the output data bit-width.** 0: 16-bit 1: 32-bit
27:24		DLMCH_CH_NUM	**DLMCH out channel number assignement.** 0: No DLMCH out channel 1: 1-ch 2: 2-ch 3: 3-ch 4: 4-ch 5: 5-ch 6: 6-ch 7: 7-ch 8: 8-ch 9: 9-ch 10: 10-ch

Bit(s)	Mnemonic	Name	Description
			11: 11-ch
			12: 12-ch
23:22		Reserved	
21:20		IEC_PBUF_SIZE	
19:18		HDMI_PBUF_SIZE	
17:16		DSDR_PBUF_SIZE	
15:14		ARB1_PBUF_SIZE	
13:12		DLMCH_PBUF_SIZE	
11:10		DL6_PBUF_SIZE	
9:8		DL5_PBUF_SIZE	
7:6		DL4_PBUF_SIZE	
5:4		DL3_PBUF_SIZE	
3:2		DL2_PBUF_SIZE	
1:0		DL1_PBUF_SIZE	

1122123C AFE_MEMIF_HD_CON0 AFE Memif HD Audio Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DLMCH_DL6_SEL	DLMCH_DL5_SEL	DLMCH_DL4_SEL	DLMCH_DL3_SEL	DLMCH_DL2_SEL	DLMCH_DL1_SEL	DSDR_HD_AUDIO	
Type									RW	RW	RW	RW	RW	RW	RW	
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARB1_HD_AUDIO		Reserved		DL6_HD_AUDIO		DL5_HD_AUDIO		DL4_HD_AUDIO		DL3_HD_AUDIO		DL2_HD_AUDIO		DL1_HD_AUDIO	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23		DLMCH_DL6_SEL	

Bit(s)	Mnemonic	Name	Description
22		DLMCH_DL5_SEL	
21		DLMCH_DL4_SEL	
20		DLMCH_DL3_SEL	
19		DLMCH_DL2_SEL	
18		DLMCH_DL1_SEL	
17:16		DSDR_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
15:14		ARB1_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
13:12		Reserved	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
11:10		DL6_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
9:8		DL5_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
7:6		DL4_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
5:4		DL3_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
3:2		DL2_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
1:0		DL1_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB

1122121C AFE_MEMIF_HD_CON1 AFE Memif HD Audio Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ULTRA_TH_1				ULTRA_TH_2				MOD_DAI_HD_AUDIO		DAI_HD_AUDIO		TDM_IN_HD_AUDIO		AWB2_HD_AUDIO	
Type	RW				RW				RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_HD_AUDIO		ULMCH_HD_AUDIO		UL6_HD_AUDIO		UL5_HD_AUDIO		UL4_HD_AUDIO		UL3_HD_AUDIO		UL2_HD_AUDIO		VUL_HD_AUDIO	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		ULTRA_TH_1	**UL AGENT**
27:24		ULTRA_TH_2	**DL AGENT**
23:22		MOD_DAI_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
21:20		DAI_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
19:18		TDM_IN_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
17:16		AWB2_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
15:14		AWB_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
13:12		ULMCH_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
11:10		UL6_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
9:8		UL5_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
7:6		UL4_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
5:4		UL3_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
3:2		UL2_HD_AUDIO	**[0]: 32bit or 16bit hd audio on** [1]: align MSB
1:0		VUL_HD_AUDIO	**[0]: 32bit or 16bit hd audio on**

Bit(s)	Mnemonic	Name	Description
			[1]: align MSB

11221240 AFE_DL1_BASE AFE DL1 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL1_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL1_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DL1_BASE	**Base address of the DL1 input in master mode.** Always set AFE_DL1_BASE[3:0] = 4'h0 for the convenience of the hardware implementation.

11221244 AFE_DL1_CUR AFE DL1 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL1_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL1_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL1_CUR	**Indicates the current address of the DL1 input buffer.**

11221248 AFE_DL1_END AFE DL1 End Address Register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL1_END															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL1_END												AFE_DL1_END_LSB			
Type	RW												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DL1_END	**Ending address of the DL1 input in master mode.** Always set AFE_DL1_END[3:0] = 4'hF for the convenience of the hardware implementation.
3:0		AFE_DL1_END_LSB	

11221250 AFE_DL2_BASE AFE DL2 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL2_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL2_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DL2_BASE	**Base address of the DL2 input in master mode.** Always set AFE_DL2_BASE[3:0] = 4'h0 for the convenience of the hardware implementation.

11221254 AFE_DL2_CUR AFE DL2 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL2_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL2_CUR															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL2_CUR	**Indicates the current address of the DL2 input buffer.**

11221258 AFE_DL2_END AFE DL2 End Address Register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL2_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL2_END												AFE_DL2_END_LSB			
Type	RW												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DL2_END	**Ending address of the DL2 input in master mode.** Always set AFE_DL2_END[3:0] = 4'hF for the convenience of the hardware implementation.
3:0		AFE_DL2_END_LSB	

11221260 AFE_DL3_BASE AFE DL3 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL3_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL3_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DL3_BASE	**Base address of the DL3 input in master mode.**

Bit(s)	Mnemonic	Name	Description
			Always set AFE_DL3_BASE[3:0] = 4'h0 for the convenience of the hardware implementation.

11221264 AFE_DL3_CUR AFE DL3 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL3_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL3_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL3_CUR	**Indicates the current address of the DL3 input buffer.**

11221268 AFE_DL3_END AFE DL3 End Address Register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL3_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL3_END												AFE_DL3_END_LSB			
Type	RW												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DL3_END	**Ending address of the DL3 input in master mode.** Always set AFE_DL3_END[3:0] = 4'hF for the convenience of the hardware implementation.
3:0		AFE_DL3_END_LSB	

11221270 AFE_DL4_BASE AFE DL4 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL4_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL4_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DL4_BASE	**Base address of the DL4 input in master mode.** Always set AFE_DL4_BASE[3:0] = 4'h0 for the convenience of the hardware implementation.

11221274 AFE_DL4_CUR AFE DL4 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL4_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL4_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL4_CUR	**Indicates the current address of the DL4 input buffer.**

11221278 AFE_DL4_END AFE DL4 End Address Register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL4_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL4_END												AFE_DL4_END_LSB			
Type	RW												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DL4_END	**Ending address of the DL4 input in master mode.** Always set AFE_DL4_END[3:0] = 4'hF for the convenience of the hardware implementation.
3:0		AFE_DL4_END_LSB	

11221280 AFE_DL5_BASE AFE DL5 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL5_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL5_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DL5_BASE	**Base address of the DL5 input in master mode.** Always set AFE_DL5_BASE[3:0] = 4'h0 for the convenience of the hardware implementation.

11221284 AFE_DL5_CUR AFE DL5 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL5_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL5_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL5_CUR	**Indicates the current address of the DL5 input buffer.**

Bit(s)	Mnemonic	Name	Description

11221288 AFE_DL5_END AFE DL5 End Address Register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL5_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL5_END												AFE_DL5_END_LSB			
Type	RW												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DL5_END	**Ending address of the DL5 input in master mode.** Always set AFE_DL5_END[3:0] = 4'hF for the convenience of the hardware implementation.
3:0		AFE_DL5_END_LSB	

11221290 AFE_DL6_BASE AFE DL6 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL6_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL6_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DL6_BASE	**Base address of the DL6 input in master mode.** Always set AFE_DL6_BASE[3:0] = 4'h0 for the convenience of the hardware implementation.

11221294 AFE_DL6_CUR AFE DL6 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL6_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL6_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL6_CUR	**Indicates the current address of the DL6 input buffer.**

11221298 AFE_DL6_END AFE DL6 End Address Register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL6_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL6_END												AFE_DL6_END_LSB			
Type	RW												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DL6_END	**Ending address of the DL6 input in master mode.** Always set AFE_DL6_END[3:0] = 4'hF for the convenience of the hardware implementation.
3:0		AFE_DL6_END_LSB	

112212A0 AFE_DLMCH_BASE AFE DLMCH Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DLMCH_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DLMCH_BASE															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
31:3		AFE_DLMCH_BASE	**Base address of the DLMCH input in master mode.** Always set AFE_DLMCH_BASE[3:0] = 4'h0 for the convenience of the hardware implementation.

112212A4 AFE_DLMCH_CUR AFE DLMCH Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DLMCH_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DLMCH_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DLMCH_CUR	**Indicates the current address of the DLMCH input buffer.**

112212A8 AFE_DLMCH_END AFE DLMCH End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DLMCH_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DLMCH_END													AFE_DLMCH_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3		AFE_DLMCH_END	**Ending address of the DLMCH input in master mode.** Always set AFE_DLMCH_END[3:0] = 4'hF for the convenience of the hardware implementation.

Bit(s)	Mnemonic	Name	Description
2:0		AFE_DLMCH_END_LSB	

112212B0 AFE_ARB1_BASE AFE ARB1 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_ARB1_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_ARB1_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		AFE_ARB1_BASE	**Base address of the ARB1 input in master mode.** Always set AFE_ARB1_BASE[3:0] = 4'h0 for the convenience of the hardware implementation.

112212B4 AFE_ARB1_CUR AFE ARB1 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_ARB1_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_ARB1_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_ARB1_CUR	**Indicates the current address of the ARB1 input buffer.**

112212B8 AFE_ARB1_END AFE ARB1 End Address Register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	AFE_ARB1_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_ARB1_END												AFE_ARB1_END_LSB			
Type	RW												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:4		AFE_ARB1_END	**Ending address of the ARB1 input in master mode.** Always set AFE_ARB1_END[3:0] = 4'hF for the convenience of the hardware implementation.
3:0		AFE_ARB1_END_LSB	

112212C0 AFE_DSDR_BASE AFE DSDR Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DSDR_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DSDR_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DSDR_BASE	**Base address of the DSDR input in master mode.** Always set AFE_DSDR_BASE[3:0] = 4'h0 for the convenience of the hardware implementation.

112212C4 AFE_DSDR_CUR AFE DSDR Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DSDR_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DSDR_CUR															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DSDR_CUR	**Indicates the current address of the DSDR input buffer.**

112212C8 AFE_DSDR_END AFE DSDR End Address Register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DSDR_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DSDR_END												AFE_DSDR_END_LSB			
Type	RW												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DSDR_END	**Ending address of the DSDR input in master mode.** Always set AFE_DSDR_END[3:0] = 4'hF for the convenience of the hardware implementation.
3:0		AFE_DSDR_END_LSB	

112212D0 AFE_AWB_BASE AFE AWB Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_AWB_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_AWB_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
31:3		AFE_AWB_BASE	**Base address of the AWB input in master mode.**

Bit(s)	Mnemonic	Name	Description
			Always set AFE_AWB_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.

112212D8 AFE_AWB_END AFE AWB End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_AWB_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_AWB_END													AFE_AWB_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3		AFE_AWB_END	**Ending address of the AWB input in master mode.** Always set AFE_AWB_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0		AFE_AWB_END_LSB	

112212DC AFE_AWB_CUR AFE AWB Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_AWB_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_AWB_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_AWB_CUR	**Indicates the current address of the AWB input buffer.**

112212E0 AFE_AWB2_BASE AFE AWB2 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_AWB2_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_AWB2_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
31:3		AFE_AWB2_BASE	**Base address of the AWB2 input in master mode.** Always set AFE_AWB2_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.

112212E8 AFE_AWB2_END AFE AWB2 End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_AWB2_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_AWB2_END													AFE_AWB2_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3		AFE_AWB2_END	**Ending address of the AWB2 input in master mode.** Always set AFE_AWB2_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0		AFE_AWB2_END_LSB	

112212EC AFE_AWB2_CUR AFE AWB2 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_AWB2_CUR															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_AWB2_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_AWB2_CUR	**Indicates the current address of the AWB2 input buffer.**

112212F0 AFE_DSDW_BASE AFE DSDW Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DSDW_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DSDW_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
31:3		AFE_DSDW_BASE	**Base address of the DSDW input in master mode.** Always set AFE_DSDW_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.

112212F8 AFE_DSDW_END AFE DSDW End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DSDW_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DSDW_END													AFE_DSDW_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3		AFE_DSDW_END	**Ending address of the DSDW input in master mode.** Always set AFE_DSDW_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0		AFE_DSDW_END_LSB	

112212FC AFE_DSDW_CUR AFE DSDW Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DSDW_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DSDW_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DSDW_CUR	**Indicates the current address of the DSDW input buffer.**

11221300 AFE_VUL_BASE AFE VUL Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_VUL_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_VUL_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
31:3		AFE_VUL_BASE	**Base address of the VUL input in master mode.** Always set AFE_VUL_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.

11221308 AFE_VUL_END AFE VUL End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_VUL_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_VUL_END													AFE_VUL_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3		AFE_VUL_END	**Ending address of the VUL input in master mode.** Always set AFE_VUL_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0		AFE_VUL_END_LSB	

1122130C AFE_VUL_CUR AFE VUL Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_VUL_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_VUL_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_VUL_CUR	**Indicates the current address of the VUL input buffer.**

11221310 AFE_UL2_BASE AFE UL2 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL2_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL2_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
31:3		AFE_UL2_BASE	**Base address of the UL2 input in master mode.** Always set AFE_UL2_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.

11221318 AFE_UL2_END AFE UL2 End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL2_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL2_END													AFE_UL2_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3		AFE_UL2_END	**Ending address of the UL2 input in master mode.** Always set AFE_UL2_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0		AFE_UL2_END_LSB	

1122131C AFE_UL2_CUR AFE UL2 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL2_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL2_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_UL2_CUR	**Indicates the current address of the UL2 input buffer.**

11221320 AFE_UL3_BASE AFE UL3 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL3_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL3_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
31:3		AFE_UL3_BASE	**Base address of the UL3 input in master mode.** Always set AFE_UL3_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.

11221328 AFE_UL3_END AFE UL3 End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL3_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL3_END													AFE_UL3_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3		AFE_UL3_END	**Ending address of the UL3 input in master mode.** Always set AFE_UL3_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0		AFE_UL3_END_LSB	

Bit(s)	Mnemonic	Name	Description

1122132C AFE_UL3_CUR AFE UL3 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL3_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL3_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_UL3_CUR	**Indicates the current address of the UL3 input buffer.**

11221330 AFE_UL4_BASE AFE UL4 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL4_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL4_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
31:3		AFE_UL4_BASE	**Base address of the UL4 input in master mode.** Always set AFE_UL4_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.

11221338 AFE_UL4_END AFE UL4 End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL4_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL4_END													AFE_UL4_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3		AFE_UL4_END	**Ending address of the UL4 input in master mode.** Always set AFE_UL4_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0		AFE_UL4_END_LSB	

1122133C AFE_UL4_CUR AFE UL4 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL4_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL4_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_UL4_CUR	**Indicates the current address of the UL4 input buffer.**

11221340 AFE_UL5_BASE AFE UL5 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL5_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL5_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
31:3		AFE_UL5_BASE	**Base address of the UL5 input in master mode.** Always set AFE_UL5_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.

11221348 AFE_UL5_END AFE UL5 End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL5_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL5_END													AFE_UL5_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3		AFE_UL5_END	**Ending address of the UL5 input in master mode.** Always set AFE_UL5_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0		AFE_UL5_END_LSB	

1122134C AFE_UL5_CUR AFE UL5 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL5_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL5_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_UL5_CUR	**Indicates the current address of the UL5 input buffer.**

Bit(s)	Mnemonic	Name	Description

11221350 AFE_UL6_BASE AFE UL6 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL6_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL6_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
31:3		AFE_UL6_BASE	**Base address of the UL6 input in master mode.** Always set AFE_UL6_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.

11221358 AFE_UL6_END AFE UL6 End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL6_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL6_END													AFE_UL6_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3		AFE_UL6_END	**Ending address of the UL6 input in master mode.** Always set AFE_UL6_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0		AFE_UL6_END_LSB	

1122135C AFE_UL6_CUR AFE UL6 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL6_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL6_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_UL6_CUR	**Indicates the current address of the UL6 input buffer.**

11221360 AFE_ULMCH_BASE AFE ULMCH Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_ULMCH_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_ULMCH_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
31:3		AFE_ULMCH_BASE	**Base address of the ULMCH input in master mode.** Always set AFE_ULMCH_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.

11221368 AFE_ULMCH_END AFE ULMCH End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_ULMCH_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_ULMCH_END													AFE_ULMCH_END_LSB		
Type	RW													RO		

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3		AFE_ULMCH_END	**Ending address of the ULMCH input in master mode.** Always set AFE_ULMCH_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0		AFE_ULMCH_END_LSB	

1122136C AFE_ULMCH_CUR AFE ULMCH Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_ULMCH_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_ULMCH_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_ULMCH_CUR	**Indicates the current address of the ULMCH input buffer.**

11221370 AFE_DAI_BASE AFE DAI Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221378 AFE_DAI_END AFE_DAI_END 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1122137C AFE_DAI_CUR AFE DAI Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221380 AFE_MOD_DAI_BASE AFE MOD_DAI Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_MOD_DAI_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_MOD_DAI_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
31:3		AFE_MOD_DAI_BASE	**Base address of the MOD_DAI input in master mode. Always set AFE_MOD_DAI_BASE[2:0]**

Bit(s)	Mnemonic	Name	Description
			= 3'h0 for the convenience of the hardware implementation.

11221388 AFE_MOD_DAI_END AFE_MOD_DAI_END 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_MOD_DAI_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_MOD_DAI_END													AFE_MOD_DAI_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3		AFE_MOD_DAI_END	**Ending address of the MOD_DAI input in master mode. Always set AFE_MOD_DAI_END[2:0] = 3'h7 for the convenience of the hardware implementation.**
2:0		AFE_MOD_DAI_END_LSB	

1122138C AFE_MOD_DAI_CUR AFE MOD_DAI Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_MOD_DAI_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_MOD_DAI_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_MOD_DAI_CUR	**Indicates the current address of the MOD_DAI input buffer.**

112213A0 AFE_DMA_BASE AFE DMA Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DMA_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DMA_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DMA_BASE	**Base address of the DMA in master mode. Always set AFE_DMA_BASE[3:0] = 4'h0 for the convenience of the hardware implementation.**

112213A4 AFE_DMA_CUR AFE DMA Read Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DMA_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DMA_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DMA_CUR	**Indicates the current address of the DMA input buffer.**

112213A8 AFE_DMA_END AFE_DMA_END 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DMA_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DMA_END												AFE_DMA_END_LSB			
Type	RW												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DMA_END	**Ending address of the DMA in master mode. Always set AFE_DMA_END[3:0] = 4'hf for the convenience of the hardware implementation.**
3:0		AFE_DMA_END_LSB	

112213AC AFE_DMA_WR_CUR AFE DMA Write Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																AFE_DMA_WR_CUR
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DMA_WR_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16:0		AFE_DMA_WR_CUR	**Indicates the current address of the DMA output SRAM.**

112213B0 AFE_DMA_CON0 AFE DMA Control Register 0 00000211

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												AFE_DMA_NEXT_OFF	Reserved	AFE_DMA_RD_COMP_EN	AFE_DL1_ALL_COMP	AFE_DL1_AUTO_OFF
Type												RW	RW	RW	RO	RW
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DMA_ALL_COMP	AFE_DMA_RD_COMP	AFE_DMA_1st_COMP	AFE_DL1_AUTO_ON	AFE_DMA_INTR	AFE_DMA_INTR_CLR	AFE_DMA_PBUF_SIZE		AFE_DMA_MAXLEN				AFE_DMA_MINLEN			
Type	RO	RO	RO	RW	RO	RW	RW		RW				RW			
Reset	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1

Bit(s)	Mnemonic	Name	Description
20		AFE_DMA_NEXT_OFF	**Sets up the DMA read DRAM method.** 0: DMA read DRAM with Ping-Pong Mode 1: DMA read DRAM with Single Mode
19		Reserved	
18		AFE_DMA_RD_COMP_EN	**Enable the unit read complete sent to DRAMC self-refresh.** 0: DMA read DRAM Unit complete signal output to DRAMC disable 1: DMA read DRAM Unit complete signal output to DRAMC enable
17		AFE_DL1_ALL_COMP	**Indicates that downlink 1 read all the data transferred from DRAM by DMA completely.**
16		AFE_DL1_AUTO_OFF	**Sets up the downlink 1 auto stop to read AUDSYSRAM with the stauts of AFE_DMA_CON0[17].** 0: Disable the auto-off option 1: Enable the auto-off option
15		AFE_DMA_ALL_COMP	**Indicates that DMA transfer all the data from DRAM to AUDSYSRAM completely.**
14		AFE_DMA_RD_COMP	**Indicates that DMA transfer the unit data from DRAM to AUDSYSRAM completely.**
13		AFE_DMA_1st_COMP	**Indicates that DMA transfer the first unit data from DRAM to AUDSYSRAM completely.**
12		AFE_DL1_AUTO_ON	**Sets up the downlink 1 auto start to read AUDSYSRAM with the stauts of AFE_DMA_CON0[13].** 0: Disable the auto-on option 1: Enable the auto-on option
11		AFE_DMA_INTR	**Indicates the interrupt status of DMA.**
10		AFE_DMA_INTR_CLR	**Clear the interrupt stauts AFE_DMA_CON0[11], and need set to 0 again if the interrupt is cleared.** 0: No 1: Clear the interrupt status

Bit(s)	Mnemonic	Name	Description
9:8		AFE_DMA_PBUF_SIZE	
7:4		AFE_DMA_MAXLEN	**0: not support** 1: 16 byte burst
3:0		AFE_DMA_MINLEN	**0: not support** 1: 16 byte burst

112213B4 AFE_DMA_THRESHOLD AFE DMA Threshold amount for downlink output FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DMA_THRESHOLD															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DMA_THRESHOLD															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DMA_THRESHOLD	**Sets up the threshold of downlink output amount to trigger AFE DMA agent Ping-Pong transaction.**

112213B8 AFE_DMA_INTR_SIZE AFE DMA Interrupt size for DMA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DMA_INTR_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DMA_INTR_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DMA_INTR_SIZE	**Sets up the remain size of DMA source content to generate CPU wakeup interrupt.**

Bit(s)	Mnemonic	Name	Description

112213BC AFE_DMA_NEXT_INTR AFE_DMA Next Interrupt Size for DMA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DMA_NEXT_INTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DMA_NEXT_INTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DMA_NEXT_INTR	**Sets up the remain size of DMA source content to generate CPU wakeup interrupt.**

112213C0 AFE_DMA_NEXT_BASE AFE DMA Next Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DMA_NEXT_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DMA_NEXT_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DMA_NEXT_BASE	**Base address of the DMA in master mode. Always set AFE_DMA_BASE[3:0] = 4'h0 for the convenience of the hardware implementation.**

112213C8 AFE_DMA_NEXT_END AFE_DMA_NEXT_END 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DMA_NEXT_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DMA_NEXT_END												AFE_DMA_NEXT_END_LSB			
Type	RW												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:4		AFE_DMA_NEXT_END	**Ending address of the DMA in master mode. Always set AFE_DMA_END[3:0] = 4'hf for the convenience of the hardware implementation.**
3:0		AFE_DMA_NEXT_END_LSB	

112213D0 AFE_TDM_IN_BASE AFE TDM IN Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_TDM_IN_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_IN_BASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Mnemonic	Name	Description
31:3		AFE_TDM_IN_BASE	**Base address of the TDM IN input in master mode.** Always set AFE_TDM_IN_BASE[2:0] = 3'h0 for the convenience of the hardware implementation.

112213D4 AFE_TDM_IN_CUR AFE TDM IN Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_TDM_IN_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_IN_CUR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_TDM_IN_CUR	**Indicates the current address of the TDM IN input buffer.**

112213D8 AFE_TDM_IN_END AFE TDM IN End Address Register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_TDM_IN_END															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_IN_END													AFE_TDM_IN_END_LSB		
Type	RW													RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:3		AFE_TDM_IN_END	**Ending address of the TDM IN input in master mode.** Always set AFE_TDM_IN_END[2:0] = 3'h7 for the convenience of the hardware implementation.
2:0		AFE_TDM_IN_END_LSB	

11221400 AFE_AWB_CHK_SUM1 AFE_AWB_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_AWB_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_AWB_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_AWB_CHK_SUM1	**Indicates the L-ch buffer data of audio write back 1.**

11221404 AFE_AWB_CHK_SUM2 AFE_AWB_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_AWB_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_AWB_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_AWB_CHK_SUM2	**Indicates the R-ch buffer data of audio write back 1.**

11221418 AFE_AWB2_CHK_SUM1 AFE_AWB2_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_AWB2_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_AWB2_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_AWB2_CHK_SUM1	**Indicates the L-ch buffer data of audio write back 2.**

1122141C AFE_AWB2_CHK_SUM2 AFE_AWB2_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_AWB2_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_AWB2_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_AWB2_CHK_SUM2	**Indicates the R-ch buffer data of audio write back 2.**

11221430 AFE_DSDW_CHK_SUM1 AFE_DSDW_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DSDW_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DSDW_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DSDW_CHK_SUM1	**Indicates the L-ch buffer data of dsd encoder write.**

11221434 AFE_DSDW_CHK_SUM2 AFE_DSDW_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DSDW_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DSDW_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DSDW_CHK_SUM2	**Indicates the R-ch buffer data of dsd encoder write.**

11221450 AFE_VUL_CHK_SUM1 AFE_VUL_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_VUL_CHK_SUM1															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_VUL_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_VUL_CHK_SUM1	**Indicates the L-ch buffer data of uplink 1.**

11221454 AFE_VUL_CHK_SUM2 AFE_VUL_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_VUL_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_VUL_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_VUL_CHK_SUM2	**Indicates the R-ch buffer data of uplink 1.**

11221458 AFE_UL2_CHK_SUM1 AFE_UL2_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL2_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL2_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_UL2_CHK_SUM1	**Indicates the L-ch buffer data of uplink 2.**

1122145C AFE_UL2_CHK_SUM2 AFE_UL2_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL2_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL2_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_UL2_CHK_SUM2	**Indicates the R-ch buffer data of uplink 2.**

11221460 AFE_UL3_CHK_SUM1 AFE_UL3_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL3_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL3_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_UL3_CHK_SUM1	**Indicates the L-ch buffer data of uplink 3.**

11221464 AFE_UL3_CHK_SUM2 AFE_UL3_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL3_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL3_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_UL3_CHK_SUM2	**Indicates the R-ch buffer data of uplink 3.**

11221468 AFE_UL4_CHK_SUM1 AFE_UL4_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL4_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL4_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_UL4_CHK_SUM1	**Indicates the L-ch buffer data of uplink 4.**

1122146C AFE_UL4_CHK_SUM2 AFE_UL4_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL4_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL4_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_UL4_CHK_SUM2	**Indicates the R-ch buffer data of uplink 4.**

11221470 AFE_UL5_CHK_SUM1 AFE_UL5_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL5_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	AFE_UL5_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_UL5_CHK_SUM1	**Indicates the L-ch buffer data of uplink 5.**

11221474 AFE_UL5_CHK_SUM2 AFE_UL5_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL5_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL5_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_UL5_CHK_SUM2	**Indicates the R-ch buffer data of uplink 5.**

11221478 AFE_UL6_CHK_SUM1 AFE_UL6_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_UL6_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL6_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_UL6_CHK_SUM1	**Indicates the L-ch buffer data of uplink 6.**

1122147C AFE_UL6_CHK_SUM2 AFE_UL6_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	AFE_UL6_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_UL6_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_UL6_CHK_SUM2	**Indicates the R-ch buffer data of uplink 6.**

11221480 AFE_ULM_CHK_SUM1 AFE_ULM_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_ULM_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_ULM_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_ULM_CHK_SUM1	**Indicates the L-ch buffer data of uplink multi-channel.**

11221484 AFE_ULM_CHK_SUM2 AFE_ULM_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_ULM_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_ULM_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_ULM_CHK_SUM2	**Indicates the R-ch buffer data of uplink multi-channel.**

Bit(s)	Mnemonic	Name	Description

11221490 AFE_DL1_CHK_SUM1 AFE_DL1_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL1_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL1_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL1_CHK_SUM1	**Indicates the L-ch buffer data of downlink 1.**

11221494 AFE_DL1_CHK_SUM2 AFE_DL1_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL1_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL1_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL1_CHK_SUM2	**Indicates the R-ch buffer data of downlink 1.**

11221498 AFE_DL1_CHK_SUM3 AFE_DL1_CHK_SUM3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL1_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL1_CHK_SUM1															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL1_CHK_SUM1	**Indicates the L-ch data of downlink 1.**

1122149C AFE_DL1_CHK_SUM4 AFE_DL1_CHK_SUM4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL1_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL1_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL1_CHK_SUM2	**Indicates the R-ch data of downlink 1.**

112214A0 AFE_DL2_CHK_SUM1 AFE_DL2_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL2_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL2_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL2_CHK_SUM1	**Indicates the L-ch buffer data of downlink 2.**

112214A4 AFE_DL2_CHK_SUM2 AFE_DL2_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL2_CHK_SUM2															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL2_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL2_CHK_SUM2	**Indicates the R-ch buffer data of downlink 2.**

112214B0 AFE_DL3_CHK_SUM1 AFE_DL3_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL3_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL3_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL3_CHK_SUM1	**Indicates the L-ch buffer data of downlink 3.**

112214B4 AFE_DL3_CHK_SUM2 AFE_DL3_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL3_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL3_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL3_CHK_SUM2	**Indicates the R-ch buffer data of downlink 3.**

112214C0 AFE_DL4_CHK_SUM1 AFE_DL4_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL4_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL4_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL4_CHK_SUM1	**Indicates the L-ch buffer data of downlink 4.**

112214C4 AFE_DL4_CHK_SUM2 AFE_DL4_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL4_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL4_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL4_CHK_SUM2	**Indicates the R-ch buffer data of downlink 4.**

112214D0 AFE_DL5_CHK_SUM1 AFE_DL5_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL5_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL5_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL5_CHK_SUM1	**Indicates the L-ch buffer data of downlink 5.**

112214D4 AFE_DL5_CHK_SUM2 AFE_DL5_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL5_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL5_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL5_CHK_SUM2	**Indicates the R-ch buffer data of downlink 5.**

112214E0 AFE_DL6_CHK_SUM1 AFE_DL6_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL6_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL6_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL6_CHK_SUM1	**Indicates the L-ch buffer data of downlink 6.**

112214E4 AFE_DL6_CHK_SUM2 AFE_DL6_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL6_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	AFE_DL6_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL6_CHK_SUM2	**Indicates the R-ch buffer data of downlink 6.**

112214F0 AFE_ARB1_CHK_SUM1 AFE_ARB1_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_ARB1_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_ARB1_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_ARB1_CHK_SUM1	**Indicates the L-ch buffer data of audio read back.**

112214F4 AFE_ARB1_CHK_SUM2 AFE_ARB1_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_ARB1_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_ARB1_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_ARB1_CHK_SUM2	**Indicates the R-ch buffer data of audio read back.**

11221500 AFE_DSDR_CHK_SUM1 AFE_DSDR_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DSDR_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DSDR_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DSDR_CHK_SUM1	**Indicates the L-ch buffer data of dsd encoder.**

11221504 AFE_DSDR_CHK_SUM2 AFE_DSDR_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DSDR_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DSDR_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DSDR_CHK_SUM2	**Indicates the R-ch buffer data of dsd encoder read.**

11221510 AFE_DLMCH_CHK_SUM1 AFE_DLMCH_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DLMCH_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DLMCH_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DLMCH_CHK_SUM1	**Indicates the ch-1 buffer data of downlink multi-channel.**

11221514 AFE_DLMCH_CHK_SUM2 AFE_DLMCH_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DLMCH_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DLMCH_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DLMCH_CHK_SUM2	**Indicates the ch-3 buffer data of downlink multi-channel.**

11221518 AFE_DLMCH_CHK_SUM3 AFE_DLMCH_CHK_SUM3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DLMCH_CHK_SUM3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DLMCH_CHK_SUM3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DLMCH_CHK_SUM3	**Indicates the ch-5 buffer data of downlink multi-channel.**

1122151C AFE_DLMCH_CHK_SUM4 AFE_DLMCH_CHK_SUM4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	AFE_DLMCH_CHK_SUM4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DLMCH_CHK_SUM4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DLMCH_CHK_SUM4	**Indicates the ch-7 buffer data of downlink multi-channel.**

11221520 AFE_TDM_OUT_CHK_SUM1 AFE_TDM_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_TDM_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_TDM_CHK_SUM1	**Indicates the ch-0 buffer data of tdm out.**

11221524 AFE_TDM_OUT_CHK_SUM2 AFE_TDM_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_TDM_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_TDM_CHK_SUM2	**Indicates the ch-2 buffer data of tdm out.**

11221528 AFE_TDM_OUT_CHK_SUM3 AFE_TDM_CHK_SUM3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_TDM_CHK_SUM3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_CHK_SUM3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_TDM_CHK_SUM3	**Indicates the ch-4 buffer data of tdm out.**

1122152C AFE_TDM_OUT_CHK_SUM4 AFE_TDM_CHK_SUM4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_TDM_CHK_SUM4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_CHK_SUM4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_TDM_CHK_SUM4	**Indicates the ch-6 buffer data of tdm out.**

11221530 AFE_SPDIF_CHK_SUM1 AFE_SPDIF_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_SPDIF_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_SPDIF_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_SPDIF_CHK_SUM1	**Indicates the buffer data of spdif out.**

11221538 AFE_SPDIF2_CHK_SUM1 AFE_SPDIF2_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221544 AFE_DL_COUNTER_CON AFE_DL_COUNTER_CON 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DL6_RD_COUNTER_RST	DL5_RD_COUNTER_RST	DL4_RD_COUNTER_RST	DL3_RD_COUNTER_RST	DL2_RD_COUNTER_RST	DL1_RD_COUNTER_RST
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5		DL6_RD_COUNTER_RST	**Toggle to reset dl read counter**

Bit(s)	Mnemonic	Name	Description
4		DL5_RD_COUNTER_RST	**Toggle to reset dl read counter**
3		DL4_RD_COUNTER_RST	**Toggle to reset dl read counter**
2		DL3_RD_COUNTER_RST	**Toggle to reset dl read counter**
1		DL2_RD_COUNTER_RST	**Toggle to reset dl read counter**
0		DL1_RD_COUNTER_RST	**Toggle to reset dl read counter**

11221550 AFE_TDM_IN_CHK_SUM1 AFE_TDM_IN_CHK_SUM1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_TDM_IN_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_IN_CHK_SUM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_TDM_IN_CHK_SUM1	**Indicates the latched lch buffer data of tdm in.**

11221554 AFE_TDM_IN_CHK_SUM2 AFE_TDM_IN_CHK_SUM2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_TDM_IN_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_IN_CHK_SUM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_TDM_IN_CHK_SUM2	**Indicates the latched rch buffer data of tdm in.**

11221558 AFE_TDM_IN_CHK_SUM3 AFE_TDM_IN_CHK_SUM3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_TDM_IN_CHK_SUM3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_IN_CHK_SUM3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_TDM_IN_CHK_SUM3	**Indicates the lch data of tdm out.**

1122155C AFE_TDM_IN_CHK_SUM4 AFE_TDM_IN_CHK_SUM4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_TDM_IN_CHK_SUM4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_IN_CHK_SUM4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_TDM_IN_CHK_SUM4	**Indicates the rch data of tdm out.**

11221560 AFE_TDM_IN_CHK_SUM5 AFE_TDM_IN_CHK_SUM5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	AFE_TDM_IN_CHK_SUM5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_IN_CHK_SUM5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_TDM_IN_CHK_SUM5	**Indicates the lch data to pre-fetch**

11221564 AFE_TDM_IN_CHK_SUM6 AFE_TDM_IN_CHK_SUM6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_TDM_IN_CHK_SUM6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_TDM_IN_CHK_SUM6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_TDM_IN_CHK_SUM6	**Indicates the rch data to pre-fetch**

11221568 AFE_DL1_RD_COUNTER AFE_DL1_RD_COUNTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL1_RD_COUNTER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL1_RD_COUNTER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL1_RD_COUNTER	**Counter of total data number for dl path**

1122156C AFE_DL2_RD_COUNTER AFE_DL2_RD_COUNTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL2_RD_COUNTER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL2_RD_COUNTER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL2_RD_COUNTER	**Counter of total data number for dl path**

11221570 AFE_DL3_RD_COUNTER AFE_DL3_RD_COUNTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL3_RD_COUNTER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL3_RD_COUNTER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL3_RD_COUNTER	**Counter of total data number for dl path**

11221574 AFE_DL4_RD_COUNTER AFE_DL4_RD_COUNTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL4_RD_COUNTER															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL4_RD_COUNTER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL4_RD_COUNTER	**Counter of total data number for dl path**

11221578 AFE_DL5_RD_COUNTER AFE_DL5_RD_COUNTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL5_RD_COUNTER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL5_RD_COUNTER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL5_RD_COUNTER	**Counter of total data number for dl path**

1122157C AFE_DL6_RD_COUNTER AFE_DL6_RD_COUNTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_DL6_RD_COUNTER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_DL6_RD_COUNTER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_DL6_RD_COUNTER	**Counter of total data number for dl path**

Bit(s)	Mnemonic	Name	Description

112215D0 AFE_MEMIF_MON0 AFE Memory Interface Monitor Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VUL_RCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL1_LCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		VUL_RCH_DATA	**Memory interface UL1 right channel data output.**
15:0		DL1_LCH_DATA	**Memory interface DL1 left channel data output.**

112215D4 AFE_MEMIF_MON1 AFE Memory Interface Monitor Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSDR_RCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARB1_LCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DSDR_RCH_DATA	**Memory interface DSDR right channel data output.**
15:0		ARB1_LCH_DATA	**Memory interface ARB1 left channel data output.**

112215D8 AFE_MEMIF_MON2 AFE Memory Interface Monitor Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MOD_DAI_DATA															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAI_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		MOD_DAI_DATA	**Memory interface MOD_DAI data input.**
15:0		DAI_DATA	**Memory interface DAI data input.**

112215DC AFE_MEMIF_MON3 AFE Memory Interface Monitor Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ULMCH_RCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ULMCH_LCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		ULMCH_RCH_DATA	**Memory interface ULMCH right channel data input.**
15:0		ULMCH_LCH_DATA	**Memory interface ULMCH left channel data input.**

112215E0 AFE_MEMIF_MON4 AFE Memory Interface Monitor Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DSDW_RCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWB_LCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DSDW_RCH_DATA	**Memory interface DSDW right channel data input.**
15:0		AWB_LCH_DATA	**Memory interface AWB left channel data input.**

11220054 AFE_TDM_CON1 TDM Config 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LRCK_TDM_WIDTH											DAC_BIT_NUM				
Type	RW											RW				
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CHANNEL_NUM			CHANNEL_BCK_CYCLES		WLEN					LEFT_ALIGN	DELAY_DATA	LRCK_INVERSE	BCK_INVERSE	TDM_EN
Type		RW			RW		RW					RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:23		LRCK_TDM_WIDTH	**Set LRCK width as number of BCK cycles.** 0: LRCK is 1 BCK cycle 1: LRCK is 2 BCK cycles 2: LRCK is 3 BCK cycles 254: LRCK is 255 BCK cycles
20:16		DAC_BIT_NUM	**Specify sample bit width for RJ format. This format is not available for TDM.**
14:12		CHANNEL_NUM	**Select number of channels for each sdata.** 0: 2 channels 1: 4 channels 2: 8 channels 3: 12 channels 4: 16 channels
11:10		CHANNEL_BCK_CYCLES	**Select number of BCK cycles for each channel.** 0: 16 BCK cycles

Bit(s)	Mnemonic	Name	Description
			1: 24 BCK cycles 2: 32 BCK cycles
9:8		WLEN	**Data word length.** 1: 16-bit 2: 24-bit 3: 32-bit
4		LEFT_ALIGN	**Set this bit for EIAJ & I2S mode.** 0: Sample is not aligned to MSB bit. 1: Sample is aligned to MSB bit.
3		DELAY_DATA	**Set this bit for I2S mode.** 0: MSB bit data is 0 BCK cycle behind LRCK trigger edge. Set for EIAJ mode. 1: MSB bit data is 1 BCK cycle behind LRCK trigger edge. Set for I2S mode.
2		LRCK_INVERSE	**TDM LRCK inverse.** 0: LRCK no inverse 1: LRCK inverse
1		BCK_INVERSE	**TDM BCK inverse.** 0: BCK no inverse 1: BCK inverse
0		TDM_EN	**TDM enable. Enable this bit when all other configurations are set. Including sampling rate.** 0: disable TDM 1: enable TDM

11220058 AFE_TDM_CON2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_FIX_VALUE									TDM_I2S_LOOPBACK_CH		TDM_I2S_LOOPBACK				TDM_FIX_VAL

																UE_SEL
Type	RW									RW		RW				RW
Reset	0	0	0	0	0	0	0	0		0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CH_PAIR_SOUT3				ST_CH_PAIR_SOUT2				ST_CH_PAIR_SOUT1				ST_CH_PAIR_SOUT0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		TDM_FIX_VALUE	**Set fix value send on TDM TX.**
22:21		TDM_I2S_LOOPBACK_CH	**Select hdmi sdatax for loopback test.** 00: select hdmi_sdata0 for loopback test 01: select hdmi_sdata1 for loopback test 10: select hdmi_sdata2 for loopback test 11: select hdmi_sdata3 for loopback test
20		TDM_I2S_LOOPBACK	**Set TDM to I2S path.** 0: disable TDM to I2S path 1: enable TDM to I2S path
16		TDM_FIX_VALUE_SEL	**TDM enable send fix value on TX.** 0: Disable fix value on TX 1: Enable fix value on TX
15:12		ST_CH_PAIR_SOUT3	**Set starting channels for SOUT0. Remaining channels are sent in assending order. e.g.** 0: channels sent will be O30, O31, O32, O33, O34, O35, O36, O37 1: channels sent will be O32, O33, O34, O35, O36, O37,0 2. channels sent will be O34, O35, O36, O37, 0 3: channels sent will be O36, O37, 0 4: channels sent will be 0 0: Channel starts from O30/O31. 1: Channel starts from O32/O33.

Bit(s)	Mnemonic	Name	Description
			2: Channel starts from O34/O35. 3: Channel starts from O36/O37. 4: Channel starts from O38/O39. 5: Channel starts from O40/O41. 6: Channel starts from O42/O43. 7: Channel starts from O44/O45.
11:8		ST_CH_PAIR_SOUT2	**Set starting channels for SOUT2. Remaining channels are sent in assending order. e.g.** 0: channels sent will be O30, O31, O32, O33, O34, O35, O36, O37 1: channels sent will be O32, O33, O34, O35, O36, O37,0 2. channels sent will be O34, O35, O36, O37, 0 3: channels sent will be O36, O37, 0 4: channels sent will be 0 0: Channel starts from O30/O31. 1: Channel starts from O32/O33. 2: Channel starts from O34/O35. 3: Channel starts from O36/O37. 4: Channel starts from O38/O39. 5: Channel starts from O40/O41. 6: Channel starts from O42/O43. 7: Channel starts from O44/O45.
7:4		ST_CH_PAIR_SOUT1	**Set starting channels for SOUT3. Remaining channels are sent in assending order. e.g.** 0: channels sent will be O30, O31, O32, O33, O34, O35, O36, O37 1: channels sent will be O32, O33, O34, O35, O36, O37,0 2. channels sent will be O34, O35, O36, O37, 0 3: channels sent will be O36, O37, 0 4: channels sent will be 0

Bit(s)	Mnemonic	Name	Description
			0: Channel starts from O30/O31. 1: Channel starts from O32/O33. 2: Channel starts from O34/O35. 3: Channel starts from O36/O37. 4: Channel starts from O38/O39. 5: Channel starts from O40/O41. 6: Channel starts from O42/O43. 7: Channel starts from O44/O45.
3:0		ST_CH_PAIR_SOUT0	

1122005C AFE_SINEGNE_CON_TDM 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				sgen_tdm_input_en				c_dac_en_tdm				c_mute_sw_tdm2				c_freq_div_tdm2
Type				RW				RW				RW				RW
Reset				0				0				0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_freq_div_tdm2							c_mute_sw_tdm1				c_freq_div_tdm1				
Type	RW							RW				RW				
Reset	0	0	0	0				0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28		sgen_tdm_input_en	
24		c_dac_en_tdm	
20		c_mute_sw_tdm2	
16:12		c_freq_div_tdm2	
8		c_mute_sw_tdm1	

Bit(s)	Mnemonic	Name	Description
4:0		c_freq_div_tdm1	

11220074 AFE_SINEGNE_CON_TDM_IN 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				sgen_tdmin_input_en				c_dac_en_tdm_in				c_mute_sw_tdm_in_2	c_amp_div_tdm_in_2			c_freq_div_tdm_in_2
Type				RW				RW				RW	RW			RW
Reset				0				0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_freq_div_tdm_in_2							c_mute_sw_tdm_in_1	c_amp_div_tdm_in_1			c_freq_div_tdm_in_1				
Type	RW							RW	RW			RW				
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28		sgen_tdmin_input_en	
24		c_dac_en_tdm_in	
20		c_mute_sw_tdm_in_2	
19:17		c_amp_div_tdm_in_2	
16:12		c_freq_div_tdm_in_2	
8		c_mute_sw_tdm_in_1	
7:5		c_amp_div_tdm_in_1	
4:0		c_freq_div_tdm_in_1	

11220078 TDMOUT_CLKDIV_CFG TDM OUT CLK DVI Control Register 00F00F03

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	tdmout_ck_div_b												tdmout_ck_div_m			
Type	RW												RW			

Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tdmout_ck_div_m										tdmout_inv_b	tdmout_inv_m		tdmout_mck_sel	tdmout_pdn_b	tdmout_pdn_m
Type	RW										RW	RW		RW	RW	RW
Reset	0	0	0	0	1	1	1	1			0	0		0	1	1

Bit(s)	Mnemonic	Name	Description
31:20		tdmout_ck_div_b	**Divider setting of tdmout_bck, n = [11:0]** tdmout_bck = clock source * [1 / (n+1)]
19:8		tdmout_ck_div_m	**Divider setting of tdmout_bck, n = [11:0]** tdmout_mck = clock source * [1 / (n+1)]
5		tdmout_inv_b	**tdmout_bck clock phase invert** 1: Enable phase invert
4		tdmout_inv_m	**tdmout_mck clock phase invert**
2		tdmout_mck_sel	**sel mck source** 0:270M 1:296M
1		tdmout_pdn_b	**Power down tdm_bck divider** 1: Enable power down
0		tdmout_pdn_m	**Power down tdm_mck divider** 1: Enable power down

11220060 AFE_TDM_IN_CON1 AFE TDM IN Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LRCK_TDM_WIDTH									tdm_in_loopback_ch		tdm_in_loopback		tdm_inout_sync	fast_lrck_cycle_sel	
Type	RW									RW		RW		RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		tdm_channel					tdm_wlen					tdm_lr_swap	tdm_fmt	tdm_lrck_inv	tdm_bck_inv	tdm_en
Type		RW					RW					RW	RW	RW	RW	RW

Reset		0	0	0			0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:23		LRCK_TDM_WIDTH	**Set LRCK width as number of BCK cycles.** 0: LRCK is 1 BCK cycle 1: LRCK is 2 BCK cycles 2: LRCK is 3 BCK cycles 254: LRCK is 255 BCK cycles
22:21		tdm_in_looback_ch	**loopback source for TDM OUT** 0:TDM OUT sdata0 1:TDM OUT sdata1 2:TDM OUT sdata2 3:TDM OUT sdata3
20		tdm_in_looback	**loopback mode** 1 : loopback fromTDM OUT
18		tdm_inout_sync	**tdm IN & OUT sync mode**
17:16		fast_lrck_cycle_sel	**Select number of BCK cycles for each channel.** 0:16BCK 1:24BCK 2:32BCK
14:12		tdm_channel	**Select number of channels for each sdata.** 0:2ch 1:4ch 2:8ch 3:12ch 4:16ch
9:8		tdm_wlen	**Data word length.** 1:16bit 2:24bit 3:32bit
4		tdm_lr_swap	**Set this bit for LR-ch swap** 0: Non-inverse LR ch 1: Inverse LR ch
3		tdm_fmt	**Set this bit for EIAJ & I2S mode.** 0: EIAJ 1: I2S
2		tdm_lrck_inv	**TDM LRCK inverse.**

Bit(s)	Mnemonic	Name	Description
			0: Does not inverse LRCK 1: Inverse LRCK for LJ mode
1		tdm_bck_inv	**TDM BCK inverse.** 0: Non-inverse 1: Inverse
0		tdm_en	**TDM enable. Enable this bit when all other configurations are set. Including sampling rate.** 0: Disable tdm 1: Enable tdm

11220064 AFE_TDM_IN_CON2 AFE TDM IN Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									two_ch_lr_swap							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	odd_flag_cfg								disable_out							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:16		two_ch_lr_swap	**two_ch_lr_swap_en for 16/12/8/4/2ch mode** [1:1:1:1:1:1:1:1] = [ch10 : ch32 : ch54 : ch76 : ch98 : ch1110 : ch1312 : ch1514]
15:8		odd_flag_cfg	**odd_flag_en for 16/12/8/4/2ch mode** [1:1:1:1:1:1:1:1] = [ch01 : ch23 : ch45 : ch67 : ch89 : ch1011 : ch1213 : ch1415]
7:0		disable_out	**disable_out for 16/12/8/4/2ch mode** [1:1:1:1:1:1:1:1] = [ch01 : ch23 : ch45 : ch67 : ch89 : ch1011 : ch1213 : ch1415]

11220068 AFE_TDM_IN_MON1 AFE TDM IN MON Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				update_data				bit_ck				test_mode				int_bcl
Type				RO				RO				RO				RO
Reset				0				0				0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ch_sel					tdm_lrck				tdm_bck				tdm_in_sdata
Type			RO					RO				RO				RO
Reset			0	0				0				0				0

Bit(s)	Mnemonic	Name	Description
28		update_data	
24		bit_ck	
20		test_mode	
16		int_bcl	
13:12		ch_sel	
8		tdm_lrck	
4		tdm_bck	
0		tdm_in_sdata	

1122006C AFE_TDM_IN_MON2 AFE TDM IN MON Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				fast_irck				update_tdm				goto_next_ch_d3t				goto_next_ch
Type				RO				RO				RO				RO
Reset				0				0				0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				new_sample_tdm_d2t				new_sample_tdm				tdm_en_rst				tdm_en_retm
Type				RO				RO				RO				RO

Reset				0				0				0				0

Bit(s)	Mnemonic	Name	Description
28		fast_lrck	
24		update_tdm	
20		goto_next_ch_d3t	
16		goto_next_ch	
12		new_sample_tdm_d2t	
8		new_sample_tdm	
4		tdm_en_rst	
0		tdm_en_retm	

11220070 AFE_TDM_IN_MON3 AFE_TDM_IN_MON Register 2 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								afe_tdm_in_outen	bit_counter							
Type								RO	RO							
Reset								0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lrck_tdm_counter											fast_lrck_counter				
Type	RO											RO				
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24		afe_tdm_in_outen	
23:16		bit_counter	
15:8		lrck_tdm_counter	
4:0		fast_lrck_counter	

1122007C TDMIN_CLKDIV_CFG TDM IN CLK DVI Control Register 00F00F03

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	tdmin_ck_div_b												tdmin_ck_div_m			
Type	RW												RW			
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tdmin_ck_div_m										tdmin_inv_b	tdmin_inv_m		tdmin_mck_sel	tdmin_pdn_b	tdmin_pdn_m
Type	RW										RW	RW		RW	RW	RW
Reset	0	0	0	0	1	1	1	1			0	0		0	1	1

Bit(s)	Mnemonic	Name	Description
31:20		tdmin_ck_div_b	**Divider setting of tdmin_bck, n = [11:0]** tdmin_bck = clock source * [1 / (n+1)]
19:8		tdmin_ck_div_m	**Divider setting of tdmin_bck, n = [11:0]** tdmin_mck = clock source * [1 / (n+1)]
5		tdmin_inv_b	**tdmin_bck clock phase invert** 1: Enable phase invert
4		tdmin_inv_m	**tdmin_mck clock phase invert**
2		tdmin_mck_sel	**sel mck source** 0:270M 1:296M
1		tdmin_pdn_b	**Power down tdm_bck divider** 1: Enable power down
0		tdmin_pdn_m	**Power down tdm_mck divider** 1: Enable power down

11221700 AFE_IRQ_ACC1_CNT AFE IRQ ACC1 Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_IRQ_ACC1_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_ACC1_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_IRQ_ACC1_CNT	

11221704 AFE_IRQ_ACC2_CNT AFE IRQ ACC2 Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_IRQ_ACC2_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_ACC2_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		AFE_IRQ_ACC2_CNT	

11221708 AFE_IRQ_ACC1_CNT_MON1 AFE IRQ ACC1 Counter MON1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1122170C AFE_IRQ_ACC1_CNT_MON2 AFE IRQ ACC1 Counter MON2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

11221710 AFE_TSF_CON WiFi TSF control registers 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							rg_tdmout_auto_en	rg_tdmout_agent_hw_dis		rg_dlmch_auto_en	rg_dl6_auto_en	rg_dl5_auto_en	rg_dl4_auto_en	rg_dl3_auto_en	rg_dl2_auto_en	rg_dl1_auto_en
Type							RW	RW		RW	RW	RW	RW	RW	RW	RW
Reset							0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												rg_dl_agent_hw_dis				connsys_tsf_intr_sel
Type												RW				RW
Reset												1				0

Bit(s)	Mnemonic	Name	Description
25		rg_tdmout_auto_en	
24		rg_tdmout_agent_hw_dis	
22		rg_dlmch_auto_en	
21		rg_dl6_auto_en	
20		rg_dl5_auto_en	
19		rg_dl4_auto_en	
18		rg_dl3_auto_en	
17		rg_dl2_auto_en	
16		rg_dl1_auto_en	

Bit(s)	Mnemonic	Name	Description
4		rg_dl_agent_hw_dis	
0		connsys_tsf_intr_sel	

11221714 AFE_TSF_MON WiFi TSF read out registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																afe_hdmiout_on_retm
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				hdmiout_agent_hw_en_retm			afe_dl2_on_retm	afe_dl1_on_retm			dl2_auto_en_mon	dl1_auto_en_mon				dl_agent_hw_en_retm
Type				RO			RO	RO			RO	RO				RO
Reset				0			0	0			0	0				0

Bit(s)	Mnemonic	Name	Description
16		afe_hdmiout_on_retm	
12		hdmiout_agent_hw_en_retm	
9		afe_dl2_on_retm	
8		afe_dl1_on_retm	
5		dl2_auto_en_mon	
4		dl1_auto_en_mon	
0		dl_agent_hw_en_retm	

11221718 AFE_IRQ_ACC2_CNT_MON AFE IRQ ACC2 Counter MON Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1122171C AFE_IRQ_MCU_CNT11 AFE IRQ11 MCU Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ_MCU_CNT11	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_MCU_CNT11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:0		AFE_IRQ_MCU_CNT11	

11221720 AFE_IRQ_MCU_CNT12 AFE IRQ12 MCU Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ_MCU_CNT12	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_MCU_CNT12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:0		AFE_IRQ_MCU_CNT12	

11221724 AFE_IRQ11_MCU_CNT_MON AFE IRQ11 MCU Count Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ11_CNT_MON	
Type															RO	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ11_CNT_MON															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:0		AFE_IRQ11_CNT_MON	

11221728 AFE_IRQ12_MCU_CNT_MON AFE IRQ12 MCU Count Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															AFE_IRQ12_CNT_MON	
Type															RO	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ12_CNT_MON															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
17:0		AFE_IRQ12_CNT_MON	

1122172C AFE_I2S_UL1_REORDER AFE I2S UL1 REORDER 00000080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									i2s_reorder_32bit_sel	i2s_reorder_ul_sel	i2s_reorder_bswap	i2s_reorder_en			i2s_reorder_chnum	
Type									RW	RW	RW	RW			RW	
Reset									1	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
7		i2s_reorder_32bit_sel	**Reserved** 0: please don't set to 0 in this project 1: default
6		i2s_reorder_ul_sel	**Reserved** 0: default, bypass u1l reorder function 1: ul1 input from reorder function
5		i2s_reorder_bswap	**Reserved** 0: default, not doing byte swapping 1: byte swapping (swapping high low byte in half-Dword)
4		i2s_reorder_en	**Reserved** 0: soft enable bit (default is off) 1: enable reorder function
1:0		i2s_reorder_chnum	**Reserved** 0: 2ch (default is off) 1: 4ch 2: 6ch 3: 8ch

1.26 Memory Stick and SD Card Controller (MSDC 0)

1.26.1 Introduction

The MSDC (Memory Stick and SD card Controller) fully supports functions as follow

- MMC/eMMC4.41 (MSDC0)
- SD memory card specification version 3.0 (MSDC1)
- SDIO card specification version 3.0 (MSDC1)

1.26.2 Features

MSDC0 contains:

- 32-bit access for control registers
- 8-bit/16-bit/32-bit access for FIFO in PIO mode
- Built-in 1K data buffer for transmit and receive
- Built-in CRC circuit
- PIO mode, Basic DMA mode, Descriptor mode for SD/eMMC
- Interrupt capabilities for SDIO
- Does not support SPI mode for SD/MMC memory card
- Does not support suspend/resume for SD/MMC memory card
- Supports SD3.0 SDR104, data rate up to 208x4Mbps
- Supports SD3.0 DDR50, data rate up to 50x4x2Mbps(4-bit with clock dual edge)
- Supports e-MMC boot-up mode (MSDC0)
- 256 programmable serial clock rates on SD/MMC bus from 100kHz to 208MHz

1.26.3 Register Definition

Module name: MSDC0 Base address: (+11230000h)

Address	Name	Width	Register Function
11230000	MSDC_CFG	32	MSDC Configuration Register The register is for general configuration of the MS/SD controller.
11230004	MSDC_IOCON	32	MSDC IO Configuration Register The register contains the receiver path data latch timing control and interface control bits.
11230008	MSDC_PS	32	MSDC Pin Status Register The register is used to storing card detection and write protection pin status. Card detection status can be disabled.
1123000C	MSDC_INT	32	MSDC Interrupt Register The register contains the status of interrupts. Note that the register still shows the status of interrupt even though the interrupt is disabled.
11230010	MSDC_INTEN	32	MSDC Interrupt Enable Register The register contains the related enable bit of interrupts.
11230014	MSDC_FIFOCS	32	MSDC FIFO Control and Status Register

Address	Name	Width	Register Function
			The register contains the control and status of embedded 128B FIFO.
11230018	MSDC_TXDATA	32	MSDC TX Data Port Register The register is for PIO mode only. Used to input MSDC write data to card. The access can be AHB 1B/2B/4B
1123001C	MSDC_RXDATA	32	MSDC RX Data Port Register The register is for PIO mode only. Used to read back MSDC read data from card. The access can be AHB 1B/2B/4B.
11230030	SDC_CFG	32	SD Configuration Register The register is used for configuring the MS/SD Memory Card Controller when it is configured as the host of SD Memory Card. If the controller is configured as the host of Memory Stick, the contents of the register have no impact on the operation of the controller.
11230034	SDC_CMD	32	SD Command Register The register defines a SD Memory Card command and its attributes. Before MS/SD controller issues a transaction onto SD bus, application shall specify other relative settings such as argument for command. After writing the register by the application, MS/SD controller will issue the corresponding transaction onto SD serial bus. If the command is GO_IDLE_STATE, the controller will have serial clock on SD/MMC bus run 128 cycles before issuing the command.
11230038	SDC_ARG	32	SD Argument Register The register contains the argument of the SD/MMC Memory Card command.
1123003C	SDC_STS	32	SD Status Register The register reflects SD bus status and contains MMC stream write status.
11230040	SDC_RESP0	32	SD Response Register 0 The register contains parts of the last SD/MMC Memory Card bus response. See description for the register field SDC_RESP3.
11230044	SDC_RESP1	32	SD Response Register 1 The register contains parts of the last SD/MMC Memory Card bus response. See description for the register field SDC_RESP3.
11230048	SDC_RESP2	32	SD Response Register 2 The register contains parts of the last SD/MMC Memory Card bus response. See description for the register field SDC_RESP3.
1123004C	SDC_RESP3	32	SD Response Register 3 The register contains parts of the last SD/MMC Memory Card bus response. The register fields SDC_RESP0, SDC_RESP1, SDC_RESP2 and SDC_RESP3 are composed of the last SD/MMC Memory card bus response. For response of type R2, that is, response of the command ALL_SEND_CID, SEND_CSD and

Address	Name	Width	Register Function
			SEND_CID, only bit 127 to 0 of response token is stored in the register field SDC_RESP0, SDC_RESP1, SDC_RESP2 and SDC_RESP3. SDC_RESP0 = bit 31~0 SDC_RESP1 = bit 63~32 SDC_RESP2 = bit 95~64 SDC_RESP3 = bit 127~96 For response of type R1b in auto CMD12 or R1 in auto CMD23, bit 39 to 8 of response token is stored in the register field of SDC_RESP3. For the responses of other types, only bit 39 to 8 of response token is stored in the register field SDC_RESP0.
11230050	SDC_BLK_NUM	32	SD Block Number Register This register defines the block number for the block transaction. For single read/write, this register should be set to 1. For multiple read/write, this register should be set to larger than 1. Set to 0 will cause unexpected result.
11230054	SDC_VOL_CHG	32	SD Voltage Change Wait Time Register This register define SD voltage change check wait time
11230058	SDC_CSTS	32	SD Card Status Register After commands with R1 and R1b response, this register will contain the status of the SD/MMC card
1123005C	SDC_CSTS_EN	32	SD Card Status Enable Register This register is used to control which bit of the SDC_CSTS will generate the MSDC_INT.SD_CSTA interrupt.
11230060	SDC_DATCRC_STS	32	SD Card Data CRC Status Register This register reflects the CRC status of data line[7:0]. This register is only for MSDC Read
11230064	SDC_ADV_CFG0	32	SDC Advance Configuration 0 This register used to config sdc advance feature
11230070	EMMC_CFG0	32	EMMC Configuration Register 0 The register is used for boot up mode general configuration of e-MMC version 4.3 and 4.4.
11230074	EMMC_CFG1	32	EMMC Configuration Register 1 The register is used for boot up mode general configuration of e-MMC version 4.3 and 4.4.
11230078	EMMC_STS	32	EMMC Status Register The register reflects the status of e-MMC boot up mode operation.
1123007C	EMMC_IOCON	32	EMMC IO Control Register The register controls the H/W reset pin of e-MMC boot up mode operation.
11230080	SD_ACMD_RESP	32	SD ACMD Response Register This register stores the response of auto command from SD card
11230084	SD_ACMD19_TRG	32	SD ACMD19 Target Register This register is used to select target delay line to run ACMD19 sequence.
11230088	SD_ACMD19_STS	32	SD ACMD19 Status Register This register stores the result of auto command 19 from SD card

Address	Name	Width	Register Function
1123008C	DMA_SA_HIGH4BIT	32	DMA Current Address Resgiter of high 4bit This register contain the start address high 4bit of 36bit address for 64G dram access
11230090	DMA_SA	32	DMA Start Address Register This register contains the start address of the DMA descriptor
11230094	DMA_CA	32	DMA Current Address Register This register contains the current DMA address
11230098	DMA_CTRL	32	DMA Control Register This register is used to control the DMA operation.
1123009C	DMA_CFG	32	DMA Configuration Register This register is used to configure the DMA operation.
112300A0	SW_DBG_SEL	32	MSDC S/W Debug Selection Register This register is used to select S/W debug output
112300A4	SW_DBG_OUT	32	MSDC S/W Debug Output Register This register shows the selected debug output
112300A8	DMA_LENGTH	32	DMA Length Register This register is used to set Basic DMA operation length
112300B0	PATCH_BIT0	32	MSDC Patch Bit Register 0 This register can configure the patch function. For normal function, these bit should keep in default value
112300B4	PATCH_BIT1	32	MSDC Patch Bit Register 1 This register can configure the patch function. For normal function, these bit should keep in default value
112300B8	PATCH_BIT2	32	MSDC Patch Bit Register 2 This register can configure the patch function. For normal function, these bit should keep in default value
112300F0	PAD_TUNE0	32	MSDC Pad Tuning Register0 This register can configure the delay line embedded in Pad Macro
112300F4	PAD_TUNE1	32	MSDC Pad Tuning Register1 This register can configure the delay line embedded in Pad Macro
112300F8	DAT_RD_DLY0	32	MSDC Data Delay Line Register 0 This register can configure the delay line embedded in Pad Macro
112300FC	DAT_RD_DLY1	32	MSDC Data Delay Line Register 1 This register can configure the delay line embedded in Pad Macro
11230100	DAT_RD_DLY2	32	MSDC Data Delay Line Register 2 This register can configure the delay line embedded in Pad Macro
11230104	DAT_RD_DLY3	32	MSDC Data Delay Line Register 3 This register can configure the delay line embedded in Pad Macro
11230110	HW_DBG_SEL	32	MSDC H/W Debug Selection Register This register can select the H/W debug output

Address	Name	Width	Register Function
11230114	MAIN_VER	32	MSDC Main Version Register This register shows the version code of MSDC IP
11230118	ECO_VER	32	MSDC ECO Version Register This register shows the ECO version code of MSDC IP
1123021C	EMMC50_CFG2	32	ahb2axi wrapper control register this register can set wrapper work mode
11230220	EMMC50_CFG3	32	
11230224	EMMC50_CFG4	32	
11230228	SDC_FIFO_CFG	32	

11230000 MSDC_CFG MSDC Configuration Register 02000099

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			BW_SEL				SCLK_STOP_SEL				CARD_CK_MODE		CARD_CK_DIV			
Type			RW				RW				RW		RW			
Reset			0				1				0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CARD_CK_DIV								CARD_CK_STABLE	BV_1P8_PASS	BV_1P8_START_DET	CARD_CK_DRV_EN	PIO_MODE	RST	CARD_CK_PWDN	MSDC
Type	RW								RU	RU	RW	RW	RW	A0	RW	RW
Reset	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
29	**BWSEL**	BW_SEL	**save power for low throughput requirement** 1'b0:the memory provide diff throughput for diff msdc speed mode 1'b1:memory provide highest throughput for all speed mode
25	**SCLKSTOPSEL**	SCLK_STOP_SEL	**In DDR mode,stop SCLK when device is idle whether check SCLK phase** 1'b0: stop sclk no check SCLK phase 1'b1 : stop sclk check SCLK phase,fix 1/4T sclk glitch in DDR mode
21:20	**CCKMD**	CARD_CK_MODE	**2'b00: Use clock divider output which divided by msdc_src_ck as msdc_ck, bit[15]~bit[8] should be programmed.**

Bit(s)	Mnemonic	Name	Description
			2'b01: Use msdc_src_ck as msdc_ck, bit[15]~bit[8] is ignored. 2'b10: DDR mode, also use clock divider output which divided by msdc_src_ck as msdc_ck, bit[15]~bit[8] should be programmed. 2'b11: HS400 mode,also use clock divider output and use msdc_src_ck as msdc_ck, bit[15]~bit[8] should be programmed 2'b00: Use clock divider output which divided by msdc_src_ck as msdc_ck, bit[19]~bit[8] should be programmed. 2'b01: Use msdc_src_ck as msdc_ck, bit[19]~bit[8] is ignored. 2'b10: DDR mode, also use clock divider output which divided by msdc_src_ck as msdc_ck, bit[19]~bit[8] should be programmed. 2'b11: HS400 mode,also use clock divider output or use msdc_src_ck as msdc_ck.when HS400_CK_MODE set to 0, bit[15]~bit[8] should be programmed.When HS400_CK_MODE set to 1,bit[19]~bit[8] is ignored.
19:8	**CCKDIV**	CARD_CK_DIV	**MS/SD Card clock divider** The register field controls clock frequency of serial clock on MS/SD bus. Please refer to Data Line Latching Timing Diagram and Response Latching Timing Diagram. For non-DDR mode, msdc_ck equals SD bus clock. (Ex: For SDR25 or HS, msdc_ck and SD bus clock will be 50MHz) For DDR mode, msdc_ck denotes the MSDC internal clock which will be dobule to SD bus clock. (Ex: For DDR50, msdc_ck should be set to 100MHz and bus clock will be 50MHz) 12'b000000000000: msdc_ck =(1/2) * msdc_src_ck 12'b000000000001: msdc_ck = (1/(4*1)) * msdc_src_ck 12'b00000010: msdc_ck = (1/(4*2)) * msdc_src_ck 12'b000000000011: msdc_ck = (1/(4*3))* msdc_src_ck 12'b000000010000: msdc_ck = (1/(4*16))* msdc_src_ck 12'b111111111111: msdc_ck = (1/(4*4095)) * msdc_src_ck
7	**CCKSB**	CARD_CK_STABLE	**MS/SD Card clock stable or not** After programming the CARD_CK_MODE or CARD_CK_DIV, this bit will immediately go to "0" and return to "1" if stable.

Bit(s)	Mnemonic	Name	Description
			User should poll this register to make sure the safety control of MSDC. 1'b0: Clock output is not stable 1'b1: Clock output is stable
6	**BV18PSS**	BV_1P8_PASS	**MSDC Bus voltage 1.8V detection status** S/W should check this bit after BUS_VOL_18V_START_DET turns to 0 from 1. 1'b0: The voltage detection has error. 1'b1: The voltage detection has no error.
5	**BV18SDT**	BV_1P8_START_DET	**MSDC Bus voltage 1.8V detection sequence start event** S/W writes this bit to 1 to trigger H/W outputs 1.8V clock for 1 ms and automatically detect CMD/DAT line sequence for voltage change is passed or not. H/Q will clear this bit to 0 after the detection has finished. The pass or fail status is stored in bit[6] BUS_VOL_18V_PASS.
4	**CCKDRVE**	CARD_CK_DRV_EN	**SD/MS Card Bus Clock drive enable bit** Set this bit to 1 to enable MSDC bus clock driver. The default bus state depends on MSDC_CFG][1] CARD_CK_PWDN bit. If MSDC_CFG[1] CARD_CK_PWDN= 1, the default clock state is free running. If MSDC_CFG[1] CARD_CK_PWDN = 0, the default clock state is gated to 0. Set this bit to 0 will put the bus state into "tri-state". Default is 1. 1'b0: Put the clock pad into tri-state 1'b1: Enable MSDC to drive clock pad, the state of CLK depends on MSDC_CFG[1] CARD_CK_PWDN
3	**PIO**	PIO_MODE	**MS/SD PIO mode** PIO mode selection. Default is in PIO mode. 1'b0: DMA mode

Bit(s)	Mnemonic	Name	Description
			1'b1: PIO mode
2	**RST**	RST	**Software reset** Writing 1 to this register will cause internal synchronous reset of MS/SD controller, and it will not reset register settings and DMA controller. The reset sequence is done when this bit goes to 0. S/W should wait this bit back to 0 after writing 1. 1'b0: MS/SD controller is not in reset state 1'b1: MS/SD controller is in reset state
1	**CCKPD**	CARD_CK_PWDN	**MSDC bus clock power down mode** This bit controls the card clock power down mode. 1'b0: Clock is gated to 0 if no command or data is transmitted. 1'b1: Clock is free running even if no command or data is transmitted. (The clock may still be stopped when MSDC write data is not enough or no space for next read data)
0	**MSDC**	MSDC	**MS/SD mode selection** The register bit is used to configure the controller as the host of Memory Stick or as the host of SD/MMC Memory card. The default value is to configure the controller as the host of Memory Stick. 1'b0: Configure the controller as the host of Memory Stick 1'b1: Configure the controller as the host of SD/MMC Memory card

11230004 MSDC_IOCON MSDC IO Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									R_D7_SMPL	R_D6_SMPL	R_D5_SMPL	R_D4_SMPL	R_D3_SMPL	R_D2_SMPL	R_D1_SMPL	R_D0_SMPL
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			W_D3_SMPL	W_D2_SMPL	W_D1_SMPL	W_D0_SMPL	W_D_SMPL_SEL	W_D_SMPL			R_D_SMPL_SEL	DDR50_DLY_SEL	D_DLYLINE_SEL	R_D_SMPL	R_SMPL	SDR104_CLK_SEL

Type			RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**RD7SPL**	R_D7_SMPL	**Read data 7 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
22	**RD6SPL**	R_D6_SMPL	**Read data 6 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
21	**RD5SPL**	R_D5_SMPL	**Read data 5 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
20	**RD4SPL**	R_D4_SMPL	**Read data 4 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
19	**RD3SPL**	R_D3_SMPL	**Read data 3 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
18	**RD2SPL**	R_D2_SMPL	**Read data 2 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
17	**RD1SPL**	R_D1_SMPL	**Read data 1 sample selection**

Bit(s)	Mnemonic	Name	Description
			This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
16	**RD0SPL**	R_D0_SMPL	**Read data 0 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
13	**WD3SPL**	W_D3_SMPL	**SDIO interrupt sample selection** This bit is only valid when bit 9 is ON 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
12	**WD2SPL**	W_D2_SMPL	**SDIO interrupt sample selection** This bit is only valid when bit 9 is ON 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
11	**WD1SPL**	W_D1_SMPL	**SDIO interrupt sample selection** This bit is only valid when bit 9 is ON 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
10	**WD0SPL**	W_D0_SMPL	**CRC Status and SDIO interrupt sample selection** This bit is only valid when bit 9 is ON 1'b0: Sample CRC Status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC Status and SDIO interrupt by external bus clock falling edge
9	**WDSPLSEL**	W_D_SMPL_SEL	**Data line rising/falling latch fine tune selection in write transaction**

Bit(s)	Mnemonic	Name	Description
			1'b0: All data line share one value indicated by MSDC_IOCON.W_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.W_D0_SMPL Data line 1: MSDC_IOCON.W_D1_SMPL Data line 2: MSDC_IOCON.W_D2_SMPL Data line 3: MSDC_IOCON.W_D3_SMPL
8	**WDSPL**	W_D_SMPL	**CRC Status and SDIO interrupt sample selection** 1'b0: Sample CRC status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC status and SDIO interrupt by external bus clock falling edge
5	**RDSPLSEL**	R_D_SMPL_SEL	**Data line rising/falling latch fine tune selection in read transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.R_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.R_D0_SMPL Data line 1: MSDC_IOCON.R_D1_SMPL Data line 2: MSDC_IOCON.R_D2_SMPL Data line 3: MSDC_IOCON.R_D3_SMPL Data line 4: MSDC_IOCON.R_D4_SMPL Data line 5: MSDC_IOCON.R_D5_SMPL Data line 6: MSDC_IOCON.R_D6_SMPL Data line 7: MSDC_IOCON.R_D7_SMPL
4	**DDR50CKD**	DDR50_DLY_SEL	**DDR50 output clock delay selection** 1'b0: Use default clock output 1'b1: Delay 1T msdc_src_ck for clock output
3	**DDLSEL**	D_DLYLINE_SEL	**Data line delay line fine tune selection**

Bit(s)	Mnemonic	Name	Description
			1'b0: All data line share one delay selection value indicated by PAD_TUNE.PAD_DAT_RD_RXDLY 1'b1: Each data line has its own delay selection value indicated by Data line 0: DAT_RD_DLY0.DAT0_RD_DLY Data line 1: DAT_RD_DLY0.DAT1_RD_DLY Data line 2: DAT_RD_DLY0.DAT2_RD_DLY Data line 3: DAT_RD_DLY0.DAT3_RD_DLY Data line 4: DAT_RD_DLY1.DAT4_RD_DLY Data line 5: DAT_RD_DLY1.DAT5_RD_DLY Data line 6: DAT_RD_DLY1.DAT6_RD_DLY Data line 7: DAT_RD_DLY1.DAT7_RD_DLY
2	**RDSPL**	R_D_SMPL	**Read data sample selection** 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
1	**RSPL**	R_SMPL	**Command response sample selection** 1'b0: Sample response by external bus clock rising edge 1'b1: Sample response by external bus clock falling edge
0	**SDR104CKS**	SDR104_CLK_SEL	**SDR104 SCLK output clock control** This bit is only used when MSDC_CFG[17:16] CARD_CK_MODE is 2'b01. 1'b0: Bus clock output equals inverted msdc_src_ck 1'b1: Bus clock output equals msdc_src_ck

11230008 MSDC_PS MSDC Pin Status Register 81FF0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SD_WP							CMD	DAT							
Type	RU							RU	RU							
Reset	1							1	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDDEBOUNCE														CDSTS	CDEN
Type	RW														RU	RW
Reset	0	0	0	0											1	0

Bit(s)	Mnemonic	Name	Description
31	**SDWP**	SD_WP	**Write Protection Switch status on SD Memory Card** The register bit shows the status of Write Protection Switch on SD Memory Card. There is no default reset value. The pin WP (Write Protection) is only useful while the controller is configured for SD Memory Card 1'b0: Write Protection Switch ON. It means that memory card is desired to be write-protected 1'b1: Write Protection Switch OFF. It means that memory card is writable
24	**CMD**	CMD	**Command line status** This bit reflects the command line value of MSDC bus.
23:16	**DAT**	DAT	**Data line status** This bit reflects the data line value of MSDC bus. (8-bits)
15:12	**CDDBCE**	CDDEBOUNCE	**Card detection de-bounce timer** The register field specifies the time interval for card detection de-bounce. Its default value is 0. It means that de-bounce interval is one 32KHz cycle. The interval will extend one cycle time of 32KHz by increasing the counter by 1
1	**CDSTS**	CDSTS	**Card detection status** 1'b0: Card detection pin status is logic low 1'b1: Card detection pin status is logic high
0	**CDEN**	CDEN	**Card detect enable** The register bit is used to control the card detection circuit 1'b0: Card detection is disable 1'b1: Card detection is enable

1123000C MSDC_INT MSDC Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name									AXI_RESP_ERR				DMA_PROTECT	GPD_CS_ERR	BD_CS_ERR	AUTOCMD19_DONE
Type									W1C				W1C	W1C	W1C	W1C
Reset									0				0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SD_DATA_CRCERR	SD_DATTO	DMA_XFER_DONE	SD_XFER_COMPLETE	SD_CSTS	SD_RESP_CRCERR	SD_CMDTO	SD_CMDRDY		DMA_Q_EMPTY	SD_AUTOCMD_RESP_CRCERR	SD_AUTOCMD_CMDTO	SD_AUTOCMD_CMDRDY		MSDC_CDSC	MMC_IRQ
Type	W1C	W1C	W1C	W1C	RU	W1C	W1C	W1C		W1C	W1C	W1C	W1C		W1C	W1C
Reset	0	0	0	0	0	0	0	0		0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
23	**AXIRSPERR**	AXI_RESP_ERR	**AXI BUS response error status**
19	**DMAPROTECT**	DMA_PROTECT	**there is write operation to DMA start address, length, start bit or last buf bit**
18	**GPDCSERR**	GPD_CS_ERR	**GPD checksum error detected**
17	**BDCSERR**	BD_CS_ERR	**BD checksum error detected**
16	**AC19DONE**	AUTOCMD19_DONE	**SD Auto command 19 status register** When auto-command 19 is enabled, H/W will clear this register to 0. As the tuning sequence is finished (32 times), this register will be set to 1 by H/W. S/W should check the AUTOCMD_STS0 and SUTOCMD_STS1 only when this bit is ON.
15	**SDDCRCERR**	SD_DATA_CRCERR	**SD Data CRC error interrupt** Indicates that MS/SD controller detects a CRC error after reading a block of data from the DAT line or SD/MMC signals a CRC error after writing a block of data to the DAT line. 1'b0: Otherwise 1'b1: MS/SD controller detected a CRC error after reading a block of data from the DAT line or SD/MMC signaled a CRC error after writing a block of data to the DAT line
14	**SDDTO**	SD_DATTO	**SD Data timeout interrupt** Indicates that SD/MMC controller detects a timeout condition while waiting for data token on the DAT line.

Bit(s)	Mnemonic	Name	Description
			This bit is for both data read and data write. For SD data read, timeout will occur when the read data is not presented. For SD data write, timeout will occur when the write data CRC status is not presented if PATCH_BIT[30] DETECT_WR_CRC_TIMEOUT = 1 1'b0: Otherwise 1'b1: SD/MMC controller detects a timeout condition while waiting for data token on the DAT line
13	**DMAXFDNE**	DMA_XFER_DONE	**DMA transfer done interrupt** The register bit indicates the status of data block transfer. 1'b0: Otherwise 1'b1: A data block was successfully transferred
12	**SDXFCPL**	SD_XFER_COMPLETE	**SD Data transfer complete interrupt** This bit indicates the transaction which contains data has completed. While performing tuning procedure (Execute Tuning is set to 1), SD_XFER_COMPLETE is not set to 1.
11	**SDCSTS**	SD_CSTS	**SD CSTA update interrupt** The register bit indicates any bit in the register SDC_CSTA is active, the register bit will be set to 1. S/W should clear the SDC_CSTA and this bit will be de-asserted automatically. 1'b0: No SD Memory Card interrupt 1'b1: SD Memory Card interrupt exists
10	**SDRCRCER**	SD_RESP_CRCERR	**SD Command CRC error interrupt** Indicates that SD/MMC controller detected a CRC error after reading a response from the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detected a CRC error after reading a response from the CMD line
9	**SDCTO**	SD_CMDTO	**SD Command timeout interrupt** Indicates that SD/MMC controller detected a timeout condition while waiting for a response on the CMD line.

Bit(s)	Mnemonic	Name	Description
			1'b0: Otherwise 1'b1: SD/MMC controller detected a timeout condition while waiting for a response on the CMD line
8	**SDCRDY**	SD_CMDRDY	**SD Command ready interrupt** For the command without response, the register bit will be 1 once the command completes on SD/MMC bus. For command with response without busy, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error. For command with response with busy in DAT0, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error and the DAT0 transited from busy to idle. 1'b0: Otherwise 1'b1: Command finish successfully without a CRC error
6	**DMAQEPTY**	DMA_Q_EMPTY	**DMA queue empty interrupt** This bit is used to indicate the current DMA queue is empty. Only for Descriptor mode and Enhance mode.
5	**SDACDRCRCER**	SD_AUTOCMD_RESP_CRCERR	**SD auto command CRC error interrupt** This bit is set when detecting a CRC error in the Auto command response.
4	**SDACDCTO**	SD_AUTOCMD_CMDTO	**SD auto command timeout interrupt** This bit is set if no response is returned within a specified cycles(64T in spec) from the end bit of Auto command.
3	**SDACDCRDY**	SD_AUTOCMD_CMDRDY	**SD auto command ready interrupt** This bit is set if auto command is executed without CRC error or time out.
1	**MSDCCDSC**	MSDC_CDSC	**MSDC Card detection status change interrupt** The register bit indicates if any interrupt for memory card insertion/removal exists. Whenever memory card is inserted or removed and card detection circuit is enabled, i.e., the register bit CDEN in the register MSDC_PS is set to 1, the register bit will be set to 1. It will be reset when the register is read. 1'b0: Otherwise

Bit(s)	Mnemonic	Name	Description
			1'b1: Card is inserted or removed
0	**MMCIRQ**	MMC_IRQ	**MMC card interrupt** 1'b0: Otherwise 1'b1: indicates that MMC card interrupt event occurs

11230010 MSDC_INTEN MSDC Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									EN_AXI_RESP_ERR				EN_DMA_PROTECT	EN_GPD_CS_ERR	EN_BDCS_ERR	EN_AUTOCMD19_DONE
Type									RW				RW	RW	RW	RW
Reset									0				0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SD_DATA_CRCERR	EN_SD_DATTO	EN_SD_DMA_XFER_DONE	EN_SD_XFER_COMPLETE	EN_SD_CSTA	EN_SD_RESP_CRCERR	EN_SD_CMDTO	EN_SD_CMDRDY	EN_SD_SDIOIRQ	EN_DMA_Q_EMPTY	EN_SD_AUTOCMD_RESP_CRCERR	EN_SD_AUTOCMD_CMDTO	EN_AUTOCMD_CMDRDY		EN_MSDC_CDSC	EN_MMC_IRQ
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
23	**ENAXIRSPERR**	EN_AXI_RESP_ERR	**AXI BUS response error status interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
19	**ENDMAPROTECT**	EN_DMA_PROTECT	**DMA protection interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
18	**ENGPDCSERR**	EN_GPD_CS_ERR	**GPD checksum error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt

Bit(s)	Mnemonic	Name	Description
17	**ENBDCSERR**	EN_BD_CS_ERR	**BD checksum error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
16	**ENAC19DONE**	EN_AUTOCMD19_DONE	**Auto-command 19 complete interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
15	**ENSDDCRCERR**	EN_SD_DATA_CRCERR	**SD Data CRC error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
14	**ENSDDTO**	EN_SD_DATTO	**SD Data timeout interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
13	**ENDMAXFDNE**	EN_SD_DMA_XFER_DONE	**DMA transfer done interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
12	**ENSDXFCPL**	EN_SD_XFER_COMPLETE	**SD Data transfer complete interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
11	**ENSDCSTA**	EN_SD_CSTA	**SD CSTA update interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
10	**ENSDRCRCER**	EN_SD_RESP_CRCERR	**SD Command CRC error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
9	**ENSDCTO**	EN_SD_CMDTO	**SD Command timeout interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt

Bit(s)	Mnemonic	Name	Description
8	**ENSDCRDY**	EN_SD_CMDRDY	**SD Command ready interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
7	**ENSDIOIRQ**	EN_SD_SDIOIRQ	**SD SDIO interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
6	**ENDMAQEPTY**	EN_DMA_Q_EMPTY	**DMA queue empty interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
5	**ENSDACDRCRCER**	EN_SD_AUTOCMD_RESP_CRCERR	**SD auto command CRC error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
4	**ENSDACDCTO**	EN_SD_AUTOCMD_CMDTO	**SD auto command timeout interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
3	**ENSDACDCRDY**	EN_AUTOCMD_CMDRDY	**SD auto command ready interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
1	**ENMSDCCDSC**	EN_MSDC_CDSC	**MSDC Card detection status change interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
0	**ENMMCIRQ**	EN_MMC_IRQ	**MMC card interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt

11230014 MSDC_FIFOCS MSDC FIFO Control and Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFOCLR								TXFIFOCNT							
Type	A0								RU							
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXFIFOCNT							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**FIFOCLR**	FIFOCLR	**Embedded FIFO clear** Write this bit to 1 makes FIFO cleared. It will goes to 0 when FIFO is cleared. S/W needs to check this bit to make sure clearing FIFO sequence is done. This bit can be used when the data read/write sequence has error and need to clean the H/W FIFO.
23:16	**TXFIFOCNT**	TXFIFOCNT	**TX FIFO count for MSDC write** 8'd0: No data in FIFO 8'd1: 1bytes data in FIFO 8'd2: 2 bytes data in FIFO 8'd131: Maximum 131 bytes data in FIFO Others: reserved
7:0	**RXFIFOCNT**	RXFIFOCNT	**RX FIFO count for MSDC read** 8'd0: No data in FIFO 8'd1: 1bytes data in FIFO 8'd2: 2 bytes data in FIFO 8'd131: Maximum 131 bytes data in FIFO Others: reserved

11230018 MSDC_TXDATA MSDC TX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_TXDATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_TXDATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIOTXDATA**	PIO_TXDATA	**PIO mode TXDATA port** This register can be accessed by Byte or Half-word or Word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

1123001C MSDC_RXDATA MSDC RX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_RXDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_RXDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIORXDATA**	PIO_RXDATA	**PIO mode RXDATA port** This register can be accessed by Byte or Half-word or Word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

11230030 SDC_CFG SD Configuration Register 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DTOC										INT_AT_BLOCK_GAP	SDIO_INT_DET_EN	SDIO		BUSWIDTH	

Type	RW										RW	RW	RW		RW	
Reset	0	0	0	0	0	0	0	0			0	1	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		WRDTOC													WAKEUP_INS_EN	WAKEUP_SDIOINT_EN
Type		RW													RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DTOC**	DTOC	**Data Timeout Counter** The period from the end of the initial host read command or the last read data block in a multiple block read operation to the start bit of the next read data block requires at least two serial clock cycles. The counter is used to extend the period (Read Data Access Time) in unit of 1048576 serial clocks. 8'b00000000: Extend 1048576 more serial clock cycle 8'b00000001: Extend 1048576x2 more serial clock cycle 8'b00000010: Extend 1048576x3 more serial clock cycle 8'b11111111: Extend 1048576x 256 more serial clock cycle
21	**INTBGP**	INT_AT_BLOCK_GAP	**Interrupt at block Gap** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. Setting to 0 disables interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the Host Driver detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. 1'b0: Disables interrupt detection at the block gap 1'b1: Enables interrupt detection at the block gap
20	**SDIOIDE**	SDIO_INT_DET_EN	**SDIO interrupt detection enable** This bit is to inform the SD controller to sense the SDIO interrupt 1'b0: SDIO interrupt detection is disabled

Bit(s)	Mnemonic	Name	Description
			1'b1: SDIO interrupt detection is enabled if the SDIO bit is also on
19	**SDIO**	SDIO	**SDIO mode enable bit** This bit is to enable the support to sense the SDIO interrupt and disable the R4 response CRC check for SDIO card 1'b0: SDIO mode is disabled 1'b1: SDIO mode is enabled
17:16	**BUSWD**	BUSWIDTH	**Bus width configuration** This field is used to define the SD/MMC bus width 2'b00: 1 bit mode 2'b01: 4 bit mode 2'b10: 8 bit mode 2'b11: reserved
14:2	**WRDTOC**	WRDTOC	**Data Timeout Counter** Timeout counter for programming.The counter is used to extend the period (Write Data Access Time) in unit of 1048576 serial clocks. 13'b0000000000000: Extend 1048576 more serial clock cycle 13'b0000000000001: Extend 1048576x2 more serial clock cycle 13'b0000000000010: Extend 1048576x3 more serial clock cycle 13'b1111111111111: Extend 1048576x 8192 more serial clock cycle
1	**ENWKUPINS**	WAKEUP_INS_EN	**Card status change wakeup event enable bit** 1'b0: Disable wakeup event for card status change 1'b1: Enable wakeup event for card status change
0	**ENWKUPSDIOINT**	WAKEUP_SDIOINT_EN	**SDIO card interrupt wakeup event enable bit** 1'b0: Disable wakeup event for SDIO card interrupt 1'b1: Enable wakeup event for SDIO card interrupt

11230034 SDC_CMD SD Command Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		VOL_SWTH	AUTO_CMD		LEN											
Type		RW	RW		RW											
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GO_IRQ	STOP	RW	DTYPE			RSPTYP			BREAK	CMD					
Type	RW	RW	RW	RW			RW			RW	RW					
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30	**VOLSWTH**	VOL_SWTH	**Voltage switch command** 1'b0: Disable voltage switch detection 1'b1: Enable voltage switch detection
29:28	**ACMD**	AUTO_CMD	**Auto command enable** This field determines use of auto command functions. This function can be used in all modes including PIO/Basic DMA/Descriptor DMA/Enhanced Mode. There are two methods to stop Multiple-block read and write operation. (1) Auto CMD12 Enable Multiple-block read and write commands for memory require CMD12 to stop the operation. When ACMD-12 is used, MSDC issues CMD12 automatically when last block transfer is completed. Auto CMD12 error is indicated to the MSDC_INT register. The Host Driver shall not set this bit if the command does not require CMD12. In particular, secure commands defined in the Part 3 File Security specification do not require CMD12. (2) Auto CMD23 Enable When ACMD-23 is used, MSDC issues a CMD23 automatically before issuing a command specified in the CMD field. The Host Controller Version 3.00 and later shall support this function. By writing the Command register, MSDC issues a CMD23 first and then issues a command specified by the CMD field in SDC_CMD register. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in the MSDC_INT

Bit(s)	Mnemonic	Name	Description
			register. 32-bit block count value for CMD23 is set to SDC_BLOCK_NUM register. 2'b00: Disable Auto Command 2'b01: Enable Auto CMD12 2'b10: Enable Auto CMD23 2'b11: Enable Re-tuning CMD19
27:16	**LEN**	LEN	**Length** The register field is used to define the length of one block in unit of byte in a data transaction of block mode or the data length in unit of byte in data transaction of byte mode. The maximal value of block length is 2048 bytes. 12'b000000000000: Reserved 12'b000000000001: Block length is 1 byte 12'b000000000010: Block length is 2 byte 12'b011111111111: Block length is 2047 byte 12'b100000000000: Block length is 2048 byte
15	**GOIRQ**	GO_IRQ	**GO_IRQ command** The register bit indicates if the command is GO_IRQ_STATE (CMD40) and used only for MMC protocol. If the command is GO_IRQ_STATE, the period between command token and response token will not be limited. 1'b0: The command is not GO_IRQ_STATE 1'b1: The command is GO_IRQ_STATE
14	**STOP**	STOP	**Stop command** The register bit indicates if the command is a stop transmission command. It should be set to 1 when CMD12 (SD/MMC) or CMD52 with I/O abort (SDIO) is to be issued. 1'b0: The command is not a stop transmission command 1'b1: The command is a stop transmission command
13	**RW**	RW	**Command read write selection** The register bit defines the command is a read command or write command. The register bit is valid only when the command will cause a transaction with data token.

Bit(s)	Mnemonic	Name	Description
			1'b0: The command is a read command 1'b1: The command is a write command
12:11	**DTYPE**	DTYPE	**Data block selection** The register field defines data token type for the command. 2'b00: No data token for the command 2'b01: Single block transaction (only available in block mode) 2'b10: Multiple block transaction. (only available in block mode) 2'b11: Stream operation. It only shall be used in MMC protocol. (only available in block mode)
9:7	**RSPTYP**	RSPTYP	**Command response type** 3'b000: This command has no response. 3'b001: The command has R1/R5/R6/R7 response. The response token is 48-bit with CRC check (For SD/MMC/SDIO) (Not include the SDIO abort command) 3'b010: The command has R2 response. The response token is 136-bit (For SD/MMC) 3'b011: The command has R3 response. The response token is 48-bit response, no CRC check (For SD/MMC) 3'b100: The command has R4 response. The response token is 48-bit without CRC check (For SDIO) The response token is 48-bit with CRC check (For MMC) 3'b111: The command has R1b response. The response token is 48-bit (For SD/MMC/SDIO)
6	**BREAK**	BREAK	**Abort a pending MMC GO_IRQ command** It is only valid for a pending GO_IRQ_MODE command waiting for MMC interrupt response. 1'b0: Not a beak command 1'b1: Break a pending MMC GO_IRQ_MODE command in the controller.
5:0	**CMD**	CMD	**SD Memory Card command**

11230038 SDC_ARG SD Argument Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ARG**	ARG	**Memory card controller argument register**

1123003C SDC_STS SD Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMC_STREAM_WR_COMPL											CMD_TIMEOUT_TYPE		DATA_TIMEOUT_TYPE		CMD_WR_BUSY
Type	RU											RU		RU		W1C
Reset	0											0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														START_BIT_CRCERR	CMDBUSY	SDCBUSY
Type														RU	RU	RU
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
31	**MMCSWRCPL**	MMC_STREAM_WR_COMPL	**MMC Stream mode write data is all flushed to MMC card** S/W can use this bit to confirm last write data are flushed to MMC then issue STOP command. This bit is only valid when the command SDC_CMD.DTYPE=2'b11. 1'b0: Last Data are partially inside MSDC 1'b1: Last data are flushed to MMC card

Bit(s)	Mnemonic	Name	Description
20:19	**CTTYPE**	CMD_TIMEOUT_TYPE	**MSDC cmd timeout type,For debug host misses r1b cmd response start bit or data0 busy too long** 2'b01:data0 busy timeout 2'b10:response start bit timeout
18:17		DATA_TIMEOUT_TYPE	**Data Timeout Error Type,For Debug and Err Handle** 2'b00: Read Data Timeout 2'b01: Write CRC Stauts Timeout 2'b10: Write Programming Timeout
16		CMD_WR_BUSY	
2	**STBCRCERR**	START_BIT_CRCERR	**Status to reflect whether host misses start bit or not** 1'b0: start bit check pass 1'b1: start bit missing error
1	**CMDBSY**	CMDBUSY	**SD Command line busy status** S/W should always read this bit to make sure the command line is not busy before sending the next command. If the command is R1B or data read/write command, S/W should check SDCBUSY bit too. Note: When Auto command 12 is enabled, this bit will be asserted immediately after SDC_CMD is written and de-asserted after auto-command 12 finishes. 1'b0: No transmission is going on CMD line on SD bus 1'b1: There exists transmission going on CMD line on SD bus
0	**SDCBSY**	SDCBUSY	**SD controller busy status** 1'b0: SD controller is idle 1'b1: SD controller is busy

11230040 SDC_RESP0 SD Response Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP0															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP0**	RESP0	**Memory card controller response register 0**

11230044 SDC_RESP1 SD Response Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP1**	RESP1	**Memory card controller response register 1**

11230048 SDC_RESP2 SD Response Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP2**	RESP2	**Memory card controller response register 2**

Bit(s)	Mnemonic	Name	Description

1123004C SDC_RESP3 SD Response Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP3**	RESP3	**Memory card controller response register 3**

11230050 SDC_BLK_NUM SD Block Number Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BLOCK_NUMBER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLOCK_NUMBER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0	**BLKNUM**	BLOCK_NUMBER	**Memory card controller Block number** This field indicates the block number of data transaction. 32'd0: Reserved 32'd1: 1 data block 32'd2: 2 data block 32'd3: 3 data block

Bit(s)	Mnemonic	Name	Description
			32'hffffffff: 4GB-1 data block

11230054 SDC_VOL_CHG SD Voltage Change Wait Time Register 00000145

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VOL_CHG_WAIT_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
15:0	**VCHGCNT**	VOL_CHG_WAIT_CNT	**This register define SD voltage change check wait time,wait time is clock frequency multiply VOL_WAIT_TIME**

11230058 SDC_CSTS SD Card Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS**	CSTS	**CSTS** The card status field in the response R1 or R1b field. Each bit can be write 1 clear individually.

1123005C SDC_CSTS_EN SD Card Status Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS_EN**	CSTS_EN	**CSTS_EN** This register is used to control which bit of the CSTA will generate the MSDC_INT.SDCSTA

11230060 SDC_DATCRC_STS SD Card Data CRC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT_CRCSTS_NEG								DAT_CRCSTS_POS							
Type	RU								RU							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**DCSSN**	DAT_CRCSTS_NEG	**MSDC DDR mode negative edge Read DATA CRC status** This register reflects the CRC status of data line[7:0] in DDR mode. The positive edge CRC status is shown in DAT_CRC_STS[7:0]. This register is only for MSDC Read. 1'b0: No CRC error 1'b1: CRC error
7:0	**DCSSP**	DAT_CRCSTS_POS	**MSDC read DATA CRC status**

Bit(s)	Mnemonic	Name	Description
			This register reflects the CRC status of data line[7:0]. This register is only for MSDC Read. 1'b0: No CRC error 1'b1: CRC error

11230064 SDC_ADV_CFG0 SDC Advance Configuration 0 0000E000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												SDC_RX_ENHANCE_EN				
Type												RW				
Reset												0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMD_INDEX_CHECK	CMD_ENDBIT_CHECK	CMD_RESP_ENDBIT	CMD_RESP_INDEX						CMD_RESP_CRC						
Type	RW	RW	RU	RU						RU						
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20		SDC_RX_ENHANCE_EN	**enhance rx ehance check en for TA remove and gap IRQ check** 1'b0: normal rx path 1'b1: enhance rx path
15		CMD_INDEX_CHECK	**Decide hardware check cmd_index in response or not** 1'b0: Software check index 1'b1: Hardware check index
14		CMD_ENDBIT_CHECK	**Decide hardware check end_bit in response or not** 1'b0: Software check endbit 1'b1: Hardware check endbit
13		CMD_RESP_ENDBIT	**CMD endbit in the cmd response**

Bit(s)	Mnemonic	Name	Description
12:7		CMD_RESP_INDEX	**CMD index in the cmd response**
6:0		CMD_RESP_CRC	**CMD crc in the cmd response**

11230070 EMMC_CFG0 EMMC Configuration Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BOOT_SUPPORT	BOOT_WAIT_DELAY											BOOT_ACK_CHK_DIS	BOOT_MODE	BOOT_STOP	BOOT_START
Type	RW	RW											RW	RW	WO	WO
Reset	0	0	0	0									0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**BTSUP**	BOOT_SUPPORT	**eMMC boot up support** The register bit indicates that boot mode is supported or not 1'b0: Not Support 1'b1: Support
14:12	**BTWDLY**	BOOT_WAIT_DELAY	**eMMC wait delay time** The register bit set the delay time to wait MMC device to exit boot up mode after boot stop bit is set. 3'b000: 0x1024 clock cycles 3'b001: 1x1024 clock cycles 3'b010: 2x1024 clock cycles 3'b111: 7x1024 clock cycles
3	**BTACHKDIS**	BOOT_ACK_CHK_DIS	**eMMC boot up mode ACK check Disable** 1'b0: Do ACK pattern check 1'b1: Bypass ACK pattern check

Bit(s)	Mnemonic	Name	Description
2	**BTMOD**	BOOT_MODE	**eMMC boot up mode** There are two kinds of boot up mode supported by eMMC 4.4. Reset CMD mode is option for eMMC 4.3. 1'b0: Pull low CMD mode 1'b1: Reset CMD mode
1	**BTSTOP**	BOOT_STOP	**eMMC boot up mode stop** The register bit is indicated that boot stop signal, read always return 0.
0	**BTSTART**	BOOT_START	**eMMC boot up start signal trigger** The register bit is boot up start signal trigger. read always return 0.

11230074 EMMC_CFG1 EMMC Configuration Register 1 00200003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BOOT_ACK_TOC												BOOT_DAT_TOC			
Type	RW												RW			
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BOOT_DAT_TOC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:20	**BTATOC**	BOOT_ACK_TOC	**eMMC ack pattern time out counter** in unit of 2^16 serial clock. SW could not set it to 12'hFFF.
19:0	**BTDTOC**	BOOT_DAT_TOC	**eMMC read boot data time out counter** in unit of 2^16 serial clock. SW could not set it to 20'hFFFFF.

11230078 EMMC_STS EMMC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BOOT_DAT_RECV	BOOT_ACK_RECV	BOOT_UP_STATE	BOOT_ACK_TO	BOOT_DAT_TO	BOOT_ACK_ERR	BOOT_CRC_ERR
Type										RU	W1C	RU	W1C	W1C	W1C	W1C
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6	**BTDRCV**	BOOT_DAT_RECV	**eMMC boot data is received** This register is for S/W to check 1st 4-byte boot data is received or not. For other data after 1st 4B data, this bit should not be referenced. S/W should check RXFIFOCNT instead. 1'b0: There's no data in RXFIFO 1'b1: 1st 4B data is in RXFIFO
5	**BTARCV**	BOOT_ACK_RECV	**eMMC ack is received** Also need to check BOOT_ACK_ERR to determine pass or fail 1'b0: No ACK pattern is received 1'b1: ACK pattern has been received
4	**BTSTS**	BOOT_UP_STATE	**eMMC boot up mode status** The register bit indicates if MMC device operating in boot up mode state. 1'b0: Not in Boot up state 1'b1: Boot up state is on-going
3	**BTATO**	BOOT_ACK_TO	**eMMC ack timeout** The register bit indicates the controller detect a time out condition while waiting for an ack pattern on DAT0. 1'b0: No ACK pattern timeout error 1'b1: ACK pattern timeout error
2	**BTDTO**	BOOT_DAT_TO	**eMMC data timeout** The register bit indicates the controller detect a time out condition while waiting for boot data.

Bit(s)	Mnemonic	Name	Description
			1'b0: No Data timeout error 1'b1: Data timeout error
1	**BTAERR**	BOOT_ACK_ERR	**eMMC ack error** The register bit indicates the status of ack pattern checking result. The bit is setting to 1 when ack pattern error. 1'b0: No ACK pattern check error 1'b1: ACK pattern check error
0	**BTDERR**	BOOT_CRC_ERR	**eMMC CRC error** The register bit indicates the CRC status of boot data. The bit is setting to 1 when data CRC error. 1'b0: No Data CRC error 1'b1: Data CRC error

1123007C EMMC_IOCON EMMC IO Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**BOOT_RST**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**BTRST**	BOOT_RST	**eMMC device boot up mode reset** The register bit is to trigger HW reset to set eMMC device entering into pre-idle state. 1'b0: de-assert RST_n to eMMC card 1'b1: Assert RST_n to eMMC card

11230080 SD_ACMD_RESP SD ACMD Response Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUTOCMD_RESP															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCMD_RESP															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ACMDRESP**	AUTOCMD_RESP	**SD Auto command response register** This register stores the response[39:8] of ACMD12/ACMD23/ACMD19.

11230084 SD_ACMD19_TRG SD ACMD19 Target Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FINE_TUNE_SEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**ACMDFTSEL**	FINE_TUNE_SEL	**SD Auto command 19 test target selection** After auto-command 19 is triggered, MSDC will only change the phase of the selected one and keep the value of other tuning registers. S/W can get the result from AUTOCMD_STS. There are total 32 phases for each delay line. 4'd0: Select PAD_CLK_TXDLY[5:0] as the target to run auto-command19.

Bit(s)	Mnemonic	Name	Description
			4'd1: Select PAD_CMD_RXDLY[5:0] as the target to run auto-command19. 4'd2: Select PAD_DAT_RD_RXDLY[5:0] as the target to run auto-command19. 4'd3: Select PAD_DAT_WR_RXDLY[5:0] as the target to run auto-command19. 4'd4: Select DAT0_RD_DLY[5:0] as the target to run auto-command19. 4'd5: Select DAT1_RD_DLY[5:0] as the target to run auto-command19. 4'd6: Select DAT2_RD_DLY[5:0] as the target to run auto-command19. 4'd7: Select DAT3_RD_DLY[5:0] as the target to run auto-command19. 4'd8: Select DAT4_RD_DLY[5:0] as the target to run auto-command19. 4'd9: Select DAT5_RD_DLY[5:0] as the target to run auto-command19. 4'd10: Select DAT6_RD_DLY[5:0] as the target to run auto-command19. 4'd11: Select DAT7_RD_DLY[5:0] as the target to run auto-command19. 4'd12: Select CMD_RESP_RXDLY[5:0] as the target to run auto-command19. Others: Reserved

11230088 SD_ACMD19_STS SD ACMD19 Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUTOCMD19_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCMD19_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ACMD19STS**	AUTOCMD19_STS	**SD Auto command 19 test result register** When auto-command 19 is enabled, H/W will automatically try 32 times of command-19 and store the result into this register. This register contains 1st to 32th results in bit[0:31]

1123008C DMA_SA_HIGH4BIT DMA Current Address Resgiter of high 4bit 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**DMA_SURR_ADDR_HIGH4BIT**			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DMASAHIGH4BIT**	DMA_SURR_ADDR_HIGH4BIT	**it is usend to set high 4bit address of start address because 64G dram need 36bit address**

11230090 DMA_SA DMA Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DMA_STR_ADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DMA_STR_ADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMASA**	DMA_STR_ADDR	**The start address of the DMA address** This register is used to set the start address of the DMA. In DMA basic mode, this field indicates the source or

Bit(s)	Mnemonic	Name	Description
			destination address of the data transfer which depends on the command. In descriptor base DMA, this is the descriptor chain start address.

11230094 DMA_CA DMA Current Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_CURR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_CURR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMACA**	DMA_CURR_ADDR	**The current address of the DMA address** This register is used to read the current address of the DMA descriptor chain.

11230098 DMA_CTRL DMA Control Register 00006008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BURST_SIZE			DMA_SPLIT_1K	LAST_BUF	DMA_ALIGN	DMA_MODE					AHB_READYM	DMA_RESUME	DMA_STOP	DMA_START
Type		RW			RW	RW	RW	RW					RO	WO	A0	WO
Reset		1	1	0	0	0	0	0					1	0	0	0

Bit(s)	Mnemonic	Name	Description
14:12	**BSTSZ**	BURST_SIZE	**DMA burst size**

Bit(s)	Mnemonic	Name	Description
			This field is used to specify the maximum transfer bytes allowed at the device per DMA burst. This field can not be modified when the DMA status is 1. 3'd3: 8 Bytes 3'd4: 16 Bytes 3'd5: 32 Bytes 3'd6: 64 Bytes Other: Reserved
11	**SPLIT1K**	DMA_SPLIT_1K	**This field is used to specify whether split burst when corss 1K boundry address** 1'b0:1K boundary not split 1'b1:1K boundary split
10	**LASTBF**	LAST_BUF	**Last buffer of the basic DMA mode** This field indicates the last buffer in the basic DMA mode
9	**DMAALIGN**	DMA_ALIGN	**This field is used to specify whether address aligment burst size** 1'b0:do not DAM burst size alignment 1'b1:DAM burst size alignment
8	**DMAMOD**	DMA_MODE	**DMA operation mode** This field indicates operation mode of DMA 1'b0: Basic DMA mode 1'b1: Descriptor base DMA mode
3	**READYM**	AHB_READYM	**only for debug when dma hang,sw can check if ahb bus is ok when gdma is hang** 1:bus is normal 0:bus not normal
2	**DMARSM**	DMA_RESUME	**DMA resume control register** This bit is used to resume the DMA transaction. Read always return 0
1	**DMASTOP**	DMA_STOP	**DMA Stop control register**

Bit(s)	Mnemonic	Name	Description
0	**DMASTART**	DMA_START	This bit is used to stop the DMA transaction. When SW issue STOP command, SW must wait this bit de-assert or DMA inactive to guarantee stop done. **DMA start control register** This bit is used to start the DMA transaction. Read always return 0

1123009C DMA_CFG DMA Configuration Register 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																DMA_CHK_SUM_12B
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MSDC_ACTIVE_EN				AHB_HPROT_2_EN							LOCK_DISABLE	DMA_DSCP_CS_EN	DMA_STATUS
Type			RW				RW							RW	RW	RU
Reset			0	0			0	0						1	0	0

Bit(s)	Mnemonic	Name	Description
16	**DMACHKSUM12B**	DMA_CHK_SUM_12B	**This register indicates GPD/BD checksum cover 16byte or 12byte** 1'b0: GPD/BD checksum cover 16byte 1'b1: GPD/BD checksum only cover 12byte
13:12	**MSDCACTIVEEN**	MSDC_ACTIVE_EN	**This register will indicate how to control msdc_active** 2'b00: dynamic control msdc_active 2'b01: msdc_active = 0 2'b10: msdc_active = 1 2'b11: Reserved
9:8	**AHBHPROT2EN**	AHB_HPROT_2_EN	**This register will determine how to control hprot_2 pin of AHB bus**

Bit(s)	Mnemonic	Name	Description
			AHB_HPROT_2_EN = 2'b00, and Basic DMA Mode All the write transfers of a burst will access by bufferable mode except the last burst of DMA AHB_HPROT2_2_EN=2'b00, and Descriptor DMA Mode all the write transfers of a burst will access by bufferable mode except HW own update transfer 2'b00: dynamic control hprot_2 2'b01: hprot_2 = 0 2'b10: hprot_2 = 1
2	**LOCKDISABLE**	LOCK_DISABLE	**should disable lock in order to improve emi efficient** 1'b0:enable ahb lock 1'b1:disable ahb lock
1	**DSCPCSEN**	DMA_DSCP_CS_EN	**DMA descriptor checksum enable** This bit is used to enable or disable the descriptor checksum validation function for the descriptor. This field can not be modified when the DMA status is 1.
0	**DMASTS**	DMA_STATUS	**DMA status** This bit is used to indicate the status of the DMA. 1'b0: DMA engine is inactive 1'b1: DMA engine is active

112300A0 SW_DBG_SEL MSDC S/W Debug Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DBG_SEL**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**SWDBGSEL**	DBG_SEL	**MSDC debug selection** This contain is reserved!

112300A4 SW_DBG_OUT MSDC S/W Debug Output Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SWDBGO**	DBG_OUT	**MSDC debug output** 32 bit output selected by SW_DBG_SEL register

112300A8 DMA_LENGTH DMA Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**XFSZ**	XFER_SIZE	**DMA total transfer size** This field is used to specify the number of DMA transfer byte required for the movement of source data through DMA. This field is only valid in basic DMA mode.

Bit(s)	Mnemonic	Name	Description

112300B0 PATCH_BIT0 MSDC Patch Bit Register 0 403C0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_MMC_DRV_RESP	DETECT_WR_CRC_TIMEOUT	SPC_ALWAYS_PUSH	SDIO_INT_DLY_SEL	SDC_CMD_CMDFAIL_SEL	SDC_CMD_IDRT_SEL	SDC_CFG_WDOD				SDC_CFG_BSYDLY				SDIO_CFG_INTC_SEL	MSDC_BLKNUM_SEL
Type	RW	RW	RW	RW	RW	RW	RW				RW				RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC_FIFO_RD_DIS	CKGEN_MSDC_DLY_SEL					INT_DAT_LATCH_CK_SEL			DESC_UP_SEL			RD_DAT_SEL	DIS_REFLECT_CMDWR_WHEN_BSY	EN_SDC_ODD_8BIT_SUP	EN_START_BIT_CHK_SUP
Type	RW	RW					RW			RW			RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0			0	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**PTCH31**	EN_MMC_DRV_RESP	**Enable MSDC always drives bus when output wakeup response (BREAK)** 1'b0: Disable 1'b1: Enable
30	**PTCH30**	DETECT_WR_CRC_TIMEOUT	**MSDC write data CRC phase timeout detection** 1'b0: Not detect CRC phase timeout 1'b1: detect CRC phase timeout
29	**PTCH29**	SPC_ALWAYS_PUSH	**SPC Buffer push mechanism** 1'b0: Push the buffer only when read transfer is on-going 1'b1: Always push the buffer
28	**PTCH28**	SDIO_INT_DLY_SEL	**SDIO interrupt latch time selection** 1'b0: Latch the data line value in internal SDIO interrupt period 1'b1: Latch the data line value in 1 clock delay of internal SDIO interrupt period

Bit(s)	Mnemonic	Name	Description
27	**PTCH27**	SDC_CMD_CMDFAIL_SEL	**SDIO interrupt period recovery selection** 1'b0: SDIO interrupt period will re-start after a CMD12 or CMD52 command is issued 1'b1: SDIO interrupt period whenever DAT line is not busy
26	**PTCH26**	SDC_CMD_IDRT_SEL	**SD identification response time selection** The register bit indicates if the command has a response with NID (that is, 5 serial clock cycles as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 1.0) response time. The register bit is valid only when the command has a response token. Thus the register bit must be set to 1 for CMD2 (ALL_SEND_CID) and ACMD41 (SD_APP_OP_CMD). 1'b0: Otherwise. 1'b1: The command has a response with NID response time.
25:22	**PTCH22**	SDC_CFG_WDOD	**SD Write Data Output Delay** The period from finish of the response for the initial host write command or the last write data block in a multiple block write operation to the start bit of the next write data block requires at least two serial clock cycles. The register field is used to extend the period (Write Data Output Delay) in unit of one serial clock. 4'b0000: No extend. 4'b0001: Extend one more serial clock cycle. 4'b0010: Extend two more serial clock cycles. 4'b1111: Extend fifteen more serial clock cycle.
21:18	**PTCH18**	SDC_CFG_BSYDLY	**SD R1B busy detection mode** The register field is only valid for the commands with R1b response. If the command has a response of R1b type, MS/SD controller must monitor the data line 0 for card busy status from the bit time that is two serial clock cycles after the command end bit to check if operations in SD/MMC Memory Card have finished. The register field is used to expand the time between the command end bit and end of detection period to detect card busy status. If time is up and there is no card busy status on data line 0, then the controller will abandon the detection. 4'b0000: No extend. 4'b0001: Extend one more serial clock cycle.

Bit(s)	Mnemonic	Name	Description
			4'b0010: Extend two more serial clock cycles. 4'b1111: Extend fifteen more serial clock cycle.
17	**PTCH17**	SDIO_CFG_INTC_SEL	**SDIO Interrupt model selection** 1'b0: Only when data line [1] = 0 and then trigger SDIO interurpt event 1'b1: Only when data line [3:0] = 4'b1101 and then trigger SDIO interurpt event
16	**PTCH16**	MSDC_BLKNUM_SEL	**Configuration support ACMD23 reliable/force prog etc. feature** 1'b0: Support ACMD23 reliable/force prog etc. feature 1'b1:Don't support ACMD23 reliable/force prog etc. feature
15	**PTCH15**	MSDC_FIFO_RD_DIS	**MSDC RXFIFO Read Disable** 1'b0: Disable FIFO read permission to RXFIFO in PIO mode 1'b1: Enable FIFO read permission to RXFIFO in PIO mode
14:10	**CKGDLYS**	CKGEN_MSDC_DLY_SEL	**CKBUF in CKGEN Delay Selection** Total 32 stages
9:7	**INTCKS**	INT_DAT_LATCH_CK_SEL	**Internal MSDC clock phase selection** Total 8 stages, each stage can delay 1 clock period of msdc_src_ck
6	**DESCUP**	DESC_UP_SEL	**sd transfer done int should be issue when GPD have been update** 1'b1:enable new function for generate sd transfer done int 1'b0:use old function for generate sd transfer done int
3	**PTCH3**	RD_DAT_SEL	**This field is used to define whther used rising or falling buf data for SDR mode** 1'b0: Used rising buf data for SDR mode 1'b1: Used falling buf data for SDR mode
2	**PTCH02**	DIS_REFLECT_CMDWR_WHEN_BSY	**Enable SD command register write montior** 1'b0: Enable monitor function 1'b1: Disable monitor function

Bit(s)	Mnemonic	Name	Description
1	**PTCH01**	EN_SDC_ODD_8BIT_SUP	**Enable SD odd number support for 8-bit data bus** 1'b0: Disable 1'b1: Enable
0	**PTCH00**	EN_START_BIT_CHK_SUP	**Enable SD start bit check function** 1'b0: Disable 1'b1: Enable

112300B4 PATCH_BIT1 MSDC Patch Bit Register 1 FFE24309

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSDC_CK_SHBFF_CKEN	MSDC_CK_RCTL_CKEN	MSDC_CK_WCTL_CKEN	MSDC_CK_SD_CKEN	MSDC_CK_ACMD_CKEN	MSDC_CK_VOLDET_CKEN	MSDC_CK_PSC_CKEN	MSDC_CK_SPC_CKEN	AHB_CK_GDMA_CKEN	AXI_WRAP_CKEN	DCM_EN				FORCE_STOP_GDMA	ENABLE_SINGLE_BURST
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1				1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESET_GDMA	DDR_CMD_FIX_SEL	BIAS_EXTBIAS_28NM	BIAS_EN18IO_28NM	STOP_DLY_SEL				BUSY_CHECK_SEL	GET_BUSY_MARGIN	CMD_RSP_TA_CNTR			WRDAT_CRCS_TA_CNTR		
Type	RW	RW	RW	RW	RW				RW	RW	RW			RW		
Reset	0	1	0	0	0	0	1	1	0	0	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
31	**MSHBFCKEN**	MSDC_CK_SHBFF_CKEN	**msdc_src_ck clock enable bit for SHBFF** 1'b0: Disable 1'b1: Enable
30	**MRCTLCKEN**	MSDC_CK_RCTL_CKEN	**msdc_src_ck clock enable bit for RCTL** 1'b0: Disable 1'b1: Enable
29	**MWCTLCKEN**	MSDC_CK_WCTL_CKEN	**msdc_src_ck clock enable bit for WCTL** 1'b0: Disable 1'b1: Enable

Bit(s)	Mnemonic	Name	Description
28	**MSDCKEN**	MSDC_CK_SD_CKEN	**msdc_src_ck clock enable bit for SD** 1'b0: Disable 1'b1: Enable
27	**MACMDCKEN**	MSDC_CK_ACMD_CKEN	**msdc_src_ck clock enable bit for ACMD** 1'b0: Disable 1'b1: Enable
26	**MVOLDTCKEN**	MSDC_CK_VOLDET_CKEN	**msdc_src_ck clock enable bit for VOLDET** 1'b0: Disable 1'b1: Enable
25	**MPSCCKEN**	MSDC_CK_PSC_CKEN	**msdc_src_ck clock enable bit for PSC** 1'b0: Disable 1'b1: Enable
24	**MSPCCKEN**	MSDC_CK_SPC_CKEN	**msdc_src_ck clock enable bit forSPC** 1'b0: Disable 1'b1: Enable
23	**HGDMACKEN**	AHB_CK_GDMA_CKEN	**hclk_ck clock enable bit for GDMA** 1'b0: Disable 1'b1: Enable
22	**AXIWRAPCKEN**	AXI_WRAP_CKEN	**axi_ck and ahb_ck enbale bit for ahb2axi wrapper.must set this bit to 1 when in dma mode for emmc50 spec,or this bit is reserverd** 1'b0:disable 1'b1:enable
21	**DCMEN**	DCM_EN	**host enable dcm for low power,when there is no transfer the ahb_ck and msdc_src_ck will divder from spurce clk** 1'b1:disable 1'b0:enable
17	**FORCESTOP**	FORCE_STOP_GDMA	**this bit can force state from WDMI_LAST_DATA to WDMI_IDLE with stop dma bit**

Bit(s)	Mnemonic	Name	Description
			1'b1 :enable stop wdmi_cs when state hang in WDMI_LAST_DATA with stop dma bit 1'b0 :disable
16	**SINGLEBURST**	ENABLE_SINGLE_BURST	**the ahb bus will not support incr1 burst type in future.And it will only affect AHB bus msdc design,not affect AXI bus design** 1'b0:hw will send incr1 burst type 1'b1: hw will send single burst typr instead of incr1 type
15	**RESETGDMA**	RESET_GDMA	**sw can sw reset gdma when design hang** 1 'b1: reset gdma 1'b0: not reset gdma
14	**DDRCMDFIXSEL**	DDR_CMD_FIX_SEL	**add T/4 margin for DDR mode cmd** 1'b1: fix DDR/HS400 mode cmd timing 1'b0: not fix
13	**BIAS28R0**	BIAS_EXTBIAS_28NM	**28NM BIAS Controler register 0**
12	**BIAS28R1**	BIAS_EN18IO_28NM	**28NM BIAS Controler register 1**
11:8	**STOPDLYSEL**	STOP_DLY_SEL	**configuration read data clock stop at block gap**
7	**BUSYCHECKSEL**	BUSY_CHECK_SEL	**1.r1b check dat0 then gen irq** 2.write prog time out check 1'b0: do not check data0 status gen cmdrdy int when send R1b cmd / do not check write prog timeout 1'b1: check data0 status gen cmdrdy int when send R1b cmd / check write prog timeout
6	**GETBUSYMARGIN**	GET_BUSY_MARGIN	**it will add margin for get busy state of data0** 1'b0: 1 cycle reserved for get busy state from src status endbit 1'b1: 3cycle reserved for get busy state from src status endbit
5:3	**CMDTA**	CMD_RSP_TA_CNTR	**CMD response turn around period** The turn around cycle = CMD_RSP_TA_CNTR + 2 In USH104 mode, this register should be set to 1

Bit(s)	Mnemonic	Name	Description
			In non-UHS104 mode, this register should be set to 0
2:0	**WRTA**	WRDAT_CRCS_TA_CNTR	**Write data and CRC status turn around period** The turn around cycle = WRDAT_CRCS_TA_CNTR + 2 In USH104 mode, this register should be set to 1 In non-UHS104 mode,this register should be set to 0

112300B8 PATCH_BIT2 MSDC Patch Bit Register 2 14881803

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRCSTS_LATCH_EN_SEL			CFG_CRCSTS	CFG_CRCSTS_CNT		CFG_CRCSTS_EDGE	CFG_CRCSTS_SEL	POP_EN_CNT				DDR50_SEL	RESP_LATCH_EN_SEL		
Type	RW			RW	RW		RW	RW	RW				RW	RW		
Reset	0	0	0	1	0	1	0	0	1	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG_RESP	CFG_RESP_CNT			INTC_RESP_SEL		CFG_RDAT	CFG_RDAT_CNT					RESP_WAIT_CNT		SUPPORT_64G	ENHANCE_WAIT_GPD
Type	RW	RW			RW		RW	RW					RW		RW	RW
Reset	0	0	0	1	1		0	0	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:29	**CRCSTSENSEL**	CRCSTS_LATCH_EN_SEL	**This register used configuration latch CRC Status enable signal for async fifo in emmc45** 3'b000: latch CRC Status enable signal not delay 3'b001: latch CRC Status enable signal delay 1T msdc_ck 3'b010: latch CRC Status enable signal delay 2T msdc_ck 3'b011: latch CRC Status enable signal delay 3T msdc_ck 3'b111: latch CRC Status enable signal delay 7T msdc_ck
28	**CFGCRCSTS**	CFG_CRCSTS	**This register used configuration CRC Status path selection,this setting only used emmc4.5 feature** 1'b0:Latch CRC Status select delay-line path 1'b1:Latch CRC Status select async fifo path

Bit(s)	Mnemonic	Name	Description
27:26	**CFGCRCSTSCNT**	CFG_CRCSTS_CNT	**This register used configuration how many data push in async fifo until start pop out data from async fifo ,this register setting min is 1 do not setting is 0,this setting only used emmc4.5 feature** 2'b00:push 0 data in async fifo when start pop out data from async fifo 2'b01:push 1 data in async fifo when start pop out data from async fifo 2'b10:push 2 data in async fifo when start pop out data from async fifo 2'b11:push 3 data in async fifo when start pop out data from async fifo
25	**CFGCRCSTSEDGE**	CFG_CRCSTS_EDGE	**This register configuration used rising async fifo or falling async fifo** 1'b0:async fifo latch CRC Status used rising async fifo 1'b1:async fifo latch CRC Status used falling async fifo
24		CFG_CRCSTS_SEL	**This register configuration async fifo path selection** 1'b0:used normal path in async fifo 1'b1:used 2DFF path in async fifo
23:20	**POPENCNT**	POP_EN_CNT	**pop enable counter** This field is used to define how many write pointer and the read pointer margin began to pop data transfer
19	**DDR50SEL**	DDR50_SEL	**new path can avoid byte swap issue** 1'b0:old path for rising and faling data 1'b1:new path that rasing data to rasing fifo and faling data to faling fifo
18:16	**RESPSTSENSEL**	RESP_LATCH_EN_SEL	**This register used configuration latch CMD Response enable signal for async fifo in emmc45** 3'b000: latch CMD Response enable signal not delay 3'b001: latch CMD Response enable signal delay 1T msdc_ck 3'b010: latch CMD Response enable signal delay 2T msdc_ck 3'b011: latch CMD Response enable signal delay 3T msdc_ck

Bit(s)	Mnemonic	Name	Description
			3'b111: latch CMD Response enable signal delay 7T msdc_ck
15	**CFGRESP**	CFG_RESP	**This register used configuration CMD Response path selection,this setting only used emmc4.5 feature** 1'b0:Latch CMD Response select async fifo path 1'b1:Latch CMD Response select delay-line path
14:12	**CFGRESPCNT**	CFG_RESP_CNT	**This register used configuration how many data push in async fifo until start pop out data from async fifo ,this register setting min is 1 do not setting is 0,this setting only used emmc4.5 feature** 3'b000:push 0 data in async fifo when start pop out data from async fifo 3'b001:push 1 data in async fifo when start pop out data from async fifo 3'b111:push 7 data in async fifo when start pop out data from async fifo
11	**INTCRESPSEL**	INTC_RESP_SEL	**This register configuration BREAK command async fifo path** 1'b0:used normal path in async fifo 1'b1:used 2DFF path in async fifo
9	**CFGRDAT**	CFG_RDAT	**This register used configuration read data path** 1'b0: read data path by pass delay line 1'b1:read data path through delay line
8:4	**CFGRDATCNT**	CFG_RDAT_CNT	**This register used configuration read data path delay line**
3:2	**RESPWAITCNT**	RESP_WAIT_CNT	**This register used configuration cmd response timeout,timeout cycle is 65T+16*RESP_WAIT_CNT** 2'b00:cmd response timeout is 65T 2'b01:cmd response timeout is 65T+ 16*1T 2'b01:cmd response timeout is 65T+ 16*2T 2'b01:cmd response timeout is 65T+ 16*3T
1	**SUPPORT64G**	SUPPORT_64G	**This register used which proj support high 64G dram space access** 1'b1:support 64G dram access

Bit(s)	Mnemonic	Name	Description
			1'b0:not support 64G dram access
0	**ENHANCEGPD**	ENHANCE_WAIT_GPD	**if sw clear int when gpd not update finish,design will hang.so you can set this bt to 1 to avoid this iuuse in enhance write mode** 1'b1:use new HW code for update gpd in enhance mode 1'b0:use old HW code

112300F0 PAD_TUNE0 MSDC Pad Tuning Register0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PAD_CLK_TXDLY					PAD_CMD_RESP_RXDLY					PAD_CMD_RD_RXDLY_SEL	PAD_CMD_RXDLY				
Type	RW					RW					RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAD_RXDLY_SEL		PAD_DAT_RD_RXDLY_SEL	PAD_DAT_RD_RXDLY					DELAY_EN			PAD_DAT_WR_RXDLY				
Type	RW		RW	RW					RW			RW				
Reset	0		0	0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:27	**CLKTDLY**	PAD_CLK_TXDLY	**CLK Pad TX Delay Control** This register is used to add delay to CLK phase. Total 32 stages
26:22	**CMDRRDLY**	PAD_CMD_RESP_RXDLY	**CMD Response Internal Delay Line Control** This register is used to fine-tune response phase latched by MSDC internal clock Total 32 stages
21	**CMDRRDLYSEL**	PAD_CMD_RD_RXDLY_SEL	**Decide CMD Response pass through data delay line1 or not** 1'b0: pass

Bit(s)	Mnemonic	Name	Description
			1'b1: do not pass
20:16	**CMDRDLY**	PAD_CMD_RXDLY	**CMD Pad RX Delay Line1 Control** This register is used to fine-tune CMD pad macro respose latch timing Total 32 stages
15	**RXDLYSEL**	PAD_RXDLY_SEL	**Decide rx delay line tune data path or clock path** 1'b0: rx delay line tune data path 1'b1: rx delay line tune clock path
13	**DATRRDLYSEL**	PAD_DAT_RD_RXDLY_SEL	**Decide rx data pass through data delay line1 or not** 1'b0: pass 1'b1: do not pass
12:8	**DATRRDLY**	PAD_DAT_RD_RXDLY	**DAT Pad RX Delay Line1 Control (for MSDC read only)** This register is used to fine-tune DAT pad macro read data latch timing Total 32 stages
7	**DELAYEN**	DELAY_EN	**enable all delay cell toogle when power on** 1'b0:disable delay cell toogle default 1'b1:enable delay cell toogle default
4:0	**DATWRDLY**	PAD_DAT_WR_RXDLY	**Write Data Status Internal Delay Line Control** This register is used to fine-tune write status phase latched by MSDC internal clock Total 32 stages

112300F4 PAD_TUNE1 MSDC Pad Tuning Register1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											PAD_CMD_RD_RXDLY2_SEL	PAD_CMD_RXDLY2				
Type											RW	RW				
Reset											0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			PAD_DAT_RD_RXDLY2_SEL	PAD_DAT_RD_RXDLY2												
Type			RW	RW												
Reset			0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
21	**CMDRRDLY2SEL**	PAD_CMD_RD_RXDLY2_SEL	**Decide CMD Response pass through data delay line2 or not** 1'b0: pass 1'b1: do not pass
20:16	**CMDRDLY2**	PAD_CMD_RXDLY2	**CMD Pad RX Delay Line2 Control** This register is used to fine-tune CMD pad macro respose latch timing in data path Total 32 stages
13	**DATRRDLY2SEL**	PAD_DAT_RD_RXDLY2_SEL	**Decide rx data pass through data delay line2 or not** 1'b0: pass 1'b1: do not pass
12:8	**DATRRDLY2**	PAD_DAT_RD_RXDLY2	**DAT Pad RX Delay Line2 Control (for MSDC read only)** This register is used to fine-tune DAT pad macro read data latch timing Total 32 stages

112300F8 DAT_RD_DLY0 MSDC Data Delay Line Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0_RD_DLY								DAT1_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT2_RD_DLY								DAT3_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT0RDDLY**	DAT0_RD_DLY	**DAT0 Pad RX Delay Line1 Control (for MSDC RD)** Total 32 stages
20:16	**DAT1RDDLY**	DAT1_RD_DLY	**DAT1 Pad RX Delay Line1 Control (for MSDC RD)** Total 32 stages
12:8	**DAT2RDDLY**	DAT2_RD_DLY	**DAT2 Pad RX Delay Line1 Control (for MSDC RD)** Total 32 stages
4:0	**DAT3RDDLY**	DAT3_RD_DLY	**DAT3 Pad RX Delay Line1 Control (for MSDC RD)** Total 32 stages

112300FC DAT_RD_DLY1 MSDC Data Delay Line Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT4_RD_DLY								DAT5_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT6_RD_DLY								DAT7_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT4RDDLY**	DAT4_RD_DLY	**DAT4 Pad RX Delay Line1 Control (for MSDC RD)** Total 32 stages
20:16	**DAT5RDDLY**	DAT5_RD_DLY	**DAT5 Pad RX Delay Line1 Control (for MSDC RD)** Total 32 stages
12:8	**DAT6RDDLY**	DAT6_RD_DLY	**DAT6 Pad RX Delay Line1 Control (for MSDC RD)** Total 32 stages
4:0	**DAT7RDDLY**	DAT7_RD_DLY	**DAT7 Pad RX Delay Line1 Control (for MSDC RD)** Total 32 stages

11230100 DAT_RD_DLY2 MSDC Data Delay Line Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0_RD_DLY2								DAT1_RD_DLY2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT2_RD_DLY2								DAT3_RD_DLY2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT0RDDLY2**	DAT0_RD_DLY2	**DAT0 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages
20:16	**DAT1RDDLY2**	DAT1_RD_DLY2	**DAT1 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages
12:8	**DAT2RDDLY2**	DAT2_RD_DLY2	**DAT2 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages
4:0	**DAT3RDDLY2**	DAT3_RD_DLY2	**DAT3 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages

11230104 DAT_RD_DLY3 MSDC Data Delay Line Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT4_RD_DLY2								DAT5_RD_DLY2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT6_RD_DLY2								DAT7_RD_DLY2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT4RDDLY2**	DAT4_RD_DLY2	**DAT4 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages

Bit(s)	Mnemonic	Name	Description
20:16	**DAT5RDDLY2**	DAT5_RD_DLY2	**DAT5 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages
12:8	**DAT6RDDLY2**	DAT6_RD_DLY2	**DAT6 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages
4:0	**DAT7RDDLY2**	DAT7_RD_DLY2	**DAT7 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages

11230110 HW_DBG_SEL MSDC H/W Debug Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HW_DBG_WRAP_SEL	HW_DBG_WRAP_TYPE_SEL		HW_DBG3_SEL					HW_DBG2_SEL							
Type	RW	RW		RW					RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_DBG1_SEL								HW_DBG0_SEL							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**DBGWSEL**	HW_DBG_WRAP_SEL	**H/W debug output selection for wrapper** 0: Select original debug pins 1: Select wrapper debug pins
30:29	**DBGWTSEL**	HW_DBG_WRAP_TYPE_SEL	**H/W debug output type selection for wrapper** 2'b00: Select dram bus debug signal 2'b01: Select risc bus debug signal 2'b10: select ahbm bus debug signal 2'b11: select ahbs bus debug signal
28:24	**DBG3SEL**	HW_DBG3_SEL	**H/W debug output selection**
23:16	**DBG2SEL**	HW_DBG2_SEL	**H/W debug output selection**
15:8	**DBG1SEL**	HW_DBG1_SEL	**H/W debug output selection**

Bit(s)	Mnemonic	Name	Description
7:0	**DBG0SEL**	HW_DBG0_SEL	**H/W debug output selection**

11230114 MAIN_VER MSDC Main Version Register 20160506

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAIN_VER															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAIN_VER															
Type	RO															
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0

Bit(s)	Mnemonic	Name	Description
31:0	**MAINVER**	MAIN_VER	**Main Version**

11230118 ECO_VER MSDC ECO Version Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ECO_VER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ECO_VER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ECOVER**	ECO_VER	**ECO Version**

1123021C EMMC50_CFG2 ahb2axi wrapper control register 0F0C0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name		AXI_BUSY	AXI_RESP_ERR_TYPE		AXI_SET_LEN				AXI_RD_OUTSTANDING_NUM					AXI_BOUND_4K	AXI_BOUND_2K	AXI_BOUND_1K
Type		RO	RO		RW				RW					RW	RW	RW
Reset		0	0	0	1	1	1	1	0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_BOUND_512B	AXI_BOUND_256B	AXI_BOUND_128B					AXI_SHARE_EN_RD_EMI	AXI_IOMMU_RD_EMI	reserved1				AXI_SHARE_EN_WR_EMI	AXI_IOMMU_WR_EMI	
Type	RW	RW	RW					RW	RW	RW				RW	RW	
Reset	0	0	0					0	0	0	0	0	0	0	0	

Bit(s)	Mnemonic	Name	Description
30	**AXIBUSY**	AXI_BUSY	**check if axi bus is busy or idle** 1'b1:axi wrapper is busy 1'b0:axi wrapper is idle
29:28	**RESPERRTYPE**	AXI_RESP_ERR_TYPE	**when sw get axi respnse error int,you can check this bits to know which type error occr** 2'b00:no error 2'b01:do not care 2'b10:slave error 2'b11:decode error
27:24	**SETLEN**	AXI_SET_LEN	**sw can program this bits to set the transfer num in one axi burst both for read and write.for perfomance,this bits can set up to f** 4'b0000:1 beats per one burst 4'b0001:2 beats per one burst 4'b0010:3 beats per one burst... 4'b1111:16 beats per one burst
23:19	**RDOUTSTANDINGNUM**	AXI_RD_OUTSTANDING_NUM	**axi support outstanding transfer,it means when there is no reponse you can also sent axi cmd.for perfomance ,sw cant set this bits up to 13** 5'b: 00001:support 1 outstanding 5'b: 00002:support 2 outstanding

Bit(s)	Mnemonic	Name	Description
			5'b: 00003:support 3 outstanding...
			5'b: 01011:support 13 outstanding
18	**BOUND4K**	AXI_BOUND_4K	**default is 4K in axi spec**
			1'b1:chose 4 K boundary
			1'b0:not chose 4K boundary
17	**BOUND2K**	AXI_BOUND_2K	**for future project option**
			1'b1:chose 2 K boundary
			1'b0:not chose 2K boundary
16	**BOUND1K**	AXI_BOUND_1K	**for future project option**
			1'b1:chose 42K boundary
			1'b0:not chose 1K boundary
15	**BOUND512B**	AXI_BOUND_512B	**for future project option**
			1'b1:chose 512B boundary
			1'b0:not chose 512B boundary
14	**BOUND256B**	AXI_BOUND_256B	**for future project option**
			1'b1:chose 256B boundary
			1'b0:not chose 256B boundary
13	**BOUND128B**	AXI_BOUND_128B	**for future project option**
			1'b1:chose 128B boundary
			1'b0:not chose 128B boundary
8	**SHAREENRDEMI**	AXI_SHARE_EN_RD_EMI	
7	**IOMMURDEMI**	AXI_IOMMU_RD_EMI	
6:3		reserved1	
2	**SHAREENWREMI**	AXI_SHARE_EN_WR_EMI	
1	**IOMMUWREMI**	AXI_IOMMU_WR_EMI	

11230220 EMMC50_CFG3 0F28A3C1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved2			PREULTRA_SET_RD						ULTRA_SET_RD						PREULTRA_SET_WR
Type	RO			RW						RW						RW
Reset	0	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PREULTRA_SET_WR					ULTRA_SET_WR						OUT_STANDING_WR				
Type	RW					RW						RW				
Reset	1	0	1	0	0	0	1	1	1	1	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:29		reserved2	
28:23	**PREULTRASETRD**	PREULTRA_SET_RD	**msdc gdma have more high priority when these bit set bigger**
22:17	**ULTRASETRD**	ULTRA_SET_RD	**msdc gdma have more high priority when these bit set bigger**
16:11	**PREULTRASETWR**	PREULTRA_SET_WR	**msdc gdma have more high priority when these bit set smaller**
10:5	**ULTRASETWR**	ULTRA_SET_WR	**msdc gdma have more high priority when these bit set smaller**
4:0	**OUTSTANDINGWR**	OUT_STANDING_WR	**axi support outstanding transfer,it means when there is no reponse you can also sent axi cmd.for improve perfomance ,sw cant set this bits up to 13**

11230224 EMMC50_CFG4 0001281E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved3									wrap_sel					ULTRA_EN	
Type	RO									RW					RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMPR_ULTRA_SET_RD								IMPR_ULTRA_SET_WR							
Type	RW								RW							
Reset	0	0	1	0	1	0	0	0	0	0	0	1	1	1	1	0

Bit(s)	Mnemonic	Name	Description
31:23		reserved3	
22:18	**WRAP_SEL**	wrap_sel	**for hw sel debug signal**
17:16	**ULTRAEN**	ULTRA_EN	**normally ,can not set to high priority,because it will reduce oher module performace** 2'b00:lowest priority 2'b01:lower priority 2'b10:middle priority 2'b11:high priority
15:8	**IMPRULTRASETRD**	IMPR_ULTRA_SET_RD	**msdc gdma have more high priority when these bit set bigger.host can improve priority at base of set ULTRA_SET_RD**
7:0	**IMPRULTRASETWR**	IMPR_ULTRA_SET_WR	**msdc gdma have more high priority when these bit set smaller.host can improve priority at base of set ULTRA_SET_WR**

11230228 SDC_FIFO_CFG 070C0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RD_VALID	WR_VALID	RD_VALID_SEL	WR_VALID_SEL	WR_PTR_MARGIN							
Type					RU	RU	RW	RW	RW							
Reset					0	1	1	1	0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								EMMC50_BLOCK_LENGTH								
Type								RW								
Reset								0	1	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27	**RDVALID**	RD_VALID	**host have whole block len data in fifo when host want transfer data to device** 1'b0:the sd fifo is not valid to read for writing device 1'b1:the sd fifo is valid to read for writing device

Bit(s)	Mnemonic	Name	Description
26	**WRVALID**	WR_VALID	**host have enough space for storing a block len data read from device** 0:the sd fifo is not valid for reading data from device 1:the sd fifo is valid for reading data from device
25	**RDVALIDSEL**	RD_VALID_SEL	**this register use for configuration read data valid case when read data transfer** 1'b0: read data always valid only that host have enough space for storing a block len data read from device 1'b1: read data always valid
24	**WRVALIDSEL**	WR_VALID_SEL	**this register use for configuration write data valid case when write data transfer** 1'b0: write data always valid only that host have whole block len data in fifo when host want transfer data to device 1'b1: write data always valid
23:16	**WRPTRMARGIN**	WR_PTR_MARGIN	**write pointer marign**
8:0	**BLOCKLENGTH**	EMMC50_BLOCK_LENGTH	**sw set the fifo water level for stop clk in diff block length.** If device block length is 512B,this register should set 9'd128 If device block length is 256B,this register should set 9'd64 If device block length is 128B,this register should set 9'd32 If device block length is 64B,this register should set 9'd16 If device block length is 32B,this register should set 9'd8

1.27 Memory Stick and SD Card Controller (MSDC 1)

1.27.1 Introduction

The MSDC (Memory Stick and SD card Controller) fully supports functions as follow

- MMC/eMMC4.41 (MSDC0)
- SD memory card specification version 3.0 (MSDC1)
- SDIO card specification version 3.0 (MSDC1)

1.27.2 Features

MSDC1 contains:

- 32-bit access for control registers
- 8-bit/16-bit/32-bit access for FIFO in PIO mode
- Built-in CRC circuit
- PIO mode, Basic DMA mode, Descriptor mode for SD/eMMC
- Interrupt capabilities for SDIO
- Does not support SPI mode for SD/MMC memory card
- Does not support suspend/resume for SD/MMC memory card
- Supports SD3.0 SDR104, data rate up to 208x4Mbps
- Supports SD3.0 DDR50, data rate up to 50x4x2Mbps(4-bit with clock dual edge)
- Supports boot-up mode (MSDC1)
- 256 programmable serial clock rates on SD/MMC bus from 100kHz to 208MHz
- Card detection capabilities (MSDC1)

1.27.3 Register Definition

Module name: MSDC1 Base address: (+11240000h)

Address	Name	Width	Register Function
11240000	MSDC_CFG	32	MSDC Configuration Register The register is for general configuration of the MS/SD controller.
11240004	MSDC_IOCON	32	MSDC IO Configuration Register The register contains the receiver path data latch timing control and interface control bits.
11240008	MSDC_PS	32	MSDC Pin Status Register The register is used to storing card detection and write protection pin status. Card detection status can be disabled.
1124000C	MSDC_INT	32	MSDC Interrupt Register The register contains the status of interrupts. Note that the register still shows the status of interrupt even though the interrupt is disabled.
11240010	MSDC_INTEN	32	MSDC Interrupt Enable Register

Address	Name	Width	Register Function
			The register contains the related enable bit of interrupts.
11240014	MSDC_FIFOCS	32	MSDC FIFO Control and Status Register The register contains the control and status of embedded 128B FIFO.
11240018	MSDC_TXDATA	32	MSDC TX Data Port Register The register is for PIO mode only. Used to input MSDC write data to card. The access can be AHB 1B/2B/4B
1124001C	MSDC_RXDATA	32	MSDC RX Data Port Register The register is for PIO mode only. Used to read back MSDC read data from card. The access can be AHB 1B/2B/4B.
11240030	SDC_CFG	32	SD Configuration Register The register is used for configuring the MS/SD Memory Card Controller when it is configured as the host of SD Memory Card. If the controller is configured as the host of Memory Stick, the contents of the register have no impact on the operation of the controller.
11240034	SDC_CMD	32	SD Command Register The register defines a SD Memory Card command and its attributes. Before MS/SD controller issues a transaction onto SD bus, application shall specify other relative settings such as argument for command. After writing the register by the application, MS/SD controller will issue the corresponding transaction onto SD serial bus. If the command is GO_IDLE_STATE, the controller will have serial clock on SD/MMC bus run 128 cycles before issuing the command.
11240038	SDC_ARG	32	SD Argument Register The register contains the argument of the SD/MMC Memory Card command.
1124003C	SDC_STS	32	SD Status Register The register reflects SD bus status and contains MMC stream write status.
11240040	SDC_RESP0	32	SD Response Register 0 The register contains parts of the last SD/MMC Memory Card bus response. See description for the register field SDC_RESP3.
11240044	SDC_RESP1	32	SD Response Register 1 The register contains parts of the last SD/MMC Memory Card bus response. See description for the register field SDC_RESP3.
11240048	SDC_RESP2	32	SD Response Register 2 The register contains parts of the last SD/MMC Memory Card bus response. See description for the register field SDC_RESP3.
1124004C	SDC_RESP3	32	SD Response Register 3 The register contains parts of the last SD/MMC Memory Card bus response. The register fields

Address	Name	Width	Register Function
			SDC_RESP0, SDC_RESP1, SDC_RESP2 and SDC_RESP3 are composed of the last SD/MMC Memory card bus response. For response of type R2, that is, response of the command ALL_SEND_CID, SEND_CSD and SEND_CID, only bit 127 to 0 of response token is stored in the register field SDC_RESP0, SDC_RESP1, SDC_RESP2 and SDC_RESP3. SDC_RESP0 = bit 31~0 SDC_RESP1 = bit 63~32 SDC_RESP2 = bit 95~64 SDC_RESP3 = bit 127~96 For response of type R1b in auto CMD12 or R1 in auto CMD23, bit 39 to 8 of response token is stored in the register field of SDC_RESP3. For the responses of other types, only bit 39 to 8 of response token is stored in the register field SDC_RESP0.
11240050	SDC_BLK_NUM	32	SD Block Number Register This register defines the block number for the block transaction. For single read/write, this register should be set to 1. For multiple read/write, this register should be set to larger than 1. Set to 0 will cause unexpected result.
11240054	SDC_VOL_CHG	32	SD Voltage Change Wait Time Register This register define SD voltage change check wait time
11240058	SDC_CSTS	32	SD Card Status Register After commands with R1 and R1b response, this register will contain the status of the SD/MMC card
1124005C	SDC_CSTS_EN	32	SD Card Status Enable Register This register is used to control which bit of the SDC_CSTS will generate the MSDC_INT.SD_CSTA interrupt.
11240060	SDC_DATCRC_STS	32	SD Card Data CRC Status Register This register reflects the CRC status of data line[7:0]. This register is only for MSDC Read
11240064	SDC_ADV_CFG0	32	SDC Advance Configuration 0 This register used to config sdc advance feature
11240070	EMMC_CFG0	32	EMMC Configuration Register 0 The register is used for boot up mode general configuration of e-MMC version 4.3 and 4.4.
11240074	EMMC_CFG1	32	EMMC Configuration Register 1 The register is used for boot up mode general configuration of e-MMC version 4.3 and 4.4.
11240078	EMMC_STS	32	EMMC Status Register The register reflects the status of e-MMC boot up mode operation.
1124007C	EMMC_IOCON	32	EMMC IO Control Register The register controls the H/W reset pin of e-MMC boot up mode operation.
11240080	SD_ACMD_RESP	32	SD ACMD Response Register This register stores the response of auto command from SD card
11240084	SD_ACMD19_TRG	32	SD ACMD19 Target Register

Address	Name	Width	Register Function
			This register is used to select target delay line to run ACMD19 sequence.
11240088	SD_ACMD19_STS	32	SD ACMD19 Status Register This register stores the result of auto command 19 from SD card
1124008C	DMA_SA_HIGH4BIT	32	DMA Current Address Resgiter of high 4bit This register contain the start address high 4bit of 36bit address for 64G dram access
11240090	DMA_SA	32	DMA Start Address Register This register contains the start address of the DMA descriptor
11240094	DMA_CA	32	DMA Current Address Register This register contains the current DMA address
11240098	DMA_CTRL	32	DMA Control Register This register is used to control the DMA operation.
1124009C	DMA_CFG	32	DMA Configuration Register This register is used to configure the DMA operation.
112400A0	SW_DBG_SEL	32	MSDC S/W Debug Selection Register This register is used to select S/W debug output
112400A4	SW_DBG_OUT	32	MSDC S/W Debug Output Register This register shows the selected debug output
112400A8	DMA_LENGTH	32	DMA Length Register This register is used to set Basic DMA operation length
112400B0	PATCH_BIT0	32	MSDC Patch Bit Register 0 This register can configure the patch function. For normal function, these bit should keep in default value
112400B4	PATCH_BIT1	32	MSDC Patch Bit Register 1 This register can configure the patch function. For normal function, these bit should keep in default value
112400B8	PATCH_BIT2	32	MSDC Patch Bit Register 2 This register can configure the patch function. For normal function, these bit should keep in default value
112400C0	DAT0_TUNE_CRC	32	DAT0 Tune Result Register This register record on-line tuning result for DAT0 line
112400C4	DAT1_TUNE_CRC	32	DAT1 Tune Result Register This register record on-line tuning result for DAT1 line
112400C8	DAT2_TUNE_CRC	32	DAT2 Tune Result Register This register record on-line tuning result for DAT2 line
112400CC	DAT3_TUNE_CRC	32	DAT3 Tune Result Register This register record on-line tuning result for DAT3 line
112400D0	CMD_TUNE_CRC	32	CMD Tune Result Register This register record on-line tuning result for CMD line
112400D4	SDIO_TUNE_WIND	32	SDIO Tune Window Register 0 This register define tuning window size for SDIO on-line CRC tuning feature
112400F0	PAD_TUNE0	32	MSDC Pad Tuning Register0

Address	Name	Width	Register Function
			This register can configure the delay line embedded in Pad Macro
112400F4	PAD_TUNE1	32	MSDC Pad Tuning Register1 This register can configure the delay line embedded in Pad Macro
112400F8	DAT_RD_DLY0	32	MSDC Data Delay Line Register 0 This register can configure the delay line embedded in Pad Macro
112400FC	DAT_RD_DLY1	32	MSDC Data Delay Line Register 1 This register can configure the delay line embedded in Pad Macro
11240100	DAT_RD_DLY2	32	MSDC Data Delay Line Register 2 This register can configure the delay line embedded in Pad Macro
11240104	DAT_RD_DLY3	32	MSDC Data Delay Line Register 3 This register can configure the delay line embedded in Pad Macro
11240110	HW_DBG_SEL	32	MSDC H/W Debug Selection Register This register can select the H/W debug output
11240114	MAIN_VER	32	MSDC Main Version Register This register shows the version code of MSDC IP
11240118	ECO_VER	32	MSDC ECO Version Register This register shows the ECO version code of MSDC IP

11240000 MSDC_CFG MSDC Configuration Register 02000099

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			BW_SEL				SCLK_STOP_SEL				CARD_CK_MODE		CARD_CK_DIV			
Type			RW				RW				RW		RW			
Reset			0				1				0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CARD_CK_DIV								CARD_CK_STABLE	BV_1P8_PASS	BV_1P8_START_DET	CARD_CK_DRV_EN	PIO_MODE	RST	CARD_CK_PWDN	MSDC
Type	RW								RU	RU	RW	RW	RW	A0	RW	RW
Reset	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
29	**BWSEL**	BW_SEL	**save power for low throughput requirement**

Bit(s)	Mnemonic	Name	Description
			1'b0:the memory provide diff throughput for diff msdc speed mode 1'b1:memory provide highest throughput for all speed mode
25	**SCLKSTOPSEL**	SCLK_STOP_SEL	**In DDR mode,stop SCLK when device is idle whether check SCLK phase** 1'b0: stop sclk no check SCLK phase 1'b1 : stop sclk check SCLK phase,fix 1/4T sclk glitch in DDR mode
21:20	**CCKMD**	CARD_CK_MODE	**2'b00: Use clock divider output which divided by msdc_src_ck as msdc_ck, bit[15]~bit[8] should be programmed.** 2'b01: Use msdc_src_ck as msdc_ck, bit[15]~bit[8] is ignored. 2'b10: DDR mode, also use clock divider output which divided by msdc_src_ck as msdc_ck, bit[15]~bit[8] should be programmed. 2'b11: HS400 mode,also use clock divider output and use msdc_src_ck as msdc_ck, bit[15]~bit[8] should be programmed 2'b00: Use clock divider output which divided by msdc_src_ck as msdc_ck, bit[19]~bit[8] should be programmed. 2'b01: Use msdc_src_ck as msdc_ck, bit[19]~bit[8] is ignored. 2'b10: DDR mode, also use clock divider output which divided by msdc_src_ck as msdc_ck, bit[19]~bit[8] should be programmed. 2'b11: HS400 mode,also use clock divider output or use msdc_src_ck as msdc_ck.when HS400_CK_MODE set to 0, bit[15]~bit[8] should be programmed.When HS400_CK_MODE set to 1,bit[19]~bit[8] is ignored.
19:8	**CCKDIV**	CARD_CK_DIV	**MS/SD Card clock divider** The register field controls clock frequency of serial clock on MS/SD bus. Please refer to Data Line Latching Timing Diagram and Response Latching Timing Diagram. For non-DDR mode, msdc_ck equals SD bus clock. (Ex: For SDR25 or HS, msdc_ck and SD bus clock will be 50MHz) For DDR mode, msdc_ck denotes the MSDC internal clock which will be dobule to SD bus clock. (Ex: For DDR50, msdc_ck should be set to 100MHz and bus clock will be 50MHz)

Bit(s)	Mnemonic	Name	Description
			12'b000000000000: msdc_ck =(1/2) * msdc_src_ck 12'b000000000001: msdc_ck = (1/(4*1)) * msdc_src_ck 12'b00000010: msdc_ck = (1/(4*2)) * msdc_src_ck 12'b000000000011: msdc_ck = (1/(4*3))* msdc_src_ck 12'b000000010000: msdc_ck = (1/(4*16))* msdc_src_ck 12'b111111111111: msdc_ck = (1/(4*4095)) * msdc_src_ck
7	**CCKSB**	CARD_CK_STABLE	**MS/SD Card clock stable or not** After programming the CARD_CK_MODE or CARD_CK_DIV, this bit will immediately go to "0" and return to "1" if stable. User should poll this register to make sure the safety control of MSDC. 1'b0: Clock output is not stable 1'b1: Clock output is stable
6	**BV18PSS**	BV_1P8_PASS	**MSDC Bus voltage 1.8V detection status** S/W should check this bit after BUS_VOL_18V_START_DET turns to 0 from 1. 1'b0: The voltage detection has error. 1'b1: The voltage detection has no error.
5	**BV18SDT**	BV_1P8_START_DET	**MSDC Bus voltage 1.8V detection sequence start event** S/W writes this bit to 1 to trigger H/W outputs 1.8V clock for 1 ms and automatically detect CMD/DAT line sequence for voltage change is passed or not. H/Q will clear this bit to 0 after the detection has finished. The pass or fail status is stored in bit[6] BUS_VOL_18V_PASS.
4	**CCKDRVE**	CARD_CK_DRV_EN	**SD/MS Card Bus Clock drive enable bit** Set this bit to 1 to enable MSDC bus clock driver. The default bus state depends on MSDC_CFG][1] CARD_CK_PWDN bit. If MSDC_CFG[1] CARD_CK_PWDN= 1, the default clock state is free running. If MSDC_CFG[1] CARD_CK_PWDN = 0, the default clock state is gated to 0.

Bit(s)	Mnemonic	Name	Description
			Set this bit to 0 will put the bus state into "tri-state". Default is 1. 1'b0: Put the clock pad into tri-state 1'b1: Enable MSDC to drive clock pad, the state of CLK depends on MSDC_CFG[1] CARD_CK_PWDN
3	**PIO**	PIO_MODE	**MS/SD PIO mode** PIO mode selection. Default is in PIO mode. 1'b0: DMA mode 1'b1: PIO mode
2	**RST**	RST	**Software reset** Writing 1 to this register will cause internal synchronous reset of MS/SD controller, and it will not reset register settings and DMA controller. The reset sequence is done when this bit goes to 0. S/W should wait this bit back to 0 after writing 1. 1'b0: MS/SD controller is not in reset state 1'b1: MS/SD controller is in reset state
1	**CCKPD**	CARD_CK_PWDN	**MSDC bus clock power down mode** This bit controls the card clock power down mode. 1'b0: Clock is gated to 0 if no command or data is transmitted. 1'b1: Clock is free running even if no command or data is transmitted. (The clock may still be stopped when MSDC write data is not enough or no space for next read data)
0	**MSDC**	MSDC	**MS/SD mode selection** The register bit is used to configure the controller as the host of Memory Stick or as the host of SD/MMC Memory card. The default value is to configure the controller as the host of Memory Stick. 1'b0: Configure the controller as the host of Memory Stick 1'b1: Configure the controller as the host of SD/MMC Memory card

11240004 MSDC_IOCON MSDC IO Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FPGA_D3_SMPL_SEL	FPGA_D2_SMPL_SEL	FPGA_D1_SMPL_SEL	FPGA_D0_SMPL_SEL					R_D7_SMPL	R_D6_SMPL	R_D5_SMPL	R_D4_SMPL	R_D3_SMPL	R_D2_SMPL	R_D1_SMPL	R_D0_SMPL
Type	RW	RW	RW	RW					RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0					0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			W_D3_SMPL	W_D2_SMPL	W_D1_SMPL	W_D0_SMPL	W_D_SMPL_SEL	W_D_SMPL			R_D_SMPL_SEL	DDR50_DLY_SEL	D_DLYLINE_SEL	R_D_SMPL	R_SMPL	SDR104_CLK_SEL
Type			RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		FPGA_D3_SMPL_SEL	
30		FPGA_D2_SMPL_SEL	
29		FPGA_D1_SMPL_SEL	
28		FPGA_D0_SMPL_SEL	
23	**RD7SPL**	R_D7_SMPL	**Read data 7 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
22	**RD6SPL**	R_D6_SMPL	**Read data 6 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
21	**RD5SPL**	R_D5_SMPL	**Read data 5 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge

Bit(s)	Mnemonic	Name	Description
			1'b1: Sample read data by external bus clock falling edge
20	**RD4SPL**	R_D4_SMPL	**Read data 4 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
19	**RD3SPL**	R_D3_SMPL	**Read data 3 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
18	**RD2SPL**	R_D2_SMPL	**Read data 2 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
17	**RD1SPL**	R_D1_SMPL	**Read data 1 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
16	**RD0SPL**	R_D0_SMPL	**Read data 0 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
13	**WD3SPL**	W_D3_SMPL	**SDIO interrupt sample selection** This bit is only valid when bit 9 is ON 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
12	**WD2SPL**	W_D2_SMPL	**SDIO interrupt sample selection** This bit is only valid when bit 9 is ON

Bit(s)	Mnemonic	Name	Description
			1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
11	**WD1SPL**	W_D1_SMPL	**SDIO interrupt sample selection** This bit is only valid when bit 9 is ON 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
10	**WD0SPL**	W_D0_SMPL	**CRC Status and SDIO interrupt sample selection** This bit is only valid when bit 9 is ON 1'b0: Sample CRC Status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC Status and SDIO interrupt by external bus clock falling edge
9	**WDSPLSEL**	W_D_SMPL_SEL	**Data line rising/falling latch fine tune selection in write transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.W_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.W_D0_SMPL Data line 1: MSDC_IOCON.W_D1_SMPL Data line 2: MSDC_IOCON.W_D2_SMPL Data line 3: MSDC_IOCON.W_D3_SMPL
8	**WDSPL**	W_D_SMPL	**CRC Status and SDIO interrupt sample selection** 1'b0: Sample CRC Status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC Status and SDIO interrupt by external bus clock falling edge
5	**RDSPLSEL**	R_D_SMPL_SEL	**Data line rising/falling latch fine tune selection in read transaction** 1'b0: All data line share one value indicated by MSDC_IOCON.R_D_SMPL

Bit(s)	Mnemonic	Name	Description
			1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.R_D0_SMPL Data line 1: MSDC_IOCON.R_D1_SMPL Data line 2: MSDC_IOCON.R_D2_SMPL Data line 3: MSDC_IOCON.R_D3_SMPL Data line 4: MSDC_IOCON.R_D4_SMPL Data line 5: MSDC_IOCON.R_D5_SMPL Data line 6: MSDC_IOCON.R_D6_SMPL Data line 7: MSDC_IOCON.R_D7_SMPL
4	**DDR50CKD**	DDR50_DLY_SEL	**DDR50 output clock delay selection** 1'b0: Use default clock output 1'b1: Delay 1T msdc_src_ck for clock output
3	**DDLSEL**	D_DLYLINE_SEL	**Data line delay line fine tune selection** 1'b0: All data line share one delay selection value indicated by PAD_TUNE.PAD_DAT_RD_RXDLY 1'b1: Each data line has its own delay selection value indicated by Data line 0: DAT_RD_DLY0.DAT0_RD_DLY Data line 1: DAT_RD_DLY0.DAT1_RD_DLY Data line 2: DAT_RD_DLY0.DAT2_RD_DLY Data line 3: DAT_RD_DLY0.DAT3_RD_DLY Data line 4: DAT_RD_DLY1.DAT4_RD_DLY Data line 5: DAT_RD_DLY1.DAT5_RD_DLY Data line 6: DAT_RD_DLY1.DAT6_RD_DLY Data line 7: DAT_RD_DLY1.DAT7_RD_DLY
2	**RDSPL**	R_D_SMPL	**Read data sample selection** 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge

Bit(s)	Mnemonic	Name	Description
1	**RSPL**	R_SMPL	**Command response sample selection** 1'b0: Sample response by external bus clock rising edge 1'b1: Sample response by external bus clock falling edge
0	**SDR104CKS**	SDR104_CLK_SEL	**SDR104 SCLK output clock control** This bit is only used when MSDC_CFG[17:16] CARD_CK_MODE is 2'b01. 1'b0: Bus clock output equals inverted msdc_src_ck 1'b1: Bus clock output equals msdc_src_ck

11240008 MSDC_PS MSDC Pin Status Register 81FF0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SD_WP							CMD	DAT							
Type	RU							RU	RU							
Reset	1							1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDDEBOUNCE														CDSTS	CDEN
Type	RW														RU	RW
Reset	0	0	0	0											1	0

Bit(s)	Mnemonic	Name	Description
31	**SDWP**	SD_WP	**Write Protection Switch status on SD Memory Card** The register bit shows the status of Write Protection Switch on SD Memory Card. There is no default reset value. The pin WP (Write Protection) is only useful while the controller is configured for SD Memory Card 1'b0: Write Protection Switch ON. It means that memory card is desired to be write-protected 1'b1: Write Protection Switch OFF. It means that memory card is writable
24	**CMD**	CMD	**Command line status** This bit reflects the command line value of MSDC bus.

Bit(s)	Mnemonic	Name	Description
23:16	**DAT**	DAT	**Data line status** This bit reflects the data line value of MSDC bus. (8-bits)
15:12	**CDDBCE**	CDDEBOUNCE	**Card detection de-bounce timer** The register field specifies the time interval for card detection de-bounce. Its default value is 0. It means that de-bounce interval is one 32KHz cycle. The interval will extend one cycle time of 32KHz by increasing the counter by 1
1	**CDSTS**	CDSTS	**Card detection status** 1'b0: Card detection pin status is logic low 1'b1: Card detection pin status is logic high
0	**CDEN**	CDEN	**Card detect enable** The register bit is used to control the card detection circuit 1'b0: Card detection is disable 1'b1: Card detection is enable

1124000C MSDC_INT MSDC Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										AUTOCMD53_FAIL	AUTOCMD53_DONE	GEAR_OUT_BOUND	DMA_PROTECT	GPD_CS_ERR	BD_CS_ERR	AUTOCMD19_DONE
Type										W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SD_DATA_CRCERR	SD_DATTO	DMA_XFER_DONE	SD_XFER_COMPLETE	SD_CSTS	SD_RESP_CRCERR	SD_CMDTO	SD_CMDRDY	SD_SDIOIRQ	DMA_Q_EMPTY	SD_AUTOCMD_RESP_CRCERR	SD_AUTOCMD_CMDTO	SD_AUTOCMD_CMDRDY		MSDC_CDSC	MMC_IRQ
Type	W1C	W1C	W1C	W1C	RU	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C		W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
22	**AC53FAIL**	AUTOCMD53_FAIL	**SD Auto command 53 status register**

Bit(s)	Mnemonic	Name	Description
			When auto-command 53 tuning sequence is failure , this register will be set to 1 by H/W.
21	**AC53DONE**	AUTOCMD53_DONE	**SD Auto command 53 status register** When auto-command 53 tuning sequence is finished , this register will be set to 1 by H/W.
20	**GEAROUTBOUND**	GEAR_OUT_BOUND	**the gear setting of delayline is out of boundary during SDIO Autocmd 53 On-Line tuning process**
19	**DMAPROTECT**	DMA_PROTECT	**there is write operation to DMA start address, length, start bit or last buf bit**
18	**GPDCSERR**	GPD_CS_ERR	**GPD checksum error detected**
17	**BDCSERR**	BD_CS_ERR	**BD checksum error detected**
16	**AC19DONE**	AUTOCMD19_DONE	**SD Auto command 19 status register** When auto-command 19 is enabled, H/W will clear this register to 0. As the tuning sequence is finished (32 times), this register will be set to 1 by H/W. S/W should check the AUTOCMD_STS0 and SUTOCMD_STS1 only when this bit is ON.
15	**SDDCRCERR**	SD_DATA_CRCERR	**SD Data CRC error interrupt** Indicates that MS/SD controller detects a CRC error after reading a block of data from the DAT line or SD/MMC signals a CRC error after writing a block of data to the DAT line. 1'b0: Otherwise 1'b1: MS/SD controller detected a CRC error after reading a block of data from the DAT line or SD/MMC signaled a CRC error after writing a block of data to the DAT line
14	**SDDTO**	SD_DATTO	**SD Data timeout interrupt** Indicates that SD/MMC controller detects a timeout condition while waiting for data token on the DAT line. This bit is for both data read and data write. For SD data read, timeout will occur when the read data is not presented. For SD data write, timeout will occur when the write data CRC status is not presented if PATCH_BIT[30] DETECT_WR_CRC_TIMEOUT = 1

Bit(s)	Mnemonic	Name	Description
			1'b0: Otherwise 1'b1: SD/MMC controller detects a timeout condition while waiting for data token on the DAT line
13	**DMAXFDNE**	DMA_XFER_DONE	**DMA transfer done interrupt** The register bit indicates the status of data block transfer. 1'b0: Otherwise 1'b1: A data block was successfully transferred
12	**SDXFCPL**	SD_XFER_COMPLETE	**SD Data transfer complete interrupt** This bit indicates the transaction which contains data has completed. While performing tuning procedure (Execute Tuning is set to 1), SD_XFER_COMPLETE is not set to 1.
11	**SDCSTS**	SD_CSTS	**SD CSTA update interrupt** The register bit indicates any bit in the register SDC_CSTA is active, the register bit will be set to 1. S/W should clear the SDC_CSTA and this bit will be de-asserted automatically. 1'b0: No SD Memory Card interrupt 1'b1: SD Memory Card interrupt exists
10	**SDRCRCER**	SD_RESP_CRCERR	**SD Command CRC error interrupt** Indicates that SD/MMC controller detected a CRC error after reading a response from the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detected a CRC error after reading a response from the CMD line
9	**SDCTO**	SD_CMDTO	**SD Command timeout interrupt** Indicates that SD/MMC controller detected a timeout condition while waiting for a response on the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detected a timeout condition while waiting for a response on the CMD line
8	**SDCRDY**	SD_CMDRDY	**SD Command ready interrupt** For the command without response, the register bit will be 1 once the command completes on SD/MMC bus.

Bit(s)	Mnemonic	Name	Description
			For command with response without busy, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error. For command with response with busy in DAT0, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error and the DAT0 transited from busy to idle. 1'b0: Otherwise 1'b1: Command finish successfully without a CRC error
7	**SDIOIRQ**	SD_SDIOIRQ	**SD SDIO interrupt** This bit indicates the interrupt is sensed in the SDIO bus. 1'b0: No interrupt on SDIO bus 1'b1: Interrupt on SDIO bus
6	**DMAQEPTY**	DMA_Q_EMPTY	**DMA queue empty interrupt** This bit is used to indicate the current DMA queue is empty. Only for Descriptor mode and Enhance mode.
5	**SDACDRCRCER**	SD_AUTOCMD_RESP_CRCERR	**SD auto command CRC error interrupt** This bit is set when detecting a CRC error in the Auto command response.
4	**SDACDCTO**	SD_AUTOCMD_CMDTO	**SD auto command timeout interrupt** This bit is set if no response is returned within a specified cycles(64T in spec) from the end bit of Auto command.
3	**SDACDCRDY**	SD_AUTOCMD_CMDRDY	**SD auto command ready interrupt** This bit is set if auto command is executed without CRC error or time out.
1	**MSDCCDSC**	MSDC_CDSC	**MSDC Card detection status change interrupt** The register bit indicates if any interrupt for memory card insertion/removal exists. Whenever memory card is inserted or removed and card detection circuit is enabled, i.e., the register bit CDEN in the register MSDC_PS is set to 1, the register bit will be set to 1. It will be reset when the register is read. 1'b0: Otherwise 1'b1: Card is inserted or removed

Bit(s)	Mnemonic	Name	Description
0	**MMCIRQ**	MMC_IRQ	**MMC card interrupt** 1'b0: Otherwise 1'b1: indicates that MMC card interrupt event occurs

11240010 MSDC_INTEN MSDC Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										EN_AUTOCMD53_FAIL	EN_AUTOCMD53_DONE	EN_GEAR_OUT_BOUND	EN_DMA_PROTECT	EN_GPD_CS_ERR	EN_BD_CS_ERR	EN_AUTOCMD19_DONE
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SD_DATA_CRCERR	EN_SD_DATTO	EN_SD_DMA_XFER_DONE	EN_SD_XFER_COMPLETE	EN_SD_CSTA	EN_SD_RESP_CRCERR	EN_SD_CMDTO	EN_SD_CMDRDY	EN_SD_SDIOIRQ	EN_DMA_Q_EMPTY	EN_SD_AUTOCMD_RESP_CRCERR	EN_SD_AUTOCMD_CMDTO	EN_AUTOCMD_CMDRDY		EN_MSDC_CDSC	EN_MMC_IRQ
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
22	**ENAC53FAIL**	EN_AUTOCMD53_FAIL	**Auto-command 53 failure interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
21	**ENAC53DONE**	EN_AUTOCMD53_DONE	**Auto-command 53 complete interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt

Bit(s)	Mnemonic	Name	Description
20	**ENGEAROUTBOUND**	EN_GEAR_OUT_BOUND	**Gear out boundary interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
19	**ENDMAPROTECT**	EN_DMA_PROTECT	**DMA protection interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
18	**ENGPDCSERR**	EN_GPD_CS_ERR	**GPD checksum error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
17	**ENBDCSERR**	EN_BD_CS_ERR	**BD checksum error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
16	**ENAC19DONE**	EN_AUTOCMD19_DONE	**Auto-command 19 complete interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
15	**ENSDDCRCERR**	EN_SD_DATA_CRCERR	**SD Data CRC error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
14	**ENSDDTO**	EN_SD_DATTO	**SD Data timeout interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
13	**ENDMAXFDNE**	EN_SD_DMA_XFER_DONE	**DMA transfer done interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
12	**ENSDXFCPL**	EN_SD_XFER_COMPLETE	**SD Data transfer complete interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt

Bit(s)	Mnemonic	Name	Description
11	**ENSDCSTA**	EN_SD_CSTA	**SD CSTA update interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
10	**ENSDRCRCER**	EN_SD_RESP_CRCERR	**SD Command CRC error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
9	**ENSDCTO**	EN_SD_CMDTO	**SD Command timeout interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
8	**ENSDCRDY**	EN_SD_CMDRDY	**SD Command ready interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
7	**ENSDIOIRQ**	EN_SD_SDIOIRQ	**SD SDIO interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
6	**ENDMAQEPTY**	EN_DMA_Q_EMPTY	**DMA queue empty interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
5	**ENSDACDRCRCER**	EN_SD_AUTOCMD_RESP_CRCERR	**SD auto command CRC error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
4	**ENSDACDCTO**	EN_SD_AUTOCMD_CMDTO	**SD auto command timeout interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
3	**ENSDACDCRDY**	EN_AUTOCMD_CMDRDY	**SD auto command ready interrupt enable** 1'b0: Disable interrupt

Bit(s)	Mnemonic	Name	Description
			1'b1: Enable interrupt
1	**ENMSDCCDSC**	EN_MSDC_CDSC	**MSDC Card detection status change interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
0	**ENMMCIRQ**	EN_MMC_IRQ	**MMC card interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt

11240014 MSDC_FIFOCS MSDC FIFO Control and Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFOCLR								TXFIFOCNT							
Type	A0								RU							
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXFIFOCNT							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**FIFOCLR**	FIFOCLR	**Embedded FIFO clear** Write this bit to 1 makes FIFO cleared. It will goes to 0 when FIFO is cleared. S/W needs to check this bit to make sure clearing FIFO sequence is done. This bit can be used when the data read/write sequence has error and need to clean the H/W FIFO.
23:16	**TXFIFOCNT**	TXFIFOCNT	**TX FIFO count for MSDC write** 8'd0: No data in FIFO 8'd1: 1bytes data in FIFO 8'd2: 2 bytes data in FIFO

Bit(s)	Mnemonic	Name	Description
			8'd131: Maximum 131 bytes data in FIFO Others: reserved
7:0	**RXFIFOCNT**	RXFIFOCNT	**RX FIFO count for MSDC read** 8'd0: No data in FIFO 8'd1: 1bytes data in FIFO 8'd2: 2 bytes data in FIFO 8'd131: Maximum 131 bytes data in FIFO Others: reserved

11240018 MSDC_TXDATA MSDC TX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_TXDATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_TXDATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIOTXDATA**	PIO_TXDATA	**PIO mode TXDATA port** This register can be accessed by Byte or Half-word or Word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

1124001C MSDC_RXDATA MSDC RX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_RXDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_RXDATA															

Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIORXDATA**	PIO_RXDATA	**PIO mode RXDATA port** This register can be accessed by Byte or Half-word or Word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

11240030 SDC_CFG SD Configuration Register 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DTOC										INT_AT_BLOCK_GAP	SDIO_INT_DET_EN	SDIO		BUSWIDTH	
Type	RW										RW	RW	RW		RW	
Reset	0	0	0	0	0	0	0	0			0	1	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		WRDTOC													WAKEUP_INS_EN	WAKEUP_SDIOINT_EN
Type		RW													RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DTOC**	DTOC	**Data Timeout Counter** The period from the end of the initial host read command or the last read data block in a multiple block read operation to the start bit of the next read data block requires at least two serial clock cycles. The counter is used to extend the period (Read Data Access Time) in unit of 1048576 serial clocks. 8'b00000000: Extend 1048576 more serial clock cycle 8'b00000001: Extend 1048576x2 more serial clock cycle 8'b00000010: Extend 1048576x3 more serial clock cycle 8'b11111111: Extend 1048576x 256 more serial clock cycle
21	**INTBGP**	INT_AT_BLOCK_GAP	**Interrupt at block Gap**

Bit(s)	Mnemonic	Name	Description
			This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. Setting to 0 disables interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the Host Driver detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. 1'b0: Disables interrupt detection at the block gap 1'b1: Enables interrupt detection at the block gap
20	**SDIOIDE**	SDIO_INT_DET_EN	**SDIO interrupt detection enable** This bit is to inform the SD controller to sense the SDIO interrupt 1'b0: SDIO interrupt detection is disabled 1'b1: SDIO interrupt detection is enabled if the SDIO bit is also on
19	**SDIO**	SDIO	**SDIO mode enable bit** This bit is to enable the support to sense the SDIO interrupt and disable the R4 response CRC check for SDIO card 1'b0: SDIO mode is disabled 1'b1: SDIO mode is enabled
17:16	**BUSWD**	BUSWIDTH	**Bus width configuration** This field is used to define the SD/MMC bus width 2'b00: 1 bit mode 2'b01: 4 bit mode 2'b10: 8 bit mode 2'b11: reserved
14:2	**WRDTOC**	WRDTOC	**Data Timeout Counter** Timeout counter for programming.The counter is used to extend the period (Write Data Access Time) in unit of 1048576 serial clocks. 13'b0000000000000: Extend 1048576 more serial clock cycle

Bit(s)	Mnemonic	Name	Description
			13'b0000000000001: Extend 1048576x2 more serial clock cycle 13'b0000000000010: Extend 1048576x3 more serial clock cycle 13'b1111111111111: Extend 1048576x 8192 more serial clock cycle
1	**ENWKUPINS**	WAKEUP_INS_EN	**Card status change wakeup event enable bit** 1'b0: Disable wakeup event for card status change 1'b1: Enable wakeup event for card status change
0	**ENWKUPSDIOINT**	WAKEUP_SDIOINT_EN	**SDIO card interrupt wakeup event enable bit** 1'b0: Disable wakeup event for SDIO card interrupt 1'b1: Enable wakeup event for SDIO card interrupt

11240034 SDC_CMD SD Command Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**AUTO_CMD53**	**VOL_SWTH**	**AUTO_CMD**		**LEN**											
Type	RW	RW	RW		RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GO_IRQ**	**STOP**	**RW**	**DTYPE**			**RSPTYP**			**BREAK**	**CMD**					
Type	RW	RW	RW	RW			RW			RW	RW					
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**ACMD53**	AUTO_CMD53	**Auto command 53 enable** This field should use exclusively with AUTO_CMD field. means that AUTO_CMD != 2'b00, this field should assign to 1'b0, if this filed is assigned to 1'b1, AUTO_CMD should set to 2'b00 1'b0: Disable Auto Command 53

Bit(s)	Mnemonic	Name	Description
			1'b1: Enable Auto Command 53
30	**VOLSWTH**	VOL_SWTH	**Voltage switch command** 1'b0: Disable voltage switch detection 1'b1: Enable voltage switch detection
29:28	**ACMD**	AUTO_CMD	**Auto command enable** This field determines use of auto command functions. This function can be used in all modes including PIO/Basic DMA/Descriptor DMA/Enhanced Mode. There are two methods to stop Multiple-block read and write operation. (1) Auto CMD12 Enable Multiple-block read and write commands for memory require CMD12 to stop the operation. When ACMD-12 is used, MSDC issues CMD12 automatically when last block transfer is completed. Auto CMD12 error is indicated to the MSDC_INT register. The Host Driver shall not set this bit if the command does not require CMD12. In particular, secure commands defined in the Part 3 File Security specification do not require CMD12. (2) Auto CMD23 Enable When ACMD-23 is used, MSDC issues a CMD23 automatically before issuing a command specified in the CMD field. The Host Controller Version 3.00 and later shall support this function. By writing the Command register, MSDC issues a CMD23 first and then issues a command specified by the CMD field in SDC_CMD register. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in the MSDC_INT register. 32-bit block count value for CMD23 is set to SDC_BLOCK_NUM register. 2'b00: Disable Auto Command 2'b01: Enable Auto CMD12 2'b10: Enable Auto CMD23 2'b11: Enable Re-tuning CMD19
27:16	**LEN**	LEN	**Length** The register field is used to define the length of one block in unit of byte in a data transaction of block mode or the data

Bit(s)	Mnemonic	Name	Description
			length in unit of byte in data transaction of byte mode. The maximal value of block length is 2048 bytes. 12'b000000000000: Reserved 12'b000000000001: Block length is 1 byte 12'b000000000010: Block length is 2 byte 12'b011111111111: Block length is 2047 byte 12'b100000000000: Block length is 2048 byte
15	**GOIRQ**	GO_IRQ	**GO_IRQ command** The register bit indicates if the command is GO_IRQ_STATE (CMD40) and used only for MMC protocol. If the command is GO_IRQ_STATE, the period between command token and response token will not be limited. 1'b0: The command is not GO_IRQ_STATE 1'b1: The command is GO_IRQ_STATE
14	**STOP**	STOP	**Stop command** The register bit indicates if the command is a stop transmission command. It should be set to 1 when CMD12 (SD/MMC) or CMD52 with I/O abort (SDIO) is to be issued. 1'b0: The command is not a stop transmission command 1'b1: The command is a stop transmission command
13	**RW**	RW	**Command read write selection** The register bit defines the command is a read command or write command. The register bit is valid only when the command will cause a transaction with data token. 1'b0: The command is a read command 1'b1: The command is a write command
12:11	**DTYPE**	DTYPE	**Data block selection** The register field defines data token type for the command. 2'b00: No data token for the command 2'b01: Single block transaction (only available in block mode) 2'b10: Multiple block transaction. (only available in block mode)

Bit(s)	Mnemonic	Name	Description
			2'b11: Stream operation. It only shall be used in MMC protocol. (only available in block mode)
9:7	**RSPTYP**	RSPTYP	**Command response type** 3'b000: This command has no response. 3'b001: The command has R1/R5/R6/R7 response. The response token is 48-bit with CRC check (For SD/MMC/SDIO) (Not include the SDIO abort command) 3'b010: The command has R2 response. The response token is 136-bit (For SD/MMC) 3'b011: The command has R3 response. The response token is 48-bit response, no CRC check (For SD/MMC) 3'b100: The command has R4 response. The response token is 48-bit without CRC check (For SDIO) The response token is 48-bit with CRC check (For MMC) 3'b111: The command has R1b response. The response token is 48-bit (For SD/MMC/SDIO)
6	**BREAK**	BREAK	**Abort a pending MMC GO_IRQ command** It is only valid for a pending GO_IRQ_MODE command waiting for MMC interrupt response. 1'b0: Not a beak command 1'b1: Break a pending MMC GO_IRQ_MODE command in the controller.
5:0	**CMD**	CMD	**SD Memory Card command**

11240038 SDC_ARG SD Argument Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ARG**	ARG	**Memory card controller argument register**

1124003C SDC_STS SD Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMC_STREAM_WR_COMPL											CMD_TIMEOUT_TYPE		DATA_TIMEOUT_TYPE		CMD_WR_BUSY
Type	RU											RU		RU		W1C
Reset	0											0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														START_BIT_CRCERR	CMDBUSY	SDCBUSY
Type														RU	RU	RU
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
31	**MMCSWRCPL**	MMC_STREAM_WR_COMPL	**MMC Stream mode write data is all flushed to MMC card** S/W can use this bit to confirm last write data are flushed to MMC then issue STOP command. This bit is only valid when the command SDC_CMD.DTYPE=2'b11. 1'b0: Last Data are partially inside MSDC 1'b1: Last data are flushed to MMC card
20:19	**CTTYPE**	CMD_TIMEOUT_TYPE	**MSDC cmd timeout type,For debug host misses r1b cmd response start bit or data0 busy too long** 2'b01:data0 busy timeout 2'b10:response start bit timeout
18:17		DATA_TIMEOUT_TYPE	**Data Timeout Error Type,For Debug and Err Handle** 2'b00: Read Data Timeout 2'b01: Write CRC Stauts Timeout

Bit(s)	Mnemonic	Name	Description
			2'b10: Write Programming Timeout
16		CMD_WR_BUSY	
2	**STBCRCERR**	START_BIT_CRCERR	**Status to reflect whether host misses start bit or not** 1'b0: start bit check pass 1'b1: start bit missing error
1	**CMDBSY**	CMDBUSY	**SD Command line busy status** S/W should always read this bit to make sure the command line is not busy before sending the next command. If the command is R1B or data read/write command, S/W should check SDCBUSY bit too. Note: When Auto command 12 is enabled, this bit will be asserted immediately after SDC_CMD is written and de-asserted after auto-command 12 finishes. 1'b0: No transmission is going on CMD line on SD bus 1'b1: There exists transmission going on CMD line on SD bus
0	**SDCBSY**	SDCBUSY	**SD controller busy status** 1'b0: SD controller is idle 1'b1: SD controller is busy

11240040 SDC_RESP0 SD Response Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP0**	RESP0	**Memory card controller response register 0**

Bit(s)	Mnemonic	Name	Description

11240044 SDC_RESP1 SD Response Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP1**	RESP1	**Memory card controller response register 1**

11240048 SDC_RESP2 SD Response Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP2**	RESP2	**Memory card controller response register 2**

1124004C SDC_RESP3 SD Response Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP3**	RESP3	**Memory card controller response register 3**

11240050 SDC_BLK_NUM SD Block Number Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BLOCK_NUMBER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLOCK_NUMBER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0	**BLKNUM**	BLOCK_NUMBER	**Memory card controller Block number** This field indicates the block number of data transaction. 32'd0: Reserved 32'd1: 1 data block 32'd2: 2 data block 32'd3: 3 data block 32'hffffffff: 4GB-1 data block

11240054 SDC_VOL_CHG SD Voltage Change Wait Time Register 00000145

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VOL_CHG_WAIT_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1

Bit(s)	Mnemonic	Name	Description
15:0	**VCHGCNT**	VOL_CHG_WAIT_CNT	**This register define SD voltage change check wait time,wait time is clock frequency multiply VOL_WAIT_TIME**

11240058 SDC_CSTS SD Card Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS**	CSTS	**CSTS** The card status field in the response R1 or R1b field. Each bit can be write 1 clear individually.

1124005C SDC_CSTS_EN SD Card Status Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS_EN**	CSTS_EN	**CSTS_EN** This register is used to control which bit of the CSTA will generate the MSDC_INT.SDCSTA

11240060 SDC_DATCRC_STS SD Card Data CRC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DAT_CRCSTS_NEG**								**DAT_CRCSTS_POS**							
Type	RU								RU							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8	**DCSSN**	DAT_CRCSTS_NEG	**MSDC DDR mode negative edge Read DATA CRC status** This register reflects the CRC status of data line[7:0] in DDR mode. The positive edge CRC status is shown in DAT_CRC_STS[7:0]. This register is only for MSDC Read. 1'b0: No CRC error 1'b1: CRC error
7:0	**DCSSP**	DAT_CRCSTS_POS	**MSDC read DATA CRC status** This register reflects the CRC status of data line[7:0]. This register is only for MSDC Read. 1'b0: No CRC error 1'b1: CRC error

11240064 SDC_ADV_CFG0 SDC Advance Configuration 0 0008E000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name												SDC_RX_ENHANCE_EN	SDIO_IRQ_ENHANCE_EN			
Type												RW	RW			
Reset												0	1			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMD_INDEX_CHECK	CMD_ENDBIT_CHECK	CMD_RESP_ENDBIT	CMD_RESP_INDEX						CMD_RESP_CRC						
Type	RW	RW	RU	RU						RU						
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20		SDC_RX_ENHANCE_EN	**enhance rx ehance check en for TA remove and gap IRQ check** 1'b0: normal rx path 1'b1: enhance rx path
19		SDIO_IRQ_ENHANCE_EN	**enhance sdio irq check en** 1'b0: normal sdio irq check 1'b1: enhance sdio irq check
15		CMD_INDEX_CHECK	**Decide hardware check cmd_index in response or not** 1'b0: Software check index 1'b1: Hardware check index
14		CMD_ENDBIT_CHECK	**Decide hardware check end_bit in response or not** 1'b0: Software check endbit 1'b1: Hardware check endbit
13		CMD_RESP_ENDBIT	**CMD endbit in the cmd response**
12:7		CMD_RESP_INDEX	**CMD index in the cmd response**
6:0		CMD_RESP_CRC	**CMD crc in the cmd response**

11240070 EMMC_CFG0 EMMC Configuration Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BOOT_SUPPORT	BOOT_WAIT_DELAY											BOOT_ACK_CHK_DIS	BOOT_MODE	BOOT_STOP	BOOT_START
Type	RW	RW											RW	RW	WO	WO
Reset	0	0	0	0									0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**BTSUP**	BOOT_SUPPORT	**eMMC boot up support** The register bit indicates that boot mode is supported or not 1'b0: Not Support 1'b1: Support
14:12	**BTWDLY**	BOOT_WAIT_DELAY	**eMMC wait delay time** The register bit set the delay time to wait MMC device to exit boot up mode after boot stop bit is set. 3'b000: 0x1024 clock cycles 3'b001: 1x1024 clock cycles 3'b010: 2x1024 clock cycles 3'b111: 7x1024 clock cycles
3	**BTACHKDIS**	BOOT_ACK_CHK_DIS	**eMMC boot up mode ACK check Disable** 1'b0: Do ACK pattern check 1'b1: Bypass ACK pattern check
2	**BTMOD**	BOOT_MODE	**eMMC boot up mode** There are two kinds of boot up mode supported by eMMC 4.4. Reset CMD mode is option for eMMC 4.3. 1'b0: Pull low CMD mode 1'b1: Reset CMD mode
1	**BTSTOP**	BOOT_STOP	**eMMC boot up mode stop** The register bit is indicated that boot stop signal, read always return 0.

Bit(s)	Mnemonic	Name	Description
0	**BTSTART**	BOOT_START	**eMMC boot up start signal trigger** The register bit is boot up start signal trigger. read always return 0.

11240074 EMMC_CFG1 EMMC Configuration Register 1 00200003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BOOT_ACK_TOC												BOOT_DAT_TOC			
Type	RW												RW			
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BOOT_DAT_TOC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:20	**BTATOC**	BOOT_ACK_TOC	**eMMC ack pattern time out counter** in unit of 2^16 serial clock. SW could not set it to 12'hFFF.
19:0	**BTDTOC**	BOOT_DAT_TOC	**eMMC read boot data time out counter** in unit of 2^16 serial clock. SW could not set it to 20'hFFFFF.

11240078 EMMC_STS EMMC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BOOT_DAT_RECV	BOOT_ACK_RECV	BOOT_UP_STATE	BOOT_ACK_TO	BOOT_DAT_TO	BOOT_ACK_ERR	BOOT_CRC_ERR
Type										RU	W1C	RU	W1C	W1C	W1C	W1C
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6	**BTDRCV**	BOOT_DAT_RECV	**eMMC boot data is received** This register is for S/W to check 1st 4-byte boot data is received or not. For other data after 1st 4B data, this bit should not be referenced. S/W should check RXFIFOCNT instead. 1'b0: There's no data in RXFIFO 1'b1: 1st 4B data is in RXFIFO
5	**BTARCV**	BOOT_ACK_RECV	**eMMC ack is received** Also need to check BOOT_ACK_ERR to determine pass or fail 1'b0: No ACK pattern is received 1'b1: ACK pattern has been received
4	**BTSTS**	BOOT_UP_STATE	**eMMC boot up mode status** The register bit indicates if MMC device operating in boot up mode state. 1'b0: Not in Boot up state 1'b1: Boot up state is on-going
3	**BTATO**	BOOT_ACK_TO	**eMMC ack timeout** The register bit indicates the controller detect a time out condition while waiting for an ack pattern on DAT0. 1'b0: No ACK pattern timeout error 1'b1: ACK pattern timeout error
2	**BTDTO**	BOOT_DAT_TO	**eMMC data timeout** The register bit indicates the controller detect a time out condition while waiting for boot data. 1'b0: No Data timeout error 1'b1: Data timeout error
1	**BTAERR**	BOOT_ACK_ERR	**eMMC ack error** The register bit indicates the status of ack pattern checking result. The bit is setting to 1 when ack pattern error. 1'b0: No ACK pattern check error 1'b1: ACK pattern check error

Bit(s)	Mnemonic	Name	Description
0	**BTDERR**	BOOT_CRC_ERR	**eMMC CRC error** The register bit indicates the CRC status of boot data. The bit is setting to 1 when data CRC error. 1'b0: No Data CRC error 1'b1: Data CRC error

1124007C EMMC_IOCON EMMC IO Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**BOOT_RST**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**BTRST**	BOOT_RST	**eMMC device boot up mode reset** The register bit is to trigger HW reset to set eMMC device entering into pre-idle state. 1'b0: de-assert RST_n to eMMC card 1'b1: Assert RST_n to eMMC card

11240080 SD_ACMD_RESP SD ACMD Response Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**AUTOCMD_RESP**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUTOCMD_RESP**															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ACMDRESP**	AUTOCMD_RESP	**SD Auto command response register** This register stores the response[39:8] of ACMD12/ACMD23/ACMD19.

11240084 SD_ACMD19_TRG SD ACMD19 Target Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**FINE_TUNE_SEL**			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**ACMDFTSEL**	FINE_TUNE_SEL	**SD Auto command 19 test target selection** After auto-command 19 is triggered, MSDC will only change the phase of the selected one and keep the value of other tuning registers. S/W can get the result from AUTOCMD_STS. There are total 32 phases for each delay line. 4'd0: Select PAD_CLK_TXDLY[5:0] as the target to run auto-command19. 4'd1: Select PAD_CMD_RXDLY[5:0] as the target to run auto-command19. 4'd2: Select PAD_DAT_RD_RXDLY[5:0] as the target to run auto-command19. 4'd3: Select PAD_DAT_WR_RXDLY[5:0] as the target to run auto-command19. 4'd4: Select DAT0_RD_DLY[5:0] as the target to run auto-command19. 4'd5: Select DAT1_RD_DLY[5:0] as the target to run auto-command19.

Bit(s)	Mnemonic	Name	Description
			4'd6: Select DAT2_RD_DLY[5:0] as the target to run auto-command19. 4'd7: Select DAT3_RD_DLY[5:0] as the target to run auto-command19. 4'd8: Select DAT4_RD_DLY[5:0] as the target to run auto-command19. 4'd9: Select DAT5_RD_DLY[5:0] as the target to run auto-command19. 4'd10: Select DAT6_RD_DLY[5:0] as the target to run auto-command19. 4'd11: Select DAT7_RD_DLY[5:0] as the target to run auto-command19. 4'd12: Select CMD_RESP_RXDLY[5:0] as the target to run auto-command19. Others: Reserved

11240088 SD_ACMD19_STS SD ACMD19 Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUTOCMD19_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCMD19_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ACMD19STS**	AUTOCMD19_STS	**SD Auto command 19 test result register** When auto-command 19 is enabled, H/W will automatically try 32 times of command-19 and store the result into this register. This register contains 1st to 32th results in bit[0:31]

1124008C DMA_SA_HIGH4BIT DMA Current Address Resgiter of high 4bit 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_SURR_ADDR_HIGH4BIT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DMASAHIGH4BIT**	DMA_SURR_ADDR_HIGH4 BIT	**it is usend to set high 4bit address of start address because 64G dram need 36bit address**

11240090 DMA_SA DMA Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMASA**	DMA_STR_ADDR	**The start address of the DMA address** This register is used to set the start address of the DMA. In DMA basic mode, this field indicates the source or destination address of the data transfer which depends on the command. In descriptor base DMA, this is the descriptor chain start address.

11240094 DMA_CA DMA Current Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_CURR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_CURR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMACA**	DMA_CURR_ADDR	**The current address of the DMA address** This register is used to read the current address of the DMA descriptor chain.

11240098 DMA_CTRL DMA Control Register 00006008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BURST_SIZE			DMA_SPLIT_1K	LAST_BUF	DMA_ALIGN	DMA_MODE					AHB_READYM	DMA_RESUME	DMA_STOP	DMA_START
Type		RW			RW	RW	RW	RW					RO	WO	A0	WO
Reset		1	1	0	0	0	0	0					1	0	0	0

Bit(s)	Mnemonic	Name	Description
14:12	**BSTSZ**	BURST_SIZE	**DMA burst size** This field is used to specify the maximum transfer bytes allowed at the device per DMA burst. This field can not be modified when the DMA status is 1. 3'd3: 8 Bytes 3'd4: 16 Bytes 3'd5: 32 Bytes 3'd6: 64 Bytes Other: Reserved
11	**SPLIT1K**	DMA_SPLIT_1K	**This field is used to specify whether split burst when corss 1K boundry address**

Bit(s)	Mnemonic	Name	Description
			1'b0:1K boundary not split 1'b1:1K boundary split
10	**LASTBF**	LAST_BUF	**Last buffer of the basic DMA mode** This field indicates the last buffer in the basic DMA mode
9	**DMAALIGN**	DMA_ALIGN	**This field is used to specify whether address aligment burst size** 1'b0:do not DAM burst size alignment 1'b1:DAM burst size alignment
8	**DMAMOD**	DMA_MODE	**DMA operation mode** This field indicates operation mode of DMA 1'b0: Basic DMA mode 1'b1: Descriptor base DMA mode
3	**READYM**	AHB_READYM	**only for debug when dma hang,sw can check if ahb bus is ok when gdma is hang** 1:bus is normal 0:bus not normal
2	**DMARSM**	DMA_RESUME	**DMA resume control register** This bit is used to resume the DMA transaction. Read always return 0
1	**DMASTOP**	DMA_STOP	**DMA Stop control register** This bit is used to stop the DMA transaction. When SW issue STOP command, SW must wait this bit de-assert or DMA inactive to guarantee stop done.
0	**DMASTART**	DMA_START	**DMA start control register** This bit is used to start the DMA transaction. Read always return 0

1124009C DMA_CFG DMA Configuration Register 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															OUT_BOUND_	DMA_CHK_S

															STOP_DMA	UM_12B
Type															RW	RW
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MSDC_ACTIVE_EN				AHB_HPROT_2_EN							LOCK_DISABLE	DMA_DSCP_CS_EN	DMA_STATUS
Type			RW				RW							RW	RW	RU
Reset			0	0			0	0						1	0	0

Bit(s)	Mnemonic	Name	Description
17	**OUTBOUNDSTOPDMA**	OUT_BOUND_STOP_DMA	**This register will determine whether stop Enhance DMA if gear setting is out-of-boundary during send training data** 1'b0: Enhance DMA will continue even if gear setting is out-of-boundary during send training data 1'b1: Enhance DMA will stop if gear setting is out-of boundary during send training data
16	**DMACHKSUM12B**	DMA_CHK_SUM_12B	**This register indicates GPD/BD checksum cover 16byte or 12byte** 1'b0: GPD/BD checksum cover 16byte 1'b1: GPD/BD checksum only cover 12byte
13:12	**MSDCACTIVEEN**	MSDC_ACTIVE_EN	**This register will indicate how to control msdc_active** 2'b00: dynamic control msdc_active 2'b01: msdc_active = 0 2'b10: msdc_active = 1 2'b11: Reserved
9:8	**AHBHPROT2EN**	AHB_HPROT_2_EN	**This register will determine how to control hprot_2 pin of AHB bus** AHB_HPROT_2_EN = 2'b00, and Basic DMA Mode All the write transfers of a burst will access by bufferable mode except the last burst of DMA AHB_HPROT2_2_EN=2'b00, and Descriptor DMA Mode all the write transfers of a burst will access by bufferable mode except HW own update transfer 2'b00: dynamic control hprot_2

Bit(s)	Mnemonic	Name	Description
			2'b01: hprot_2 = 0 2'b10: hprot_2 = 1
2	**LOCKDISABLE**	LOCK_DISABLE	**should disable lock in order to improve emi efficient** 1'b0:enable ahb lock 1'b1:disable ahb lock
1	**DSCPCSEN**	DMA_DSCP_CS_EN	**DMA descriptor checksum enable** This bit is used to enable or disable the descriptor checksum validation function for the descriptor. This field can not be modified when the DMA status is 1.
0	**DMASTS**	DMA_STATUS	**DMA status** This bit is used to indicate the status of the DMA. 1'b0: DMA engine is inactive 1'b1: DMA engine is active

112400A0 SW_DBG_SEL MSDC S/W Debug Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DBG_SEL**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**SWDBGSEL**	DBG_SEL	**MSDC debug selection** This contain is reserved!

112400A4 SW_DBG_OUT MSDC S/W Debug Output Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SWDBGO**	DBG_OUT	**MSDC debug output** 32 bit output selected by SW_DBG_SEL register

112400A8 DMA_LENGTH DMA Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**XFSZ**	XFER_SIZE	**DMA total transfer size** This field is used to specify the number of DMA transfer byte required for the movement of source data through DMA. This field is only valid in basic DMA mode.

112400B0 PATCH_BIT0 MSDC Patch Bit Register 0 403C0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_MMC_DRV_RESP	DETECT_WR_CRC_TIMEOUT	SPC_ALWAYS_PUSH	SDIO_INT_DLY_SEL	SDC_CMD_CMDFAIL_SEL	SDC_CMD_IDRT_SEL	SDC_CFG_WDOD				SDC_CFG_BSYDLY				SDIO_CFG_INTC_SEL	MSDC_BLKNUM_SEL
Type	RW	RW	RW	RW	RW	RW	RW				RW				RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC_FIFO_RD_DIS	CKGEN_MSDC_DLY_SEL					INT_DAT_LATCH_CK_SEL			DESC_UP_SEL	ACMD53_FAIL_ONE_SHOT	MASK_ACMD53_CRC_ERR_INTR	RD_DAT_SEL	DIS_REFLECT_CMDWR_WHEN_BSY	EN_SDC_ODD_8BIT_SUP	EN_START_BIT_CHK_SUP
Type	RW	RW					RW			RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**PTCH31**	EN_MMC_DRV_RESP	**Enable MSDC always drives bus when output wakeup response (BREAK)** 1'b0: Disable 1'b1: Enable
30	**PTCH30**	DETECT_WR_CRC_TIMEOUT	**MSDC write data CRC phase timeout detection** 1'b0: Not detect CRC phase timeout 1'b1: detect CRC phase timeout
29	**PTCH29**	SPC_ALWAYS_PUSH	**SPC Buffer push mechanism** 1'b0: Push the buffer only when read transfer is on-going 1'b1: Always push the buffer
28	**PTCH28**	SDIO_INT_DLY_SEL	**SDIO interrupt latch time selection** 1'b0: Latch the data line value in internal SDIO interrupt period 1'b1: Latch the data line value in 1 clock delay of internal SDIO interrupt period
27	**PTCH27**	SDC_CMD_CMDFAIL_SEL	**SDIO interrupt period recovery selection** 1'b0: SDIO interrupt period will re-start after a CMD12 or CMD52 command is issued 1'b1: SDIO interrupt period whenever DAT line is not busy
26	**PTCH26**	SDC_CMD_IDRT_SEL	**SD identification response time selection** The register bit indicates if the command has a response with NID (that is, 5 serial clock cycles as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 1.0) response time. The register bit is valid only when the command has a response token. Thus

Bit(s)	Mnemonic	Name	Description
			the register bit must be set to 1 for CMD2 (ALL_SEND_CID) and ACMD41 (SD_APP_OP_CMD). 1'b0: Otherwise. 1'b1: The command has a response with NID response time.
25:22	**PTCH22**	SDC_CFG_WDOD	**SD Write Data Output Delay** The period from finish of the response for the initial host write command or the last write data block in a multiple block write operation to the start bit of the next write data block requires at least two serial clock cycles. The register field is used to extend the period (Write Data Output Delay) in unit of one serial clock. 4'b0000: No extend. 4'b0001: Extend one more serial clock cycle. 4'b0010: Extend two more serial clock cycles. 4'b1111: Extend fifteen more serial clock cycle.
21:18	**PTCH18**	SDC_CFG_BSYDLY	**SD R1B busy detection mode** The register field is only valid for the commands with R1b response. If the command has a response of R1b type, MS/SD controller must monitor the data line 0 for card busy status from the bit time that is two serial clock cycles after the command end bit to check if operations in SD/MMC Memory Card have finished. The register field is used to expand the time between the command end bit and end of detection period to detect card busy status. If time is up and there is no card busy status on data line 0, then the controller will abandon the detection. 4'b0000: No extend. 4'b0001: Extend one more serial clock cycle. 4'b0010: Extend two more serial clock cycles. 4'b1111: Extend fifteen more serial clock cycle.
17	**PTCH17**	SDIO_CFG_INTC_SEL	**SDIO Interrupt model selection** 1'b0: Only when data line [1] = 0 and then trigger SDIO interurpt event 1'b1: Only when data line [3:0] = 4'b1101 and then trigger SDIO interurpt event

Bit(s)	Mnemonic	Name	Description
16	**PTCH16**	MSDC_BLKNUM_SEL	**Configuration support ACMD23 reliable/force prog etc. feature** 1'b0: Support ACMD23 reliable/force prog etc. feature 1'b1:Don't support ACMD23 reliable/force prog etc. feature
15	**PTCH15**	MSDC_FIFO_RD_DIS	**MSDC RXFIFO Read Disable** 1'b0: Disable FIFO read permission to RXFIFO in PIO mode 1'b1: Enable FIFO read permission to RXFIFO in PIO mode
14:10	**CKGDLYS**	CKGEN_MSDC_DLY_SEL	**CKBUF in CKGEN Delay Selection** Total 32 stages
9:7	**INTCKS**	INT_DAT_LATCH_CK_SEL	**Internal MSDC clock phase selection** Total 8 stages, each stage can delay 1 clock period of msdc_src_ck
6	**DESCUP**	DESC_UP_SEL	**sd transfer done int should be issue when GPD have been update** 1'b1:enable new function for generate sd transfer done int 1'b0:use old function for generate sd transfer done int
5	**PTCH5**	ACMD53_FAIL_ONE_SHOT	**determine interrupt method of AUTOCMD53_FAIL** 1'b0: AUTOCMD53_FAIL interrupt will assert whenever CMD/DAT crc error occur 1'b1: AUTOCMD53_FAIL interrupt will assert only when AUTOCMD53_DONE assert if there is CMD/DAT crc error
4	**PTCH4**	MASK_ACMD53_CRC_ERR_INTR	**mask CMD/DAT crc error interrupt during execute AUTOCMD53 training sequence** 1'b0: enable CMD/DAT crc error interrupt during execute AUTOCMD53 training sequence 1'b1: mask CMD/DAT crc error interrupt during execute AUTOCMD53 training sequence
3	**PTCH3**	RD_DAT_SEL	**This field is used to define whther used rising or falling buf data for SDR mode** 1'b0: Used rising buf data for SDR mode 1'b1: Used falling buf data for SDR mode
2	**PTCH02**	DIS_REFLECT_CMDWR_WHEN_BSY	**Enable SD command register write montior**

Bit(s)	Mnemonic	Name	Description
			1'b0: Enable monitor function
			1'b1: Disable monitor function
1	**PTCH01**	EN_SDC_ODD_8BIT_SUP	**Enable SD odd number support for 8-bit data bus**
			1'b0: Disable
			1'b1: Enable
0	**PTCH00**	EN_START_BIT_CHK_SUP	**Enable SD start bit check function**
			1'b0: Disable
			1'b1: Enable

112400B4 PATCH_BIT1 MSDC Patch Bit Register 1 FFA04309

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSDC_CK_SHBFF_CKEN	MSDC_CK_RCTL_CKEN	MSDC_CK_WCTL_CKEN	MSDC_CK_SD_CKEN	MSDC_CK_ACMD_CKEN	MSDC_CK_VOLDET_CKEN	MSDC_CK_PSC_CKEN	MSDC_CK_SPC_CKEN	AHB_CK_GDMA_CKEN		DCM_EN					ENABLE_SINGLE_BURST
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW					RW
Reset	1	1	1	1	1	1	1	1	1		1					0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESET_GDMA	DDR_CMD_FIX_SEL	BIAS_EXTBIAS_28NM	BIAS_EN18IO_28NM	STOP_DLY_SEL				BUSY_CHECK_SEL	GET_BUSY_MARGIN	CMD_RSP_TA_CNTR			WRDAT_CRCS_TA_CNTR		
Type	RW	RW	RW	RW	RW				RW	RW	RW			RW		
Reset	0	1	0	0	0	0	1	1	0	0	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
31	**MSHBFCKEN**	MSDC_CK_SHBFF_CKEN	**msdc_src_ck clock enable bit for SHBFF**
			1'b0: Disable
			1'b1: Enable

Bit(s)	Mnemonic	Name	Description
30	**MRCTLCKEN**	MSDC_CK_RCTL_CKEN	**msdc_src_ck clock enable bit for RCTL** 1'b0: Disable 1'b1: Enable
29	**MWCTLCKEN**	MSDC_CK_WCTL_CKEN	**msdc_src_ck clock enable bit for WCTL** 1'b0: Disable 1'b1: Enable
28	**MSDCKEN**	MSDC_CK_SD_CKEN	**msdc_src_ck clock enable bit for SD** 1'b0: Disable 1'b1: Enable
27	**MACMDCKEN**	MSDC_CK_ACMD_CKEN	**msdc_src_ck clock enable bit for ACMD** 1'b0: Disable 1'b1: Enable
26	**MVOLDTCKEN**	MSDC_CK_VOLDET_CKEN	**msdc_src_ck clock enable bit for VOLDET** 1'b0: Disable 1'b1: Enable
25	**MPSCCKEN**	MSDC_CK_PSC_CKEN	**msdc_src_ck clock enable bit for PSC** 1'b0: Disable 1'b1: Enable
24	**MSPCCKEN**	MSDC_CK_SPC_CKEN	**msdc_src_ck clock enable bit forSPC** 1'b0: Disable 1'b1: Enable
23	**HGDMACKEN**	AHB_CK_GDMA_CKEN	**hclk_ck clock enable bit for GDMA** 1'b0: Disable 1'b1: Enable
21	**DCMEN**	DCM_EN	**host enable dcm for low power,when there is no transfer the ahb_ck and msdc_src_ck will divder from spurce clk** 1'b1:disable 1'b0:enable

Bit(s)	Mnemonic	Name	Description
16	**SINGLEBURST**	ENABLE_SINGLE_BURST	**the ahb bus will not support incr1 burst type in future.And it will only affect AHB bus msdc design,not affect AXI bus design** 1'b0:hw will send incr1 burst type 1'b1: hw will send single burst typr instead of incr1 type
15	**RESETGDMA**	RESET_GDMA	**sw can sw reset gdma when design hang** 1 'b1: reset gdma 1'b0: not reset gdma
14	**DDRCMDFIXSEL**	DDR_CMD_FIX_SEL	**add T/4 margin for DDR mode cmd** 1'b1: fix DDR/HS400 mode cmd timing 1'b0: not fix
13	**BIAS28R0**	BIAS_EXTBIAS_28NM	**28NM BIAS Controler register 0**
12	**BIAS28R1**	BIAS_EN18IO_28NM	**28NM BIAS Controler register 1**
11:8	**STOPDLYSEL**	STOP_DLY_SEL	**configuration read data clock stop at block gap**
7	**BUSYCHECKSEL**	BUSY_CHECK_SEL	**1.r1b check dat0 then gen irq** 2.write prog time out check 1'b0: do not check data0 status gen cmdrdy int when send R1b cmd / do not check write prog timeout 1'b1: check data0 status gen cmdrdy int when send R1b cmd / check write prog timeout
6	**GETBUSYMARGIN**	GET_BUSY_MARGIN	**it will add margin for get busy state of data0** 1'b0: 1 cycle reserved for get busy state from src status endbit 1'b1: 3cycle reserved for get busy state from src status endbit
5:3	**CMDTA**	CMD_RSP_TA_CNTR	**CMD response turn around period** The turn around cycle = CMD_RSP_TA_CNTR + 2 In USH104 mode, this register should be set to 1 In non-UHS104 mode, this register should be set to 0
2:0	**WRTA**	WRDAT_CRCS_TA_CNTR	**Write data and CRC status turn around period** The turn around cycle = WRDAT_CRCS_TA_CNTR + 2

Bit(s)	Mnemonic	Name	Description
			In USH104 mode, this register should be set to 1 In non-UHS104 mode,this register should be set to 0

112400B8 PATCH_BIT2 MSDC Patch Bit Register 2 14881803

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRCSTS_LATCH_EN_SEL			CFG_CRCSTS	CFG_CRCSTS_CNT		CFG_CRCSTS_EDGE	CFG_CRCSTS_SEL	POP_EN_CNT				DDR50_SEL	RESP_LATCH_EN_SEL		
Type	RW			RW	RW		RW	RW	RW				RW	RW		
Reset	0	0	0	1	0	1	0	0	1	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG_RESP	CFG_RESP_CNT			INTC_RESP_SEL		CFG_RDAT	CFG_RDAT_CNT					RESP_WAIT_CNT		SUPPORT_64G	ENHANCE_WAIT_GPD
Type	RW	RW			RW		RW	RW					RW		RW	RW
Reset	0	0	0	1	1		0	0	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:29	**CRCSTSENSEL**	CRCSTS_LATCH_EN_SEL	**This register used configuration latch CRC Status enable signal for async fifo in emmc45** 3'b000: latch CRC Status enable signal not delay 3'b001: latch CRC Status enable signal delay 1T msdc_ck 3'b010: latch CRC Status enable signal delay 2T msdc_ck 3'b011: latch CRC Status enable signal delay 3T msdc_ck 3'b111: latch CRC Status enable signal delay 7T msdc_ck
28	**CFGCRCSTS**	CFG_CRCSTS	**This register used configuration CRC Status path selection,this setting only used emmc4.5 feature** 1'b0:Latch CRC Status select delay-line path 1'b1:Latch CRC Status select async fifo path
27:26	**CFGCRCSTSCNT**	CFG_CRCSTS_CNT	**This register used configuration how many data push in async fifo until start pop out data from async fifo ,this**

Bit(s)	Mnemonic	Name	Description
			register setting min is 1 do not setting is 0,this setting only used emmc4.5 feature 2'b00:push 0 data in async fifo when start pop out data from async fifo 2'b01:push 1 data in async fifo when start pop out data from async fifo 2'b10:push 2 data in async fifo when start pop out data from async fifo 2'b11:push 3 data in async fifo when start pop out data from async fifo
25	**CFGCRCSTSEDGE**	CFG_CRCSTS_EDGE	**This register configuration used rising async fifo or falling async fifo** 1'b0:async fifo latch CRC Status used rising async fifo 1'b1:async fifo latch CRC Status used falling async fifo
24		CFG_CRCSTS_SEL	**This register configuration async fifo path selection** 1'b0:used normal path in async fifo 1'b1:used 2DFF path in async fifo
23:20	**POPENCNT**	POP_EN_CNT	**pop enable counter** This field is used to define how many write pointer and the read pointer margin began to pop data transfer
19	**DDR50SEL**	DDR50_SEL	**new path can avoid byte swap issue** 1'b0:old path for rising and faling data 1'b1:new path that rasing data to rasing fifo and faling data to faling fifo
18:16	**RESPSTSENSEL**	RESP_LATCH_EN_SEL	**This register used configuration latch CMD Response enable signal for async fifo in emmc45** 3'b000: latch CMD Response enable signal not delay 3'b001: latch CMD Response enable signal delay 1T msdc_ck 3'b010: latch CMD Response enable signal delay 2T msdc_ck 3'b011: latch CMD Response enable signal delay 3T msdc_ck

Bit(s)	Mnemonic	Name	Description
			3'b111: latch CMD Response enable signal delay 7T msdc_ck
15	**CFGRESP**	CFG_RESP	**This register used configuration CMD Response path selection,this setting only used emmc4.5 feature** 1'b0:Latch CMD Response select async fifo path 1'b1:Latch CMD Response select delay-line path
14:12	**CFGRESPCNT**	CFG_RESP_CNT	**This register used configuration how many data push in async fifo until start pop out data from async fifo ,this register setting min is 1 do not setting is 0,this setting only used emmc4.5 feature** 3'b000:push 0 data in async fifo when start pop out data from async fifo 3'b001:push 1 data in async fifo when start pop out data from async fifo 3'b111:push 7 data in async fifo when start pop out data from async fifo
11	**INTCRESPSEL**	INTC_RESP_SEL	**This register configuration BREAK command async fifo path** 1'b0:used normal path in async fifo 1'b1:used 2DFF path in async fifo
9	**CFGRDAT**	CFG_RDAT	**This register used configuration read data path** 1'b0: read data path by pass delay line 1'b1:read data path through delay line
8:4	**CFGRDATCNT**	CFG_RDAT_CNT	**This register used configuration read data path delay line**
3:2	**RESPWAITCNT**	RESP_WAIT_CNT	**This register used configuration cmd response timeout,timeout cycle is 65T+16*RESP_WAIT_CNT** 2'b00:cmd response timeout is 65T 2'b01:cmd response timeout is 65T+ 16*1T 2'b01:cmd response timeout is 65T+ 16*2T 2'b01:cmd response timeout is 65T+ 16*3T
1	**SUPPORT64G**	SUPPORT_64G	**This register used which proj support high 64G dram space access** 1'b1:support 64G dram access

Bit(s)	Mnemonic	Name	Description
			1'b0:not support 64G dram access
0	**ENHANCEGPD**	ENHANCE_WAIT_GPD	**if sw clear int when gpd not update finish,design will hang.so you can set this bt to 1 to avoid this iuuse in enhance write mode** 1'b1:use new HW code for update gpd in enhance mode 1'b0:use old HW code

112400C0 DAT0_TUNE_CRC DAT0 Tune Result Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT0_CRC_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT0_CRC_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DAT0CRCSTS**	DAT0_CRC_STS	**SDIO Auto command 53 test result register** When auto-command 53 is enabled, H/W will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT0 into this register. This register contains 1st to 32th results in bit[0:31]

112400C4 DAT1_TUNE_CRC DAT1 Tune Result Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT1_CRC_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT1_CRC_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DAT1CRCSTS**	DAT1_CRC_STS	**SDIO Auto command 53 test result register** When auto-command 53 is enabled, H/W will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT1 into this register. This register contains 1st to 32th results in bit[0:31]

112400C8 DAT2_TUNE_CRC DAT2 Tune Result Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT2_CRC_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT2_CRC_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DAT2CRCSTS**	DAT2_CRC_STS	**SDIO Auto command 53 test result register** When auto-command 53 is enabled, H/W will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT2 into this register. This register contains 1st to 32th results in bit[0:31]

112400CC DAT3_TUNE_CRC DAT3 Tune Result Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT3_CRC_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT3_CRC_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DAT3CRCSTS**	DAT3_CRC_STS	**SDIO Auto command 53 test result register** When auto-command 53 is enabled, H/W will automatically try TUNE_WINDOW times of command-53 and store CRC result of DAT3 into this register. This register contains 1st to 32th results in bit[0:31]

112400D0 CMD_TUNE_CRC CMD Tune Result Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMD_CRC_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMD_CRC_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CMDCRCSTS**	CMD_CRC_STS	**SDIO Auto command 53 test result register** When auto-command 53 is enabled, H/W will automatically try TUNE_WINDOW times of command-53 and store CRC result of CMD into this register. This register contains 1st to 32th results in bit[0:31]

112400D4 SDIO_TUNE_WIND SDIO Tune Window Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TUNE_WINDOW				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0	**TUNEWINDOW**	TUNE_WINDOW	**SDIO Auto command 53 tuning window setting. the window range will be** 1. for CMD PAD low bound: max(0, PAD_CMD_RXDLY-TUNE_WINDOW) high bound: min(31, PAD_CMD_RXDLY+TUNE_WINDOW) 2. for DAT PAD low bound: max(0, DAT(0:3)_RD_DLY-TUNE_WINDOW) high bound:min(31: DAT(0:3)_RD_DLY+TUNE_WINDOW)

112400F0 PAD_TUNE0 MSDC Pad Tuning Register0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PAD_CLK_TXDLY					PAD_CMD_RESP_RXDLY					PAD_CMD_RD_RXDLY_SEL	PAD_CMD_RXDLY				
Type	RW					RW					RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAD_RXDLY_SEL		PAD_DAT_RD_RXDLY_SEL	PAD_DAT_RD_RXDLY					DELAY_EN			PAD_DAT_WR_RXDLY				
Type	RW		RW	RW					RW			RW				
Reset	0		0	0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:27	**CLKTDLY**	PAD_CLK_TXDLY	**CLK Pad TX Delay Control** This register is used to add delay to CLK phase. Total 32 stages
26:22	**CMDRRDLY**	PAD_CMD_RESP_RXDLY	**CMD Response Internal Delay Line Control** This register is used to fine-tune response phase latched by MSDC internal clock Total 32 stages

Bit(s)	Mnemonic	Name	Description
21	**CMDRRDLYSEL**	PAD_CMD_RD_RXDLY_SEL	**Decide CMD Response pass through data delay line1 or not** 1'b0: pass 1'b1: do not pass
20:16	**CMDRDLY**	PAD_CMD_RXDLY	**CMD Pad RX Delay Line1 Control** This register is used to fine-tune CMD pad macro respose latch timing Total 32 stages
15	**RXDLYSEL**	PAD_RXDLY_SEL	**Decide rx delay line tune data path or clock path** 1'b0: rx delay line tune data path 1'b1: rx delay line tune clock path
13	**DATRRDLYSEL**	PAD_DAT_RD_RXDLY_SEL	**Decide rx data pass through data delay line1 or not** 1'b0: pass 1'b1: do not pass
12:8	**DATRRDLY**	PAD_DAT_RD_RXDLY	**DAT Pad RX Delay Line1 Control (for MSDC read only)** This register is used to fine-tune DAT pad macro read data latch timing Total 32 stages
7	**DELAYEN**	DELAY_EN	**enable all delay cell toogle when power on** 1'b0:disable delay cell toogle default 1'b1:enable delay cell toogle default
4:0	**DATWRDLY**	PAD_DAT_WR_RXDLY	**Write Data Status Internal Delay Line Control** This register is used to fine-tune write status phase latched by MSDC internal clock Total 32 stages

112400F4 PAD_TUNE1 MSDC Pad Tuning Register1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											PAD_CMD_RD	PAD_CMD_RXDLY2				

											_RXDLY2_SEL					
Type											RW	RW				
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			PAD_DAT_RD_RXDLY2_SEL	PAD_DAT_RD_RXDLY2												
Type			RW	RW												
Reset			0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
21	**CMDRRDLY2SEL**	PAD_CMD_RD_RXDLY2_SEL	**Decide CMD Response pass through data delay line2 or not** 1'b0: pass 1'b1: do not pass
20:16	**CMDRDLY2**	PAD_CMD_RXDLY2	**CMD Pad RX Delay Line2 Control** This register is used to fine-tune CMD pad macro respose latch timing in data path Total 32 stages
13	**DATRRDLY2SEL**	PAD_DAT_RD_RXDLY2_SEL	**Decide rx data pass through data delay line2 or not** 1'b0: pass 1'b1: do not pass
12:8	**DATRRDLY2**	PAD_DAT_RD_RXDLY2	**DAT Pad RX Delay Line2 Control (for MSDC read only)** This register is used to fine-tune DAT pad macro read data latch timing Total 32 stages

112400F8 DAT_RD_DLY0 MSDC Data Delay Line Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0_RD_DLY								DAT1_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name				DAT2_RD_DLY								DAT3_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT0RDDLY**	DAT0_RD_DLY	**DAT0 Pad RX Delay Line1 Control (for MSDC RD)** Total 32 stages
20:16	**DAT1RDDLY**	DAT1_RD_DLY	**DAT1 Pad RX Delay Line1 Control (for MSDC RD)** Total 32 stages
12:8	**DAT2RDDLY**	DAT2_RD_DLY	**DAT2 Pad RX Delay Line1 Control (for MSDC RD)** Total 32 stages
4:0	**DAT3RDDLY**	DAT3_RD_DLY	**DAT3 Pad RX Delay Line1 Control (for MSDC RD)** Total 32 stages

112400FC DAT_RD_DLY1 MSDC Data Delay Line Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT4_RD_DLY								DAT5_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT6_RD_DLY								DAT7_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT4RDDLY**	DAT4_RD_DLY	**DAT4 Pad RX Delay Line1 Control (for MSDC RD)** Total 32 stages
20:16	**DAT5RDDLY**	DAT5_RD_DLY	**DAT5 Pad RX Delay Line1 Control (for MSDC RD)** Total 32 stages
12:8	**DAT6RDDLY**	DAT6_RD_DLY	**DAT6 Pad RX Delay Line1 Control (for MSDC RD)** Total 32 stages
4:0	**DAT7RDDLY**	DAT7_RD_DLY	**DAT7 Pad RX Delay Line1 Control (for MSDC RD)**

Bit(s)	Mnemonic	Name	Description
			Total 32 stages

11240100 DAT_RD_DLY2 MSDC Data Delay Line Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0_RD_DLY2								DAT1_RD_DLY2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT2_RD_DLY2								DAT3_RD_DLY2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT0RDDLY2**	DAT0_RD_DLY2	**DAT0 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages
20:16	**DAT1RDDLY2**	DAT1_RD_DLY2	**DAT1 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages
12:8	**DAT2RDDLY2**	DAT2_RD_DLY2	**DAT2 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages
4:0	**DAT3RDDLY2**	DAT3_RD_DLY2	**DAT3 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages

11240104 DAT_RD_DLY3 MSDC Data Delay Line Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT4_RD_DLY2								DAT5_RD_DLY2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT6_RD_DLY2								DAT7_RD_DLY2				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT4RDDLY2**	DAT4_RD_DLY2	**DAT4 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages
20:16	**DAT5RDDLY2**	DAT5_RD_DLY2	**DAT5 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages
12:8	**DAT6RDDLY2**	DAT6_RD_DLY2	**DAT6 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages
4:0	**DAT7RDDLY2**	DAT7_RD_DLY2	**DAT7 Pad RX Delay Line2 Control (for MSDC RD)** Total 32 stages

11240110 HW_DBG_SEL MSDC H/W Debug Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HW_DBG_WRAP_SEL	HW_DBG_WRAP_TYPE_SEL		HW_DBG3_SEL					HW_DBG2_SEL							
Type	RW	RW		RW					RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_DBG1_SEL								HW_DBG0_SEL							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**DBGWSEL**	HW_DBG_WRAP_SEL	**H/W debug output selection for wrapper** 0: Select original debug pins 1: Select wrapper debug pins
30:29	**DBGWTSEL**	HW_DBG_WRAP_TYPE_SEL	**H/W debug output type selection for wrapper** 2'b00: Select dram bus debug signal 2'b01: Select risc bus debug signal 2'b10: select ahbm bus debug signal 2'b11: select ahbs bus debug signal
28:24	**DBG3SEL**	HW_DBG3_SEL	**H/W debug output selection**

Bit(s)	Mnemonic	Name	Description
23:16	**DBG2SEL**	HW_DBG2_SEL	**H/W debug output selection**
15:8	**DBG1SEL**	HW_DBG1_SEL	**H/W debug output selection**
7:0	**DBG0SEL**	HW_DBG0_SEL	**H/W debug output selection**

11240114 MAIN_VER MSDC Main Version Register 20160506

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**MAIN_VER**															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MAIN_VER**															
Type	RO															
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0

Bit(s)	Mnemonic	Name	Description
31:0	**MAINVER**	MAIN_VER	**Main Version**

11240118 ECO_VER MSDC ECO Version Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**ECO_VER**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ECO_VER**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ECOVER**	ECO_VER	**ECO Version**

2 High Speed Interface

2.1 Register Definition

2.1.1 USB MAC

2.1.1.1 ssusb_host

Module name: ssusb_host Base address: (+1a0c0000h)

Address	Name	Width	Register Function
1A0C0000	CAPLENGTH	32	Capability Register Length
1A0C0004	HCSPARAMS1	32	Structural Parameters 1
1A0C0008	HCSPARAMS2	32	Structural Parameters 2
1A0C000C	HCSPARAMS3	32	Structural Parameters 3
1A0C0010	HCCPARAMS	32	Capability Parameters
1A0C0014	DBSOFF	32	Doorbell Offset
1A0C0018	RTSOFF	32	Runtime Register Space Offset
1A0C0020	USBCMD	32	USB Command
1A0C0024	USBSTS	32	USB Status
1A0C0028	PAGESIZE	32	Page Size
1A0C0034	DNCTRL	32	Device Notification Control
1A0C0038	CRCR1	32	Command Ring Control 1
1A0C003C	CRCR2	32	Command Ring Control 2
1A0C0050	DCBAAP_LO	32	Device Context Base Address Array Pointer Lo
1A0C0054	DCBAAP_HI	32	Device Context Base Address Array Pointer High
1A0C0058	CONFIG	32	Configure
1A0C0500	SUPP_PTCL_REG1	32	xHCI Supported Protocol Capability 1 Register
1A0C0504	SUPP_PTCL_REG2	32	xHCI Supported Protocol Capability 2 Register
1A0C0508	SUPP_PTCL_REG3	32	xHCI Supported Protocol Capability 3 Register
1A0C0510	SUPP_PTCL_REG4	32	xHCI Supported Protocol Capability 1 Register
1A0C0514	SUPP_PTCL_REG5	32	xHCI Supported Protocol Capability 2 Register
1A0C0518	SUPP_PTCL_REG6	32	xHCI Supported Protocol Capability 3 Register
1A0C0600	MFINDEX	32	Microframe Index
1A0C0620	IMAN	32	Interrupter Management
1A0C0624	IMOD	32	Interrupter Moderation
1A0C0628	ERSTSZ	32	Event Ring Segment Table Size
1A0C0630	ERSTBA_LO	32	Event Ring Segment Table Base Address Lo
1A0C0634	ERSTBA_HI	32	Event Ring Segment Table Base Address Hi
1A0C0638	ERDP_LO	32	Event Ring Segment Table Base Address Lo
1A0C063C	ERDP_HI	32	Event Ring Segment Table Base Address Hi
1A0C0800	HOST_CMD_DB	32	Host Controller Doorbell Registers
1A0C0804	DEVICE1_DB	32	Device 1 Doorbell Registers
1A0C0808	DEVICE2_DB	32	Device 2 Doorbell Registers
1A0C080C	DEVICE3_DB	32	Device 3 Doorbell Registers

Address	Name	Width	Register Function
1A0C0810	DEVICE4_DB	32	Device 4 Doorbell Registers
1A0C0814	DEVICE5_DB	32	Device 5 Doorbell Registers
1A0C0818	DEVICE6_DB	32	Device 6 Doorbell Registers
1A0C081C	DEVICE7_DB	32	Device 7 Doorbell Registers
1A0C0820	DEVICE8_DB	32	Device 8 Doorbell Registers
1A0C0824	DEVICE9_DB	32	Device 9 Doorbell Registers
1A0C0828	DEVICE10_DB	32	Device 10 Doorbell Registers
1A0C082C	DEVICE11_DB	32	Device 11 Doorbell Registers
1A0C0830	DEVICE12_DB	32	Device 12 Doorbell Registers
1A0C0834	DEVICE13_DB	32	Device 13 Doorbell Registers
1A0C0838	DEVICE14_DB	32	Device 14 Doorbell Registers
1A0C083C	DEVICE15_DB	32	Device 15 Doorbell Registers
1A0C0900	HSRAM_DBGCTL	32	Host SRAM Debug Control Register
1A0C0904	HSRAM_DBGMODE	32	Host SRAM Debug Mode Register
1A0C0908	HSRAM_DBGSEL	32	Host SRAM Debug Select Register
1A0C090C	HSRAM_DBGADR	32	Host SRAM Debug Address Register
1A0C0910	HSRAM_DBGDR	32	Host SRAM Debug Data Register
1A0C0920	HSRAM_DELSEL_0	32	Host SRAM Delay Select 0
1A0C0924	HSRAM_DELSEL_1	32	Host SRAM Delay Select 1
1A0C092C	AXI_ID	32	AXI DMA ID configuration register
1A0C0930	LS_EOF	32	Low Speed EOF Start Offset
1A0C0934	FS_EOF	32	Full Speed EOF Start Offset
1A0C0938	SYNC_HS_EOF	32	Synchronous High Speed EOF Start Offset
1A0C093C	SS_EOF	32	Super Speed EOF Start Offset
1A0C0940	SOF_OFFSET	32	SOF Offset
1A0C0944	HFCNTR_CFG	32	Host Frame Counter Configuration
1A0C0948	XACT3_CFG	32	Super Speed Transaction Configuration
1A0C094C	XACT2_CFG	32	USB2 Transaction Configuration
1A0C0950	HDMA_CFG	32	Host DMA Configuration
1A0C0954	ASYNC_HS_EOF	32	Asynchronous High Speed EOF Start Offset
1A0C0958	AXI_WR_DMA_CFG	32	AXI WR DMA configuration register.
1A0C095C	AXI_RD_DMA_CFG	32	AXI RD DMA configuration register.
1A0C0960	HSCH_CFG1	32	Host Scheduler Configuration Register 1
1A0C0964	CMD_CFG	32	Command Configuration
1A0C0968	EP_CFG	32	Endpoint Status Configuration
1A0C096C	EVT_CFG	32	Event Configuration
1A0C0970	TRBQ_CFG	32	TRBQ Configuration
1A0C0974	U3PORT_CFG	32	USB3 Port Configuration
1A0C0978	U2PORT_CFG	32	USB2 Port Configuration
1A0C097C	HSCH_CFG2	32	Host Scheduler Configuration Register 2
1A0C0980	SW_ERDY	32	Software ERDY
1A0C09A0	SLOT_EP_STS0	32	Slot and EP Resource Status0
1A0C09A4	SLOT_EP_STS1	32	Slot and EP Resource Status1
1A0C09A8	SLOT_EP_STS2	32	Slot and EP Resource Status2
1A0C09B0	RST_CTRL0	32	Host reset control Register 2

Address	Name	Width	Register Function
1A0C09B4	RST_CTRL1	32	Host reset control Register 3
1A0C09F0	SPARE0	32	Spare Register 0
1A0C09F4	SPARE1	32	Spare Register 1

1A0C0000 CAPLENGTH Capability Register Length 00960020

Bit	31	30	29	28	27	26	25	24
Name	HCIVERSION							
Type	RO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	HCIVERSION							
Type	RO							
Reset	1	0	0	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	CAPLENGTH							
Type	RO							
Reset	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		HCIVERSION	**This is a two-byte register containing a BCD encoding of the xHCI specification revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision. e.g. 0100h corresponds to xHCI version 1.0.** Note: Pre-release versions of the xHC shall declare the specific version of the xHCI that it was implemented against. e.g. 0090h = version 0.9.
7:0		CAPLENGTH	**This register is used as an offset to add to register base to find the beginning of the Operational Register Space**

1A0C0004 HCSPARAMS1 Structural Parameters 1 0700010F

Bit	31	30	29	28	27	26	25	24
Name	MAXPORTS							
Type	RO							

Reset	0	0	0	0	0	1	1	1
Bit	23	22	21	20	19	18	17	16
Name						**MAXINTRS**		
Type						RO		
Reset						0	0	0
Bit	15	14	13	12	11	10	9	8
Name	**MAXINTRS**							
Type	RO							
Reset	0	0	0	0	0	0	0	1
Bit	7	6	5	4	3	2	1	0
Name	**MAXSLOTS**							
Type	RO							
Reset	0	0	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:24		MAXPORTS	**Number of Ports (MaxPorts).** This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space (refer to Table 26). Valid values are in the range of 1h to FFh.
18:8		MAXINTRS	**Number of Interrupters (MaxIntrs).** This field specifies the number of Interrupters implemented on this host controller. Each Interrupter is allocated to a vector of MSI-X and controls its generation and moderation. The value of this field determines how many Interrupter Register Sets are addressable in the Runtime Register Space (refer to section 5.5). Valid values are in the range of 1h to 400h. A '0' in this field is undefined.
7:0		MAXSLOTS	**Number of Device Slots (MaxSlots).** This field specifies the maximum number of Device Context Structures and Doorbell Array entries this host controller can support. Valid values are in the range of 1 to 255. The value of '0' is reserved.

1A0C0008 HCSPARAMS2 Structural Parameters 2 00001004

Bit	31	30	29	28	27	26	25	24
Name	**MAX_SCRATCHPAD_BUFS**					**SPR**		
Type	RO					RO		
Reset	0	0	0	0	0	0		

Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name				IOC_INTERVAL				
Type				RO				
Reset				1	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	ERST_MAX				IST			
Type	RO				RW			
Reset	0	0	0	0	0	1	0	0

Bit(s)	Mnemonic	Name	Description
31:27		MAX_SCRATCHPAD_BUFS	**Max Scratchpad Buffers (Max Scratchpad Bufs).** Default = implementation dependent. Valid values are 0-31. This field indicates the number of Scratchpad Buffers system software shall reserve for the xHC. Refer to section 4.20 for more information.
26		SPR	**Scratchpad Restore (SPR).** Default = implementation dependent. If Max Scratchpad Buffers is > '0' then this flag indicates whether the xHC uses the Scratchpad Buffers for saving state when executing Save and Restore State operations. If Max Scratchpad Buffers is = '0' then this flag shall be '0'. Refer to section 4.23.2 for more information. A value of '1' indicates that the xHC requires the integrity of the Scratchpad Buffer space to be maintained across power events. A value of '0' indicates that the Scratchpad Buffer space may be freed and reallocated between power events.
12:8		IOC_INTERVAL	**IOC Interval.** Default = implementation dependent. Valid values are 0 - 23. This field determines the maximum frequency with which the IOC flag may be set for this xHC implementation. The IOC flag may be set in TRBs that define data buffers that are more than 2 IOC Interval bytes apart. Refer to section 4.11.7.1 for more information on the use and interpretation of the IOC Interval.
7:4		ERST_MAX	**Event Ring Segment Table Max (ERST Max).**

Bit(s)	Mnemonic	Name	Description
			Default = implementation dependent. Valid values are 0 - 15. This field determines the maximum value supported the Event Ring Segment Table Base Size registers (5.5.2.3.1), where: The maximum number of Event Ring Segment Table entries = 2 ERST Max. e.g. if the ERST Max = 7, then the xHC Event Ring Segment Table(s) supports up to 128 entries, 15 then 32K entries, etc.
3:0		IST	**Isochronous Scheduling Threshold (IST).** Default = implementation dependent. The value in this field indicates to system software the minimum distance (in time) that it is required to stay ahead of the host controller while adding TRBs, in order to have the host controller process them at the correct time. The value shall be specified in terms of number of frames/microframes. If bit [3] of IST is cleared to '0', software can add a TRB no later than IST[2:0] Microframes before that TRB is scheduled to be executed. If bit [3] of IST is set to '1', software can add a TRB no later than IST[2:0] Frames before that TRB is scheduled to be executed. Refer to Section 4.14.2 for details on how software uses this information for scheduling isochronous transfers.

1A0C000C HCSPARAMS3 Structural Parameters 3 00010001

Bit	31	30	29	28	27	26	25	24
Name	U2_DEVICE_EXIT_LATENCY							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	U2_DEVICE_EXIT_LATENCY							
Type	RW							
Reset	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	U1_DEVICE_EXIT_LATENCY							
Type	RW							
Reset	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:16		U2_DEVICE_EXIT_LATENCY	**U2 Device Exit Latency.** Worst case latency to transition from U2 to U0. Applies to all root hub ports. The following are permissible values: Value Description 0000h Zero 0001h Less than 1 us. 0002h Less than 2 us. ... 07FFh Less than 2047 us. 0800-FFFFh Reserved
7:0		U1_DEVICE_EXIT_LATENCY	**U1 Device Exit Latency.** Worst case latency to transition a root hub Port Link State (PLS) from U1 to U0. Applies to all root hub ports. The following are permissible values: Value Description 00h Zero 01h Less than 1 us 02h Less than 2 us. ... 0Ah Less than 10 us. 0B-FFh Reserved

1A0C0010 HCCPARAMS Capability Parameters 01401198

Bit	31	30	29	28	27	26	25	24
Name	XECP							
Type	RO							
Reset	0	0	0	0	0	0	0	1
Bit	23	22	21	20	19	18	17	16
Name	XECP							
Type	RO							
Reset	0	1	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Name	MAXPSASIZE						SBD	PAE
Type	RO						RO	RO
Reset	0	0	0	1			0	1
Bit	7	6	5	4	3	2	1	0
Name	NSS	LTC	LHRC	PIND	PPC	CSZ	BNC	AC64
Type	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	0	0	1	1	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		XECP	**xHCI Extended Capabilities Pointer (xECP).** This field indicates the existence of a capabilities list. The value of this field indicates a relative offset, in 32-bit words, from Base to the beginning of the first extended capability. For example, using the offset of Base is 1000h and the xECP value of 0068h, we can calculated the following effective address of the first extended capability: 1000h + (0068h << 2) -> 1000h + 01A0h -> 11A0h
15:12		MAXPSASIZE	**Maximum Primary Stream Array Size (MaxPSASize).** This fields identifies the maximum size Primary Stream Array that the xHC supports. The Primary Stream Array size = 2MaxPSASize+1. Valid MaxPSASize values are 1 to 15.
9		SBD	**Secondary Bandwidth Domain Reporting (SBD).** This flag indicates whether the host controller implementation is capable of reporting Secondary Bandwidth Domain information. A '1' in this bit indicates that Secondary Bandwidth Domain reporting is supported. A '0' in this bit indicates that Secondary Bandwidth Domain reporting is not supported. Refer to Section 4.16.2 for more information on the use of this flag.
8		PAE	**Parse All Event Data (PAE). This flag indicates whether the host controller implementation** Parses all Event Data TRBs while advancing to the next TD after a short packet, or it skips all but the first Event Data TRB. A '1' in this bit indicates that all Event Data TRBs are parsed. A '0' in this bit indicates that only the first Event Data TRB is parsed (refer to section 4.10.1.1).

Bit(s)	Mnemonic	Name	Description
7		NSS	**No Secondary SID Support (NSS).** This flag indicates whether the host controller implementation supports Secondary Stream IDs. A '1' in this bit indicates that Secondary Stream ID decoding is not supported. A '0' in this bit indicates that Secondary Stream ID decoding is supported. (refer to Sections 4.12.2 and 6.2.3).
6		LTC	**Latency Tolerance Messaging Capability (LTC).** This flag indicates whether the host controller implementation supports Latency Tolerance Messaging (LTM). A '1' in this bit indicates that LTM is supported. A '0' in this bit indicates that LTM is not supported. Refer to section 4.13.1 for more information on LTM.
5		LHRC	**Light HC Reset Capability (LHRC).** This flag indicates whether the host controller implementation supports a Light Host Controller Reset. A '1' in this bit indicates that Light Host Controller Reset is supported. A '0' in this bit indicates that Light Host Controller Reset is not supported. The value of this flag affects the functionality of the Light Host Controller Reset (LHCRST) flag in the USBCMD register (refer to Section 5.4.1).
4		PIND	**Port Indicators (PIND).** This bit indicates whether the xHC root hub ports support port indicator control. When this bit is a '1', the port status and control registers include a read/ writeable field for controlling the state of the port indicator. Refer to Section 5.4.8 for definition of the Port Indicator Control field.
3		PPC	**Port Power Control (PPC).** This flag indicates whether the host controller implementation includes port power control. A '1' in this bit indicates the ports have port power switches. A '0' in this bit indicates the port do not have port power switches. The value of this flag affects the functionality of the PP flag in each port status and control register (refer to Section 5.4.8).
2		CSZ	**Context Size (CSZ).** If this bit is set to '1', then the xHC uses 64 byte Context data structures. If this bit is cleared to '0', then the xHC uses 32 byte Context data structures. Note: This flag does not apply to Stream Contexts.
1		BNC	**BW Negotiation Capability (BNC).**

Bit(s)	Mnemonic	Name	Description
			This flag identifies whether the xHC has implemented the Bandwidth Negotiation. Values for this flag have the following interpretation: Value Description 0 BW Negotiation not implemented 1 BW Negotiation implemented Refer to section 4.16 for more information on Bandwidth Negotiation.
0		AC64	**64-bit Addressing Capabilitya (AC64).** This flag documents the addressing range capability of this implementation. The value of this flag determines whether the xHC has implemented the high order 32 bits of 64 bit register and data structure pointer fields. Values for this flag have the following interpretation: Value Description 0 32-bit address memory pointers implemented 1 64-bit address memory pointers implemented If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32 bits of 64 bit data structure pointer fields, and system software shall ignore the high order 32 bits of 64 bit xHC registers.

1A0C0014 DBSOFF Doorbell Offset 00000800

Bit	31	30	29	28	27	26	25	24
Name	DBSOFF							
Type	RO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	DBSOFF							
Type	RO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	DBSOFF							
Type	RO							
Reset	0	0	0	0	1	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	DBSOFF							
Type	RO							
Reset	0	0	0	0	0	0		

Bit(s)	Mnemonic	Name	Description
31:2		DBSOFF	**Doorbell Array Offset.** Default = implementation dependent. This field defines the Dword offset of the Doorbell Array base address from the Base (i.e. the base address of the xHCI Capability register address space).

1A0C0018 RTSOFF Runtime Register Space Offset 00000600

Bit	31	30	29	28	27	26	25	24
Name	RTSOFF							
Type	RO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	RTSOFF							
Type	RO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	RTSOFF							
Type	RO							
Reset	0	0	0	0	0	1	1	0
Bit	7	6	5	4	3	2	1	0
Name	RTSOFF							
Type	RO							
Reset	0	0	0					

Bit(s)	Mnemonic	Name	Description
31:5		RTSOFF	**Runtime Register Space Offset.** Default = implementation dependent. This field defines the 32-byte offset of the xHCI Runtime Registers from the Base. i.e. Runtime Register Base Address = Base + Runtime Register Set Offset.

1A0C0020 USBCMD USB Command 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								

Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name					**EU3S**	**EWE**	**CRS**	**CSS**
Type					RW	RW	RO	RO
Reset					0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	**LHCRST**				**HSEE**	**INTE**	**HCRST**	**R_S**
Type	RO				RW	RW	RW	RW
Reset	0				0	0	0	0

Bit(s)	Mnemonic	Name	Description
11		EU3S	**Enable U3 MFINDEX Stop (EU3S).** When set to '1', the xHC may stop the MFINDEX counting action if all Root Hub ports are in the U3, Disconnected, Disabled, or Powered-off state. When cleared to '0' the xHC may stop the MFINDEX counting action if all Root Hub ports are in the Disconnected, Disabled, or Powered-off state.
10		EWE	**Enable Wrap Event (EWE).** Default = '0'. When set to '1', the xHC shall generate a MFINDEX Wrap Event every time the MFINDEX register transitions from 03FFFh to 0. When set to '0' no MFINDEX Wrap Events are generated. When this register is exposed by a Virtual Function (VF), the generation of MFINDEX Wrap Events to VFs must be emulated by the VMM.
9		CRS	**Controller Restore State (CRS).** When set to '1', Run/Stop = '0', and Save State = '1', the xHC shall perform a Restore State operation and restore its internal state. When set to '1' and Run/Stop = '1' or Save State = '0', or when set to '0', no Restore State operation shall be performed. This field always returns '0' when read. See the Restore State Status flag in the USBSTS register for information on Restore State completion. When this register is exposed by a Virtual Function (VF), this bit only controls restoring the state of the xHC instance presented by the selected VF.
8		CSS	**Controller Save State (CSS).**

Bit(s)	Mnemonic	Name	Description
			When written by software with '1' and Run/ Stop = '0', the xHC shall save any internal state that will be restored by a subsequent Restore State operation. When written by software with '1' and Run/ Stop = '1', or written with '0', no Save State operation shall be performed. See the Save State Status flag in the USBSTS register for information on Save State completion. This field is set to '0' after initial power-up of the Auxiliary Power Well, by HCRST, or by LHCRST. When this register is exposed by a Virtual Function (VF), this bit only controls saving the state of the xHC instance presented by the selected VF
7		LHCRST	**Light Host Controller Reset (LHCRST).** Optional normative. If the Light HC Reset Capability (LHRC) bit in the HCCPARAMS register is '1', then this field allows the driver to reset the xHC without affecting the state of the ports. A system software read of this bit as '0' indicates the Light Host Controller Reset has completed and it is safe for software to re-initialize the xHC. A software read of this bit as a '1' indicates the Light Host Controller Reset has not yet completed. If not implemented, a read of this field will always return a '0'. All registers in the Auxiliary well will maintain the values that had been asserted prior to the Light Host Controller Reset. When this register is exposed by a Virtual Function (VF), this bit only generates a Light Reset to the xHC instance presented by the selected VF, e.g. Disable the VFs' device slots and set the associated VF Run bit to Stopped.
3		HSEE	**Host System Error Enable (HSEE).** When this bit is a '1', and the HSE bit in the USBSTS register is a '1', the xHC shall assert out-of-band error signaling to the host. The signaling is acknowledged by software clearing the HSE bit. When this register is exposed by a Virtual Function (VF), the effect of the assertion of this bit on the Physical Function (PF0) is determined by the VMM.
2		INTE	**Interrupter Enable (INTE).** This bit provides system software with a means of enabling or disabling the host system interrupts generated by Interrupters. When this bit is a '1', then Interrupter host system interrupt generation is allowed, e.g. the xHC shall issue an interrupt at the next interrupt threshold if the host system interrupt mechanism (e.g. MSI, MSI-X, etc.) is enabled. The interrupt is acknowledged by a host system interrupt specific mechanism. When this register is exposed by a Virtual Function (VF), this bit only enables the set of Interrupters assigned to the selected VF.
1		HCRST	**Host Controller Reset (HCRST).**

Bit(s)	Mnemonic	Name	Description
			This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. When software writes a '1' to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. This bit is set to '0' by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a '0' to this bit. Software shall not set this bit to a '1' when the HCHalted bit in the USBSTS register is a '0'. Attempting to reset an actively running host controller will result in undefined behavior. When this register is exposed by a Virtual Function (VF), this bit only resets the xHC instance presented by the selected.
0		R_S	**Run/Stop (R/S).** '1' = Run. '0' = Stop. When set to a '1', the xHCI proceeds with execution of the schedule. The xHCI continues execution as long as this bit is set to a '1'. When this bit is set to '0', the xHCI completes the current and any actively pipelined transactions on the USB and then halts. The xHCI must halt within 16 microframes after software clears the Run/Stop bit. The HC Halted bit in the USBSTS register indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Softwaremust not write a '1' to this field unless the xHC is in the Halted state (i.e. HCHalted in the USBSTS register is '1'). Doing so will yield undefined results. When this register is exposed by a Virtual Function (VF), this bit only controls the run state of the xHC instance presented by the selected VF.

1A0C0024 USBSTS USB Status 00000801

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8

Name				HCE	CNR	SRE	RSS	SSS
Type				RO	RU	RO	RO	RO
Reset				0	1	0	0	0
Bit	7	6	5	4	3	2	1	0
Name				PCD	EINT	HSE		HCH
Type				W1C	W1C	RO		RO
Reset				0	0	0		1

Bit(s)	Mnemonic	Name	Description
12		HCE	**Host Controller Error (HCE).** 0' = No internal xHC error conditions exist and '1' = Internal xHC error condition. This flag shall be set to indicate that an internal error condition has been detected which requires software to reset and reinitialize the xHC.
11		CNR	**Controller Not Ready (CNR).** '0' = Ready and '1' = Not Ready. Software shall not write any Doorbell or Operational register of the xHC, other than the USBSTS register, until CNR = '0'. This flag is set by the xHC after a Chip Hardware Reset and cleared when the xHC is ready to begin accepting register writes. This flag shall remain cleared ('0') until the next Chip Hardware Reset.
10		SRE	**Save/Restore Error (SRE).** If an error occurs during a Save or Restore operation this bit shall be set to '1'. This bit shall be set to '0' when a Save or Restore operation is initiated or when written with '1'When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the Save/Restore completion status for the selected VF.
9		RSS	**Restore State Status (RSS).** When the Controller Restore State flag in the USBCMD register is written with '1' this bit shall be set to '1' and remain 1 while the xHC restores its internal state. When the Restore State operation is complete, this bit shall be set to '0'. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the restoring the state for the selected VF.
8		SSS	**Save State Status (SSS).** When the Controller Save State flag in the USBCMD register is written with '1' this bit shall be set to '1' and remain 1 while the xHC saves its internal state. When the Save State operation is complete, this bit shall be set to '0'. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this

Bit(s)	Mnemonic	Name	Description
			bit as a function of the saving the state for the selected VF.
4		PCD	**Port Change Detect (PCD).** The xHC sets this bit to a '1' when any port has a change bit transition from a '0' to a '1' or a Force Port Resume bit transition from a '0' to a '1' as a result of a resume detected on a suspended port. This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the xHC, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, over-current change, enable/disable change and connect status change). This bit provides system software an efficient means of determining if there has been Root Hub port activity. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the Root Hub Ports associated with the Device Slots assigned to the selected VF.
3		EINT	**Event Interrupt (EINT).** The xHC sets this bit to '1' when the Interrupt Pending (IP) bit of any Interrupter is transitions from '0' to '1'. Software that uses EINT shall clear it prior to clearing any IP flags. A race condition will occur if software clears the IP flags then clears the EINT flag, and between the operations another IP '0' to '1' transition occurs. In this case the new IP transition will be lost. When this register is exposed by a Virtual Function (VF), this bit is the logical 'OR' of the IP bits for the Interrupters assigned to the selected VF. And it shall be cleared to '0' when all associated interrupter IP bits are cleared, i.e. all the VFs Interrupter Event Ring(s) are empty.
2		HSE	**Host System Error (HSE).** The xHC sets this bit to '1' when a serious error is detected, either internal to the xHC or during a host system access involving the xHC module. (In a PCI system, conditions that set this bit to '1' include PCI Parity error, PCI Master Abort, and PCI Target Abort.) When this error occurs, the xHC clears the Run/Stop bit in the USBCMD register to prevent further execution of the scheduled TDs. If the HSEE bit in the USBCMD register is a '1', the xHC shall also assert out-of-band error signaling to the host. When this register is exposed by a Virtual Function (VF), the assertion of this bit affects all VFs and reflects the Host System Error state of the Physical Function (PF0).
0		HCH	**HCHalted (HCH).** This bit is a '0' whenever the Run/Stop bit is a '1'. The xHC sets this bit to '1' after it has stopped executing as a result of the Run/Stop bit being set to '0', either by

Bit(s)	Mnemonic	Name	Description
			software or by the xHC hardware (e.g. internal error). When this register is exposed by a Virtual Function (VF), this bit only reflects the Halted state of the xHC instance presented by the selected VF.

1A0C0028 PAGESIZE Page Size 00000001

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name	PAGESIZE							
Type	RO							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	PAGESIZE							
Type	RO							
Reset	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
15:0		PAGESIZE	**Page Size.** Default = Implementation defined. This field defines the page size supported by the xHC implementation. This xHC supports a page size of 2^(n+12) if bit n is Set. For example, if bit 0 is Set, the xHC supports 4k byte page sizes. For a Virtual Function, this register reflects the page size selected in the System Page Size field of the SR-IOV Extended Capability structure. For the Physical Function 0, this register reflects the implementation dependent default xHC page size. Various xHC resources reference PAGESIZE to describe their minimum alignment requirements. The maximum possible page size is 128M.

1A0C0034 DNCTRL Device Notification Control 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name	DNCTRL							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	DNCTRL							
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		DNCTRL	**Notification Enable (No-N15).** When a Notification Enable bit is set, a Device Notification Event will be generated when a Device Notification Transaction Packet is received with the matching value in the Notification Type field. For example, setting N1 to '1' enables Device Notification Event generation if a Device Notification TP is received with its Notification Type field set to '1' (FUNCTION_WAKE), etc.

1A0C0038 CRCR1 Command Ring Control 1 00000000

Bit	31	30	29	28	27	26	25	24
Name	CRP_Lo							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	CRP_Lo							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	CRP_Lo							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Name	CRP_Lo				CRR	CA	CS	RCS
Type	WO				RO	WO	WO	WO
Reset	0	0			0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:6		CRP_Lo	**Command Ring Pointer.** Default = '0'. This field defines high order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Writes to this field are ignored when Command Ring Running (CRR) = '1'. If the CRCR is written while the Command Ring is stopped (CCR = '0'), the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped (CCR = '0') then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. Reading this field always returns '0'.
3		CRR	**Command Ring Running (CRR).** Default = 0. This flag is set to '1' if the Run/Stop (R/S) bit is '1' and the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. It is cleared to '0' when the Command Ring is "stopped" after writing a '1'to the Command Stop (CS) or Command Abort (CA) flags, or if the R/S bit is cleared to '0'.
2		CA	**Command Abort (CA).** Default = '0'. Writing a '1' to this bit shall immediately terminate the currently executing command, stop the Command Ring, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped. Refer to section 4.6.1.2 for more information on aborting a command. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = '0'. Reading this bit always returns '0'.
1		CS	**Command Stop (CS).**

Bit(s)	Mnemonic	Name	Description
			Default = '0'. Writing a '1' to this bit shall stop the operation of the Command Ring after the completion of the currently executing command, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped and the Command TRB Pointer set to the current value of the Command Ring Dequeue Pointer. Refer to section 4.6.1.1 for more information on stopping a command. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = '0'. Reading this bit shall always return '0'.
0		RCS	**Ring Cycle State (RCS).** This bit identifies the value of the xHC Consumer Cycle State (CCS) flag for the TRB referenced by the Command Ring Pointer. Refer to section 4.9.3 for more information. Writes to this flag are ignored if Command Ring Running (CRR) is '1'. If the CRCR is written while the Command Ring is stopped (CRR = '0'), then the value of this flag shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped (CRR = '0'), then the Command Ring will begin fetching Command TRBs using the current value of the internal Command Ring CCS flag. Reading this flag always returns '0'.

1A0C003C CRCR2 Command Ring Control 2 00000000

Bit	31	30	29	28	27	26	25	24
Name	CRP_Hi							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	CRP_Hi							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8

Name	CRP_Hi							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	CRP_Hi							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CRP_Hi	**Command Ring Pointer.** Default = '0'. This field defines high order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Writes to this field are ignored when Command Ring Running (CRR) = '1'. If the CRCR is written while the Command Ring is stopped (CCR = '0'), the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped (CCR = '0') then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. Reading this field always returns '0'.

1A0C0050 DCBAAP_LO Device Context Base Address Array Pointer Lo 00000000

Bit	31	30	29	28	27	26	25	24
Name	DCBAAP_Lo							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	DCBAAP_Lo							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	DCBAAP_Lo							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	DCBAAP_Lo							

Type	RW							
Reset	0	0						

Bit(s)	Mnemonic	Name	Description
31:6		DCBAAP_Lo	**Device Context Base Address Array Pointer.** Default = '0'. This field defines high order bits of the 64-bit base address of the Device Context Pointer Array table. A table of address pointers that reference Device Context structures for the devices attached to the host.

1A0C0054 DCBAAP_HI Device Context Base Address Array Pointer High 00000000

Bit	31	30	29	28	27	26	25	24
Name	**DCBAAP_Hi**							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	**DCBAAP_Hi**							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	**DCBAAP_Hi**							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	**DCBAAP_Hi**							
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DCBAAP_Hi	**Device Context Base Address Array Pointer.** This field defines [63:32] bits of the 64-bit base address of the Device Context Pointer Array table. A table of address pointers that reference Device Context structures for the devices attached to the host.

1A0C0058 CONFIG Configure 00000000

Bit	31	30	29	28	27	26	25	24

Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	**MaxSlotsEn**							
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		MaxSlotsEn	**Max Device Slots Enabled (MaxSlotsEn).** Default = '0'. This field specifies the maximum number of enabled Device Slots. Valid values are in the range of 0 to MaxSlots. Enabled Devices Slots are allocated contiguously. e.g. A value of 16 specifies that Device Slots 1 to 16 are active. A value of '0' disables all Device Slots. A disabled Device Slot shall not respond to Doorbell Register references. This field shall not be modified if the xHC is running (Run/Stop (R/S) = '1').

1A0C0500 SUPP_PTCL_REG1 xHCI Supported Protocol Capability 1 Register 03000402

Bit	31	30	29	28	27	26	25	24
Name	**Revision_Major**							
Type	RO							
Reset	0	0	0	0	0	0	1	1
Bit	23	22	21	20	19	18	17	16
Name	**Revision_Minor**							
Type	RO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	**Next_Capability_Pointer**							

Type	RO							
Reset	0	0	0	0	0	1	0	0
Bit	7	6	5	4	3	2	1	0
Name	**Capability_ID**							
Type	RO							
Reset	0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:24		Revision_Major	**Major Revision.** Major Specification Release Number in Binary-Coded Decimal (i.e., version 3.x is 03h). This field identifies the major release number component of the specification with which the xHC is compliant.
23:16		Revision_Minor	**Minor Revision.** Minor Specification Release Number in Binary-Coded Decimal (i.e., version x.10 is 10h). This field identifies the minor release number component of the specification with which the xHC is compliant.
15:8		Next_Capability_Pointer	**Next Capability Pointer.** This field indicates the location of the next capability with respect to the effective address of this capability. Refer to Table 137 for more information on this field.
7:0		Capability_ID	**Capability ID.** Refer to Table 138 for the value that identifies the capability as Supported Protocol.

1A0C0504 SUPP_PTCL_REG2 xHCI Supported Protocol Capability 2 Register 20425355

Bit	31	30	29	28	27	26	25	24
Name	**Name_String**							
Type	RO							
Reset	0	0	1	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Name	Name_String							
Type	RO							
Reset	0	1	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8
Name	Name_String							
Type	RO							
Reset	0	1	0	1	0	0	1	1
Bit	7	6	5	4	3	2	1	0
Name	Name_String							
Type	RO							
Reset	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
31:0		Name_String	**Name String.** This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined. Allowed characters are: alphanumeric, space, and underscore. Alpha characters are case sensitive. Refer to Table 145 for defined values.

1A0C0508 SUPP_PTCL_REG3 xHCI Supported Protocol Capability 3 Register 00000201

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name						IHI	HSO	L1C
Type						RO	RO	RO
Reset						0	0	0
Bit	15	14	13	12	11	10	9	8
Name	Compatible_Port_Count							
Type	RO							
Reset	0	0	0	0	0	0	1	0
Bit	7	6	5	4	3	2	1	0
Name	Compatible_Port_Offset							
Type	RO							

Reset	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
18		IHI	**Integrated Hub Implemented (IHI).** Default = Implementation dependent. This field only applies to the USB2 protocol. If this bit is cleared to '0', the Root Hub to External xHC port mapping adheres to the default mapping described in section 4.24.2.1. If this bit is set to '1', the Root Hub to External xHC port mapping does not adhere to the default mapping described in section 4.24.2.1, and an ACPI or other mechanism is required to define the mapping.
17		HSO	**High-speed Only (HSO).** Default = Implementation dependent. This field only applies to the USB2 protocol. If this bit is set to '0', the USB2 ports described by this capability are Low-, Full-, and High-speed capable. If this bit is set to '1', the USB2 ports described by this capability are High-speed only, e.g. the ports don't support Low- or Full-speed operation. High-speed only implementations may introduce a "Tier mismatch", refer to section 4.24.2 for more information.
16		L1C	**L1 Capability (L1C).** Default = Implementation dependent. This field only applies to the USB2 protocol. If this bit is set to '1' the xHC supports the USB2 Link Power Management L1 (Sleep) state and the associated USB2 protocol fields as defined in the PORTSC and USB2 PORTPMSC registers are valid, specifically USB2 protocol functionality of the PLS and PLC fields in the PORTSC register, and the fields of the USB2 PORTPMSC register. Note that software is prohibited from using the PLS field initiate a transition to an L1 state or

Bit(s)	Mnemonic	Name	Description
			using the USB2 PORTPMSC fields unless this bit is set to '1'.
15:8		Compatible_Port_Count	**Compatible Port Count.** This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are 1 to MaxPorts.
7:0		Compatible_Port_Offset	**Compatible Port Offset.** This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are '1' to MaxPorts.

1A0C0510 SUPP_PTCL_REG4 xHCI Supported Protocol Capability 1 Register 02000002

Bit	31	30	29	28	27	26	25	24
Name	Revision_Major							
Type	RO							
Reset	0	0	0	0	0	0	1	0
Bit	23	22	21	20	19	18	17	16
Name	Revision_Minor							
Type	RO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	Next_Capability_Pointer							
Type	RO							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	Capability_ID							
Type	RO							
Reset	0	0	0	0	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:24		Revision_Major	**Major Revision.** Major Specification Release Number in Binary-Coded Decimal (i.e.,

Bit(s)	Mnemonic	Name	Description
			version 3.x is 03h). This field identifies the major release number component of the specification with which the xHC is compliant.
23:16		Revision_Minor	**Minor Revision.** Minor Specification Release Number in Binary-Coded Decimal (i.e., version x.10 is 10h). This field identifies the minor release number component of the specification with which the xHC is compliant.
15:8		Next_Capability_Pointer	**Next Capability Pointer.** This field indicates the location of the next capability with respect to the effective address of this capability. Refer to Table 137 for more information on this field.
7:0		Capability_ID	**Capability ID.** Refer to Table 138 for the value that identifies the capability as Supported Protocol.

1A0C0514 SUPP_PTCL_REG5 xHCI Supported Protocol Capability 2 Register 20425355

Bit	31	30	29	28	27	26	25	24
Name	Name_String							
Type	RO							
Reset	0	0	1	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	Name_String							
Type	RO							
Reset	0	1	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8
Name	Name_String							
Type	RO							
Reset	0	1	0	1	0	0	1	1
Bit	7	6	5	4	3	2	1	0
Name	Name_String							
Type	RO							

Reset	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
31:0		Name_String	**Name String.** This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined. Allowed characters are: alphanumeric, space, and underscore. Alpha characters are case sensitive. Refer to Table 145 for defined values.

1A0C0518 SUPP_PTCL_REG6 xHCI Supported Protocol Capability 3 Register 00010503

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name						**IHI**	**HSO**	**L1C**
Type						RO	RO	RO
Reset						0	0	1
Bit	15	14	13	12	11	10	9	8
Name	**Compatible_Port_Count**							
Type	RO							
Reset	0	0	0	0	0	1	0	1
Bit	7	6	5	4	3	2	1	0
Name	**Compatible_Port_Offset**							
Type	RO							
Reset	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
18		IHI	**Integrated Hub Implemented (IHI).** Default = Implementation dependent. This field only applies to the USB2 protocol. If this bit is cleared to '0', the Root Hub to External xHC port mapping adheres to the default mapping described in section 4.24.2.1. If this bit is set to '1', the

Bit(s)	Mnemonic	Name	Description
			Root Hub to External xHC port mapping does not adhere to the default mapping described in section 4.24.2.1, and an ACPI or other mechanism is required to define the mapping.
17		HSO	**High-speed Only (HSO).** Default = Implementation dependent. This field only applies to the USB2 protocol. If this bit is set to '0', the USB2 ports described by this capability are Low-, Full-, and High-speed capable. If this bit is set to '1', the USB2 ports described by this capability are High-speed only, e.g. the ports don't support Low- or Full-speed operation. High-speed only implementations may introduce a "Tier mismatch", refer to section 4.24.2 for more information.
16		L1C	**L1 Capability (L1C).** Default = Implementation dependent. This field only applies to the USB2 protocol. If this bit is set to '1' the xHC supports the USB2 Link Power Management L1 (Sleep) state and the associated USB2 protocol fields as defined in the PORTSC and USB2 PORTPMSC registers are valid, specifically USB2 protocol functionality of the PLS and PLC fields in the PORTSC register, and the fields of the USB2 PORTPMSC register. Note that software is prohibited from using the PLS field initiate a transition to an L1 state or using the USB2 PORTPMSC fields unless this bit is set to '1'.
15:8		Compatible_Port_Count	**Compatible Port Count.** This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are 1 to MaxPorts.
7:0		Compatible_Port_Offset	**Compatible Port Offset.**

Bit(s)	Mnemonic	Name	Description
			This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are '1' to MaxPorts.

1A0C0600 MFINDEX Microframe Index 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name			**MICROFRAME_INDEX**					
Type			RO					
Reset			0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	**MICROFRAME_INDEX**							
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13:0		MICROFRAME_INDEX	**Microframe Index.** The value in this register increments at the end of each microframe (e.g. 125us.). Bits [13:3] may be used to determine the current 1ms. Frame Index.

1A0C0620 IMAN Interrupter Management 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								

Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name							**IE**	**IP**
Type							RW	W1C
Reset							0	0

Bit(s)	Mnemonic	Name	Description
1		IE	**Interrupt Enable (IE).** Default = '0'. This flag specifies whether the Interrupter is capable of generating an interrupt. When this bit and the IP bit are set ('1'), the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches '0'. If this bit is '0', then the Interrupter is prohibited from generating interrupts.
0		IP	**Interrupt Pending (IP).** Default = '0'. This flag represents the current state of the Interrupter. If IP = '1', an interrupt is pending for this Interrupter. This flag is set to '1' when IE = '1', the IMODC Interrupt Moderation Counter field = '0' the Event Ring associated with the Interrupter is not empty, and EHB = '0'. A '0' value indicates that no interrupt is pending for the Interrupter. If MSI interrupts are enabled, this flag shall be cleared automatically when the PCI Dword write generated by the Interrupt assertion is complete. If PCI Pin Interrupts are enabled, this flag shall be cleared by software.

1A0C0624 IMOD Interrupter Moderation 00000FA0

Bit	31	30	29	28	27	26	25	24
Name	**IMODC**							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	**IMODC**							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	**IMODI**							

Type	RW							
Reset	0	0	0	0	1	1	1	1
Bit	7	6	5	4	3	2	1	0
Name	**IMODI**							
Type	RW							
Reset	1	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		IMODC	**Interrupt Moderation Counter (IMODC).** Default = undefined. Down counter. Loaded with Interval value whenever IP is cleared to '0', counts down to '0', and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be directly written by software at any time to alter the interrupt rate.
15:0		IMODI	**Interrupt Moderation Interval (IMODI).** Default = '4000'. Minimum inter-interrupt interval. The interval is specified inunit of 256 internal xHC clock cycles. A value of '0' disables interrupt throttling logic and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty.

1A0C0628 ERSTSZ Event Ring Segment Table Size 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name	**ERSTSZ**							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	**ERSTSZ**							
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		ERSTSZ	**Event Ring Segment Table Size.** Default = '0'. This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HSCPARAMS2 register (5.3.4). For Secondary Interrupters: Writing a value of '0' to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of '0' to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled.

1A0C0630 ERSTBA_LO Event Ring Segment Table Base Address Lo 00000000

Bit	31	30	29	28	27	26	25	24
Name	ERSTBA_LO							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	ERSTBA_LO							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	ERSTBA_LO							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	ERSTBA_LO							
Type	RW							
Reset	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
31:4		ERSTBA_LO	**Event Ring Segment Table Base Address Register.** Default = '0'. This field defines the high order bits of the start address of the Event Ring Segment Table.

Bit(s)	Mnemonic	Name	Description
			Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to Figure 20 for more information. This field shall not be modified if HCHalted (HCH) = '0'.

1A0C0634 ERSTBA_HI Event Ring Segment Table Base Address Hi 00000000

Bit	31	30	29	28	27	26	25	24
Name	ERSTBA_HI							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	ERSTBA_HI							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	ERSTBA_HI							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	ERSTBA_HI							
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		ERSTBA_HI	**Event Ring Segment Table Base Address Register.** Default = '0'. This field defines the high order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to Figure 20 for more information. This field shall not be modified if HCHalted (HCH) = '0'.

1A0C0638 ERDP_LO Event Ring Segment Table Base Address Lo 00000000

Bit	31	30	29	28	27	26	25	24
Name	ERDP_LO							

Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	**ERDP_LO**							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	**ERDP_LO**							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	**ERDP_LO**				**EHB**	**DESI**		
Type	RW				W1C	RW		
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:4		ERDP_LO	**Event Ring Dequeue Pointer.** Default = '0'. This field defines the high order bits of the 64-bit address of the current Event Ring Dequeue Pointer.
3		EHB	**Event Handler Busy (EHB).** Default = '0'. This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written. Refer to section 4.17.2 for more information
2:0		DESI	**Dequeue ERST Segment Index (DESI).** Default = '0'. This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that Event Ring Dequeue Pointer resides in.

1A0C063C ERDP_HI Event Ring Segment Table Base Address Hi 00000000

Bit	31	30	29	28	27	26	25	24
Name	**ERDP_HI**							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	**ERDP_HI**							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8

Name	ERDP_HI							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	ERDP_HI							
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		ERDP_HI	**Event Ring Dequeue Pointer.** Default = '0'. This field defines the high order bits of the 64- bit address of the current Event Ring Dequeue Pointer.

1A0C0800 HOST_CMD_DB Host Controller Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24
Name	HOST_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	HOST_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	HOST_DB_TARGET							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		HOST_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid.

Bit(s)	Mnemonic	Name	Description
			If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
7:0		HOST_DB_TARGET	**DB Target.** Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update 3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update ... 30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition 0 Host Controller Command 1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

Bit(s)	Mnemonic	Name	Description

1A0C0804 DEVICE1_DB Device 1 Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24
Name	DEVICE1_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	DEVICE1_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	DEVICE1_DB_TARGET							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DEVICE1_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
7:0		DEVICE1_DB_TARGET	**DB Target.** Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers.

Bit(s)	Mnemonic	Name	Description
			Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update 3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update ... 30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition 0 Host Controller Command 1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

1A0C0808 DEVICE2_DB Device 2 Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24
Name	DEVICE2_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	DEVICE2_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8

Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	DEVICE2_DB_TARGET							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DEVICE2_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
7:0		DEVICE2_DB_TARGET	**DB Target.** Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update 3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update ... 30 EP 15 OUT Enqueue Pointer Update

Bit(s)	Mnemonic	Name	Description
			31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition 0 Host Controller Command 1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

1A0C080C DEVICE3_DB Device 3 Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24
Name	DEVICE3_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	DEVICE3_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	DEVICE3_DB_TARGET							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DEVICE3_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is

Bit(s)	Mnemonic	Name	Description
			responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
7:0		DEVICE3_DB_TARGET	**DB Target.** Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update 3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update ... 30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition 0 Host Controller Command 1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software.

Bit(s)	Mnemonic	Name	Description
			When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

1A0C0810 DEVICE4_DB Device 4 Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24
Name	DEVICE4_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	DEVICE4_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	DEVICE4_DB_TARGET							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DEVICE4_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
7:0		DEVICE4_DB_TARGET	**DB Target.** Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to

Bit(s)	Mnemonic	Name	Description
			Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update 3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update ... 30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition 0 Host Controller Command 1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

1A0C0814 DEVICE5_DB Device 5 Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24
Name	DEVICE5_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	DEVICE5_DB_STREAM_ID							
Type	WO							

Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	DEVICE5_DB_TARGET							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DEVICE5_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
7:0		DEVICE5_DB_TARGET	**DB Target.** Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update 3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update ...

Bit(s)	Mnemonic	Name	Description
			30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition 0 Host Controller Command 1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

1A0C0818 DEVICE6_DB Device 6 Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24
Name	DEVICE6_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	DEVICE6_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	DEVICE6_DB_TARGET							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DEVICE6_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall

Bit(s)	Mnemonic	Name	Description
			be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
7:0		DEVICE6_DB_TARGET	**DB Target - RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers.** Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update 3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update ... 30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition 0 Host Controller Command 1:247 Reserved 248:255 Vendor Defined

Bit(s)	Mnemonic	Name	Description
			This field returns '0' when read and should be treated as "undefined" by software. When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

1A0C081C DEVICE7_DB Device 7 Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24
Name	DEVICE7_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	DEVICE7_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	DEVICE7_DB_TARGET							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DEVICE7_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
7:0		DEVICE7_DB_TARGET	**DB Target.** Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC

Bit(s)	Mnemonic	Name	Description
			notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update 3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update ... 30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition 0 Host Controller Command 1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

1A0C0820 DEVICE8_DB Device 8 Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24
Name	DEVICE8_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16

Name	DEVICE8_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	DEVICE8_DB_TARGET							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DEVICE8_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
7:0		DEVICE8_DB_TARGET	**DB Target.** Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update 3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update

Bit(s)	Mnemonic	Name	Description
			5 EP 2 IN Enqueue Pointer Update ... 30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition 0 Host Controller Command 1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

1A0C0824 DEVICE9_DB Device 9 Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24
Name	DEVICE9_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	DEVICE9_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	DEVICE9_DB_TARGET							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DEVICE9_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
7:0		DEVICE9_DB_TARGET	**DB Target.** Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update 3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update ... 30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition 0 Host Controller Command

Bit(s)	Mnemonic	Name	Description
			1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

1A0C0828 DEVICE10_DB Device 10 Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24
Name	DEVICE10_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	DEVICE10_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	DEVICE10_DB_TARGET							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DEVICE10_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.

Bit(s)	Mnemonic	Name	Description
7:0		DEVICE10_DB_TARGET	**DB Target.** Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update 3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update ... 30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition 0 Host Controller Command 1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

1A0C082C DEVICE11_DB Device 11 Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24
Name	DEVICE11_DB_STREAM_ID							

Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	**DEVICE11_DB_STREAM_ID**							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	**DEVICE11_DB_TARGET**							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DEVICE11_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
7:0		DEVICE11_DB_TARGET	**DB Target.** Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update

Bit(s)	Mnemonic	Name	Description
			3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update ... 30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition 0 Host Controller Command 1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

1A0C0830 DEVICE12_DB Device 12 Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24
Name	DEVICE12_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	DEVICE12_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	DEVICE12_DB_TARGET							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DEVICE12_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
7:0		DEVICE12_DB_TARGET	**DB Target.** Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update 3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update ... 30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition

Bit(s)	Mnemonic	Name	Description
			0 Host Controller Command 1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

1A0C0834 DEVICE13_DB Device 13 Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24
Name	DEVICE13_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	DEVICE13_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	DEVICE13_DB_TARGET							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DEVICE13_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands.

Bit(s)	Mnemonic	Name	Description
			This field returns '0' when read.
7:0		DEVICE13_DB_TARGET	**DB Target.** Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update 3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update ... 30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition 0 Host Controller Command 1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

1A0C0838 DEVICE14_DB Device 14 Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24

Name	DEVICE14_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	DEVICE14_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	DEVICE14_DB_TARGET							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DEVICE14_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
7:0		DEVICE14_DB_TARGET	**DB Target.** Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update

Bit(s)	Mnemonic	Name	Description
			3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update ... 30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition 0 Host Controller Command 1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

1A0C083C DEVICE15_DB Device 15 Doorbell Registers 00000000

Bit	31	30	29	28	27	26	25	24
Name	DEVICE15_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	DEVICE15_DB_STREAM_ID							
Type	WO							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	DEVICE15_DB_TARGET							
Type	WO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		DEVICE15_DB_STREAM_ID	**DB Stream ID.** Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
7:0		DEVICE15_DB_TARGET	**DB Target.** Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) Value Definition 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update 3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update ... 30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) Value Definition

Bit(s)	Mnemonic	Name	Description
			0 Host Controller Command 1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Host Controller Doorbell (0) is written, the DB Stream ID field shall be cleared to '0'.

1A0C0900 HSRAM_DBGCTL Host SRAM Debug Control Register 00000002

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name							**SRAM_DBG_WP**	**SRAM_DBG_EN**
Type							RW	RW
Reset							1	0

Bit(s)	Mnemonic	Name	Description
1		SRAM_DBG_WP	**SRAM Write Protect for Debug Mode** 0: allow SRAM Debug Write 1: prohibit SRAM Debug Write
0		SRAM_DBG_EN	**SRAM Debug Access Enable** 0: SRAM Debug Access is ignored 1: SRAM Debug Access is allowed

Bit(s)	Mnemonic	Name	Description

1A0C0904 HSRAM_DBGMODE Host SRAM Debug Mode Register 00000000

Bit	31	30	29	28	27	26	25	24
Name	SRAM_DBG_MODE							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	SRAM_DBG_MODE							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	SRAM_DBG_MODE							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	SRAM_DBG_MODE							
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		SRAM_DBG_MODE	**Debug mode for host SRAM** Each bit indicates the SRAM debug mode of corresponding SRAM. For each bit, 0: SRAM in normal Mode. HW access is allowed. 1: SRAM in Debug Mode. HW access is prevented. bit[0]: ER SRAM (32x128) bit[1]: CMD SRAM (15x30) bit[2]: EP MAP (480x7) bit[3]: EP Slot (15x41) bit[4]: EP Static (64x75) bit[5]: EP Dynamic (64x51) bit[6]: TRBQ (64x114) bit[7]: USB2_DMA (64x128) bit[8]: SCH3 IN SRAM (256x128)

Bit(s)	Mnemonic	Name	Description
			bit[9]: SCH3 OUT SRAM (256x128) bit[10]: SCH2_0 (256x128) bit[11]: SCH2_1 (256x128) bit[12]: SCH2_2 (256x128) bit[13]: SCH2_3 (256x128) bit[14]: SCH2_4 (256x128) Note: More then one bit can be set to 1'b1 in HSRAM_DBGMODE, but only one of them in HSRAM_DBGSEL can be set to 1'b1.

1A0C0908 HSRAM_DBGSEL Host SRAM Debug Select Register 00000000

Bit	31	30	29	28	27	26	25	24
Name	SRAM_DBG_SEL							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	SRAM_DBG_SEL							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	SRAM_DBG_SEL							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	SRAM_DBG_SEL							
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		SRAM_DBG_SEL	**Debug Select for Host SRAM** Each bit indicates whether the access through HSRAM_DBGADR and HSRAM_DBGDR are targeted to related SRAM. Note: at most one bit in HSRAM_DBGSEL can be set to 1'b1 Note: when a specific bit is set to 1'b1, the related bit in HSRAM_DBGMODE shall be set to 1'b1 too.

Bit(s)	Mnemonic	Name	Description

1A0C090C HSRAM_DBGADR Host SRAM Debug Address Register 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								SRAM_DBG_ADDR
Type								RW
Reset								0
Bit	15	14	13	12	11	10	9	8
Name	SRAM_DBG_ADDR							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	SRAM_DBG_ADDR					SRAM_DBG_DWSEL		
Type	RW					RW		
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16:3		SRAM_DBG_ADDR	**SRAM Address (16-byte access) for Debug Mode** This is equivalent to SRAM Address in HW because the SRAM's width is limit to 192-bit. Because the Host Slave interface is 32-bit, the SRAM_DBG_DWSEL[2:0] decide which 4-byte is read/write through SRAM_DBG_DATA[31:0]
2:0		SRAM_DBG_DWSEL	**SRAM DW Select (6-byte access) for Debug Mode** This 3-bit selects which 6-byte out of the 16-byte indicated by SRAM_DBG_ADDR[13:0] is read/write through SRAM_DBG_DATA[31:0] Note: The constraints on SRAM_DBG_DWSEL[2:0] according to the actual SRAM width in HW shall be followed: - For SRAM with 0 < width <= 32, the valid value of SRAM_DBG_DWSEL[2:0] = 0

Bit(s)	Mnemonic	Name	Description
			- For SRAM with 32 < width <= 64, the valid value of SRAM_DBG_DWSEL[2:0] = 0, 1 - For SRAM with 64 < width <= 96, the valid value of SRAM_DBG_DWSEL[2:0] = 0, 1, 2 - For SRAM with 96 < width <= 128, the valid value of SRAM_DBG_DWSEL[2:0] = 0, 1, 2, 3 - For SRAM with 128 < width <= 160, the valid value of SRAM_DBG_DWSEL[2:0] = 0, 1, 2, 3, 4 - For SRAM with 160 < width <= 192, the valid value of SRAM_DBG_DWSEL[2:0] = 0, 1, 2, 3, 4, 5

1A0C0910 HSRAM_DBGDR Host SRAM Debug Data Register 00000000

Bit	31	30	29	28	27	26	25	24
Name	SRAM_DBG_DATA							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	SRAM_DBG_DATA							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	SRAM_DBG_DATA							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	SRAM_DBG_DATA							
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		SRAM_DBG_DATA	**SRAM Debug Data Register** When Read, need to program HSRAM_DBGADR first and then read HSRAM_DBGDR and the selected SRAM's related 4-byte data is returned. When Write, need to program HSRAM_DBGADR first then read HSRAM_DBGDR and the data is stored to target location at specified address of the selected SRAM

1A0C0920 HSRAM_DELSEL_0 Host SRAM Delay Select 0 0000AAAA

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name	DELSEL_U2DMA_0		DELSEL_TRBQ		DELSEL_EP_DYN		DELSEL_EP_STA	
Type	RW		RW		RW		RW	
Reset	1	0	1	0	1	0	1	0
Bit	7	6	5	4	3	2	1	0
Name	DELSEL_EP_SLT		DELSEL_EP_MAP		DELSEL_CMD		DELSEL_ER	
Type	RW		RW		RW		RW	
Reset	1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
15:14		DELSEL_U2DMA_0	**DELSEL for USB2 DMA SRAM**
13:12		DELSEL_TRBQ	**DELSEL for CMD SRAM**
11:10		DELSEL_EP_DYN	**DELSEL for EP Dynamic SRAM**
9:8		DELSEL_EP_STA	**DELSEL for EP Static SRAM**
7:6		DELSEL_EP_SLT	**DELSEL for EP SLOT SRAM**
5:4		DELSEL_EP_MAP	**DELSEL for EP MAP SRAM**
3:2		DELSEL_CMD	**DELSEL for CMD SRAM SRAM**
1:0		DELSEL_ER	**DELSEL for ER SRAM**

1A0C0924 HSRAM_DELSEL_1 Host SRAM Delay Select 1 00002AAA

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								

Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name			DELSEL_SCH2_4		DELSEL_SCH2_3		DELSEL_SCH2_2	
Type			RW		RW		RW	
Reset			1	0	1	0	1	0
Bit	7	6	5	4	3	2	1	0
Name	DELSEL_SCH2_1		DELSEL_SCH2_0		DELSEL_SCH3_OUT		DELSEL_SCH3_IN	
Type	RW		RW		RW		RW	
Reset	1	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
13:12		DELSEL_SCH2_4	**DELSEL for USB2 Port 4 Scheduler SRAM**
11:10		DELSEL_SCH2_3	**DELSEL for USB2 Port 3 Scheduler SRAM**
9:8		DELSEL_SCH2_2	**DELSEL for USB2 Port 2 Scheduler SRAM**
7:6		DELSEL_SCH2_1	**DELSEL for USB2 Port 1 Scheduler SRAM**
5:4		DELSEL_SCH2_0	**DELSEL for USB2 Port 0 Scheduler SRAM**
3:2		DELSEL_SCH3_OUT	**DELSEL for USB3 OUT Scheduler SRAM**
1:0		DELSEL_SCH3_IN	**DELSEL for USB3 IN Scheduler SRAM**

1A0C092C AXI_ID AXI DMA ID configuration register 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	AXI_DMA_MAS_ID				AXI_DMA_DATA_ID			
Type	RW				RW			
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:4		AXI_DMA_MAS_ID	**AXI ID configration for master**
3:0		AXI_DMA_DATA_ID	**AXI ID configration for data TX/RX**

1A0C0930 LS_EOF Low Speed EOF Start Offset 07130089

Bit	31	30	29	28	27	26	25	24
Name						**LS_EOF_UFRAME**		
Type						RW		
Reset						1	1	1
Bit	23	22	21	20	19	18	17	16
Name				**LS_EOF_BANK**				
Type				RW				
Reset				1	0	0	1	1
Bit	15	14	13	12	11	10	9	8
Name								**LS_EOF_OFFSET**
Type								RW
Reset								0
Bit	7	6	5	4	3	2	1	0
Name	**LS_EOF_OFFSET**							
Type	RW							
Reset	1	0	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
26:24		LS_EOF_UFRAME	**Low Speed EOF uFrame** The LS is using 1ms, 8 micro frame, as frame period. This register set the micro number that LSEOF asserts
20:16		LS_EOF_BANK	**Low Speed EOF Bank** One micro frame, 125 us, is divided into 20 banks which is (INIT_FRMCNT_LEV1_FULL_RANGE + 1) cycles of frmcnt_ck for each. This register set the bank that LSEOF asserts. The valid value can be 0 to 19.
8:0		LS_EOF_OFFSET	**Low Speed EOF Offset** This register set the offset within a bank that LSEOF asserts. The valid value is 0~INIT_FRMCNT_LEV1_FULL_RANGE.

Bit(s)	Mnemonic	Name	Description

1A0C0934 FS_EOF Full Speed EOF Start Offset 070A002E

Bit	31	30	29	28	27	26	25	24
Name						FS_EOF_UFRAME		
Type						RW		
Reset						1	1	1
Bit	23	22	21	20	19	18	17	16
Name				FS_EOF_BANK				
Type				RW				
Reset				0	1	0	1	0
Bit	15	14	13	12	11	10	9	8
Name								FS_EOF_OFFSET
Type								RW
Reset								0
Bit	7	6	5	4	3	2	1	0
Name	FS_EOF_OFFSET							
Type	RW							
Reset	0	0	1	0	1	1	1	0

Bit(s)	Mnemonic	Name	Description
26:24		FS_EOF_UFRAME	**Full Speed EOF uFrame** The FS is using 1ms, 8 micro frame, as frame period. This register set the micro number that FSEOF asserts
20:16		FS_EOF_BANK	**Full Speed EOF Bank** One micro frame, 125 us, is divided into 20 banks which is (INIT_FRMCNT_LEV1_FULL_RANGE + 1) cycles of frmcnt_ck for each. This register set the bank that FSEOF asserts. The valid value can be 0 to 19.
8:0		FS_EOF_OFFSET	**Full Speed EOF Offset** This register set the offset within a bank that FSEOF asserts. The valid value is 0~INIT_FRMCNT_LEV1_FULL_RANGE.

1A0C0938 SYNC_HS_EOF Synchronous High Speed EOF Start Offset 00040000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name				SYNC_HS_EOF_BANK				
Type				RW				
Reset				0	0	1	0	0
Bit	15	14	13	12	11	10	9	8
Name								SYNC_HS_EOF_OFFSET
Type								RW
Reset								0
Bit	7	6	5	4	3	2	1	0
Name	SYNC_HS_EOF_OFFSET							
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:16		SYNC_HS_EOF_BANK	**Synchronous High Speed EOF Bank** One micro frame, 125 us, is divided into 20 banks which is (INIT_FRMCNT_LEV1_FULL_RANGE + 1) cycles of frmcnt_ck for each. This register set the bank that Synchronous HSEOF asserts. The valid value can be 0 to 19.
8:0		SYNC_HS_EOF_OFFSET	**Synchronous High Speed EOF Offset** This register set the offset within a bank that Synchronous HSEOF asserts. The valid value is 0~INIT_FRMCNT_LEV1_FULL_RANGE.

1A0C093C SS_EOF Super Speed EOF Start Offset 00000078

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name				SS_EOF_BANK				
Type				RW				

Reset				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								**SS_EOF_OFFSET**
Type								RW
Reset								0
Bit	7	6	5	4	3	2	1	0
Name	**SS_EOF_OFFSET**							
Type	RW							
Reset	0	1	1	1	1	0	0	0

Bit(s)	Mnemonic	Name	Description
20:16		SS_EOF_BANK	**Super Speed EOF Bank** One micro frame, 125 us, is divided into 20 banks which is (INIT_FRMCNT_LEV1_FULL_RANGE + 1) cycles of frmcnt_ck for each. This register set the bank that SSEOF asserts. The valid value can be 0 to 19.
8:0		SS_EOF_OFFSET	**Super Speed EOF Offset** This register set the offset within a bank that SSEOF asserts. The valid value is 0~INIT_FRMCNT_LEV1_FULL_RANGE.

1A0C0940 SOF_OFFSET SOF Offset 00000000

Bit	31	30	29	28	27	26	25	24
Name	**SOF_U2_PORT5**				**SOF_U2_PORT4**			
Type	RW				RW			
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	**SOF_U2_PORT3**				**SOF_U2_PORT2**			
Type	RW				RW			
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	**SOF_U2_PORT1**				**SOF_U2_PORT0**			
Type	RW				RW			
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	**SOF_U3_PORT1**				**SOF_U3_PORT0**			
Type	RW				RW			
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		SOF_U2_PORT5	**USB2 PORT 5 SOF Bank** This register configures the offset bank for USB2 Port 5 SOF. The valid value can be 0 to 14.
27:24		SOF_U2_PORT4	**USB2 PORT 4 SOF Bank** This register configures the offset bank for USB2 Port 4 SOF. The valid value can be 0 to 14.
23:20		SOF_U2_PORT3	**USB2 PORT 3 SOF Bank** This register configures the offset bank for USB2 Port 3 SOF. The valid value can be 0 to 14.
19:16		SOF_U2_PORT2	**USB2 PORT 2 SOF Bank** This register configures the offset bank for USB2 Port 2 SOF. The valid value can be 0 to 14.
15:12		SOF_U2_PORT1	**USB2 PORT 1 SOF Bank** This register configures the offset bank for USB2 Port 1 SOF. The valid value can be 0 to 14.
11:8		SOF_U2_PORT0	**USB2 PORT 0 SOF Bank** This register configures the offset bank for USB2 Port 0 SOF. The valid value can be 0 to 14.
7:4		SOF_U3_PORT1	**USB3 PORT 1 SOF Bank** This register configures the offset bank for USB3 Port 1 SOF. The valid value can be 0 to 14.
3:0		SOF_U3_PORT0	**USB3 PORT 0 SOF Bank** This register configures the offset bank for USB3 Port 0 SOF. The valid value can be 0 to 14.

1A0C0944 HFCNTR_CFG Host Frame Counter Configuration 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8

Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name								FCNTR_DIS
Type								RW
Reset								0

Bit(s)	Mnemonic	Name	Description
0		FCNTR_DIS	**Frame Counter Disable** When this bit is set, the frame counter will stop counting.

1A0C0948 XACT3_CFG Super Speed Transaction Configuration 01010020

Bit	31	30	29	28	27	26	25	24
Name								XACT3_PM_TRANS_EN
Type								RW
Reset								1
Bit	23	22	21	20	19	18	17	16
Name							XACT3_ISO_OUT_TX_ZLP_DIS	XACT3_ISO_IN_CRC_CHK_DIS
Type							RW	RW
Reset							0	1
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	XACT3_TMOUT							
Type	RW							
Reset	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24		XACT3_PM_TRANS_EN	**Xactor3 Power Mode transfer enable**

Bit(s)	Mnemonic	Name	Description
			When set to 1'b1, if there were residual transactions that not transfer to device in power mode, the Xactor3 will let the link go back to U0 and transfer them. When set to 1'b0, the Xactor3 will not transfer the residual transaction when in power mode.
17		XACT3_ISO_OUT_TX_ZLP_DIS	**Xactor3 Isochronous OUT TX ZLP Disable** When set to 1'b1, the Xactor3 does not TX ZLP for Isochronous OUT endpoint. When set to 1'b0, the Xactor3 can TX ZLP for Isochronous OUT endpoint.
16		XACT3_ISO_IN_CRC_CHK_DIS	**Xactor3 Isochronous IN CRC Check Disable** When set to 1'b1, the CRC Error of Isoch IN DP is ignored When set to 1'b0, the CRC Error of Isoch IN DP is reported
7:0		XACT3_TMOUT	**USB3 Transactor Timeout Value** This register controls the timeout value of XACT3. Unit in us.

1A0C094C XACT2_CFG USB2 Transaction Configuration 00000001

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name						XACT2_ISO_OUT_TX_ZLP_DIS	XACT2_SPLIT_ISO_IN_CRC_CHK_DIS	XACT2_NON_SPLIT_ISO_IN_CRC_CHK_DIS

Type						RW	RW	RW
Reset						0	0	1

Bit(s)	Mnemonic	Name	Description
2		XACT2_ISO_OUT_TX_ZLP_DIS	**Xactor2 Isochronous OUT TX ZLP Disable** When set to 1'b1, the Xactor3 does not TX ZLP for Isochronous OUT endpont. When set to 1'b0, the Xactor3 can TX ZLP for Isochronous OUT endpont.
1		XACT2_SPLIT_ISO_IN_CRC_CHK_DIS	**Xactor2 non Split Isochronous IN CRC Check Disable** When set to 1'b1, the CRC Error of Isoch IN DP is ignored When set to 1'b0, the CRC Error of Isoch IN DP is reported
0		XACT2_NON_SPLIT_ISO_IN_CRC_CHK_DIS	**Xactor2 non Split Isochronous IN CRC Check Disable** When set to 1'b1, the CRC Error of Isoch IN DP is ignored When set to 1'b0, the CRC Error of Isoch IN DP is reported

1A0C0950 HDMA_CFG Host DMA Configuration 01020200

Bit	31	30	29	28	27	26	25	24
Name								**DYN_DRAM_CG_EN**
Type								RW
Reset								1
Bit	23	22	21	20	19	18	17	16
Name		**DMAU2_LIMITER**			**DMAU2_BURST**		**DMAU2_BUFFERABLE**	**DMAU2_FAKE**
Type		RW			RW		RW	RW
Reset		0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8
Name	**DMAW_LAST_NONBUF**	**DMAW_LIMITER**			**DMAW_BURST**		**DMAW_BUFFERABLE**	**DMAW_FAKE**
Type	RW	RW			RW		RW	RW
Reset	0	0	0	0	0	0	1	0

Bit	7	6	5	4	3	2	1	0
Name		DMAR_LIMITER			DMAR_BURST			DMAR_FAKE
Type		RW			RW			RW
Reset		0	0	0	0	0		0

Bit(s)	Mnemonic	Name	Description
24		DYN_DRAM_CG_EN	**Dynamic DRAM Clock Gating Enable** 0: Dynamic clock gating is disabled. The clock gating on dram_ck is controlled by all root hub ports' link state 1: Dynamic clock gating is enabled. The clock gating is controll by the related dma requests
22:20		DMAU2_LIMITER	**DMA U2 Limiter Configuration** This register configures the number of DRAM cycle between two DMA request. 0: at least 1T 1: at least 2T 2: at least 4T 3: at least 8T 4: at least 16T 5: at least 32T 6: at least 64T 7: at least 128T
19:18		DMAU2_BURST	**DMA U2 Burst Size Configuraiton** This register configures the maximum burst size per DMA request to DRAM bus. 0: 1024 bytes 1: 512 bytes 2: 256 bytes 3: 128 bytes
17		DMAU2_BUFFERABLE	**DMA U2 Bufferable Configuration** When this bit is set, the DMA U2 write operation is bufferable on target DMA bus

Bit(s)	Mnemonic	Name	Description
16		DMAU2_FAKE	**DMA U2 Fake Configuration** When this bit is set, no data will be moved but DMA returns ack immediately.
15		DMAW_LAST_NONBUF	**DMA Write Last burst Nonbufferable** 0: fully controled by DMAW_BUFFERABLE 1: force nonbufferable when last burst.
14:12		DMAW_LIMITER	**DMA Write Limiter Configuration** This register configures the number of DRAM cycle between two DMA request. 0: at least 1T 1: at least 2T 2: at least 4T 3: at least 8T 4: at least 16T 5: at least 32T 6: at least 64T 7: at least 128T
11:10		DMAW_BURST	**DMA Write Burst Size Configuraiton** This register configures the maximum burst size per DMA request to DRAM bus. 0: 1024 bytes 1: 512 bytes 2: 256 bytes 3: 128 bytes
9		DMAW_BUFFERABLE	**DMA Write Bufferable Configuration** When this bit is set, the DMA write operation is bufferable on target DMA bus
8		DMAW_FAKE	**DMA Write Fake Configuration** When this bit is set, no data will be moved but DMA returns ack immediately.
6:4		DMAR_LIMITER	**DMA Read Limiter Configuration**

Bit(s)	Mnemonic	Name	Description
			This register configures the number of DRAM cycle between two DMA request. 0: at least 1T 1: at least 2T 2: at least 4T 3: at least 8T 4: at least 16T 5: at least 32T 6: at least 64T 7: at least 128T
3:2		DMAR_BURST	**DMA Read Burst Size Configuraiton** This register configures the maximum burst size per DMA request to DRAM bus. 0: 1024 bytes 1: 512 bytes 2: 256 bytes 3: 128 bytes
0		DMAR_FAKE	**DMA Read Fake Configuration** When this bit is set, no data will be moved but DMA returns ack immediately.

1A0C0954 ASYNC_HS_EOF Asynchronous High Speed EOF Start Offset 00020000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name				**ASYNC_HS_EOF_BANK**				
Type				RW				
Reset				0	0	0	1	0
Bit	15	14	13	12	11	10	9	8

Name								ASYNC_HS_EOF_OFFSET
Type								RW
Reset								0
Bit	7	6	5	4	3	2	1	0
Name	ASYNC_HS_EOF_OFFSET							
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20:16		ASYNC_HS_EOF_BANK	**Asynchronous High Speed EOF Bank** One micro frame, 125 us, is divided into 20 banks which is (INIT_FRMCNT_LEV1_FULL_RANGE + 1) cycles of frmcnt_ck for each. This register set the bank that Asynchronous HSEOF asserts. The valid value can be 0 to 19.
8:0		ASYNC_HS_EOF_OFFSET	**Asynchronous High Speed EOF Offset** This register set the offset within a bank that Asynchronous HSEOF asserts. The valid value is 0~INIT_FRMCNT_LEV1_FULL_RANGE.

1A0C0958 AXI_WR_DMA_CFG AXI WR DMA configuration register. 00401810

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name	axi_wr_outstand_num				axi_wr_coherence	axi_wr_iommu	axi_wr_cacheable	axi_wr_ultra_en
Type	RW				RW	RW	RW	RW
Reset	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	axi_wr_ultra_num							
Type	RW							
Reset	0	0	0	1	1	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	axi_wr_pre_ultra_num							
Type	RW							
Reset	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:20		axi_wr_outstand_num	**The max outstand request for AXI DMA** valid value : 1 ~ 4 The register are only for AXI DMA.
19		axi_wr_coherence	**AXI coherence capability.** 0 : disalbe 1 : enable
18		axi_wr_iommu	**AXI iommu capability.** 0 : disalbe 1 : enable
17		axi_wr_cacheable	**AXI cache capability.** 0 : disalbe 1 : enable
16		axi_wr_ultra_en	**AXI WR channel ultra capability which is used to indicate async fifo in AXI DMA is almost full.** 0 : disalbe 1 : enable
15:8		axi_wr_ultra_num	**The high threshold to assert ultra signal. The valid can't be smaller than pre_ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert ultra.** valid : 0 ~ 15
7:0		axi_wr_pre_ultra_num	**The low threshold to assert pre_ultra signal. The valid can't be larger than ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert pre_ultra.** valid : 0 ~ 15

1A0C095C AXI_RD_DMA_CFG AXI RD DMA configuration register. 00401810

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name	**axi_rd_outstand_num**				**axi_rd_coherence**	**axi_rd_iommu**	**axi_rd_cacheable**	**axi_rd_ultra_en**

Type	RW				RW	RW	RW	RW
Reset	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	axi_rd_ultra_num							
Type	RW							
Reset	0	0	0	1	1	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	axi_rd_pre_ultra_num							
Type	RW							
Reset	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:20		axi_rd_outstand_num	**The max outstand request for AXI DMA** valid value : 1 ~ 4 The register are only for AXI DMA.
19		axi_rd_coherence	**AXI coherence capability.** 0 : disalbe 1 : enable
18		axi_rd_iommu	**AXI iommu capability.** 0 : disalbe 1 : enable
17		axi_rd_cacheable	**AXI cache capability.** 0 : disalbe 1 : enable
16		axi_rd_ultra_en	**AXI RD channel ultra capability which is used to indicate async fifo in AXI DMA is almost empty.** 0 : disalbe 1 : enable
15:8		axi_rd_ultra_num	**The high threshold to assert ultra signal. The valid can't be smaller than pre_ultra_num. When available buffer space is more than the threshold, AXI DMA would assert ultra.** valid : 0 ~ 15
7:0		axi_rd_pre_ultra_num	**The low threshold to assert pre_ultra signal. The valid can't be larger than ultra_num. When available buffer space is more than the threshold, AXI DMA would assert pre_ultra.**

Bit(s)	Mnemonic	Name	Description
			valid : 0 ~ 15

1A0C0960 HSCH_CFG1 Host Scheduler Configuration Register 1 003FDC20

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name			SCH3_RX_FIFO_DEPTH		SCH3_TX_FIFO_DEPTH		SCH2_FIFO_DEPTH	
Type			RW		RW		RW	
Reset			1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8
Name	UPDATE_XACT_NUMP_INTIME	SCH_DIS_INT_CS_NYET_RST_BEC	PORT_IDLE_WITH_INT	SCH3_INT_PING_TD_CHK	SCH2_INT_PING_TD_CHK	SCH2_BULK_PING_TD_CHK	SCH_SPLIT_ISO_IN_RETRY_OPT	
Type	RW	RW	RW	RW	RW	RW	RW	
Reset	1	1	0	1	1	1	0	0
Bit	7	6	5	4	3	2	1	0
Name	SCH_IN_ACK_RTY_EN	SCH_ASYNC_NEXT_FRAME	OUT_NUMP_REF_DYN	OUT_NUMP_REF	BURST_IN_OFF	BURST_TD_OFF	BURST_OUT_OFF	PORT_IDLE_WITH_ISO
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21:20		SCH3_RX_FIFO_DEPTH	**Scheduler 3 RX Data FIFO Depth** This register control the available RX FIFO depth in Scheduler3 2'b11: 4KByte 2'b10: 3KByte 2'b01: 2KByte 2'b00: 1KByte Note: the default value matches the actual SRAM size. SW can only program this register with size smaller or equal to SRAM size.

Bit(s)	Mnemonic	Name	Description
19:18		SCH3_TX_FIFO_DEPTH	**Scheduler 3 TX Data FIFO Depth** This register control the available TX FIFO depth in Scheduler3 2'b11: 4KByte 2'b10: 3KByte 2'b01: 2KByte 2'b00: 1KByte Note: the default value matches the actual SRAM size. SW can only program this register with size smaller or equal to SRAM size.
17:16		SCH2_FIFO_DEPTH	**Scheduler 2 Data FIFO Depth** This register control the available FIFO depth in Scheduler2 2'b11: 4KByte 2'b10: 3KByte 2'b01: 2KByte 2'b00: 1KByte Note: the default value matches the actual SRAM size. SW can only program this register with size smaller or equal to SRAM size.
15		UPDATE_XACT_NUMP_INTIME	**Scheduler 3 Bulk IN transaction update NumP in Time** Update xact3's NumP in time when do the Bulk IN transaction for performance improve 1'b1: Enable, default 1'b0: Disable
14		SCH_DIS_INT_CS_NYET_RST_BEC	**Scheduler 2 Disable NYET Reset BEC When Interrupt Split CS** 1'b1: disable, default 1'b0: not disable
13		PORT_IDLE_WITH_INT	**Port Idle with INT Configuration** When this bit is set, the port_idle signal to transactor will gated with Interrupt endpoint active flags.
12		SCH3_INT_PING_TD_CHK	**Scheduler 3 Interrupt Pseudo-PrePing TD Check**

Bit(s)	Mnemonic	Name	Description
			1'b0: When Pseudo-PrePing is indicated by EP lookup, SCH3 directly wake link from U1/U2 to U0 whthout checking if there is TD to serve 1'b1: When Pseudo-PrePing is indicated by EP lookup, SCH3 only wake link from U1/U2 to U0 when the check result is with TD to serve
11		SCH2_INT_PING_TD_CHK	**Scheduler 2 Interrupt Pseudo-PrePing TD Check** 1'b0: When Pseudo-PrePing is indicated by EP lookup, SCH2 directly wake link from U1/U2 to U0 whthout checking if there is TD to serve 1'b1: When Pseudo-PrePing is indicated by EP lookup, SCH2 only wake link from U1/U2 to U0 when the check result is with TD to serve
10		SCH2_BULK_PING_TD_CHK	**Scheduler 2 Bulk Pseudo-PrePing TD Check** 1'b0: When and OUT EP is with flow control, PING is sent without checking if there is OUT TD first. 1'b1: When and OUT EP is with flow control, PING is sent only when checking shows that there is OUT TD.
9:8		SCH_SPLIT_ISO_IN_RETRY_OPT	**Scheduler 2 Split Iso In Retry Option** 2'b00: Whe transaction Error, retry 3 times 2'b01: Never Retry when transaction Error 2'b10:Infinitely retry until EOF when transaction Error 2'b11: Reserved
7		SCH_IN_ACK_RTY_EN	**Scheduler Send Ack with Retry set in 2nd Ack for IN Transfer** When this bit is set, the scheduler will request XACT3 to send Ack(NumP!=0, Retry=1) to resume IN transaction when this endpoint suffered DPP error by sending Aci(NumP=0, Retry=1) earlier
6		SCH_ASYNC_NEXT_FRAME	**Schedule Asynchrous EP in next micro Frame** When this bit is set, the scheduler will power down if no more asynchronous EP is active in current micro frame. The actived asynchronous EP might be delay serviced in the next micro frame.
5		OUT_NUMP_REF_DYN	**OUT Nump Reference Dynamically Configuration** When this bit is set, SSUSB OUT scheduler will reference the NUMP value in every ACK and not exceed device's capability dynamically.

Bit(s)	Mnemonic	Name	Description
4		OUT_NUMP_REF	**OUT Nump Reference Configuration** When this bit is set, SSUSB OUT scheduler will reference the NUMP value of last ERDY to determine the number of packets in this opportunity. It only applies to asynchronous endpoints.
3		BURST_IN_OFF	**Burst IN Off Configuration** When this bit is set, SSUSB IN scheduler will disable burst capability and launch IN ACK with NUMP = 1 only.
2		BURST_TD_OFF	**Burst TD Off Configuration** When this bit is set, SSUSB OUT scheduler will disable burst TD capability of bulk endpoint. It will end this endpoint service when current TD is finished no matter next endpoint is available.
1		BURST_OUT_OFF	**Burst OUT Off Configuration** When this bit is set, SSUSB OUT scheduler will disable burst capability and launch next OUT until ACK is returned.
0		PORT_IDLE_WITH_ISO	**Port Idle with ISO Configuration** When this bit is set, the port_idle signal to transactor will gated with isochronous endpoint active flags.

1A0C0964 CMD_CFG Command Configuration 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name								PARAM_ERR_CHK_DIS

Type								RW
Reset								0

Bit(s)	Mnemonic	Name	Description
0		PARAM_ERR_CHK_DIS	**Disable Parameter Error Check** When this bit is set, the parameter error check in command ring is disabled. Whe this be is not set, the parameter error check in command ring is enabled.

1A0C0968 EP_CFG Endpoint Status Configuration 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name								**HUB_TTT_EN**
Type								RW
Reset								0

Bit(s)	Mnemonic	Name	Description
0		HUB_TTT_EN	**Enable TT Thing Time of HUB** When this bit is set, the EP will read related TT Hub's TT Think Time when serving a Lookup request and forward it to SCH2 and then XACT2. Whe this be is not set, the EP does not read related TT Hub's TT Think Time for Lookup request and the XACT2 simply ignores the TT Think Time provided.

1A0C096C EVT_CFG Event Configuration 00000001

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name								**INTR_BEI_EN**
Type								RW
Reset								1

Bit(s)	Mnemonic	Name	Description
0		INTR_BEI_EN	**Enable BEI Support for Interrupt** When this bit is set, the BEI (Block Event Interrupt) feature is supported Whe this be is not set, the BEI (Block Event Interrupt) feature is not supported

1A0C0970 TRBQ_CFG TRBQ Configuration 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name								
Type								

Reset								
Bit	7	6	5	4	3	2	1	0
Name								**TRB_ERR_CHK_DIS**
Type								RW
Reset								0

Bit(s)	Mnemonic	Name	Description
0		TRB_ERR_CHK_DIS	**Disable TRB Error Check** When this bit is set, the TRB error check in command ring is disabled. Whe this be is not set, the TRB error check in command ring is enabled.

1A0C0974 U3PORT_CFG USB3 Port Configuration 00000001

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name								**U3PORT_WRP_BY_HCRST_EN**
Type								RW
Reset								1

Bit(s)	Mnemonic	Name	Description
0		U3PORT_WRP_BY_HCRST_EN	**Enable USB3 Port Warm Reset by HCRST**

Bit(s)	Mnemonic	Name	Description
			When this bit is set, the USB3 Port will send Warm Reset Whe this be is not set, the the USB3 Port will not send Warm Reset

1A0C0978 U2PORT_CFG USB2 Port Configuration 00000004

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name	LPM_L1_EXIT_TIMER							
Type	RW							
Reset	0	0	0	0	0	1	0	0

Bit(s)	Mnemonic	Name	Description
7:0		LPM_L1_EXIT_TIMER	**LPM L1 Exit Timer** This register indicate the no. of uFrame to stay in L1 if there is no EP are masked by NYET.

1A0C097C HSCH_CFG2 Host Scheduler Configuration Register 2 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								

Reset								
Bit	15	14	13	12	11	10	9	8
Name				SCH_INT_NAK_ACTIVE_MASK_4P	SCH_INT_NAK_ACTIVE_MASK_3P	SCH_INT_NAK_ACTIVE_MASK_2P	SCH_INT_NAK_ACTIVE_MASK_1P	SCH_INT_NAK_ACTIVE_MASK
Type				RW	RW	RW	RW	RW
Reset				0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name				SCH_BULK_NYET_ACTIVE_MASK_4P	SCH_BULK_NYET_ACTIVE_MASK_3P	SCH_BULK_NYET_ACTIVE_MASK_2P	SCH_BULK_NYET_ACTIVE_MASK_1P	SCH_BULK_NYET_ACTIVE_MASK
Type				RW	RW	RW	RW	RW
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12		SCH_INT_NAK_ACTIVE_MASK_4P	**Scheduler 2 Port 4 Active Mask when Interrupt is NAKed** 1'b0: Active Mask is not set when Interrupt is NAKed. xHC can actively exilt USB2 LPM 1'b1: Active Mask is set when Interrupt is NAKed. xHC cannot actively exilt USB2 LPM. Wait remove LPM wakeup
11		SCH_INT_NAK_ACTIVE_MASK_3P	**Scheduler 2 Port 3 Active Mask when Interrupt is NAKed** 1'b0: Active Mask is not set when Interrupt is NAKed. xHC can actively exilt USB2 LPM 1'b1: Active Mask is set when Interrupt is NAKed. xHC cannot actively exilt USB2 LPM. Wait remove LPM wakeup
10		SCH_INT_NAK_ACTIVE_MASK_2P	**Scheduler 2 Port 2 Active Mask when Interrupt is NAKed** 1'b0: Active Mask is not set when Interrupt is NAKed. xHC can actively exilt USB2 LPM 1'b1: Active Mask is set when Interrupt is NAKed. xHC cannot actively exilt USB2 LPM. Wait remove LPM wakeup
9		SCH_INT_NAK_ACTIVE_MASK_1P	**Scheduler 2 Port 1 Active Mask when Interrupt is NAKed** 1'b0: Active Mask is not set when Interrupt is NAKed. xHC can actively exilt USB2 LPM

Bit(s)	Mnemonic	Name	Description
			1'b1: Active Mask is set when Interrupt is NAKed. xHC cannot actively exilt USB2 LPM. Wait remove LPM wakeup
8		SCH_INT_NAK_ACTIVE_MASK	**Scheduler 2 Port 0 Active Mask when Interrupt is NAKed** 1'b0: Active Mask is not set when Interrupt is NAKed. xHC can actively exilt USB2 LPM 1'b1: Active Mask is set when Interrupt is NAKed. xHC cannot actively exilt USB2 LPM. Wait remove LPM wakeup
4		SCH_BULK_NYET_ACTIVE_MASK_4P	**Scheduler 2 Port 4 Active Mask when Bulk OUT is NYETed** 1'b0: Active Mask is not set when Bulk OUT is NYETed. xHC can actively exilt USB2 LPM 1'b1: Active Mask is set when Bulk OUT is NYETed. xHC cannot actively exilt USB2 LPM. Wait remove LPM wakeup
3		SCH_BULK_NYET_ACTIVE_MASK_3P	**Scheduler 2 Port 3 Active Mask when Bulk OUT is NYETed** 1'b0: Active Mask is not set when Bulk OUT is NYETed. xHC can actively exilt USB2 LPM 1'b1: Active Mask is set when Bulk OUT is NYETed. xHC cannot actively exilt USB2 LPM. Wait remove LPM wakeup
2		SCH_BULK_NYET_ACTIVE_MASK_2P	**Scheduler 2 Port 2 Active Mask when Bulk OUT is NYETed** 1'b0: Active Mask is not set when Bulk OUT is NYETed. xHC can actively exilt USB2 LPM 1'b1: Active Mask is set when Bulk OUT is NYETed. xHC cannot actively exilt USB2 LPM. Wait remove LPM wakeup
1		SCH_BULK_NYET_ACTIVE_MASK_1P	**Scheduler 2 Port 1 Active Mask when Bulk OUT is NYETed** 1'b0: Active Mask is not set when Bulk OUT is NYETed. xHC can actively exilt USB2 LPM 1'b1: Active Mask is set when Bulk OUT is NYETed. xHC cannot actively exilt USB2 LPM. Wait remove LPM wakeup
0		SCH_BULK_NYET_ACTIVE_MASK	**Scheduler 2 Port 0 Active Mask when Bulk OUT is NYETed**

Bit(s)	Mnemonic	Name	Description
			1'b0: Active Mask is not set when Bulk OUT is NYETed. xHC can actively exilt USB2 LPM 1'b1: Active Mask is set when Bulk OUT is NYETed. xHC cannot actively exilt USB2 LPM. Wait remove LPM wakeup

1A0C0980 SW_ERDY Software ERDY 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name	SW_ERDY_CMD			SW_ERDY_DCI				
Type	A0			RW				
Reset	0			0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	SW_ERDY_SLOT_ID							
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		SW_ERDY_CMD	**Software ERDY CMD** When set to 1'b1, software ERDY with target Slot ID and DCI are requested When xHC complete processing of the software ERDY, this bit is cleared by HW. Note that this request only take effect when the endpoint state is Running and is flow controlled state, otherwise the request will be ignored. Note: ERDY_CMD should be 1'b0, before set ERDY_SLOT_ID and ERDY_DCI.
12:8		SW_ERDY_DCI	**Software ERDY DCI**

Bit(s)	Mnemonic	Name	Description
			When SOFT_ERDY_CMD is set to 1'b1, this represents the DCI of software ERDY. For EP0 of a device, DCI shall be 1
7:0		SW_ERDY_SLOT_ID	**Software ERDY Slot ID** When SOFT_ERDY_CMD is set to 1'b1, this represents the Slot ID of software ERDY. Software shall guarantee the Slot ID of the device is operating at Super Speed, otherwise undefined result may happen. The software must al guarantees the Slot ID cannot be 0's

1A0C09A0 SLOT_EP_STS0 Slot and EP Resource Status0 00000F40

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name	AVAIL_SLOT_NUM							
Type	RO							
Reset	0	0	0	0	1	1	1	1
Bit	7	6	5	4	3	2	1	0
Name	AVAIL_EP_NUM							
Type	RO							
Reset	0	1	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8		AVAIL_SLOT_NUM	**Available Slot Number** This register indicates the remaining Slot number to be allocated for Enable Slot command
7:0		AVAIL_EP_NUM	**Available EP Number** This register indicates the remaining EP number to be allocated for Address Device and Configure Endpoint commands

1A0C09A4 SLOT_EP_STS1 Slot and EP Resource Status1 FFFFFFFF

Bit	31	30	29	28	27	26	25	24
Name	AVAIL_EP_BITMAP_LO							
Type	RO							
Reset	1	1	1	1	1	1	1	1
Bit	23	22	21	20	19	18	17	16
Name	AVAIL_EP_BITMAP_LO							
Type	RO							
Reset	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8
Name	AVAIL_EP_BITMAP_LO							
Type	RO							
Reset	1	1	1	1	1	1	1	1
Bit	7	6	5	4	3	2	1	0
Name	AVAIL_EP_BITMAP_LO							
Type	RO							
Reset	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		AVAIL_EP_BITMAP_LO	**Available EP Bitmap Lo** This register represned whether EP index 31~0 are available for SW to add endpoint. A bit of value equal to 1'b1, means that this EP index is still available

1A0C09A8 SLOT_EP_STS2 Slot and EP Resource Status2 FFFFFFFF

Bit	31	30	29	28	27	26	25	24
Name	AVAIL_EP_BITMAP_HI							
Type	RO							
Reset	1	1	1	1	1	1	1	1
Bit	23	22	21	20	19	18	17	16
Name	AVAIL_EP_BITMAP_HI							
Type	RO							
Reset	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8
Name	AVAIL_EP_BITMAP_HI							
Type	RO							
Reset	1	1	1	1	1	1	1	1
Bit	7	6	5	4	3	2	1	0
Name	AVAIL_EP_BITMAP_HI							
Type	RO							
Reset	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		AVAIL_EP_BITMAP_HI	**Available EP Bitmap Hi** This register represned whether EP index 63~32 are available for SW to add endpoint. A bit of value equal to 1'b1, means that this EP index is still available

1A0C09B0 RST_CTRL0 Host reset control Register 2 0000000F

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name					**HCRST_DRAM_EN**	**HCRST_SYS60_EN**	**HCRST_SYS125_EN**	**HCRST_XHCI_EN**
Type					RW	RW	RW	RW
Reset					1	1	1	1

Bit(s)	Mnemonic	Name	Description
3		HCRST_DRAM_EN	**dram_rst_b by HCRST Enable** When this bit is 1'b1, the HCRST results in dram_rst_b
2		HCRST_SYS60_EN	**sys60_rst_b by HCRST Enable** When this bit is 1'b1, the HCRST results in sys60_rst_b
1		HCRST_SYS125_EN	**sys125_rst_b by HCRST Enable** When this bit is 1'b1, the HCRST results in sys125_rst_b
0		HCRST_XHCI_EN	**xhci_rst_b by HCRST Enable** When this bit is 1'b1, the HCRST results in xhci_rst_b

Bit(s)	Mnemonic	Name	Description

1A0C09B4 RST_CTRL1 Host reset control Register 3 03FF000F

Bit	31	30	29	28	27	26	25	24
Name							HCRST_U2_PHYD_EN_4P	HCRST_U2_MAC_EN_4P
Type							RW	RW
Reset							1	1
Bit	23	22	21	20	19	18	17	16
Name	HCRST_U2_PHYD_EN_3P	HCRST_U2_MAC_EN_3P	HCRST_U2_PHYD_EN_2P	HCRST_U2_MAC_EN_2P	HCRST_U2_PHYD_EN_1P	HCRST_U2_MAC_EN_1P	HCRST_U2_PHYD_EN_0P	HCRST_U2_MAC_EN_0P
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8
Name								
Type								
Reset								
Bit	7	6	5	4	3	2	1	0
Name					HCRST_U3_PHYD_EN_1P	HCRST_U3_MAC_EN_1P	HCRST_U3_PHYD_EN_0P	HCRST_U3_MAC_EN_0P
Type					RW	RW	RW	RW
Reset					1	1	1	1

Bit(s)	Mnemonic	Name	Description
25		HCRST_U2_PHYD_EN_4P	**Enable HCRST as software reset for USB2 PHYD Port4** 1'b0: HCRST does not imply software reest for target USB2 PHYD 1'b1: HCRST implies software reset for target USB2 PHYD
24		HCRST_U2_MAC_EN_4P	**Enable HCRST as software reset for USB2 MAC Port4** 1'b0: HCRST does not imply software reest for target USB2 MAC

Bit(s)	Mnemonic	Name	Description
			1'b1: HCRST implies software reset for target USB2 MAC
23		HCRST_U2_PHYD_EN_3P	**Enable HCRST as software reset for USB2 PHYD Port3** 1'b0: HCRST does not imply software reest for target USB2 PHYD 1'b1: HCRST implies software reset for target USB2 PHYD
22		HCRST_U2_MAC_EN_3P	**Enable HCRST as software reset for USB2 MAC Port3** 1'b0: HCRST does not imply software reest for target USB2 MAC 1'b1: HCRST implies software reset for target USB2 MAC
21		HCRST_U2_PHYD_EN_2P	**Enable HCRST as software reset for USB2 PHYD Port2** 1'b0: HCRST does not imply software reest for target USB2 PHYD 1'b1: HCRST implies software reset for target USB2 PHYD
20		HCRST_U2_MAC_EN_2P	**Enable HCRST as software reset for USB2 MAC Port2** 1'b0: HCRST does not imply software reest for target USB2 MAC 1'b1: HCRST implies software reset for target USB2 MAC
19		HCRST_U2_PHYD_EN_1P	**Enable HCRST as software reset for USB2 PHYD Port1** 1'b0: HCRST does not imply software reest for target USB2 PHYD 1'b1: HCRST implies software reset for target USB2 PHYD
18		HCRST_U2_MAC_EN_1P	**Enable HCRST as software reset for USB2 MAC Port1** 1'b0: HCRST does not imply software reest for target USB2 MAC 1'b1: HCRST implies software reset for target USB2 MAC
17		HCRST_U2_PHYD_EN_0P	**Enable HCRST as software reset for USB2 PHYD Port0**

Bit(s)	Mnemonic	Name	Description
			1'b0: HCRST does not imply software reest for target USB2 PHYD 1'b1: HCRST implies software reset for target USB2 PHYD
16		HCRST_U2_MAC_EN_0P	**Enable HCRST as software reset for USB2 MAC Porto** 1'b0: HCRST does not imply software reest for target USB2 MAC 1'b1: HCRST implies software reset for target USB2 MAC
3		HCRST_U3_PHYD_EN_1P	**Enable HCRST as software reset for USB3 PHYD Port1** 1'b0: HCRST does not imply software reest for target USB3 PHYD 1'b1: HCRST implies software reset for target USB3 PHYD
2		HCRST_U3_MAC_EN_1P	**Enable HCRST as software reset for USB3 MAC Port1** 1'b0: HCRST does not imply software reest for target USB3 MAC 1'b1: HCRST implies software reset for target USB3 MAC
1		HCRST_U3_PHYD_EN_0P	**Enable HCRST as software reset for USB3 PHYD Porto** 1'b0: HCRST does not imply software reest for target USB3 PHYD 1'b1: HCRST implies software reset for target USB3 PHYD
0		HCRST_U3_MAC_EN_0P	**Enable HCRST as software reset for USB3 MAC Porto** 1'b0: HCRST does not imply software reest for target USB3 MAC 1'b1: HCRST implies software reset for target USB3 MAC

1A0C09F0 SPARE0 Spare Register 0 00000000

Bit	31	30	29	28	27	26	25	24
Name	SPARE0							

Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
Name	**SPARE0**							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	**SPARE0**							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	**SPARE0**							
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		SPARE0	**Spare Register 0** This register is with default value 0's and is prepared for ECO purpose

1A0C09F4 SPARE1 Spare Register 1 FFFFFFFF

Bit	31	30	29	28	27	26	25	24
Name	**SPARE1**							
Type	RW							
Reset	1	1	1	1	1	1	1	1
Bit	23	22	21	20	19	18	17	16
Name	**SPARE1**							
Type	RW							
Reset	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8
Name	**SPARE1**							
Type	RW							
Reset	1	1	1	1	1	1	1	1
Bit	7	6	5	4	3	2	1	0
Name	**SPARE1**							
Type	RW							
Reset	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		SPARE1	**Spare Register 1**

Bit(s)	Mnemonic	Name	Description
			This register is with default value 1's and is prepared for ECO purpose

2.1.1.2 xhci_u3_port

Module name: xhci_u3_port Base address: (+1a0c0420h)

Address	Name	Width	Register Function
1A0C0420	USB3_PORT_SC	32	USB3_PORT Port Status and Control
1A0C0424	USB3_PORT_PMSC	32	USB3_PORT PM Status and Control
1A0C0428	USB3_PORT_LI	32	USB3_PORT Link Info

1A0C0420 USB3_PORT_SC USB3_PORT Port Status and Control 000002A0

Bit	31	30	29	28	27	26	25	24
Name	USB3_PORT_WPR	USB3_PORT_DR			USB3_PORT_WOE	USB3_PORT_WDE	USB3_PORT_WCE	
Type	WO	RO			RW	RW	RW	
Reset	0	0			0	0	0	
Bit	23	22	21	20	19	18	17	16
Name	USB3_PORT_CEC	USB3_PORT_PLC	USB3_PORT_PRC	USB3_PORT_OCC	USB3_PORT_WRC	USB3_PORT_PEC	USB3_PORT_CSC	USB3_PORT_LWS
Type	W1C	W1C	W1C	W1C	W1C	RO	W1C	WO
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	USB3_PORT_PIC		USB3_PORT_Port_Speed				USB3_PORT_PP	USB3_PORT_PLS
Type	RW		RO				RW	RW
Reset	0	0	0	0	0	0	1	0
Bit	7	6	5	4	3	2	1	0
Name	USB3_PORT_PLS			USB3_PORT_PR	USB3_PORT_OCA		USB3_PORT_PED	USB3_PORT_CCS
Type	RW			W1C	RO		W1C	RO
Reset	1	0	1	0	0		0	0

Bit(s)	Mnemonic	Name	Description
31		USB3_PORT_WPR	**Warm Port Reset (WPR).** Default = '0'. When software writes a '1' to this bit, the Warm Reset sequence as defined in the USB3 Specification is initiated and the PR flag is set to '1'. Once initiated, the PR, PRC, and WRC flags shall reflect the progress of the Warm Reset sequence. This flag shall always return '0' when read. Refer to section 4.19.5.1. This flag only applies to USB3 protocol ports. For USB2 protocol ports it shall be RsvdZ
30		USB3_PORT_DR	**Device Removablej (DR).** This flag indicates if this port has a removable device attached. '1' = Device is non-removable. '0' = Device is removable.
27		USB3_PORT_WOE	**Wake on Over-current Enable (WOE).** Default = '0'. Writing this bit to a '1' enables the port to be sensitive to over-current conditions as system wake-up eventsi. Refer to section 4.15 for operational model.
26		USB3_PORT_WDE	**Wake on Disconnect Enable (WDE).** Default = '0'. Writing this bit to a '1' enables the port to be sensitive to device disconnects as system wake-up eventsi. Refer to section 4.15 for operational model.
25		USB3_PORT_WCE	**Wake on Connect Enable (WCE).** Default = '0'. Writing this bit to a '1' enables the port to be sensitive to device connects as system wake-up eventsi. Refer to section 4.15 for operational model.
23		USB3_PORT_CEC	**Port Config Error Change (CEC).** Default = '0'. This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 for more information on change bit usage. Note: This flag is valid only for USB3 protocol ports. For USB2 protocol ports this bit shall be RsvdZ.
22		USB3_PORT_PLC	**Port Link State Change (PLC).** Default = '0'. This flag is set to '1' due to the following PLS transitions: Transition Condition U3 -> Resume Wakeup signaling from a device Resume -> Recovery -> U0 Device Resume complete (USB3 protocol ports only)

Bit(s)	Mnemonic	Name	Description
			Resume -> U0 Device Resume complete (USB2 protocol ports only) U3 -> Recovery -> U0 Software Resume complete (USB3 protocol ports only) U3 -> U0 Software Resume complete (USB2 protocol ports only) U2 -> U0 L1 Resume complete (USB2 protocol ports only)h U0 -> U0 L1 Entry Reject (USB2 protocol ports only)h Any state -> Inactive Error (USB3 protocol ports only). Note: PLC is asserted only if there is an SS.Inactive.Disconnect.Detect to SS.Inactive.Quiet transition in the LTSSM. Note that this flag shall not be set if the PLS transition was due to software setting PP to '0'. Refer to section 4.23.5 for more information. '0' = No change. '1' = Link Status Changed. Software shall clear this bit by writing a '1' to it. Refer to "PLC Condition:" references in section 4.19.1 for the specific port state transitions that set this flag. Refer to section 4.19.2 for more information on change bit usage.
21		USB3_PORT_PRC	**Port Reset Change (PRC).** Default = '0'. This flag is set to '1' due a '1' to '0' transition of Port Reset (PR). e.g. when any reset processing (Warm or Hot) on this port is complete. Note that this flag shall not be set to '1' if the reset processing was forced to terminate due to software clearing PP or PED to '0'. '0' = No change. '1' = Reset complete. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5. Refer to section 4.19.2 for more information on change bit usage.
20		USB3_PORT_OCC	**Over-current Change (OCC).** Default = '0'. This bit shall be set to a '1' when there is a '0' to '1' or '1' to '0' transition of Over-current Active (OCA). Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 for more information on change bit usage.
19		USB3_PORT_WRC	**Warm Port Reset Change (WRC).** Default = '0'. This bit is set when Warm Reset processing on this port completes. '0' = No change. '1' = Warm Reset complete. Note that this flag shall not be set to '1' if the Warm Reset processing was forced to terminate due to software clearing PP or PED to '0'. Software shall clear this bit by writing a '1' to it. Refer

Bit(s)	Mnemonic	Name	Description
			to section 4.19.5.1. Refer to section 4.19.2 for more information on change bit usage. This bit only applies to USB3 protocol ports. For USB2 protocol ports it shall be RsvdZ.
18		USB3_PORT_PEC	**Port Enabled/Disabled Change (PEC).** Default = '0'. '1' = change in PED. '0' = No change. Note that this flag shall not be set if the PED transition was due to software setting PP to '0'. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 for more information on change bit usage. For a USB2 protocol port, this bit shall be set to '1' only when the port is disabled due to the appropriate conditions existing at the EOF2 point (refer to section 11.8.1 of the USB2 Specification for the definition of a Port Error). For a USB3 protocol port, this bit shall never be set to '1'.
17		USB3_PORT_CSC	**Connect Status Change (CSC) .** Default = '0'. '1' = Change in CCS. '0' = No change. This flag indicates a change has occurred in the port's Current Connect Status (CCS). Note that this flag shall not be set if the CCS transition was due to software setting PP to '0'. The xHC sets this bit to '1' for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 for more information on change bit usage.
16		USB3_PORT_LWS	**Port Link State Write Strobe (LWS).** Default = '0'. When this bit is set to '1' on a write reference to this register, this flag enables writes to the PLS field. When '0', write data in PLS field is ignored. Reads to this bit return '0'.
15:14		USB3_PORT_PIC	**Port Indicator Control (PIC).** Default = 0. Writing to these bits has no effect if the Port Indicators (PIND) bit in the HCCPARAMS register is a '0'. If PIND bit is a '1', then the bit encodings are: Value Meaning 0 Port indicators are off 1 Amber

Bit(s)	Mnemonic	Name	Description
			2 Green 3 Undefined Refer to the USB2 Specification for a description on how these bits are to be used. This field is '0' if PP is '0'.
13:10		USB3_PORT_Port_Speed	**Port Speed (Port Speed).** Default = '0'. This field identifies the speed of the attached USB Device. This field is only relevant if a device is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed. Value Meaning 0 Undefined Speed 1 Full-speed device attached 2 Low-speed device attached 3 High-speed device attached 4 SuperSpeed device attached 5-15 Reserved Note: Values the 1, 2 and 3 are exclusive to USB2 protocol ports and the value 4 is exclusive to USB3 protocol ports
9		USB3_PORT_PP	**Port Power (PP).** Default = '1'. This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When PP equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report over-current conditions when PP = '0' if PPC = '0'. 0 = This port is in the Powered-off state. 1 = This port is not in the Powered-off state. If the Port Power Control (PPC) flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ('0' = off, '1' = on). If the Port Power Control (PPC) flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit.

Bit(s)	Mnemonic	Name	Description
			When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a '1' to '0' (removing power from the port). Refer to section 4.19.4 for more information.
8:5		USB3_PORT_PLS	**Port Link State (PLS).** Default = RxDetect ('5'). This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Value Description 0 The link shall transition to a U0 state from any of the U states. 2b USB2 protocol ports only. The link should transition to the U2 State. 3 The link shall transition to a U3 state from any of the U states. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub will respond to resume signaling from the port. 5 USB3 protocol ports only. If the port is in the Disabled state (PLS = Disabled, PP = 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 1b,4,6-14 Ignored. 15 USB2 protocol ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit substate, else ignored. Refer to section 4.15.2 for more information. Note: The Port Link State Write Strobe (LWS) shall also be set to '1' to write this field. For USB2 protocol ports: Writing a value of '2' to this field shall request LPM, asserting L1 signaling on the USB2 bus. Software may read this field to determine if the transition to the U2 state was successful. Writing a value of '0' shall deassert L1 signaling on the USB. Writing a value of '1' shall have no affect. The U1 state shall never be reported by a USB2 protocol port. Read Value Meaning 0 Link is in the U0 State 1 Link is in the U1 State

Bit(s)	Mnemonic	Name	Description
			2 Link is in the U2 State 3 Link is in the U3 State (Device Suspended) 4 Link is in the Disabled Statec 5 Link is in the RxDetect Stated 6 Link is in the Inactive Statee 7 Link is in the Polling State 8 Link is in the Recovery State 9 Link is in the Hot Reset State 10 Link is in the Compliance Mode State 11 Link is in the Test Modef State 12:13 Reserved 14: Link is in the Reset state (MTK) 15 Link is in the Resume Stateg This field is undefined if PP = '0'. Note: Transitions between different states are not reflected until the transition is complete. Refer to sections 4.15.2 and 4.23.5 for more information on the use of this field. Refer to the USB2 LPM ECR for more information on USB link power management operation. Refer to section 7.2 for supported USB protocols.
4		USB3_PORT_PR	**Port Reset (PR).** Default = '0'. '1' = Port Reset signaling is asserted. '0' = Port is not in Reset. When software writes a '1' to this bit (from a '0') the bus reset sequence is initiated; USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Spec. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Spec. PR remains set until reset signaling is completed by the root hub. Note that software shall write a '1' to the this flag to transition a USB2 port from the Polling state to the Enabled state. Refer to sections 4.15.2.3 and 4.19.1.1. This flag is '0' if PP is '0'.
3		USB3_PORT_OCA	**Over-current Active (OCA).** Default = '0'. '1' = This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically

Bit(s)	Mnemonic	Name	Description
			transition from a '1' to a '0' when the over-current condition is removed.
1		USB3_PORT_PED	**Port Enabled/Disabled (PED).** Default = '0'. '1' = Enabled. '0' = Disabled. Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag. This flag shall automatically be cleared to '0' by a disconnect event or other fault condition. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled (PED = '0') downstream propagation of data is blocked on this port, except for reset. For USB2 protocol ports: When the port is in the Disabled state, software shall reset the port (PR = '1') to transition PED to '1' and the port to the Enabled state. For USB3 protocol ports: When the port is in the Polling state (after detecting an attach), the port shall automatically transition to the Enabled state and set PED to '1' upon the completion of successful link training. When the port is in the Disabled state, software shall write a '5' (RxDetect) to the PLS field to transition the port to the Disconnected state. Refer to section 4.19.1.2. PED shall automatically be cleared to '0' when PR is set to '1', and set to '1' when PR transitions from '1' to '0' after a successful reset. Refer to Port Reset (PR) bit for more information on how the PED bit is managed. Note that when software writes this bit to a '1', it shall also write a '0' to the PR bita. This flag is '0' if PP is '0'.
0		USB3_PORT_CCS	**Current Connect Status (CCS).** Default = '0'. '1' = Device is present on port. '0' = No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change (CSC) bit to be set to '1'. Refer to section 4.19.4 for more details on the Connect Status Change (CSC) assertion conditions. This flag is '0' if PP is '0'.

Bit(s)	Mnemonic	Name	Description

1A0C0424 USB3_PORT_PMSC USB3_PORT PM Status and Control 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								**USB3_PORT_FLA**
Type								RW
Reset								0
Bit	15	14	13	12	11	10	9	8
Name	**USB3_PORT_U2_Timeout**							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	**USB3_PORT_U1_Timeout**							
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16		USB3_PORT_FLA	**Force Link PM Accept (FLA).** Default = '0'. When this bit is set to '1', the port shall generate a Set Link Function LMP with the Force_LinkPM_Accept bit asserted. . This flag shall be set to '0' by the assertion of PR to '1' or when CCS = transitions from '0' to '1'. Writes to this flag have no affect if PP = '0'. The Set Link Function LMP is sent by the xHC to the device connected on this port when this bit transitions from '0' to '1'. Refer to Sections 8.4.1, 10.4.2.2 and 10.4.2.9 of the USB3 specification for more details. Improper use of the SS Force_LinkPM_Accept functionality can impact the performance of the

Bit(s)	Mnemonic	Name	Description
			link significantly. This bit shall only be used for compliance and testing purposes. Software shall ensure that there are no pending packets at the link level before setting this bit. This flag is '0' if PP is '0'.
15:8		USB3_PORT_U2_Timeout	**U2 Timeout.** Default = '0'. Timeout value for U2 inactivity timer. If equal to FFh, the port is disabled from initiating U2 entry. This field shall be set to '0' by the assertion of PR to '1'. Refer to section 4.19.4.1 for more information on U2 Timeout operation. The following are permissible values: Value Description 00h Zero (default) 01h 256 us 02h 512 us ... FEh 65.024 ms FFh Infinite A U2 Inactivity Timeout LMP shall be sent by the xHC to the device connected on this port when this field is written. Refer to Sections 8.4.3 and 10.4.2.10 of the USB3 specification for more details.
7:0		USB3_PORT_U1_Timeout	**U1 Timeout.** Default = '0'. Timeout value for U1 inactivity timer. If equal to FFh, the port is disabled from initiating U1 entry. This field shall be set to '0' by the assertion of PR to '1'. Refer to section 4.19.4.1 for more information on U1 Timeout operation. The following are permissible values: Value Description 00h Zero (default)

Bit(s)	Mnemonic	Name	Description
			01h 1 us. 02h 2 us. ... 7Fh 127 us. 80h-FEh Reserved FFh Infinite

1A0C0428 USB3_PORT_LI USB3_PORT Link Info 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name	USB3_PORT_Link_Error_Count							
Type	RO							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	USB3_PORT_Link_Error_Count							
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		USB3_PORT_Link_Error_Count	**Link Error Count.** Default = '0'. This field returns the number of link errors detected by the port. This value shall be reset to '0' by the assertion of a Chip Hardware Reset, HCRST, when PR transitions from '1' to '0', or when CCS = transitions from '0' to '1'.

2.1.1.3 xhci_u2_port

Module name: xhci_u2_port Base address: (+1a0c0440h)

Address	Name	Width	Register Function
1A0C0440	USB2_PORT_SC	32	USB2_PORT Port Status and Control
1A0C0444	USB2_PORT_PMSC	32	USB2_PORT PM Status and Control
1A0C0448	USB2_PORT_LI	32	USB2_PORT Link Info
1A0C044C	USB2_PORT_HLPMC	32	USB2_PORT Hardware LPM Control Register

1A0C0440 USB2_PORT_SC USB2_PORT Port Status and Control 000002A0

Bit	31	30	29	28	27	26	25	24
Name	USB2_PORT_WPR	USB2_PORT_DR			USB2_PORT_WOE	USB2_PORT_WDE	USB2_PORT_WCE	
Type	RO	RO			RW	RW	RW	
Reset	0	0			0	0	0	
Bit	23	22	21	20	19	18	17	16
Name	USB2_PORT_CEC	USB2_PORT_PLC	USB2_PORT_PRC	USB2_PORT_OCC	USB2_PORT_WRC	USB2_PORT_PEC	USB2_PORT_CSC	USB2_PORT_LWS
Type	RO	W1C	W1C	W1C	W1C	W1C	W1C	WO
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	USB2_PORT_PIC		USB2_PORT_Port_Speed				USB2_PORT_PP	USB2_PORT_PLS
Type	RW		RO				RW	RW
Reset	0	0	0	0	0	0	1	0
Bit	7	6	5	4	3	2	1	0
Name	USB2_PORT_PLS			USB2_PORT_PR	USB2_PORT_OCA		USB2_PORT_PED	USB2_PORT_CCS
Type	RW			W1C	RO		W1C	RO
Reset	1	0	1	0	0		0	0

Bit(s)	Mnemonic Name	Description
31	USB2_PORT_WPR	**Warm Port Reset (WPR).** Default = '0'. When software writes a '1' to this bit, the Warm Reset sequence as defined in the USB3 Specification is initiated and the PR flag is set to '1'. Once initiated, the PR, PRC, and WRC flags shall reflect the progress of the Warm Reset sequence. This flag shall always return '0' when read. Refer to section

Bit(s)	Mnemonic	Name	Description
			4.19.5.1. This flag only applies to USB3 protocol ports. For USB2 protocol ports it shall be RsvdZ.
30		USB2_PORT_DR	**Device Removablej (DR).** This flag indicates if this port has a removable device attached. '1' = Device is non-removable. '0' = Device is removable.
27		USB2_PORT_WOE	**Wake on Over-current Enable (WOE).** Default = '0'. Writing this bit to a '1' enables the port to be sensitive to over-current conditions as system wake-up eventsi. Refer to section 4.15 for operational model.
26		USB2_PORT_WDE	**Wake on Disconnect Enable (WDE).** Default = '0'. Writing this bit to a '1' enables the port to be sensitive to device disconnects as system wake-up eventsi. Refer to section 4.15 for operational model.
25		USB2_PORT_WCE	**Wake on Connect Enable (WCE).Default = '0'. Writing this bit to a '1' enables the port to be sensitive to device connects as system wake-up eventsi. Refer to section 4.15 for operational model.**
23		USB2_PORT_CEC	**Port Config Error Change (CEC).** Default = '0'. This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 for more information on change bit usage. Note: This flag is valid only for USB3 protocol ports. For USB2 protocol ports this bit shall be RsvdZ.
22		USB2_PORT_PLC	**Port Link State Change (PLC).** Default = '0'. This flag is set to '1' due to the following PLS transitions: Transition Condition U3 -> Resume Wakeup signaling from a device Resume -> Recovery -> U0 Device Resume complete (USB3 protocol ports only) Resume -> U0 Device Resume complete (USB2 protocol ports only) U3 -> Recovery -> U0 Software Resume complete (USB3 protocol ports only) U3 -> U0 Software Resume complete (USB2 protocol ports only)

Bit(s)	Mnemonic	Name	Description
			U2 -> U0 L1 Resume complete (USB2 protocol ports only)h U0 -> U0 L1 Entry Reject (USB2 protocol ports only)h Any state -> Inactive Error (USB3 protocol ports only). Note: PLC is asserted only if there is an SS.Inactive.Disconnect.Detect to SS.Inactive.Quiet transition in the LTSSM. Note that this flag shall not be set if the PLS transition was due to software setting PP to '0'. Refer to section 4.23.5 for more information. '0' = No change. '1' = Link Status Changed. Software shall clear this bit by writing a '1' to it. Refer to "PLC Condition:" references in section 4.19.1 for the specific port state transitions that set this flag. Refer to section 4.19.2 for more information on change bit usage.
21		USB2_PORT_PRC	**Port Reset Change (PRC).** Default = '0'. This flag is set to '1' due a '1' to '0' transition of Port Reset (PR). e.g. when any reset processing (Warm or Hot) on this port is complete. Note that this flag shall not be set to '1' if the reset processing was forced to terminate due to software clearing PP or PED to '0'. '0' = No change. '1' = Reset complete. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5. Refer to section 4.19.2 for more information on change bit usage.
20		USB2_PORT_OCC	**Over-current Change (OCC).** Default = '0'. This bit shall be set to a '1' when there is a '0' to '1' or '1' to '0' transition of Over-current Active (OCA). Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 for more information on change bit usage.
19		USB2_PORT_WRC	**Warm Port Reset Change (WRC).** Default = '0'. This bit is set when Warm Reset processing on this port completes. '0' = No change. '1' = Warm Reset complete. Note that this flag shall not be set to '1' if the Warm Reset processing was forced to terminate due to software clearing PP or PED to '0'. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5.1. Refer to section 4.19.2 for more information on change bit usage. This bit only applies to USB3 protocol ports. For USB2 protocol ports it shall be RsvdZ.
18		USB2_PORT_PEC	**Port Enabled/Disabled Change (PEC).** Default = '0'. '1' = change in PED. '0' = No change. Note that this flag shall not be set if the PED transition was due to software setting PP to '0'. Software shall clear

Bit(s)	Mnemonic	Name	Description
			this bit by writing a '1' to it. Refer to section 4.19.2 for more information on change bit usage. For a USB2 protocol port, this bit shall be set to '1' only when the port is disabled due to the appropriate conditions existing at the EOF2 point (refer to section 11.8.1 of the USB2 Specification for the definition of a Port Error). For a USB3 protocol port, this bit shall never be set to '1'.
17		USB2_PORT_CSC	**Connect Status Change (CSC).** Default = '0'. '1' = Change in CCS. '0' = No change. This flag indicates a change has occurred in the port's Current Connect Status (CCS). Note that this flag shall not be set if the CCS transition was due to software setting PP to '0'. The xHC sets this bit to '1' for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 for more information on change bit usage.
16		USB2_PORT_LWS	**Port Link State Write Strobe (LWS).** Default = '0'. When this bit is set to '1' on a write reference to this register, this flag enables writes to the PLS field. When '0', write data in PLS field is ignored. Reads to this bit return '0'.
15:14		USB2_PORT_PIC	**Port Indicator Control (PIC).** Default = 0. Writing to these bits has no effect if the Port Indicators (PIND) bit in the HCCPARAMS register is a '0'. If PIND bit is a '1', then the bit encodings are: Value Meaning 0 Port indicators are off 1 Amber 2 Green 3 Undefined Refer to the USB2 Specification for a description on how these bits are to be used. This field is '0' if PP is '0'.
13:10		USB2_PORT_Port_Speed	**Port Speed (Port Speed).** Default = '0'. This field identifies the speed of the attached USB Device. This field is only relevant if a

Bit(s)	Mnemonic	Name	Description
			device is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed. Value Meaning 0 Undefined Speed 1 Full-speed device attached 2 Low-speed device attached 3 High-speed device attached 4 SuperSpeed device attached 5-15 Reserved Note: Values the 1, 2 and 3 are exclusive to USB2 protocol ports and the value 4 is exclusive to USB3 protocol ports
9		USB2_PORT_PP	**Port Power (PP).** Default = '1'. This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When PP equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report over-current conditions when PP = '0' if PPC = '0'. 0 = This port is in the Powered-off state. 1 = This port is not in the Powered-off state. If the Port Power Control (PPC) flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ('0' = off, '1' = on). If the Port Power Control (PPC) flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a '1' to '0' (removing power from the port). Refer to section 4.19.4 for more information.
8:5		USB2_PORT_PLS	**Port Link State (PLS).**

Bit(s)	Mnemonic	Name	Description
			Default = RxDetect ('5'). This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Value Description 0 The link shall transition to a U0 state from any of the U states. 2b USB2 protocol ports only. The link should transition to the U2 State. 3 The link shall transition to a U3 state from any of the U states. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub will respond to resume signaling from the port. 5 USB3 protocol ports only. If the port is in the Disabled state (PLS = Disabled, PP = 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 1b,4,6-14 Ignored. 15 USB2 protocol ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit substate, else ignored. Refer to section 4.15.2 for more information. Note: The Port Link State Write Strobe (LWS) shall also be set to '1' to write this field. For USB2 protocol ports: Writing a value of '2' to this field shall request LPM, asserting L1 signaling on the USB2 bus. Software may read this field to determine if the transition to the U2 state was successful. Writing a value of '0' shall deassert L1 signaling on the USB. Writing a value of '1' shall have no affect. The U1 state shall never be reported by a USB2 protocol port. Read Value Meaning 0 Link is in the U0 State 1 Link is in the U1 State 2 Link is in the U2 State 3 Link is in the U3 State (Device Suspended) 4 Link is in the Disabled Statec 5 Link is in the RxDetect Stated 6 Link is in the Inactive Statee

Bit(s)	Mnemonic	Name	Description
			7 Link is in the Polling State 8 Link is in the Recovery State 9 Link is in the Hot Reset State 10 Link is in the Compliance Mode State 11 Link is in the Test Modef State 12:14 Reserved 15 Link is in the Resume Stateg This field is undefined if PP = '0'. Note: Transitions between different states are not reflected until the transition is complete. Refer to sections 4.15.2 and 4.23.5 for more information on the use of this field. Refer to the USB2 LPM ECR for more information on USB link power management operation. Refer to section 7.2 for supported USB protocols.
4		USB2_PORT_PR	**Port Reset (PR).** Default = '0'. '1' = Port Reset signaling is asserted. '0' = Port is not in Reset. When software writes a '1' to this bit (from a '0') the bus reset sequence is initiated; USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Spec. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Spec. PR remains set until reset signaling is completed by the root hub. Note that software shall write a '1' to the this flag to transition a USB2 port from the Polling state to the Enabled state. Refer to sections 4.15.2.3 and 4.19.1.1. This flag is '0' if PP is '0'.
3		USB2_PORT_OCA	**Over-current Active (OCA).** Default = '0'. '1' = This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a '0' when the over-current condition is removed.
1		USB2_PORT_PED	**Port Enabled/Disabled (PED).** Default = '0'. '1' = Enabled. '0' = Disabled. Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag.

Bit(s)	Mnemonic	Name	Description
			This flag shall automatically be cleared to '0' by a disconnect event or other fault condition. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled (PED = '0') downstream propagation of data is blocked on this port, except for reset. For USB2 protocol ports: When the port is in the Disabled state, software shall reset the port (PR = '1') to transition PED to '1' and the port to the Enabled state. For USB3 protocol ports: When the port is in the Polling state (after detecting an attach), the port shall automatically transition to the Enabled state and set PED to '1' upon the completion of successful link training. When the port is in the Disabled state, software shall write a '5' (RxDetect) to the PLS field to transition the port to the Disconnected state. Refer to section 4.19.1.2. PED shall automatically be cleared to '0' when PR is set to '1', and set to '1' when PR transitions from '1' to '0' after a successful reset. Refer to Port Reset (PR) bit for more information on how the PED bit is managed. Note that when software writes this bit to a '1', it shall also write a '0' to the PR bita. This flag is '0' if PP is '0'.
0		USB2_PORT_CCS	**Current Connect Status (CCS).** Default = '0'. '1' = Device is present on port. '0' = No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change (CSC) bit to be set to '1'. Refer to section 4.19.4 for more details on the Connect Status Change (CSC) assertion conditions. This flag is '0' if PP is '0'.

1A0C0444 USB2_PORT_PMSC USB2_PORT PM Status and Control 00000000

Bit	31	30	29	28	27	26	25	24
Name	USB2_PORT_Port_Test_Ctrl							
Type	RW							
Reset	0	0	0	0				
Bit	23	22	21	20	19	18	17	16

Name								USB2_PORT_HW_LPM_EN
Type								RW
Reset								0
Bit	15	14	13	12	11	10	9	8
Name	USB2_PORT_L1_Device_Slot							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	USB2_PORT_BESL				USB2_PORT_RWE	USB2_PORT_L1S		
Type	RW				RW	RO		
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		USB2_PORT_Port_Test_Ctrl	**Port Test Control.** Default = '0'. When this field is '0', the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Powered-Off state (PLS = Disabled). If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. Refer to section 4.19.6 for the operational model for using these test modes. The encoding of the Test Mode bits for a USB2 protocol port are: Value Test Mode 0 Test mode not enabled 1 Test J_STATE 2 Test K_STATE 3 Test SE0_NAK 4 Test Packet

Bit(s)	Mnemonic	Name	Description
			5 Test FORCE_ENABLE 6-14 Reserved. 15 Port Test Control Error. Refer to the sections 7.1.20 and 11.24.2.13 of the USB2 spec for more information on Test Modes.
16		USB2_PORT_HW_LPM_EN	**Hardware LPM Enable** Default = '0'. If this bit is set to '1', then hardware controlled LPM shall be enabled for this port. Refer to section 4.23.5.1.1.1. If the USB2 Hardware LMP Capability is not supported (HLC = '0') this field shall be RsvdZ.
15:8		USB2_PORT_L1_Device_Slot	**L1 Device Slot.** Default = '0'. System software sets this field to indicate the ID of the Device Slot associated with the device directly attached to the Root Hub port. A value of '0' indicates no device is present. The xHC uses this field to lookup information necessary to generate the LMP Token packet. If the USB2 L1 Capability is not supported (L1C = '0') this field shall be RsvdZ.
7:4		USB2_PORT_BESL	**Best Effort Service Latency (BESL).** Default = '0'. System software sets this field to indicate to the recipient device how long the xHC will drive resume if it (the xHC) initiates an exit from L1. The BESL value encoding is defined in Table 13. Note that the BESL field is used by both software and hardware controlled LPM. Refer to section 4.23.5.1.1 for more information on BESL use. Refer to section 5.2.5 for information on how DBESL may be used to establish an initial value for BESL.
3		USB2_PORT_RWE	**Remote Wake Enable (RWE).** Default = '0'. The host system sets this flag to enable or

Bit(s)	Mnemonic	Name	Description
			disable the device for remote wake from L1. The value of this flag will temporarily (while in L1) override the current setting of the Remote Wake feature set by the standard Set/ClearFeature() commands defined in Universal Serial Bus Specification, revision 2.0, Chapter 9.
2:0		USB2_PORT_L1S	**L1 Status (L1S).** Default = 0. This field is used by software to determine whether an L1- based suspend request (LMP transaction) was successful, specifically: Value Meaning 0 Invalid - This field shall be ignored by software. 1 Success - Port successfully transitioned to L1 (ACK) 2 Not Yet - Device is unable to enter L1 at this time (NYET) 3 Not Supported - Device does not support L1 transitions (STALL) 4 Timeout/Error - Device failed to respond to the LPM Transaction or an error occurred 5-7 Reserved The value of this field is only valid when the port resides in the L0 or L1 state (PLS = '0' or '2'). Refer to section 4.23.5.1.1 for more information. If the USB2 L1 Capability is not supported (L1C = '0') this field shall be RsvdZ.

1A0C0448 USB2_PORT_LI USB2_PORT Link Info 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								

Reset								
Bit	15	14	13	12	11	10	9	8
Name	**USB2_PORT_Link_Error_Count**							
Type	RO							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	**USB2_PORT_Link_Error_Count**							
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		USB2_PORT_Link_Error_Count	**Link Error Count.** Default = '0'. This field returns the number of link errors detected by the port. This value shall be reset to '0' by the assertion of a Chip Hardware Reset, HCRST, when PR transitions from '1' to '0', or when CCS = transitions from '0' to '1'.

1A0C044C USB2_PORT_HLPMC USB2_PORT Hardware LPM Control Register 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name			**USB2_PORT_BESLD**				**USB2_PORT_L1_TIMEOUT**	
Type			RW				RW	
Reset			0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	**USB2_PORT_L1_TIMEOUT**						**USB2_PORT_HIRDM**	
Type	RW						RW	
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13:10		USB2_PORT_BESLD	**Best Effort Service Latency Deep (BESLD) - RWS. Default = '0'. System software sets this** field to indicate to the recipient device how long the xHC will drive resume on an exit from U2. Refer to section 4.23.5.1.1.1 for more information on BESLD use. The BESLD value encoding is defined in Table 13. Refer to section 5.2.6 for information on how DBESLD may be used to establish an initial value for BESLD.
9:2		USB2_PORT_L1_TIMEOUT	**L1 Timeout - RWS. Default = 00h. Timeout value for the L1 inactivity timer (LPM Timer). This** field shall be set to 00h by the assertion of PR to '1'. Refer to section 4.23.5.1.1.1 for more information on L1 Timeout operation. The following are permissible values: Value Description 00h 128 us. (default) 01h 256 us. 02h 512 us. 03h 768 us. ... FFh 65,280 us.
1:0		USB2_PORT_HIRDM	**Host Initiated Resume Duration Mode (HIRDM) - RWS. Default = 0h. Indicates which HIRD** value should be used. The following are permissible values: 0 Initiate L1 using BESL only on timeout. (default) 1 Initiate L1 using BESLD on timeout. If rejected by device, initiate L1 using BESL. 3-2 Reserved.

2.1.1.4 xhci_u2_port_1p

Module name: xhci_u2_port_1p Base address: (+1a0c0450h)

Address	Name	Width	Register Function
1A0C0450	USB2_PORT_SC	32	USB2_PORT Port Status and Control
1A0C0454	USB2_PORT_PMSC	32	USB2_PORT PM Status and Control
1A0C0458	USB2_PORT_LI	32	USB2_PORT Link Info
1A0C045C	USB2_PORT_HLPMC	32	USB2_PORT Hardware LPM Control Register

1A0C0450 USB2_PORT_SC USB2_PORT Port Status and Control 000002A0

Bit	31	30	29	28	27	26	25	24
Name	USB2_PORT_WPR	USB2_PORT_DR			USB2_PORT_WOE	USB2_PORT_WDE	USB2_PORT_WCE	
Type	RO	RO			RW	RW	RW	
Reset	0	0			0	0	0	
Bit	23	22	21	20	19	18	17	16
Name	USB2_PORT_CEC	USB2_PORT_PLC	USB2_PORT_PRC	USB2_PORT_OCC	USB2_PORT_WRC	USB2_PORT_PEC	USB2_PORT_CSC	USB2_PORT_LWS
Type	RO	W1C	W1C	W1C	W1C	W1C	W1C	WO
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name	USB2_PORT_PIC		USB2_PORT_Port_Speed				USB2_PORT_PP	USB2_PORT_PLS
Type	RW		RO				RW	RW
Reset	0	0	0	0	0	0	1	0
Bit	7	6	5	4	3	2	1	0
Name	USB2_PORT_PLS			USB2_PORT_PR	USB2_PORT_OCA		USB2_PORT_PED	USB2_PORT_CCS
Type	RW			W1C	RO		W1C	RO
Reset	1	0	1	0	0		0	0

Bit(s)	Mnemonic	Name	Description
31		USB2_PORT_WPR	**Warm Port Reset (WPR).** Default = '0'. When software writes a '1' to this bit, the Warm Reset sequence as defined in the USB3 Specification is initiated and the PR flag is set to '1'. Once initiated, the PR, PRC, and WRC flags shall reflect the progress of the Warm Reset sequence. This flag shall always return '0' when read. Refer to section

Bit(s)	Mnemonic	Name	Description
			4.19.5.1. This flag only applies to USB3 protocol ports. For USB2 protocol ports it shall be RsvdZ.
30		USB2_PORT_DR	**Device Removablej (DR).** This flag indicates if this port has a removable device attached. '1' = Device is non-removable. '0' = Device is removable.
27		USB2_PORT_WOE	**Wake on Over-current Enable (WOE).** Default = '0'. Writing this bit to a '1' enables the port to be sensitive to over-current conditions as system wake-up eventsi. Refer to section 4.15 for operational model.
26		USB2_PORT_WDE	**Wake on Disconnect Enable (WDE).** Default = '0'. Writing this bit to a '1' enables the port to be sensitive to device disconnects as system wake-up eventsi. Refer to section 4.15 for operational model.
25		USB2_PORT_WCE	**Wake on Connect Enable (WCE).Default = '0'. Writing this bit to a '1' enables the port to be sensitive to device connects as system wake-up eventsi. Refer to section 4.15 for operational model.**
23		USB2_PORT_CEC	**Port Config Error Change (CEC).** Default = '0'. This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 for more information on change bit usage. Note: This flag is valid only for USB3 protocol ports. For USB2 protocol ports this bit shall be RsvdZ.
22		USB2_PORT_PLC	**Port Link State Change (PLC).** Default = '0'. This flag is set to '1' due to the following PLS transitions: Transition Condition U3 -> Resume Wakeup signaling from a device Resume -> Recovery -> U0 Device Resume complete (USB3 protocol ports only) Resume -> U0 Device Resume complete (USB2 protocol ports only) U3 -> Recovery -> U0 Software Resume complete (USB3 protocol ports only) U3 -> U0 Software Resume complete (USB2 protocol ports only)

Bit(s)	Mnemonic	Name	Description
			U2 -> U0 L1 Resume complete (USB2 protocol ports only)h U0 -> U0 L1 Entry Reject (USB2 protocol ports only)h Any state -> Inactive Error (USB3 protocol ports only). Note: PLC is asserted only if there is an SS.Inactive.Disconnect.Detect to SS.Inactive.Quiet transition in the LTSSM. Note that this flag shall not be set if the PLS transition was due to software setting PP to '0'. Refer to section 4.23.5 for more information. '0' = No change. '1' = Link Status Changed. Software shall clear this bit by writing a '1' to it. Refer to "PLC Condition:" references in section 4.19.1 for the specific port state transitions that set this flag. Refer to section 4.19.2 for more information on change bit usage.
21		USB2_PORT_PRC	**Port Reset Change (PRC).** Default = '0'. This flag is set to '1' due a '1' to '0' transition of Port Reset (PR). e.g. when any reset processing (Warm or Hot) on this port is complete. Note that this flag shall not be set to '1' if the reset processing was forced to terminate due to software clearing PP or PED to '0'. '0' = No change. '1' = Reset complete. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5. Refer to section 4.19.2 for more information on change bit usage.
20		USB2_PORT_OCC	**Over-current Change (OCC).** Default = '0'. This bit shall be set to a '1' when there is a '0' to '1' or '1' to '0' transition of Over-current Active (OCA). Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 for more information on change bit usage.
19		USB2_PORT_WRC	**Warm Port Reset Change (WRC).** Default = '0'. This bit is set when Warm Reset processing on this port completes. '0' = No change. '1' = Warm Reset complete. Note that this flag shall not be set to '1' if the Warm Reset processing was forced to terminate due to software clearing PP or PED to '0'. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5.1. Refer to section 4.19.2 for more information on change bit usage. This bit only applies to USB3 protocol ports. For USB2 protocol ports it shall be RsvdZ.
18		USB2_PORT_PEC	**Port Enabled/Disabled Change (PEC).** Default = '0'. '1' = change in PED. '0' = No change. Note that this flag shall not be set if the PED transition was due to software setting PP to '0'. Software shall clear

Bit(s)	Mnemonic	Name	Description
			this bit by writing a '1' to it. Refer to section 4.19.2 for more information on change bit usage. For a USB2 protocol port, this bit shall be set to '1' only when the port is disabled due to the appropriate conditions existing at the EOF2 point (refer to section 11.8.1 of the USB2 Specification for the definition of a Port Error). For a USB3 protocol port, this bit shall never be set to '1'.
17		USB2_PORT_CSC	**Connect Status Change (CSC).** Default = '0'. '1' = Change in CCS. '0' = No change. This flag indicates a change has occurred in the port's Current Connect Status (CCS). Note that this flag shall not be set if the CCS transition was due to software setting PP to '0'. The xHC sets this bit to '1' for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 for more information on change bit usage.
16		USB2_PORT_LWS	**Port Link State Write Strobe (LWS).** Default = '0'. When this bit is set to '1' on a write reference to this register, this flag enables writes to the PLS field. When '0', write data in PLS field is ignored. Reads to this bit return '0'.
15:14		USB2_PORT_PIC	**Port Indicator Control (PIC).** Default = 0. Writing to these bits has no effect if the Port Indicators (PIND) bit in the HCCPARAMS register is a '0'. If PIND bit is a '1', then the bit encodings are: Value Meaning 0 Port indicators are off 1 Amber 2 Green 3 Undefined Refer to the USB2 Specification for a description on how these bits are to be used. This field is '0' if PP is '0'.
13:10		USB2_PORT_Port_Speed	**Port Speed (Port Speed).** Default = '0'. This field identifies the speed of the attached USB Device. This field is only relevant if a

Bit(s)	Mnemonic	Name	Description
			device is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed. Value Meaning 0 Undefined Speed 1 Full-speed device attached 2 Low-speed device attached 3 High-speed device attached 4 SuperSpeed device attached 5-15 Reserved Note: Values the 1, 2 and 3 are exclusive to USB2 protocol ports and the value 4 is exclusive to USB3 protocol ports
9		USB2_PORT_PP	**Port Power (PP).** Default = '1'. This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When PP equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report over-current conditions when PP = '0' if PPC = '0'. 0 = This port is in the Powered-off state. 1 = This port is not in the Powered-off state. If the Port Power Control (PPC) flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ('0' = off, '1' = on). If the Port Power Control (PPC) flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a '1' to '0' (removing power from the port). Refer to section 4.19.4 for more information.
8:5		USB2_PORT_PLS	**Port Link State (PLS).**

Bit(s)	Mnemonic	Name	Description
			Default = RxDetect ('5'). This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Value Description 0 The link shall transition to a U0 state from any of the U states. 2b USB2 protocol ports only. The link should transition to the U2 State. 3 The link shall transition to a U3 state from any of the U states. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub will respond to resume signaling from the port. 5 USB3 protocol ports only. If the port is in the Disabled state (PLS = Disabled, PP = 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 1b,4,6-14 Ignored. 15 USB2 protocol ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit substate, else ignored. Refer to section 4.15.2 for more information. Note: The Port Link State Write Strobe (LWS) shall also be set to '1' to write this field. For USB2 protocol ports: Writing a value of '2' to this field shall request LPM, asserting L1 signaling on the USB2 bus. Software may read this field to determine if the transition to the U2 state was successful. Writing a value of '0' shall deassert L1 signaling on the USB. Writing a value of '1' shall have no affect. The U1 state shall never be reported by a USB2 protocol port. Read Value Meaning 0 Link is in the U0 State 1 Link is in the U1 State 2 Link is in the U2 State 3 Link is in the U3 State (Device Suspended) 4 Link is in the Disabled Statec 5 Link is in the RxDetect Stated 6 Link is in the Inactive Statee

Bit(s)	Mnemonic	Name	Description
			7 Link is in the Polling State 8 Link is in the Recovery State 9 Link is in the Hot Reset State 10 Link is in the Compliance Mode State 11 Link is in the Test Modef State 12:14 Reserved 15 Link is in the Resume Stateg This field is undefined if PP = '0'. Note: Transitions between different states are not reflected until the transition is complete. Refer to sections 4.15.2 and 4.23.5 for more information on the use of this field. Refer to the USB2 LPM ECR for more information on USB link power management operation. Refer to section 7.2 for supported USB protocols.
4		USB2_PORT_PR	**Port Reset (PR).** Default = '0'. '1' = Port Reset signaling is asserted. '0' = Port is not in Reset. When software writes a '1' to this bit (from a '0') the bus reset sequence is initiated; USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Spec. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Spec. PR remains set until reset signaling is completed by the root hub. Note that software shall write a '1' to the this flag to transition a USB2 port from the Polling state to the Enabled state. Refer to sections 4.15.2.3 and 4.19.1.1. This flag is '0' if PP is '0'.
3		USB2_PORT_OCA	**Over-current Active (OCA).** Default = '0'. '1' = This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a '0' when the over-current condition is removed.
1		USB2_PORT_PED	**Port Enabled/Disabled (PED).** Default = '0'. '1' = Enabled. '0' = Disabled. Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag.

Bit(s)	Mnemonic	Name	Description
			This flag shall automatically be cleared to '0' by a disconnect event or other fault condition. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled (PED = '0') downstream propagation of data is blocked on this port, except for reset. For USB2 protocol ports: When the port is in the Disabled state, software shall reset the port (PR = '1') to transition PED to '1' and the port to the Enabled state. For USB3 protocol ports: When the port is in the Polling state (after detecting an attach), the port shall automatically transition to the Enabled state and set PED to '1' upon the completion of successful link training. When the port is in the Disabled state, software shall write a '5' (RxDetect) to the PLS field to transition the port to the Disconnected state. Refer to section 4.19.1.2. PED shall automatically be cleared to '0' when PR is set to '1', and set to '1' when PR transitions from '1' to '0' after a successful reset. Refer to Port Reset (PR) bit for more information on how the PED bit is managed. Note that when software writes this bit to a '1', it shall also write a '0' to the PR bita. This flag is '0' if PP is '0'.
0		USB2_PORT_CCS	**Current Connect Status (CCS).** Default = '0'. '1' = Device is present on port. '0' = No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change (CSC) bit to be set to '1'. Refer to section 4.19.4 for more details on the Connect Status Change (CSC) assertion conditions. This flag is '0' if PP is '0'.

1A0C0454 USB2_PORT_PMSC USB2_PORT PM Status and Control 00000000

Bit	31	30	29	28	27	26	25	24
Name	USB2_PORT_Port_Test_Ctrl							
Type	RW							
Reset	0	0	0	0				
Bit	23	22	21	20	19	18	17	16

Name								USB2_PORT_HW_LPM_EN
Type								RW
Reset								0
Bit	15	14	13	12	11	10	9	8
Name	USB2_PORT_L1_Device_Slot							
Type	RW							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	USB2_PORT_BESL				USB2_PORT_RWE	USB2_PORT_L1S		
Type	RW				RW	RO		
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		USB2_PORT_Port_Test_Ctrl	**Port Test Control.** Default = '0'. When this field is '0', the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Powered-Off state (PLS = Disabled). If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. Refer to section 4.19.6 for the operational model for using these test modes. The encoding of the Test Mode bits for a USB2 protocol port are: Value Test Mode 0 Test mode not enabled 1 Test J_STATE 2 Test K_STATE 3 Test SE0_NAK 4 Test Packet

Bit(s)	Mnemonic	Name	Description
			5 Test FORCE_ENABLE 6-14 Reserved. 15 Port Test Control Error. Refer to the sections 7.1.20 and 11.24.2.13 of the USB2 spec for more information on Test Modes.
16		USB2_PORT_HW_LPM_EN	**Hardware LPM Enable** Default = '0'. If this bit is set to '1', then hardware controlled LPM shall be enabled for this port. Refer to section 4.23.5.1.1.1. If the USB2 Hardware LMP Capability is not supported (HLC = '0') this field shall be RsvdZ.
15:8		USB2_PORT_L1_Device_Slot	**L1 Device Slot.** Default = '0'. System software sets this field to indicate the ID of the Device Slot associated with the device directly attached to the Root Hub port. A value of '0' indicates no device is present. The xHC uses this field to lookup information necessary to generate the LMP Token packet. If the USB2 L1 Capability is not supported (L1C = '0') this field shall be RsvdZ.
7:4		USB2_PORT_BESL	**Best Effort Service Latency (BESL).** Default = '0'. System software sets this field to indicate to the recipient device how long the xHC will drive resume if it (the xHC) initiates an exit from L1. The BESL value encoding is defined in Table 13. Note that the BESL field is used by both software and hardware controlled LPM. Refer to section 4.23.5.1.1 for more information on BESL use. Refer to section 5.2.5 for information on how DBESL may be used to establish an initial value for BESL.
3		USB2_PORT_RWE	**Remote Wake Enable (RWE).** Default = '0'. The host system sets this flag to enable or

Bit(s)	Mnemonic	Name	Description
			disable the device for remote wake from L1. The value of this flag will temporarily (while in L1) override the current setting of the Remote Wake feature set by the standard Set/ClearFeature() commands defined in Universal Serial Bus Specification, revision 2.0, Chapter 9.
2:0		USB2_PORT_L1S	**L1 Status (L1S).** Default = 0. This field is used by software to determine whether an L1- based suspend request (LMP transaction) was successful, specifically: Value Meaning 0 Invalid - This field shall be ignored by software. 1 Success - Port successfully transitioned to L1 (ACK) 2 Not Yet - Device is unable to enter L1 at this time (NYET) 3 Not Supported - Device does not support L1 transitions (STALL) 4 Timeout/Error - Device failed to respond to the LPM Transaction or an error occurred 5-7 Reserved The value of this field is only valid when the port resides in the L0 or L1 state (PLS = '0' or '2'). Refer to section 4.23.5.1.1 for more information. If the USB2 L1 Capability is not supported (L1C = '0') this field shall be RsvdZ.

1A0C0458 USB2_PORT_LI USB2_PORT Link Info 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								

Reset								
Bit	15	14	13	12	11	10	9	8
Name	**USB2_PORT_Link_Error_Count**							
Type	RO							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	**USB2_PORT_Link_Error_Count**							
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		USB2_PORT_Link_Error_Count	**Link Error Count.** Default = '0'. This field returns the number of link errors detected by the port. This value shall be reset to '0' by the assertion of a Chip Hardware Reset, HCRST, when PR transitions from '1' to '0', or when CCS = transitions from '0' to '1'.

1A0C045C USB2_PORT_HLPMC USB2_PORT Hardware LPM Control Register 00000000

Bit	31	30	29	28	27	26	25	24
Name								
Type								
Reset								
Bit	23	22	21	20	19	18	17	16
Name								
Type								
Reset								
Bit	15	14	13	12	11	10	9	8
Name			**USB2_PORT_BESLD**				**USB2_PORT_L1_TIMEOUT**	
Type			RW				RW	
Reset			0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	**USB2_PORT_L1_TIMEOUT**						**USB2_PORT_HIRDM**	
Type	RW						RW	
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13:10		USB2_PORT_BESLD	**Best Effort Service Latency Deep (BESLD) - RWS. Default = '0'. System software sets this** field to indicate to the recipient device how long the xHC will drive resume on an exit from U2. Refer to section 4.23.5.1.1.1 for more information on BESLD use. The BESLD value encoding is defined in Table 13. Refer to section 5.2.6 for information on how DBESLD may be used to establish an initial value for BESLD.
9:2		USB2_PORT_L1_TIMEOUT	**L1 Timeout - RWS. Default = 00h. Timeout value for the L1 inactivity timer (LPM Timer). This** field shall be set to 00h by the assertion of PR to '1'. Refer to section 4.23.5.1.1.1 for more information on L1 Timeout operation. The following are permissible values: Value Description 00h 128 us. (default) 01h 256 us. 02h 512 us. 03h 768 us. ... FFh 65,280 us.
1:0		USB2_PORT_HIRDM	**Host Initiated Resume Duration Mode (HIRDM) - RWS. Default = 0h. Indicates which HIRD** value should be used. The following are permissible values: 0 Initiate L1 using BESL only on timeout. (default) 1 Initiate L1 using BESLD on timeout. If rejected by device, initiate L1 using BESL. 3-2 Reserved.

2.1.2 PCIE 0 MAC

Module name: PCIE_MAC0 Base address: (+1a143000h)

Address	Name	Width	Register Function
1A143000	K_GBL_1	32	Core variables can be set using the XpressRich2 Configuration Wizard. However, ASIC customers are encouraged to implement a programming mechanism that enables them to access and modify these settings if needed. Note: These variables should only be modified when the Core is in reset mode. Do not modify these variables if reset is not active as this may cause a malfunction of the Core.Core variables can be set using the XpressRich2 Configuration Wizard. However, ASIC customers are encouraged to implement a programming mechanism that enables them to access and modify these settings if needed. Note: These variables should only be modified when the Core is in reset mode. Do not modify these variables if reset is not active as this may cause a malfunction of the Core.
1A143004	K_GBL_2	32	Global configuration registers: the 2nd DW
1A143008	K_DP	32	Device & Port setup
1A14300C	K_CNT_0	32	Counter-related Configurations 1
1A143010	K_CNT_1	32	Counter-related Configurations 2
1A143014	K_CNT_2	32	Counter-related Configurations 3
1A143018	K_CNT_3	32	Counter-related Configurations 4
1A14301C	K_CNT_4	32	Counter-related Configurations 5
1A143020	K_RTRY	32	Replay Buffer Information
1A143024	MISC_CONF	32	Misllaneous Configuration
1A143030	K_FC_VC0_0	32	Flow Control Information for Virtual Cannel 0 (similar for VC1-7) - the 1st DW
1A143034	K_FC_VC0_1	32	Flow Control Information for Virtual Cannel 0 (similar for VC1-7) - the 2nd DW
1A143038	K_PTR_VC0_0	32	Recive Buffer Pointers VC 0 (similar for VC1-7) - the 1st DW
1A14303C	K_PTR_VC0_1	32	Recive Buffer Pointers VC 0 (similar for VC1-7) - the 2nd DW
1A143040	K_PTR_VC0_2	32	Recive Buffer Pointers VC 0 (similar for VC1-7) - the 3rd DW
1A143044	K_PTR_VC0_3	32	Recive Buffer Pointers VC 0 (similar for VC1-7) - the 4th DW
1A143100	K_CONF_FUNC0_0	32	Configuration Space Header 00h
1A143104	K_CONF_FUNC0_1	32	Configuration Space Header 08h
1A143108	K_CONF_FUNC0_2	32	Configuration Space Header 2Ch
1A14310C	K_CONF_FUNC0_3	32	Individual function 0 configuration, the 4th DW
1A143110	K_CONF_FUNC0_4	32	Individual function 0 configuration, the 5th DW
1A143114	K_CONF_FUNC0_5	32	Individual function 0 configuration, the 6th DW
1A143118	K_CONF_FUNC0_6	32	Individual function 0 configuration, the 7th DW
1A14311C	K_CONF_FUNC0_7	32	Individual function 0 configuration, the 8th DW
1A143120	K_CONF_FUNC0_8	32	Individual function 0 configuration, the 9th DW
1A143124	K_CONF_FUNC0_9	32	Individual function 0 configuration, the 10th DW

Address	Name	Width	Register Function
1A143128	K_CONF_FUNC0_10	32	Individual function 0 configuration, the 11th DW
1A14312C	K_CONF_FUNC0_11	32	Individual function 0 configuration, the 12th DW
1A143130	K_CONF_FUNC0_12	32	Individual function 0 configuration, the 13th DW
1A143134	K_BAR_FUNC0_0	32	BAR0 Configuration. Note:A BAR cannot be modified if the previous BAR uses 64-bit addressing.
1A143138	K_BAR_FUNC0_1	32	BAR1 Configuration.
1A14313C	K_BAR_FUNC0_2	32	BAR2 Configuration.
1A143140	K_BAR_FUNC0_3	32	BAR3 Configuration.
1A143144	K_BAR_FUNC0_4	32	BAR4 Configuration.
1A143148	K_BAR_FUNC0_5	32	BAR5 Configuration.
1A14314C	K_BAR_FUNC0_6	32	Expansion ROM Configuration 1.
1A143150	K_BAR_FUNC0_7	32	Expansion ROM Configuration 2.
1A143154	K_CONF_LTR_OBFF	32	LTR AND OBFF Support Hwinit
1A143158	K_CPL_RESOURCE	32	Complete resource
1A14315C	L_LOCAL_TCOMMON_MODE	32	Tcommon mode time requred by Local PHY RX
1A143180	K_CONF_FUNC0_13	32	MPCIe Configuration space capability
1A143400	WDMA_PCIE_ADDR_L	32	Write DMA start PCIe address LSB
1A143404	WDMA_PCIE_ADDR_H	32	Write DMA start PCIe address MSB
1A143408	WDMA_BUS_ADDR	32	Write DMA start BUS address
1A14340C	WDMA_CONTROL	32	Write DMA control parameters
1A143410	RDMA_PCIE_ADDR_L	32	Read DMA start PCIe address LSB
1A143414	RDMA_PCIE_ADDR_H	32	Read DMA start PCIe address MSB
1A143418	RDMA_BUS_ADDR	32	Read DMA start BUS address
1A14341C	RDMA_CONTROL	32	Read DMA control parameters
1A143420	INT_MASK	32	Interrupt Mask
1A143424	INT_STATUS	32	Interrupt Status
1A143428	INT_RMT_MASK	32	Interrupt Remote Mask
1A14342C	IMSI_STATUS	32	MSI Status
1A143430	IMSI_ADDR	32	Root port MSI capture address
1A143434	ICMD	32	Interrupt Command
1A143438	AHB2PCIE_BASE0_L	32	AHB slave to PCIe tranlsation table0 LSB
1A14343C	AHB2PCIE_BASE0_H	32	AHB slave to PCIe translation table0 MSB
1A143440	AHB2PCIE_BASE1_L	32	AHB slave to PCIe translation table1 LSB
1A143444	AHB2PCIE_BASE1_H	32	AHB slave to PCIe translation table1 MSB
1A143448	PCIE2AXI_WIN0	32	PCIe to AXI window0 control register
1A14344C	PCIE2AXI_WIN1	32	PCIe to AXI window1 control register
1A143450	PCIE2AXI_WIN2	32	PCIe to AXI window2 control register
1A143454	PCIE2AXI_WIN3	32	PCIe to AXI window3 control register
1A143458	PCIE2AXI_WIN4	32	PCIe to AXI window4 control register
1A14345C	PCIE2AXI_WIN5	32	PCIe to AXI window4 control register
1A143460	CFG_HEADER_0	32	CFG request TLP header DW0
1A143464	CFG_HEADER_1	32	CFG request TLP header DW1
1A143468	CFG_HEADER_2	32	CFG request TLP header DW2
1A14346C	CFG_HEADER_3	32	CFG request TLP header DW3

Address	Name	Width	Register Function
1A143470	CFG_WDATA	32	CfgWr request TLP data
1A143474	MSG_HEADER_0	32	MSG request TLP header DW0
1A143478	MSG_HEADER_1	32	MSG request TLP header DW1
1A14347C	MSG_HEADER_2	32	MSG request TLP header DW2
1A143480	MSG_HEADER_3	32	MSG request TLP header DW3
1A143484	MSG_DATA	32	MSG request TLP data
1A143488	APP_TLP_REQ	32	APP request TLP start command
1A14348C	CFG_RDATA	32	Returned CfgRd request CplD data
1A143490	CFG_BAR0	32	BAR0 content in configuration space
1A143494	CFG_BAR1	32	BAR1 content in configuration space
1A143498	CFG_BAR2	32	BAR2 content in configuration space
1A14349C	CFG_BAR3	32	BAR3 content in configuration space
1A1434A0	CFG_BAR4	32	BAR4 content in configuration space
1A1434A4	CFG_BAR5	32	BAR5 content in configuration space
1A1434AC	LTR_LATENCY_VALUE	32	LTR max snoop and no-snoop latency Register
1A1434B0	MSI_MISC	32	MSI control and status Register
1A1434D0	AHB_DISCARD_TIMER	32	AHB discard timer
1A1434D8	ASPM_CONF	32	Active State power management configuration ASPM_CONF register contains information for PCI Express native power management.
1A1434DC	PM_STATUS	32	PCI legacy power management status This is used in Endpoint mode only
1A1434E0	PM_CONF_0	32	PCI legacy power management configuration This is used in Endpoint mode only PM_CONF register contains information for PCI power management capabilities register and local processor must initialize it at power-up.
1A1434E4	PM_CONF_1	32	
1A1434E8	PM_CONF_2	32	
1A1434EC	PCI_SLOTCAP	32	PCI Express slot capabilities
1A1434F0	PCI_DV	32	PCI device and vendor ID.
1A1434F4	PCI_SUB	32	PCI subsystem device and vendor ID
1A1434F8	PCI_CREV	32	PCI class code and revision ID
1A1434FC	PCI_SLOTCSR	32	PCI Express slot control and status register
1A143500	PCI_PRMCSR	32	PCI primary command and status register
1A143504	PCI_DEVCSR	32	PCI Express device control and status register
1A143508	PCI_LINKCSR	32	PCI Express link control and status register
1A14350C	PCI_ROOTCSR	32	PCI Express root status register
1A143510	PCI_RSTCR	32	PCI Express IP reset control register
1A143514	PCI_MAC_HW_VERSION	32	PCI Express MAC HW Version
1A143518	REG_DBG_MOD_SEL	32	PCI Express Debugging Module Select
1A14351C	REG_DBG_PORT_SEL	32	PCI Express Debugging Port Select
1A143520	REG_OBFF_0	32	OBFF Control Register 0
1A143524	REG_OBFF_1	32	OBFF Control Register 1
1A143528	REG_PHYMAC_CONF	32	PHYMAC Control Register
1A14352C	REG_WAKE_CONTROL	32	Wake_n or Clkreq_n Control Register
1A143530	REG_WCH_WEIGHT_0	32	Write channel WRR weighting control register 0

Address	Name	Width	Register Function
1A143534	REG_WCH_WEIGHT_1	32	Write channel WRR weighting control register 1
1A143538	REG_RCH_WEIGHT_0	32	Read channel WRR weighting control register 0
1A14353C	REG_RCH_WEIGHT_1	32	Read channel WRR weighting control register 1
1A143540	REG_AXI_RD_MMIO_CTRL	32	AXI RD MMIO DMA configuration register.
1A143544	REG_AXI_WR_MMIO_CTRL	32	AXI WR MMIO DMA configuration register.
1A143548	REG_AXI_RD_DMA_CTRL	32	AXI RD DATA DMA configuration register.
1A14354C	REG_AXI_WR_DMA_CTRL	32	AXI WR DATA DMA configuration register.
1A143550	REG_DMA_CK_CTRL	32	Data and MMIO DMA Clock Gate Control
1A143554	REG_IP_SLEEP_CTRL	32	PE2 IP SLEEP control
1A143560	REG_ASPM_L1_CTRL	32	ASPM L1 Reject Timing Value
1A143564	REG_MMIO_CTRL	32	MMIO Control
1A143568	REG_LTR_LATENCY	32	LTR Lattency Value
1A143570	REG_MPCIE_EN	32	MPCIE FUNCTION CONTROL
1A143574	REG_MPCIE_CLK_CTRL_1	32	MPCIE CLOCK CTRL 1
1A143578	REG_MPCIE_CLK_CTRL_2	32	MPCIE CLOCK CTRL 1
1A14357C	REG_MPCIE_CLK_CTRL_3	32	MPCIE CLOCK CTRL 2
1A143580	REG_MPCIE_EBUF	32	MPCIE EBUF Control
1A143584	REG_AHB_ATTR_CTRL	32	MPCIE AHB Access ATTR Control
1A143588	REG_AHB_ATTR_RDDATA	32	MPCIE AHB Access ATTR Read Data
1A14358C	LTSSM_TIME_VALUE_1	32	LTSSM timing value 1
1A143590	LTSSM_TIME_VALUE_2	32	LTSSM timing value 2
1A1435A0	REG_ES_7COUNT_LANE0	32	Error Statistic Count7 of Lane0
1A1435A4	REG_ES_7COUNT_LANE1	32	Error Statistic Count7 of Lane1
1A1435A8	REG_ES_8COUNT_LANE0	32	Error Statistic Count8 of Lane0
1A1435AC	REG_ES_8COUNT_LANE1	32	Error Statistic Count8 of Lane1
1A1435B0	REG_ES_STATUS_LANE0	32	Error Statistic Status register of Lane0
1A1435B8	REG_ES_0COUNT_LANE0	32	Error Statistic Count0 of Lane0
1A1435BC	REG_ES_0COUNT_LANE1	32	Error Statistic Count0 of Lane1
1A1435C0	REG_ES_1COUNT	32	Error Statistic Count1 of VC0
1A1435C4	REG_ES_2COUNT	32	Error Statistic Count2 of VC0
1A1435C8	REG_ES_3COUNT	32	Error Statistic Count3
1A1435CC	REG_ES_CLEAR_ALL	32	Error Statistic Clear
1A1435D0	REG_ES_4COUNT	32	Error Statistic Count4 of VC0
1A1435D4	REG_ES_5COUNT	32	Error Statistic Count5 of VC0
1A1435D8	REG_ES_6COUNT	32	Error Statistic Count6

Address	Name	Width	Register Function
1A1435E0	REG_I2C_CONTROL_OUT_0	32	I2C Output Control Register
1A1435E4	REG_I2C_CONTROL_IN_0	32	I2C Input Control Register
1A1435F0	REG_PE2_MAC_DBG_OUT	32	PE2 MAC Debug Out
1A1435F4	EP_LTSSM_FLAG	32	EP LTSSM Flag
1A1435F8	SW_PROBE_OUT	32	Software Probe Out Register
1A1435FC	PCI_MAC_HW_SUB_VERSION	32	PCI Express MAC HW Sub Version
1A143800	TEST_IN_00	32	Error Injection for Test Purpose
1A143804	TEST_OUT_00	32	Internal State for Monitoring Purpose
1A143808	TEST_IN_01	32	Error Injection for Test Purpose
1A14380C	TEST_IN_02	32	K FIX ID source

1A143000 K_GBL_1 Core variables can be set using the XpressRich2 Configuration Wizard. However, ASIC customers are encouraged to implement a programming mechanism that enables them to access and modify these settings if needed. Note: These variables should only be modified when the Core is in reset mode. Do not modify these variables if reset is not active as this may cause a malfunction of the Core.Core variables can be set using the XpressRich2 Configuration Wizard. However, ASIC customers are encouraged to implement a programming mechanism that enables them to access and modify these settings if needed. Note: These variables should only be modified when the Core is in reset mode. Do not modify these variables if reset is not active as this may cause a malfunction of the Core. 00804201

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_gbl_rcvr_det				k_gbl_derr_rcv_imp	k_gbl_tlp_rx_reorder	k_gbl_com_dpram	k_gbl_cdc_meso ch	k_gbl_cdc_imp	k_gbl_func_imp						
Type	RW				RW	RW	RW	RW	RW	RW						
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_gbl_port_type				k_gbl_bf	k_gbl_ct_	k_gbl_slot	k_gbl_pip	k_gbl_vc_imp							k_gbl_pci

					m_mode	imp	_imp	e_if								e_2o
Type	RW				RW	RW	RW	RW	RW							RW
Reset	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:28	k_gbl_rcvr_det	**k_gbl[31:28]: Only one receiver detection is performed if the result of the receiver detection corresponds to the programmed value. Otherwise, receive detection is performed twice.** - 0100: Receiver detected on lanes 0-3 only - 0010: Receiver detected on lanes 0 or 1 only - 0001: Receiver detected on lane 0 only - 1100: Receiver detected on lanes 4-7 only - 1010: Receiver detected on lanes 6 and 7 only - 1001: Receiver detected on lane 7 only - 0110: Receiver detected on lanes 2 and 3 only - 0101: Receiver detected on lane 3 only - 0011: Receiver detected on lane 1 only Otherwise: Receiver detected all lanes. For example, when this signal is set to 1100 and a receiver is detected on lanes 4-7 only, the LTSSM moves directly to polling state without performing a second receiver detection.
27	k_gbl_derr_rcv_imp	**k_gbl[27]: 1 = Receive buffer error checking using the DERR_RCV signal implemented.**
26	k_gbl_tlp_rx_reorder	**k_gbl[26]: 1 = TLP reordering on the Receive path implemented.**
25	k_gbl_com_dpram	**k_gbl[25]: DPRAM mode** - 0: Dedicated DPRAM per VC defined for Receive buffer - 1: Common DPRAM for all VCs defined for Receive buffer.
24	k_gbl_cdc_mesoch	**k_gbl[24]: Active only when CDC mode is active** - 0: CDC compensates for plesiochronous clock relationship - 1: CDC compensates for mesochronous clock relationship
23	k_gbl_cdc_imp	**k_gbl[23]: CDC implementation**

Bit(s)	Name	Description
		- 0: CDC bypassed - 1: CDC active
22:16	k_gbl_func_imp	**k_gbl[22:16]: Indicates if a particular function is implemented in the Core.** For example, if bit 4 if set to 1, function 4 is implemented.
15:12	k_gbl_port_type	**k_gbl[15:12]: Port type:** - 0100: Rootport - 0000: Endpoint (PCI Express) - 0001: Endpoint (Legacy) - 0101: Switch port (upstream) - 0110: Switch port (downstream) - 0111: Bridge (PCI Express to PCI / PCI-X) - 1110: Type of Core controlled by the mode[1:0] signal for Switch upstream/downstream shared silicon - 1111: Type of Core controlled by the mode[1:0] signal for Rootport, Endpoint shared silicon
11	k_gbl_bfm_mode	**k_gbl[11]: BFM mode: This variable should be set to 0.** The value 1 is used for BFM mode only.
10	k_gbl_ct_imp	**k_gbl[10]: 1 = cut-through mode implemented (switch only)**
9	k_gbl_slot_imp	**k_gbl[9]: Slot register implemented**
8	k_gbl_pipe_if	**k_gbl[8]: PIPE interface width** - 0: 16-bit PIPE data interface - 1: 8-bit PIPE data interface
7:1	k_gbl_vc_imp	**k_gbl[7:1]: Indicates if a particular VC is implemented in the Core.** For example, if bit 4 if set to 1, VC4 is implemented.
0	k_gbl_pcie_20	**k_gbl[0]: PCI Express specification compliance.** This variable should be set to 1. Value 0 is used for backwards-compatibility with PCIe Specification 1.0a.

Bit(s)	Name	Description

1A143004 K_GBL_2 Global configuration registers: the 2nd DW 40004004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_gbl_comp_tlp_bypass	k_gbl_pipe_turn_off_en	k_gbl_ct_mode_en	k_gbl_big_end	k_gbl_pcie_mode_sel	k_gbl_rsv										
Type	RW	RW	RW	RW	RW	RW										
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_gbl_rsv	k_err_lane_en	k_gbl_ignore_train_ctrl	k_gbl_elect_idle_en	k_gbl_x2_down_cfg	k_gbl_lane_ignore								k_gbl_speed_sup	k_gbl_trans_layer_bypass	k_gbl_ecrc_imp
Type	RW	RW	RW	RW	RW	RW								RW	RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
31	k_gbl_comp_tlp_bypass	**k_gbl[63]: Receive buffer bypass for completion TLPs** This variable should be set to 0. Set to 1 means completion TLPs can bypass the Receive buffer.
30	k_gbl_pipe_turn_off_en	**k_gbl[62]: 1 = "turn off" mechanism described in the PIPE Interface specifications is enabled.**
29	k_gbl_ct_mode_en	**k_gbl[61]: 1 = enable CT mode (for switch designs only).**
28	k_gbl_big_end	**k_gbl[60]** - 0: Little-endian data flow - 1: Big-endian data flow
27	k_gbl_pcie_mode_sel	**k_gbl[59]** Only for pcie configuration include pcie and mpcie.

Bit(s)	Name	Description
		0 : pcie 1 : mpcie
26:15	k_gbl_rsv	**k_gbl[58:47]: reserved**
14	k_err_lane_en	**k_gbl[46]** 0 : disable detect lane data error. 1 : enable detect lane data error.
13	k_gbl_ignore_train_ctrl	**k_gbl[45]: 1 = all training control bits (except hot reset) in training order sets are ignored.**
12	k_gbl_elect_idle_en	**k_gbl[44]** - 0: Inferred Electrical Idle disabled. - 1: Inferred Electrical Idle enabled.
11	k_gbl_x2_down_cfg	**k_gbl[43]: 0 enables x2 Down Configuration.** This means that x2 lane configuration is possible when a link down configuration (recovery) from x4 or x8 occurs.
10:3	k_gbl_lane_ignore	**k_gbl[42:35]: 1 = the corresponding PCIe lane is ignored.** - k_gbl[35]:PCIe lane 0 ignored - k_gbl[36]:PCIe lane 1 ignored - k_gbl[37]:PCIe lane 2 ignored - k_gbl[38]:PCIe lane 3 ignored - k_gbl[39]:PCIe lane 4 ignored - k_gbl[40]:PCIe lane 5 ignored - k_gbl[41]:PCIe lane 6 ignored - k_gbl[42]:PCIe lane 7 ignored
2	k_gbl_speed_sup	**k_gbl[34]: Speed support.** - 0: implements 2.5 Gbps speed support. - 1: implements both 2.5 and 5.0 Gbps speed support.
1	k_gbl_trans_layer_bypass	**k_gbl[33]: Transaction layer bypass** This variable should be set to 0. Set to 1 means the transaction layer is bypassed.
0	k_gbl_ecrc_imp	**k_gbl[32]: 1 = ECRC forwarding to and from the Application Layer implemented.**

Bit(s)	Name	Description

1A143008 K_DP Device & Port setup 00000020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**k_port**								**k_dev**				
Type				RW								RW				
Reset				0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
12:5	k_port	**Port Link number.**
4:0	k_dev	**Indicates the device number for Switch or Rootport components.**

1A14300C K_CNT_0 Counter-related Configurations 1 0140FF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**k_cnt_pwr_trans_delay_cnt**								**k_cnt_dummy_inst_stop**				**k_cnt_rsv**
Type				RW								RW				RW
Reset				0	0	0	0	1	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_cnt_clk_elect_idle**								**k_cnt_rx_cdc_almost_full**				**k_cnt_tx_cdc_almost_full**			
Type	RW								RW				RW			
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:21	k_cnt_pwr_trans_delay_cnt	**k_cnt[64:57]: Powerdown Transition Delay Counter.**

Bit(s)	Name	Description
		Delays the transition to powerdown phase when a TXELECIDLE signal is asserted in states where the RXELECIDLE signal is not used (such as Los, detect, disable and hot reset). Note:The recommended value of this counter is 10.
20:17	k_cnt_dummy_inst_stop	**k_cnt[56:53]: Value used for stopping dummy insertion at the CDC Transmit FIFO when the Almost Full condition is reached. Used when k_gbl(24:23)="01" (user clock is used and CDC compensates for plesiochronous relation).** Note:When set to 0000, the Core defaults to 1011.
16	k_cnt_rsv	**k_cnt[52]: reserved**
15:8	k_cnt_clk_elect_idle	**k_cnt[51:44]: Number of clock cycles for inferring Electrical Idle exit when Core Rx lanes are in Los state.** This value is used when k_conf_func0[371] is asserted.
7:4	k_cnt_rx_cdc_almost_full	**k_cnt[43:40]:Rx CDC Almost Full condition** Indicates when the CDC Receive FIFO is almost full. Note:When set to 0000, the Core defaults to 1011.
3:0	k_cnt_tx_cdc_almost_full	**k_cnt[39:36]:Tx CDC Almost Full condition** Indicates when the CDC Transmit FIFO is almost full. Note:When set to 0000, the Core defaults to 1011.

1A143010 K_CNT_1 Counter-related Configurations 2 0001E847

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		k_cnt_skp_os_cnt											k_cnt_recov_speed_cnt			
Type		RW											RW			
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_cnt_recov_speed_cnt															

Type	RW															
Reset	1	1	1	0	1	0	0	0	0	1	0	0	0	1	1	1

Bit(s)	Name	Description
30:20	k_cnt_skp_os_cnt	**k_cnt[95:85]: SKP OS Scheduling Counter.** When set to 0000, the Core defaults to the PCIe Specification value (0x252).
19:0	k_cnt_recov_speed_cnt	**k_cnt[84:65]: Recovery.Speed Counter** Counts 1 ms using uclk when the LTSSM state is Recovery.Speed (applies to 5.0 Gbps configuration speed only). See the PCI Express Specifications. Default : 125MHz

1A143014 K_CNT_2 Counter-related Configurations 3 C8042341

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_cnt_fc_to_check								k_cnt_l1_entry_lat							
Type	RW								RW							
Reset	1	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_cnt_los_entry_lat					k_cnt_fc_init_timer					k_cnt_2_rsv			k_cnt_max_payload_size		
Type	RW					RW					RW			RW		
Reset	0	0	1	0	0	0	1	1	0	1	0	0	0	0	0	1

Bit(s)	Name	Description
31:24	k_cnt_fc_to_check	**k_cnt[127:120]: Flow Control Time-Out Check (1us unit).** If the Core does not receive an update flow control packet within the time range specified by this counter, it transitions to Recovery state.
23:16	k_cnt_l1_entry_lat	**k_cnt[178:171] : L1 entry latency (256ns unit)** When the Core remains idle for the time range specified by this counter, it transitions to L1 state.
15:11	k_cnt_los_entry_lat	**k_cnt[111:107]: Los entry latency (256ns unit)**

Bit(s)	Name	Description
		When the Core remains idle for the time range specified by this counter, it transitions to Los state.
10:6	k_cnt_fc_init_timer	**k_cnt[106:102]: FC init timer (256ns unit)** Time between consecutive sets of init flow control sent for VCs other than VC0.
5:3	k_cnt_2_rsv	**k_cnt[101:99] not used**
2:0	k_cnt_max_payload_size	**k_cnt[98:96]** Device Control Register.Max_payload_Size - 000: 128 bytes - 001: 256 bytes - 010: 512 bytes - 011: 1024 bytes - 100: 2048 bytes - 101: 4096 bytes - 110: reserved - 111: reserved

1A143018 K_CNT_3 Counter-related Configurations 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		k_cnt_replay_to														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		k_cnt_ack_lat_to														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:16	k_cnt_replay_to	**k_cnt[157:143]: Timeout value for the Replay timer. When set to 0, the Core defaults to the PCIe Specification value.**

Bit(s)	Name	Description
14:0	k_cnt_ack_lat_to	**k_cnt[142:128]: Timeout value for the ACK latency timer. When set to 0, the Core defaults to the PCIe Specification value.**

1A14301C K_CNT_4 Counter-related Configurations 5 14BD0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			k_cnt_cpl_timeout						k_cnt_read_request_size			k_cnt_fc_update_timer				
Type			RW						RW			RW				
Reset			0	1	0	1	0	0	1	0	1	1	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				k_aux_tick					k_cnt_pwr_down_to				k_cnt_txelecidle_lat			
Type				RW					RW				RW			
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:24	k_cnt_cpl_timeout	**Completion timeout value (1ms unit).** 6'h0 means completion timeout event will never occurs.
23:21	k_cnt_read_request_size	**Device Control Register.Max_Read_Request_Size** This field sets the maximum read request size for the function as a Requester. The function must not generate read requests with a size exceeding the set value. - 000: 128 bytes - 001: 256 bytes - 010: 512 bytes - 011: 1024 bytes - 100: 2048 bytes - 101: 4096 bytes - 110: reserved - 111: reserved

Bit(s)	Name	Description
20:16	k_cnt_fc_update_timer	**k_cnt[116:112]: Update Flow Control Credit Timer (1us unit).** The Core sends update flow control packets when this timer expires.
12:8	k_aux_tick	**k_cnt[170:166]:ticks of auxclk in one us. Used for timer in L1.2 state.** 00:1 tick (1MHz) 01:2 ticks (2MHz) 02:3 ticks (3MHz) 03:4 ticks (4MHz) 04:5 ticks (5MHz) 05:6 ticks (6MHz) 06:8 ticks (8MHz) 07:10 ticks (10MHz) 08:12 ticks (12MHz) 09:16 ticks (16MHz) 0A:20 ticks (20MHz) 0B:22 ticks (22MHz) 0C:26 ticks (26MHz) 0D:30 ticks (30MHz) 0E:32 ticks (32MHz) 0F:36 ticks (36MHz) 10:40 tick (40MHz) 11:44 ticks (44MHz) 12:48 ticks (48MHz) 13:50 ticks 14:56 ticks 15:60 ticks 16:64 ticks 17:72 ticks 18:80 ticks

Bit(s)	Name	Description
		19:84 ticks 1A:88 ticks 1B:92 ticks 1C:96 ticks 1D:100 ticks 1E:112 ticks 1F:128 ticks
7:4	k_cnt_pwr_down_to	**k_cnt[165:162]: Configurable powerdown timeout.** Sets the maximum time (in ms) allowed for PHY to acknowledge a powerdown transition. This timeout prevents an LTSSM freeze caused by a missing PHY acknowledge after a powerdown request. The default value of 0 means that no timeout is used.
3:0	k_cnt_txelecidle_lat	**k_cnt[161:158]: Sets the latency for the assertion of the pipe signal TXELECIDLE after the Electrical Idle Order Set (EIOS) is sent.**

1A143020 K_RTRY Replay Buffer Information 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_rtry_replay**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	k_rtry_replay	**Replay Buffer Last Active Address: For Replay buffers whose size is 2G_RTRY_BUF, this input is set to all 1s.**

1A143024 MISC_CONF Misllaneous Configuration 00000006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														slotclk_cfg	mode	
Type														RW	RW	
Reset														1	1	0

Bit(s)	Name	Description
2	slotclk_cfg	**Slot Clock Configuration: This variable is used to inform the Configuration Space if the PHY uses the same Reference Clock as the slot (Receive in Upstream mode, Transmit in Downstream mode).** - 0: independent clock. - 1 slot clock. This signal is synchronous to the UCLK.
1:0	mode	**Mode: This variable indicates the type of Core configuration.** Whhe Core is implemented in Endpoint/Rootport Shared Silicon mode: - 00: Native Endpoint. - 01: Legacy Endpoint. - 1x: Rootport. When the Core is implemented in Switch upstream/downstream port shared silicon mode: - 00: Native Endpoint. - 01: Legacy Endpoin. - 10: Switch downstream port. - 11: Switch upstream port. Mode selection should be performed when the Core is in a reset state.

1A143030 K_FC_VC0_0 Flow Control Information for Virtual Cannel 0 (similar for VC1-7) - the 1st DW 01008020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_fc_vc0_0															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_fc_vc0_0															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:0	k_fc_vc0_0	**Credit VC 0: This variable provides flow control information for VC0.** - k_vc0[7:0]: Receive flow control credit for Posted Headers. - k_vc0[19:8]: Receive flow control credit for Posted Data. - k_vc0[27:20]: Receive flow control credit for Non-Posted Headers. The corresponding registers for VC1-VC7 of K_FC_VC0_0 (0030h) to k_PTR_VC0_3 (0044h) range from 0048h to 00ECh, subsequently. For example, for VC1, the registers take the address range 0048h-005Ch...etc

1A143034 K_FC_VC0_1 Flow Control Information for Virtual Cannel 0 (similar for VC1-7) - the 2nd DW 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									k_fc_vc0_1							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_fc_vc0_1															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
23:0	k_fc_vc0_1	**Credit VC 0: This variable provides flow control information for VC0.** - k_vc0[35:28]: Receive flow control credit for Non-Posted Data. - k_vc0[43:36]: Receive flow control credit for Completion Headers. - k_vc0[55:44]: Receive flow control credit for Completion Data. The corresponding registers for VC1-VC7 of K_FC_VC0_0 (0030h) to k_PTR_VC0_3 (0044h) range from 0048h to 00ECh, subsequently. For example, for VC1, the registers take the address range 0048h-005Ch...etc

1A143038 K_PTR_VC0_0 Recive Buffer Pointers VC 0 (similar for VC1-7) - the 1st DW 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_ptr_vc0_pc_min**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	k_ptr_vc0_pc_min	**Pointer 0: Pointer signals maintain address boundaries for Posted and Non-Posted requests stored in the Receive buffer.** [G_RX_BUF - 1:0]: pc_min0: The minimum Receive buffer address for Posted requests stored in DPRAM.

Bit(s)	Name	Description
		The corresponding registers for VC1-VC7 of K_FC_VC0_0 (0030h) to k_PTR_VC0_3 (0044h) range from 0048h to 00ECh, subsequently. For example, for VC1, the registers take the address range 0048h-005Ch...etc

1A14303C K_PTR_VC0_1 Recive Buffer Pointers VC 0 (similar for VC1-7) - the 2nd DW 000003BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_ptr_vco_pc_max**															
Type	RW															
Reset	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	k_ptr_vco_pc_max	**[2 X G_RX_BUF -1:G_RX_BUF]: pc_max0** The maximum Receive buffer address for Posted requests stored in DPRAM. The corresponding registers for VC1-VC7 of K_FC_VC0_0 (0030h) to k_PTR_VC0_3 (0044h) range from 0048h to 00ECh, subsequently. For example, for VC1, the registers take the address range 0048h-005Ch...etc

1A143040 K_PTR_VC0_2 Recive Buffer Pointers VC 0 (similar for VC1-7) - the 3rd DW 000003C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_ptr_vc0_np_min															
Type	RW															
Reset	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	k_ptr_vc0_np_min	**[3 X G_RX_BUF -1: G_RX_BUF X 2]: np_mino** The minimum Receive buffer address for Non-Posted requests stored in DPRAM. The corresponding registers for VC1-VC7 of K_FC_VC0_0 (0030h) to k_PTR_VC0_3 (0044h) range from 0048h to 00ECh, subsequently. For example, for VC1, the registers take the address range 0048h-005Ch...etc

1A143044 K_PTR_VC0_3 Recive Buffer Pointers VC 0 (similar for VC1-7) - the 4th DW 000003FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_ptr_vc0_np_max															
Type	RW															
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	k_ptr_vc0_np_max	**[4 X G_RX_BUF -1: G_RX_BUF X 3]: np_maxo** The maximum Receive buffer address for Non-Posted requests stored in DPRAM.

Bit(s)	Name	Description
		The corresponding registers for VC1-VC7 of K_FC_VC0_0 (0030h) to k_PTR_VC0_3 (0044h) range from 0048h to 00ECh, subsequently. For example, for VC1, the registers take the address range 0048h-005Ch...etc

1A143100 K_CONF_FUNC0_0 Configuration Space Header 00h 32580E8D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_dev_id															
Type	RW															
Reset	0	0	1	1	0	0	1	0	0	1	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_conf_vendor_id															
Type	RW															
Reset	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0	1

Bit(s)	Name	Description
31:16	k_conf_dev_id	**k_conf[31:16]: Device ID**
15:0	k_conf_vendor_id	**k_conf[15:0]: Vendor ID**

1A143104 K_CONF_FUNC0_1 Configuration Space Header 08h 00020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_class_code															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_conf_class_code								k_conf_rev_id							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	k_conf_class_code	**k_conf[63:40]: Class code.**
7:0	k_conf_rev_id	**k_conf[39:32]: Revision ID**

1A143108 K_CONF_FUNC0_2 Configuration Space Header 2Ch 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**k_conf_subsys_dev_id**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_conf_subsys_vendor_id**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	k_conf_subsys_dev_id	**k_conf[95:80]: Subsystem device ID**
15:0	k_conf_subsys_vendor_id	**k_conf[79:64]: Subsystem vendor ID**

1A14310C K_CONF_FUNC0_3 Individual function 0 configuration, the 4th DW 000001C1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**k_conf_rej_snoop_trans**								**k_conf_vc_arb_cap**				**k_conf_lpvc_num**			**k_conf_aer_en**
Type	RW								RW				RW			RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_conf_pme_sup**					**k_conf_d2_sup**	**k_conf_d1_sup**	**k_conf_max_current**			**k_conf_dsi**	**k_conf_pme_imp**	**k_conf_pme_clk**		**k_conf_flr_cap**	**k_conf_no_soft_rst**

Type	RW					RW	RW	RW			RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	1	1	1	0	0	0		0	1

Bit(s)	Name	Description
31:24	k_conf_rej_snoop_trans	**k_conf_FUNC1[127:120]: Reject Snoop Transaction (VC Resource Capability Register).** This variable is reserved for future use and should be set to 0.
23:20	k_conf_vc_arb_cap	**k_conf_FUNC1[119:116]: VC arbitration capabilities (Port VC Capability Register 2).** This variable should be hardwired to 0001 (simple RR).
19:17	k_conf_lpvc_num	**k_conf_FUNC1[115:113]: Number of Low Priority VCs (LPVC)** (Port VC Capability Register 1)
16	k_conf_aer_en	**k_conf_FUNC1[112]: 1 = Advanced Error Reporting enabled.**
15:11	k_conf_pme_sup	**k_conf_FUNC1[111:107]: PME Support (PMC).** This signal indicates the PM states within which a Power Management Event (PME) message can be sent. A bit set to 0 indicates that a message cannot be sent in the respective state. - k_conf_FUNC1[107]: D0 PME - k_conf_FUNC1[108]: D1 PME - k_conf_FUNC1[109]: D2 PME - k_conf_FUNC1[110]: D3 hot PME - k_conf_FUNC1[111]: D3 cold
10	k_conf_d2_sup	**k_conf[106]: D2 support (PMC).**
9	k_conf_d1_sup	**k_conf[105]: D1 support (PMC).**
8:6	k_conf_max_current	**k_conf[104:102]: Maximum Current Required (PMC).** - 111: 375 mA - 110: 320 mA - 101: 270 mA - 100: 220 mA - 011: 160 mA - 010: 100 mA

Bit(s)	Name	Description
		- 001: 55 mA - 000: 0 mA (If either D3Cold or PM Data Register are not checked
5	k_conf_dsi	**k_conf[101]: Device-specific initialization (DSI) (Power Management Capabilities)**
4	k_conf_pme_imp	**k_conf[100]:** - 0: Power Management Capability Structure registers not implemented - 1: Power Management Capability Structure registers implemented
3	k_conf_pme_clk	**k_conf[99]: PME clock** Does not apply to PCI Express and must be hardwired to 0.
1	k_conf_flr_cap	**k_conf[97]: Function Level Reset (FLR) capability for Endpoints only (Device Capabilities Register).** - 0: Function does not support FLR - 1: Function supports FLR When the port is not an Endpoint, this register is set to 0.
0	k_conf_no_soft_rst	**k_conf[96]: No Soft Reset (PMCSR).** - 0: Devices perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset, and the full reinitialization sequence is required to return the device to D0 Initialized. - 1: Devices transitioning from D3hot to D0 due to PowerState commands do not perform an internal reset. No additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. Note: if PME is enabled, then devices that transition from D3hot to D0 via a system or bus segment reset will return to the D0 Uninitialized device state with only the PME context preserved

1A143110 K_CONF_FUNC0_4 Individual function 0 configuration, the 5th DW 27088341

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_l1_exit_lat_sep			k_conf_l1_exit_lat_com			k_conf_l1	k_conf_lo	k_conf_max_link_width						k_conf_slot_pwr_scale	

							s_sup	s_sup								
Type	RW			RW			RW	RW	RW						RW	
Reset	0	0	1	0	0	1	1	1	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_conf_rcb**	**k_conf_pwr_ind_present**	**k_conf_att_ind_present**	**k_conf_att_but_present**	**k_conf_l1s_lat**			**k_conf_los_lat**			**k_conf_ext_tag_sup**	**k_conf_dlink_active_rpt**	**k_conf_surp_down_rpt**	**k_conf_max_payload**		
Type	RW	RW	RW	RW	RW			RW			RW	RW	RW	RW		
Reset	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	k_conf_l1_exit_lat_sep	**k_conf_FUNC1[159:157]: L1 exit latency for separated clock (Link Capabilities Register).**
28:26	k_conf_l1_exit_lat_com	**k_conf_FUNC1[156:154]: L1 exit latency for common clock (Link Capabilities Register).**
25	k_conf_l1s_sup	**k_conf_FUNC1[153]: L1 Active State power management support (Link Capabilities Register).**
24	k_conf_los_sup	**k_conf_FUNC1[152]: Los Active State power management support (Link Capabilities Register).**
23:18	k_conf_max_link_width	**k_conf_FUNC1[151:146]: Max Link width (Link Capabilites Register).** - 00 000b: Reserved - 00 0001b: x1 - 00 0010b: x2 - 00 0100b: x4 - 00 1000b: x8 - 00 1100b: x12 - 01 0000b: x16 - 10 0000b: x32
17:16	k_conf_slot_pwr_scale	**k_conf_FUNC1[145:144]: Slot Power Limit Scale (Device Capabilities Register)** From Set_Slot_Power_Limit Message or hardwired to 00b.

Bit(s)	Name	Description
15	k_conf_rcb	**k_conf_FUNC1[143]: Read Completion Boundary (RCB) support (Link Control Register).** - 0: 64 bytes - 1: 128 bytes
14	k_conf_pwr_ind_present	**k_conf_FUNC1[142]: Power indicator present for an Endpoint (Device Capabilities Register).**
13	k_conf_att_ind_present	**k_conf_FUNC1[141]: Attention indicator present for an Endpoint (Device Capabilities Register).**
12	k_conf_att_but_present	**k_conf_FUNC1[140]: Attention button present on the device (Device Capabilities Register).**
11:9	k_conf_l1s_lat	**k_conf_FUNC1[139:137]: Endpoint L1 acceptable latency (Link Capabilities Register).**
8:6	k_conf_los_lat	**k_conf_FUNC1[136:134]: Endpoint Los acceptable latency (Link Capabilities Register).**
5	k_conf_ext_tag_sup	**k_conf_FUNC1[133]: Extended TAG field supported (Device Capabilities Register).** - 0: 5-bit Tag field supported - 1: 8-bit Tag field supported
4	k_conf_dlink_active_rpt	**k_conf_FUNC1[132]: Data Link Layer active reporting capabilities (not available for PCIe 1.0a compliant Cores) (Link Capabilities Register).** Downstream Port: 1 = component can report the DL_Active state of the Data Link Control and Management state machine. Upstream Port: this variable is hardwired to 0.
3	k_conf_surp_down_rpt	**k_conf_FUNC1[131]: Surprise Down error reporting capabilities (not available for PCI Express Base Specification Revision 1.0a compliant Cores) (Link Capabilities Register).** Downstream Port: 1 = component can detect and report a Surprise Down error condition. Upstream Port: this variable is hardwired to 0.
2:0	k_conf_max_payload	**k_conf_FUNC1[130:128]: Max payload size supported (Device Capabilities Register).** - 000: 128 bytes - 001: 256 bytes - 010: 512 bytes - 011: 1024 bytes

Bit(s)	Name	Description
		- 100: 2048 bytes - 101: 4096 bytes Otherwise: Reserved

1A143114 K_CONF_FUNC0_5 Individual function 0 configuration, the 6th DW 00000080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_phy_slot_num													k_conf_electro_intlk_present	k_conf_slot_pwr_limit_value	
Type	RW													RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_conf_slot_pwr_limit_value								k_conf_clk_pwr_mgm_sup	k_conf_hot_plug						
Type	RW								RW	RW						
Reset	0	0	0	0	0	0			1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:19	k_conf_phy_slot_num	**k_conf_FUNC1[191:179]: Physical Slot Number (if slot implemented) (Slot Capabilities Register).** This signal indicates the physical slot number associated with this port and must be unique within the fabric.
18	k_conf_electro_intlk_present	**k_conf_FUNC1[178]: 1 = Electromechanical Interlock present (not available with PCIe 1.0a) (Slot Capabilities Register).**

Bit(s)	Name	Description
17:10	k_conf_slot_pwr_limit_value	**k_conf_FUNC1[177:170]: Slot Power Limit Value (Slot Capabilites Register).**
7	k_conf_clk_pwr_mgm_sup	**k_conf_FUNC1[167]: Clock power management support (Link Capabilities Register).**
6:0	k_conf_hot_plug	**k_conf_FUNC1[166:160]: Hot-plug feature (only applies to downstream ports and only when slot is implemented) (Slot Capabilities Register).** - k_conf_FUNC1[160]: 1 = Attention button implemented on the chassis - k_conf_FUNC1[161]: 1 = Power controller present - k_conf_FUNC1[162]: 1 = Manually Operated Retention Latch (MRL) sensor present - k_conf_FUNC1[163]: 1 = Attention indicator present for a Rootport, Switch, or Bridge. - k_conf_FUNC1[164]: 1 = Power indicator present for a Rootport, Switch, or Bridge. - k_conf_FUNC1[165]: Hot-plug surprise: 1 = device can be removed from this slot without prior notification. - k_conf_FUNC1[166]: 1 = Hot-plug capable

1A143118 K_CONF_FUNC0_6 Individual function 0 configuration, the 7th DW 0700FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_funco_6_rcv_27					k_conf_no_cmd_comp_sup	k_conf_ecrc_check	k_conf_ecrc_gen	k_conf_funco_6_rcv_21			k_conf_comp_to_dis_sup	k_conf_comp_to_range_sup			
Type	RO					RW	RW	RW	RO			RW	RW			
Reset	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_conf_fast_train_cfg															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:27	k_conf_func0_6_rcv_27	**Reserved**
26	k_conf_no_cmd_comp_sup	**k_conf_FUNC1[218]: (Slot Capabilities Register).** 1 = No command completed support (not available with PCIe 1.0a) When set, this bit indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug controller. This bit is only permitted to be set if the hot-plug capable port is able to accept writes to all fields of the Slot Control register without delay between successive writes.
25	k_conf_ecrc_check	**k_conf_FUNC1[217] (Advanced Error Capabilities and Control Register).** - 0: Disable ECRC check capability - 1: Enable ECRC check capability
24	k_conf_ecrc_gen	**k_conf_FUNC1[216] (Advanced Error Capabilities and Control Register).** - 0: Disable ECRC generation capability - 1: Enable ECRC generation capability
23:21	k_conf_func0_6_rcv_21	**Reserved**
20	k_conf_comp_to_dis_sup	**k_conf_FUNC1[212]: 1 = Completion timeout mechanism disable support (Device Capabilities 2 Register).** When set to 0, the Core use the default completion timeout period of 50 ms for each transaction. This setting is optional for Rootports, but must be hardwired to 0 for all other devices.
19:16	k_conf_comp_to_range_sup	**k_conf_FUNC1[211:208]: Completion timeout range supported (Device Capabilities 2 Register).** - 0000: Completion timeout programming not supported. The function must implement a timeout value in the range 50us ~ 50ms. - 0001: 50us ~ 10ms - 0010: 10ms ~ 250ms - 0011: 50us ~ 250ms - 0110: 10ms ~ 4s - 0111: 50us ~ 4s - 1110: 10ms ~ 4s - 1111: 50us ~ 4s

Bit(s)	Name	Description
15:0	k_conf_fast_train_cfg	**k_conf_FUNC1[207:192]:** - k_conf_FUNC1[199:192]: NFTS_SEPCLK: Number of fast training sequences for the separate clock at 2.5Gbps. - k_conf_FUNC1[207:200]: NFTS_COMCLK: Number of fast training sequences for the common clock at 2.5Gbps.

1A14311C K_CONF_FUNC0_7 Individual function 0 configuration, the 8th DW 20000068

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_lpbk_exit_tim								k_conf_func0_7_rsv23	k_conf_msix_tab_size						
Type	RW								RO	RW						
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_conf_msix_tab_size				k_conf_msix_sup	k_conf_func0_7_rsv9		k_conf_int_pin			k_conf_msi_sup	k_conf_msi_per_bit_mask	k_conf_msi_addr_mode	k_conf_msi_num		
Type	RW				RW	RO		RW			RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0

Bit(s)	Name	Description
31:24	k_conf_lpbk_exit_tim	**extend txdetectrx when exiting loopback mode for 8 EIOS** 8ns~1024ns, 8ns/scale
23	k_conf_func0_7_rsv23	**Reserved**
22:12	k_conf_msix_tab_size	**k_conf_FUNC1[305:295]: MSI-X Table Size**
11	k_conf_msix_sup	**k_conf_FUNC1[230]: 1 = Function supports MSI-X**
10:9	k_conf_func0_7_rsv9	**Reserved**

Bit(s)	Name	Description
8:6	k_conf_int_pin	**k_conf_FUNC1[227:225]: Interrupt pin (Configuration Space Header)** - 0: Do not use INTx pin - 1: Use INTA pin - 2: Use INTB pin - 3: Use INTC pin - 4: Use INTD pin Otherwise: reserved
5	k_conf_msi_sup	**k_conf_FUNC1[224]:** - 0: Function not support MSI - 1: Function supports MSI
4	k_conf_msi_per_bit_mask	**k_conf_FUNC1[223]: MSI per-bit vector masking (read-only field) (Message Control)**
3	k_conf_msi_addr_mode	**k_conf_FUNC1[222]: MSI 32/64-bit addressing mode (Message Control).** - 0: 32 bits addressing only - 1: 32 or 64 bits addressing available
2:0	k_conf_msi_num	**k_conf_FUNC1[221:219]: Number of MSI the function can generate (Message Control).** - 000: 1 MSI - 001: 2 MSI - 010: 4 MSI - 011: 8 MSI - 100: 16 MSI - 101: 32 MSI

1A143120 K_CONF_FUNC0_8 Individual function 0 configuration, the 9th DW 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_msix_pba_offset															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_conf_msix_pba_offset**													**k_conf_msix_pba_bir**		
Type	RW													RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:3	k_conf_msix_pba_offset	**k_conf_FUNC1[262:234]: MSI-X PBA Offset**
2:0	k_conf_msix_pba_bir	**k_conf_FUNC1[233:231]: MSI-X PBA BIR**

1A143124 K_CONF_FUNC0_9 Individual function 0 configuration, the 10th DW 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**k_conf_msix_tab_offset**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_conf_msix_tab_offset**													**k_conf_msix_tab_bir**		
Type	RW													RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:3	k_conf_msix_tab_offset	**k_conf_FUNC1[294:266]: MSI-X Table Offset**
2:0	k_conf_msix_tab_bir	**k_conf_FUNC1[265:263]: MSI-X Table BIR**

1A143128 K_CONF_FUNC0_10 Individual function 0 configuration, the 11th DW 013FFFE0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**k_conf_funco_10_rcv_27**					**k_conf_ver_cap**				**k_conf_sel_d**	**k_conf_nfts_comclk**					

										ee mp						
Type	RO					RW				RW	RW					
Reset	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_conf_nfts_comclk**		**k_conf_nfts_sepclk**								**k_conf_eie_num**				**k_conf_ssid_cap_imp**	**k_conf_vga_en**
Type	RW		RW								RW				RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
31:27	k_conf_func0_10_rcv_27	**Reserved**
26:23	k_conf_ver_cap	**k_conf_FUNC1[364:361]:** PCI Express specification version capability - 0001: Core is compliant with PCIe Specification 1.0a or 1.1 (depending on the setting for k_gbl[0] - 0010: Core is compliant with PCIe Specification 2.0
22	k_conf_sel_deemp	**k_conf_FUNC1[360]: Selectable de-emphasis** Selects the level of de-emphasis for an upstream component when the link is operating at 5.0 Gbps - 0: de-emphasis of 6 dB - 1: de-emphasis of 3.5 dB When the link is operating at 2.5 Gbps, this variable should be hardwired to 0.
21:14	k_conf_nfts_comclk	**k_conf_FUNC1[359:352]: NFTS_COMCLK** Number of fast training sequences for the common clock at 5.0 Gbps. Minimum is 5.
13:6	k_conf_nfts_sepclk	**k_conf_FUNC1[351:344]: NFTS_SEPCLK**

Bit(s)	Name	Description
		Number of fast training sequences for the separate clock at 5.0 Gbps. Minimum is 5.
5:2	k_conf_eie_num	**k_conf_FUNC1[343:340]: Number of Electrical Idle Exit (EIE) symbols sent before transmitting the first FTS.** For the 8-bit PIPE version of the Core, any value between 4-8 is permitted, but for the 16-bit PIPE version, only the values 6 and 8 are permitted. The default value for both versions is 8.
1	k_conf_ssid_cap_imp	**k_conf_FUNC1[307]: 1 = SSID/SSVID capabilities implemented (Bridge ports only)**
0	k_conf_vga_en	**k_conf_FUNC1[306]: 1 = VGA Enable (Bridge ports only)**

1A14312C K_CONF_FUNC0_11 Individual function 0 configuration, the 12th DW 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_ssid															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_conf_ssvid															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	k_conf_ssid	**k_conf_FUNC1[339:324]: SSID (Bridge ports only)**
15:0	k_conf_ssvid	**k_conf_FUNC1[323:308]: SSVID (Bridge ports only)**

1A143130 K_CONF_FUNC0_12 Individual function 0 configuration, the 13th DW 051F1E40

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		k_arb_check_cred	k_lock_support	k_power_on_value						k_power_on_scale		k_l1ss_supported				
Type		RW	RW	RW						RW		RW				
Reset		0	0	0	0	1	0	1		0	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_rxlos_exit_tim									k_conf_elect_idle_exit	k_conf_los_exit_lat_sep			k_conf_los_exit_lat_com		
Type	RW									RW	RW			RW		
Reset	0	0	0	1	1	1	1	0		1	0	0	0	0	0	0

Bit(s)	Name	Description
30	k_arb_check_cred	
29	k_lock_support	
28:24	k_power_on_value	**Along with the k_power_on_scale field in the L1SS capabilities register sets the time (in us) that thist requires the port on the opposite side of Link to wait in L1.2 exit after sampling CLKREQ# asserted before actively driving the interface. The value of T_POWER_ON is calculated by multiplying the value in this field by the scale in this field by the scale value.**
22:21	k_power_on_scale	**Specifies the scale used for the k_power_on_value field in the L1SS capabilities register** 00 : 2us 01 : 10us 10 : 100us 11: Reserved
20:16	k_l1ss_supported	**k_l1ss_supported[0] : PCI-PM L1.2 supported** k_l1ss_supported[1] : PCI-PM L1.1 supported k_l1ss_supported[2] : ASPM L1.2 supported k_l1ss_supported[3] : ASPM L1.1 supported

Bit(s)	Name	Description
		k_l1ss_supported[4] : L1SS supported
15:8	k_rxlos_exit_tim	**L1ss_common_mode_restore_time capability.** The register will be used to Port_Common_Mode_Restore_Time in L1SS capability regiseter (offset 0x04) The register shall be Local PHY TX common mode restore time.
6	k_conf_elect_idle_exit	**k_conf_FUNC1[371]: Electrical Idle exit condition** This signal defines when the Core exits Electrical Idle. - 0: Exit Electrical Idle when the signal RXELECIDLE is de-asserted for all configured lanes (normal operation). - 1: When the Core Rx lanes are in Los or L1 state, exit Electrical Idle after the signal RXELECIDLE is inactive for the number of clock cycles defined by k_cnt[51:44].
5:3	k_conf_los_exit_lat_sep	**k_conf_FUNC1[370:368]: Los exit latency for separated clock at 5 Gbps (Link Capabilities Register).** - 000: < 64ns - 001: 64ns ~ 128ns - 010: 128ns ~ 256ns - 011: 256ns ~ 512ns - 100: 512ns ~ 1us - 101: 1us ~ 2us - 110: 2us ~ 4us - 111: > 4us
2:0	k_conf_los_exit_lat_com	**k_conf_FUNC1[367:365]: Los exit latency for common clock at 5 Gbps (Link Capabilities Register).** - 000: < 64ns - 001: 64ns ~ 128ns - 010: 128ns ~ 256ns - 011: 256ns ~ 512ns - 100: 512ns ~ 1us

Bit(s)	Name	Description
		- 101: 1us ~ 2us - 110: 2us ~ 4us - 111: > 4us

1A143134 K_BAR_FUNC0_0 BAR0 Configuration. Note:A BAR cannot be modified if the previous BAR uses 64-bit addressing. FFF00004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_baro															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_baro															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
31:0	k_baro	**BAR0[31:0]** - BAR0[0]: I/O Space - BAR0[2:1]: Memory Space -> 10: 64-bit address -> 00: 32-bit address - BAR0[3]: Prefetchable - BAR0[31:4]: Bar size mask

1A143138 K_BAR_FUNC0_1 BAR1 Configuration. FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_bar1															
Type	RW															

Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_bar1**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	k_bar1	**BAR1[63:32]** - BAR1[32]: I/O Space - BAR1[34:33]: Memory Space (see bit settings for BAR0) - BAR1[35]: Prefetchable - BAR1[63:36]: Bar size mask

1A14313C K_BAR_FUNC0_2 BAR2 Configuration. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**k_bar2**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_bar2**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	k_bar2	**BAR2[95:64]** - BAR2[64]: I/O Space - BAR2[66:65]: Memory Space (see bit settings for BAR0) - BAR2[67]: Prefetchable - BAR2[95:68]: Bar size mask

1A143140 K_BAR_FUNC0_3 BAR3 Configuration. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_bar3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_bar3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	k_bar3	**BAR3[127:96]** - BAR3[96]: I/O Space - BAR3[98:97]: Memory Space (see bit settings for BAR0) - BAR3[99]: Prefetchable - BAR3[127:100]: Bar size mask

1A143144 K_BAR_FUNC0_4 BAR4 Configuration. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_bar4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_bar4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	k_bar4	**BAR4[159:128]** - BAR4[128]: I/O Space

Bit(s)	Name	Description
		- BAR4[130:129]: Memory Space (see bit settings for BAR0) - BAR4[131]: Prefetchable - BAR4[159:132]: Bar size mask

1A143148 K_BAR_FUNC0_5 BAR5 Configuration. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_bar5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_bar5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	k_bar5	**BAR5[191:160]** - BAR5[160]: I/O Space - BAR5[162:161]: Memory Space (see bit settings for BAR0) - BAR5[163]: Prefetchable - BAR5[191:164]: Bar size mask

1A14314C K_BAR_FUNC0_6 Expansion ROM Configuration 1. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_bar_exp_rom_mask															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_bar_exp_rom_mask															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	k_bar_exp_rom_mask	**k_bar_func[223:192]: Bar size mask**

1A143150 K_BAR_FUNC0_7 Expansion ROM Configuration 2. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**k_bar_exp_rom_pref**		**k_bar_exp_rom_mode**	
Type													RW		RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3:2	k_bar_exp_rom_pref	**k_bar_FUNC1[227:226] prefetchable** - 00: not implemented - 01: prefetchable 32 - 11: prefetchable 64
1:0	k_bar_exp_rom_mode	**k_bar_FUNC1[225:224]: IO** - 00: no IO windows - 01: IO 16 bit - 11: IO 32 bit

1A143154 K_CONF_LTR_OBFF LTR AND OBFF Support Hwinit 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											k_conf_obff_sup					k_conf_ltr_sup
Type											RW					RW
Reset											0	0				1

Bit(s)	Name	Description
5:4	k_conf_obff_sup	**- 00: OBFF not support** - 01: OBFF supprted using message signaling only - 10: OBFF suppoted using WAKE# signaling only - 11: OBFF suppoted using WAKE# and message signaling
0	k_conf_ltr_sup	**- 0: noT support LTR** - 1: support LTR

1A143158 K_CPL_RESOURCE Complete resource 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_cpl_resource															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	k_cpl_resource	

1A14315C L_LOCAL_TCOMMON_MODE Tcommon mode time requred by Local PHY RX 00000023

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**k_local_rx_tcommon_mode**							
Type									RW							
Reset									0	0	1	0	0	0	1	1

Bit(s)	Name	Description
7:0	k_local_rx_tcommon_mode	**The time for Local PHY RX to establish common mode when exit from L1P2.** unit : 1us

1A143180 K_CONF_FUNC0_13 MPCIe Configuration space capability 01010303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**k_mpcie_rxwidth_cap**								**k_mpcie_txwidth_cap**							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**k_mpcie_hsrate_cap**								**k_mpcie_hsgear_cap**	
Type							RW								RW	
Reset							1	1							1	1

Bit(s)	Name	Description
31:24	k_mpcie_rxwidth_cap	**MPCIe support RX land width capability** Bit 0 : x1 RX lane is supported Bit 1 : x2 RX lane is supported Bit 2 : x4 RX lane is supported

Bit(s)	Name	Description
		Bit 3 : x8 RX lane is supported
		Bit 4 : x12 RX lane is supported
		Bit 5 : x16 RX lane is supported
		Bit 6 : x32 RX lane is supported
		Bit7 : Reserved
23:16	k_mpcie_txwidth_cap	**MPCIe support TX land width capability**
		Bit 0 : x1 TX lane is supported
		Bit 1 : x2 TX lane is supported
		Bit 2 : x4 TX lane is supported
		Bit 3 : x8 TX lane is supported
		Bit 4 : x12 TX lane is supported
		Bit 5 : x16 TX lane is supported
		Bit 6 : x32 TX lane is supported
		Bit7 : Reserved
9:8	k_mpcie_hsrate_cap	**MPCIe support HS RATE capability**
		Bit 0 : RATE A
		Bit 1 : RATE B
1:0	k_mpcie_hsgear_cap	**MPCIe support HS GEAR capability**
		Bit 0 : Gear 1
		Bit 1 : Gear 2

1A143400 WDMA_PCIE_ADDR_L Write DMA start PCIe address LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	wdma_pciaddr_l															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdma_pciaddr_l															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	wdma_pciaddr_l	**This register specifies the LSB start PCIe address of the write DMA transfer. For IO, configuration and DW transfers this address must be 32-bit aligned.**

1A143404 WDMA_PCIE_ADDR_H Write DMA start PCIe address MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	wdma_pciaddr_h															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdma_pciaddr_h															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	wdma_pciaddr_h	**This register specifies the MSB start PCIe address of the write DMA transfer.**

1A143408 WDMA_BUS_ADDR Write DMA start BUS address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	wdma_bus_addr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdma_bus_addr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	wdma_bus_addr	**This register specifies the start bus address of the memory location where data must be read from. For IO, configuration and DW transfers this address must be 32-bit aligned.**

1A14340C WDMA_CONTROL Write DMA control parameters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	wdma_length															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdma_length				wdma_be				wdma_multi_outstanding	wdma_cmd			wdma_rsv_2		wdma_stop	wdma_start
Type	RW				RW				RW	RW			RO		WO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	wdma_length	**This field specifies the amount of data in byte unit. Burst transfer up to 1MB. IO, configuration and Memory DW transfers must be 4 bytes (0x00004). The value must not cross a 4GB address boundary.** 0x00001 & wdma_be = 4'b0 : 0B 0x00001 : 1B 0x00002 : 2B 0xFFFFF : (2^20-1)B 0x00000 : 1MB
11:8	wdma_be	**This field specifies the byte enable for IO, configuration and Memory DW transfers.**

Bit(s)	Name	Description
7	wdma_multi_outstanding	**WDMA can send multi memory read with different tag. But target must send completion in order.**
6:4	wdma_cmd	**This field specifies the PCIe command used to transfer data.** - 000: I/O Read (not allowed if device is a native EP) - 010: Memory Read DW - 100: Configuration Read (not allowed if device is an EP) - 110 Memory Read Burst
3:2	wdma_rsv_2	**Reserved**
1	wdma_stop	**This bit is used to abort a transfer in progress. A partial and unknown amount of data can be transferred before transfer stops.** Always returns 0 when read.
0	wdma_start	**Assertion of this bit initiates WDMA transfer. This bit is automatically cleared when the transfer is completed. This bit can be monitored by software in order to verify whether the WDMA channel is busy.** Note that the wdma_start is ignored if wdma_cmd is illigal or if wdma_length is null, in which case no transfer is initialted and no interrupt is generated.

1A143410 RDMA_PCIE_ADDR_L Read DMA start PCIe address LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rdma_pciaddr_l															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdma_pciaddr_l															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rdma_pciaddr_l	**This register specifies the LSB start PCIe address of the read DMA transfer. For IO, configuration and DW transfers this address must be 32-bit aligned.**

1A143414 RDMA_PCIE_ADDR_H Read DMA start PCIe address MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rdma_pciaddr_h															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdma_pciaddr_h															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rdma_pciaddr_h	**This register specifies the MSB start PCIe address of the read DMA transfer.**

1A143418 RDMA_BUS_ADDR Read DMA start BUS address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rdma_bus_addr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdma_bus_addr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rdma_bus_addr	**This register specifies the start bus address of the memory location where data must be written to.** For IO, configuration and DW transfers this address must be 32-bit aligned.

1A14341C RDMA_CONTROL Read DMA control parameters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rdma_length															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdma_length				rdma_be				rdma_rsv_7	rdma_cmd			rdma_rsv_2		rdma_stop	rdma_start
Type	RW				RW				RO	RW			RO		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	rdma_length	**This field specifies the amount of data in byte unit. Burst transfer up to 1MB. IO, configuration and Memory DW transfers must be 4 bytes (0x00004). The value must not cross a 4GB address boundary.** 0x00001 & rdma_be = 4'b0 : 0B 0x00001 : 1B 0x00002 : 2B 0xFFFFF : (2^20-1)B 0x00000 : 1MB
11:8	rdma_be	**This field specifies the byte enable for IO, configuration and Memory DW transfers.**
7	rdma_rsv_7	**Reserved**
6:4	rdma_cmd	**This field specifies the PCIe command used to transfer data.**

Bit(s)	Name	Description
		- 001: I/O Write (not allowed if device is a native EP) - 011: Memory Write DW - 101: Configuration Write (not allowed if device is an EP) - 111 Memory Write Burst
3:2	rdma_rsv_2	**Reserved**
1	rdma_stop	**This bit is used to abort a transfer in progress. A partial and unknown amount of data can be transferred before transfer stops.** Always returns 0 when read.
0	rdma_start	**Assertion of this bit initiates RDMA transfer. This bit is automatically cleared when the transfer is completed. This bit can be monitored by software in order to verify whether the RDMA channel is busy.** Note that the rdma_start is ignored if rdma_cmd is illigal or if rdma_length is null, in which case no transfer is initialted and no interrupt is generated.

1A143420 INT_MASK Interrupt Mask FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mpcie_cfg_soft_mask	pcie_rc_l2_wake_mask	legacy_pm_chg_mask	ltr_en_mask	ltr_msg_mask	cpu_active_mask	obff_mask	obff_idle_mask	msi_mask	aer_event_mask	pm_hp_event_mask	serr_mask	intd_mask	intc_mask	intb_mask	inta_mask
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_mask_rsv_15	b2p_disc ard_mask	b2p_rerr_mask	int_mask_rsv_12	p2b_wr_win1_mask	p2b_wr_win0_mask	p2b_rerr_mask	p2b_werr_mask	int_mask_rsv_7	rdma_berr_mask	rdma_perr_mask	rdma_end_mask	int_mask_rsv_3	wdma_berr_mask	wdma_perr_mask	wdma_end_mask
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	mpcie_cfg_soft_mask	**The bit indicate MPCIe LTSSM has entered cfg.software status and SW can start link discovery and configuration flow.** 1 : disable interrupt. 0 : enable interrupt.
30	pcie_rc_l2_wake_mask	**The bit indicate PCIe RC detect remote wakeup from EP in L2 state.** 1 : disable interrupt. 0 : enable interrupt.
29	legacy_pm_chg_mask	**This bit indicates that the PCI legacy power management state has been modified on the PCI PMCSR configuration register. In order to re-establish power state D0, the local processor must generate the PME# interrupt to PCI host processor.**
28	ltr_en_mask	**This bit asserts when LTR is enabled by RC.**
27	ltr_msg_mask	**This bit asserts when LTR message is received.**
26	cpu_active_mask	**This bit asserts when obff_cpu_active message is received.**
25	obff_mask	**This bit asserts when obff_obff message is received.**
24	obff_idle_mask	**This bit asserts when obff_idle message is received.**
23	msi_mask	**This bit is asserted each time an MSI interrupt is received. Local processor should clear this bit and read IMSISTATUS register to identify the interrupt source.** EP mode always returns 0.
22	aer_event_mask	**This bit is asserted each time an error is detected by AER if this feature is enabled. Local processor should clear this bit and then read AER capabilities registers located in configuration space to identify the error source.** EP mode always returns 0.
21	pm_hp_event_mask	**This bit is asserted each time a hot-plug or power management message is received. Local processor should clear this bit and then read Slot and Root CSR registers to identify the event source.** EP mode always returns 0.
20	serr_mask	**This bit is asserted when a system error is detected by the root port. Events and conditions that result in system errors are defined in PCI Express specification.** EP mode always returns 0.

Bit(s)	Name	Description
19	intd_mask	**This bit indicates when interrupt line INTD is asserted. Note the bit remains asserted (even if cleared by an AHB/AXI write) as long as INTD line is not de-asserted by EP.** EP mode always returns 0.
18	intc_mask	**This bit indicates when interrupt line INTC is asserted. Note the bit remains asserted (even if cleared by an AHB/AXI write) as long as INTC line is not de-asserted by EP.** EP mode always returns 0.
17	intb_mask	**This bit indicates when interrupt line INTB is asserted. Note the bit remains asserted (even if cleared by an AHB/AXI write) as long as INTB line is not de-asserted by EP.** EP mode always returns 0.
16	inta_mask	**This bit indicates when interrupt line INTA is asserted. Note the bit remains asserted (even if cleared by an AHB/AXI write) as long as INTA line is not de-asserted by EP.** EP mode always returns 0.
15	int_mask_rsv_15	**Reserved**
14	b2p_discard_mask	**This interrupt is issued to signal that the number of clock cycles specified by the AHB_TIMER register has been reached an that remaining data is being flushed.**
13	b2p_rerr_mask	**This interrupt is asserted if the data requested from the bus cannot be read by the PCIe.**
12	int_mask_rsv_12	**Reserved**
11	p2b_wr_win1_mask	**This interrupt is asserted when a write request received from the PCIe bus has been successfully posted to the AHB/AXI bus by the PCI2BUS window 1.**
10	p2b_wr_win0_mask	**This interrupt is asserted when a write request received from the PCIe bus has been successfully posted to the AHB/AXI bus by the PCI2BUS window 0.**
9	p2b_rerr_mask	**This interrupt is asserted when a read request is received from the PCIe but the corresponding data cannot be read from the AHB/AXI bus because an AHB/AXI error has occured.**
8	p2b_werr_mask	**This interrupt is asserted when a request received from the PCIe cannot be posted to the AHB/AXI bus because an AHB/AXI error has occured.**
7	int_mask_rsv_7	**Reserved**

Bit(s)	Name	Description
6	rdma_berr_mask	**This interrupt indicates that an error occured on the AHB/AXI bus reading or writing data. This is a fatal error and any data received should be discarded. The local processor should not try to restart the transfer.**
5	rdma_perr_mask	**This interrupt indicates that the requested DMA transfer was ended with an error on PCIe. This is a fatal error and any data received should be discarded. The local processor should not try to restart the transfer.**
4	rdma_end_mask	**This interrupt indicates that the requested DMA transfer is complete or has been stopped as a result of a software request.**
3	int_mask_rsv_3	**Reserved**
2	wdma_berr_mask	**This interrupt indicates that an error occured on the AHB/AXI bus reading or writing data. This is a fatal error and any data received should be discarded. The local processor should not try to restart the transfer.**
1	wdma_perr_mask	**This interrupt indicates that the requested DMA transfer was ended with an error on PCIe. This is a fatal error and any data received should be discarded. The local processor should not try to restart the transfer.**
0	wdma_end_mask	**This interrupt indicates that the requested DMA transfer is complete or has been stopped as a result of a software request.**

1A143424 INT_STATUS Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mpcie_cfg_soft_status	pcie_rc_l2_wake_status	legacy_pm_chg_status	ltr_en_status	ltr_msg_status	cpu_active_status	obff_status	obff_idle_status	msi_status	aer_event_status	pm_hp_event_status	serr_status	intd_status	intc_status	intb_status	inta_status
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		b2p_discard_status	b2p_rerr_status	p2b_wr_win2_s	p2b_wr_win1_s	p2b_wr_win0_s	p2b_rerr_status	p2b_werr_status		rdma_berr_status	rdma_perr_status	rdma_end_status		wdma_berr_status	wdma_perr_status	wdma_end_status

				tat us	tat us	tat us										
Type		W1C	W1C	W1C	W1C	W1C	W1C	W1C		W1C	W1C	W1C		W1C	W1C	W1C
Reset		0	0	0	0	0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
31	mpcie_cfg_soft_status	**MPCIe only.** The bit indicate MPCIe LTSSM has entered cfg software status and SW can start link discovery and configuration flow.
30	pcie_rc_l2_wake_status	**The bit indicate PCIe RC detect remote wake from EP in L2 state.**
29	legacy_pm_chg_status	**This bit indicates that the PCI legacy power management state has been modified on the PCI PMCSR configuration register. In order to re-establish power state D0, the local processor must generate the PME# interrupt to PCI host processor.**
28	ltr_en_status	**This bit asserts when LTR is enabled by RC.**
27	ltr_msg_status	**This bit asserts when LTR message is received.**
26	cpu_active_status	**This bit asserts when obff_cpu_active message is received.**
25	obff_status	**This bit asserts when obff_obff message is received.**
24	obff_idle_status	**This bit asserts when obff_idle message is received.**
23	msi_status	**This bit is asserted each time an MSI interrupt is received. Local processor should clear this bit and read IMSISTATUS register to identify the interrupt source.**
22	aer_event_status	**This bit is asserted each time an error is detected by AER if this feature is enabled. Local processor should clear this bit and then read AER capabilities registers located in configuration space to identify the error source.**
21	pm_hp_event_status	**This bit is asserted each time a hot-plug or power management message is received. Local processor should clear this bit and then read Slot and Root CSR registers to identify the event source.**
20	serr_status	**This bit is asserted when a system error is detected by the root port. Events and conditions that result in system errors are defined in PCI Express specification.**
19	intd_status	**This bit indicates when interrupt line INTD is asserted. Note the bit remains asserted (even if cleared by an AHB/AXI write) as long as INTD line is not de-asserted by EP.**
18	intc_status	**This bit indicates when interrupt line INTC is asserted. Note the bit remains asserted (even if cleared by an**

Bit(s)	Name	Description
		AHB/AXI write) as long as INTC line is not de-asserted by EP.
17	intb_status	This bit indicates when interrupt line INTB is asserted. Note the bit remains asserted (even if cleared by an AHB/AXI write) as long as INTB line is not de-asserted by EP.
16	inta_status	This bit indicates when interrupt line INTA is asserted. Note the bit remains asserted (even if cleared by an AHB/AXI write) as long as INTA line is not de-asserted by EP.
14	b2p_discard_status	This interrupt is issued to signal that the number of clock cycles specified by the AHB_TIMER register has been reached an that remaining data is being flushed.
13	b2p_rerr_status	This interrupt is asserted if the data requested from the bus cannot be read by the PCIe.
12	p2b_wr_win2_status	This interrupt is asserted when a write request received from the PCIe bus has been successfully posted to the AHB/AXI bus by the PCI2BUS window 2.
11	p2b_wr_win1_status	This interrupt is asserted when a write request received from the PCIe bus has been successfully posted to the AHB/AXI bus by the PCI2BUS window 1.
10	p2b_wr_win0_status	This interrupt is asserted when a write request received from the PCIe bus has been successfully posted to the AHB/AXI bus by the PCI2BUS window 0.
9	p2b_rerr_status	This interrupt is asserted when a read request is received from the PCIe but the corresponding data cannot be read from the AHB/AXI bus because an AHB/AXI error has occured.
8	p2b_werr_status	This interrupt is asserted when a request received from the PCIe cannot be posted to the AHB/AXI bus because an AHB/AXI error has occured.
6	rdma_berr_status	This interrupt indicates that an error occured on the AHB/AXI bus reading or writing data. This is a fatal error and any data received should be discarded. The local processor should not try to restart the transfer.
5	rdma_perr_status	This interrupt indicates that the requested DMA transfer was ended with an error on PCIe. This is a fatal error and any data received should be discarded. The local processor should not try to restart the transfer.
4	rdma_end_status	This interrupt indicates that the requested DMA transfer is complete or has been stopped as a result of a software request.
2	wdma_berr_status	This interrupt indicates that an error occured on the AHB/AXI bus reading or writing data. This is a fatal error

Bit(s)	Name	Description
		and any data received should be discarded. The local processor should not try to restart the transfer.
1	wdma_perr_status	**This interrupt indicates that the requested DMA transfer was ended with an error on PCIe. This is a fatal error and any data received should be discarded. The local processor should not try to restart the transfer.**
0	wdma_end_status	**This interrupt indicates that the requested DMA transfer is complete or has been stopped as a result of a software request.**

1A143428 INT_RMT_MASK Interrupt Remote Mask 3FFF7F77

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			legacy_pm_chg_rmt_mask	ltr_en_event_mask	ltr_msg_event_mask	cpu_active_event_mask	obff_event_mask	obff_idle_event_mask	serr_rmt_mask	pm_hp_event_rmt_mask	aer_event_rmt_mask	msi_rmt_mask	intd_rmt_mask	intc_rmt_mask	intb_rmt_mask	inta_rmt_mask
Type			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		b2p_discard_rmt_mask	b2p_rerr_rmt_mask	p2b_wr_win2_rmt_mask	p2b_wr_win1_rmt_mask	p2b_wr_win0_rmt_mask	p2b_rerr_rmt_mask	p2b_werr_rmt_mask		rdma_berr_rmt_mask	rdma_perr_rmt_mask	rdma_end_rmt_mask		wdma_berr_rmt_mask	wdma_perr_rmt_mask	wdma_end_rmt_mask
Type		W1C	RW	RW	RW	RW	RW	RW		RW	RW	RW		RW	RW	RW
Reset		1	1	1	1	1	1	1		1	1	1		1	1	1

Bit(s)	Name	Description
29	legacy_pm_chg_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if legacy_pm_chg_status asserts.**
28	ltr_en_event_mask	**The PCIe core will issue MSI or INT message to remote device if LTR is enabled by RC.**

Bit(s)	Name	Description
27	ltr_msg_event_mask	**The PCIe core will issue MSI or INT message to remote device if LTR message is received.**
26	cpu_active_event_mask	**The PCIe core will issue MSI or INT message to remote device if obff_cpu_active message is received.**
25	obff_event_mask	**The PCIe core will issue MSI or INT message to remote device if obff_obff message is received.**
24	obff_idle_event_mask	**The PCIe core will issue MSI or INT message to remote device if obff_idle message is received.**
23	serr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if serr_status asserts.**
22	pm_hp_event_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if pm_hp_event_status asserts.**
21	aer_event_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if aer_event_status asserts.**
20	msi_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if msi_status asserts.**
19	intd_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if intd_status asserts.**
18	intc_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if intc_status asserts.**
17	intb_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if intb_status asserts.**
16	inta_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if inta_status asserts.**
14	b2p_discard_rmt_mask	**This interrupt is issued to signal that the number of clock cycles specified by the AHB_TIMER register has been reached an that remaining data is being flushed.**
13	b2p_rerr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if b2p_rerr_status asserts.**
12	p2b_wr_win2_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if p2b_wr_win2_status asserts.**
11	p2b_wr_win1_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if p2b_wr_win1_status asserts.**
10	p2b_wr_win0_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if p2b_wr_win0_status asserts.**
9	p2b_rerr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if p2b_rerr_status asserts.**
8	p2b_werr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if p2b_werr_status asserts.**

Bit(s)	Name	Description
6	rdma_berr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if rdma_berr_status asserts.**
5	rdma_perr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if rdma_perr_status asserts.**
4	rdma_end_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if rdma_end_status asserts.**
2	wdma_berr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if wdma_berr_status asserts.**
1	wdma_perr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if wdma_perr_status asserts.**
0	wdma_end_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if wdma_end_status asserts.**

1A14342C IMSI_STATUS MSI Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**imsi_status**															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**imsi_status**															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	imsi_status	**The content of this register is asserted when an MSI with message number 0~31 is received by the root port. The local processor must monitor and clear these bits by writing 1. Note that MSI with message number greater than 31 are ignored and discarded.**

1A143430 IMSI_ADDR Root port MSI capture address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**imsi_addr**															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	imsi_addr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	imsi_addr	**This register contains MSI capture address. Root port captures all memory writes at this address and treats them as MSI. If specified address is in a PCI-BUS window range then the MSI is not captured and is forwarded to AHB/AXI bus. Note that this address must be 64-bit aligned.**

1A143434 ICMD Interrupt Command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												icmd_to_link	icmd_deassert_clkreq	icmd_send_pme	icmd_int_state	icmd_send_int
Type												WO	WO	WO	RO	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	icmd_to_link	**Local processor write 1 to start L2 state entry negotiation. If EP is also ready to enter this state then both devices will enter L2 and link will be turned off. This bit is immediately cleared by bridge and local processor does not need to clear it.**

Bit(s)	Name	Description
3	icmd_deassert_clkreq	**This bit is used to deassert CLKREQ# pin in order to indicate that PCIe 100MHz reference clock can be safely removed. This pin can only be asserted if:** - CLKREQ# support is enabled - clock power management is enabled in PCIe link control register
2	icmd_send_pme	**Local processor write 1 to generate a PME event on the PCIe link. This is used ask PCI host processor to restore bridge to a fully functional legacy power state. This bit is immediately cleared by bridge and local processor does not need to clear it.**
1	icmd_int_state	**This RO bit reflect the state of PCI interrupt.** - 0: the bridge is not asserting PCI interrupt - 1: the bridge is asserting PCI interrupt
0	icmd_send_int	**The local processor can send interrupts to the PCI host processor through the PCI** Express link. The interrupt is sent using Message Signaled Interrupt if the PCI host processor enabled MSI, or using ASSERT_INTx and DEASSERT_INTx messages otherwise. The local processor must write 1 to send PCI interrupt bit in order to send interrupt. Then it must wait until software driver clears the interrupt (this must be signaled via a user-defined mechanism, usually a register implemented in application logic). And then local processor must write 0 to send PCI interrupt bit in order to release interrupt. The PCI_INT_ASSERT signal can be used instead of this register in order to assert and de-assert a PCI interrupt.

1A143438 AHB2PCIE_BASE0_L AHB slave to PCIe tranlsation table0 LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ahb2pcie_base0_l															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ahb2pcie_baseo_l									ahb2pcie_baseo_noprefetch	ahb2pcie_baseo_reserved	ahb2pcie_baseo_size				
Type	RW									RW	RO	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:7	ahb2pcie_baseo_l	**Translated windowo PCIe base address[31:7].**
6	ahb2pcie_baseo_nopreferch	**No-prefetch disables data prefetch when set.** When it is not set then window is allowed to read data in advance for undefined length AHB read requests.
5	ahb2pcie_baseo_reserved	**reserved**
4:0	ahb2pcie_baseo_size	**This field specifies the windowo size.** Possible values are 7 to 31 which mean 2^7 to 2^31 bytes. Leaving this field to 0 causes windowo to be disabled.

1A14343C AHB2PCIE_BASEo_H AHB slave to PCIe translation tableo MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ahb2pcie_baseo_h															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ahb2pcie_baseo_h															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ahb2pcie_baseo_h	**Translated windowo PCIe base address[63:32].**

Bit(s)	Name	Description
		If 32-bit addreessing is used or no-prefetch bit is set then ahb2pcie_base0_h must be 32'h0.

1A143440 AHB2PCIE_BASE1_L AHB slave to PCIe translation table1 LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ahb2pcie_base1_l															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ahb2pcie_base1_l									ahb2pcie_base1_nopreferch	ahb2pcie_base1_reserved	ahb2pcie_base1_size				
Type	RW									RW	RO	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:7	ahb2pcie_base1_l	**Translated window1 PCIe base address[31:7].**
6	ahb2pcie_base1_nopreferch	**No-prefetch disables data prefetch when set.** When it is not set then window is allowed to read data in advance for undefined length AHB read requests.
5	ahb2pcie_base1_reserved	**reserved**
4:0	ahb2pcie_base1_size	**This field specifies the window1 size.** Possible values are 7 to 31 which mean 2^7 to 2^31 bytes. Leaving this field to 0 causes window1 to be disabled.

1A143444 AHB2PCIE_BASE1_H AHB slave to PCIe translation table1 MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ahb2pcie_base1_h															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ahb2pcie_base1_h**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ahb2pcie_base1_h	**Translated window1 PCIe base address[63:32].** If 32-bit addreessing is used or no-prefetch bit is set then ahb2pcie_base1_h must be 32'h0.

1A143448 PCIE2AXI_WIN0 PCIe to AXI window0 control register E00000D4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**pcie2axi_win0_dest**															
Type	RW															
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**pcie2axi_win0_dest**								**pcie2axi_win0_enable**	**pcie2axi_win0_noprefetch**	**pcie2axi_win0_size**					
Type	RW								RW	RW	RW					
Reset	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0

Bit(s)	Name	Description
31:8	pcie2axi_win0_dest	**Translated AXI base address [35:12]**
7	pcie2axi_win0_enable	**Enable bit is used to control whether bridge reponds to PCI requests targeting PCI-AXI window.** When not set than all PCI requests in window are treated as "unsupported request".

Bit(s)	Name	Description
6	pcie2axi_wino_noprefetch	**No-prefetch bit causes window to be mapped in PCI non-prefetchable memory space when set.** When it is not set then window is mapped in PCI prefetchable memory space.
5:0	pcie2axi_wino_size	**This field specifies the size of windowo.** Possible values are 12 to 36 which mean 2^12 to 2^36 bytes. Leaving this field to 0 causes windowo to be disabled.

1A14344C PCIE2AXI_WIN1 PCIe to AXI window1 control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pcie2axi_win1_dest															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie2axi_win1_dest								pcie2axi_win1_enable	pcie2axi_win1_noprefetch	pcie2axi_win1_size					
Type	RW								RW	RW	RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	pcie2axi_win1_dest	**Translated AXI base address [35:12]**
7	pcie2axi_win1_enable	**Enable bit is used to control whether bridge reponds to PCI requests targeting PCI-AXI window.** When not set than all PCI requests in window are treated as "unsupported request".
6	pcie2axi_win1_noprefetch	**No-prefetch bit causes window to be mapped in PCI non-prefetchable memory space when set.** When it is not set then window is mapped in PCI prefetchable memory space.
5:0	pcie2axi_win1_size	**This field specifies the size of window1.**

Bit(s)	Name	Description
		Possible values are 12 to 36 which mean 2^12 to 2^36 bytes. Leaving this field to 0 causes window1 to be disabled.

1A143450 PCIE2AXI_WIN2 PCIe to AXI window2 control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pcie2axi_win2_dest															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie2axi_win2_dest								pcie2axi_win2_enable	pcie2axi_win2_noprefetch		pcie2axi_win2				
Type	RW								RW	RW		RW				
Reset	0	0	0	0					0	0		0	0	0	0	0

Bit(s)	Name	Description
31:12	pcie2axi_win2_dest	**Translated AXI base address [31:12]**
7	pcie2axi_win2_enable	**Enable bit is used to control whether bridge reponds to PCI requests targeting PCI-AXI window.** When not set than all PCI requests in window are treated as "unsupported request".
6	pcie2axi_win2_noprefetch	**No-prefetch bit causes window to be mapped in PCI non-prefetchable memory space when set.** When it is not set then window is mapped in PCI prefetchable memory space.
4:0	pcie2axi_win2	**This field specifies the size of window2.** Possible values are 12 to 31 which mean 2^12 to 2^31 bytes. Leaving this field to 0 causes window2 to be disabled.

1A143454 PCIE2AXI_WIN3 PCIe to AXI window3 control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pcie2axi_win3_dest															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie2axi_win3_dest								pcie2axi_win3_enable	pcie2axi_win3_noprefetch		pcie2axi_win3				
Type	RW								RW	RW		RW				
Reset	0	0	0	0					0	0		0	0	0	0	0

Bit(s)	Name	Description
31:12	pcie2axi_win3_dest	**Translated AXI base address [31:12]**
7	pcie2axi_win3_enable	**Enable bit is used to control whether bridge reponds to PCI requests targeting PCI-AXI window.** When not set than all PCI requests in window are treated as "unsupported request".
6	pcie2axi_win3_noprefetch	**No-prefetch bit causes window to be mapped in PCI non-prefetchable memory space when set.** When it is not set then window is mapped in PCI prefetchable memory space.
4:0	pcie2axi_win3	**This field specifies the size of window3.** Possible values are 12 to 31 which mean 2^12 to 2^31 bytes. Leaving this field to 0 causes window3 to be disabled.

1A143458 PCIE2AXI_WIN4 PCIe to AXI window4 control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pcie2axi_win4_dest															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie2axi_win4_dest								pcie2axi_win4_enable	pcie2axi_win4_noprefetch		pcie2axi_win4				
Type	RW								RW	RW		RW				
Reset	0	0	0	0					0	0		0	0	0	0	0

Bit(s)	Name	Description
31:12	pcie2axi_win4_dest	**Translated AXI base address [31:12]**
7	pcie2axi_win4_enable	**Enable bit is used to control whether bridge reponds to PCI requests targeting PCI-AXI window.** When not set than all PCI requests in window are treated as "unsupported request".
6	pcie2axi_win4_noprefetch	**No-prefetch bit causes window to be mapped in PCI non-prefetchable memory space when set.** When it is not set then window is mapped in PCI prefetchable memory space.
4:0	pcie2axi_win4	**This field specifies the size of window4.** Possible values are 12 to 31 which mean 2^12 to 2^31 bytes. Leaving this field to 0 causes window0 to be disabled.

1A14345C PCIE2AXI_WIN5 PCIe to AXI window4 control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pcie2axi_win5_dest															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie2axi_win5_dest								pcie2axi_win	pcie2axi_win		pcie2axi_win5				

									5_enable	5_noprefetch						
Type	RW								RW	RW		RW				
Reset	0	0	0	0					0	0		0	0	0	0	0

Bit(s)	Name	Description
31:12	pcie2axi_win5_dest	**Translated AXI base address [31:12]**
7	pcie2axi_win5_enable	**Enable bit is used to control whether bridge reponds to PCI requests targeting PCI-AXI window.** When not set than all PCI requests in window are treated as "unsupported request".
6	pcie2axi_win5_noprefetch	**No-prefetch bit causes window to be mapped in PCI non-prefetchable memory space when set.** When it is not set then window is mapped in PCI prefetchable memory space.
4:0	pcie2axi_win5	**This field specifies the size of window5.** Possible values are 12 to 31 which mean 2^12 to 2^31 bytes. Leaving this field to 0 causes window1 to be disabled.

1A143460 CFG_HEADER_0 CFG request TLP header DW0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**app_cfg_fmt**			**app_cfg_type**						**app_cfg_tc**						
Type	RW			RW						RW						
Reset	0	0	0	0	0	0	0	0		0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**app_cfg_id**	**app_cfg_ep**	**app_cfg_attr**				**app_cfg_length**									
Type	RW	RW	RW				RW									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:29	app_cfg_fmt	**Format field in Configuration Request TLP.**
28:24	app_cfg_type	**Type field in Configuration Request TLP.**
22:20	app_cfg_tc	**TC field in Configuration Request TLP.**
15	app_cfg_td	**TD field in Configuration Request TLP.**
14	app_cfg_ep	**EP field in Configuration Request TLP.**
13:12	app_cfg_attr	**Attr field in Configuration Request TLP.**
9:0	app_cfg_length	**Length field in Configuration Request TLP.**

1A143464 CFG_HEADER_1 CFG request TLP header DW1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	app_cfg_rid															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	app_cfg_tag								app_cfg_lbe				app_cfg_fbe			
Type	RW								RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	app_cfg_rid	**Requester ID field in Configuration Request TLP.**
15:8	app_cfg_tag	**Tag field in Configuration Request TLP.**
7:4	app_cfg_lbe	**Last DW BE field in Configuration Request TLP.**
3:0	app_cfg_fbe	**First DW BE field in Configuration Request TLP.**

1A143468 CFG_HEADER_2 CFG request TLP header DW2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	app_cfg_bus								app_cfg_dev					app_cfg_fun		
Type	RW								RW					RW		

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					app_cfg_ext_regnum				app_cfg_regnum							
Type					RW				RW							
Reset					0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:24	app_cfg_bus	**Bus Number field in Configuration Request TLP.**
23:19	app_cfg_dev	**Device Number field in Configuration Request TLP.**
18:16	app_cfg_fun	**Function Number field in Configuration Request TLP.**
11:8	app_cfg_ext_regnum	**Ext. Register Number field in Configuration Request TLP.**
7:2	app_cfg_regnum	**Register Number field in Configuration Request TLP.**

1A14346C CFG_HEADER_3 CFG request TLP header DW3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									app_cfg_desc3							
Type									RW							
Reset									0	0	0	0	0	0		

Bit(s)	Name	Description
7:2	app_cfg_desc3	**app_cfg_desc3**

1A143470 CFG_WDATA CfgWr request TLP data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	app_cfg_wdata															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**app_cfg_wdata**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	app_cfg_wdata	**For CfgWr, this field specifies application layer prepared CFG request data and triggered by APP_TLP_REQ.app_cfg_req.**

1A143474 MSG_HEADER_0 MSG request TLP header DW0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**app_msg_fmt**			**app_msg_type**						**app_msg_tc**						
Type	RW			RW						RW						
Reset	0	0	0	0	0	0	0	0		0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**app_msg_td**	**app_msg_ep**	**app_msg_attr**				**app_msg_length**									
Type	RW	RW	RW				RW									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:29	app_msg_fmt	**Format field in Message TLP.**
28:24	app_msg_type	**Type field in Message TLP.**
22:20	app_msg_tc	**TC field in Message TLP.**
15	app_msg_td	**TD field in Message TLP.**
14	app_msg_ep	**EP field in Message TLP.**
13:12	app_msg_attr	**Attr field in Message TLP.**
9:0	app_msg_length	**Length field in Message TLP.**

Bit(s)	Name	Description

1A143478 MSG_HEADER_1 MSG request TLP header DW1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	app_msg_rid															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	app_msg_tag								app_msg_code							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	app_msg_rid	**Requester ID field in Message TLP.**
15:8	app_msg_tag	**Tag field in Message TLP.**
7:0	app_msg_code	**Message Code field in Message TLP.**

1A14347C MSG_HEADER_2 MSG request TLP header DW2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	app_msg_addr_o															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	app_msg_addr_o															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	app_msg_addr_o	**Application layer prepared MSG request header DW2.**

Bit(s)	Name	Description
		Triggered by APP_TLP_REQ.app_msg_req.

1A143480 MSG_HEADER_3 MSG request TLP header DW3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	app_msg_addr_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	app_msg_addr_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	app_msg_addr_1	**Application layer prepared MSG request header DW3.** Triggered by APP_TLP_REQ.app_msg_req.

1A143484 MSG_DATA MSG request TLP data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	app_msg_data															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	app_msg_data															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	app_msg_data	**Application layer prepared MSG request data.**

Bit(s)	Name	Description
		Triggered by APP_TLP_REQ.app_msg_req.

1A143488 APP_TLP_REQ APP request TLP start command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved1								app_cpl_status			reservedo			app_msg_req	app_cfg_req
Type	RO								RO			RO			RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	reserved1	**Reserved**
7:5	app_cpl_status	**Completion Status of PIO.** - 000: Success - 001: UR - 010: CRS - 100: CA - 111: Completion Timeout Others are reserved.
4:2	reservedo	**Reserved**
1	app_msg_req	**Application initiated MSG TLP start command.** MSG_HEADER and MSG_DATA must be ready before setting app_msg_req. When Msg/MsgD TLP is triggerd by application layer, this bit will keep asserting until Msg TLP is transmitted.
0	app_cfg_req	**Application initiated CGG TLP start command.**

Bit(s)	Name	Description
		CFG_HEADER and CFG_WDATA must be ready before setting app_cfg_req. When Cfg TLP is triggerd by application layer, this bit will keep asserting until Cpl/CplD is received.

1A14348C CFG_RDATA Returned CfgRd request CplD data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cfg_rdata															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cfg_rdata															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	cfg_rdata	**This field specifies the received CplD for CfgRd when app_cfg_status deasserted**

1A143490 CFG_BAR0 BAR0 content in configuration space 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cfg_baro															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cfg_baro															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
31:0	cfg_bar0	**BAR0 content in configuration space offset 0x10h**

1A143494 CFG_BAR1 BAR1 content in configuration space 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cfg_bar1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cfg_bar1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	cfg_bar1	**BAR1 content in configuration space offset 0x14h**

1A143498 CFG_BAR2 BAR2 content in configuration space 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cfg_bar2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cfg_bar2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	cfg_bar2	**BAR2 content in configuration space offset 0x18h**

1A14349C CFG_BAR3 BAR3 content in configuration space 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cfg_bar3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cfg_bar3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	cfg_bar3	**BAR3 content in configuration space offset 0x1Ch**

1A1434A0 CFG_BAR4 BAR4 content in configuration space 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cfg_bar4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cfg_bar4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	cfg_bar4	**BAR4 content in configuration space offset 0x20h**

1A1434A4 CFG_BAR5 BAR5 content in configuration space 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cfg_bar5															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cfg_bar5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	cfg_bar5	**BAR5 content in configuration space offset 0x24h**

1A1434AC LTR_LATENCY_VALUE LTR max snoop and no-snoop latency Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				max_no_snoop_latency_scale			max_no_snoop_latency_value									
Type				RO			RO									
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				max_snoop_latency_scale			max_snoop_latency_value									
Type				RO			RO									
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:26	max_no_snoop_latency_scale	**L1 exit latency in separated clock mode**
25:16	max_no_snoop_latency_value	**Endpoint L1 acceptable latency**
12:10	max_snoop_latency_scale	**Endpoint L0s acceptable latency**
9:0	max_snoop_latency_value	**BAR5 content in configuration space offset 0x24h**

1A1434B0 MSI_MISC MSI control and status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																msi_inter

																rupt
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	msi_bdf															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	msi_interrupt	**1: MSI interrupt status from dma done** 0: original interrupt structure RC mode only
15:0	msi_bdf	**Bus#, Device#, Function# of EP send MSI to RC** RC mode only

1A1434D0 AHB_DISCARD_TIMER AHB discard timer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AHB_DISCARD_TIMER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AHB_DISCARD_TIMER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AHB_DISCARD_TIMER	**A timeout value to discard AHB read transaction and release pending HREADY.** HCLK clock cycle unit. 0 means no time-out will be applied.

Bit(s)	Name	Description

1A1434D8 ASPM_CONF Active State power management configuration ASPM_CONF register contains information for PCI Express native power management. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IDLE_TO_LoS_L1			L1_SUPPORT	L1_EXIT_COMMON_CK_LATENCY			L1_EXIT_SEPARATE_CK_LATENCY			L1_ACCEPT_LATENCY			LoS_ACCEPT_LATENCY		
Type	RW			RW	RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMMON_CK_FTS								SEPARATE_CK_FTS							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:29	IDLE_TO_LoS_L1	**Idle time to enter Los/L1**
28	L1_SUPPORT	**Enable L1 support**
27:25	L1_EXIT_COMMON_CK_LATENCY	**L1 exit latency in common clock mode**
24:22	L1_EXIT_SEPARATE_CK_LATENCY	**L1 exit latency in separated clock mode**
21:19	L1_ACCEPT_LATENCY	**Endpoint L1 acceptable latency**
18:16	LoS_ACCEPT_LATENCY	**Endpoint Los acceptable latency**
15:8	COMMON_CK_FTS	**Number of FTS in common clock mode at 2.5 Gbps (5 to 255)**
7:0	SEPARATE_CK_FTS	**Number of FTS in separated clock mode at 2.5 Gbps (5 to 255)**
		Analysis: - k_aspm[31:0] all covered by k_conf_func

1A1434DC PM_STATUS PCI legacy power management status This is used in Endpoint mode only 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**PM_STATUS**		
Type														RU		
Reset														0	0	0

Bit(s)	Name	Description
2:0	PM_STATUS	**This register specifies the PCI Legacy Power Management state (00=D0, 01=D1, 10=D2 or 11=D3hot or D3cold). Note that change of power management state is reported by an interrupt in ISTATUS register.**

1A1434E0 PM_CONF_0 PCI legacy power management configuration This is used in Endpoint mode only PM_CONF register contains information for PCI power management capabilities register and local processor must initialize it at power-up. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DATA_SCALE**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PM_CAP**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DATA_SCALE	**Data scale at index 7 to 0**

Bit(s)	Name	Description
15:0	PM_CAP	**PM Capabilities** Analysis: - k_pm[15:0] covered by k_conf_func

1A1434E4 PM_CONF_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA_INDEX_3								DATA_INDEX_2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_INDEX_1								DATA_INDEX_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DATA_INDEX_3	**Data at index 3**
23:16	DATA_INDEX_2	**Data at index 2**
15:8	DATA_INDEX_1	**Data at index 1**
7:0	DATA_INDEX_0	**Data at index 0**

1A1434E8 PM_CONF_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA_INDEX_7								DATA_INDEX_6							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_INDEX_5								DATA_INDEX_4							
Type	RW								RW							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DATA_INDEX_7	**Data at index 7**
23:16	DATA_INDEX_6	**Data at index 6**
15:8	DATA_INDEX_5	**Data at index 5**
7:0	DATA_INDEX_4	**Data at index 4**

1A1434EC PCI_SLOTCAP PCI Express slot capabilities 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PCI_SLOTCAP**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PCI_SLOTCAP**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PCI_SLOTCAP	**PCI Express slot capabilities** Analysis: - k_slot[31:0] all covered by k_conf_func

1A1434F0 PCI_DV PCI device and vendor ID. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DEVICE_ID**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	VENDOR_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DEVICE_ID	**This register specifies the value of the PCI Device ID register, located at offset 00h in the PCI Configuration Space** Analysis: - k_pciid[95:0] all covered by k_conf_func
15:0	VENDOR_ID	**This register specifies the value of the PCI Vendor ID register, located at offset 00h in the PCI Configuration Space** Analysis: - k_pciid[95:0] all covered by k_conf_func

1A1434F4 PCI_SUB PCI subsystem device and vendor ID 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SUBSYSTEM_DEVICE_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SUBSYSTEM_VENDOR_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SUBSYSTEM_DEVICE_ID	**This register specifies the value of the PCI Subsystem Device ID register, located at offset 2Ch in the PCI Configuration Space** Analysis: - k_pciid[95:0] all covered by k_conf_func

Bit(s)	Name	Description
15:0	SUBSYSTEM_VENDOR_ID	**This register specifies the value of the PCI Subsystem Vendor ID register, located at offset 2Ch in the PCI Configuration Space** Analysis: - k_pciid[95:0] all covered by k_conf_func

1A1434F8 PCI_CREV PCI class code and revision ID 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLASS_CODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLASS_CODE								REVISION_ID							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	CLASS_CODE	**This register specifies the value of the PCI Class Code register, located at offset 08h in the PCI Configuration Space** Analysis: - k_pciid[95:0] all covered by k_conf_func
7:0	REVISION_ID	**This register specifies the value of the PCI Revision ID register, located at offset 08h in the PCI Configuration Space** Analysis: - k_pciid[95:0] all covered by k_conf_func

1A1434FC PCI_SLOTCSR PCI Express slot control and status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCI_SLOTCSR															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCI_SLOTCSR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PCI_SLOTCSR	**PCI_SLOTCSR specifies the value of the PCI Express Slot Control & Status register located at offset 98h in the PCI Configuration Space.** Reflect the value of pex18.

1A143500 PCI_PRMCSR PCI primary command and status register 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCI_PRMCSR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCI_PRMCSR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PCI_PRMCSR	**PCI_PRMCSR specifies the value of the PCI Command & Status register located at offset 04h in the PCI Configuration Space.** Reflect the value of sc_reg.

1A143504 PCI_DEVCSR PCI Express device control and status register 00002810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCI_DEVCSR															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCI_DEVCSR															
Type	RU															
Reset	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	PCI_DEVCSR	**PCI_DEVCSR specifies the value of the PCI Express Device Control & Status register located at offset 88h in the PCI Configuration Space.** Reflect the value of pex08.

1A143508 PCI_LINKCSR PCI Express link control and status register 10000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCI_LINKCSR															
Type	RU															
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCI_LINKCSR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:0	PCI_LINKCSR	**PCI_LINKCSR specifies the value of the PCI Express Link Control & Status register located at offset 90h in the PCI Configuration Space.** Reflect the value of pex10.

1A14350C PCI_ROOTCSR PCI Express root status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCI_ROOTCSR															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCI_ROOTCSR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PCI_ROOTCSR	**PCI_ROOTCSR specifies the value of the PCI Express Root Control & Status register located at offset 9Ch and ACh in the PCI Configuration Space.** Reflect the value of {pex20[23:0], pex1C[7:0]}.

1A143510 PCI_RSTCR PCI Express IP reset control register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCI_CONF_RST_OUT_EN	PCI_MAC_RST_OUT_EN	PCI_PIPE_RST_OUT_EN					PCI_PERSTB	PCI_PERSTB_CONFIG_ENABLE	PCI_PERSTB_MAC_ENABLE	PCI_PERSTB_PIPE_ENABLE	PCI_PERSTB_PHY_ENABLE	PCI_CRSTB	PCI_MAC_SRSTB	PCI_PIPE_SRSTB	PCI_PHY_RSTB
Type	RW	RW	RW					RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0					0	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
15	PCI_CONF_RST_OUT_EN	**If PCIe MAC will reset configration space register when LTSSM exit disable/ L2/ Hot reset or Link state from LINK_UP to LINK_DOWN.** 0 : Disable reset.

Bit(s)	Name	Description
		1 : Enable reset.
14	PCI_MAC_RST_OUT_EN	**If PCIe MAC will reset register of mac clock domain when LTSSM exit disable/ L2/ Hot reset or Link state from LINK_UP to LINK_DOWN.** 0 : Disable reset. 1 : Enable reset.
13	PCI_PIPE_RST_OUT_EN	**If PCIe MAC will reset register of pipe clock domain when LTSSM exit disable/ L2/ Hot reset or Link state from LINK_UP to LINK_DOWN.** 0 : Disable reset. 1 : Enable reset.
8	PCI_PERSTB	**For RC only, SW control PERST#.** 0 : PERST# is low. 1 : PERST# is high.
7	PCI_PERSTB_CONF_ENABLE	**PERSTB to reset MAC configuration space domain** 0 : disable 1 : enable
6	PCI_PERSTB_MAC_ENABLE	**PERSTB to reset MAC USER clock domain** 0 : disable 1 : enable
5	PCI_PERSTB_PIPE_ENABLE	**PERSTB to reset MAC PIPE clock domain** 0 : disable 1 : enable
4	PCI_PERSTB_PHY_ENABLE	**PERSTB to reset PHY** 0 : disable 1 : enable
3	PCI_CRSTB	**SW Configuration Reset.** Active low
2	PCI_MAC_SRSTB	**PCIe MAC USER clock Software Reset.** Active low.
1	PCI_PIPE_SRSTB	**PCIe MAC PIPE Clock Software Reset.** Active low.

Bit(s)	Name	Description
0	PCI_PHY_RSTB	**PCIe PHY Software Reset.** Active low.

1A143514 PCI_MAC_HW_VERSION PCI Express MAC HW Version 20150730

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_hw_version															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_hw_version															
Type	RO															
Reset	0	0	0	0	0	1	1	1	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
31:0	reg_hw_version	**PCI Express MAC HW Version** EX : yyyy_mmdd

1A143518 REG_DBG_MOD_SEL PCI Express Debugging Module Select FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBG_MOD_SEL3								DBG_MOD_SEL2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_MOD_SEL1								DBG_MOD_SEL0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	DBG_MOD_SEL3	**- 0: pe2_mac_top.pe2_mac_dbg_out[31:24] reflects TRANS debugging probes** - 1: pe2_mac_top.pe2_mac_dbg_out[31:24] reflects DLL debugging probes - 2: pe2_mac_top.pe2_mac_dbg_out[31:24] reflects CONF debugging probes - 3: pe2_mac_top.pe2_mac_dbg_out[31:24] reflects MAC debugging probes - 4: pe2_mac_top.pe2_mac_dbg_out[31:24] reflects Bridge debugging probes - f: pe2_mac_top.pe2_mac_dbg_out[31:24] reflects SW_PRB_OUT (0x05f8) - ff : disable debug mux
23:16	DBG_MOD_SEL2	**- 0: pe2_mac_top.pe2_mac_dbg_out[23:16] reflects TRANS debugging probes** - 1: pe2_mac_top.pe2_mac_dbg_out[23:16] reflects DLL debugging probes - 2: pe2_mac_top.pe2_mac_dbg_out[23:16] reflects CONF debugging probes - 3: pe2_mac_top.pe2_mac_dbg_out[23:16] reflects MAC debugging probes - 4: pe2_mac_top.pe2_mac_dbg_out[23:16] reflects Bridge debugging probes - f: pe2_mac_top.pe2_mac_dbg_out[23:16] reflects SW_PRB_OUT (0x05f8) - ff : disable debug mux
15:8	DBG_MOD_SEL1	**- 0: pe2_mac_top.pe2_mac_dbg_out[15:8] reflects TRANS debugging probes** - 1: pe2_mac_top.pe2_mac_dbg_out[15:8] reflects DLL debugging probes - 2: pe2_mac_top.pe2_mac_dbg_out[15:8] reflects CONF debugging probes - 3: pe2_mac_top.pe2_mac_dbg_out[15:8] reflects MAC debugging probes - 4: pe2_mac_top.pe2_mac_dbg_out[15:8] reflects Bridge debugging probes - f: pe2_mac_top.pe2_mac_dbg_out[15:8] reflects SW_PRB_OUT (0x05f8) - ff : disable debug mux

Bit(s)	Name	Description
7:0	DBG_MOD_SEL0	**- 0: pe2_mac_top.pe2_mac_dbg_out[7:0] reflects TRANS debugging probes** - 1: pe2_mac_top.pe2_mac_dbg_out[7:0] reflects DLL debugging probes - 2: pe2_mac_top.pe2_mac_dbg_out[7:0] reflects CONF debugging probes - 3: pe2_mac_top.pe2_mac_dbg_out[7:0] reflects MAC debugging probes - 4: pe2_mac_top.pe2_mac_dbg_out[7:0] reflects Bridge debugging probes - f: pe2_mac_top.pe2_mac_dbg_out[7:0] reflects SW_PRB_OUT (0x05f8) - ff : disable debug mux

1A14351C REG_DBG_PORT_SEL PCI Express Debugging Port Select 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBG_PORT_SEL3								DBG_PORT_SEL2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_PORT_SEL1								DBG_PORT_SEL0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DBG_PORT_SEL3	**debugging port selection of pe2_mac_top.pe2_mac_dbg_out[31:24]**
23:16	DBG_PORT_SEL2	**debugging port selection of pe2_mac_top.pe2_mac_dbg_out[23:16]**
15:8	DBG_PORT_SEL1	**debugging port selection of pe2_mac_top.pe2_mac_dbg_out[15:8]**
7:0	DBG_PORT_SEL0	**debugging port selection of pe2_mac_top.pe2_mac_dbg_out[7:0]**

1A143520 REG_OBFF_0 OBFF Control Register 0 00000364

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**csr_obff_state**		**csr_obff_waken_edge_1us_ticks**							
Type							RW		RW							
Reset							1	1	0	1	1	0	0	1	0	0

Bit(s)	Name	Description
9:8	csr_obff_state	**OBFF state, RW type in RC mode. RO type in EP mode** 00=cpu active, 01=obff, 10=idle, 11=reseeved.
7:0	csr_obff_waken_edge_1us_ticks	**EP mode : Ticks for 1us based on OBFF clock.** RC mode : Ticks for 1us based on U_CLK clock.

1A143524 REG_OBFF_1 OBFF Control Register 1 100F0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**csr_obff_expire_timer**								**csr_obff_trigger_mode**			**csr_obff_reqid_cmp_en**	**csr_obff_state_en**			
Type	RW								RW			RW	RW			
Reset	0	0	0	1	0	0	0	0	0	0		0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**csr_clinento_remote_req_id**															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	csr_obff_expire_timer	**EP mode only, 0~255 timer scale unit, 8 ticks per scale unit if trigger mode is 10. Based on OBFF clock**
23:22	csr_obff_trigger_mode	**incoming packet trigger mode in obff mode or in idle mode.** 00 : no trigger mode, ltach PCIe immediately when pacjet incoming. 01 : FCE queue level mode. 10 : Timer expired mode. 11 : Reserved
20	csr_obff_reqid_cmp_en	**Expected reuest id comparator enable**
19:16	csr_obff_state_en	**csr_obff_state_en[0]:obff_state_idle enable** csr_obff_state_en[1]:obff_state_obff dma enable csr_obff_state_en[2]:obff_state_obff intr enable csr_obff_state_en[3]:obff_state_cpu_act enable
15:0	csr_clinento_remote_req_id	**Expected reuest id from RC**

1A143528 REG_PHYMAC_CONF PHYMAC Control Register 00110002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						**rec_rxcfg_txts2_num**										
Type						RW										
Reset						0	0	0	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**rx_eios_filter_en**	**rxlos_fts_filter_en**
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
26:16	rec_rxcfg_txts2_num	**Adjustable number of tx TS2 when ltssm is in recvoery.rxcfg**
1	rx_eios_filter_en	**Enable the filter of garbage data after receiving EIOS**
0	rxlos_fts_filter_en	**Enable the filter of FTS from PIPE. Avoid from receiving bad FTS from PHY.**

1A14352C REG_WAKE_CONTROL Wake_n or Clkreq_n Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**rg_rc_l2_clkreq_out**	**rg_rc_drive_clkreq_dis**							**rg_wake_n_enable**	**rg_clkreq_n_enable**
Type							RW	RW							RW	RW
Reset							0	0							0	0

Bit(s)	Name	Description
9	rg_rc_l2_clkreq_out	**The register is for RC and only useful for "rg_rc_drive_clkreq_dis" is 0** 0 : RC will dirve clkreq_n to 0 in L2. (100MHz is enable) 1 : RC will dirve clkreq_n to 1 in L2.. (100MHz is disable)
8	rg_rc_drive_clkreq_dis	**The register is for RC.** If EP support clock power management - CLKPM, it means EP can drive clkreq_n, then SW can set the register to 1'b1. 0 : RC will control clkreq_n

Bit(s)	Name	Description
		1 : RC won't control clkreq_n except for L1SS is enabled. (In normal mode, EP can control clkreq_n)
1	rg_wake_n_enable	**The register can be used to request DUT as EP to exit L2 state.** EP : L2 - 0: WAKE# output disable, this means WAKE# will be external pull-high - 1: WAKE# output enable, this means WAKE# output low to wakeup from L2
0	rg_clkreq_n_enable	**The reigster can be used to request DUT to exit power mode.** RC : L1 with reference clock disabled. L1SS. L2. EP : L1 with reference clock disabled. L1SS. 0: disable SW activate clkreqn 1: SW activate clkreqn to enable reference clock reqeust

1A143530 REG_WCH_WEIGHT_0 Write channel WRR weighting control register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	wch7_weight				wch6_weight				wch5_weight				wch4_wight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wch3_weight				wch2_weight				wch1_weight				wch0_weight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	wch7_weight	**Arbitration weighting of write DMA channel 7 for MWr TLPs.** Similar to wch0_weight.
27:24	wch6_weight	**Arbitration weighting of write DMA channel 6 for MWr TLPs.** Similar to wch0_weight.
23:20	wch5_weight	**Arbitration weighting of write DMA channel 5 for MWr TLPs.** Similar to wch0_weight.
19:16	wch4_wight	**Arbitration weighting of write DMA channel 4 for MWr TLPs.** Similar to wch0_weight.
15:12	wch3_weight	**Arbitration weighting of write DMA channel 3 for MWr TLPs.** Similar to wch0_weight.
11:8	wch2_weight	**Arbitration weighting of write DMA channel 2 for MWr TLPs.** Similar to wch0_weight.
7:4	wch1_weight	**Arbitration weighting of write DMA channel 1 for MWr TLPs.** Similar to wch0_weight.
3:0	wch0_weight	**Arbitration weighting of write DMA channel 0 for MWr TLPs.** - 0: weighting = 1 - 1: weighting = 2 - 2: weighting = 3 - 3: weighting = 4 - 4: weighting = 5 - 5: weighting = 6 - 6: weighting = 7 - 7: weighting = 8 - 8: weighting = 9 - 9: weighting = 10 - 10: weighting = 11

Bit(s)	Name	Description
		- 11: weighting = 12 - 12: weighting = 13 - 14: weighting = 14 - 15: weighting = 16

1A143534 REG_WCH_WEIGHT_1 Write channel WRR weighting control register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	wch15_weight				wch14_weight				wch13_weight				wch12_wight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wch11_weight				wch10_weight				wch9_weight				wch8_weight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	wch15_weight	**Arbitration weighting of write DMA channel 15 for MWr TLPs.** Similar to wch0_weight.
27:24	wch14_weight	**Arbitration weighting of write DMA channel 14 for MWr TLPs.** Similar to wch0_weight.
23:20	wch13_weight	**Arbitration weighting of write DMA channel 13 for MWr TLPs.** Similar to wch0_weight.
19:16	wch12_wight	**Arbitration weighting of write DMA channel 12 for MWr TLPs.** Similar to wch0_weight.
15:12	wch11_weight	**Arbitration weighting of write DMA channel 11 for MWr TLPs.** Similar to wch0_weight.

Bit(s)	Name	Description
11:8	wch10_weight	**Arbitration weighting of write DMA channel 10 for MWr TLPs.** Similar to wch0_weight.
7:4	wch9_weight	**Arbitration weighting of write DMA channel 9 for MWr TLPs.** Similar to wch0_weight.
3:0	wch8_weight	**Arbitration weighting of write DMA channel 8 for MWr TLPs.** Similar to wch0_weight.

1A143538 REG_RCH_WEIGHT_0 Read channel WRR weighting control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rch7_weight				rch6_weight				rch5_weight				rch4_wight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rch3_weight				rch2_weight				rch1_weight				rch0_weight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	rch7_weight	**Arbitration weighting of read DMA channel 7 for MRd TLPs.** Similar to rch0_weight.
27:24	rch6_weight	**Arbitration weighting of read DMA channel 6 for MRd TLPs.** Similar to rch0_weight.
23:20	rch5_weight	**Arbitration weighting of read DMA channel 5 for MRd TLPs.** Similar to rch0_weight.
19:16	rch4_wight	**Arbitration weighting of read DMA channel 4 for MRd TLPs.**

Bit(s)	Name	Description
		Similar to rch0_weight.
15:12	rch3_weight	**Arbitration weighting of read DMA channel 3 for MRd TLPs.** Similar to rch0_weight.
11:8	rch2_weight	**Arbitration weighting of read DMA channel 2 for MRd TLPs.** Similar to rch0_weight.
7:4	rch1_weight	**Arbitration weighting of read DMA channel 1 for MRd TLPs.** Similar to rch0_weight.
3:0	rch0_weight	**Arbitration weighting of read DMA channel 0 for MRd TLPs.** - 0: weighting = 1 - 1: weighting = 2 - 2: weighting = 3 - 3: weighting = 4 - 4: weighting = 5 - 5: weighting = 6 - 6: weighting = 7 - 7: weighting = 8 - 8: weighting = 9 - 9: weighting = 10 - 10: weighting = 11 - 11: weighting = 12 - 12: weighting = 13 - 14: weighting = 14 - 15: weighting = 16

1A14353C REG_RCH_WEIGHT_1 Read channel WRR weighting control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	rch15_weight				rch14_weight				rch13_weight				rch12_wight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rch11_weight				rch10_weight				rch9_weight				rch8_weight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	rch15_weight	**Arbitration weighting of read DMA channel 15 for MRd TLPs.** Similar to rcho_weight.
27:24	rch14_weight	**Arbitration weighting of read DMA channel 14 for MRd TLPs.** Similar to rcho_weight.
23:20	rch13_weight	**Arbitration weighting of read DMA channel 13 for MRd TLPs.** Similar to rcho_weight.
19:16	rch12_wight	**Arbitration weighting of read DMA channel 12 for MRd TLPs.** Similar to rcho_weight.
15:12	rch11_weight	**Arbitration weighting of read DMA channel 11 for MRd TLPs.** Similar to rcho_weight.
11:8	rch10_weight	**Arbitration weighting of read DMA channel 10 for MRd TLPs.** Similar to rcho_weight.
7:4	rch9_weight	**Arbitration weighting of read DMA channel 9 for MRd TLPs.** Similar to rcho_weight.
3:0	rch8_weight	**Arbitration weighting of read DMA channel 8 for MRd TLPs.** Similar to rcho_weight.

1A143540 REG_AXI_RD_MMIO_CTRL AXI RD MMIO DMA configuration register. 01800C08

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AXI_DMA_ID				AXI_DMA_BURST			AXI_DMA_CMD_Q_EN	AXI_DMA_OUTSTAND_NUM				AXI_DMA_COHERENCE	AXI_DMA_IOMMU	AXI_DMA_CACHEABLE	AXI_DMA_ULTRA_EN
Type	RW				RW			RW	RW				RW	RW	RW	RW
Reset	0	0	0	0	0	0		1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_DMA_ULTRA_NUM								AXI_DMA_PRE_ULTRA_NUM							
Type	RW								RW							
Reset	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	AXI_DMA_ID	**AXI ID** The register are only for AXI DMA.
27:26	AXI_DMA_BURST	**AXI burst length.** 00 : 128 byte 01 : 64 byte 10 : 32 byte 11 : 16 byte The register are only for AXI DMA.
24	AXI_DMA_CMD_Q_EN	**AXI will use command queue to record DMA command.** The register are only for AXI DMA.
23:20	AXI_DMA_OUTSTAND_NUM	**The max outstand request for AXI DMA** valid value : 1 ~ 4

Bit(s)	Name	Description
19	AXI_DMA_COHERENCE	The register are only for AXI DMA. **AXI coherence capability.** 0 : disalbe 1 : enable
18	AXI_DMA_IOMMU	The register are only for AXI DMA. **AXI iommu capability.** 0 : disalbe 1 : enable
17	AXI_DMA_CACHEABLE	The register are only for AXI DMA. **AXI cacheable capability.** 0 : disalbe 1 : enable
16	AXI_DMA_ULTRA_EN	The register are only for AXI DMA. **AXI RD channel ultra capability which is used to indicate async fifo in AXI DMA is almost empty.** 0 : disalbe 1 : enable
15:8	AXI_DMA_ULTRA_NUM	The register are only for AXI DMA. **The high threshold to assert ultra signal. The value can't be smaller than pre_ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert ultra.** valid : 0 ~ 31
7:0	AXI_DMA_PRE_ULTRA_NUM	The register are only for AXI DMA. **The low threshold to assert pre_ultra signal. The value can't be larger than ultra_num. When buffer data depth is**

Bit(s)	Name	Description
		more than the threshold, AXI DMA would assert pre_ultra. valid : 0 ~ 31 The register are only for AXI DMA.

1A143544 REG_AXI_WR_MMIO_CTRL AXI WR MMIO DMA configuration register. 01800C08

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AXI_DMA_ID				AXI_DMA_BURST			AXI_DMA_CMD_Q_EN	AXI_DMA_OUTSTAND_NUM				AXI_DMA_COHERENCE	AXI_DMA_IOMMU	AXI_DMA_CACHEABLE	AXI_DMA_ULTRA_EN
Type	RW				RW			RW	RW				RW	RW	RW	RW
Reset	0	0	0	0	0	0		1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_DMA_ULTRA_NUM								AXI_DMA_PRE_ULTRA_NUM							
Type	RW								RW							
Reset	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	AXI_DMA_ID	**AXI ID** The register are only for AXI DMA.
27:26	AXI_DMA_BURST	**AXI burst length.** 00 : 128 byte 01 : 64 byte 10 : 32 byte 11 : 16 byte

Bit(s)	Name	Description
		The register are only for AXI DMA.
24	AXI_DMA_CMD_Q_EN	**AXI will use command queue to record DMA command.**
		The register are only for AXI DMA.
23:20	AXI_DMA_OUTSTAND_NUM	**The max outstand request for AXI DMA** valid value : 1 ~ 4
		The register are only for AXI DMA.
19	AXI_DMA_COHERENCE	**AXI coherence capability.** 0 : disalbe 1 : enable
		The register are only for AXI DMA.
18	AXI_DMA_IOMMU	**AXI iommu capability.** 0 : disalbe 1 : enable
		The register are only for AXI DMA.
17	AXI_DMA_CACHEABLE	**AXI cacheable capability.** 0 : disalbe 1 : enable
		The register are only for AXI DMA.
16	AXI_DMA_ULTRA_EN	**AXI RD channel ultra capability which is used to indicate async fifo in AXI DMA is almost empty.** 0 : disalbe 1 : enable
		The register are only for AXI DMA.

Bit(s)	Name	Description
15:8	AXI_DMA_ULTRA_NUM	**The high threshold to assert ultra signal. The value can't be smaller than pre_ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert ultra.** valid : 0 ~ 31 The register are only for AXI DMA.
7:0	AXI_DMA_PRE_ULTRA_NUM	**The low threshold to assert pre_ultra signal. The value can't be larger than ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert pre_ultra.** valid : 0 ~ 31 The register are only for AXI DMA.

1A143548 REG_AXI_RD_DMA_CTRL AXI RD DATA DMA configuration register. 00800C08

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AXI_DMA_ID				AXI_DMA_BURST				AXI_DMA_OUTSTAND_NUM				AXI_DMA_COHERENCE	AXI_DMA_IOMMU	AXI_DMA_CACHEABLE	AXI_DMA_ULTRA_EN
Type	RW				RW				RW				RW	RW	RW	RW
Reset	0	0	0	0	0	0			1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_DMA_ULTRA_NUM								AXI_DMA_PRE_ULTRA_NUM							
Type	RW								RW							
Reset	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	AXI_DMA_ID	**AXI ID**

Bit(s)	Name	Description
		The register are only for AXI DMA.
27:26	AXI_DMA_BURST	**AXI burst length.** 00 : 128 byte 01 : 64 byte 10 : 32 byte 11 : 16 byte
		The register are only for AXI DMA.
23:20	AXI_DMA_OUTSTAND_NUM	**The max outstand request for AXI DMA** valid value : 1 ~ 4
		The register are only for AXI DMA.
19	AXI_DMA_COHERENCE	**AXI coherence capability.** 0 : disalbe 1 : enable
		The register are only for AXI DMA.
18	AXI_DMA_IOMMU	**AXI iommu capability.** 0 : disalbe 1 : enable
		The register are only for AXI DMA.
17	AXI_DMA_CACHEABLE	**AXI cacheable capability.** 0 : disalbe 1 : enable
		The register are only for AXI DMA.
16	AXI_DMA_ULTRA_EN	**AXI RD channel ultra capability which is used to indicate async fifo in AXI DMA is almost empty.** 0 : disalbe

Bit(s)	Name	Description
		1 : enable The register are only for AXI DMA.
15:8	AXI_DMA_ULTRA_NUM	**The high threshold to assert ultra signal. The value can't be smaller than pre_ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert ultra.** valid : 0 ~ 31 The register are only for AXI DMA.
7:0	AXI_DMA_PRE_ULTRA_NUM	**The low threshold to assert pre_ultra signal. The value can't be larger than ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert pre_ultra.** valid : 0 ~ 31 The register are only for AXI DMA.

1A14354C REG_AXI_WR_DMA_CTRL AXI WR DATA DMA configuration register. 00800C08

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AXI_DMA_ID				AXI_DMA_BURST				AXI_DMA_OUTSTAND_NUM				AXI_DMA_COHERENCE	AXI_DMA_IOMMU	AXI_DMA_CACHEABLE	AXI_DMA_ULTRA_EN
Type	RW				RW				RW				RW	RW	RW	RW
Reset	0	0	0	0	0	0			1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_DMA_ULTRA_NUM								AXI_DMA_PRE_ULTRA_NUM							
Type	RW								RW							
Reset	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	AXI_DMA_ID	**AXI ID** The register are only for AXI DMA.
27:26	AXI_DMA_BURST	**AXI burst length.** 00 : 128 byte 01 : 64 byte 10 : 32 byte 11 : 16 byte The register are only for AXI DMA.
23:20	AXI_DMA_OUTSTAND_NUM	**The max outstand request for AXI DMA** valid value : 1 ~ 4 The register are only for AXI DMA.
19	AXI_DMA_COHERENCE	**AXI coherence capability.** 0 : disalbe 1 : enable The register are only for AXI DMA.
18	AXI_DMA_IOMMU	**AXI iommu capability.** 0 : disalbe 1 : enable The register are only for AXI DMA.
17	AXI_DMA_CACHEABLE	**AXI cacheable capability.** 0 : disalbe 1 : enable The register are only for AXI DMA.

Bit(s)	Name	Description
16	AXI_DMA_ULTRA_EN	**AXI RD channel ultra capability which is used to indicate async fifo in AXI DMA is almost empty.** 0 : disalbe 1 : enable The register are only for AXI DMA.
15:8	AXI_DMA_ULTRA_NUM	**The high threshold to assert ultra signal. The value can't be smaller than pre_ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert ultra.** valid : 0 ~ 31 The register are only for AXI DMA.
7:0	AXI_DMA_PRE_ULTRA_NUM	**The low threshold to assert pre_ultra signal. The value can't be larger than ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert pre_ultra.** valid : 0 ~ 31 The register are only for AXI DMA.

1A143550 REG_DMA_CK_CTRL Data and MMIO DMA Clock Gate Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**reg_dma_bus_ck_gate_dis**	**reg_mmio_ck_gate_dis**
Type															RW	RW

Reset															0	0

Bit(s)	Name	Description
1	reg_dma_bus_ck_gate_dis	**0 : dma_bus_ck will be gated by PCIe IP internal CG if DATA DMA is not active.** 1 : dma_bus_ck will not be gated by PCIe IP internal CG if DATA DMA is not active.
0	reg_mmio_ck_gate_dis	**0 : mmio_ck will be gated by PCIe IP internal CG if mmio DMA is not active.** 1 : mmio_ck will not be gated by PCIe IP internal CG if mmio DMA is not active.

1A143554 REG_IP_SLEEP_CTRL PE2 IP SLEEP control 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**reg_l2_sleep_en**	**reg_l1p2_sleep_en**	**reg_l1p1_sleep_en**	**reg_l1_sleep_en**
Type													RW	RW	RW	RW
Reset													1	1	1	1

Bit(s)	Name	Description
3	reg_l2_sleep_en	**For PCIe L2.** For MPCIe L2. 0 : PCIe controller don't assert "pe2_ip_sleep" when LTSSM in L2 state. 1 : PCIe controller will assert "pe2_ip_sleep" when LTSSM in L2 state.
2	reg_l1p2_sleep_en	**For PCIe L1SS L1.2.**

Bit(s)	Name	Description
		For MPCIe L1 Deep Hibern8. 0 : PCIe controller don't assert "pe2_ip_sleep" when LTSSM in L1.2 state. 1 : PCIe controller will assert "pe2_ip_sleep" when LTSSM in L1.2 state.
1	reg_l1p1_sleep_en	**For PCIe L1SS L1.1.** 0 : PCIe controller don't assert "pe2_ip_sleep" when LTSSM in L1.1 state. 1 : PCIe controller will assert "pe2_ip_sleep" when LTSSM in L1.1 state.
0	reg_l1_sleep_en	**For PCIe L1PM.** For MPCIe L1. 0 : PCIe controller don't assert "pe2_ip_sleep" when LTSSM in L1 state. 1 : PCIe controller will assert "pe2_ip_sleep" when LTSSM in L1 state.

1A143560 REG_ASPM_L1_CTRL ASPM L1 Reject Timing Value 0000006D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**reg_rc_l1_reject_time**				**reg_ep_l1_reject_time**			
Type									RW				RW			
Reset									0	1	1	0	1	1	0	1

Bit(s)	Name	Description
7:4	reg_rc_l1_reject_time	**The register is for RC to counter the interval between last transmission of the PM_Active_State_Request_L1 DLLP**

Bit(s)	Name	Description
		and next transmission of the PM_Active_State_Request_L1 DLLP. Unit : 1us
3:0	reg_ep_l1_reject_time	**The register is for EP to counter the interval between last transmission of the PM_Active_State_Request_L1 DLLP and next transmission of the PM_Active_State_Request_L1 DLLP.** Unit : 1us

1A143564 REG_MMIO_CTRL MMIO Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**reg_mmio_rd_lock_en**	**reg_mmio_wr_lock_en**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	reg_mmio_rd_lock_en	**The register is for RC to block memory write TLP if memory read operation is active.** 0 : memory write will wait until memory read finished. 1 : memory write won't wait memory read.
0	reg_mmio_wr_lock_en	**The register is for RC to block memory read TLP if memory write operation is active.** 0 : memory read will wait until memory write finished. 1 : memory read won't wait memory write.

Bit(s)	Name	Description

1A143568 REG_LTR_LATENCY LTR Lattency Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rx_msg_ltr_no_snoop_lat															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_msg_ltr_snoop_lat															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	rx_msg_ltr_no_snoop_lat	**Extract No Snoop Latency value from received LTR message.**
15:0	rx_msg_ltr_snoop_lat	**Extract Snoop Latency value from received LTR message.**

1A143570 REG_MPCIE_EN MPCIE FUNCTION CONTROL 01000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							reg_mpcie_hsrate_ctrl									reg_w1c_mpcie_config
Type							RW									W1C
Reset							0	1								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								reg_mpcie_t2r_						reg_mpcie_stall_en	reg_mpcie_sw_ltss	reg_mpcie_func_en

								lpbk							m_en	
Type								RW						RW	RW	RW
Reset								0						0	0	0

Bit(s)	Name	Description
25:24	reg_mpcie_hsrate_ctrl	**For dynamic bandwidth change.** SW can set the register then set retrain bit of RC configuration space to change MPHY Rate. 2'b01 : Rate A. 2'b10 : Rate B. other : Reserved.
16	reg_w1c_mpcie_config	**For debug purpose.** SW can write one to clear MPCIe config bit of configuration space.
8	reg_mpcie_t2r_lpbk	**0 : normal mode** 1 : IF MPHY TX connect to itself RX, SW can set the register to 1 to link up.
2	reg_mpcie_stall_en	**0 : MPCIe don't enter stall in L0 state.** 1 : MPCIe can enter stall in L0 state. If MPCIe enter stall then LTSSM will go to L0s state
1	reg_mpcie_sw_ltssm_en	**0 : ltssm will stay in RXDET QUIET (HIBERN8)** If the register is 0 , SW can access mPCIe or MPHY attributes by mPCIe AHB access ATTR control register. 1 : ltssm will start RXDET process. If the register is 1, SW can't access mPCIe or MPHY attributes by mPCIe AHB access ATTR control register. For Toshiba testchip, SW may need to set the register to 0 for config MPHY attributes.
0	reg_mpcie_func_en	**0 : disable mpcie function.** 1. : enable mpcie function.

Bit(s)	Name	Description
		If disable, mPCIe MAC will force MPHY power down to save power.

1A143574 REG_MPCIE_CLK_CTRL_1 MPCIE CLOCK CTRL 1 01241F1A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_sel_100us_unit				reg_ls_pwmg1_10us_cycle				reg_hs_g1b_1us_cycle							
Type	RW				RW				RW							
Reset	0				0	0	0	1	0	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_hs_g1a_1us_cycle								reg_cfg_1us_cycle							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	1	0	0	0	1	1	0	1	0

Bit(s)	Name	Description
31	reg_sel_100us_unit	**Select timing unit for "Tactivate time" and "Hibern8 time" in MPCIe.** 0 : timing unit is 1us 1 : timing unit is 100us
27:24	reg_ls_pwmg1_10us_cycle	**the clock cycle number of PWM G1 clock to reach 10us.** EX : 200KHz need 2 cycle to reash 10us.
23:16	reg_hs_g1b_1us_cycle	**the clock cycle number of HS GEAR1 Rate B clock to reach 1us.** EX : 36.44 MHz need 36 cycle to reash 1us.
15:8	reg_hs_g1a_1us_cycle	**the clock cycle number of HS GEAR1 Rate A clock to reach 1us.** EX : 31.2MHz need 31 cycle to reash 1us.
7:0	reg_cfg_1us_cycle	**the clock cycle number of rmmi_cfg_ck to reach 1us.** EX : 26MHz need 26 cycle to reach 1us.

Bit(s)	Name	Description

1A143578 REG_MPCIE_CLK_CTRL_2 MPCIE CLOCK CTRL 1 00100A28

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_ls_pwmg1_100us_cycle															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_cfg_100us_cycle															
Type	RW															
Reset	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0

Bit(s)	Name	Description
31:16	reg_ls_pwmg1_100us_cycle	**the clock cycle number of PWM G1 clock to reach 100us.** EX : 200KHz need 20 cycle to reash 100us.
15:0	reg_cfg_100us_cycle	**the clock cycle number of rmmi_cfg_ck to reach 100us.** EX : 26MHz need 2600 cycle to reach 100us.

1A14357C REG_MPCIE_CLK_CTRL_3 MPCIE CLOCK CTRL 2 0E3C0C30

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_hs_g1b_100us_cycle															
Type	RW															
Reset	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_hs_g1a_100us_cycle															
Type	RW															
Reset	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
31:16	reg_hs_g1b_100us_cycle	**the clock cycle number of HS GEAR1 Rate B clock to reach 100us.** EX : 36.44 MHz need 3644 cycle to reash 100us.
15:0	reg_hs_g1a_100us_cycle	**the clock cycle number of HS GEAR1 Rate A clock to reach 100us.** EX : 31.2MHz need 3120 cycle to reash 100us.

1A143580 REG_MPCIE_EBUF MPCIE EBUF Control 00070405

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				reg_mpcie_skp_rmv_mode				reg_mpcie_ebuf_swrst					reg_mpcie_k_ful			
Type				RW				RW					RW			
Reset				0				0					0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					reg_mpcie_k_mid								reg_mpcie_k_emp			
Type					RW								RW			
Reset					0	1	0	0					0	1	0	1

Bit(s)	Name	Description
28	reg_mpcie_skp_rmv_mode	**The register can use to decide how many SKP will be removed in MPCIe elastic buffer.** 0 : remote at most 2 SKP. 1 : remove all SKP.
24	reg_mpcie_ebuf_swrst	**SW can set 1 to reset ebuf module and clear to release reset.** 1 : reset ebuf module.
19:16	reg_mpcie_k_ful	**The almost full threshold for MPCIe ebuf.** If available data is more than the threshold, ebuf will start remove SKP OS.

Bit(s)	Name	Description
11:8	reg_mpcie_k_mid	**The middle threshold for MPCIe ebuf.** If available data is more than the threshold, controller will start to read data which is in ebuf.
3:0	reg_mpcie_k_emp	**The almost empty threshold for MPCIe ebuf.** If available data is less than the threshold, ebuf will start insert SKP OS.

1A143584 REG_AHB_ATTR_CTRL MPCIE AHB Access ATTR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ahb_attr_req						ahb_attr_wrn	ahb_attr_ext_acc	ahb_attr_wrdata							
Type	RW						RW	RW	RW							
Reset	0						0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ahb_attr_upaddr						ahb_attr_lowaddr							
Type			RW						RW							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	ahb_attr_req	**SW can set the register to request access MPCIe or mPHY attribute through RMMI interface when "reg_mpcie_sw_ltssm_en" is 0 and LTSSM stay in RXDET.QUIET state.** SW should set data, address, write/ read register before set the register and wait the register is clear by HW.
25	ahb_attr_wrn	**0 : read access.** 1 : write access.
24	ahb_attr_ext_acc	**For toshiba mPHY.** Because toshiba mPHY has some user define attribute, those attribute must access by "ext_acc" signal.

Bit(s)	Name	Description
		If SW would access user defined attributes in toshiba mPHY, please set the register to 1. 0 : HW don't assert "rmmi_attr_ext_acc" signal. 1 : HW will assert "rmmi_attr_ext_acc" signal.
23:16	ahb_attr_wrdata	**The data to write into attribute.**
13:8	ahb_attr_upaddr	**High address of attribute in mPCIe or mPHY.** Please refer to MPCIe or mPHY SPEC about attribute content. 0x00 ~ 0x1f : lane0 ~ lane31 mPHY. 0x21 : MPCIe.
7:0	ahb_attr_lowaddr	**Low address of attribute in mPCIe or mPHY.** Please refer to MPCIe or mPHY SPEC about attribute content.

1A143588 REG_AHB_ATTR_RDDATA MPCIE AHB Access ATTR Read Data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**ahb_attr_rddata**							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	ahb_attr_rddata	**The register will keep read data in last read request.** The read data is valid when "ah_attr_req" is clear by HW.

1A14358C LTSSM_TIME_VALUE_1 LTSSM timing value 1 00F00014

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							reg_ltssm_24ms									
Type							RW									
Reset							0	0	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							reg_ltssm_2ms									
Type							RW									
Reset							0	0	0	0	0	1	0	1	0	0

Bit(s)	Name	Description
25:16	reg_ltssm_24ms	**LTSSM 24ms timing value. The value can effect all 24ms timer in LTSSM.** Unit : 100us
9:0	reg_ltssm_2ms	**LTSSM 2ms timing value. The value can effect all 2ms timer in LTSSM.** Unit : 100us

1A143590 LTSSM_TIME_VALUE_2 LTSSM timing value 2 000A0258

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									reg_stall_noconfig_cycle							
Type									RW							
Reset									0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							reg_rrap_rsp_time									
Type							RW									
Reset							1	0	0	1	0	1	1	0	0	0

Bit(s)	Name	Description
23:16	reg_stall_noconfig_cycle	**The clock cycle MAC must stay in STALL.**
9:0	reg_rrap_rsp_time	**MPCIe RRAP response timeout value.**

Bit(s)	Name	Description
		Unit : 100us

1A1435A0 REG_ES_7COUNT_LANE0 Error Statistic Count7 of Lane0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	es_7count_lane0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	es_7count_lane0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	es_7count_lane0	**Lane0 :** SKP remove counter. Stop at FFFF_FFFF PIPE: RxStatus[2:0]=010

1A1435A4 REG_ES_7COUNT_LANE1 Error Statistic Count7 of Lane1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	es_7count_lane1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	es_7count_lane1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	es_7count_lane1	**Lane1 :** SKP remove counter. Stop at FFFF_FFFF PIPE: RxStatus[2:0]=010

1A1435A8 REG_ES_8COUNT_LANE0 Error Statistic Count8 of Lane0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	es_8count_lane0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	es_8count_lane0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	es_8count_lane0	**Lane0 :** SKP add counter. Stop at FFFF_FFFF PIPE: RxStatus[2:0]=001

1A1435AC REG_ES_8COUNT_LANE1 Error Statistic Count8 of Lane1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	es_8count_lane1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	es_8count_lane1															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	es_8count_lane1	**Lane1 :** SKP add counter. Stop at FFFF_FFFF PIPE: RxStatus[2:0]=001

1A1435B0 REG_ES_STATUS_LANE0 Error Statistic Status register of Lane0 00008108

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**rpl_avail_tlp**	**cred_over_cpl**	**cred_over_np**	**cred_over_p**	**cred_avail_cpl**	**cred_avail_np**	**cred_avail_p**	**rpl_avail_cfg**	**laneo_skp_rmv_add**	**laneo_ebuf_underflow**	**laneo_ebuf_overflow**	**laneo_linkdown**	**laneo_elecidle**	**laneo_LTSSM**		
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO		
Reset	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
15	rpl_avail_tlp	**0: replay buffer space is not available to handle next TLP from application layer.** 1: replay buffer space is available to handle next TLP from application layer.
14	cred_over_cpl	**0: local device Cpl credit is NOT overflowed by peer node** 1: local device Cpl credit is overflowed by peer node
13	cred_over_np	**0: local device NP credit is NOT overflowed by peer node** 1: local device NP credit is overflowed by peer node
12	cred_over_p	**0: local device Posted credit is NOT overflowed by peer node**

Bit(s)	Name	Description
		1: local device Posted credit is overflowed by peer node
11	cred_avail_cpl	**0: peer node credit is NOT available to handle next CplD TLP from local device** 1: peer node credit is available to handle next CplD TLP from local device
10	cred_avail_np	**0: peer node credit is NOT available to handle next NP TLP from local device** 1: peer node credit is available to handle next NP TLP from local device
9	cred_avail_p	**0: peer node credit is NOT available to handle next Posted TLP from local device** 1: peer node credit is available to handle next Posted TLP from local device
8	rpl_avail_cfg	**0: replay buffer space is not available to handle next TLP from configuraiton space.** 1: replay buffer space is available to handle next TLP from configuration space. - AssertINTx message - DeassertINTx message - MSI message - Completion which the status is not SC - Error message - PM message - LTR message
7	lane0_skp_rmv_add	**0: Never SKIP removed or added** 1: SKIP removed or added at least once PIPE: RxStatus[2:0]=001 or 010
6	lane0_ebuf_underflow	**0: Never elastic buffer underflow** 1: Elastic buffer underflow at least once PIPE: RxStatus[2:0]=110
5	lane0_ebuf_overflow	**0: Never elastic buffer overflow** 1: Elastic buffer overflow at least once PIPE: RxStatus[2:0]=101
4	lane0_linkdown	**0:link-down never happened after enter L0**

Bit(s)	Name	Description
		1:link-down has ever happened after first link-up
3	lane0_elecidle	**0: Non-Eletrical Idle** 1: Electrical Idle
2:0	lane0_LTSSM	**000: Detect** 001: Polling 011: L0s 010: L0 110: L1 111:Config 101:Recovery 100:Loopback or disable

1A1435B8 REG_ES_0COUNT_LANE0 Error Statistic Count0 of Lane0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**es_ocount_lane0**							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	es_ocount_lane0	**Lane0 :** Count 8b/10b or disparity error. Stop at FF PIPE: RxStatus[2:0]=100 or 111

1A1435BC REG_ES_0COUNT_LANE1 Error Statistic Count0 of Lane1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**es_0count_lane1**							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	es_0count_lane1	**Lane1 :** Count 8b/10b or disparity error. Stop at FF PIPE: RxStatus[2:0]=100 or 111

1A1435C0 REG_ES_1COUNT Error Statistic Count1 of VC0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**es_1count**							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	es_1count	**Count transmitted NAK DLLP of VC0. Stop at 0xFF.** Cleared by MAC reset or REG_ES_CLEAR_ALL.

1A1435C4 REG_ES_2COUNT Error Statistic Count2 of VC0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**es_2count**							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	es_2count	**Count received NAK DLLP of VC0. Stop at 0xFF.** Cleared by MAC reset or REG_ES_CLEAR_ALL.

1A1435C8 REG_ES_3COUNT Error Statistic Count3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**es_3count**							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	es_3count	**Count enter recovery times. Stop at FF** Note : Exlude Power management and other possible regular cases.

1A1435CC REG_ES_CLEAR_ALL Error Statistic Clear 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																es_clear_all
Type																RW
Reset																0

Bit(s)	Name	Description
0	es_clear_all	**0 : don't clear all status and counter.** 1 : clear all status and counter. Write 1 and then wirte 0 to procced an entire ES reset event.

1A1435D0 REG_ES_4COUNT Error Statistic Count4 of VC0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	es_4count															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	es_4count	**Bit[2:0]: Remaining PH credit of peer node.** Bit[15:4]: Remaining PD credit of peer node. Run time update.

1A1435D4 REG_ES_5COUNT Error Statistic Count5 of VC0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	es_5count															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	es_5count															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	es_5count	**Bit[2:0]: Remaining CPLH credit of peer node.** Bit[15:4]: Remaining CPLD credit of peer node. Bit[18:16]: Remaining NPH credit of peer node. Bit[22:20]: Remaining NPD credit of peer node. Bit[24]: Peer node have infinite PH credits. Bit[25]: Peer node have infinite PD credits. Bit[26]: Peer node have infinite CPLH credits. Bit[27]: Peer node have infinite CPLD credits. Bit[28]: Peer node have infinite NPH credits. Bit[29]: Peer node have infinite NPD credits. Run time update.

1A1435D8 REG_ES_6COUNT Error Statistic Count6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									es_6count							
Type									RO							

Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	es_6count	**Bit[0]: MRd TLP with TAG = 0 is waiting for CplD** Bit[1]: MRd TLP with TAG = 1 is waiting for CplD Bit[2]: MRd TLP with TAG = 2 is waiting for CplD Bit[3]: MRd TLP with TAG = 3 is waiting for CplD Bit[4]: MRd TLP with TAG = 4 is waiting for CplD Bit[5]: MRd TLP with TAG = 5 is waiting for CplD Bit[6]: MRd TLP with TAG = 6 is waiting for CplD Bit[7]: MRd TLP with TAG = 7 is waiting for CplD

1A1435E0 REG_I2C_CONTROL_OUT_0 I2C Output Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**I2C_SCL_OEN**	**I2C_SCL_OUT**	**I2C_SDA_OEN**	**I2C_SDA_OUT**
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	I2C_SCL_OEN	**I2C clock output enable.** Not used when I2C_INCLUDED is not defined.
2	I2C_SCL_OUT	**I2C clock out.**

Bit(s)	Name	Description
		Not used when I2C_INCLUDED is not defined.
1	I2C_SDA_OEN	**I2C data output enable.** Not used when I2C_INCLUDED is not defined.
0	I2C_SDA_OUT	**I2C data out.** Not used when I2C_INCLUDED is not defined.

1A1435E4 REG_I2C_CONTROL_IN_0 I2C Input Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**I2C_SCL_IN**	**I2C_SDA_IN**
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	I2C_SCL_IN	**I2C clock in.** Not used when I2C_INCLUDED is not defined.
0	I2C_SDA_IN	**I2C data in.** Not used when I2C_INCLUDED is not defined.

1A1435F0 REG_PE2_MAC_DBG_OUT PE2 MAC Debug Out 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_pe2_mac_dbg_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_pe2_mac_dbg_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	reg_pe2_mac_dbg_out	**The register can reflect debug output.** SW can select debug signal by setting 0x0518 and 0x051c.

1A1435F4 EP_LTSSM_FLAG EP LTSSM Flag 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																pcie_ep_l2_flag
Type																W1C
Reset																0

Bit(s)	Name	Description
0	pcie_ep_l2_flag	**The bit indicate PCIe EP enter L2 state and software can toggle "rg_wake_n_enable" register to execute remote wakeup.**

1A1435F8 SW_PROBE_OUT Software Probe Out Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_sw_prb_out															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_sw_prb_out															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	reg_sw_prb_out	**For Software debug.** Need to set module select debugging to 0x0F0F0F0F

1A1435FC PCI_MAC_HW_SUB_VERSION PCI Express MAC HW Sub Version 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_hw_sub_version															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_hw_sub_version															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	reg_hw_sub_version	**For record ECO version.**

1A143800 TEST_IN_00 Error Injection for Test Purpose 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1A143804 TEST_OUT_00 Internal State for Monitoring Purpose 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1A143808 TEST_IN_01 Error Injection for Test Purpose 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																

Type																
Reset																

Bit(s)	Name	Description

1A14380C TEST_IN_02 K FIX ID source 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

2.1.3 PCIE 1 MAC

Module name: PCIE_MAC1 Base address: (+1a145000h)

Address	Name	Width	Register Function
1A145000	K_GBL_1	32	Core variables can be set using the XpressRich2 Configuration Wizard. However, ASIC customers are encouraged to implement a programming mechanism that enables them to access and modify these settings if needed. Note: These variables should only be modified when the Core is in reset mode. Do not modify these variables if reset is not active as this may cause a malfunction of the Core.Core variables can be set using the XpressRich2 Configuration Wizard. However, ASIC customers are encouraged to implement a programming mechanism that enables them to access and modify these settings if needed. Note: These variables should only be modified when the Core is in reset mode. Do not modify these variables if reset is not active as this may cause a malfunction of the Core.
1A145004	K_GBL_2	32	Global configuration registers: the 2nd DW
1A145008	K_DP	32	Device & Port setup
1A14500C	K_CNT_0	32	Counter-related Configurations 1
1A145010	K_CNT_1	32	Counter-related Configurations 2
1A145014	K_CNT_2	32	Counter-related Configurations 3
1A145018	K_CNT_3	32	Counter-related Configurations 4
1A14501C	K_CNT_4	32	Counter-related Configurations 5
1A145020	K_RTRY	32	Replay Buffer Information
1A145024	MISC_CONF	32	Misllaneous Configuration
1A145030	K_FC_VC0_0	32	Flow Control Information for Virtual Cannel 0 (similar for VC1-7) - the 1st DW
1A145034	K_FC_VC0_1	32	Flow Control Information for Virtual Cannel 0 (similar for VC1-7) - the 2nd DW
1A145038	K_PTR_VC0_0	32	Recive Buffer Pointers VC 0 (similar for VC1-7) - the 1st DW
1A14503C	K_PTR_VC0_1	32	Recive Buffer Pointers VC 0 (similar for VC1-7) - the 2nd DW
1A145040	K_PTR_VC0_2	32	Recive Buffer Pointers VC 0 (similar for VC1-7) - the 3rd DW
1A145044	K_PTR_VC0_3	32	Recive Buffer Pointers VC 0 (similar for VC1-7) - the 4th DW
1A145100	K_CONF_FUNC0_0	32	Configuration Space Header 00h
1A145104	K_CONF_FUNC0_1	32	Configuration Space Header 08h
1A145108	K_CONF_FUNC0_2	32	Configuration Space Header 2Ch
1A14510C	K_CONF_FUNC0_3	32	Individual function 0 configuration, the 4th DW
1A145110	K_CONF_FUNC0_4	32	Individual function 0 configuration, the 5th DW
1A145114	K_CONF_FUNC0_5	32	Individual function 0 configuration, the 6th DW
1A145118	K_CONF_FUNC0_6	32	Individual function 0 configuration, the 7th DW
1A14511C	K_CONF_FUNC0_7	32	Individual function 0 configuration, the 8th DW
1A145120	K_CONF_FUNC0_8	32	Individual function 0 configuration, the 9th DW
1A145124	K_CONF_FUNC0_9	32	Individual function 0 configuration, the 10th DW

Address	Name	Width	Register Function
1A145128	K_CONF_FUNC0_10	32	Individual function 0 configuration, the 11th DW
1A14512C	K_CONF_FUNC0_11	32	Individual function 0 configuration, the 12th DW
1A145130	K_CONF_FUNC0_12	32	Individual function 0 configuration, the 13th DW
1A145134	K_BAR_FUNC0_0	32	BAR0 Configuration. Note:A BAR cannot be modified if the previous BAR uses 64-bit addressing.
1A145138	K_BAR_FUNC0_1	32	BAR1 Configuration.
1A14513C	K_BAR_FUNC0_2	32	BAR2 Configuration.
1A145140	K_BAR_FUNC0_3	32	BAR3 Configuration.
1A145144	K_BAR_FUNC0_4	32	BAR4 Configuration.
1A145148	K_BAR_FUNC0_5	32	BAR5 Configuration.
1A14514C	K_BAR_FUNC0_6	32	Expansion ROM Configuration 1.
1A145150	K_BAR_FUNC0_7	32	Expansion ROM Configuration 2.
1A145154	K_CONF_LTR_OBFF	32	LTR AND OBFF Support Hwinit
1A145158	K_CPL_RESOURCE	32	Complete resource
1A14515C	L_LOCAL_TCOMMON_MODE	32	Tcommon mode time requred by Local PHY RX
1A145180	K_CONF_FUNC0_13	32	MPCIe Configuration space capability
1A145400	WDMA_PCIE_ADDR_L	32	Write DMA start PCIe address LSB
1A145404	WDMA_PCIE_ADDR_H	32	Write DMA start PCIe address MSB
1A145408	WDMA_BUS_ADDR	32	Write DMA start BUS address
1A14540C	WDMA_CONTROL	32	Write DMA control parameters
1A145410	RDMA_PCIE_ADDR_L	32	Read DMA start PCIe address LSB
1A145414	RDMA_PCIE_ADDR_H	32	Read DMA start PCIe address MSB
1A145418	RDMA_BUS_ADDR	32	Read DMA start BUS address
1A14541C	RDMA_CONTROL	32	Read DMA control parameters
1A145420	INT_MASK	32	Interrupt Mask
1A145424	INT_STATUS	32	Interrupt Status
1A145428	INT_RMT_MASK	32	Interrupt Remote Mask
1A14542C	IMSI_STATUS	32	MSI Status
1A145430	IMSI_ADDR	32	Root port MSI capture address
1A145434	ICMD	32	Interrupt Command
1A145438	AHB2PCIE_BASE0_L	32	AHB slave to PCIe tranlsation table0 LSB
1A14543C	AHB2PCIE_BASE0_H	32	AHB slave to PCIe translation table0 MSB
1A145440	AHB2PCIE_BASE1_L	32	AHB slave to PCIe translation table1 LSB
1A145444	AHB2PCIE_BASE1_H	32	AHB slave to PCIe translation table1 MSB
1A145448	PCIE2AXI_WIN0	32	PCIe to AXI window0 control register
1A14544C	PCIE2AXI_WIN1	32	PCIe to AXI window1 control register
1A145450	PCIE2AXI_WIN2	32	PCIe to AXI window2 control register
1A145454	PCIE2AXI_WIN3	32	PCIe to AXI window3 control register
1A145458	PCIE2AXI_WIN4	32	PCIe to AXI window4 control register
1A14545C	PCIE2AXI_WIN5	32	PCIe to AXI window4 control register
1A145460	CFG_HEADER_0	32	CFG request TLP header DW0
1A145464	CFG_HEADER_1	32	CFG request TLP header DW1
1A145468	CFG_HEADER_2	32	CFG request TLP header DW2
1A14546C	CFG_HEADER_3	32	CFG request TLP header DW3

Address	Name	Width	Register Function
1A145470	CFG_WDATA	32	CfgWr request TLP data
1A145474	MSG_HEADER_0	32	MSG request TLP header DW0
1A145478	MSG_HEADER_1	32	MSG request TLP header DW1
1A14547C	MSG_HEADER_2	32	MSG request TLP header DW2
1A145480	MSG_HEADER_3	32	MSG request TLP header DW3
1A145484	MSG_DATA	32	MSG request TLP data
1A145488	APP_TLP_REQ	32	APP request TLP start command
1A14548C	CFG_RDATA	32	Returned CfgRd request CplD data
1A145490	CFG_BAR0	32	BAR0 content in configuration space
1A145494	CFG_BAR1	32	BAR1 content in configuration space
1A145498	CFG_BAR2	32	BAR2 content in configuration space
1A14549C	CFG_BAR3	32	BAR3 content in configuration space
1A1454A0	CFG_BAR4	32	BAR4 content in configuration space
1A1454A4	CFG_BAR5	32	BAR5 content in configuration space
1A1454AC	LTR_LATENCY_VALUE	32	LTR max snoop and no-snoop latency Register
1A1454B0	MSI_MISC	32	MSI control and status Register
1A1454D0	AHB_DISCARD_TIMER	32	AHB discard timer
1A1454D8	ASPM_CONF	32	Active State power management configuration ASPM_CONF register contains information for PCI Express native power management.
1A1454DC	PM_STATUS	32	PCI legacy power management status This is used in Endpoint mode only
1A1454E0	PM_CONF_0	32	PCI legacy power management configuration This is used in Endpoint mode only PM_CONF register contains information for PCI power management capabilities register and local processor must initialize it at power-up.
1A1454E4	PM_CONF_1	32	
1A1454E8	PM_CONF_2	32	
1A1454EC	PCI_SLOTCAP	32	PCI Express slot capabilities
1A1454F0	PCI_DV	32	PCI device and vendor ID.
1A1454F4	PCI_SUB	32	PCI subsystem device and vendor ID
1A1454F8	PCI_CREV	32	PCI class code and revision ID
1A1454FC	PCI_SLOTCSR	32	PCI Express slot control and status register
1A145500	PCI_PRMCSR	32	PCI primary command and status register
1A145504	PCI_DEVCSR	32	PCI Express device control and status register
1A145508	PCI_LINKCSR	32	PCI Express link control and status register
1A14550C	PCI_ROOTCSR	32	PCI Express root status register
1A145510	PCI_RSTCR	32	PCI Express IP reset control register
1A145514	PCI_MAC_HW_VERSION	32	PCI Express MAC HW Version
1A145518	REG_DBG_MOD_SEL	32	PCI Express Debugging Module Select
1A14551C	REG_DBG_PORT_SEL	32	PCI Express Debugging Port Select
1A145520	REG_OBFF_0	32	OBFF Control Register 0
1A145524	REG_OBFF_1	32	OBFF Control Register 1
1A145528	REG_PHYMAC_CONF	32	PHYMAC Control Register
1A14552C	REG_WAKE_CONTROL	32	Wake_n or Clkreq_n Control Register
1A145530	REG_WCH_WEIGHT_0	32	Write channel WRR weighting control register 0

Address	Name	Width	Register Function
1A145534	REG_WCH_WEIGHT_1	32	Write channel WRR weighting control register 1
1A145538	REG_RCH_WEIGHT_0	32	Read channel WRR weighting control register 0
1A14553C	REG_RCH_WEIGHT_1	32	Read channel WRR weighting control register 1
1A145540	REG_AXI_RD_MMIO_CTRL	32	AXI RD MMIO DMA configuration register.
1A145544	REG_AXI_WR_MMIO_CTRL	32	AXI WR MMIO DMA configuration register.
1A145548	REG_AXI_RD_DMA_CTRL	32	AXI RD DATA DMA configuration register.
1A14554C	REG_AXI_WR_DMA_CTRL	32	AXI WR DATA DMA configuration register.
1A145550	REG_DMA_CK_CTRL	32	Data and MMIO DMA Clock Gate Control
1A145554	REG_IP_SLEEP_CTRL	32	PE2 IP SLEEP control
1A145560	REG_ASPM_L1_CTRL	32	ASPM L1 Reject Timing Value
1A145564	REG_MMIO_CTRL	32	MMIO Control
1A145568	REG_LTR_LATENCY	32	LTR Lattency Value
1A145570	REG_MPCIE_EN	32	MPCIE FUNCTION CONTROL
1A145574	REG_MPCIE_CLK_CTRL_1	32	MPCIE CLOCK CTRL 1
1A145578	REG_MPCIE_CLK_CTRL_2	32	MPCIE CLOCK CTRL 1
1A14557C	REG_MPCIE_CLK_CTRL_3	32	MPCIE CLOCK CTRL 2
1A145580	REG_MPCIE_EBUF	32	MPCIE EBUF Control
1A145584	REG_AHB_ATTR_CTRL	32	MPCIE AHB Access ATTR Control
1A145588	REG_AHB_ATTR_RDDATA	32	MPCIE AHB Access ATTR Read Data
1A14558C	LTSSM_TIME_VALUE_1	32	LTSSM timing value 1
1A145590	LTSSM_TIME_VALUE_2	32	LTSSM timing value 2
1A1455A0	REG_ES_7COUNT_LANE0	32	Error Statistic Count7 of Lane0
1A1455A4	REG_ES_7COUNT_LANE1	32	Error Statistic Count7 of Lane1
1A1455A8	REG_ES_8COUNT_LANE0	32	Error Statistic Count8 of Lane0
1A1455AC	REG_ES_8COUNT_LANE1	32	Error Statistic Count8 of Lane1
1A1455B0	REG_ES_STATUS_LANE0	32	Error Statistic Status register of Lane0
1A1455B8	REG_ES_0COUNT_LANE0	32	Error Statistic Count0 of Lane0
1A1455BC	REG_ES_0COUNT_LANE1	32	Error Statistic Count0 of Lane1
1A1455C0	REG_ES_1COUNT	32	Error Statistic Count1 of VC0
1A1455C4	REG_ES_2COUNT	32	Error Statistic Count2 of VC0
1A1455C8	REG_ES_3COUNT	32	Error Statistic Count3
1A1455CC	REG_ES_CLEAR_ALL	32	Error Statistic Clear
1A1455D0	REG_ES_4COUNT	32	Error Statistic Count4 of VC0
1A1455D4	REG_ES_5COUNT	32	Error Statistic Count5 of VC0
1A1455D8	REG_ES_6COUNT	32	Error Statistic Count6

Address	Name	Width	Register Function
1A1455E0	REG_I2C_CONTROL_OUT_0	32	I2C Output Control Register
1A1455E4	REG_I2C_CONTROL_IN_0	32	I2C Input Control Register
1A1455F0	REG_PE2_MAC_DBG_OUT	32	PE2 MAC Debug Out
1A1455F4	EP_LTSSM_FLAG	32	EP LTSSM Flag
1A1455F8	SW_PROBE_OUT	32	Software Probe Out Register
1A1455FC	PCI_MAC_HW_SUB_VERSION	32	PCI Express MAC HW Sub Version
1A145800	TEST_IN_00	32	Error Injection for Test Purpose
1A145804	TEST_OUT_00	32	Internal State for Monitoring Purpose
1A145808	TEST_IN_01	32	Error Injection for Test Purpose
1A14580C	TEST_IN_02	32	K FIX ID source

1A145000 K_GBL_1 Core variables can be set using the XpressRich2 Configuration Wizard. However, ASIC customers are encouraged to implement a programming mechanism that enables them to access and modify these settings if needed. Note: These variables should only be modified when the Core is in reset mode. Do not modify these variables if reset is not active as this may cause a malfunction of the Core.Core variables can be set using the XpressRich2 Configuration Wizard. However, ASIC customers are encouraged to implement a programming mechanism that enables them to access and modify these settings if needed. Note: These variables should only be modified when the Core is in reset mode. Do not modify these variables if reset is not active as this may cause a malfunction of the Core. 00804201

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_gbl_rcvr_det				k_gbl_derr_rcv_imp	k_gbl_tlp_rx_reorder	k_gbl_com_dpram	k_gbl_cdc_meso ch	k_gbl_cdc_imp	k_gbl_func_imp						
Type	RW				RW	RW	RW	RW	RW	RW						
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_gbl_port_type				k_gbl_bf	k_gbl_ct_	k_gbl_slot	k_gbl_pip	k_gbl_vc_imp							k_gbl_pci

					m_mode	imp	_imp	e_if								e_2o
Type	RW				RW	RW	RW	RW	RW							RW
Reset	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:28	k_gbl_rcvr_det	**k_gbl[31:28]: Only one receiver detection is performed if the result of the receiver detection corresponds to the programmed value. Otherwise, receive detection is performed twice.** - 0100: Receiver detected on lanes 0-3 only - 0010: Receiver detected on lanes 0 or 1 only - 0001: Receiver detected on lane 0 only - 1100: Receiver detected on lanes 4-7 only - 1010: Receiver detected on lanes 6 and 7 only - 1001: Receiver detected on lane 7 only - 0110: Receiver detected on lanes 2 and 3 only - 0101: Receiver detected on lane 3 only - 0011: Receiver detected on lane 1 only Otherwise: Receiver detected all lanes. For example, when this signal is set to 1100 and a receiver is detected on lanes 4-7 only, the LTSSM moves directly to polling state without performing a second receiver detection.
27	k_gbl_derr_rcv_imp	**k_gbl[27]: 1 = Receive buffer error checking using the DERR_RCV signal implemented.**
26	k_gbl_tlp_rx_reorder	**k_gbl[26]: 1 = TLP reordering on the Receive path implemented.**
25	k_gbl_com_dpram	**k_gbl[25]: DPRAM mode** - 0: Dedicated DPRAM per VC defined for Receive buffer - 1: Common DPRAM for all VCs defined for Receive buffer.
24	k_gbl_cdc_mesoch	**k_gbl[24]: Active only when CDC mode is active** - 0: CDC compensates for plesiochronous clock relationship - 1: CDC compensates for mesochronous clock relationship
23	k_gbl_cdc_imp	**k_gbl[23]: CDC implementation**

Bit(s)	Name	Description
		- 0: CDC bypassed - 1: CDC active
22:16	k_gbl_func_imp	**k_gbl[22:16]: Indicates if a particular function is implemented in the Core.** For example, if bit 4 if set to 1, function 4 is implemented.
15:12	k_gbl_port_type	**k_gbl[15:12]: Port type:** - 0100: Rootport - 0000: Endpoint (PCI Express) - 0001: Endpoint (Legacy) - 0101: Switch port (upstream) - 0110: Switch port (downstream) - 0111: Bridge (PCI Express to PCI / PCI-X) - 1110: Type of Core controlled by the mode[1:0] signal for Switch upstream/downstream shared silicon - 1111: Type of Core controlled by the mode[1:0] signal for Rootport, Endpoint shared silicon
11	k_gbl_bfm_mode	**k_gbl[11]: BFM mode: This variable should be set to 0.** The value 1 is used for BFM mode only.
10	k_gbl_ct_imp	**k_gbl[10]: 1 = cut-through mode implemented (switch only)**
9	k_gbl_slot_imp	**k_gbl[9]: Slot register implemented**
8	k_gbl_pipe_if	**k_gbl[8]: PIPE interface width** - 0: 16-bit PIPE data interface - 1: 8-bit PIPE data interface
7:1	k_gbl_vc_imp	**k_gbl[7:1]: Indicates if a particular VC is implemented in the Core.** For example, if bit 4 if set to 1, VC4 is implemented.
0	k_gbl_pcie_20	**k_gbl[0]: PCI Express specification compliance.** This variable should be set to 1. Value 0 is used for backwards-compatibility with PCIe Specification 1.0a.

Bit(s)	Name	Description

1A145004 K_GBL_2 Global configuration registers: the 2nd DW 40004004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_gbl_comp_tlp_bypass	k_gbl_pipe_turn_off_en	k_gbl_ct_mode_en	k_gbl_big_end	k_gbl_pcie_mode_sel	k_gbl_rsv										
Type	RW	RW	RW	RW	RW	RW										
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_gbl_rsv	k_err_lane_en	k_gbl_ignore_train_ctrl	k_gbl_elect_idle_en	k_gbl_x2_down_cfg	k_gbl_lane_ignore								k_gbl_speed_sup	k_gbl_trans_layer_bypass	k_gbl_ecrc_imp
Type	RW	RW	RW	RW	RW	RW								RW	RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
31	k_gbl_comp_tlp_bypass	**k_gbl[63]: Receive buffer bypass for completion TLPs** This variable should be set to 0. Set to 1 means completion TLPs can bypass the Receive buffer.
30	k_gbl_pipe_turn_off_en	**k_gbl[62]: 1 = "turn off" mechanism described in the PIPE Interface specifications is enabled.**
29	k_gbl_ct_mode_en	**k_gbl[61]: 1 = enable CT mode (for switch designs only).**
28	k_gbl_big_end	**k_gbl[60]** - 0: Little-endian data flow - 1: Big-endian data flow
27	k_gbl_pcie_mode_sel	**k_gbl[59]** Only for pcie configuration include pcie and mpcie.

Bit(s)	Name	Description
		0 : pcie 1 : mpcie
26:15	k_gbl_rsv	**k_gbl[58:47]: reserved**
14	k_err_lane_en	**k_gbl[46]** 0 : disable detect lane data error. 1 : enable detect lane data error.
13	k_gbl_ignore_train_ctrl	**k_gbl[45]: 1 = all training control bits (except hot reset) in training order sets are ignored.**
12	k_gbl_elect_idle_en	**k_gbl[44]** - 0: Inferred Electrical Idle disabled. - 1: Inferred Electrical Idle enabled.
11	k_gbl_x2_down_cfg	**k_gbl[43]: 0 enables x2 Down Configuration.** This means that x2 lane configuration is possible when a link down configuration (recovery) from x4 or x8 occurs.
10:3	k_gbl_lane_ignore	**k_gbl[42:35]: 1 = the corresponding PCIe lane is ignored.** - k_gbl[35]:PCIe lane 0 ignored - k_gbl[36]:PCIe lane 1 ignored - k_gbl[37]:PCIe lane 2 ignored - k_gbl[38]:PCIe lane 3 ignored - k_gbl[39]:PCIe lane 4 ignored - k_gbl[40]:PCIe lane 5 ignored - k_gbl[41]:PCIe lane 6 ignored - k_gbl[42]:PCIe lane 7 ignored
2	k_gbl_speed_sup	**k_gbl[34]: Speed support.** - 0: implements 2.5 Gbps speed support. - 1: implements both 2.5 and 5.0 Gbps speed support.
1	k_gbl_trans_layer_bypass	**k_gbl[33]: Transaction layer bypass** This variable should be set to 0. Set to 1 means the transaction layer is bypassed.
0	k_gbl_ecrc_imp	**k_gbl[32]: 1 = ECRC forwarding to and from the Application Layer implemented.**

Bit(s)	Name	Description

1A145008 K_DP Device & Port setup 00000020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**k_port**								**k_dev**				
Type				RW								RW				
Reset				0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
12:5	k_port	**Port Link number.**
4:0	k_dev	**Indicates the device number for Switch or Rootport components.**

1A14500C K_CNT_0 Counter-related Configurations 1 0140FF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**k_cnt_pwr_trans_delay_cnt**								**k_cnt_dummy_inst_stop**				**k_cnt_rsv**
Type				RW								RW				RW
Reset				0	0	0	0	1	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_cnt_clk_elect_idle**								**k_cnt_rx_cdc_almost_full**				**k_cnt_tx_cdc_almost_full**			
Type	RW								RW				RW			
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:21	k_cnt_pwr_trans_delay_cnt	**k_cnt[64:57]: Powerdown Transition Delay Counter.**

Bit(s)	Name	Description
		Delays the transition to powerdown phase when a TXELECIDLE signal is asserted in states where the RXELECIDLE signal is not used (such as Los, detect, disable and hot reset). Note:The recommended value of this counter is 10.
20:17	k_cnt_dummy_inst_stop	**k_cnt[56:53]: Value used for stopping dummy insertion at the CDC Transmit FIFO when the Almost Full condition is reached. Used when k_gbl(24:23)="01" (user clock is used and CDC compensates for plesiochronous relation).** Note:When set to 0000, the Core defaults to 1011.
16	k_cnt_rsv	**k_cnt[52]: reserved**
15:8	k_cnt_clk_elect_idle	**k_cnt[51:44]: Number of clock cycles for inferring Electrical Idle exit when Core Rx lanes are in Los state.** This value is used when k_conf_func0[371] is asserted.
7:4	k_cnt_rx_cdc_almost_full	**k_cnt[43:40]:Rx CDC Almost Full condition** Indicates when the CDC Receive FIFO is almost full. Note:When set to 0000, the Core defaults to 1011.
3:0	k_cnt_tx_cdc_almost_full	**k_cnt[39:36]:Tx CDC Almost Full condition** Indicates when the CDC Transmit FIFO is almost full. Note:When set to 0000, the Core defaults to 1011.

1A145010 K_CNT_1 Counter-related Configurations 2 0001E847

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		k_cnt_skp_os_cnt											k_cnt_recov_speed_cnt			
Type		RW											RW			
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_cnt_recov_speed_cnt															

Type	RW															
Reset	1	1	1	0	1	0	0	0	0	1	0	0	0	1	1	1

Bit(s)	Name	Description
30:20	k_cnt_skp_os_cnt	**k_cnt[95:85]: SKP OS Scheduling Counter.** When set to 0000, the Core defaults to the PCIe Specification value (0x252).
19:0	k_cnt_recov_speed_cnt	**k_cnt[84:65]: Recovery.Speed Counter** Counts 1 ms using uclk when the LTSSM state is Recovery.Speed (applies to 5.0 Gbps configuration speed only). See the PCI Express Specifications. Default : 125MHz

1A145014 K_CNT_2 Counter-related Configurations 3 C8042341

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_cnt_fc_to_check								k_cnt_l1_entry_lat							
Type	RW								RW							
Reset	1	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_cnt_los_entry_lat					k_cnt_fc_init_timer					k_cnt_2_rsv			k_cnt_max_payload_size		
Type	RW					RW					RW			RW		
Reset	0	0	1	0	0	0	1	1	0	1	0	0	0	0	0	1

Bit(s)	Name	Description
31:24	k_cnt_fc_to_check	**k_cnt[127:120]: Flow Control Time-Out Check (1us unit).** If the Core does not receive an update flow control packet within the time range specified by this counter, it transitions to Recovery state.
23:16	k_cnt_l1_entry_lat	**k_cnt[178:171] : L1 entry latency (256ns unit)** When the Core remains idle for the time range specified by this counter, it transitions to L1 state.
15:11	k_cnt_los_entry_lat	**k_cnt[111:107]: Los entry latency (256ns unit)**

Bit(s)	Name	Description
		When the Core remains idle for the time range specified by this counter, it transitions to Los state.
10:6	k_cnt_fc_init_timer	**k_cnt[106:102]: FC init timer (256ns unit)** Time between consecutive sets of init flow control sent for VCs other than VC0.
5:3	k_cnt_2_rsv	**k_cnt[101:99] not used**
2:0	k_cnt_max_payload_size	**k_cnt[98:96]** Device Control Register.Max_payload_Size - 000: 128 bytes - 001: 256 bytes - 010: 512 bytes - 011: 1024 bytes - 100: 2048 bytes - 101: 4096 bytes - 110: reserved - 111: reserved

1A145018 K_CNT_3 Counter-related Configurations 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		k_cnt_replay_to														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		k_cnt_ack_lat_to														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:16	k_cnt_replay_to	**k_cnt[157:143]: Timeout value for the Replay timer. When set to 0, the Core defaults to the PCIe Specification value.**

Bit(s)	Name	Description
14:0	k_cnt_ack_lat_to	**k_cnt[142:128]: Timeout value for the ACK latency timer. When set to 0, the Core defaults to the PCIe Specification value.**

1A14501C K_CNT_4 Counter-related Configurations 5 14BD0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			k_cnt_cpl_timeout						k_cnt_read_request_size			k_cnt_fc_update_timer				
Type			RW						RW			RW				
Reset			0	1	0	1	0	0	1	0	1	1	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				k_aux_tick					k_cnt_pwr_down_to				k_cnt_txelecidle_lat			
Type				RW					RW				RW			
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:24	k_cnt_cpl_timeout	**Completion timeout value (1ms unit).** 6'h0 means completion timeout event will never occurs.
23:21	k_cnt_read_request_size	**Device Control Register.Max_Read_Request_Size** This field sets the maximum read request size for the function as a Requester. The function must not generate read requests with a size exceeding the set value. - 000: 128 bytes - 001: 256 bytes - 010: 512 bytes - 011: 1024 bytes - 100: 2048 bytes - 101: 4096 bytes - 110: reserved - 111: reserved

Bit(s)	Name	Description
20:16	k_cnt_fc_update_timer	**k_cnt[116:112]: Update Flow Control Credit Timer (1us unit).** The Core sends update flow control packets when this timer expires.
12:8	k_aux_tick	**k_cnt[170:166]:ticks of auxclk in one us. Used for timer in L1.2 state.** 00:1 tick (1MHz) 01:2 ticks (2MHz) 02:3 ticks (3MHz) 03:4 ticks (4MHz) 04:5 ticks (5MHz) 05:6 ticks (6MHz) 06:8 ticks (8MHz) 07:10 ticks (10MHz) 08:12 ticks (12MHz) 09:16 ticks (16MHz) 0A:20 ticks (20MHz) 0B:22 ticks (22MHz) 0C:26 ticks (26MHz) 0D:30 ticks (30MHz) 0E:32 ticks (32MHz) 0F:36 ticks (36MHz) 10:40 tick (40MHz) 11:44 ticks (44MHz) 12:48 ticks (48MHz) 13:50 ticks 14:56 ticks 15:60 ticks 16:64 ticks 17:72 ticks 18:80 ticks

Bit(s)	Name	Description
		19:84 ticks 1A:88 ticks 1B:92 ticks 1C:96 ticks 1D:100 ticks 1E:112 ticks 1F:128 ticks
7:4	k_cnt_pwr_down_to	**k_cnt[165:162]: Configurable powerdown timeout.** Sets the maximum time (in ms) allowed for PHY to acknowledge a powerdown transition. This timeout prevents an LTSSM freeze caused by a missing PHY acknowledge after a powerdown request. The default value of 0 means that no timeout is used.
3:0	k_cnt_txelecidle_lat	**k_cnt[161:158]: Sets the latency for the assertion of the pipe signal TXELECIDLE after the Electrical Idle Order Set (EIOS) is sent.**

1A145020 K_RTRY Replay Buffer Information 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_rtry_replay**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	k_rtry_replay	**Replay Buffer Last Active Address: For Replay buffers whose size is 2G_RTRY_BUF, this input is set to all 1s.**

1A145024 MISC_CONF Misllaneous Configuration 00000006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														slotclk_cfg	mode	
Type														RW	RW	
Reset														1	1	0

Bit(s)	Name	Description
2	slotclk_cfg	**Slot Clock Configuration: This variable is used to inform the Configuration Space if the PHY uses the same Reference Clock as the slot (Receive in Upstream mode, Transmit in Downstream mode).** - 0: independent clock. - 1 slot clock. This signal is synchronous to the UCLK.
1:0	mode	**Mode: This variable indicates the type of Core configuration.** Whhe Core is implemented in Endpoint/Rootport Shared Silicon mode: - 00: Native Endpoint. - 01: Legacy Endpoint. - 1x: Rootport. When the Core is implemented in Switch upstream/downstream port shared silicon mode: - 00: Native Endpoint. - 01: Legacy Endpoin. - 10: Switch downstream port. - 11: Switch upstream port. Mode selection should be performed when the Core is in a reset state.

1A145030 K_FC_VC0_0 Flow Control Information for Virtual Cannel 0 (similar for VC1-7) - the 1st DW 01008020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_fc_vc0_0															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_fc_vc0_0															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:0	k_fc_vc0_0	**Credit VC 0: This variable provides flow control information for VC0.** - k_vc0[7:0]: Receive flow control credit for Posted Headers. - k_vc0[19:8]: Receive flow control credit for Posted Data. - k_vc0[27:20]: Receive flow control credit for Non-Posted Headers. The corresponding registers for VC1-VC7 of K_FC_VC0_0 (0030h) to k_PTR_VC0_3 (0044h) range from 0048h to 00ECh, subsequently. For example, for VC1, the registers take the address range 0048h-005Ch...etc

1A145034 K_FC_VC0_1 Flow Control Information for Virtual Cannel 0 (similar for VC1-7) - the 2nd DW 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									k_fc_vc0_1							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_fc_vc0_1															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
23:0	k_fc_vc0_1	**Credit VC 0: This variable provides flow control information for VC0.** - k_vc0[35:28]: Receive flow control credit for Non-Posted Data. - k_vc0[43:36]: Receive flow control credit for Completion Headers. - k_vc0[55:44]: Receive flow control credit for Completion Data. The corresponding registers for VC1-VC7 of K_FC_VC0_0 (0030h) to k_PTR_VC0_3 (0044h) range from 0048h to 00ECh, subsequently. For example, for VC1, the registers take the address range 0048h-005Ch...etc

1A145038 K_PTR_VC0_0 Recive Buffer Pointers VC 0 (similar for VC1-7) - the 1st DW 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_ptr_vc0_pc_min**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	k_ptr_vc0_pc_min	**Pointer 0: Pointer signals maintain address boundaries for Posted and Non-Posted requests stored in the Receive buffer.** [G_RX_BUF - 1:0]: pc_min0: The minimum Receive buffer address for Posted requests stored in DPRAM.

Bit(s)	Name	Description
		The corresponding registers for VC1-VC7 of K_FC_VC0_0 (0030h) to k_PTR_VC0_3 (0044h) range from 0048h to 00ECh, subsequently. For example, for VC1, the registers take the address range 0048h-005Ch...etc

1A14503C K_PTR_VC0_1 Recive Buffer Pointers VC 0 (similar for VC1-7) - the 2nd DW 000003BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_ptr_vc0_pc_max**															
Type	RW															
Reset	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	k_ptr_vc0_pc_max	**[2 X G_RX_BUF -1:G_RX_BUF]: pc_max0** The maximum Receive buffer address for Posted requests stored in DPRAM. The corresponding registers for VC1-VC7 of K_FC_VC0_0 (0030h) to k_PTR_VC0_3 (0044h) range from 0048h to 00ECh, subsequently. For example, for VC1, the registers take the address range 0048h-005Ch...etc

1A145040 K_PTR_VC0_2 Recive Buffer Pointers VC 0 (similar for VC1-7) - the 3rd DW 000003C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_ptr_vc0_np_min															
Type	RW															
Reset	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	k_ptr_vc0_np_min	**[3 X G_RX_BUF -1: G_RX_BUF X 2]: np_mino** The minimum Receive buffer address for Non-Posted requests stored in DPRAM. The corresponding registers for VC1-VC7 of K_FC_VC0_0 (0030h) to k_PTR_VC0_3 (0044h) range from 0048h to 00ECh, subsequently. For example, for VC1, the registers take the address range 0048h-005Ch...etc

1A145044 K_PTR_VC0_3 Recive Buffer Pointers VC 0 (similar for VC1-7) - the 4th DW 000003FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_ptr_vc0_np_max															
Type	RW															
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	k_ptr_vc0_np_max	**[4 X G_RX_BUF -1: G_RX_BUF X 3]: np_maxo** The maximum Receive buffer address for Non-Posted requests stored in DPRAM.

Bit(s)	Name	Description
		The corresponding registers for VC1-VC7 of K_FC_VC0_0 (0030h) to k_PTR_VC0_3 (0044h) range from 0048h to 00ECh, subsequently. For example, for VC1, the registers take the address range 0048h-005Ch...etc

1A145100 K_CONF_FUNC0_0 Configuration Space Header 00h 32580E8D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_dev_id															
Type	RW															
Reset	0	0	1	1	0	0	1	0	0	1	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_conf_vendor_id															
Type	RW															
Reset	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0	1

Bit(s)	Name	Description
31:16	k_conf_dev_id	**k_conf[31:16]: Device ID**
15:0	k_conf_vendor_id	**k_conf[15:0]: Vendor ID**

1A145104 K_CONF_FUNC0_1 Configuration Space Header 08h 00020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_class_code															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_conf_class_code								k_conf_rev_id							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	k_conf_class_code	**k_conf[63:40]: Class code.**
7:0	k_conf_rev_id	**k_conf[39:32]: Revision ID**

1A145108 K_CONF_FUNC0_2 Configuration Space Header 2Ch 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**k_conf_subsys_dev_id**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_conf_subsys_vendor_id**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	k_conf_subsys_dev_id	**k_conf[95:80]: Subsystem device ID**
15:0	k_conf_subsys_vendor_id	**k_conf[79:64]: Subsystem vendor ID**

1A14510C K_CONF_FUNC0_3 Individual function 0 configuration, the 4th DW 000001C1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**k_conf_rej_snoop_trans**								**k_conf_vc_arb_cap**				**k_conf_lpvc_num**			**k_conf_aer_en**
Type	RW								RW				RW			RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_conf_pme_sup**					**k_conf_d2_sup**	**k_conf_d1_sup**	**k_conf_max_current**			**k_conf_dsi**	**k_conf_pme_imp**	**k_conf_pme_clk**		**k_conf_flr_cap**	**k_conf_no_soft_rst**

Type	RW					RW	RW	RW			RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	1	1	1	0	0	0		0	1

Bit(s)	Name	Description
31:24	k_conf_rej_snoop_trans	**k_conf_FUNC1[127:120]: Reject Snoop Transaction (VC Resource Capability Register).** This variable is reserved for future use and should be set to 0.
23:20	k_conf_vc_arb_cap	**k_conf_FUNC1[119:116]: VC arbitration capabilities (Port VC Capability Register 2).** This variable should be hardwired to 0001 (simple RR).
19:17	k_conf_lpvc_num	**k_conf_FUNC1[115:113]: Number of Low Priority VCs (LPVC)** (Port VC Capability Register 1)
16	k_conf_aer_en	**k_conf_FUNC1[112]: 1 = Advanced Error Reporting enabled.**
15:11	k_conf_pme_sup	**k_conf_FUNC1[111:107]: PME Support (PMC).** This signal indicates the PM states within which a Power Management Event (PME) message can be sent. A bit set to 0 indicates that a message cannot be sent in the respective state. - k_conf_FUNC1[107]: D0 PME - k_conf_FUNC1[108]: D1 PME - k_conf_FUNC1[109]: D2 PME - k_conf_FUNC1[110]: D3 hot PME - k_conf_FUNC1[111]: D3 cold
10	k_conf_d2_sup	**k_conf[106]: D2 support (PMC).**
9	k_conf_d1_sup	**k_conf[105]: D1 support (PMC).**
8:6	k_conf_max_current	**k_conf[104:102]: Maximum Current Required (PMC).** - 111: 375 mA - 110: 320 mA - 101: 270 mA - 100: 220 mA - 011: 160 mA - 010: 100 mA

Bit(s)	Name	Description
		- 001: 55 mA - 000: 0 mA (If either D3Cold or PM Data Register are not checked
5	k_conf_dsi	**k_conf[101]: Device-specific initialization (DSI) (Power Management Capabilities)**
4	k_conf_pme_imp	**k_conf[100]:** - 0: Power Management Capability Structure registers not implemented - 1: Power Management Capability Structure registers implemented
3	k_conf_pme_clk	**k_conf[99]: PME clock** Does not apply to PCI Express and must be hardwired to 0.
1	k_conf_flr_cap	**k_conf[97]: Function Level Reset (FLR) capability for Endpoints only (Device Capabilities Register).** - 0: Function does not support FLR - 1: Function supports FLR When the port is not an Endpoint, this register is set to 0.
0	k_conf_no_soft_rst	**k_conf[96]: No Soft Reset (PMCSR).** - 0: Devices perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset, and the full reinitialization sequence is required to return the device to D0 Initialized. - 1: Devices transitioning from D3hot to D0 due to PowerState commands do not perform an internal reset. No additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. Note: if PME is enabled, then devices that transition from D3hot to D0 via a system or bus segment reset will return to the D0 Uninitialized device state with only the PME context preserved

1A14511C K_CONF_FUNC0_4 Individual function 0 configuration, the 5th DW 27088341

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_l1_exit_lat_sep			k_conf_l1_exit_lat_com			k_conf_l1	k_conf_lo	k_conf_max_link_width						k_conf_slot_pwr_scale	

							s_sup	s_sup								
Type	RW			RW			RW	RW	RW						RW	
Reset	0	0	1	0	0	1	1	1	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_conf_rcb**	**k_conf_pwr_ind_present**	**k_conf_att_ind_present**	**k_conf_att_but_present**	**k_conf_l1s_lat**			**k_conf_los_lat**			**k_conf_ext_tag_sup**	**k_conf_dlink_active_rpt**	**k_conf_surp_down_rpt**	**k_conf_max_payload**		
Type	RW	RW	RW	RW	RW			RW			RW	RW	RW	RW		
Reset	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	k_conf_l1_exit_lat_sep	**k_conf_FUNC1[159:157]: L1 exit latency for separated clock (Link Capabilities Register).**
28:26	k_conf_l1_exit_lat_com	**k_conf_FUNC1[156:154]: L1 exit latency for common clock (Link Capabilities Register).**
25	k_conf_l1s_sup	**k_conf_FUNC1[153]: L1 Active State power management support (Link Capabilities Register).**
24	k_conf_los_sup	**k_conf_FUNC1[152]: Los Active State power management support (Link Capabilities Register).**
23:18	k_conf_max_link_width	**k_conf_FUNC1[151:146]: Max Link width (Link Capabilites Register).** - 00 000b: Reserved - 00 0001b: x1 - 00 0010b: x2 - 00 0100b: x4 - 00 1000b: x8 - 00 1100b: x12 - 01 0000b: x16 - 10 0000b: x32
17:16	k_conf_slot_pwr_scale	**k_conf_FUNC1[145:144]: Slot Power Limit Scale (Device Capabilities Register)** From Set_Slot_Power_Limit Message or hardwired to 00b.

Bit(s)	Name	Description
15	k_conf_rcb	**k_conf_FUNC1[143]: Read Completion Boundary (RCB) support (Link Control Register).** - 0: 64 bytes - 1: 128 bytes
14	k_conf_pwr_ind_present	**k_conf_FUNC1[142]: Power indicator present for an Endpoint (Device Capabilities Register).**
13	k_conf_att_ind_present	**k_conf_FUNC1[141]: Attention indicator present for an Endpoint (Device Capabilities Register).**
12	k_conf_att_but_present	**k_conf_FUNC1[140]: Attention button present on the device (Device Capabilities Register).**
11:9	k_conf_l1s_lat	**k_conf_FUNC1[139:137]: Endpoint L1 acceptable latency (Link Capabilities Register).**
8:6	k_conf_los_lat	**k_conf_FUNC1[136:134]: Endpoint Los acceptable latency (Link Capabilities Register).**
5	k_conf_ext_tag_sup	**k_conf_FUNC1[133]: Extended TAG field supported (Device Capabilities Register).** - 0: 5-bit Tag field supported - 1: 8-bit Tag field supported
4	k_conf_dlink_active_rpt	**k_conf_FUNC1[132]: Data Link Layer active reporting capabilities (not available for PCIe 1.0a compliant Cores) (Link Capabilities Register).** Downstream Port: 1 = component can report the DL_Active state of the Data Link Control and Management state machine. Upstream Port: this variable is hardwired to 0.
3	k_conf_surp_down_rpt	**k_conf_FUNC1[131]: Surprise Down error reporting capabilities (not available for PCI Express Base Specification Revision 1.0a compliant Cores) (Link Capabilities Register).** Downstream Port: 1 = component can detect and report a Surprise Down error condition. Upstream Port: this variable is hardwired to 0.
2:0	k_conf_max_payload	**k_conf_FUNC1[130:128]: Max payload size supported (Device Capabilities Register).** - 000: 128 bytes - 001: 256 bytes - 010: 512 bytes - 011: 1024 bytes

Bit(s)	Name	Description
		- 100: 2048 bytes - 101: 4096 bytes Otherwise: Reserved

1A145114 K_CONF_FUNC0_5 Individual function 0 configuration, the 6th DW 00000080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_phy_slot_num													k_conf_electro_intlk_present	k_conf_slot_pwr_limit_value	
Type	RW													RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_conf_slot_pwr_limit_value								k_conf_clk_pwr_mgm_sup	k_conf_hot_plug						
Type	RW								RW	RW						
Reset	0	0	0	0	0	0			1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:19	k_conf_phy_slot_num	**k_conf_FUNC1[191:179]: Physical Slot Number (if slot implemented) (Slot Capabilities Register).** This signal indicates the physical slot number associated with this port and must be unique within the fabric.
18	k_conf_electro_intlk_present	**k_conf_FUNC1[178]: 1 = Electromechanical Interlock present (not available with PCIe 1.0a) (Slot Capabilities Register).**

Bit(s)	Name	Description
17:10	k_conf_slot_pwr_limit_value	**k_conf_FUNC1[177:170]: Slot Power Limit Value (Slot Capabilites Register).**
7	k_conf_clk_pwr_mgm_sup	**k_conf_FUNC1[167]: Clock power management support (Link Capabilities Register).**
6:0	k_conf_hot_plug	**k_conf_FUNC1[166:160]: Hot-plug feature (only applies to downstream ports and only when slot is implemented) (Slot Capabilities Register).** - k_conf_FUNC1[160]: 1 = Attention button implemented on the chassis - k_conf_FUNC1[161]: 1 = Power controller present - k_conf_FUNC1[162]: 1 = Manually Operated Retention Latch (MRL) sensor present - k_conf_FUNC1[163]: 1 = Attention indicator present for a Rootport, Switch, or Bridge. - k_conf_FUNC1[164]: 1 = Power indicator present for a Rootport, Switch, or Bridge. - k_conf_FUNC1[165]: Hot-plug surprise: 1 = device can be removed from this slot without prior notification. - k_conf_FUNC1[166]: 1 = Hot-plug capable

1A145118 K_CONF_FUNC0_6 Individual function 0 configuration, the 7th DW 0700FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_funco_6_rcv_27					k_conf_no_cmd_comp_sup	k_conf_ecrc_check	k_conf_ecrc_gen	k_conf_funco_6_rcv_21			k_conf_comp_to_dis_sup	k_conf_comp_to_range_sup			
Type	RO					RW	RW	RW	RO			RW	RW			
Reset	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_conf_fast_train_cfg															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:27	k_conf_func0_6_rcv_27	**Reserved**
26	k_conf_no_cmd_comp_sup	**k_conf_FUNC1[218]: (Slot Capabilities Register).** 1 = No command completed support (not available with PCIe 1.0a) When set, this bit indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug controller. This bit is only permitted to be set if the hot-plug capable port is able to accept writes to all fields of the Slot Control register without delay between successive writes.
25	k_conf_ecrc_check	**k_conf_FUNC1[217] (Advanced Error Capabilities and Control Register).** - 0: Disable ECRC check capability - 1: Enable ECRC check capability
24	k_conf_ecrc_gen	**k_conf_FUNC1[216] (Advanced Error Capabilities and Control Register).** - 0: Disable ECRC generation capability - 1: Enable ECRC generation capability
23:21	k_conf_func0_6_rcv_21	**Reserved**
20	k_conf_comp_to_dis_sup	**k_conf_FUNC1[212]: 1 = Completion timeout mechanism disable support (Device Capabilities 2 Register).** When set to 0, the Core use the default completion timeout period of 50 ms for each transaction. This setting is optional for Rootports, but must be hardwired to 0 for all other devices.
19:16	k_conf_comp_to_range_sup	**k_conf_FUNC1[211:208]: Completion timeout range supported (Device Capabilities 2 Register).** - 0000: Completion timeout programming not supported. The function must implement a timeout value in the range 50us ~ 50ms. - 0001: 50us ~ 10ms - 0010: 10ms ~ 250ms - 0011: 50us ~ 250ms - 0110: 10ms ~ 4s - 0111: 50us ~ 4s - 1110: 10ms ~ 4s - 1111: 50us ~ 4s

Bit(s)	Name	Description
15:0	k_conf_fast_train_cfg	**k_conf_FUNC1[207:192]:** - k_conf_FUNC1[199:192]: NFTS_SEPCLK: Number of fast training sequences for the separate clock at 2.5Gbps. - k_conf_FUNC1[207:200]: NFTS_COMCLK: Number of fast training sequences for the common clock at 2.5Gbps.

1A14511C K_CONF_FUNC0_7 Individual function 0 configuration, the 8th DW 20000068

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_lpbk_exit_tim								k_conf_func0_7_rsv23	k_conf_msix_tab_size						
Type	RW								RO	RW						
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_conf_msix_tab_size				k_conf_msix_sup	k_conf_func0_7_rsv9		k_conf_int_pin			k_conf_msi_sup	k_conf_msi_per_bit_mask	k_conf_msi_addr_mode	k_conf_msi_num		
Type	RW				RW	RO		RW			RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0

Bit(s)	Name	Description
31:24	k_conf_lpbk_exit_tim	**extend txdetectrx when exiting loopback mode for 8 EIOS** 8ns~1024ns, 8ns/scale
23	k_conf_func0_7_rsv23	**Reserved**
22:12	k_conf_msix_tab_size	**k_conf_FUNC1[305:295]: MSI-X Table Size**
11	k_conf_msix_sup	**k_conf_FUNC1[230]: 1 = Function supports MSI-X**
10:9	k_conf_func0_7_rsv9	**Reserved**

Bit(s)	Name	Description
8:6	k_conf_int_pin	**k_conf_FUNC1[227:225]: Interrupt pin (Configuration Space Header)** - 0: Do not use INTx pin - 1: Use INTA pin - 2: Use INTB pin - 3: Use INTC pin - 4: Use INTD pin Otherwise: reserved
5	k_conf_msi_sup	**k_conf_FUNC1[224]:** - 0: Function not support MSI - 1: Function supports MSI
4	k_conf_msi_per_bit_mask	**k_conf_FUNC1[223]: MSI per-bit vector masking (read-only field) (Message Control)**
3	k_conf_msi_addr_mode	**k_conf_FUNC1[222]: MSI 32/64-bit addressing mode (Message Control).** - 0: 32 bits addressing only - 1: 32 or 64 bits addressing available
2:0	k_conf_msi_num	**k_conf_FUNC1[221:219]: Number of MSI the function can generate (Message Control).** - 000: 1 MSI - 001: 2 MSI - 010: 4 MSI - 011: 8 MSI - 100: 16 MSI - 101: 32 MSI

1A145120 K_CONF_FUNC0_8 Individual function 0 configuration, the 9th DW 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_msix_pba_offset															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_conf_msix_pba_offset**													**k_conf_msix_pba_bir**		
Type	RW													RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:3	k_conf_msix_pba_offset	**k_conf_FUNC1[262:234]: MSI-X PBA Offset**
2:0	k_conf_msix_pba_bir	**k_conf_FUNC1[233:231]: MSI-X PBA BIR**

1A145124 K_CONF_FUNC0_9 Individual function 0 configuration, the 10th DW 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**k_conf_msix_tab_offset**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_conf_msix_tab_offset**													**k_conf_msix_tab_bir**		
Type	RW													RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:3	k_conf_msix_tab_offset	**k_conf_FUNC1[294:266]: MSI-X Table Offset**
2:0	k_conf_msix_tab_bir	**k_conf_FUNC1[265:263]: MSI-X Table BIR**

1A145128 K_CONF_FUNC0_10 Individual function 0 configuration, the 11th DW 013FFFE0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**k_conf_funco_10_rcv_27**					**k_conf_ver_cap**				**k_conf_sel_d**	**k_conf_nfts_comclk**					

										ee mp						
Type	RO					RW				RW	RW					
Reset	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**k_conf_nfts_comclk**		**k_conf_nfts_sepclk**								**k_conf_eie_num**				**k_conf_ssid_cap_imp**	**k_conf_vga_en**
Type	RW		RW								RW				RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
31:27	k_conf_func0_10_rcv_27	**Reserved**
26:23	k_conf_ver_cap	**k_conf_FUNC1[364:361]:** PCI Express specification version capability - 0001: Core is compliant with PCIe Specification 1.0a or 1.1 (depending on the setting for k_gbl[0] - 0010: Core is compliant with PCIe Specification 2.0
22	k_conf_sel_deemp	**k_conf_FUNC1[360]: Selectable de-emphasis** Selects the level of de-emphasis for an upstream component when the link is operating at 5.0 Gbps - 0: de-emphasis of 6 dB - 1: de-emphasis of 3.5 dB When the link is operating at 2.5 Gbps, this variable should be hardwired to 0.
21:14	k_conf_nfts_comclk	**k_conf_FUNC1[359:352]: NFTS_COMCLK** Number of fast training sequences for the common clock at 5.0 Gbps. Minimum is 5.
13:6	k_conf_nfts_sepclk	**k_conf_FUNC1[351:344]: NFTS_SEPCLK**

Bit(s)	Name	Description
		Number of fast training sequences for the separate clock at 5.0 Gbps. Minimum is 5.
5:2	k_conf_eie_num	**k_conf_FUNC1[343:340]: Number of Electrical Idle Exit (EIE) symbols sent before transmitting the first FTS.** For the 8-bit PIPE version of the Core, any value between 4-8 is permitted, but for the 16-bit PIPE version, only the values 6 and 8 are permitted. The default value for both versions is 8.
1	k_conf_ssid_cap_imp	**k_conf_FUNC1[307]: 1 = SSID/SSVID capabilities implemented (Bridge ports only)**
0	k_conf_vga_en	**k_conf_FUNC1[306]: 1 = VGA Enable (Bridge ports only)**

1A14512C K_CONF_FUNC0_11 Individual function 0 configuration, the 12th DW 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_conf_ssid															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_conf_ssvid															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	k_conf_ssid	**k_conf_FUNC1[339:324]: SSID (Bridge ports only)**
15:0	k_conf_ssvid	**k_conf_FUNC1[323:308]: SSVID (Bridge ports only)**

1A145130 K_CONF_FUNC0_12 Individual function 0 configuration, the 13th DW 051F1E40

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		k_arb_check_cred	k_lock_support	k_power_on_value						k_power_on_scale		k_l1ss_supported				
Type		RW	RW	RW						RW		RW				
Reset		0	0	0	0	1	0	1		0	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_rxlos_exit_tim									k_conf_elect_idle_exit	k_conf_los_exit_lat_sep			k_conf_los_exit_lat_com		
Type	RW									RW	RW			RW		
Reset	0	0	0	1	1	1	1	0		1	0	0	0	0	0	0

Bit(s)	Name	Description
30	k_arb_check_cred	
29	k_lock_support	
28:24	k_power_on_value	**Along with the k_power_on_scale field in the L1SS capabilities register sets the time (in us) that thist requires the port on the opposite side of Link to wait in L1.2 exit after sampling CLKREQ# asserted before actively driving the interface. The value of T_POWER_ON is calculated by multiplying the value in this field by the scale in this field by the scale value.**
22:21	k_power_on_scale	**Specifies the scale used for the k_power_on_value field in the L1SS capabilities register** 00 : 2us 01 : 10us 10 : 100us 11: Reserved
20:16	k_l1ss_supported	**k_l1ss_supported[0] : PCI-PM L1.2 supported** k_l1ss_supported[1] : PCI-PM L1.1 supported k_l1ss_supported[2] : ASPM L1.2 supported k_l1ss_supported[3] : ASPM L1.1 supported

Bit(s)	Name	Description
		k_l1ss_supported[4] : L1SS supported
15:8	k_rxlos_exit_tim	**L1ss_common_mode_restore_time capability.** The register will be used to Port_Common_Mode_Restore_Time in L1SS capability regiseter (offset 0x04) The register shall be Local PHY TX common mode restore time.
6	k_conf_elect_idle_exit	**k_conf_FUNC1[371]: Electrical Idle exit condition** This signal defines when the Core exits Electrical Idle. - 0: Exit Electrical Idle when the signal RXELECIDLE is de-asserted for all configured lanes (normal operation). - 1: When the Core Rx lanes are in Los or L1 state, exit Electrical Idle after the signal RXELECIDLE is inactive for the number of clock cycles defined by k_cnt[51:44].
5:3	k_conf_los_exit_lat_sep	**k_conf_FUNC1[370:368]: Los exit latency for separated clock at 5 Gbps (Link Capabilities Register).** - 000: < 64ns - 001: 64ns ~ 128ns - 010: 128ns ~ 256ns - 011: 256ns ~ 512ns - 100: 512ns ~ 1us - 101: 1us ~ 2us - 110: 2us ~ 4us - 111: > 4us
2:0	k_conf_los_exit_lat_com	**k_conf_FUNC1[367:365]: Los exit latency for common clock at 5 Gbps (Link Capabilities Register).** - 000: < 64ns - 001: 64ns ~ 128ns - 010: 128ns ~ 256ns - 011: 256ns ~ 512ns - 100: 512ns ~ 1us

Bit(s)	Name	Description
		- 101: 1us ~ 2us - 110: 2us ~ 4us - 111: > 4us

1A145134 K_BAR_FUNC0_0 BAR0 Configuration. Note:A BAR cannot be modified if the previous BAR uses 64-bit addressing. FFF00004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_baro															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_baro															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
31:0	k_baro	**BAR0[31:0]** - BAR0[0]: I/O Space - BAR0[2:1]: Memory Space -> 10: 64-bit address -> 00: 32-bit address - BAR0[3]: Prefetchable - BAR0[31:4]: Bar size mask

1A145138 K_BAR_FUNC0_1 BAR1 Configuration. FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_bar1															
Type	RW															

Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_bar1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	k_bar1	**BAR1[63:32]** - BAR1[32]: I/O Space - BAR1[34:33]: Memory Space (see bit settings for BAR0) - BAR1[35]: Prefetchable - BAR1[63:36]: Bar size mask

1A14513C K_BAR_FUNC0_2 BAR2 Configuration. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_bar2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_bar2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	k_bar2	**BAR2[95:64]** - BAR2[64]: I/O Space - BAR2[66:65]: Memory Space (see bit settings for BAR0) - BAR2[67]: Prefetchable - BAR2[95:68]: Bar size mask

1A145140 K_BAR_FUNC0_3 BAR3 Configuration. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_bar3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_bar3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	k_bar3	**BAR3[127:96]** - BAR3[96]: I/O Space - BAR3[98:97]: Memory Space (see bit settings for BAR0) - BAR3[99]: Prefetchable - BAR3[127:100]: Bar size mask

1A145144 K_BAR_FUNC0_4 BAR4 Configuration. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_bar4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_bar4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	k_bar4	**BAR4[159:128]** - BAR4[128]: I/O Space

Bit(s)	Name	Description
		- BAR4[130:129]: Memory Space (see bit settings for BAR0) - BAR4[131]: Prefetchable - BAR4[159:132]: Bar size mask

1A145148 K_BAR_FUNC0_5 BAR5 Configuration. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_bar5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_bar5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	k_bar5	**BAR5[191:160]** - BAR5[160]: I/O Space - BAR5[162:161]: Memory Space (see bit settings for BAR0) - BAR5[163]: Prefetchable - BAR5[191:164]: Bar size mask

1A14514C K_BAR_FUNC0_6 Expansion ROM Configuration 1. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	k_bar_exp_rom_mask															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_bar_exp_rom_mask															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	k_bar_exp_rom_mask	**k_bar_func[223:192]: Bar size mask**

1A145150 K_BAR_FUNC0_7 Expansion ROM Configuration 2. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**k_bar_exp_rom_pref**		**k_bar_exp_rom_mode**	
Type													RW		RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3:2	k_bar_exp_rom_pref	**k_bar_FUNC1[227:226] prefetchable** - 00: not implemented - 01: prefetchable 32 - 11: prefetchable 64
1:0	k_bar_exp_rom_mode	**k_bar_FUNC1[225:224]: IO** - 00: no IO windows - 01: IO 16 bit - 11: IO 32 bit

1A145154 K_CONF_LTR_OBFF LTR AND OBFF Support Hwinit 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											k_conf_obff_sup					k_conf_ltr_sup
Type											RW					RW
Reset											0	0				1

Bit(s)	Name	Description
5:4	k_conf_obff_sup	**- 00: OBFF not support** - 01: OBFF supprted using message signaling only - 10: OBFF suppoted using WAKE# signaling only - 11: OBFF suppoted using WAKE# and message signaling
0	k_conf_ltr_sup	**- 0: noT support LTR** - 1: support LTR

1A145158 K_CPL_RESOURCE Complete resource 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	k_cpl_resource															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	k_cpl_resource	

1A14515C L_LOCAL_TCOMMON_MODE Tcommon mode time requred by Local PHY RX 00000023

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**k_local_rx_tcommon_mode**							
Type									RW							
Reset									0	0	1	0	0	0	1	1

Bit(s)	Name	Description
7:0	k_local_rx_tcommon_mode	**The time for Local PHY RX to establish common mode when exit from L1P2.** unit : 1us

1A145180 K_CONF_FUNC0_13 MPCIe Configuration space capability 01010303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**k_mpcie_rxwidth_cap**								**k_mpcie_txwidth_cap**							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**k_mpcie_hsrate_cap**								**k_mpcie_hsgear_cap**	
Type							RW								RW	
Reset							1	1							1	1

Bit(s)	Name	Description
31:24	k_mpcie_rxwidth_cap	**MPCIe support RX land width capability** Bit 0 : x1 RX lane is supported Bit 1 : x2 RX lane is supported Bit 2 : x4 RX lane is supported

Bit(s)	Name	Description
		Bit 3 : x8 RX lane is supported
		Bit 4 : x12 RX lane is supported
		Bit 5 : x16 RX lane is supported
		Bit 6 : x32 RX lane is supported
		Bit7 : Reserved
23:16	k_mpcie_txwidth_cap	**MPCIe support TX land width capability**
		Bit 0 : x1 TX lane is supported
		Bit 1 : x2 TX lane is supported
		Bit 2 : x4 TX lane is supported
		Bit 3 : x8 TX lane is supported
		Bit 4 : x12 TX lane is supported
		Bit 5 : x16 TX lane is supported
		Bit 6 : x32 TX lane is supported
		Bit7 : Reserved
9:8	k_mpcie_hsrate_cap	**MPCIe support HS RATE capability**
		Bit 0 : RATE A
		Bit 1 : RATE B
1:0	k_mpcie_hsgear_cap	**MPCIe support HS GEAR capability**
		Bit 0 : Gear 1
		Bit 1 : Gear 2

1A145400 WDMA_PCIE_ADDR_L Write DMA start PCIe address LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	wdma_pciaddr_l															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdma_pciaddr_l															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	wdma_pciaddr_l	**This register specifies the LSB start PCIe address of the write DMA transfer. For IO, configuration and DW transfers this address must be 32-bit aligned.**

1A145404 WDMA_PCIE_ADDR_H Write DMA start PCIe address MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	wdma_pciaddr_h															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdma_pciaddr_h															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	wdma_pciaddr_h	**This register specifies the MSB start PCIe address of the write DMA transfer.**

1A145408 WDMA_BUS_ADDR Write DMA start BUS address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	wdma_bus_addr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdma_bus_addr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	wdma_bus_addr	**This register specifies the start bus address of the memory location where data must be read from. For IO, configuration and DW transfers this address must be 32-bit aligned.**

1A14540C WDMA_CONTROL Write DMA control parameters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	wdma_length															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdma_length				wdma_be				wdma_multi_outstanding	wdma_cmd			wdma_rsv_2		wdma_stop	wdma_start
Type	RW				RW				RW	RW			RO		WO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	wdma_length	**This field specifies the amount of data in byte unit. Burst transfer up to 1MB. IO, configuration and Memory DW transfers must be 4 bytes (0x00004). The value must not cross a 4GB address boundary.** 0x00001 & wdma_be = 4'b0 : 0B 0x00001 : 1B 0x00002 : 2B 0xFFFFF : (2^20-1)B 0x00000 : 1MB
11:8	wdma_be	**This field specifies the byte enable for IO, configuration and Memory DW transfers.**

Bit(s)	Name	Description
7	wdma_multi_outstanding	**WDMA can send multi memory read with different tag. But target must send completion in order.**
6:4	wdma_cmd	**This field specifies the PCIe command used to transfer data.** - 000: I/O Read (not allowed if device is a native EP) - 010: Memory Read DW - 100: Configuration Read (not allowed if device is an EP) - 110 Memory Read Burst
3:2	wdma_rsv_2	**Reserved**
1	wdma_stop	**This bit is used to abort a transfer in progress. A partial and unknown amount of data can be transferred before transfer stops.** Always returns 0 when read.
0	wdma_start	**Assertion of this bit initiates WDMA transfer. This bit is automatically cleared when the transfer is completed. This bit can be monitored by software in order to verify whether the WDMA channel is busy.** Note that the wdma_start is ignored if wdma_cmd is illigal or if wdma_length is null, in which case no transfer is initialted and no interrupt is generated.

1A145410 RDMA_PCIE_ADDR_L Read DMA start PCIe address LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rdma_pciaddr_l															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdma_pciaddr_l															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rdma_pciaddr_l	**This register specifies the LSB start PCIe address of the read DMA transfer. For IO, configuration and DW transfers this address must be 32-bit aligned.**

1A145414 RDMA_PCIE_ADDR_H Read DMA start PCIe address MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rdma_pciaddr_h															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdma_pciaddr_h															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rdma_pciaddr_h	**This register specifies the MSB start PCIe address of the read DMA transfer.**

1A145418 RDMA_BUS_ADDR Read DMA start BUS address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rdma_bus_addr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdma_bus_addr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rdma_bus_addr	**This register specifies the start bus address of the memory location where data must be written to.** For IO, configuration and DW transfers this address must be 32-bit aligned.

1A14541C RDMA_CONTROL Read DMA control parameters 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rdma_length															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdma_length				rdma_be				rdma_rsv_7	rdma_cmd			rdma_rsv_2		rdma_stop	rdma_start
Type	RW				RW				RO	RW			RO		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	rdma_length	**This field specifies the amount of data in byte unit. Burst transfer up to 1MB. IO, configuration and Memory DW transfers must be 4 bytes (0x00004). The value must not cross a 4GB address boundary.** 0x00001 & rdma_be = 4'b0 : 0B 0x00001 : 1B 0x00002 : 2B 0xFFFFF : (2^20-1)B 0x00000 : 1MB
11:8	rdma_be	**This field specifies the byte enable for IO, configuration and Memory DW transfers.**
7	rdma_rsv_7	**Reserved**
6:4	rdma_cmd	**This field specifies the PCIe command used to transfer data.**

Bit(s)	Name	Description
		- 001: I/O Write (not allowed if device is a native EP) - 011: Memory Write DW - 101: Configuration Write (not allowed if device is an EP) - 111 Memory Write Burst
3:2	rdma_rsv_2	**Reserved**
1	rdma_stop	**This bit is used to abort a transfer in progress. A partial and unknown amount of data can be transferred before transfer stops.** Always returns 0 when read.
0	rdma_start	**Assertion of this bit initiates RDMA transfer. This bit is automatically cleared when the transfer is completed. This bit can be monitored by software in order to verify whether the RDMA channel is busy.** Note that the rdma_start is ignored if rdma_cmd is illigal or if rdma_length is null, in which case no transfer is initialted and no interrupt is generated.

1A145420 INT_MASK Interrupt Mask FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mpcie_cfg_soft_mask	pcie_rc_l2_wake_mask	legacy_pm_chg_mask	ltr_en_mask	ltr_msg_mask	cpu_active_mask	obff_mask	obff_idle_mask	msi_mask	aer_event_mask	pm_hp_event_mask	ser_mask	intd_mask	intc_mask	intb_mask	inta_mask
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_mask_rsv_15	b2p_disc ard_mask	b2p_rerr_mask	int_mask_rsv_12	p2b_wr_win1_mask	p2b_wr_win0_mask	p2b_rerr_mask	p2b_werr_mask	int_mask_rsv_7	rdma_berr_mask	rdma_perr_mask	rdma_end_mask	int_mask_rsv_3	wdma_berr_mask	wdma_perr_mask	wdma_end_mask
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31	mpcie_cfg_soft_mask	**The bit indicate MPCIe LTSSM has entered cfg.software status and SW can start link discovery and configuration flow.** 1 : disable interrupt. 0 : enable interrupt.
30	pcie_rc_l2_wake_mask	**The bit indicate PCIe RC detect remote wakeup from EP in L2 state.** 1 : disable interrupt. 0 : enable interrupt.
29	legacy_pm_chg_mask	**This bit indicates that the PCI legacy power management state has been modified on the PCI PMCSR configuration register. In order to re-establish power state D0, the local processor must generate the PME# interrupt to PCI host processor.**
28	ltr_en_mask	**This bit asserts when LTR is enabled by RC.**
27	ltr_msg_mask	**This bit asserts when LTR message is received.**
26	cpu_active_mask	**This bit asserts when obff_cpu_active message is received.**
25	obff_mask	**This bit asserts when obff_obff message is received.**
24	obff_idle_mask	**This bit asserts when obff_idle message is received.**
23	msi_mask	**This bit is asserted each time an MSI interrupt is received. Local processor should clear this bit and read IMSISTATUS register to identify the interrupt source.** EP mode always returns 0.
22	aer_event_mask	**This bit is asserted each time an error is detected by AER if this feature is enabled. Local processor should clear this bit and then read AER capabilities registers located in configuration space to identify the error source.** EP mode always returns 0.
21	pm_hp_event_mask	**This bit is asserted each time a hot-plug or power management message is received. Local processor should clear this bit and then read Slot and Root CSR registers to identify the event source.** EP mode always returns 0.
20	serr_mask	**This bit is asserted when a system error is detected by the root port. Events and conditions that result in system errors are defined in PCI Express specification.** EP mode always returns 0.

Bit(s)	Name	Description
19	intd_mask	**This bit indicates when interrupt line INTD is asserted. Note the bit remains asserted (even if cleared by an AHB/AXI write) as long as INTD line is not de-asserted by EP.** EP mode always returns 0.
18	intc_mask	**This bit indicates when interrupt line INTC is asserted. Note the bit remains asserted (even if cleared by an AHB/AXI write) as long as INTC line is not de-asserted by EP.** EP mode always returns 0.
17	intb_mask	**This bit indicates when interrupt line INTB is asserted. Note the bit remains asserted (even if cleared by an AHB/AXI write) as long as INTB line is not de-asserted by EP.** EP mode always returns 0.
16	inta_mask	**This bit indicates when interrupt line INTA is asserted. Note the bit remains asserted (even if cleared by an AHB/AXI write) as long as INTA line is not de-asserted by EP.** EP mode always returns 0.
15	int_mask_rsv_15	**Reserved**
14	b2p_discard_mask	**This interrupt is issued to signal that the number of clock cycles specified by the AHB_TIMER register has been reached an that remaining data is being flushed.**
13	b2p_rerr_mask	**This interrupt is asserted if the data requested from the bus cannot be read by the PCIe.**
12	int_mask_rsv_12	**Reserved**
11	p2b_wr_win1_mask	**This interrupt is asserted when a write request received from the PCIe bus has been successfully posted to the AHB/AXI bus by the PCI2BUS window 1.**
10	p2b_wr_win0_mask	**This interrupt is asserted when a write request received from the PCIe bus has been successfully posted to the AHB/AXI bus by the PCI2BUS window 0.**
9	p2b_rerr_mask	**This interrupt is asserted when a read request is received from the PCIe but the corresponding data cannot be read from the AHB/AXI bus because an AHB/AXI error has occured.**
8	p2b_werr_mask	**This interrupt is asserted when a request received from the PCIe cannot be posted to the AHB/AXI bus because an AHB/AXI error has occured.**
7	int_mask_rsv_7	**Reserved**

Bit(s)	Name	Description
6	rdma_berr_mask	**This interrupt indicates that an error occured on the AHB/AXI bus reading or writing data. This is a fatal error and any data received should be discarded. The local processor should not try to restart the transfer.**
5	rdma_perr_mask	**This interrupt indicates that the requested DMA transfer was ended with an error on PCIe. This is a fatal error and any data received should be discarded. The local processor should not try to restart the transfer.**
4	rdma_end_mask	**This interrupt indicates that the requested DMA transfer is complete or has been stopped as a result of a software request.**
3	int_mask_rsv_3	**Reserved**
2	wdma_berr_mask	**This interrupt indicates that an error occured on the AHB/AXI bus reading or writing data. This is a fatal error and any data received should be discarded. The local processor should not try to restart the transfer.**
1	wdma_perr_mask	**This interrupt indicates that the requested DMA transfer was ended with an error on PCIe. This is a fatal error and any data received should be discarded. The local processor should not try to restart the transfer.**
0	wdma_end_mask	**This interrupt indicates that the requested DMA transfer is complete or has been stopped as a result of a software request.**

1A145424 INT_STATUS Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	mpcie_cfg_soft_status	pcie_rc_l2_wake_status	legacy_pm_chg_status	ltr_en_status	ltr_msg_status	cpu_active_status	obff_status	obff_idle_status	msi_status	aer_event_status	pm_hp_event_status	serr_status	intd_status	intc_status	intb_status	inta_status
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		b2p_discard_status	b2p_rerr_status	p2b_wr_win2_s	p2b_wr_win1_s	p2b_wr_win0_s	p2b_rerr_status	p2b_werr_status		rdma_berr_status	rdma_perr_status	rdma_end_status		wdma_berr_status	wdma_perr_status	wdma_end_status

				tat us	tat us	tat us										
Type		W1C	W1C	W1C	W1C	W1C	W1C	W1C		W1C	W1C	W1C		W1C	W1C	W1C
Reset		0	0	0	0	0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
31	mpcie_cfg_soft_status	**MPCIe only.** The bit indicate MPCIe LTSSM has entered cfg software status and SW can start link discovery and configuration flow.
30	pcie_rc_l2_wake_status	**The bit indicate PCIe RC detect remote wake from EP in L2 state.**
29	legacy_pm_chg_status	**This bit indicates that the PCI legacy power management state has been modified on the PCI PMCSR configuration register. In order to re-establish power state D0, the local processor must generate the PME# interrupt to PCI host processor.**
28	ltr_en_status	**This bit asserts when LTR is enabled by RC.**
27	ltr_msg_status	**This bit asserts when LTR message is received.**
26	cpu_active_status	**This bit asserts when obff_cpu_active message is received.**
25	obff_status	**This bit asserts when obff_obff message is received.**
24	obff_idle_status	**This bit asserts when obff_idle message is received.**
23	msi_status	**This bit is asserted each time an MSI interrupt is received. Local processor should clear this bit and read IMSISTATUS register to identify the interrupt source.**
22	aer_event_status	**This bit is asserted each time an error is detected by AER if this feature is enabled. Local processor should clear this bit and then read AER capabilities registers located in configuration space to identify the error source.**
21	pm_hp_event_status	**This bit is asserted each time a hot-plug or power management message is received. Local processor should clear this bit and then read Slot and Root CSR registers to identify the event source.**
20	serr_status	**This bit is asserted when a system error is detected by the root port. Events and conditions that result in system errors are defined in PCI Express specification.**
19	intd_status	**This bit indicates when interrupt line INTD is asserted. Note the bit remains asserted (even if cleared by an AHB/AXI write) as long as INTD line is not de-asserted by EP.**
18	intc_status	**This bit indicates when interrupt line INTC is asserted. Note the bit remains asserted (even if cleared by an**

Bit(s)	Name	Description
		AHB/AXI write) as long as INTC line is not de-asserted by EP.
17	intb_status	This bit indicates when interrupt line INTB is asserted. Note the bit remains asserted (even if cleared by an AHB/AXI write) as long as INTB line is not de-asserted by EP.
16	inta_status	This bit indicates when interrupt line INTA is asserted. Note the bit remains asserted (even if cleared by an AHB/AXI write) as long as INTA line is not de-asserted by EP.
14	b2p_discard_status	This interrupt is issued to signal that the number of clock cycles specified by the AHB_TIMER register has been reached an that remaining data is being flushed.
13	b2p_rerr_status	This interrupt is asserted if the data requested from the bus cannot be read by the PCIe.
12	p2b_wr_win2_status	This interrupt is asserted when a write request received from the PCIe bus has been successfully posted to the AHB/AXI bus by the PCI2BUS window 2.
11	p2b_wr_win1_status	This interrupt is asserted when a write request received from the PCIe bus has been successfully posted to the AHB/AXI bus by the PCI2BUS window 1.
10	p2b_wr_win0_status	This interrupt is asserted when a write request received from the PCIe bus has been successfully posted to the AHB/AXI bus by the PCI2BUS window 0.
9	p2b_rerr_status	This interrupt is asserted when a read request is received from the PCIe but the corresponding data cannot be read from the AHB/AXI bus because an AHB/AXI error has occured.
8	p2b_werr_status	This interrupt is asserted when a request received from the PCIe cannot be posted to the AHB/AXI bus because an AHB/AXI error has occured.
6	rdma_berr_status	This interrupt indicates that an error occured on the AHB/AXI bus reading or writing data. This is a fatal error and any data received should be discarded. The local processor should not try to restart the transfer.
5	rdma_perr_status	This interrupt indicates that the requested DMA transfer was ended with an error on PCIe. This is a fatal error and any data received should be discarded. The local processor should not try to restart the transfer.
4	rdma_end_status	This interrupt indicates that the requested DMA transfer is complete or has been stopped as a result of a software request.
2	wdma_berr_status	This interrupt indicates that an error occured on the AHB/AXI bus reading or writing data. This is a fatal error

Bit(s)	Name	Description
		and any data received should be discarded. The local processor should not try to restart the transfer.
1	wdma_perr_status	**This interrupt indicates that the requested DMA transfer was ended with an error on PCIe. This is a fatal error and any data received should be discarded. The local processor should not try to restart the transfer.**
0	wdma_end_status	**This interrupt indicates that the requested DMA transfer is complete or has been stopped as a result of a software request.**

1A145428 INT_RMT_MASK Interrupt Remote Mask 3FFF7F77

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			legacy_pm_chg_rmt_mask	ltr_en_event_mask	ltr_msg_event_mask	cpu_active_event_mask	obff_event_mask	obff_idle_event_mask	serr_rmt_mask	pm_hp_event_rmt_mask	aer_event_rmt_mask	msi_rmt_mask	intd_rmt_mask	intc_rmt_mask	intb_rmt_mask	inta_rmt_mask
Type			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		b2p_discard_rmt_mask	b2p_rerr_rmt_mask	p2b_wr_win2_rmt_mask	p2b_wr_win1_rmt_mask	p2b_wr_win0_rmt_mask	p2b_rerr_rmt_mask	p2b_werr_rmt_mask		rdma_berr_rmt_mask	rdma_perr_rmt_mask	rdma_end_rmt_mask		wdma_berr_rmt_mask	wdma_perr_rmt_mask	wdma_end_rmt_mask
Type		W1C	RW	RW	RW	RW	RW	RW		RW	RW	RW		RW	RW	RW
Reset		1	1	1	1	1	1	1		1	1	1		1	1	1

Bit(s)	Name	Description
29	legacy_pm_chg_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if legacy_pm_chg_status asserts.**
28	ltr_en_event_mask	**The PCIe core will issue MSI or INT message to remote device if LTR is enabled by RC.**

Bit(s)	Name	Description
27	ltr_msg_event_mask	**The PCIe core will issue MSI or INT message to remote device if LTR message is received.**
26	cpu_active_event_mask	**The PCIe core will issue MSI or INT message to remote device if obff_cpu_active message is received.**
25	obff_event_mask	**The PCIe core will issue MSI or INT message to remote device if obff_obff message is received.**
24	obff_idle_event_mask	**The PCIe core will issue MSI or INT message to remote device if obff_idle message is received.**
23	serr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if serr_status asserts.**
22	pm_hp_event_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if pm_hp_event_status asserts.**
21	aer_event_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if aer_event_status asserts.**
20	msi_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if msi_status asserts.**
19	intd_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if intd_status asserts.**
18	intc_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if intc_status asserts.**
17	intb_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if intb_status asserts.**
16	inta_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if inta_status asserts.**
14	b2p_discard_rmt_mask	**This interrupt is issued to signal that the number of clock cycles specified by the AHB_TIMER register has been reached an that remaining data is being flushed.**
13	b2p_rerr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if b2p_rerr_status asserts.**
12	p2b_wr_win2_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if p2b_wr_win2_status asserts.**
11	p2b_wr_win1_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if p2b_wr_win1_status asserts.**
10	p2b_wr_win0_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if p2b_wr_win0_status asserts.**
9	p2b_rerr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if p2b_rerr_status asserts.**
8	p2b_werr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if p2b_werr_status asserts.**

Bit(s)	Name	Description
6	rdma_berr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if rdma_berr_status asserts.**
5	rdma_perr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if rdma_perr_status asserts.**
4	rdma_end_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if rdma_end_status asserts.**
2	wdma_berr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if wdma_berr_status asserts.**
1	wdma_perr_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if wdma_perr_status asserts.**
0	wdma_end_rmt_mask	**The PCIe core will issue MSI or INT message to remote device if wdma_end_status asserts.**

1A14542C IMSI_STATUS MSI Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	imsi_status															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	imsi_status															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	imsi_status	**The content of this register is asserted when an MSI with message number 0~31 is received by the root port. The local processor must monitor and clear these bits by writing 1. Note that MSI with message number greater than 31 are ignored and discarded.**

1A145430 IMSI_ADDR Root port MSI capture address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	imsi_addr															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	imsi_addr															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	imsi_addr	**This register contains MSI capture address. Root port captures all memory writes at this address and treats them as MSI. If specified address is in a PCI-BUS window range then the MSI is not captured and is forwarded to AHB/AXI bus. Note that this address must be 64-bit aligned.**

1A145434 ICMD Interrupt Command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												icmd_to_link	icmd_deassert_clkreq	icmd_send_pme	icmd_int_state	icmd_send_int
Type												WO	WO	WO	RO	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	icmd_to_link	**Local processor write 1 to start L2 state entry negotiation. If EP is also ready to enter this state then both devices will enter L2 and link will be turned off. This bit is immediately cleared by bridge and local processor does not need to clear it.**

Bit(s)	Name	Description
3	icmd_deassert_clkreq	**This bit is used to deassert CLKREQ# pin in order to indicate that PCIe 100MHz reference clock can be safely removed. This pin can only be asserted if:** - CLKREQ# support is enabled - clock power management is enabled in PCIe link control register
2	icmd_send_pme	**Local processor write 1 to generate a PME event on the PCIe link. This is used ask PCI host processor to restore bridge to a fully functional legacy power state. This bit is immediately cleared by bridge and local processor does not need to clear it.**
1	icmd_int_state	**This RO bit reflect the state of PCI interrupt.** - 0: the bridge is not asserting PCI interrupt - 1: the bridge is asserting PCI interrupt
0	icmd_send_int	**The local processor can send interrupts to the PCI host processor through the PCI** Express link. The interrupt is sent using Message Signaled Interrupt if the PCI host processor enabled MSI, or using ASSERT_INTx and DEASSERT_INTx messages otherwise. The local processor must write 1 to send PCI interrupt bit in order to send interrupt. Then it must wait until software driver clears the interrupt (this must be signaled via a user-defined mechanism, usually a register implemented in application logic). And then local processor must write 0 to send PCI interrupt bit in order to release interrupt. The PCI_INT_ASSERT signal can be used instead of this register in order to assert and de-assert a PCI interrupt.

1A145438 AHB2PCIE_BASE0_L AHB slave to PCIe tranlsation table0 LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ahb2pcie_base0_l															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ahb2pcie_baseo_l									ahb2pcie_baseo_noprefetch	ahb2pcie_baseo_reserved	ahb2pcie_baseo_size				
Type	RW									RW	RO	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:7	ahb2pcie_baseo_l	**Translated windowo PCIe base address[31:7].**
6	ahb2pcie_baseo_nopreferch	**No-prefetch disables data prefetch when set.** When it is not set then window is allowed to read data in advance for undefined length AHB read requests.
5	ahb2pcie_baseo_reserved	**reserved**
4:0	ahb2pcie_baseo_size	**This field specifies the windowo size.** Possible values are 7 to 31 which mean 2^7 to 2^31 bytes. Leaving this field to 0 causes windowo to be disabled.

1A14543C AHB2PCIE_BASEo_H AHB slave to PCIe translation tableo MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ahb2pcie_baseo_h															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ahb2pcie_baseo_h															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ahb2pcie_baseo_h	**Translated windowo PCIe base address[63:32].**

Bit(s)	Name	Description
		If 32-bit addreessing is used or no-prefetch bit is set then ahb2pcie_base0_h must be 32'h0.

1A145440 AHB2PCIE_BASE1_L AHB slave to PCIe translation table1 LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ahb2pcie_base1_l															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ahb2pcie_base1_l									ahb2pcie_base1_nopreferch	ahb2pcie_base1_reserved	ahb2pcie_base1_size				
Type	RW									RW	RO	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:7	ahb2pcie_base1_l	**Translated window1 PCIe base address[31:7].**
6	ahb2pcie_base1_nopreferch	**No-prefetch disables data prefetch when set.** When it is not set then window is allowed to read data in advance for undefined length AHB read requests.
5	ahb2pcie_base1_reserved	**reserved**
4:0	ahb2pcie_base1_size	**This field specifies the window1 size.** Possible values are 7 to 31 which mean 2^7 to 2^31 bytes. Leaving this field to 0 causes window1 to be disabled.

1A145444 AHB2PCIE_BASE1_H AHB slave to PCIe translation table1 MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ahb2pcie_base1_h															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ahb2pcie_base1_h**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ahb2pcie_base1_h	**Translated window1 PCIe base address[63:32].** If 32-bit addreessing is used or no-prefetch bit is set then ahb2pcie_base1_h must be 32'h0.

1A145448 PCIE2AXI_WIN0 PCIe to AXI window0 control register E00000D4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**pcie2axi_win0_dest**															
Type	RW															
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**pcie2axi_win0_dest**								**pcie2axi_win0_enable**	**pcie2axi_win0_noprefetch**	**pcie2axi_win0_size**					
Type	RW								RW	RW	RW					
Reset	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0

Bit(s)	Name	Description
31:8	pcie2axi_win0_dest	**Translated AXI base address [35:12]**
7	pcie2axi_win0_enable	**Enable bit is used to control whether bridge reponds to PCI requests targeting PCI-AXI window.** When not set than all PCI requests in window are treated as "unsupported request".

Bit(s)	Name	Description
6	pcie2axi_wino_noprefetch	**No-prefetch bit causes window to be mapped in PCI non-prefetchable memory space when set.** When it is not set then window is mapped in PCI prefetchable memory space.
5:0	pcie2axi_wino_size	**This field specifies the size of windowo.** Possible values are 12 to 36 which mean 2^12 to 2^36 bytes. Leaving this field to 0 causes windowo to be disabled.

1A14544C PCIE2AXI_WIN1 PCIe to AXI window1 control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pcie2axi_win1_dest															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie2axi_win1_dest								pcie2axi_win1_enable	pcie2axi_win1_noprefetch	pcie2axi_win1_size					
Type	RW								RW	RW	RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	pcie2axi_win1_dest	**Translated AXI base address [35:12]**
7	pcie2axi_win1_enable	**Enable bit is used to control whether bridge reponds to PCI requests targeting PCI-AXI window.** When not set than all PCI requests in window are treated as "unsupported request".
6	pcie2axi_win1_noprefetch	**No-prefetch bit causes window to be mapped in PCI non-prefetchable memory space when set.** When it is not set then window is mapped in PCI prefetchable memory space.
5:0	pcie2axi_win1_size	**This field specifies the size of window1.**

Bit(s)	Name	Description
		Possible values are 12 to 36 which mean 2^12 to 2^36 bytes. Leaving this field to 0 causes window1 to be disabled.

1A145450 PCIE2AXI_WIN2 PCIe to AXI window2 control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pcie2axi_win2_dest															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie2axi_win2_dest								pcie2axi_win2_enable	pcie2axi_win2_noprefetch		pcie2axi_win2				
Type	RW								RW	RW		RW				
Reset	0	0	0	0					0	0		0	0	0	0	0

Bit(s)	Name	Description
31:12	pcie2axi_win2_dest	**Translated AXI base address [31:12]**
7	pcie2axi_win2_enable	**Enable bit is used to control whether bridge reponds to PCI requests targeting PCI-AXI window.** When not set than all PCI requests in window are treated as "unsupported request".
6	pcie2axi_win2_noprefetch	**No-prefetch bit causes window to be mapped in PCI non-prefetchable memory space when set.** When it is not set then window is mapped in PCI prefetchable memory space.
4:0	pcie2axi_win2	**This field specifies the size of window2.** Possible values are 12 to 31 which mean 2^12 to 2^31 bytes. Leaving this field to 0 causes window2 to be disabled.

1A145454 PCIE2AXI_WIN3 PCIe to AXI window3 control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pcie2axi_win3_dest															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie2axi_win3_dest								pcie2axi_win3_enable	pcie2axi_win3_noprefetch		pcie2axi_win3				
Type	RW								RW	RW		RW				
Reset	0	0	0	0					0	0		0	0	0	0	0

Bit(s)	Name	Description
31:12	pcie2axi_win3_dest	**Translated AXI base address [31:12]**
7	pcie2axi_win3_enable	**Enable bit is used to control whether bridge reponds to PCI requests targeting PCI-AXI window.** When not set than all PCI requests in window are treated as "unsupported request".
6	pcie2axi_win3_noprefetch	**No-prefetch bit causes window to be mapped in PCI non-prefetchable memory space when set.** When it is not set then window is mapped in PCI prefetchable memory space.
4:0	pcie2axi_win3	**This field specifies the size of window3.** Possible values are 12 to 31 which mean 2^12 to 2^31 bytes. Leaving this field to 0 causes window3 to be disabled.

1A145458 PCIE2AXI_WIN4 PCIe to AXI window4 control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pcie2axi_win4_dest															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie2axi_win4_dest								pcie2axi_win4_enable	pcie2axi_win4_noprefetch		pcie2axi_win4				
Type	RW								RW	RW		RW				
Reset	0	0	0	0					0	0		0	0	0	0	0

Bit(s)	Name	Description
31:12	pcie2axi_win4_dest	**Translated AXI base address [31:12]**
7	pcie2axi_win4_enable	**Enable bit is used to control whether bridge reponds to PCI requests targeting PCI-AXI window.** When not set than all PCI requests in window are treated as "unsupported request".
6	pcie2axi_win4_noprefetch	**No-prefetch bit causes window to be mapped in PCI non-prefetchable memory space when set.** When it is not set then window is mapped in PCI prefetchable memory space.
4:0	pcie2axi_win4	**This field specifies the size of window4.** Possible values are 12 to 31 which mean 2^12 to 2^31 bytes. Leaving this field to 0 causes window0 to be disabled.

1A14545C PCIE2AXI_WIN5 PCIe to AXI window4 control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pcie2axi_win5_dest															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie2axi_win5_dest								pcie2axi_win	pcie2axi_win		pcie2axi_win5				

									5_enable	5_noprefetch						
Type	RW								RW	RW		RW				
Reset	0	0	0	0					0	0		0	0	0	0	0

Bit(s)	Name	Description
31:12	pcie2axi_win5_dest	**Translated AXI base address [31:12]**
7	pcie2axi_win5_enable	**Enable bit is used to control whether bridge reponds to PCI requests targeting PCI-AXI window.** When not set than all PCI requests in window are treated as "unsupported request".
6	pcie2axi_win5_noprefetch	**No-prefetch bit causes window to be mapped in PCI non-prefetchable memory space when set.** When it is not set then window is mapped in PCI prefetchable memory space.
4:0	pcie2axi_win5	**This field specifies the size of window5.** Possible values are 12 to 31 which mean 2^12 to 2^31 bytes. Leaving this field to 0 causes window1 to be disabled.

1A145460 CFG_HEADER_0 CFG request TLP header DW0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**app_cfg_fmt**			**app_cfg_type**						**app_cfg_tc**						
Type	RW			RW						RW						
Reset	0	0	0	0	0	0	0	0		0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**app_cfg_id**	**app_cfg_ep**	**app_cfg_attr**				**app_cfg_length**									
Type	RW	RW	RW				RW									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:29	app_cfg_fmt	**Format field in Configuration Request TLP.**
28:24	app_cfg_type	**Type field in Configuration Request TLP.**
22:20	app_cfg_tc	**TC field in Configuration Request TLP.**
15	app_cfg_td	**TD field in Configuration Request TLP.**
14	app_cfg_ep	**EP field in Configuration Request TLP.**
13:12	app_cfg_attr	**Attr field in Configuration Request TLP.**
9:0	app_cfg_length	**Length field in Configuration Request TLP.**

1A145464 CFG_HEADER_1 CFG request TLP header DW1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	app_cfg_rid															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	app_cfg_tag								app_cfg_lbe				app_cfg_fbe			
Type	RW								RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	app_cfg_rid	**Requester ID field in Configuration Request TLP.**
15:8	app_cfg_tag	**Tag field in Configuration Request TLP.**
7:4	app_cfg_lbe	**Last DW BE field in Configuration Request TLP.**
3:0	app_cfg_fbe	**First DW BE field in Configuration Request TLP.**

1A145468 CFG_HEADER_2 CFG request TLP header DW2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	app_cfg_bus								app_cfg_dev					app_cfg_fun		
Type	RW								RW					RW		

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					app_cfg_ext_regnum				app_cfg_regnum							
Type					RW				RW							
Reset					0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:24	app_cfg_bus	**Bus Number field in Configuration Request TLP.**
23:19	app_cfg_dev	**Device Number field in Configuration Request TLP.**
18:16	app_cfg_fun	**Function Number field in Configuration Request TLP.**
11:8	app_cfg_ext_regnum	**Ext. Register Number field in Configuration Request TLP.**
7:2	app_cfg_regnum	**Register Number field in Configuration Request TLP.**

1A14546C CFG_HEADER_3 CFG request TLP header DW3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									app_cfg_desc3							
Type									RW							
Reset									0	0	0	0	0	0		

Bit(s)	Name	Description
7:2	app_cfg_desc3	**app_cfg_desc3**

1A145470 CFG_WDATA CfgWr request TLP data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	app_cfg_wdata															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**app_cfg_wdata**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	app_cfg_wdata	**For CfgWr, this field specifies application layer prepared CFG request data and triggered by APP_TLP_REQ.app_cfg_req.**

1A145474 MSG_HEADER_0 MSG request TLP header DW0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**app_msg_fmt**			**app_msg_type**						**app_msg_tc**						
Type	RW			RW						RW						
Reset	0	0	0	0	0	0	0	0		0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**app_msg_td**	**app_msg_ep**	**app_msg_attr**				**app_msg_length**									
Type	RW	RW	RW				RW									
Reset	0	0	0	0			0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:29	app_msg_fmt	**Format field in Message TLP.**
28:24	app_msg_type	**Type field in Message TLP.**
22:20	app_msg_tc	**TC field in Message TLP.**
15	app_msg_td	**TD field in Message TLP.**
14	app_msg_ep	**EP field in Message TLP.**
13:12	app_msg_attr	**Attr field in Message TLP.**
9:0	app_msg_length	**Length field in Message TLP.**

Bit(s)	Name	Description

1A145478 MSG_HEADER_1 MSG request TLP header DW1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	app_msg_rid															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	app_msg_tag								app_msg_code							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	app_msg_rid	**Requester ID field in Message TLP.**
15:8	app_msg_tag	**Tag field in Message TLP.**
7:0	app_msg_code	**Message Code field in Message TLP.**

1A14547C MSG_HEADER_2 MSG request TLP header DW2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	app_msg_addr_o															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	app_msg_addr_o															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	app_msg_addr_o	**Application layer prepared MSG request header DW2.**

Bit(s)	Name	Description
		Triggered by APP_TLP_REQ.app_msg_req.

1A145480 MSG_HEADER_3 MSG request TLP header DW3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	app_msg_addr_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	app_msg_addr_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	app_msg_addr_1	**Application layer prepared MSG request header DW3.** Triggered by APP_TLP_REQ.app_msg_req.

1A145484 MSG_DATA MSG request TLP data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	app_msg_data															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	app_msg_data															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	app_msg_data	**Application layer prepared MSG request data.**

Bit(s)	Name	Description
		Triggered by APP_TLP_REQ.app_msg_req.

1A145488 APP_TLP_REQ APP request TLP start command 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved1								app_cpl_status			reservedo			app_msg_req	app_cfg_req
Type	RO								RO			RO			RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	reserved1	**Reserved**
7:5	app_cpl_status	**Completion Status of PIO.** - 000: Success - 001: UR - 010: CRS - 100: CA - 111: Completion Timeout Others are reserved.
4:2	reservedo	**Reserved**
1	app_msg_req	**Application initiated MSG TLP start command.** MSG_HEADER and MSG_DATA must be ready before setting app_msg_req. When Msg/MsgD TLP is triggerd by application layer, this bit will keep asserting until Msg TLP is transmitted.
0	app_cfg_req	**Application initiated CGG TLP start command.**

Bit(s)	Name	Description
		CFG_HEADER and CFG_WDATA must be ready before setting app_cfg_req. When Cfg TLP is triggerd by application layer, this bit will keep asserting until Cpl/CplD is received.

1A14548C CFG_RDATA Returned CfgRd request CplD data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cfg_rdata															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cfg_rdata															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	cfg_rdata	**This field specifies the received CplD for CfgRd when app_cfg_status deasserted**

1A145490 CFG_BAR0 BAR0 content in configuration space 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cfg_baro															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cfg_baro															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
31:0	cfg_bar0	**BAR0 content in configuration space offset 0x10h**

1A145494 CFG_BAR1 BAR1 content in configuration space 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cfg_bar1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cfg_bar1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	cfg_bar1	**BAR1 content in configuration space offset 0x14h**

1A145498 CFG_BAR2 BAR2 content in configuration space 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cfg_bar2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cfg_bar2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	cfg_bar2	**BAR2 content in configuration space offset 0x18h**

1A14549C CFG_BAR3 BAR3 content in configuration space 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cfg_bar3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cfg_bar3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	cfg_bar3	**BAR3 content in configuration space offset 0x1Ch**

1A1454A0 CFG_BAR4 BAR4 content in configuration space 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cfg_bar4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cfg_bar4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	cfg_bar4	**BAR4 content in configuration space offset 0x20h**

1A1454A4 CFG_BAR5 BAR5 content in configuration space 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cfg_bar5															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cfg_bar5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	cfg_bar5	**BAR5 content in configuration space offset 0x24h**

1A1454AC LTR_LATENCY_VALUE LTR max snoop and no-snoop latency Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				max_no_snoop_latency_scale			max_no_snoop_latency_value									
Type				RO			RO									
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				max_snoop_latency_scale			max_snoop_latency_value									
Type				RO			RO									
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:26	max_no_snoop_latency_scale	**L1 exit latency in separated clock mode**
25:16	max_no_snoop_latency_value	**Endpoint L1 acceptable latency**
12:10	max_snoop_latency_scale	**Endpoint L0s acceptable latency**
9:0	max_snoop_latency_value	**BAR5 content in configuration space offset 0x24h**

1A1454B0 MSI_MISC MSI control and status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																msi_inter

																rupt
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	msi_bdf															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	msi_interrupt	**1: MSI interrupt status from dma done** 0: original interrupt structure RC mode only
15:0	msi_bdf	**Bus#, Device#, Function# of EP send MSI to RC** RC mode only

1A1454D0 AHB_DISCARD_TIMER AHB discard timer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AHB_DISCARD_TIMER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AHB_DISCARD_TIMER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AHB_DISCARD_TIMER	**A timeout value to discard AHB read transaction and release pending HREADY.** HCLK clock cycle unit. 0 means no time-out will be applied.

Bit(s)	Name	Description

1A1454D8 ASPM_CONF Active State power management configuration ASPM_CONF register contains information for PCI Express native power management. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IDLE_TO_LoS_L1			L1_SUPPORT	L1_EXIT_COMMON_CK_LATENCY			L1_EXIT_SEPARATE_CK_LATENCY			L1_ACCEPT_LATENCY			LoS_ACCEPT_LATENCY		
Type	RW			RW	RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMMON_CK_FTS								SEPARATE_CK_FTS							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:29	IDLE_TO_LoS_L1	**Idle time to enter Los/L1**
28	L1_SUPPORT	**Enable L1 support**
27:25	L1_EXIT_COMMON_CK_LATENCY	**L1 exit latency in common clock mode**
24:22	L1_EXIT_SEPARATE_CK_LATENCY	**L1 exit latency in separated clock mode**
21:19	L1_ACCEPT_LATENCY	**Endpoint L1 acceptable latency**
18:16	LoS_ACCEPT_LATENCY	**Endpoint Los acceptable latency**
15:8	COMMON_CK_FTS	**Number of FTS in common clock mode at 2.5 Gbps (5 to 255)**
7:0	SEPARATE_CK_FTS	**Number of FTS in separated clock mode at 2.5 Gbps (5 to 255)**
		Analysis: - k_aspm[31:0] all covered by k_conf_func

1A1454DC PM_STATUS PCI legacy power management status This is used in Endpoint mode only 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**PM_STATUS**		
Type														RU		
Reset														0	0	0

Bit(s)	Name	Description
2:0	PM_STATUS	**This register specifies the PCI Legacy Power Management state (00=D0, 01=D1, 10=D2 or 11=D3hot or D3cold). Note that change of power management state is reported by an interrupt in ISTATUS register.**

1A1454E0 PM_CONF_0 PCI legacy power management configuration This is used in Endpoint mode only PM_CONF register contains information for PCI power management capabilities register and local processor must initialize it at power-up. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DATA_SCALE**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PM_CAP**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DATA_SCALE	**Data scale at index 7 to 0**

Bit(s)	Name	Description
15:0	PM_CAP	**PM Capabilities** Analysis: - k_pm[15:0] covered by k_conf_func

1A1454E4 PM_CONF_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA_INDEX_3								DATA_INDEX_2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_INDEX_1								DATA_INDEX_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DATA_INDEX_3	**Data at index 3**
23:16	DATA_INDEX_2	**Data at index 2**
15:8	DATA_INDEX_1	**Data at index 1**
7:0	DATA_INDEX_0	**Data at index 0**

1A1454E8 PM_CONF_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA_INDEX_7								DATA_INDEX_6							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_INDEX_5								DATA_INDEX_4							
Type	RW								RW							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DATA_INDEX_7	**Data at index 7**
23:16	DATA_INDEX_6	**Data at index 6**
15:8	DATA_INDEX_5	**Data at index 5**
7:0	DATA_INDEX_4	**Data at index 4**

1A1454EC PCI_SLOTCAP PCI Express slot capabilities 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PCI_SLOTCAP**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PCI_SLOTCAP**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PCI_SLOTCAP	**PCI Express slot capabilities** Analysis: - k_slot[31:0] all covered by k_conf_func

1A1454F0 PCI_DV PCI device and vendor ID. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**DEVICE_ID**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	VENDOR_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DEVICE_ID	**This register specifies the value of the PCI Device ID register, located at offset 00h in the PCI Configuration Space** Analysis: - k_pciid[95:0] all covered by k_conf_func
15:0	VENDOR_ID	**This register specifies the value of the PCI Vendor ID register, located at offset 00h in the PCI Configuration Space** Analysis: - k_pciid[95:0] all covered by k_conf_func

1A1454F4 PCI_SUB PCI subsystem device and vendor ID 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SUBSYSTEM_DEVICE_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SUBSYSTEM_VENDOR_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SUBSYSTEM_DEVICE_ID	**This register specifies the value of the PCI Subsystem Device ID register, located at offset 2Ch in the PCI Configuration Space** Analysis: - k_pciid[95:0] all covered by k_conf_func

Bit(s)	Name	Description
15:0	SUBSYSTEM_VENDOR_ID	**This register specifies the value of the PCI Subsystem Vendor ID register, located at offset 2Ch in the PCI Configuration Space** Analysis: - k_pciid[95:0] all covered by k_conf_func

1A1454F8 PCI_CREV PCI class code and revision ID 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLASS_CODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLASS_CODE								REVISION_ID							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	CLASS_CODE	**This register specifies the value of the PCI Class Code register, located at offset 08h in the PCI Configuration Space** Analysis: - k_pciid[95:0] all covered by k_conf_func
7:0	REVISION_ID	**This register specifies the value of the PCI Revision ID register, located at offset 08h in the PCI Configuration Space** Analysis: - k_pciid[95:0] all covered by k_conf_func

1A1454FC PCI_SLOTCSR PCI Express slot control and status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCI_SLOTCSR															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCI_SLOTCSR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PCI_SLOTCSR	**PCI_SLOTCSR specifies the value of the PCI Express Slot Control & Status register located at offset 98h in the PCI Configuration Space.** Reflect the value of pex18.

1A145500 PCI_PRMCSR PCI primary command and status register 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCI_PRMCSR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCI_PRMCSR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PCI_PRMCSR	**PCI_PRMCSR specifies the value of the PCI Command & Status register located at offset 04h in the PCI Configuration Space.** Reflect the value of sc_reg.

1A145504 PCI_DEVCSR PCI Express device control and status register 00002810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCI_DEVCSR															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCI_DEVCSR															
Type	RU															
Reset	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	PCI_DEVCSR	**PCI_DEVCSR specifies the value of the PCI Express Device Control & Status register located at offset 88h in the PCI Configuration Space.** Reflect the value of pex08.

1A145508 PCI_LINKCSR PCI Express link control and status register 10000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCI_LINKCSR															
Type	RU															
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCI_LINKCSR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:0	PCI_LINKCSR	**PCI_LINKCSR specifies the value of the PCI Express Link Control & Status register located at offset 90h in the PCI Configuration Space.** Reflect the value of pex10.

1A14550C PCI_ROOTCSR PCI Express root status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PCI_ROOTCSR															
Type	RU															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCI_ROOTCSR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PCI_ROOTCSR	**PCI_ROOTCSR specifies the value of the PCI Express Root Control & Status register located at offset 9Ch and ACh in the PCI Configuration Space.** Reflect the value of {pex20[23:0], pex1C[7:0]}.

1A145510 PCI_RSTCR PCI Express IP reset control register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PCI_CONF_RST_OUT_EN	PCI_MAC_RST_OUT_EN	PCI_PIPE_RST_OUT_EN					PCI_PERSTB	PCI_PERSTB_CONFIG_ENABLE	PCI_PERSTB_MAC_ENABLE	PCI_PERSTB_PIPE_ENABLE	PCI_PERSTB_PHY_ENABLE	PCI_CRSTB	PCI_MAC_SRSTB	PCI_PIPE_SRSTB	PCI_PHY_RSTB
Type	RW	RW	RW					RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0					0	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
15	PCI_CONF_RST_OUT_EN	**If PCIe MAC will reset configration space register when LTSSM exit disable/ L2/ Hot reset or Link state from LINK_UP to LINK_DOWN.** 0 : Disable reset.

Bit(s)	Name	Description
		1 : Enable reset.
14	PCI_MAC_RST_OUT_EN	**If PCIe MAC will reset register of mac clock domain when LTSSM exit disable/ L2/ Hot reset or Link state from LINK_UP to LINK_DOWN.** 0 : Disable reset. 1 : Enable reset.
13	PCI_PIPE_RST_OUT_EN	**If PCIe MAC will reset register of pipe clock domain when LTSSM exit disable/ L2/ Hot reset or Link state from LINK_UP to LINK_DOWN.** 0 : Disable reset. 1 : Enable reset.
8	PCI_PERSTB	**For RC only, SW control PERST#.** 0 : PERST# is low. 1 : PERST# is high.
7	PCI_PERSTB_CONF_ENABLE	**PERSTB to reset MAC configuration space domain** 0 : disable 1 : enable
6	PCI_PERSTB_MAC_ENABLE	**PERSTB to reset MAC USER clock domain** 0 : disable 1 : enable
5	PCI_PERSTB_PIPE_ENABLE	**PERSTB to reset MAC PIPE clock domain** 0 : disable 1 : enable
4	PCI_PERSTB_PHY_ENABLE	**PERSTB to reset PHY** 0 : disable 1 : enable
3	PCI_CRSTB	**SW Configuration Reset.** Active low
2	PCI_MAC_SRSTB	**PCIe MAC USER clock Software Reset.** Active low.
1	PCI_PIPE_SRSTB	**PCIe MAC PIPE Clock Software Reset.** Active low.

Bit(s)	Name	Description
0	PCI_PHY_RSTB	**PCIe PHY Software Reset.** Active low.

1A145514 PCI_MAC_HW_VERSION PCI Express MAC HW Version 20150730

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_hw_version															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_hw_version															
Type	RO															
Reset	0	0	0	0	0	1	1	1	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
31:0	reg_hw_version	**PCI Express MAC HW Version** EX : yyyy_mmdd

1A145518 REG_DBG_MOD_SEL PCI Express Debugging Module Select FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBG_MOD_SEL3								DBG_MOD_SEL2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_MOD_SEL1								DBG_MOD_SEL0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	DBG_MOD_SEL3	**- 0: pe2_mac_top.pe2_mac_dbg_out[31:24] reflects TRANS debugging probes** - 1: pe2_mac_top.pe2_mac_dbg_out[31:24] reflects DLL debugging probes - 2: pe2_mac_top.pe2_mac_dbg_out[31:24] reflects CONF debugging probes - 3: pe2_mac_top.pe2_mac_dbg_out[31:24] reflects MAC debugging probes - 4: pe2_mac_top.pe2_mac_dbg_out[31:24] reflects Bridge debugging probes - f: pe2_mac_top.pe2_mac_dbg_out[31:24] reflects SW_PRB_OUT (0x05f8) - ff : disable debug mux
23:16	DBG_MOD_SEL2	**- 0: pe2_mac_top.pe2_mac_dbg_out[23:16] reflects TRANS debugging probes** - 1: pe2_mac_top.pe2_mac_dbg_out[23:16] reflects DLL debugging probes - 2: pe2_mac_top.pe2_mac_dbg_out[23:16] reflects CONF debugging probes - 3: pe2_mac_top.pe2_mac_dbg_out[23:16] reflects MAC debugging probes - 4: pe2_mac_top.pe2_mac_dbg_out[23:16] reflects Bridge debugging probes - f: pe2_mac_top.pe2_mac_dbg_out[23:16] reflects SW_PRB_OUT (0x05f8) - ff : disable debug mux
15:8	DBG_MOD_SEL1	**- 0: pe2_mac_top.pe2_mac_dbg_out[15:8] reflects TRANS debugging probes** - 1: pe2_mac_top.pe2_mac_dbg_out[15:8] reflects DLL debugging probes - 2: pe2_mac_top.pe2_mac_dbg_out[15:8] reflects CONF debugging probes - 3: pe2_mac_top.pe2_mac_dbg_out[15:8] reflects MAC debugging probes - 4: pe2_mac_top.pe2_mac_dbg_out[15:8] reflects Bridge debugging probes - f: pe2_mac_top.pe2_mac_dbg_out[15:8] reflects SW_PRB_OUT (0x05f8) - ff : disable debug mux

Bit(s)	Name	Description
7:0	DBG_MOD_SEL0	**- 0: pe2_mac_top.pe2_mac_dbg_out[7:0] reflects TRANS debugging probes** - 1: pe2_mac_top.pe2_mac_dbg_out[7:0] reflects DLL debugging probes - 2: pe2_mac_top.pe2_mac_dbg_out[7:0] reflects CONF debugging probes - 3: pe2_mac_top.pe2_mac_dbg_out[7:0] reflects MAC debugging probes - 4: pe2_mac_top.pe2_mac_dbg_out[7:0] reflects Bridge debugging probes - f: pe2_mac_top.pe2_mac_dbg_out[7:0] reflects SW_PRB_OUT (0x05f8) - ff : disable debug mux

1A14551C REG_DBG_PORT_SEL PCI Express Debugging Port Select 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBG_PORT_SEL3								DBG_PORT_SEL2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_PORT_SEL1								DBG_PORT_SEL0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DBG_PORT_SEL3	**debugging port selection of pe2_mac_top.pe2_mac_dbg_out[31:24]**
23:16	DBG_PORT_SEL2	**debugging port selection of pe2_mac_top.pe2_mac_dbg_out[23:16]**
15:8	DBG_PORT_SEL1	**debugging port selection of pe2_mac_top.pe2_mac_dbg_out[15:8]**
7:0	DBG_PORT_SEL0	**debugging port selection of pe2_mac_top.pe2_mac_dbg_out[7:0]**

1A145520 REG_OBFF_0 OBFF Control Register 0 00000364

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**csr_obff_state**		**csr_obff_waken_edge_1us_ticks**							
Type							RW		RW							
Reset							1	1	0	1	1	0	0	1	0	0

Bit(s)	Name	Description
9:8	csr_obff_state	**OBFF state, RW type in RC mode. RO type in EP mode** 00=cpu active, 01=obff, 10=idle, 11=reseeved.
7:0	csr_obff_waken_edge_1us_ticks	**EP mode : Ticks for 1us based on OBFF clock.** RC mode : Ticks for 1us based on U_CLK clock.

1A145524 REG_OBFF_1 OBFF Control Register 1 100F0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**csr_obff_expire_timer**								**csr_obff_trigger_mode**			**csr_obff_reqid_cmp_en**	**csr_obff_state_en**			
Type	RW								RW			RW	RW			
Reset	0	0	0	1	0	0	0	0	0	0		0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**csr_clinento_remote_req_id**															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	csr_obff_expire_timer	**EP mode only, 0~255 timer scale unit, 8 ticks per scale unit if trigger mode is 10. Based on OBFF clock**
23:22	csr_obff_trigger_mode	**incoming packet trigger mode in obff mode or in idle mode.** 00 : no trigger mode, ltach PCIe immediately when pacjet incoming. 01 : FCE queue level mode. 10 : Timer expired mode. 11 : Reserved
20	csr_obff_reqid_cmp_en	**Expected reuest id comparator enable**
19:16	csr_obff_state_en	**csr_obff_state_en[0]:obff_state_idle enable** csr_obff_state_en[1]:obff_state_obff dma enable csr_obff_state_en[2]:obff_state_obff intr enable csr_obff_state_en[3]:obff_state_cpu_act enable
15:0	csr_clinento_remote_req_id	**Expected reuest id from RC**

1A145528 REG_PHYMAC_CONF PHYMAC Control Register 00110002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						**rec_rxcfg_txts2_num**										
Type						RW										
Reset						0	0	0	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**rx_eios_filter_en**	**rxlos_fts_filter_en**
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
26:16	rec_rxcfg_txts2_num	**Adjustable number of tx TS2 when ltssm is in recvoery.rxcfg**
1	rx_eios_filter_en	**Enable the filter of garbage data after receiving EIOS**
0	rxlos_fts_filter_en	**Enable the filter of FTS from PIPE. Avoid from receiving bad FTS from PHY.**

1A14552C REG_WAKE_CONTROL Wake_n or Clkreq_n Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**rg_rc_l2_clkreq_out**	**rg_rc_drive_clkreq_dis**							**rg_wake_n_enable**	**rg_clkreq_n_enable**
Type							RW	RW							RW	RW
Reset							0	0							0	0

Bit(s)	Name	Description
9	rg_rc_l2_clkreq_out	**The register is for RC and only useful for "rg_rc_drive_clkreq_dis" is 0** 0 : RC will dirve clkreq_n to 0 in L2. (100MHz is enable) 1 : RC will dirve clkreq_n to 1 in L2.. (100MHz is disable)
8	rg_rc_drive_clkreq_dis	**The register is for RC.** If EP support clock power management - CLKPM, it means EP can drive clkreq_n, then SW can set the register to 1'b1. 0 : RC will control clkreq_n

Bit(s)	Name	Description
		1 : RC won't control clkreq_n except for L1SS is enabled. (In normal mode, EP can control clkreq_n)
1	rg_wake_n_enable	**The register can be used to request DUT as EP to exit L2 state.** EP : L2 - 0: WAKE# output disable, this means WAKE# will be external pull-high - 1: WAKE# output enable, this means WAKE# output low to wakeup from L2
0	rg_clkreq_n_enable	**The reigster can be used to request DUT to exit power mode.** RC : L1 with reference clock disabled. L1SS. L2. EP : L1 with reference clock disabled. L1SS. 0: disable SW activate clkreqn 1: SW activate clkreqn to enable reference clock reqeust

1A145530 REG_WCH_WEIGHT_0 Write channel WRR weighting control register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	wch7_weight				wch6_weight				wch5_weight				wch4_wight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wch3_weight				wch2_weight				wch1_weight				wch0_weight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	wch7_weight	**Arbitration weighting of write DMA channel 7 for MWr TLPs.** Similar to wch0_weight.
27:24	wch6_weight	**Arbitration weighting of write DMA channel 6 for MWr TLPs.** Similar to wch0_weight.
23:20	wch5_weight	**Arbitration weighting of write DMA channel 5 for MWr TLPs.** Similar to wch0_weight.
19:16	wch4_wight	**Arbitration weighting of write DMA channel 4 for MWr TLPs.** Similar to wch0_weight.
15:12	wch3_weight	**Arbitration weighting of write DMA channel 3 for MWr TLPs.** Similar to wch0_weight.
11:8	wch2_weight	**Arbitration weighting of write DMA channel 2 for MWr TLPs.** Similar to wch0_weight.
7:4	wch1_weight	**Arbitration weighting of write DMA channel 1 for MWr TLPs.** Similar to wch0_weight.
3:0	wch0_weight	**Arbitration weighting of write DMA channel 0 for MWr TLPs.** - 0: weighting = 1 - 1: weighting = 2 - 2: weighting = 3 - 3: weighting = 4 - 4: weighting = 5 - 5: weighting = 6 - 6: weighting = 7 - 7: weighting = 8 - 8: weighting = 9 - 9: weighting = 10 - 10: weighting = 11

Bit(s)	Name	Description
		- 11: weighting = 12 - 12: weighting = 13 - 14: weighting = 14 - 15: weighting = 16

1A145534 REG_WCH_WEIGHT_1 Write channel WRR weighting control register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	wch15_weight				wch14_weight				wch13_weight				wch12_wight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wch11_weight				wch10_weight				wch9_weight				wch8_weight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	wch15_weight	**Arbitration weighting of write DMA channel 15 for MWr TLPs.** Similar to wch0_weight.
27:24	wch14_weight	**Arbitration weighting of write DMA channel 14 for MWr TLPs.** Similar to wch0_weight.
23:20	wch13_weight	**Arbitration weighting of write DMA channel 13 for MWr TLPs.** Similar to wch0_weight.
19:16	wch12_wight	**Arbitration weighting of write DMA channel 12 for MWr TLPs.** Similar to wch0_weight.
15:12	wch11_weight	**Arbitration weighting of write DMA channel 11 for MWr TLPs.** Similar to wch0_weight.

Bit(s)	Name	Description
11:8	wch10_weight	**Arbitration weighting of write DMA channel 10 for MWr TLPs.** Similar to wch0_weight.
7:4	wch9_weight	**Arbitration weighting of write DMA channel 9 for MWr TLPs.** Similar to wch0_weight.
3:0	wch8_weight	**Arbitration weighting of write DMA channel 8 for MWr TLPs.** Similar to wch0_weight.

1A145538 REG_RCH_WEIGHT_0 Read channel WRR weighting control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rch7_weight				rch6_weight				rch5_weight				rch4_wight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rch3_weight				rch2_weight				rch1_weight				rch0_weight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	rch7_weight	**Arbitration weighting of read DMA channel 7 for MRd TLPs.** Similar to rch0_weight.
27:24	rch6_weight	**Arbitration weighting of read DMA channel 6 for MRd TLPs.** Similar to rch0_weight.
23:20	rch5_weight	**Arbitration weighting of read DMA channel 5 for MRd TLPs.** Similar to rch0_weight.
19:16	rch4_wight	**Arbitration weighting of read DMA channel 4 for MRd TLPs.**

Bit(s)	Name	Description
		Similar to rch0_weight.
15:12	rch3_weight	**Arbitration weighting of read DMA channel 3 for MRd TLPs.** Similar to rch0_weight.
11:8	rch2_weight	**Arbitration weighting of read DMA channel 2 for MRd TLPs.** Similar to rch0_weight.
7:4	rch1_weight	**Arbitration weighting of read DMA channel 1 for MRd TLPs.** Similar to rch0_weight.
3:0	rch0_weight	**Arbitration weighting of read DMA channel 0 for MRd TLPs.** - 0: weighting = 1 - 1: weighting = 2 - 2: weighting = 3 - 3: weighting = 4 - 4: weighting = 5 - 5: weighting = 6 - 6: weighting = 7 - 7: weighting = 8 - 8: weighting = 9 - 9: weighting = 10 - 10: weighting = 11 - 11: weighting = 12 - 12: weighting = 13 - 14: weighting = 14 - 15: weighting = 16

1A14553C REG_RCH_WEIGHT_1 Read channel WRR weighting control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	rch15_weight				rch14_weight				rch13_weight				rch12_wight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rch11_weight				rch10_weight				rch9_weight				rch8_weight			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	rch15_weight	**Arbitration weighting of read DMA channel 15 for MRd TLPs.** Similar to rch0_weight.
27:24	rch14_weight	**Arbitration weighting of read DMA channel 14 for MRd TLPs.** Similar to rch0_weight.
23:20	rch13_weight	**Arbitration weighting of read DMA channel 13 for MRd TLPs.** Similar to rch0_weight.
19:16	rch12_wight	**Arbitration weighting of read DMA channel 12 for MRd TLPs.** Similar to rch0_weight.
15:12	rch11_weight	**Arbitration weighting of read DMA channel 11 for MRd TLPs.** Similar to rch0_weight.
11:8	rch10_weight	**Arbitration weighting of read DMA channel 10 for MRd TLPs.** Similar to rch0_weight.
7:4	rch9_weight	**Arbitration weighting of read DMA channel 9 for MRd TLPs.** Similar to rch0_weight.
3:0	rch8_weight	**Arbitration weighting of read DMA channel 8 for MRd TLPs.** Similar to rch0_weight.

1A145540 REG_AXI_RD_MMIO_CTRL AXI RD MMIO DMA configuration register. 01800C08

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AXI_DMA_ID				AXI_DMA_BURST			AXI_DMA_CMD_Q_EN	AXI_DMA_OUTSTAND_NUM				AXI_DMA_COHERENCE	AXI_DMA_IOMMU	AXI_DMA_CACHEABLE	AXI_DMA_ULTRA_EN
Type	RW				RW			RW	RW				RW	RW	RW	RW
Reset	0	0	0	0	0	0		1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_DMA_ULTRA_NUM								AXI_DMA_PRE_ULTRA_NUM							
Type	RW								RW							
Reset	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	AXI_DMA_ID	**AXI ID** The register are only for AXI DMA.
27:26	AXI_DMA_BURST	**AXI burst length.** 00 : 128 byte 01 : 64 byte 10 : 32 byte 11 : 16 byte The register are only for AXI DMA.
24	AXI_DMA_CMD_Q_EN	**AXI will use command queue to record DMA command.** The register are only for AXI DMA.
23:20	AXI_DMA_OUTSTAND_NUM	**The max outstand request for AXI DMA** valid value : 1 ~ 4

Bit(s)	Name	Description
19	AXI_DMA_COHERENCE	The register are only for AXI DMA. **AXI coherence capability.** 0 : disalbe 1 : enable
18	AXI_DMA_IOMMU	The register are only for AXI DMA. **AXI iommu capability.** 0 : disalbe 1 : enable
17	AXI_DMA_CACHEABLE	The register are only for AXI DMA. **AXI cacheable capability.** 0 : disalbe 1 : enable
16	AXI_DMA_ULTRA_EN	The register are only for AXI DMA. **AXI RD channel ultra capability which is used to indicate async fifo in AXI DMA is almost empty.** 0 : disalbe 1 : enable
15:8	AXI_DMA_ULTRA_NUM	The register are only for AXI DMA. **The high threshold to assert ultra signal. The value can't be smaller than pre_ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert ultra.** valid : 0 ~ 31
7:0	AXI_DMA_PRE_ULTRA_NUM	The register are only for AXI DMA. **The low threshold to assert pre_ultra signal. The value can't be larger than ultra_num. When buffer data depth is**

Bit(s)	Name	Description
		more than the threshold, AXI DMA would assert pre_ultra. valid : 0 ~ 31 The register are only for AXI DMA.

1A145544 REG_AXI_WR_MMIO_CTRL AXI WR MMIO DMA configuration register. 01800C08

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AXI_DMA_ID				AXI_DMA_BURST			AXI_DMA_CMD_Q_EN	AXI_DMA_OUTSTAND_NUM				AXI_DMA_COHERENCE	AXI_DMA_IOMMU	AXI_DMA_CACHEABLE	AXI_DMA_ULTRA_EN
Type	RW				RW			RW	RW				RW	RW	RW	RW
Reset	0	0	0	0	0	0		1	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_DMA_ULTRA_NUM								AXI_DMA_PRE_ULTRA_NUM							
Type	RW								RW							
Reset	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	AXI_DMA_ID	**AXI ID** The register are only for AXI DMA.
27:26	AXI_DMA_BURST	**AXI burst length.** 00 : 128 byte 01 : 64 byte 10 : 32 byte 11 : 16 byte

Bit(s)	Name	Description
		The register are only for AXI DMA.
24	AXI_DMA_CMD_Q_EN	**AXI will use command queue to record DMA command.**
		The register are only for AXI DMA.
23:20	AXI_DMA_OUTSTAND_NUM	**The max outstand request for AXI DMA** valid value : 1 ~ 4
		The register are only for AXI DMA.
19	AXI_DMA_COHERENCE	**AXI coherence capability.** 0 : disalbe 1 : enable
		The register are only for AXI DMA.
18	AXI_DMA_IOMMU	**AXI iommu capability.** 0 : disalbe 1 : enable
		The register are only for AXI DMA.
17	AXI_DMA_CACHEABLE	**AXI cacheable capability.** 0 : disalbe 1 : enable
		The register are only for AXI DMA.
16	AXI_DMA_ULTRA_EN	**AXI RD channel ultra capability which is used to indicate async fifo in AXI DMA is almost empty.** 0 : disalbe 1 : enable
		The register are only for AXI DMA.

Bit(s)	Name	Description
15:8	AXI_DMA_ULTRA_NUM	**The high threshold to assert ultra signal. The value can't be smaller than pre_ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert ultra.** valid : 0 ~ 31 The register are only for AXI DMA.
7:0	AXI_DMA_PRE_ULTRA_NUM	**The low threshold to assert pre_ultra signal. The value can't be larger than ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert pre_ultra.** valid : 0 ~ 31 The register are only for AXI DMA.

1A145548 REG_AXI_RD_DMA_CTRL AXI RD DATA DMA configuration register. 00800C08

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AXI_DMA_ID				AXI_DMA_BURST				AXI_DMA_OUTSTAND_NUM				AXI_DMA_COHERENCE	AXI_DMA_IOMMU	AXI_DMA_CACHEABLE	AXI_DMA_ULTRA_EN
Type	RW				RW				RW				RW	RW	RW	RW
Reset	0	0	0	0	0	0			1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_DMA_ULTRA_NUM								AXI_DMA_PRE_ULTRA_NUM							
Type	RW								RW							
Reset	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	AXI_DMA_ID	**AXI ID**

Bit(s)	Name	Description
		The register are only for AXI DMA.
27:26	AXI_DMA_BURST	**AXI burst length.** 00 : 128 byte 01 : 64 byte 10 : 32 byte 11 : 16 byte
		The register are only for AXI DMA.
23:20	AXI_DMA_OUTSTAND_NUM	**The max outstand request for AXI DMA** valid value : 1 ~ 4
		The register are only for AXI DMA.
19	AXI_DMA_COHERENCE	**AXI coherence capability.** 0 : disalbe 1 : enable
		The register are only for AXI DMA.
18	AXI_DMA_IOMMU	**AXI iommu capability.** 0 : disalbe 1 : enable
		The register are only for AXI DMA.
17	AXI_DMA_CACHEABLE	**AXI cacheable capability.** 0 : disalbe 1 : enable
		The register are only for AXI DMA.
16	AXI_DMA_ULTRA_EN	**AXI RD channel ultra capability which is used to indicate async fifo in AXI DMA is almost empty.** 0 : disalbe

Bit(s)	Name	Description
		1 : enable The register are only for AXI DMA.
15:8	AXI_DMA_ULTRA_NUM	**The high threshold to assert ultra signal. The value can't be smaller than pre_ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert ultra.** valid : 0 ~ 31 The register are only for AXI DMA.
7:0	AXI_DMA_PRE_ULTRA_NUM	**The low threshold to assert pre_ultra signal. The value can't be larger than ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert pre_ultra.** valid : 0 ~ 31 The register are only for AXI DMA.

1A14554C REG_AXI_WR_DMA_CTRL AXI WR DATA DMA configuration register. 00800C08

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AXI_DMA_ID				AXI_DMA_BURST				AXI_DMA_OUTSTAND_NUM				AXI_DMA_COHERENCE	AXI_DMA_IOMMU	AXI_DMA_CACHEABLE	AXI_DMA_ULTRA_EN
Type	RW				RW				RW				RW	RW	RW	RW
Reset	0	0	0	0	0	0			1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_DMA_ULTRA_NUM								AXI_DMA_PRE_ULTRA_NUM							
Type	RW								RW							
Reset	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:28	AXI_DMA_ID	**AXI ID** The register are only for AXI DMA.
27:26	AXI_DMA_BURST	**AXI burst length.** 00 : 128 byte 01 : 64 byte 10 : 32 byte 11 : 16 byte The register are only for AXI DMA.
23:20	AXI_DMA_OUTSTAND_NUM	**The max outstand request for AXI DMA** valid value : 1 ~ 4 The register are only for AXI DMA.
19	AXI_DMA_COHERENCE	**AXI coherence capability.** 0 : disalbe 1 : enable The register are only for AXI DMA.
18	AXI_DMA_IOMMU	**AXI iommu capability.** 0 : disalbe 1 : enable The register are only for AXI DMA.
17	AXI_DMA_CACHEABLE	**AXI cacheable capability.** 0 : disalbe 1 : enable The register are only for AXI DMA.

Bit(s)	Name	Description
16	AXI_DMA_ULTRA_EN	**AXI RD channel ultra capability which is used to indicate async fifo in AXI DMA is almost empty.** 0 : disalbe 1 : enable The register are only for AXI DMA.
15:8	AXI_DMA_ULTRA_NUM	**The high threshold to assert ultra signal. The value can't be smaller than pre_ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert ultra.** valid : 0 ~ 31 The register are only for AXI DMA.
7:0	AXI_DMA_PRE_ULTRA_NUM	**The low threshold to assert pre_ultra signal. The value can't be larger than ultra_num. When buffer data depth is more than the threshold, AXI DMA would assert pre_ultra.** valid : 0 ~ 31 The register are only for AXI DMA.

1A145550 REG_DMA_CK_CTRL Data and MMIO DMA Clock Gate Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**reg_dma_bus_ck_gate_dis**	**reg_mmio_ck_gate_dis**
Type															RW	RW

Reset															0	0

Bit(s)	Name	Description
1	reg_dma_bus_ck_gate_dis	**0 : dma_bus_ck will be gated by PCIe IP internal CG if DATA DMA is not active.** 1 : dma_bus_ck will not be gated by PCIe IP internal CG if DATA DMA is not active.
0	reg_mmio_ck_gate_dis	**0 : mmio_ck will be gated by PCIe IP internal CG if mmio DMA is not active.** 1 : mmio_ck will not be gated by PCIe IP internal CG if mmio DMA is not active.

1A145554 REG_IP_SLEEP_CTRL PE2 IP SLEEP control 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**reg_l2_sleep_en**	**reg_l1p2_sleep_en**	**reg_l1p1_sleep_en**	**reg_l1_sleep_en**
Type													RW	RW	RW	RW
Reset													1	1	1	1

Bit(s)	Name	Description
3	reg_l2_sleep_en	**For PCIe L2.** For MPCIe L2. 0 : PCIe controller don't assert "pe2_ip_sleep" when LTSSM in L2 state. 1 : PCIe controller will assert "pe2_ip_sleep" when LTSSM in L2 state.
2	reg_l1p2_sleep_en	**For PCIe L1SS L1.2.**

Bit(s)	Name	Description
		For MPCIe L1 Deep Hibern8. 0 : PCIe controller don't assert "pe2_ip_sleep" when LTSSM in L1.2 state. 1 : PCIe controller will assert "pe2_ip_sleep" when LTSSM in L1.2 state.
1	reg_l1p1_sleep_en	**For PCIe L1SS L1.1.** 0 : PCIe controller don't assert "pe2_ip_sleep" when LTSSM in L1.1 state. 1 : PCIe controller will assert "pe2_ip_sleep" when LTSSM in L1.1 state.
0	reg_l1_sleep_en	**For PCIe L1PM.** For MPCIe L1. 0 : PCIe controller don't assert "pe2_ip_sleep" when LTSSM in L1 state. 1 : PCIe controller will assert "pe2_ip_sleep" when LTSSM in L1 state.

1A145560 REG_ASPM_L1_CTRL ASPM L1 Reject Timing Value 0000006D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**reg_rc_l1_reject_time**				**reg_ep_l1_reject_time**			
Type									RW				RW			
Reset									0	1	1	0	1	1	0	1

Bit(s)	Name	Description
7:4	reg_rc_l1_reject_time	**The register is for RC to counter the interval between last transmission of the PM_Active_State_Request_L1 DLLP**

Bit(s)	Name	Description
		and next transmission of the PM_Active_State_Request_L1 DLLP. Unit : 1us
3:0	reg_ep_l1_reject_time	**The register is for EP to counter the interval between last transmission of the PM_Active_State_Request_L1 DLLP and next transmission of the PM_Active_State_Request_L1 DLLP.** Unit : 1us

1A145564 REG_MMIO_CTRL MMIO Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**reg_mmio_rd_lock_en**	**reg_mmio_wr_lock_en**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	reg_mmio_rd_lock_en	**The register is for RC to block memory write TLP if memory read operation is active.** 0 : memory write will wait until memory read finished. 1 : memory write won't wait memory read.
0	reg_mmio_wr_lock_en	**The register is for RC to block memory read TLP if memory write operation is active.** 0 : memory read will wait until memory write finished. 1 : memory read won't wait memory write.

Bit(s)	Name	Description

1A145568 REG_LTR_LATENCY LTR Lattency Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rx_msg_ltr_no_snoop_lat															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_msg_ltr_snoop_lat															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	rx_msg_ltr_no_snoop_lat	**Extract No Snoop Latency value from received LTR message.**
15:0	rx_msg_ltr_snoop_lat	**Extract Snoop Latency value from received LTR message.**

1A145570 REG_MPCIE_EN MPCIE FUNCTION CONTROL 01000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							reg_mpcie_hsrate_ctrl									reg_w1c_mpcie_config
Type							RW									W1C
Reset							0	1								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								reg_mpcie_t2r_						reg_mpcie_stall_en	reg_mpcie_sw_ltss	reg_mpcie_func_en

								lpbk							**m_en**	
Type								RW						RW	RW	RW
Reset								0						0	0	0

Bit(s)	Name	Description
25:24	reg_mpcie_hsrate_ctrl	**For dynamic bandwidth change.** SW can set the register then set retrain bit of RC configuration space to change MPHY Rate. 2'b01 : Rate A. 2'b10 : Rate B. other : Reserved.
16	reg_w1c_mpcie_config	**For debug purpose.** SW can write one to clear MPCIe config bit of configuration space.
8	reg_mpcie_t2r_lpbk	**0 : normal mode** 1 : IF MPHY TX connect to itself RX, SW can set the register to 1 to link up.
2	reg_mpcie_stall_en	**0 : MPCIe don't enter stall in L0 state.** 1 : MPCIe can enter stall in L0 state. If MPCIe enter stall then LTSSM will go to L0s state
1	reg_mpcie_sw_ltssm_en	**0 : ltssm will stay in RXDET QUIET (HIBERN8)** If the register is 0 , SW can access mPCIe or MPHY attributes by mPCIe AHB access ATTR control register. 1 : ltssm will start RXDET process. If the register is 1, SW can't access mPCIe or MPHY attributes by mPCIe AHB access ATTR control register. For Toshiba testchip, SW may need to set the register to 0 for config MPHY attributes.
0	reg_mpcie_func_en	**0 : disable mpcie function.** 1. : enable mpcie function.

Bit(s)	Name	Description
		If disable, mPCIe MAC will force MPHY power down to save power.

1A145574 REG_MPCIE_CLK_CTRL_1 MPCIE CLOCK CTRL 1 01241F1A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_sel_100us_unit				reg_ls_pwmg1_10us_cycle				reg_hs_g1b_1us_cycle							
Type	RW				RW				RW							
Reset	0				0	0	0	1	0	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_hs_g1a_1us_cycle								reg_cfg_1us_cycle							
Type	RW								RW							
Reset	0	0	0	1	1	1	1	1	0	0	0	1	1	0	1	0

Bit(s)	Name	Description
31	reg_sel_100us_unit	**Select timing unit for "Tactivate time" and "Hibern8 time" in MPCIe.** 0 : timing unit is 1us 1 : timing unit is 100us
27:24	reg_ls_pwmg1_10us_cycle	**the clock cycle number of PWM G1 clock to reach 10us.** EX : 200KHz need 2 cycle to reash 10us.
23:16	reg_hs_g1b_1us_cycle	**the clock cycle number of HS GEAR1 Rate B clock to reach 1us.** EX : 36.44 MHz need 36 cycle to reash 1us.
15:8	reg_hs_g1a_1us_cycle	**the clock cycle number of HS GEAR1 Rate A clock to reach 1us.** EX : 31.2MHz need 31 cycle to reash 1us.
7:0	reg_cfg_1us_cycle	**the clock cycle number of rmmi_cfg_ck to reach 1us.** EX : 26MHz need 26 cycle to reach 1us.

Bit(s)	Name	Description

1A145578 REG_MPCIE_CLK_CTRL_2 MPCIE CLOCK CTRL 1 00100A28

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_ls_pwmg1_100us_cycle															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_cfg_100us_cycle															
Type	RW															
Reset	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0

Bit(s)	Name	Description
31:16	reg_ls_pwmg1_100us_cycle	**the clock cycle number of PWM G1 clock to reach 100us.** EX : 200KHz need 20 cycle to reash 100us.
15:0	reg_cfg_100us_cycle	**the clock cycle number of rmmi_cfg_ck to reach 100us.** EX : 26MHz need 2600 cycle to reach 100us.

1A14557C REG_MPCIE_CLK_CTRL_3 MPCIE CLOCK CTRL 2 0E3C0C30

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_hs_g1b_100us_cycle															
Type	RW															
Reset	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_hs_g1a_100us_cycle															
Type	RW															
Reset	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
31:16	reg_hs_g1b_100us_cycle	**the clock cycle number of HS GEAR1 Rate B clock to reach 100us.** EX : 36.44 MHz need 3644 cycle to reash 100us.
15:0	reg_hs_g1a_100us_cycle	**the clock cycle number of HS GEAR1 Rate A clock to reach 100us.** EX : 31.2MHz need 3120 cycle to reash 100us.

1A145580 REG_MPCIE_EBUF MPCIE EBUF Control 00070405

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				reg_mpcie_skp_rmv_mode				reg_mpcie_ebuf_swrst					reg_mpcie_k_ful			
Type				RW				RW					RW			
Reset				0				0					0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					reg_mpcie_k_mid								reg_mpcie_k_emp			
Type					RW								RW			
Reset					0	1	0	0					0	1	0	1

Bit(s)	Name	Description
28	reg_mpcie_skp_rmv_mode	**The register can use to decide how many SKP will be removed in MPCIe elastic buffer.** 0 : remote at most 2 SKP. 1 : remove all SKP.
24	reg_mpcie_ebuf_swrst	**SW can set 1 to reset ebuf module and clear to release reset.** 1 : reset ebuf module.
19:16	reg_mpcie_k_ful	**The almost full threshold for MPCIe ebuf.** If available data is more than the threshold, ebuf will start remove SKP OS.

Bit(s)	Name	Description
11:8	reg_mpcie_k_mid	**The middle threshold for MPCIe ebuf.** If available data is more than the threshold, controller will start to read data which is in ebuf.
3:0	reg_mpcie_k_emp	**The almost empty threshold for MPCIe ebuf.** If available data is less than the threshold, ebuf will start insert SKP OS.

1A145584 REG_AHB_ATTR_CTRL MPCIE AHB Access ATTR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ahb_attr_req						ahb_attr_wrn	ahb_attr_ext_acc	ahb_attr_wrdata							
Type	RW						RW	RW	RW							
Reset	0						0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ahb_attr_upaddr						ahb_attr_lowaddr							
Type			RW						RW							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	ahb_attr_req	**SW can set the register to request access MPCIe or mPHY attribute through RMMI interface when "reg_mpcie_sw_ltssm_en" is 0 and LTSSM stay in RXDET.QUIET state.** SW should set data, address, write/ read register before set the register and wait the register is clear by HW.
25	ahb_attr_wrn	**0 : read access.** 1 : write access.
24	ahb_attr_ext_acc	**For toshiba mPHY.** Because toshiba mPHY has some user define attribute, those attribute must access by "ext_acc" signal.

Bit(s)	Name	Description
		If SW would access user defined attributes in toshiba mPHY, please set the register to 1. 0 : HW don't assert "rmmi_attr_ext_acc" signal. 1 : HW will assert "rmmi_attr_ext_acc" signal.
23:16	ahb_attr_wrdata	**The data to write into attribute.**
13:8	ahb_attr_upaddr	**High address of attribute in mPCIe or mPHY.** Please refer to MPCIe or mPHY SPEC about attribute content. 0x00 ~ 0x1f : lane0 ~ lane31 mPHY. 0x21 : MPCIe.
7:0	ahb_attr_lowaddr	**Low address of attribute in mPCIe or mPHY.** Please refer to MPCIe or mPHY SPEC about attribute content.

1A145588 REG_AHB_ATTR_RDDATA MPCIE AHB Access ATTR Read Data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**ahb_attr_rddata**							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	ahb_attr_rddata	**The register will keep read data in last read request.** The read data is valid when "ah_attr_req" is clear by HW.

1A14558C LTSSM_TIME_VALUE_1 LTSSM timing value 1 00F00014

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							reg_ltssm_24ms									
Type							RW									
Reset							0	0	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							reg_ltssm_2ms									
Type							RW									
Reset							0	0	0	0	0	1	0	1	0	0

Bit(s)	Name	Description
25:16	reg_ltssm_24ms	**LTSSM 24ms timing value. The value can effect all 24ms timer in LTSSM.** Unit : 100us
9:0	reg_ltssm_2ms	**LTSSM 2ms timing value. The value can effect all 2ms timer in LTSSM.** Unit : 100us

1A145590 LTSSM_TIME_VALUE_2 LTSSM timing value 2 000A0258

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									reg_stall_noconfig_cycle							
Type									RW							
Reset									0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							reg_rrap_rsp_time									
Type							RW									
Reset							1	0	0	1	0	1	1	0	0	0

Bit(s)	Name	Description
23:16	reg_stall_noconfig_cycle	**The clock cycle MAC must stay in STALL.**
9:0	reg_rrap_rsp_time	**MPCIe RRAP response timeout value.**

Bit(s)	Name	Description
		Unit : 100us

1A1455A0 REG_ES_7COUNT_LANE0 Error Statistic Count7 of Lane0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	es_7count_lane0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	es_7count_lane0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	es_7count_lane0	**Lane0 :** SKP remove counter. Stop at FFFF_FFFF PIPE: RxStatus[2:0]=010

1A1455A4 REG_ES_7COUNT_LANE1 Error Statistic Count7 of Lane1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	es_7count_lane1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	es_7count_lane1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	es_7count_lane1	**Lane1 :** SKP remove counter. Stop at FFFF_FFFF PIPE: RxStatus[2:0]=010

1A1455A8 REG_ES_8COUNT_LANE0 Error Statistic Count8 of Lane0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	es_8count_lane0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	es_8count_lane0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	es_8count_lane0	**Lane0 :** SKP add counter. Stop at FFFF_FFFF PIPE: RxStatus[2:0]=001

1A1455AC REG_ES_8COUNT_LANE1 Error Statistic Count8 of Lane1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	es_8count_lane1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	es_8count_lane1															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	es_8count_lane1	**Lane1 :** SKP add counter. Stop at FFFF_FFFF PIPE: RxStatus[2:0]=001

1A1455B0 REG_ES_STATUS_LANE0 Error Statistic Status register of Lane0 00008108

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**rpl_avail_tlp**	**cred_over_cpl**	**cred_over_np**	**cred_over_p**	**cred_avail_cpl**	**cred_avail_np**	**cred_avail_p**	**rpl_avail_cfg**	**laneo_skp_rmv_add**	**laneo_ebuf_underflow**	**laneo_ebuf_overflow**	**laneo_linkdown**	**laneo_elecidle**	**laneo_LTSSM**		
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO		
Reset	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
15	rpl_avail_tlp	**0: replay buffer space is not available to handle next TLP from application layer.** 1: replay buffer space is available to handle next TLP from application layer.
14	cred_over_cpl	**0: local device Cpl credit is NOT overflowed by peer node** 1: local device Cpl credit is overflowed by peer node
13	cred_over_np	**0: local device NP credit is NOT overflowed by peer node** 1: local device NP credit is overflowed by peer node
12	cred_over_p	**0: local device Posted credit is NOT overflowed by peer node**

Bit(s)	Name	Description
		1: local device Posted credit is overflowed by peer node
11	cred_avail_cpl	**0: peer node credit is NOT available to handle next CplD TLP from local device** 1: peer node credit is available to handle next CplD TLP from local device
10	cred_avail_np	**0: peer node credit is NOT available to handle next NP TLP from local device** 1: peer node credit is available to handle next NP TLP from local device
9	cred_avail_p	**0: peer node credit is NOT available to handle next Posted TLP from local device** 1: peer node credit is available to handle next Posted TLP from local device
8	rpl_avail_cfg	**0: replay buffer space is not available to handle next TLP from configuraiton space.** 1: replay buffer space is available to handle next TLP from configuration space. - AssertINTx message - DeassertINTx message - MSI message - Completion which the status is not SC - Error message - PM message - LTR message
7	lane0_skp_rmv_add	**0: Never SKIP removed or added** 1: SKIP removed or added at least once PIPE: RxStatus[2:0]=001 or 010
6	lane0_ebuf_underflow	**0: Never elastic buffer underflow** 1: Elastic buffer underflow at least once PIPE: RxStatus[2:0]=110
5	lane0_ebuf_overflow	**0: Never elastic buffer overflow** 1: Elastic buffer overflow at least once PIPE: RxStatus[2:0]=101
4	lane0_linkdown	**0:link-down never happened after enter L0**

Bit(s)	Name	Description
		1:link-down has ever happened after first link-up
3	lane0_elecidle	**0: Non-Eletrical Idle** 1: Electrical Idle
2:0	lane0_LTSSM	**000: Detect** 001: Polling 011: Los 010: Lo 110: L1 111:Config 101:Recovery 100:Loopback or disable

1A1455B8 REG_ES_0COUNT_LANE0 Error Statistic Count0 of Lane0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**es_ocount_lane0**							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	es_ocount_lane0	**Lane0 :** Count 8b/10b or disparity error. Stop at FF PIPE: RxStatus[2:0]=100 or 111

1A1455BC REG_ES_0COUNT_LANE1 Error Statistic Count0 of Lane1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**es_0count_lane1**							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	es_0count_lane1	**Lane1 :** Count 8b/10b or disparity error. Stop at FF PIPE: RxStatus[2:0]=100 or 111

1A1455C0 REG_ES_1COUNT Error Statistic Count1 of VC0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**es_1count**							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	es_1count	**Count transmitted NAK DLLP of VC0. Stop at 0xFF.** Cleared by MAC reset or REG_ES_CLEAR_ALL.

1A1455C4 REG_ES_2COUNT Error Statistic Count2 of VC0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**es_2count**							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	es_2count	**Count received NAK DLLP of VC0. Stop at 0xFF.** Cleared by MAC reset or REG_ES_CLEAR_ALL.

1A1455C8 REG_ES_3COUNT Error Statistic Count3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**es_3count**							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	es_3count	**Count enter recovery times. Stop at FF** Note : Exlude Power management and other possible regular cases.

1A1455CC REG_ES_CLEAR_ALL Error Statistic Clear 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																es_clear_all
Type																RW
Reset																0

Bit(s)	Name	Description
0	es_clear_all	**0 : don't clear all status and counter.** 1 : clear all status and counter. Write 1 and then wirte 0 to procced an entire ES reset event.

1A1455D0 REG_ES_4COUNT Error Statistic Count4 of VC0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	es_4count															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	es_4count	**Bit[2:0]: Remaining PH credit of peer node.** Bit[15:4]: Remaining PD credit of peer node. Run time update.

1A1455D4 REG_ES_5COUNT Error Statistic Count5 of VC0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	es_5count															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	es_5count															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	es_5count	**Bit[2:0]: Remaining CPLH credit of peer node.** Bit[15:4]: Remaining CPLD credit of peer node. Bit[18:16]: Remaining NPH credit of peer node. Bit[22:20]: Remaining NPD credit of peer node. Bit[24]: Peer node have infinite PH credits. Bit[25]: Peer node have infinite PD credits. Bit[26]: Peer node have infinite CPLH credits. Bit[27]: Peer node have infinite CPLD credits. Bit[28]: Peer node have infinite NPH credits. Bit[29]: Peer node have infinite NPD credits. Run time update.

1A1455D8 REG_ES_6COUNT Error Statistic Count6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									es_6count							
Type									RO							

Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	es_6count	**Bit[0]: MRd TLP with TAG = 0 is waiting for CplD** Bit[1]: MRd TLP with TAG = 1 is waiting for CplD Bit[2]: MRd TLP with TAG = 2 is waiting for CplD Bit[3]: MRd TLP with TAG = 3 is waiting for CplD Bit[4]: MRd TLP with TAG = 4 is waiting for CplD Bit[5]: MRd TLP with TAG = 5 is waiting for CplD Bit[6]: MRd TLP with TAG = 6 is waiting for CplD Bit[7]: MRd TLP with TAG = 7 is waiting for CplD

1A1455E0 REG_I2C_CONTROL_OUT_0 I2C Output Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**I2C_SCL_OEN**	**I2C_SCL_OUT**	**I2C_SDA_OEN**	**I2C_SDA_OUT**
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	I2C_SCL_OEN	**I2C clock output enable.** Not used when I2C_INCLUDED is not defined.
2	I2C_SCL_OUT	**I2C clock out.**

Bit(s)	Name	Description
		Not used when I2C_INCLUDED is not defined.
1	I2C_SDA_OEN	**I2C data output enable.** Not used when I2C_INCLUDED is not defined.
0	I2C_SDA_OUT	**I2C data out.** Not used when I2C_INCLUDED is not defined.

1A1455E4 REG_I2C_CONTROL_IN_0 I2C Input Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**I2C_SCL_IN**	**I2C_SDA_IN**
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	I2C_SCL_IN	**I2C clock in.** Not used when I2C_INCLUDED is not defined.
0	I2C_SDA_IN	**I2C data in.** Not used when I2C_INCLUDED is not defined.

1A1455F0 REG_PE2_MAC_DBG_OUT PE2 MAC Debug Out 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_pe2_mac_dbg_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_pe2_mac_dbg_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	reg_pe2_mac_dbg_out	**The register can reflect debug output.** SW can select debug signal by setting 0x0518 and 0x051c.

1A1455F4 EP_LTSSM_FLAG EP LTSSM Flag 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																pcie_ep_l2_flag
Type																W1C
Reset																0

Bit(s)	Name	Description
0	pcie_ep_l2_flag	**The bit indicate PCIe EP enter L2 state and software can toggle "rg_wake_n_enable" register to execute remote wakeup.**

1A1455F8 SW_PROBE_OUT Software Probe Out Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_sw_prb_out															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_sw_prb_out															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	reg_sw_prb_out	**For Software debug.** Need to set module select debugging to 0x0F0F0F0F

1A1455FC PCI_MAC_HW_SUB_VERSION PCI Express MAC HW Sub Version 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_hw_sub_version															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_hw_sub_version															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	reg_hw_sub_version	**For record ECO version.**

1A145800 TEST_IN_00 Error Injection for Test Purpose 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1A145804 TEST_OUT_00 Internal State for Monitoring Purpose 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

1A145808 TEST_IN_01 Error Injection for Test Purpose 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																

Type																
Reset																

Bit(s)	Name	Description

1A14580C TEST_IN_02 K FIX ID source 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

2.1.4 SATA AHCI

Module name: sata Base address: (+1a200000h)

Address	Name	Width	Register Function
1A200000	CAP	32	HBA Capabilities Register
1A200004	GHC	32	Global HBA Control Register
1A200008	IS	32	Interrupt Status Register
1A20000C	PI	32	Ports Implemented Register
1A200010	VS	32	AHCI Version Register
1A200014	CCC_CTL	32	Command Completion Coalescing Control Register
1A200018	CCC_PORTS	32	Command Completion Coalescing Ports Register
1A200024	CAP2	32	HBA Capabilities Extended Register
1A2000A0	BISTAFR	32	BIST Activate FIS Register
1A2000A4	BISTCR	32	BIST Control Register
1A2000A8	BISTFCTR	32	BIST FIS Count Register
1A2000AC	BISTSR	32	BIST Status Register

Address	Name	Width	Register Function
1A2000B0	BISTDECR	32	BIST DWORD Error Count Register
1A2000B4	DIAGNR	32	Diagnostic Register
1A2000B8	DIAGNR1	32	Diagnostic1 Register
1A2000C8	DBGCTL	32	Debug Control Register
1A2000CC	DBGTRGMSK	32	Debug Trigger Mask Register
1A2000D0	GPCR	32	General Purpose Control Register
1A2000D8	DBGCHGMSK	32	Debug Change Mask Register
1A2000DC	PHYDONE	32	PHY Reset Done Register
1A2000E0	TIMER1MS	32	Timer 1-ms Register
1A2000E4	DBGTRGREC	32	Debug Trigger Record Register
1A2000E8	GPARAM1R	32	Global Parameter 1 Register
1A2000EC	GPARAM2R	32	Global Parameter 2 Register
1A2000F0	PPARAMR	32	Port Parameter Register
1A2000F4	TESTR	32	Test Register
1A2000F8	VERSIONR	32	Version Register
1A2000FC	IDR	32	ID Register
1A200100	PxCLB	32	Port x Command List Base Address Register
1A200104	PxCLBU	32	Port x Command List Base Address Upper 32-Bits Register
1A200108	PxFB	32	Port x FIS Base Address Register
1A20010C	PxFBU	32	Port x FIS Base Address Upper 32-Bits Register
1A200110	PxIS	32	Port x Interrupt Status Register
1A200114	PxIE	32	Port x Interrupt Enable Register
1A200118	PxCMD	32	Port x Command and Status Register
1A200120	PxTFD	32	Port x Task File Data Register
1A200124	PxSIG	32	Port x Signature Register
1A200128	PxSSTS	32	Port x Serial ATA Status Register
1A20012C	PxSCTL	32	Port x Serial ATA Control Register
1A200130	PxSERR	32	Port x Serial ATA Error Register
1A200134	PxSACT	32	Port x Serial ATA Active Register
1A200138	PxCI	32	Port x Command Issue Register
1A20013C	PxSNTF	32	Port x Serial ATA Notification Register
1A200174	PxVS1	32	Port x Vendor Specific Register

1A200000 CAP HBA Capabilities Register 6536FF80

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	S64A	SNCQ	SSNTF	SMPS	SSS	SALP	SAL	SCLO	ISS				SNZO	SAM	SPM	FBSS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO				RO	RO	RO	RO
Reset	0	1	1	0	0	1	0	1	0	0	1	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	PMD	SSC	PSC	NCS					CCCS	EMS	SXS	NP					
Type	RO	RO	RO	RO					RO	RO	RO	RO					
Reset	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	

Bit(s)	Mnemonic	Name	Description
31		S64A	**Supports 64-bit Addressing** Indicate whether the HBA can access 64-bit data structures.
30		SNCQ	**Supports Native Command Queuing** Indicate whether the HBA supports SATA NCQ.
29		SSNTF	**Supports SNotification Register** Indicate whether the HBA supports the PxSNTF (SNotification) register and its associated functionality.
28		SMPS	**Supports Mechanical Presence Switch** Indicate whether the HBA supports mechanical presence switches on its ports for use in hot plug operations.
27		SSS	**Supports Staggered Spin-up** Indicate whether the HBA supports staggered spin-up on its ports, for use in balancing power spikes.
26		SALP	**Supports Aggressive Link Power Management** Indicate whether the HBA can support auto-generating link requests to the Partial or Slumber states when there are no commands to process.
25		SAL	**Supports Activity LED** Indicate whether the HBA supports a single activity indication output pin.
24		SCLO	**Supports Command List Override** Indicate whether the HBA supports the PxCMD.CLO bit and its associated function.
23:20		ISS	**Interface Speed Support** Indicate the maximum speed the HBA can support on its ports. 0001: Gen. 1 (1.5 Gbps) 0010: Gen. 2 (3.0 Gbps)

Bit(s)	Mnemonic	Name	Description
			0011: Gen. 3 (6.0 Gbps) Others: Reserved
19		SNZO	**Supports Non-Zero DMA Offsets** This feature is not supported.
18		SAM	**Supports AHCI Mode Only** Indicate whether that the SATA controller implements a legacy, task-file based register interface. 0: Support AHCI and legacy mode 1: Support AHCI mode only
17		SPM	**Supports Port Multiplier** Indicate whether the HBA can support a Port Multiplier.
16		FBSS	**FIS-based Switching Supported** Indicate whether the HBA supports Port Multiplier FIS-based switching.
15		PMD	**PIO Multiple DRQ Block** Indicate whether the HBA supports multiple DRQ block data transfers for the PIO command protocol.
14		SSC	**Slumber State Capable** Indicate whether the HBA can support transitions to the Slumber state.
13		PSC	**Partial State Capable** Indicate whether the HBA can support transitions to the Partial state.
12:8		NCS	**Number of Command Slots** 0's based value indicating the number of command slots per port supported by this HBA.
7		CCCS	**Command Completion Coalescing Support** Indicate whether the HBA supports command completion coalescing. If the HBA supports it, the CCC_CTL and CCC_PORTS global HBA registers are implemented.
6		EMS	**Enclosure Management Support**

Bit(s)	Mnemonic	Name	Description
			Indicate whether the HBA supports enclosure management. If the HBA supports it, the EM_LOC and EM_CTL global HBA registers are implemented.
5		SXS	**Supports External SATA** Indicate whether the HBA has one or more SATA ports which has a signal only connector which is externally accessible (e.g. eSATA connector).
4:0		NP	**Number of Ports** 0's based value indicating the maximum number of ports supported by the HBA. 00000: 1 Port Others: Reserved

1A200004 GHC Global HBA Control Register 80000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE															
Type	RO															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															IE	HR
Type															RW	WO
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31		AE	**AHCI Enable** Indicate that communication to the HBA shall be via AHCI mechanisms.
1		IE	**Interrupt Enable** Root interrupt enable of the HBA
0		HR	**HBA Reset** Internal reset of the HBA. This bit is set to '1' by SW and cleared to '0' by the HBA.

Bit(s)	Mnemonic	Name	Description

1A200008 IS Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**IPS**
Type																W1C
Reset																0

Bit(s)	Mnemonic	Name	Description
0		IPS	**Interrupt Pending Status** This register is bit significant. Indicates that the corresponding port has an interrupt event pending in the PxIS bits and enabled by PxIE, or CCC interrupt defined by CCC_CTL.INT.

1A20000C PI Ports Implemented Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**PI**
Type																RO
Reset																0

Bit(s)	Mnemonic	Name	Description
0		PI	**Ports Implemented** This register is bit significant and can be write once after reset. If a bit is set to '1', the corresponding port is available for software to use.

1A200010 VS AHCI Version Register 00010300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MJR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MNR															
Type	RO															
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:16		MJR	**Major Version Number**
15:0		MNR	**Minor Version Number**

1A200014 CCC_CTL Command Completion Coalescing Control Register 00010108

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TV															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CC								INT							EN
Type	RW								RO							RW
Reset	0	0	0	0	0	0	0	1	0	0	0	0	1			0

Bit(s)	Mnemonic	Name	Description
31:16		TV	**Time-out Value (unit: 1 ms)** Set this value before enable CCC. The HBA would decrease the timer when commands are outstanding on selected ports, and will signal a CCC interrupt when the timer value is equal to zero.
15:8		CC	**Command Completions** Set this value before enable CCC. Specifies the number of command completions that are necessary to cause a CCC interrupt. Zero value to disable this feature.
7:3		INT	**Interrupt** Specifies which port interrupt to be used by the CCC feature. Set to the max. port number corresponds to PI register.
0		EN	**Enable** CCC feature enable

1A200018 CCC_PORTS Command Completion Coalescing Ports Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PRT
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		PRT	**Ports** This field is bit significant. Indicate whether the corresponding port is part of the command completion coalescing feature.

1A200024 CAP2 HBA Capabilities Extended Register 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**APST**	**NVMP**	**BOH**
Type														RO	RO	RO
Reset														1	0	0

Bit(s)	Mnemonic	Name	Description
2		APST	**Automatic Partial to Slumber Transitions** Indicate whether the HBA supports Automatic Partial to Slumber Transitions.
1		NVMP	**NVMHCI Present** Indicate whether the HBA supports NVMHCI and the registers at offset 60h-9Fh.
0		BOH	**BIOS/OS Handoff** Indicate whether the HBA supports the BIOS/OS handoff mechanism.

1A2000A0 BISTAFR BIST Activate FIS Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**NCP**								**PD**							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:8		NCP	**Non-Compliant Pattern** Indicates the "Data1" field (DWORD 1[7:0]) of the received BIST Activate FIS. Applicable only in BIST-T mode (BISTAFR.PD = 0xC0 or 0xE0). 0xF1: Low transition density pattern (LTDP) 0xB5: High transition density pattern (HTDP) 0xAB: Low frequency spectral component pattern (LFSCP) 0x7F: Simultaneous switching outputs pattern (SSOP) Others: Lone bit pattern (LBP) 0x78: Mid frequency test pattern (MFTP) 0x4A: High frequency test pattern (HFTP) 0x7E: Low frequency test pattern (LFTP)
7:0		PD	**Pattern Definition** Indicates the "Pattern Definition" field (DWORD 0[23:16]) of the received BIST Activate FIS 0x10: Far-end retimed (BIST-L) 0x08: Far-end analog (when PHY supports this mode) Not support 0xC0: Far-end transmit only (BIST-T) 0xE0: Far-end transmit only with scrambler bypassed (BIST-T) Others: Negatively acknowledged with R_ERRp

1A2000A4 BISTCR BIST Control Register 00001700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												FERLB		TXO	CNTCLR	NEALB
Type												WO		WO	WO	WO
Reset												0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name				SDFE		LLC				ERREN	FLIP	PV	PATTERN			
Type				RW		RW				RW	RW	RW	RW			
Reset				1		1	1	1		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20		FERLB	**Far-end Retimed Loopback** Let the HBA enter Far-end Retimed mode (BIST-L), w/o the BIST Activate FIS, regardless whether the device is connected or disconnected. This field is one-shot type and reads returns '0'.
18		TXO	**Transmit Only** Let the HBA enter Transmit Only mode (BIST-T) and transmit the pattern defined in BISTCR.PATTERN field. This field is one-shot type and reads returns '0'.
17		CNTCLR	**Counter Clear** Clear BISTFCTR, BISTSR, and BISTDECR registers. This field is one-shot type and reads returns '0'.
16		NEALB	**Near-End External Loopback** Let the HBA enter Near-end external loopback mode and transmit the pattern defined in BISTCR.PATTERN field. This mode should be initiated with the device disconnected. This field is one-shot type and reads returns '0'.
12		SDFE	**Signal Detect Feature Enable** Handle unstable/absent phy_sig_det signal in link layer 0: Disable 1: Enable
10:8		LLC	**Link Layer Control** Controls the Port Link Layer functions: scrambler, de-scrambler, and repeat primitive drop. Bit [10] - RPD 0: Repeat primitive drop function disabled in normal mode, NA in BIST mode 1: Repeat primitive drop function enabled in normal mode, NA in BIST mode Bit [9] - DESCRAM

Bit(s)	Mnemonic	Name	Description
			0: Descrambler disabled in normal mode, enabled in BIST mode 1: Descrambler enabled in normal mode, disabled in BIST mode Bit [8] - SCRAM 0: Scrambler disabled in normal mode, enabled in BIST mode 1: Scrambler enabled in normal mode, disabled in BIST mode In normal mode, these functions can be changed only during port reset (PxSCTL.DET = 0x1)
6		ERREN	**Error Enable** Enable PHY internal errors outside the FIS boundary to set corresponding PxSERR bits.
5		FLIP	**Flip Disparity** Change disparity of the current test pattern to the opposite every time its state is changed by the software.
4		PV	**Pattern Version** Select either short or long version of the SSOP, HTDP, LTDP, LFSCP, COMP patterns. 0: Short pattern version 1: Long pattern version
3:0		PATTERN	**Compliant / Non-compliant Patterns** Compliant patterns for Far-end retimed / Near-end external initiator modes, or non-compliant patterns for Transmit only responder mode when initiated by the SW writing to the BISTCR.TXO bit 0x0: Simultaneous switching outputs pattern (SSOP) 0x1: High transition density pattern (HTDP) 0x2: Low transition density pattern (LTDP) 0x3: Low frequency spectral component pattern (LFSCP) 0x4: Composite pattern (COMP) 0x5: Lone bit pattern (LBP) 0x6: Mid frequency test pattern (MFTP)

Bit(s)	Mnemonic	Name	Description
			0x7: High frequency test pattern (HFTP) 0x8: Low frequency test pattern (LFTP) Others: Composite pattern (COMP)

1A2000A8 BISTFCTR BIST FIS Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	count															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	count															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		count	**Received BIST FIS Count** Count the received BIST FIS in Far-end retimed and Near-end external initiator mode. This value does not roll over and freezes at 0xFFFF_FFFF.

1A2000AC BISTSR BIST Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BRSTERR							
Type									RO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FRAMERR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23:16		BRSTERR	**Burst Error** Count error which is detected in received frames and 1.5 sec. (27,000 frames) passed since the previous burst error was detected. This value does not roll over and freezes at 0xFF.
15:0		FRAMERR	**Frame Error** Count the number of frames with CRC error. This value does not roll over and freezes at 0xFFFF.

1A2000B0 BISTDECR BIST DWORD Error Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DWERR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DWERR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DWERR	**DWORD Error Count** Count DWORD error which is detected in the received frame. This value does not roll over and freezes at 0xFFFF_F000.

1A2000B4 DIAGNR Diagnostic Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERR_RX FIS_OV	ERR_ALL		LNK_ST					TCHK_ST					TSM_ST		

Type	W1C	W1C		RO					RO					RO		
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TSM_ST			RXFIS_ST					PORT_ST							
Type	RO			RO					RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		ERR_RXFIS_OV	**Received FIS overflow (?)**
30		ERR_ALL	**Link and Physical layer err (?)**
28:24		LNK_ST	**Link State**
23:19		TCHK_ST	**Transport Check State**
18:13		TSM_ST	**Transport State**
12:7		RXFIS_ST	**Received FIS State**
6:0		PORT_ST	**HBA Port State**

1A2000B8 DIAGNR1 Diagnostic1 Register 00020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PRIM_ERR	DISP_ERR	CODE_ERR												PREFETCH_DIS	
Type	W1C	W1C	W1C												RW	
Reset	0	0	0												1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Mnemonic	Name	Description
31		PRIM_ERR	**Primitive Error** Indicates that one or more primitive errors occurred.
30		DISP_ERR	**Disparity Error** Indicates that one or more 10b/8b disparity errors occurred inside the data window.
29		CODE_ERR	**Decoding Error** Indicates that one or more 10b/8b coding errors occurred inside the data window.
17		PREFETCH_DIS	**Prefetch Disable** Notice: modify when PxCMD.ST = 0 0: Enable prefetch 1: Disable prefetch

1A2000C8 DBGCTL Debug Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OFFLINE_DET_COMINIT_DIS	SERR_DIAG_D_EN	SW_DBG_EN	SW_DBG_TRIG_EN	SW_DBG_TRIG_CNT				SW_DBG_TRIG_BSY	SW_DBG_TRIG_VAL						
Type	RW	RW	RW	RW	RW				RO	RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SW_DBG_TRIG_VAL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		OFFLINE_DET_COMINIT_DIS	**Detect COMINIT in Offline**

Bit(s)	Mnemonic	Name	Description
			Option to fix DIAG_X behavior in offline mode 0: Enable detect COMINIT 1: Disable detect COMINIT
30		SERR_DIAG_D_EN	**Enable DIAG_D in PxSERR for all received data** 0: Disable PxSERR.DIAG_D 1: Enable PxSERR.DIAG_D
29		SW_DBG_EN	**Software Debug Enable** Enable SW debug selector 0: H/W debug 1: S/W debug
28		SW_DBG_TRIG_EN	**Software Debug Trigger Mode Enable** 0: Bypass mode 1: Trigger mode
27:24		SW_DBG_TRIG_CNT	**Software Debug Trigger Pass Counter**
23		SW_DBG_TRIG_BSY	**Software Debug Trigger Busy** 0: Record stop 1: Recording
22:0		SW_DBG_TRIG_VAL	**Software Debug Trigger Value**

1A2000CC DBGTRGMSK Debug Trigger Mask Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SW_DBG_TRIG_SEL			SW_DBG_LOW_SEL						SW_DBG_TRIG_MASK						
Type	RW			RW						RW						
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SW_DBG_TRIG_MASK															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:29		SW_DBG_TRIG_SEL	**Software Debug Trigger Mode Selector** Select 1 of 8 results before trigger
28:24		SW_DBG_LOW_SEL	**Software Debug Low Selector** Select debug output
22:0		SW_DBG_TRIG_MASK	**Software Debug Trigger Mask**

1A2000D0 GPCR General Purpose Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**Reserved**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**Reserved**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		Reserved	

1A2000D8 DBGCHGMSK Debug Change Mask Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				**SW_DBG_HIGH_SEL**						**SW_DBG_CHG_MASK**						
Type				RW						RW						
Reset				0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SW_DBG_CHG_MASK**															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24		SW_DBG_HIGH_SEL	**Software Debug High Selector** Select debug output
22:0		SW_DBG_CHG_MASK	**Software Debug Change Mask**

1A2000DC PHYDONE PHY Reset Done Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PHYDONE
Type																RO
Reset																0

Bit(s)	Mnemonic	Name	Description
0		PHYDONE	**Phy Reset Done**

1A2000E0 TIMER1MS Timer 1-ms Register 0004C2C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PM_EN												TIMV			
Type	RW												RW			
Reset	0												0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIMV															

Type	RW															
Reset	1	1	0	0	0	0	1	0	1	1	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		PM_EN	**Enable Timer in PM_CK** Count 1ms timer in PM clock domain
19:0		TIMV	**1ms Timer Value** A 1-ms tick based on AXI bus clock frequency for CCC feature. Change this value before enable CCC.

1A2000E4 DBGTRGREC Debug Trigger Record Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SW_DBG_REC_CNT					SW_DBG_REC_VAL						
Type					RO					RO						
Reset					0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SW_DBG_REC_VAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24		SW_DBG_REC_CNT	**Software Debug Record Count**
22:0		SW_DBG_REC_VAL	**Software Debug Record Value**

1A2000E8 GPARAM1R Global Parameter 1 Register D0000409

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALIGN_M	RX_BUFFER	PHY_DATA		PHY_RST	PHY_CTRL						PHY_STAT				
Type	RO	RO	RO		RO	RO						RO				

Reset	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PHY_STAT	LATCH_M	PHY_TYPE			RETURN_ERR	AHB_ENDIAN		S_HADDR	M_HADDR	S_HDATA			M_HDATA		
Type	RO	RO	RO			RO	RO		RO	RO	RO			RO		
Reset	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
31		ALIGN_M	**RX Data Alignment**
30		RX_BUFFER	**RX Data Buffer**
29:28		PHY_DATA	**PHY Data Width** 0x0: 1 0x1: 2 0x2: 4 Others: Reserved
27		PHY_RST	**PHY Reset Mode** 0: Low 1: High
26:21		PHY_CTRL	**PHY Control Width**
20:15		PHY_STAT	**PHY Status Width**
14		LATCH_M	**LATCH_M**
13:11		PHY_TYPE	**PHY Interface Type**
10		RETURN_ERR	**AMBA Error Response** 0: False 1: True
9:8		AHB_ENDIAN	**AHB Bus Endianness** 0x0: Little 0x1: Big 0x2: Dynamic

Bit(s)	Mnemonic	Name	Description
7		S_HADDR	**AMBA Slave Address Bus Width** 0: 32 bits 1: 64 bits
6		M_HADDR	**AMBA Master Address Bus Width** 0: 32 bits 1: 64 bits
5:3		S_HDATA	**AMBA Slave Data Width** 0x0: 32 bits 0x1: 64 bits 0x2: 128 bits 0x3: 256 bits
2:0		M_HDATA	**AMBA Master Data Width** 0x0: 32 bits 0x1: 64 bits 0x2: 128 bits 0x3: 256 bits

1A2000EC GPARAM2R Global Parameter 2 Register 0008124B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BIST_M	FBS_MEM_S	FBS_PMPN	
Type													RO	RO	RO	
Reset													1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FBS_SUPPORT	DEV_CP	DEV_MP	ENCODE_M	RXOOB_CLK_M	RX_OOB_M	TX_OOB_M	RXOOB_CLK								

Type	RO	RO	RO	RO	RO	RO	RO	RO									
Reset	0	0	0	1	0	0	1	0	0	1	0	0	1	0	1	1

Bit(s)	Mnemonic	Name	Description
19		BIST_M	**BIST Loopback Checking Depth** 0: FIS 1: DWORD
18		FBS_MEM_S	**Context RAM memory location** 0: External 1: Internal
17:16		FBS_PMPN	**Maximum Number of Port Multiplier Ports** 0x0: N/A 0x1: 5 0x2: 10 0x3: 15
15		FBS_SUPPORT	**FIS-Based Switching Support** 0: Exclude 1: Include
14		DEV_CP	**Cold Presence Detect** 0: Exclude 1: Include
13		DEV_MP	**Mechanical Presence Switch** 0: Exclude 1: Include
12		ENCODE_M	**8b/10b Encoding/Decoding** 0: Exclude 1: Include
11		RXOOB_CLK_M	**RX OOB Clock Mode** 0: Rx clock

Bit(s)	Mnemonic	Name	Description
			1: Separate
10		RX_OOB_M	**RX OOB Mode** 0: Exclude 1: Include
9		TX_OOB_M	**TX OOB Mode** 0: Exclude 1: Include
8:0		RXOOB_CLK	**RX OOB Clock Frequency**

1A2000F0 PPARAMR Port Parameter Register 00000588

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_MEM_M	TX_MEM_S	RX_MEM_M	RX_MEM_S	TXFIFO_DEPTH				RXFIFO_DEPTH			
Type					RO	RO	RO	RO	RO				RO			
Reset					0	1	0	1	1	0	0	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
11		TX_MEM_M	**TX FIFO Memory Read Port Type** 0: Async 1: Sync
10		TX_MEM_S	**TX FIFO Memory Type** 0: External 1: Internal
9		RX_MEM_M	**RX FIFO Memory Read Port Type**

Bit(s)	Mnemonic	Name	Description
			0: Async
			1: Sync
8		RX_MEM_S	**RX FIFO Memory Type**
			0: External
			1: Internal
7:4		TXFIFO_DEPTH	**TX FIFO Depth (in FIFO words)**
			0x3: 8
			0x4: 16
			0x5: 32
			0x6: 64
			0x7: 128
			0x8: 256
			0x9: 512
			0xA: 1024
			0xB: 2048
			Others: Reserved
3:0		RXFIFO_DEPTH	**RX FIFO Depth (in FIFO words)**
			0x4: 16
			0x5: 32
			0x6: 64
			0x7: 128
			0x8: 256
			0x9: 512
			0xA: 1024
			0xB: 2048
			Others: Reserved

1A2000F4 TESTR Test Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INIT_TSM_EN	AXI_ALIGN_128_EN												PSEL		
Type	RW	RW												RW		
Reset	0	0												0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TEST_IF
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
31		INIT_TSM_EN	**Enable G_INIT for TSM module** Let TSM module can reset by HBA reset 0: TSM cannot rest by HBA reset 1: TSM can rest by HBA reset
30		AXI_ALIGN_128_EN	**AXI Align to 128-byte Enable** Let AXI master interface uses address aligned to 128 bytes 0: Align to bus width (8 bytes) 1: Align to 128 bytes
18:16		PSEL	**Port Select** Select a Port for BIST operation. 0x0: Porto is selected Others: Reserved
0		TEST_IF	**Test Interface** Let AXI slave interface enter the test mode 0: Normal mode 1: Test mode

Bit(s)	Mnemonic	Name	Description

1A2000F8 VERSIONR Version Register 3431302A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VERN															
Type	RO															
Reset	0	0	1	1	0	1	0	0	0	0	1	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VERN															
Type	RO															
Reset	0	0	1	1	0	0	0	0	0	0	1	0	1	0	1	0

Bit(s)	Mnemonic	Name	Description
31:0		VERN	**Version Number (4.10a)** A hard-coded hexadecimal version value (ASCII code).

1A2000FC IDR ID Register 37363232

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ID															
Type	RO															
Reset	0	0	1	1	0	1	1	1	0	0	1	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ID															
Type	RO															
Reset	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	0

Bit(s)	Mnemonic	Name	Description
31:0		ID	**ID Number** A hard-coded hexadecimal identification value.

Bit(s)	Mnemonic	Name	Description

1A200100 PxCLB Port x Command List Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLB															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLB															
Type	RW															
Reset	0	0	0	0	0	0										

Bit(s)	Mnemonic	Name	Description
31:10		CLB	**Command List Base Address** Indicate the 32-bit base physical address for the command list for this port. This base is used when fetching commands to execute. The structure pointed to by this address range is 1K-bytes in length. This address must be 1K-byte aligned as indicated by bits [9:0] being read only.

1A200104 PxCLBU Port x Command List Base Address Upper 32-Bits Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CLBU															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLBU															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CLBU	**Command List Base Address Upper** Indicate the upper 32-bits for the command list base physical address for this port. This base is used when fetching commands to execute.

1A200108 PxFB Port x FIS Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FB															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FB															
Type	RW															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Mnemonic	Name	Description
31:8		FB	**FIS Base Address** Indicate the 32-bit base physical address for received FISes. The structure pointed to by this address range is 256 bytes in length. This address must be 256-byte aligned as indicated by bits [7:0] being read only.

1A20010C PxFBU Port x FIS Base Address Upper 32-Bits Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FBU															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FBU															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		FBU	**FIS Base Address Upper** Indicate the upper 32-bits for the received FIS base physical address for this port.

1A200110 PxIS Port x Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CPDS	TFES	HBFS	HBDS	IFS	INFS		OFS	IPMS	PRCS						
Type	RO	W1C	W1C	W1C	W1C	W1C		W1C	W1C	RO						
Reset	0	0	0	0	0	0		0	0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DMPS	PCS	DPS	UFS	SDBS	DSS	PSS	DHRS
Type									RO	RO	W1C	RO	W1C	W1C	W1C	W1C
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		CPDS	**Cold Port Detect Status** This feature is not support.
30		TFES	**Task File Error Status** This bit is set whenever PxTFD.STS is updated by the device and the error bit (bit 0 of the Status field in the received FIS) is set.
29		HBFS	**Host Bus Fatal Error Status** This bit is set when the HBA AXI master detects an SLVERR or DECERR response from the slave.
28		HBDS	**Host Bus Data Error Status** This feature is not support.
27		IFS	**Interface Fatal Error Status**

Bit(s)	Mnemonic	Name	Description
			This bit is set when any of the following conditions is detected: - SYNC escape is received from the device during non-data or data FIS transmission or reception (PxSERR.DIAG_S and PxSERR.ERR_P are set) - One or more of the following errors are detected during data FIS transfer: * Protocol (PxSERR.ERR_P) * CRC (PxSERR.DIAG_C) * Handshake (PxSERR.DIAG_H) * PHY Not Ready (PxSERR.ERR_C) - Unknown FIS is received with good CRC, but the length exceeds 64 bytes. - PRD table byte count is zero. - DMA Setup FIS is received with a TAG corresponding to inactive (PxSACT bit is cleared) command slot. Port DMA transitions to a fatal state until the software clears PxCMD.ST bit or resets the interface by way of Port or Global reset.
26		INFS	**Interface Non-fatal Error Status** This bit is set when any of the following conditions is detected: - One or more of the following errors are detected during non-data FIS transfer * Protocol (PxSERR.ERR_P) * CRC (PxSERR.DIAG_C) * Handshake (PxSERR.DIAG_H) * PHY Not Ready (PxSERR.ERR_C) - Command list underflow during read operation (i.e. DMA read) when the software builds command table that has more total bytes than the transaction given to the device. In both cases Port operation continues normally. When error is detected during non-data FIS transmission, this FIS is retransmitted continuously until it succeeds, or until the software times out and resets the interface.
24		OFS	**Overflow Status**

Bit(s)	Mnemonic	Name	Description
			This bit is set when the HBA received more bytes from a device than was specified in the PRD table for the command.
23		IPMS	**Incorrect Port Multiplier Status** This bit is set when the HBA received a FIS from a device that did not match what was expected. This bit may be set during enumeration of devices on a Port Multiplier due to the normal Port Multiplier enumeration process. The software must use the IPMS bit only after enumeration is complete on the Port Multiplier.
22		PRCS	**PHY Ready Change Status** This bit is set when the internal phy ready signal changed state. This bit reflects the state of the PxSERR.DIAG_N. To clear this bit, the software must clear the PxSERR.DIAG_N bit to 0.
7		DMPS	**Device Mechanical Presence Status** This feature is not support.
6		PCS	**Port Connect Change Status** This bit reflects the state of the PxSERR.DIAG_X bit. This bit is only cleared when PxSERR.DIAG_X is cleared. 0: No change in Current Connect Status 1: Change in Current Connect Status
5		DPS	**Descriptor Processed** A PRD with the 'I' bit set has transferred all of its data.
4		UFS	**Unknown FIS Interrupt** When set to '1', indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to '0' by software clearing the PxSERR.DIAG_F bit to '0'. Note that this bit does not directly reflect the PxSERR.DIAG_F bit. PxSERR.DIAG_F is set immediately when an unknown FIS is detected, whereas this bit is set when that FIS is posted to memory. SW should wait to act on an unknown FIS until this bit is set to '1' or the two bits may become out of sync.
3		SDBS	**Set Device Bits Interrupt** A Set Device Bits FIS has been received with the 'I' bit set and has been copied into system memory.

Bit(s)	Mnemonic	Name	Description
2		DSS	**DMA Setup FIS Interrupt** A DMA Setup FIS has been received with the 'I' bit set and has been copied into system memory.
1		PSS	**PIO Setup FIS Interrupt** A PIO Setup FIS has been received with the 'I' bit set, it has been copied into system memory, and the data related to that FIS has been transferred. This bit shall be set even if the data transfer resulted in an error.
0		DHRS	**Device to Host Register FIS Interrupt** A D2H Register FIS has been received with the 'I' bit set, and has been copied into system memory.

1A200114 PxIE Port x Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CPDE	TFEE	HBFE	HBDE	IFE	INFE		OFE	IPME	PRCE						
Type	RO	RW	RW	RW	RW	RW		RW	RW	RW						
Reset	0	0	0	0	0	0		0	0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DMPE	PCE	DPE	UFE	SDBE	DSE	PSE	DHRE
Type									RO	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		CPDE	**Cold Port Detect Enable** This feature is not support.
30		TFEE	**Task File Error Enable** When set, GHC.IE is set, and PxS.TFES is set, the HBA shall generate an interrupt.
29		HBFE	**Host Bus Fatal Error Enable** When set, GHC.IE is set, and PxIS.HBFS is set, the HBA shall generate an interrupt.
28		HBDE	**Host Bus Data Error Enable**

Bit(s)	Mnemonic	Name	Description
			When set, GHC.IE is set, and PxIS.HBDS is set, the HBA shall generate an interrupt.
27		IFE	**Interface Fatal Error Enable** When set, GHC.IE is set, and PxIS.IFS is set, the HBA shall generate an interrupt.
26		INFE	**Interface Non-Fatal Error Enable** When set, GHC.IE is set, and PxIS.INFS is set, the HBA shall generate an interrupt.
24		OFE	**Overflow Enable** When set, and GHC.IE is set, and PxIS.OFS is set, the HBA shall generate an interrupt.
23		IPME	**Incorrect Port Multiplier Enable** When set, and GHC.IE is set, and PxIS.IPMS is set, the HBA shall generate an interrupt.
22		PRCE	**PHY Ready Change Enable** When set, and GHC.IE is set, and PxIS.PRCS is set, the HBA shall generate an interrupt.
7		DMPE	**Device Mechanical Presence Enable** This feature is not support.
6		PCE	**Port Change Interrupt Enable** When set, GHC.IE is set, and PxIS.PCS is set, the HBA shall generate an interrupt.
5		DPE	**Descriptor Processed Interrupt Enable** When set, GHC.IE is set, and PxIS.DPS is set, the HBA shall generate an interrupt.
4		UFE	**Unknown FIS Interrupt Enable** When set, GHC.IE is set, and PxIS.UFS is set, the HBA shall generate an interrupt.
3		SDBE	**Set Device Bits FIS Interrupt Enable** When set, GHC.IE is set, and PxIS.SDBS is set, the HBA shall generate an interrupt.
2		DSE	**DMA Setup FIS Interrupt Enable** When set, GHC.IE is set, and PxIS.DSS is set, the HBA shall generate an interrupt.
1		PSE	**PIO Setup FIS Interrupt Enable**

Bit(s)	Mnemonic	Name	Description
			When set, GHC.IE is set, and PxIS.PSS is set, the HBA shall generate an interrupt.
0		DHRE	**Device to Host Register FIS Interrupt Enable** When set, GHC.IE is set, and PxIS.DHRS is set, the HBA shall generate an interrupt.

1A200118 PxCMD Port x Command and Status Register 00000006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ICC				ASP	ALPE	DLAE	ATAPI	APSTE	FBSCP	ESP	CPD	MPSP	HPCP	PMA	CPS
Type	RW				RW	RW	RW	RW	RW	RO	RO	RO	RO	RO	RW	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CR	FR	MPSS	CCS								FRE	CLO	POD	SUD	ST
Type	RO	RO	RO	RO								RW	WO	RO	RO	RW
Reset	0	0	0	0	0	0	0	0				0	0	1	1	0

Bit(s)	Mnemonic	Name	Description
31:28		ICC	**Interface Communication Control** This field is used to control power management states of the interface. If the Link layer is currently in the L_IDLE state, writes to this field shall cause the HBA to initiate a transition to the interface power management state requested. If the Link layer is not currently in the L_IDLE state, writes to this field shall have no effect. When the software writes a non-reserved value other than No-Op (0x0), the Port performs the action and updates this field back to Idle (0x0). When the SW writes to this field to change the state to a state the link is already in (such as, interface is in the active state and a request is made to go to the active state), the Port takes no action and returns this field to Idle. When the interface is in a low power state and the SW wants to transition to a different low power state, the SW must first bring the link to active and then initiate the transition to the desired low power state. 0x0: No-Op/ Idle. This value indicates the HBA is ready to accept a new interface control command,

Bit(s)	Mnemonic	Name	Description
			although the transition to the previously selected state may not yet have occurred. 0x1: Active: This causes the HBA to request a transition of the interface into the active state. 0x2: Partial. This causes the Port to request a transition of the interface to the Partial state. The SATA device can reject the request and the interface remains in its current state. 0x6: Slumber. This causes the Port to request a transition of the interface to the Slumber state. The SATA device can reject the request and the interface remains in its current state. Others: Reserved
27		ASP	**Aggressive Slumber/ Partial** - When set to 1, and PxCMD.ALPE=1, the Port aggressively enters the slumber state when one of the following conditions is true: * The Port clears the PxCI and the PxSACT register is cleared. * The Port clears the PxSACT register and PxCI is cleared. - When cleared to 0, and PxCMD.ALPE=1, the Port aggressively enters the partial state when one of the following conditions is true: * The Port clears the PxCI register and the PxSACT register is cleared. * The Port clears the PxSACT register and P#CI is cleared. 0: Partial 1: Slumber
26		ALPE	**Aggressive Link Power Management Enable** When set to '1', the HBA shall aggressively enter a lower link power state (partial or slumber) based upon the setting of the ASP bit.
25		DLAE	**Drive LED on ATAPI Enable** This feature is not support.
24		ATAPI	**Device is ATAPI** This bit is used by the Port to control the LED. This feature is not support.

Bit(s)	Mnemonic	Name	Description
23		APSTE	**Automatic Partial to Slumber Transitions Enable** When set to '1', the HBA may perform Automatic Partial to Slumber Transitions. When cleared to '0' the port shall not perform Automatic Partial to Slumber Transitions. SW shall only set this bit to '1' if CAP2.APST is set to '1'; if CAP2.APST is cleared to '0' SW shall treat this bit as reserved.
22		FBSCP	**FIS-based Switching Capable Port** This feature is not support.
21		ESP	**External SATA Port** This feature is not support.
20		CPD	**Cold Presence Detection** This feature is not support.
19		MPSP	**Mechanical Presence Switch Attached to Port** This feature is not support.
18		HPCP	**Hot Plug Capable Port** When set to '1', indicates that this port's signal and power connectors are externally accessible via a joint signal and power connector for blind-mate device hot plug. When cleared to '0', indicates that this port's signal and power connectors are not externally accessible via a joint signal and power connector. HPCP is mutually exclusive with the ESP bit in this register.
17		PMA	**Port Multiplier Attached** When set to '1' by SW, a Port Multiplier is attached to the HBA for this port. When cleared to '0' by SW, a Port Multiplier is not attached to the HBA for this port. SW is responsible for detecting whether a Port Multiplier is present; HW does not auto-detect the presence of a Port Multiplier. SW shall only set this bit to '1' when PxCMD.ST is cleared to '0'. 0: A Port Multiplier is not attached to this Port. 1: A Port Multiplier is attached to this Port.
16		CPS	**Cold Presence State** This feature is not support.
15		CR	**Command List Running**

Bit(s)	Mnemonic	Name	Description
			When this bit is set, the command list DMA engine for the port is running.
14		FR	**FIS Receive Running** When set, the FIS Receive DMA engine for the port is running.
13		MPSS	**Mechanical Presence Switch State** This feature is not support.
12:8		CCS	**Current Command Slot** This field is set to the command slot value of the command that is currently being issued by the Port. - When P#CMD.ST transitions from 1 to 0, this field is cleared again to 0x00. - After P#CMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is PxCMD.CCS+1. For example, after the Port has issued its first command, when CCS=0x00 and PxCI is set to 0x3, the next command issued is from command slot 1. This field is valid only when PxCMD.ST is set to 1.
4		FRE	**FIS Receive Enable** When set, the HBA may post received FISes into the FIS receive area pointed to by PxFB (and for 64-bit HBAs, PxFBU). When cleared, received FISes are not accepted by the HBA, except for the first D2H register FIS after the initialization sequence, and no FISes are posted to the FIS receive area. System SW must not set this bit until PxFB (PxFBU) have been programmed with a valid pointer to the FIS receive area, and if SW wishes to move the base, this bit must first be cleared, and SW must wait for the FR bit in this register to be cleared.
3		CLO	**Command List Override** Setting this bit to '1' causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to '0'. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The HBA sets this bit to '0' when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to '0'. A write to this register with a value of '0' shall have no effect. This bit shall only be set to '1' immediately prior to setting the PxCMD.ST bit to '1' from a previous value of '0'. Setting this bit to '1' at any other time is not

Bit(s)	Mnemonic	Name	Description
			supported and will result in indeterminate behavior. Software must wait for CLO to be cleared to '0' before setting PxCMD.ST to '1'.
2		POD	**Power On Device** This feature is not support.
1		SUD	**Spin-Up Device** This feature is not support. The value is 0 after reset and changed to 1 after S/W set CAP register.
0		ST	**Start** When set, the HBA may process the command list. When cleared, the HBA may not process the command list. Whenever this bit is changed from a '0' to a '1', the HBA starts processing the command list at entry '0'. Whenever this bit is changed from a '1' to a '0', the PxCI register is cleared by the HBA upon the HBA putting the controller into an idle state. This bit shall only be set to '1' by SW after PxCMD.FRE has been set to '1'.

1A200120 PxTFD Port x Task File Data Register 0000007F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ERR**								**STS**							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
15:8		ERR	**Error** Contain the latest copy of the task file error register.
7:0		STS	**Status**

Bit(s)	Mnemonic	Name	Description
			Contain the latest copy of the task file status register.

1A200124 PxSIG Port x Signature Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SIG															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIG															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		SIG	**Signature** Bits [31:24] - LBA High (Cylinder High) Register Bits [23:16] - LBA Mid (Cylinder Low) Register Bits [15:8] - LBA Low (Sector Number) Register Bits [7:0] - Sector Count Register

1A200128 PxSSTS Port x Serial ATA Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					IPM				SPD				DET			
Type					RO				RO				RO			
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8		IPM	**Interface Power Management** Indicates the current interface state. 0x0: Device not present or communication not established 0x1: Interface in active state 0x2: Interface in Partial power management state 0x6: Interface in Slumber power management state
7:4		SPD	**Current Interface Speed** Indicates the negotiated interface communication speed. 0x0: Device not present or communication not established 0x1: Gen. 1 communication rate negotiated 0x2: Gen. 2 communication rate negotiated 0x3: Gen. 3 communication rate negotiated
3:0		DET	**Device Detection** Indicates the interface device detection and Phy state. 0x0: No device detected and Phy communication not established 0x1: Device presence detected but Phy communication not established 0x3: Device presence detected and Phy communication established 0x4: Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode

1A20012C PxSCTL Port x Serial ATA Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					IPM				SPD				DET			
Type					RW				RW				RW			
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:8		IPM	**Interface Power Management Transitions Allowed** Indicates which power states the HBA is allowed to transition to. 0x0: No interface restrictions 0x1: Transitions to the Partial state disabled 0x2: Transitions to the Slumber state disabled 0x3: Transitions to both Partial and Slumber states disabled
7:4		SPD	**Speed Allowed** Indicates the highest allowable speed of the interface. 0x0: No speed negotiation restrictions 0x1: Limit speed negotiation to Gen. 1 communication rate 0x2: Limit speed negotiation to a rate not greater than Gen. 2 communication rate 0x3: Limit speed negotiation to a rate not greater than Gen. 3 communication rate
3:0		DET	**Device Detection Initialization** Controls the HBA's device detection and interface initialization. 0x0: No device detection or initialization action requested 0x1: Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. While this field is 0x1, COMRESET is transmitted on the interface. Software should leave the DET field set to 0x1 for a minimum of 1 ms to ensure that a COMRESET is sent on the interface.

Bit(s)	Mnemonic	Name	Description
			0x4: Disable the Serial ATA interface and put Phy in offline mode.

1A200130 PxSERR Port x Serial ATA Error Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						DIAG_X	DIAG_F	DIAG_T	DIAG_S	DIAG_H	DIAG_C	DIAG_D	DIAG_B	DIAG_W	DIAG_I	DIAG_N
Type						W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ERR_E	ERR_P	ERR_C	ERR_T							ERR_M	ERR_I
Type					W1C	W1C	W1C	W1C							W1C	W1C
Reset					0	0	0	0							0	0

Bit(s)	Mnemonic	Name	Description
26		DIAG_X	**Exchanged** Indicates that a change in device presence has been detected since the last time this bit was cleared. This bit is set to one when a COMINIT signal is received. This bit is reflected in the PxIS.PCS bit.
25		DIAG_F	**Unknown FIS Type** Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized/known and the length was less than or equal to 64bytes. When the Unknown FIS length exceeds 64 bytes, the DIAG_F bit is not set and the DIAG_T bit is set instead.
24		DIAG_T	**Transport State Transition Error** Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.
23		DIAG_S	**Link Sequence Error** Indicates that one or more Link state machine error conditions were encountered. The Link Layer state

Bit(s)	Mnemonic	Name	Description
			machine defines the conditions under which the link layer detects an erroneous transition.
22		DIAG_H	**Handshake Error** Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21		DIAG_C	**CRC Error** Indicates that one or more CRC errors occurred with the Link Layer.
20		DIAG_D	**Disparity Error** Indicates that one or more 10B to 8B coding/disparity errors occurred outside the data window. Set DBGCTL.SERR_DIAG_D_EN to enable this feature.
19		DIAG_B	**10B to 8B Decode Error** Indicates that one or more 10B to 8B decoding errors occurred.
18		DIAG_W	**Comm Wake** Indicates that a COMMWAKE signal was detected by the Phy.
17		DIAG_I	**PHY Internal Error** Indicates that the Phy detected some internal error.
16		DIAG_N	**PHY Ready Change** Indicates that the PhyRdy signal changed state. This bit is reflected in the PxIS.PRCS bit.
11		ERR_E	**Internal Error** Indicate one or more AMBA bus ERROR responses are detected on the master interface.
10		ERR_P	**Protocol Error** Any of the following conditions are detected. - Transport state transition error (DIAG_T) - Link sequence error (DIAG_S) - RX FIFO overflow

Bit(s)	Mnemonic	Name	Description
			- Link bad end error (WTRM instead of EOF is received).
9		ERR_C	**Persistent Communication or Data Integrity Error** A communication error that was not recovered occurred that is expected to be persistent.
8		ERR_T	**Transient Data Integrity Error** A data integrity error occurred that was not recovered by the interface.
1		ERR_M	**Recovered Communications Error** Communications between the device and host was temporarily lost but was re-established.
0		ERR_I	**Recovered Data Integrity Error** A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

1A200134 PxSACT Port x Serial ATA Active Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DS															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DS															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		DS	**Device Status** This field is bit significant. Each bit corresponds to the TAG and command slot of a native queued command, where bit 0 corresponds to TAG 0 and command slot 0. This field is set by software prior to issuing a native queued command for a particular command slot. Prior to writing PxCI[TAG] to '1', software will set DS[TAG] to '1' to indicate that a command with that TAG is

Bit(s)	Mnemonic	Name	Description
			outstanding. The device clears bits in this field by sending a Set Device Bits FIS to the host. The HBA clears bits in this field that are set to '1' in the SActive field of the Set Device Bits FIS. The HBA only clears bits that correspond to native queued commands that have completed successfully. Software should only write this field when PxCMD.ST is set to '1'. This field is cleared when PxCMD.ST is written from a '1' to a '0' by software. This field is not cleared by a COMRESET or software reset.

1A200138 PxCI Port x Command Issue Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CI															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CI															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CI	**Command Issued** This field is bit significant. Each bit corresponds to a command slot, where bit 0 corresponds to command slot 0. This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, DRQ, and ERR bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to '1' by software when PxCMD.ST is set to '1'. This field is also cleared when PxCMD.ST is written from a '1' to a '0' by software.

1A20013C PxSNTF Port x Serial ATA Notification Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PMN															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		PMN	**PM Notify** This field indicates whether a particular device with the corresponding PM Port number issued a Set Device Bits FIS to the host with the Notification bit set. PM Port 0h sets bit 0 ~ PM Port Fh sets bit 15 Individual bits are cleared by software writing 1's to the corresponding bit positions. This field is reset to default on a HBA Reset, but it is not reset by COMRESET or software reset.

1A200174 PxVS1 Port x Vendor Specific Register 0F000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PHY_RSTDA	PHY_RSTDA_INIT_EN			CFG_CDC				BIST_SYNC_EN	SUPP_FARAFE_EN	FAST_WDMA_EN	ABN_SDBF_EN			SPD_DET_EN	EXT_D102
Type	RW	RW			RW				RW	RW	RW	RW			RW	RW
Reset	0	0			1	1	1	1	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	EXT_D102															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31		PHY_RSTDA	**Reset PHYD+PHYA (pipe reset)** Active HIGH
30		PHY_RSTDA_INIT_EN	**Fix reset PHYD+PHYA (pipe reset)** Active HIGH
27:24		CFG_CDC	**Fix CDC Issues Enable**
23		BIST_SYNC_EN	**BIST Sync Enable** Change default primitive from ALIGNp to SYNCp in BIST mode 0: ALIGNp 1: SYNCp
22		SUPP_FARAFE_EN	**Support Far-end AFE Enable** Response R_OKp or R_ERRp when receiving BIST-FFIS 0: R_ERRp (not support) 1: R_OKp (support)
21		FAST_WDMA_EN	**Enhance WDMA Enable** Send X_RDYp of DFIS as early as possible 0: Normal mode 1: Early send X_RDYp of DFIS
20		ABN_SDBF_EN	**Abnormal SDB FIS Enable** Accept non-spec. SDB FIS before receiving signature 0: Normal mode (hang up) 1: Accept SDB FIS before signature
17		SPD_DET_EN	**Speed Detect Enable** Co-work with PHY to use transition density detection during speed negotiation

Bit(s)	Mnemonic	Name	Description
			0: Normal mode 1: Transition density detection mode
16:0		EXT_D102	**An Extend D10.2 Counter** Use for I_SEND_D10_2 state in TX initialization state machine to extend the time of D10.2

3 Ethernet Subsys

3.1 Frame Engine (FE)

3.1.1 Introduction

Frame engine is a high-performance network processing engine for network protocol layer 2 to layer 4, provides a DMA interface to transfer Ethernet packets between CPU and GMACs. Frame engine includes PDAM, QDMA, PSE, PPE, GDM, and CDM.

3.1.2 Features

The main features of these functions are list below.

- Frame engine with PPE, PDMA and QDMA that connects to DRAM via AXI bus (64-bit)
- IPv4 routing, NAT
- IPv6 routing, DS-lite, 6RD, 6to4
- QOS
- IP/TCP/UDP checksum offload
- TSO (TCP segmentation offload)
- LRO (Larger receive offload)

3.1.2.1 PSE Features

- Wire-speed (2.5Gbps) Ethernet LAN/WAN NAT/NAPT routing
- Egress rate limiting/shaping (by GDM)
- Flow control for no-packet-loss guarantee
- Emulated multicast support for keep-alive (can mirror a Tx packet to CPU)
- IP/TCP/UDP Checksum offload (by GDM)
- IP/TCP/UDP Checksum Generation (by CDM)
- VLAN & PPPOE header insertion (by CDM)
- TCP Segmentation Offload (by CDM)
- Auto-Padding for sub-64 B packets

3.1.2.2 PPE Features

- IPV4 NAT/NAPT, ipv6 Routing and Tunnel IP (DS-Lite, 6RD)
- 1/2/4/8/16 K flows
- Virtual server, port-triggering & port forwarding
- All types of IPV4 NAT(NAPT, Twice NAT)
- All types of MAC/VLAN/PPPOE/IP/TCP/UDP binding
- 4 VLAN tagging (Q-in-Q)
- VID Swapping
- Support for 65536 PPPOE sessions
- PPPOE pass-through
- Cone-NAT, port-restricted NAT & Symmetric NAT

- Per flow accounting or rate limiting
- DDOS avoidance by rate limiting
- Stateful packet filtering (SPI)
- Patent-pending flow offloading technology for flexible/high performance packet L3/L4 packet processing.
- Multi-WAN load balancing with hardware and software cooperation
- QoS for multimedia traffic
- Within 16 flows, 2 Gbps wire-speed is supported for any packet size.
- Per flow MIB

NOTE: All PPE features mentioned above require software porting to function.

3.1.2.3 PDMA/ADMA Features

- Supports 4 Tx descriptor rings and 4 Rx descriptor rings
- Scatter/Gather DMA
- Delayed interrupt
- Configurable 4/8/16/32 32-bit word burst length
- Support LRO(Large Receive Offload) with 1 normal RX ring and 3 LRO RX ring
- Support TSO(TCP Segmentation Offload)

3.1.2.4 QDMA Features

- Supports 1 Tx descriptor link list from software
- Supports directly Tx packet hardware forwarding from PPE
- Supports 2 Rx descriptor rings
- Configurable 4/8/16/32 32-bit word burst length
- Delayed interrupt
- Supports 64 Tx queues
- Per Tx queue forward/drop packet accounting
- Per Tx queue forward byte accounting
- Per Tx queue minimum/maximum rate control
- Strict priority arbitration between 64 Tx queues, for under MIN rate traffic
- Either Strict priority or Round-robin arbitration between 64 Tx queues, for over MIN rate traffic
- 64 Tx queues can be separated into 2 scheduling group
- Supports Random Early Drop with configurable dropping probability
- 8 Tx queues support SFQ and DRR scheduling, with virtual queue capability
- Supports up to 1024 virtual queues, those are shared by 8 Tx queues
- Supports SFQ/DRR hash perturb
- Per virtual queue forward packet/byte and drop packet accounting

3.1.3 Register Definition

Module name: FE Base address: (+1b100000h)

Address	Name	Width	Register Function
1B100000	FE_GLO_CFG	32	Frame Engine Global Configuration
1B100004	FE_RST_GLO	32	Frame Engine Global Reset
1B100008	FE_INT_STATUS	32	Frame Engine Interrupt Status
1B10000C	FE_INT_ENABLE	32	Frame Engine Interrupt Enable
1B100010	FE_FOE_TS_T	32	Frame Engine Time Stamp
1B100014	FE_IPV6_EXT	32	Frame Engine IPv6 Extension Header
1B100018	FE_RATE_COMP	32	Frame Engine Rate Limit Compensation
1B100020	FE_INT_GRP	32	Frame Engine Interrupt Group
1B100100	PSE_FQFC_CFG	32	PSE Free Queue Flow Control
1B100108	PSE_IQ_REV1	32	PSE Input Queue Reservation-I
1B10010C	PSE_IQ_REV2	32	PSE Input Queue Reservation-II
1B100110	PSE_IQ_STA1	32	PSE Input Queue Status-I
1B100114	PSE_IQ_STA2	32	PSE Input Queue Status-II
1B100118	PSE_OQ_STA1	32	PSE Output Queue Status-I
1B10011C	PSE_OQ_STA2	32	PSE Output Queue Status-II
1B100128	PSE_OQ_TH1	32	PSE Output Queue Threshold-I
1B10012C	PSE_OQ_TH2	32	PSE Output Queue Threshold-II
1B100130	FE_GDM_RXID1	32	FE GDM RXID Control 1
1B100134	FE_GDM_RXID2	32	FE GDM RXID Control 2
1B100240	FE_PSE_FREE	32	PSE Free Page Count
1B100244	FE_DROP_FQ	32	FE Packet Drop by Free Queue
1B100248	FE_DROP_FC	32	FE Packet Drop by Flow Control
1B10024C	FE_DROP_PPE	32	FE Packet Drop by PPE
1B100400	CDMP_IG_CTRL	32	CDM Ingress Control
1B100404	CDMP_EG_CTRL	32	CDM Egress Control
1B100408	CDMP_PPE_GEN	32	CDM PPPoE Generation
1B100500	GDM1_IG_CTRL	32	GDM Ingress Control
1B100504	GDM1_EG_CTRL	32	GDM Egress Control
1B100508	GDM1_MAC_LSB	32	GDM MY_MAC Address LSB
1B10050C	GDM1_MAC_MSB	32	GDM MY_MAC Address MSB
1B100510	GDM1_VLAN_GEN	32	GDM VLAN Generation
1B100800	TX_BASE_PTR_0	32	TX Ring #0 Base Pointer
1B100804	TX_MAX_CNT_0	32	TX Ring #0 Maximum Count
1B100808	TX_CTX_IDX_0	32	TX Ring #0 CPU pointer
1B10080C	TX_DTX_IDX_0	32	TX Ring #0 DMA pointer
1B100810	TX_BASE_PTR_1	32	TX Ring #1 Base Pointer
1B100814	TX_MAX_CNT_1	32	TX Ring #1 Maximum Count
1B100818	TX_CTX_IDX_1	32	TX Ring #1 CPU pointer
1B10081C	TX_DTX_IDX_1	32	TX Ring #1 DMA pointer
1B100820	TX_BASE_PTR_2	32	TX Ring #2 Base Pointer
1B100824	TX_MAX_CNT_2	32	TX Ring #2 Maximum Count
1B100828	TX_CTX_IDX_2	32	TX Ring #2 CPU pointer
1B10082C	TX_DTX_IDX_2	32	TX Ring #2 DMA pointer
1B100830	TX_BASE_PTR_3	32	TX Ring #3 Base Pointer
1B100834	TX_MAX_CNT_3	32	TX Ring #3 Maximum Count

Address	Name	Width	Register Function
1B100838	TX_CTX_IDX_3	32	TX Ring #3 CPU pointer
1B10083C	TX_DTX_IDX_3	32	TX Ring #3 DMA pointer
1B100900	RX_BASE_PTR_0	32	RX Ring #0 Base Pointer
1B100904	RX_MAX_CNT_0	32	RX Ring #0 Maximum Count
1B100908	RX_CRX_IDX_0	32	RX Ring #0 CPU pointer
1B10090C	RX_DRX_IDX_0	32	RX Ring #0 DMA pointer
1B100910	RX_BASE_PTR_1	32	RX Ring #1 Base Pointer
1B100914	RX_MAX_CNT_1	32	RX Ring #1 Maximum Count
1B100918	RX_CRX_IDX_1	32	RX Ring #1 CPU pointer
1B10091C	RX_DRX_IDX_1	32	RX Ring #1 DMA pointer
1B100920	RX_BASE_PTR_2	32	RX Ring #2 Base Pointer
1B100924	RX_MAX_CNT_2	32	RX Ring #2 Maximum Count
1B100928	RX_CRX_IDX_2	32	RX Ring #2 CPU pointer
1B10092C	RX_DRX_IDX_2	32	RX Ring #2 DMA pointer
1B100930	RX_BASE_PTR_3	32	RX Ring #3 Base Pointer
1B100934	RX_MAX_CNT_3	32	RX Ring #3 Maximum Count
1B100938	RX_CRX_IDX_3	32	RX Ring #3 CPU pointer
1B10093C	RX_DRX_IDX_3	32	RX Ring #3 DMA pointer
1B100A00	PDMA_INFO	32	PDMA Information
1B100A04	PDMA_GLO_CFG	32	PDMA Global Configuration
1B100A08	PDMA_RST_IDX	32	PDMA Reset Index
1B100A0C	DELAY_INT_CFG	32	Delay Interrupt Configuration
1B100A10	FREEQ_THRES	32	Free Queue Threshold
1B100A20	INT_STATUS	32	Interrupt Status
1B100A28	INT_MASK	32	Interrupt Mask
1B100A40	PDMA_INT1_VEC_GRP0	32	PDMA Interrupt Status Group 0
1B100A44	PDMA_INT1_VEC_GRP1	32	PDMA Interrupt Status Group 1
1B100A48	PDMA_INT1_VEC_GRP2	32	PDMA Interrupt Status Group 2
1B100A50	PDMA_INT_GRP1	32	PDMA Interrupt Group 1 Control
1B100A54	PDMA_INT_GRP2	32	PDMA Interrupt Group 2 Control
1B100A80	SCH_Q01_CFG	32	Scheduler Configuration for Q0&Q1
1B100A84	SCH_Q23_CFG	32	Scheduler Configuration for Q2&Q3
1B101400	CDMQ_IG_CTRL	32	CDM VLAN Control
1B101404	CDMQ_EG_CTRL	32	CDM Egress Control
1B101408	CDMQ_PPP_GEN	32	CDM PPPoE Generation
1B101500	GDM2_IG_CTRL	32	GDM Ingress Control
1B101504	GDM2_EG_CTRL	32	GDM Egress Control
1B101508	GDM2_MAC_LSB	32	GDM MY_MAC Address LSB
1B10150C	GDM2_MAC_MSB	32	GDM MY_MAC Address MSB
1B101510	GDM2_VLAN_GEN	32	GDM VLAN Generation
1B101514	GDM2_FILTER_CRTL	32	GDM Filter Control
1B101518	GDM2_VIDF01	32	GDM VID Filter Control 01
1B10151C	GDM2_VIDF23	32	GDM VID Filter Control 23

Address	Name	Width	Register Function
1B101600	CDMW_IG_CTRL	32	CDM VLAN Control
1B101604	CDMW_EG_CTRL	32	CDM Egress Control
1B101608	CDMW_PPP_GEN	32	CDM PPPoE Generation
1B101800	QTX_CFG_0	32	TX Queue #0, #(16 * n) Configuration
1B101804	QTX_SCH_0	32	TX Queue #0, #(16 * n) Schedule
1B101808	QTX_HEAD_0	32	TX Queue #0, #(16 * n) Head Pointer
1B10180C	QTX_TAIL_0	32	TX Queue #0, #(16 * n) Tail Pointer
1B101810	QTX_CFG_1	32	TX Queue #1, #(16 * n + 1) Configuration
1B101814	QTX_SCH_1	32	TX Queue #1, #(16 * n + 1) Schedule
1B101818	QTX_HEAD_1	32	TX Queue #1, #(16 * n + 1) Head Pointer
1B10181C	QTX_TAIL_1	32	TX Queue #1, #(16 * n + 1) Tail Pointer
1B101820	QTX_CFG_2	32	TX Queue #2, #(16 * n + 2) Configuration
1B101824	QTX_SCH_2	32	TX Queue #2, #(16 * n + 2) Schedule
1B101828	QTX_HEAD_2	32	TX Queue #2, #(16 * n + 2) Head Pointer
1B10182C	QTX_TAIL_2	32	TX Queue #2, #(16 * n + 2) Tail Pointer
1B101830	QTX_CFG_3	32	TX Queue #3, #(16 * n + 3) Configuration
1B101834	QTX_SCH_3	32	TX Queue #3, #(16 * n + 3) Schedule
1B101838	QTX_HEAD_3	32	TX Queue #3, #(16 * n + 3) Head Pointer
1B10183C	QTX_TAIL_3	32	TX Queue #3, #(16 * n + 3) Tail Pointer
1B101840	QTX_CFG_4	32	TX Queue #4, #(16 * n + 4) Configuration
1B101844	QTX_SCH_4	32	TX Queue #4, #(16 * n + 4) Schedule
1B101848	QTX_HEAD_4	32	TX Queue #4, #(16 * n + 4) Head Pointer
1B10184C	QTX_TAIL_4	32	TX Queue #4, #(16 * n + 4) Tail Pointer
1B101850	QTX_CFG_5	32	TX Queue #5, #(16 * n + 5) Configuration
1B101854	QTX_SCH_5	32	TX Queue #5, #(16 * n + 5) Schedule
1B101858	QTX_HEAD_5	32	TX Queue #5, #(16 * n + 5) Head Pointer
1B10185C	QTX_TAIL_5	32	TX Queue #5, #(16 * n + 5) Tail Pointer
1B101860	QTX_CFG_6	32	TX Queue #6, #(16 * n + 6) Configuration
1B101864	QTX_SCH_6	32	TX Queue #6, #(16 * n + 6) Schedule
1B101868	QTX_HEAD_6	32	TX Queue #6, #(16 * n + 6) Head Pointer
1B10186C	QTX_TAIL_6	32	TX Queue #6, #(16 * n + 6) Tail Pointer
1B101870	QTX_CFG_7	32	TX Queue #7, #(16 * n + 7) Configuration
1B101874	QTX_SCH_7	32	TX Queue #7, #(16 * n + 7) Schedule
1B101878	QTX_HEAD_7	32	TX Queue #7, #(16 * n + 7) Head Pointer
1B10187C	QTX_TAIL_7	32	TX Queue #7, #(16 * n + 7) Tail Pointer
1B101880	QTX_CFG_8	32	TX Queue #8, #(16 * n + 8) Configuration
1B101884	QTX_SCH_8	32	TX Queue #8, #(16 * n + 8) Schedule
1B101888	QTX_HEAD_8	32	TX Queue #8, #(16 * n + 8) Head Pointer
1B10188C	QTX_TAIL_8	32	TX Queue #8, #(16 * n + 8) Tail Pointer
1B101890	QTX_CFG_9	32	TX Queue #9, #(16 * n + 9) Configuration
1B101894	QTX_SCH_9	32	TX Queue #9, #(16 * n + 9) Schedule
1B101898	QTX_HEAD_9	32	TX Queue #9, #(16 * n + 9) Head Pointer
1B10189C	QTX_TAIL_9	32	TX Queue #9, #(16 * n + 9) Tail Pointer
1B1018A0	QTX_CFG_10	32	TX Queue #10, #(16 * n + 10) Configuration
1B1018A4	QTX_SCH_10	32	TX Queue #10, #(16 * n + 10) Schedule

Address	Name	Width	Register Function
1B1018A8	QTX_HEAD_10	32	TX Queue #10, #(16 * n + 10) Head Pointer
1B1018AC	QTX_TAIL_10	32	TX Queue #10, #(16 * n + 10) Tail Pointer
1B1018B0	QTX_CFG_11	32	TX Queue #11, #(16 * n + 11) Configuration
1B1018B4	QTX_SCH_11	32	TX Queue #11, #(16 * n + 11) Schedule
1B1018B8	QTX_HEAD_11	32	TX Queue #11, #(16 * n + 11) Head Pointer
1B1018BC	QTX_TAIL_11	32	TX Queue #11, #(16 * n + 11) Tail Pointer
1B1018C0	QTX_CFG_12	32	TX Queue #12, #(16 * n + 12) Configuration
1B1018C4	QTX_SCH_12	32	TX Queue #12, #(16 * n + 12) Schedule
1B1018C8	QTX_HEAD_12	32	TX Queue #12, #(16 * n + 12) Head Pointer
1B1018CC	QTX_TAIL_12	32	TX Queue #12, #(16 * n + 12) Tail Pointer
1B1018D0	QTX_CFG_13	32	TX Queue #13, #(16 * n + 13) Configuration
1B1018D4	QTX_SCH_13	32	TX Queue #13, #(16 * n + 13) Schedule
1B1018D8	QTX_HEAD_13	32	TX Queue #13, #(16 * n + 13) Head Pointer
1B1018DC	QTX_TAIL_13	32	TX Queue #13, #(16 * n + 13) Tail Pointer
1B1018E0	QTX_CFG_14	32	TX Queue #14, #(16 * n + 14) Configuration
1B1018E4	QTX_SCH_14	32	TX Queue #14, #(16 * n + 14) Schedule
1B1018E8	QTX_HEAD_14	32	TX Queue #14, #(16 * n + 14) Head Pointer
1B1018EC	QTX_TAIL_14	32	TX Queue #14, #(16 * n + 14) Tail Pointer
1B1018F0	QTX_CFG_15	32	TX Queue #15, #(16 * n + 15) Configuration
1B1018F4	QTX_SCH_15	32	TX Queue #15, #(16 * n + 15) Schedule
1B1018F8	QTX_HEAD_15	32	TX Queue #15, #(16 * n + 15) Head Pointer
1B1018FC	QTX_TAIL_15	32	TX Queue #15, #(16 * n + 15) Tail Pointer
1B101900	QRX_BASE_PTR_0	32	RX Ring #0 Base Pointer
1B101904	QRX_MAX_CNT_0	32	RX Ring #0 Maximum Count
1B101908	QRX_CRX_IDX_0	32	RX Ring #0 CPU pointer
1B10190C	QRX_DRX_IDX_0	32	RX Ring #0 DMA pointer
1B101980	VQTX_TB_BASE_0	32	TX Virtual Queue Table #0 Base Address
1B101984	VQTX_TB_BASE_1	32	TX Virtual Queue Table #1 Base Address
1B101988	VQTX_TB_BASE_2	32	TX Virtual Queue Table #2 Base Address
1B10198C	VQTX_TB_BASE_3	32	TX Virtual Queue Table #3 Base Address
1B101990	VQTX_TB_BASE_4	32	TX Virtual Queue Table #4 Base Address
1B101994	VQTX_TB_BASE_5	32	TX Virtual Queue Table #5 Base Address
1B101998	VQTX_TB_BASE_6	32	TX Virtual Queue Table #6 Base Address
1B10199C	VQTX_TB_BASE_7	32	TX Virtual Queue Table #7 Base Address
1B1019F0	QDMA_PAGE	32	QDMA Configuration Page
1B101A00	QDMA_INFO	32	QDMA Information
1B101A04	QDMA_GLO_CFG	32	QDMA Global Configuration
1B101A08	QDMA_RST_IDX	32	QDMA Reset Index
1B101A0C	QDMA_DELAY_INT	32	Delay Interrupt Configuration
1B101A10	QDMA_FC_THRES	32	Flow Control Threshold
1B101A14	QDMA_TX_SCH	32	TX Scheduler Rate Control
1B101A18	QDMA_INT_STS	32	Interrupt Status
1B101A1C	QDMA_INT_MASK	32	Interrupt Mask
1B101A20	QDMA_INT_GRP1	32	QDMA Interrupt Group 1 Control
1B101A24	QDMA_INT_GRP2	32	QDMA Interrupt Group 2 Control

Address	Name	Width	Register Function
1B101A2C	QDMA_DROP_PREC	32	QDMA Drop by FFA Percentage Control
1B101A40	QDMA_HRED1	32	QDMA HW RED Distribution - I
1B101A44	QDMA_HRED2	32	QDMA HW RED Distribution - II
1B101A48	QDMA_SRED1	32	QDMA SW RED Distribution - I
1B101A4C	QDMA_SRED2	32	QDMA SW RED Distribution - II
1B101A70	QDMA_INT_STS_G0	32	QDMA Interrupt Status Group 0
1B101A74	QDMA_INT_STS_G1	32	QDMA Interrupt Status Group 1
1B101A78	QDMA_INT_STS_G2	32	QDMA Interrupt Status Group 2
1B101A80	VQTX_GLO	32	TX Virtual Queue Global Configuration
1B101A8C	VQTX_INVLD_PTR	32	TX Virtual Queue Invalid Pointer
1B101A90	VQTX_NUM	32	Number of TX Virtual Queue Configuration
1B101A98	VQTX_SCH	32	TX Virtual Queue Schedule Configuration
1B101AA0	VQTX_HASH_CFG	32	TX Virtual Queue Hash Configuration
1B101AA4	VQTX_HASH_SD	32	TX Virtual Queue Hash Seed
1B101AB0	VQTX_VLD_CFG	32	TX Virtual Queue Valid Configuration
1B101ABC	QTX_MIB_IF	32	TX Queue MIB Interface
1B101AC0	VQTX_MIB_PCNT	32	TX Virtual Queue MIB Packet Count
1B101AC4	VQTX_MIB_BCNTL	32	TX Virtual Queue MIB Byte Count Low Bytes
1B101AC8	VQTX_MIB_BCNTH	32	TX Virtual Queue MIB Byte Count High Bytes
1B101ACC	VQTX_MIB_DPCNT	32	TX Virtual Queue MIB Drop Packet Count
1B101AD0	QTX_MIB_PCNT	32	TX Physical Queue MIB Forward Packet Count
1B101AD4	QTX_MIB_DPCNT	32	TX Physical Queue MIB Dropped Packet Count
1B101AD8	QTX_MIB_BCNTL	32	TX Physical Queue MIB Byte Count Low Bytes
1B101ADC	QTX_MIB_BCNTH	32	TX Physical Queue MIB Byte Count High Bytes
1B101B00	QTX_CTX_PTR	32	TX Forward CPU Pointer
1B101B04	QTX_DTX_PTR	32	TX Forward DMA Pointer
1B101B08	QTX_FWD_CNT	32	TX Forward DMA Counter
1B101B10	QTX_CRX_PTR	32	TX Release CPU Pointer
1B101B14	QTX_DRX_PTR	32	TX Release DMA Pointer
1B101B18	QTX_RLS_CNT	32	TX Release DMA Counter
1B101B20	QDMA_FQ_HEAD	32	Free Page Head Pointer
1B101B24	QDMA_FQ_TAIL	32	Free Page Tail Pointer
1B101B28	QDMA_FQ_CNT	32	Free Page Counter
1B101B2C	QDMA_FQ_BLEN	32	Free Page Buffer Length
1B101BC0	VQTX_0_3_BIND_QID	32	QDMA Virtual Queue Group #0~3 to Physical Queue Binding
1B101BC4	VQTX_4_7_BIND_QID	32	QDMA Virtual Queue Group #4~7 to Physical Queue Binding
1B101BE0	QTX_FC_SW_STS_0_31	32	Tx Queue#0~31 Software Path Flow Control Status

Address	Name	Width	Register Function
1B101BE4	QTX_FC_SW_STS_32_63	32	Tx Queue#32~63 Software Path Flow Control Status

1B100000 FE_GLO_CFG Frame Engine Global Configuration 810000B0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EXT_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LINK_DWN								L2_SPACE				INF_SPACE			
Type	RW								RW				RW			
Reset	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31:16	EXT_TPID	**Extended VLAN TPID** User-defined TPID except for 0x8100, 0x88a8. [note] This TPID field is used by CDM/GDM RX direction.
15:8	LINK_DWN	**Disable PSE Port** When PSE port is not valid on the Frame Engine, user is suggested to disable the corresponding port.
7:4	L2_SPACE	**L2 space** The space unit is 8 bytes.
3:0	INF_SPACE	**PKT_INFO space** The space unit is 8 bytes. [Note1*] Per received packet has already occupied 8 bytes (1 unit) by default. The actual PKT_INFO space is equal to (INF_SPACE + 1) [Note2*] (L2_SPACE + INF_SPACE + 1) <= 0xF

1B100004 FE_RST_GLO Frame Engine Global Reset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV0													PSE_RAM	PSE_MEM_EN	PSE_RESET
Type	RO													RW	RW	W1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:3	RESV0	**Reserved**
2	PSE_RAM	**PSE accessible RAM mode** [note*1] when this bit is reset, PSE packet memory is only accessible by Pbus (0xA000~0xDFFF). [note*2] when this bit is set, PSE packet memory is only accessible by Pbus (0x8000~0xDFFF) 0: Only 8KB PSE memory is left for iNIC initialization. 1: Make the whole PSE memory be used for Pbus access
1	PSE_MEM_EN	**PSE access enable**

Bit(s)	Name	Description
0	PSE_RESET	0: disable 1: Enable PSE memory is accessible by PBUs **PSE soft reset (self-cleared)** [note*1] Whenever SW set this bit, PSE will be initialized again and enter the normal mode. 0: invalid 1: Write 1 to reset PSE

1B100008 FE_INT_STATUS Frame Engine Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PPE_AF	REV0	GDM2_AF	GDM1_AF	REV1		MAC2_LINK	MAC1_LINK	GDM2_ERR	GDM2_CRC	GDM1_ERR	GDM1_CRC	RFIFO_UF	RFIFO_OV	INFIFO_GET_ERR	AFIFO_GET_ERR
Type	W1C	RO	W1C	W1C	RO		W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	CDM_TSO_ALIGN	CDM_TSO_ILLEGAL	CDM_TSO_FAIL	REV3		PSE_DROP	FQ_EMPTY	PSE_FC_ON							
Type	RO	W1C	W1C	W1C	RO		W1C	W1C	W1C							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PPE_AF	**MIB counter is almost full on PPE**
30	REV0	**Reserved**
29	GDM2_AF	**MIB counter is almost full on GDM2**
28	GDM1_AF	**MIB counter is almost full on GDM1**
27:26	REV1	**Reserved**
25	MAC2_LINK	**Link Status Change on MAC2**
24	MAC1_LINK	**Link Status Change on MAC1**
23	GDM2_ERR	**Packet error (checksum, length, etc.) on GDM2** Including FIFO overflow, checksum error, undersize, oversize
22	GDM2_CRC	**Packet CRC error on GDM2**
21	GDM1_ERR	**Packet error (checksum, length, etc.) on GDM1** Including FIFO overflow, checksum error, undersize, oversize
20	GDM1_CRC	**Packet CRC error on GDM1**
19	RFIFO_UF	**Ring FIFO Underrun Defect**
18	RFIFO_OV	**Ring FIFO Overflow Defect**
17	INFIFO_GET_ERR	**IN FIFO Get Defect**
16	AFIFO_GET_ERR	**ASYNC FIFO Get Defect**
15	REV2	**Reserved**
14	CDM_TSO_ALIGN	**Detect EOF Alignment**
13	CDM_TSO_ILLEGAL	**Ignored illegal packet on CDM TSO**
12	CDM_TSO_FAIL	**TSO Fail on CDM**
11:10	REV3	**Reserved**
9	PSE_DROP	**Packet drop by PSE**
8	FQ_EMPTY	**PSE free queue is empty**
7:0	PSE_FC_ON	**PSE PORT flow control is asserted** PSE port[n] enables the flow control.

1B10000C FE_INT_ENABLE Frame Engine Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PPE_AF	REV0	GDM2_AF	GDM1_AF	REV1		MAC2_LINK	MAC1_LINK	GDM2_ERR	GDM2_CRC	GDM1_ERR	GDM1_CRC	RFIFO_UF	RFIFO_OV	INFIFO_GET_ERR	AFIFO_GET_ERR
Type	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	CDM_TSO_ALIGN	CDM_TSO_ILLEGAL	CDM_TSO_FAIL	REV3		PSE_DROP	FQ_EMPTY	PSE_FC_ON							
Type	RW	RW	RW	RW	RW		RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PPE_AF	
30	REV0	
29	GDM2_AF	
28	GDM1_AF	
27:26	REV1	
25	MAC2_LINK	
24	MAC1_LINK	
23	GDM2_ERR	
22	GDM2_CRC	
21	GDM1_ERR	
20	GDM1_CRC	
19	RFIFO_UF	
18	RFIFO_OV	
17	INFIFO_GET_ERR	
16	AFIFO_GET_ERR	
15	REV2	
14	CDM_TSO_ALIGN	
13	CDM_TSO_ILLEGAL	
12	CDM_TSO_FAIL	
11:10	REV3	
9	PSE_DROP	
8	FQ_EMPTY	
7:0	PSE_FC_ON	

1B100010 FE_FOE_TS_T Frame Engine Time Stamp 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FOE_TS_T															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RESV0	**Reserved**
15:0	FOE_TS_T	**Time stamp** Time stamp unit is 1 sec. [Note] This timer is driven by free-running 125MHz clock

Bit(s)	Name	Description

1B100014 FE_IPV6_EXT Frame Engine IPv6 Extension Header 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IP6_EXT3								IP6_EXT2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IP6_EXT1								IP6_EXT0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	IP6_EXT3	**IPv6 extension header #3**
23:16	IP6_EXT2	**IPv6 extension header #2**
15:8	IP6_EXT1	**IPv6 extension header #1**
7:0	IP6_EXT0	**IPv6 extension header #0**

1B100018 FE_RATE_COMP Frame Engine Rate Limit Compensation 00001818

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_RATE_MINUS	DMA_RATE_BYTE							PSE_RATE_MINUS	PSE_RATE_BYTE						
Type	RW	RW							RW	RW						
Reset	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0

Bit(s)	Name	Description
31:16	REV0	**Reserved**
15	DMA_RATE_MINUS	1'b0 : a specific byte count is added to the frame length according to FE_GLO_CFG.RATE_BYTE 1'b1: a specific byte count is subtracted from the incoming frame length.
14:8	DMA_RATE_BYTE	**Byte number for rate control** The byte number should be subtracted while calculating the rate limit.
7	PSE_RATE_MINUS	1'b0 : a specific byte count is added to the frame length according to FE_GLO_CFG.RATE_BYTE 1'b1: a specific byte count is subtracted from the incoming frame length.
6:0	PSE_RATE_BYTE	**Byte number for rate control** The byte number should be subtracted while calculating the rate limit.

1B100020 FE_INT_GRP Frame Engine Interrupt Group 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_G2_ASG				QDMA_INT_G1_ASG				QDMA_INT_Go_ASG				PDMA_INT_G2_ASG			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PDMA_INT_G1_ASG				PDMA_INT_Go_ASG								FE_MISC_INT_ASG			
Type	RW				RW								RW			
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
31:28	QDMA_INT_G2_ASG	**QDMA group 2 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] Others: Reserved
27:24	QDMA_INT_G1_ASG	**QDMA group 1 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] Others: Reserved
23:20	QDMA_INT_Go_ASG	**QDMA group 0 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] Others: Reserved
19:16	PDMA_INT_G2_ASG	**PDMA group 2 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] Others: Reserved
15:12	PDMA_INT_G1_ASG	**PDMA group 1 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] Others: Reserved
11:8	PDMA_INT_Go_ASG	**PDMA group 0 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] Others: Reserved
3:0	FE_MISC_INT_ASG	**Frame engine misc. interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] Others: Reserved

1B100100 PSE_FQFC_CFG PSE Free Queue Flow Control FFFF9070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FQ_PCNT								FQ_MAX_PCNT							
Type	RO								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	FQ_HIGH								FQ_LOW							
Type	RW								RW							
Reset	1	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0

Bit(s)	Name	Description
31:24	FQ_PCNT	**Free queue page count**
23:16	FQ_MAX_PCNT	**Maximum free Q page count.** Please reset PSE after re-programming this register
15:8	FQ_HIGH	**Free Buffer Count High Threshold** When the free buffer count is higher than this threshold, PSE will disable the flow control mechanism.
7:0	FQ_LOW	**Free Buffer Count Low Threshold** When the free buffer count is lower than this threshold, PSE engine will check the ingress buffer reservation and the egress queue depth.

1B100108 PSE_IQ_REV1 PSE Input Queue Reservation-I 080C0C08

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P3_IQ_RES								P2_IQ_RES							
Type	RW								RW							
Reset	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_IQ_RES								P0_IQ_RES							
Type	RW								RW							
Reset	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:24	P3_IQ_RES	**Virtual input Q reservation** [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
23:16	P2_IQ_RES	**Virtual input Q reservation** [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
15:8	P1_IQ_RES	**Virtual input Q reservation** [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
7:0	P0_IQ_RES	**Virtual input Q reservation** [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

1B10010C PSE_IQ_REV2 PSE Input Queue Reservation-II 100808FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FREE_DROP								P6_IQ_RES							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5_IQ_RES								REVo							
Type	RW								RW							
Reset	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FREE_DROP	**Free Buffer Drop Threshold**
23:16	P6_IQ_RES	**Virtual input Q reservation** [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
15:8	P5_IQ_RES	**Virtual input Q reservation** [note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
7:0	REV0	**Reserved**

1B100110 PSE_IQ_STA1 PSE Input Queue Status-I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P3_IQ_PCNT								P2_IQ_PCNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_IQ_PCNT								P0_IQ_PCNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	P3_IQ_PCNT	**Virtual input Q page count**
23:16	P2_IQ_PCNT	**Virtual input Q page count**
15:8	P1_IQ_PCNT	**Virtual input Q page count**
7:0	P0_IQ_PCNT	**Virtual input Q page count**

1B100114 PSE_IQ_STA2 PSE Input Queue Status-II 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								P6_IQ_PCNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5_IQ_PCNT								REV1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:16	P6_IQ_PCNT	**Virtual input Q page count**
15:8	P5_IQ_PCNT	**Virtual input Q page count**
7:0	REV1	**Reserved**

1B100118 PSE_OQ_STA1 PSE Output Queue Status-I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P3_OQ_PCNT								P2_OQ_PCNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_OQ_PCNT								P0_OQ_PCNT							

Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	P3_OQ_PCNT	**Output Q page count**
23:16	P2_OQ_PCNT	**Output Q page count**
15:8	P1_OQ_PCNT	**Output Q page count**
7:0	P0_OQ_PCNT	**Output Q page count**

1B10011C PSE_OQ_STA2 PSE Output Queue Status-II 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVo								P6_OQ_PCNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5_OQ_PCNT								PPE_PCNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REVo	**Reserved**
23:16	P6_OQ_PCNT	**Output Q page count**
15:8	P5_OQ_PCNT	**Output Q page count**
7:0	PPE_PCNT	**PPE Queue page count**

1B100128 PSE_OQ_TH1 PSE Output Queue Threshold-I 20303020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P3_OQ_TH								P2_OQ_TH							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_OQ_TH								P0_OQ_TH							
Type	RW								RW							
Reset	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:24	P3_OQ_TH	**Output Queue FC Threshold** [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
23:16	P2_OQ_TH	**Output Queue FC Threshold** [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
15:8	P1_OQ_TH	**Output Queue FC Threshold** [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
7:0	P0_OQ_TH	**Output Queue FC Threshold** [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

1B10012C PSE_OQ_TH2 PSE Output Queue Threshold-II 002020FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								P6_OQ_TH							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5_OQ_TH								REV1							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:16	P6_OQ_TH	**Output Queue FC Threshold** [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
15:8	P5_OQ_TH	**Output Queue FC Threshold** [note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
7:0	REV1	**Reserved**

1B100130 FE_GDM_RXID1 FE GDM RXID Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_VLAN_PRI7_RXID_SEL		GDM_VLAN_PRI6_RXID_SEL		GDM_VLAN_PRI5_RXID_SEL		GDM_VLAN_PRI4_RXID_SEL		GDM_VLAN_PRI3_RXID_SEL		GDM_VLAN_PRI2_RXID_SEL		GDM_VLAN_PRI1_RXID_SEL		GDM_VLAN_PRI0_RXID_SEL	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GDM_TCP_ACK_RXID_SEL		GDM_TCP_ACK_WZPC	GDM_RXID_PRI_SEL		
Type											RW		RW	RW		
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
31:30	GDM_VLAN_PRI7_RXID_SEL	**GDM RXID Select for VLAN Priority = 7** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
29:28	GDM_VLAN_PRI6_RXID_SEL	**GDM RXID Select for VLAN Priority = 6** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
27:26	GDM_VLAN_PRI5_RXID_SEL	**GDM RXID Select for VLAN Priority = 5** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
25:24	GDM_VLAN_PRI4_RXID_SEL	**GDM RXID Select for VLAN Priority = 4**

Bit(s)	Name	Description
		2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
23:22	GDM_VLAN_PRI3_RXID_SEL	**GDM RXID Select for VLAN Priority = 3** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
21:20	GDM_VLAN_PRI2_RXID_SEL	**GDM RXID Select for VLAN Priority = 2** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
19:18	GDM_VLAN_PRI1_RXID_SEL	**GDM RXID Select for VLAN Priority = 1** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
17:16	GDM_VLAN_PRI0_RXID_SEL	**GDM RXID Select for VLAN Priority = 0** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
5:4	GDM_TCP_ACK_RXID_SEL	**GDM RXID Select for TCP ACK** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
3	GDM_TCP_ACK_WZPC	**GDM TCP ACK with zero payload check (L3 payload = L4 header)**
2:0	GDM_RXID_PRI_SEL	**GDM RXID Select Priority Setting** Select Priority by PID/STAG, VLAD_PRI, and TCP_ACK 3'b000: PID/STAG 3'b001: VLAN_PRI --> PID/STAG 3'b010: TCP_ACK --> PID/STAG 3'b011: VLAN_PRI --> TCP_ACK --> PID/STAG 3'b100: TCP_ACK --> VLAN_PRI --> PID/STAG

1B100134 FE_GDM_RXID2 FE GDM RXID Control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_STAG7_RXID_SEL		GDM_STAG6_RXID_SEL		GDM_STAG5_RXID_SEL		GDM_STAG4_RXID_SEL		GDM_STAG3_RXID_SEL		GDM_STAG2_RXID_SEL		GDM_STAG1_RXID_SEL		GDM_STAG0_RXID_SEL	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													GDM_PID2_RXID_SEL		GDM_PID1_RXID_SEL	
Type													RW		RW	
Reset													0	0	0	0

Bit(s)	Name	Description
31:30	GDM_STAG7_RXID_SEL	**GDM RXID Select for STAG = 7** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
29:28	GDM_STAG6_RXID_SEL	**GDM RXID Select for STAG = 6** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
27:26	GDM_STAG5_RXID_SEL	**GDM RXID Select for STAG = 5** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
25:24	GDM_STAG4_RXID_SEL	**GDM RXID Select for STAG = 4** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
23:22	GDM_STAG3_RXID_SEL	**GDM RXID Select for STAG = 3** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
21:20	GDM_STAG2_RXID_SEL	**GDM RXID Select for STAG = 2** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
19:18	GDM_STAG1_RXID_SEL	**GDM RXID Select for STAG = 1** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
17:16	GDM_STAG0_RXID_SEL	**GDM RXID Select for STAG = 0** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
3:2	GDM_PID2_RXID_SEL	**GDM RXID Select for GDM2 (Port ID = 2)** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
1:0	GDM_PID1_RXID_SEL	**GDM RXID Select for GDM1 (Port ID = 1)** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)

1B100240 FE_PSE_FREE PSE Free Page Count 00FF00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									FQ_PCNT_MIN							
Type									RC							
Reset									1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FQ_PCNT							
Type									RO							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
23:16	FQ_PCNT_MIN	**Free queue minimum page count since the last read** The minimum free page count will update the value whenever the free page is lower than the current record. The field will be reset to FF after MCU reads it.
7:0	FQ_PCNT	**Free queue page count**

1B100244 FE_DROP_FQ FE Packet Drop by Free Queue 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_FQ															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_FQ															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PSE_DROP_FQ	**Packet dropped by PSE when the free queue is low.** When GDM is receiving a packets and the free buffer is almost exhausted, PSE will drop any received packet no matter if FC is on or off. The filed is reset to 0 after MCU reads it.

1B100248 FE_DROP_FC FE Packet Drop by Flow Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_FC															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_FC															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PSE_DROP_FC	**Packet dropped by PSE when the flow control is off** When GDM receive the packets over the FC threshold and the flow control is off, PSE will drop the received packet to prevent the free buffer from being exhausted. The filed is reset to 0 after MCU reads it.

1B10024C FE_DROP_PPE FE Packet Drop by PPE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PSE_DROP_PPE	**Packet dropped by PPE** The PPE forwarded packet is dropped due to PDMA RX Ring is almost full when PSE_MIB_PORT.Po_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it.

1B100400 CDMP_IG_CTRL CDM Ingress Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	CDM_TPID	**Inserted VLAN TPID**
0	STAG_EN	**Special tag indication** Indicate that the received packets is carrying the special tag from CPU. 0: no special tag inserted. 1: The first 2-byte after Source Address is the special tag.

1B100404 CDMP_EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																UNTAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	UNTAG_EN	**VLAN un-tag**

Bit(s)	Name	Description
		Un-tag the egress packets which are transmitted from CDM to CPU 0: disable 1: The first 4-bytes VLAN tag after Source Address will be untagged

1B100408 CDMP_PPE_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_INS
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	**PPPoE Header Insertion**
15:0	SESS_ID	**PPPoE Session ID**

1B100500 GDM1_IG_CTRL GDM Ingress Control 00717777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							INSV_EN	STAG_EN		GDM_ICS_EN	GDM_TCS_EN	GDM_UCS_EN	DROP_256B			STRP_CRC
Type							RW	RW		RW	RW	RW	RW			RW
Reset							0	0		1	1	1	0			1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MYMAC_DP				BC_DP				MC_DP				UN_DP			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1

Bit(s)	Name	Description
25	INSV_EN	**VLAN insertion** Insert Port VID on the received packets on the corresponding GDM port. 0: disable 1: Insert 4-byte VLAN tag after Source Address
24	STAG_EN	**Special tag indication** Indicate that the received packets is carrying the special tag from GDM port. 0: no special tag inserted. 1: The first 2-byte after Source Address is the special tag.
22	GDM_ICS_EN	**IPv4 header checksum error drop** 0: checksum error status reported on RX descriptor (IP4F) 1: checksum error packet will be dropped
21	GDM_TCS_EN	**TCP checksum error drop** 0: checksum error status reported on RX descriptor (L4F) 1: checksum error packet will be dropped
20	GDM_UCS_EN	**UDP checksum error drop** 0: checksum error status reported on RX descriptor (L4F)

Bit(s)	Name	Description
		1: checksum error packet will be dropped
19	DROP_256B	**A special mode to drop packets with payload > 256-bytes** 0: Drop packets according to the standard Ethernet frame length limitation. 1: Drop packets with payload > 256 bytes
16	STRP_CRC	**GDM RX CRC Stripping** 1'b: Disable GDM RX CRC stripping 1'b1: Enable GDM RX CRC stripping
15:12	MYMAC_DP	**MY_MAC frames destination port** 4'b0000 : PDMA 4'b0001 : GDM1 4'b0010 : GDM2 4'b0011 : Reserved 4'b0100 : PPE 4'b0101 : QDMA 4'b0110 : Reserved 4'b0111 : Discard 4'b1xxx: Reserved
11:8	BC_DP	**Broadcast frame destination port** 4'b0000 : PDMA 4'b0001 : GDM1 4'b0010 : GDM2 4'b0011 : Reserved 4'b0100 : PPE 4'b0101 : QDMA 4'b0110 : Reserved 4'b0111 : Discard 4'b1xxx: Reserved
7:4	MC_DP	**Multicast frame destination port** 4'b0000 : PDMA 4'b0001 : GDM1 4'b0010 : GDM2 4'b0011 : Reserved 4'b0100 : PPE 4'b0101 : QDMA 4'b0110 : Reserved 4'b0111 : Discard 4'b1xxx: Reserved
3:0	UN_DP	**Other frame destination port** 4'b0000 : PDMA 4'b0001 : GDM1 4'b0010 : GDM2 4'b0011 : Reserved 4'b0100 : PPE 4'b0101 : QDMA 4'b0110 : Reserved 4'b0111 : Discard 4'b1xxx: Reserved

1B100504 GDM1_EG_CTRL GDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name		UNTAG_EN	DIS_PAD	DIS_CRC				SHPR_EN	BK_SIZE							
Type		RW	RW	RW				RW	RW							
Reset		0	0	0				0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TK_TICK		TK_RATE													
Type	RW		RW													
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	UNTAG_EN	**VLAN un-tag** Un-tag the egress packets which are transmitted from GDM. 0: disable 1: The first 4-bytes VLAN tag after Source Address will be untagged
29	DIS_PAD	**GMAC Tx padding function** 1'b0: Enable GMAC Tx padding 1'b1: Disable GMAC Tx padding
28	DIS_CRC	**GMAC TX CRC generation** 1'b0: Enable GMAC Tx CRC generation 1'b1: Disable GMAC Tx CRC generation
24	SHPR_EN	**GDM output shaper enable** 1'b0: Disable 1'b1: Enable
23:16	BK_SIZE	**GDM output shaper bucket size.** This unit is 1K-byte
15	TK_TICK	**GDM shaper token period** 1'b0: GDM shaper add token every 1ms 1'b1: GDM shaper add token every 20us
13:0	TK_RATE	**GDM output shaper token rate** The unit is 8-Byte/ms or 8-Byte/20us according to TK_TICK.

1B100508 GDM1_MAC_LSB GDM MY_MAC Address LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MAC_ADR	**MY_MAC Address [31:0]**

1B10050C GDM1_MAC_MSB GDM MY_MAC Address MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	MAC_ADR	**MY_MAC Address [47:32]**

1B100510 GDM1_VLAN_GEN GDM VLAN Generation 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM_PRI			GDM_CFI	GDM_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GDM_TPID	**Inserted VLAN TPID**
15:13	GDM_PRI	**Inserted PRI**
12	GDM_CFI	**Inserted CFI**
11:0	GDM_VID	**Inserted VLAN ID**

1B100800 TX_BASE_PTR_0 TX Ring #0 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	**Point to the base address of TX Ring #0 (4-DW aligned address)**

1B100804 TX_MAX_CNT_0 TX Ring #0 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV				TX_MAX_CNT											
Type	RO				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_MAX_CNT	**The maximum number of TXD count in TX Ring #0**

1B100808 TX_CTX_IDX_0 TX Ring #0 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV				TX_CTX_IDX											
Type	RO				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_CTX_IDX	**Point to the next TXD CPU wants to use**

1B10080C TX_DTX_IDX_0 TX Ring #0 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV				TX_DTX_IDX											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_DTX_IDX	**Point to the next TXD DMA wants to use**

1B100810 TX_BASE_PTR_1 TX Ring #1 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	**Point to the base address of TX Ring #0 (4-DW aligned address)**

1B100814 TX_MAX_CNT_1 TX Ring #1 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV				TX_MAX_CNT											
Type	RO				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	Reserved
11:0	TX_MAX_CNT	The maximum number of TXD count in TX Ring #0

1B100818 TX_CTX_IDX_1 TX Ring #1 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV				TX_CTX_IDX											
Type	RO				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	Reserved
11:0	TX_CTX_IDX	Point to the next TXD CPU wants to use

1B10081C TX_DTX_IDX_1 TX Ring #1 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV				TX_DTX_IDX											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	Reserved
11:0	TX_DTX_IDX	Point to the next TXD DMA wants to use

1B100820 TX_BASE_PTR_2 TX Ring #2 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	Point to the base address of TX Ring #0 (4-DW aligned address)

1B100824 TX_MAX_CNT_2 TX Ring #2 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV				TX_MAX_CNT											
Type	RO				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	Reserved
11:0	TX_MAX_CNT	The maximum number of TXD count in TX Ring #0

1B100828 TX_CTX_IDX_2 TX Ring #2 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV				TX_CTX_IDX											
Type	RO				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	Reserved
11:0	TX_CTX_IDX	Point to the next TXD CPU wants to use

1B10082C TX_DTX_IDX_2 TX Ring #2 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV				TX_DTX_IDX											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_DTX_IDX	**Point to the next TXD DMA wants to use**

1B100830 TX_BASE_PTR_3 TX Ring #3 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	**Point to the base address of TX Ring #0 (4-DW aligned address)**

1B100834 TX_MAX_CNT_3 TX Ring #3 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV				TX_MAX_CNT											
Type	RO				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_MAX_CNT	**The maximum number of TXD count in TX Ring #0**

1B100838 TX_CTX_IDX_3 TX Ring #3 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV				TX_CTX_IDX											
Type	RO				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_CTX_IDX	**Point to the next TXD CPU wants to use**

1B10083C TX_DTX_IDX_3 TX Ring #3 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV				TX_DTX_IDX											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	Reserved
11:0	TX_DTX_IDX	Point to the next TXD DMA wants to use

1B100900 RX_BASE_PTR_0 RX Ring #0 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring #0 (4-DW aligned address)

1B100904 RX_MAX_CNT_0 RX Ring #0 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV				RX_MAX_CNT											
Type	RO				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	Reserved
11:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #0

1B100908 RX_CRX_IDX_0 RX Ring #0 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV				RX_CRX_IDX											
Type	RO				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	Reserved
11:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

1B10090C RX_DRX_IDX_0 RX Ring #0 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV				RX_DRX_IDX											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	Reserved
11:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

1B100910 RX_BASE_PTR_1 RX Ring #1 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring #0 (4-DW aligned address)

1B100914 RX_MAX_CNT_1 RX Ring #1 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_MAX_CNT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #0

1B100918 RX_CRX_IDX_1 RX Ring #1 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_CRX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

1B10091C RX_DRX_IDX_1 RX Ring #1 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_DRX_IDX											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

1B100920 RX_BASE_PTR_2 RX Ring #2 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring #2 (4-DW aligned address)

1B100924 RX_MAX_CNT_2 RX Ring #2 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_MAX_CNT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #0

1B100928 RX_CRX_IDX_2 RX Ring #2 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_CRX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

1B10092C RX_DRX_IDX_2 RX Ring #2 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_DRX_IDX											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

1B100930 RX_BASE_PTR_3 RX Ring #3 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring #3 (4-DW aligned address)**

1B100934 RX_MAX_CNT_3 RX Ring #3 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_MAX_CNT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #0**

1B100938 RX_CRX_IDX_3 RX Ring #3 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_CRX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1B10093C RX_DRX_IDX_3 RX Ring #3 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_DRX_IDX											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

1B100A00 PDMA_INFO PDMA Information 3C000404

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					INDEX_WIDTH				BASE_PTR_WIDTH							
Type					RO				RO							
Reset					1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_RING_NUM								TX_RING_NUM							
Type	RO								RO							
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
27:24	INDEX_WIDTH	**Point to the next RXD CPU wants to use**
23:16	BASE_PTR_WIDTH	**Base pointer width, x** Base_addr[31:32-x] is shared with all ring base address. Only ring #0 base address[31:32-x] field is writable. [note]: "0" means no bit of base_address is shared.
15:8	RX_RING_NUM	**Rx ring number**
7:0	TX_RING_NUM	**Tx ring number**

1B100A04 PDMA_GLO_CFG PDMA Global Configuration 40001450

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_2B_OFFSET	CSR_CLKGATE_BYP	BYTE_SWAP	REVo												
Type	RW	RW	RW	RO												
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REVo			ADMA_RX_BT_SIZE		MULTI_EN	EXT_FIFO_EN	DESC_32B_E	BIG_ENDIAN	TX_WB_DDONE	PDMA_BT_SIZE		RX_DMA_BUSY	RX_DMA_EN	TX_DMA_BUSY	TX_DMA_EN
Type	RO			RW		RW	RW	RW	RW	RW	RW		RO	RW	RO	RW
Reset	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
31	RX_2B_OFFSET	**2-Byte offset** 0: Rx-buffer will be 4-byte offset 1: Rx-buffer will be 2-byte offset
30	CSR_CLKGATE_BYP	**Clock gated Bypass** 1: PDMA clock is free-running 0: PDMA clock is gating as idle
29	BYTE_SWAP	**Byte Swap** 0: PDMA will not do byte swapping for TX/RX packet descriptor 1: PDMA will do byte swapping for TX/RX packet descriptor
28:13	REVo	**Reserved**
12:11	ADMA_RX_BT_SIZE	**The burst size of ADMA RX** 0: 4 DWORDs (16-bytes) 1: 8 DWORDs (32-bytes)

Bit(s)	Name	Description
		2: 16 DWORDs (64-bytes) 3: 32 DWORDs (128-bytes)
10	MULTI_EN	**Enable Multi-burst DMA transfer** 0: disabled 1: Multi-burst DMA enabled
9	EXT_FIFO_EN	**Enable multi-burst DMA transfer for the external FIFO.** 0: Only check internal FIFO 1: Check both internal/external FIFO
8	DESC_32B_E	**Enable 32-Byte Descriptor Length** 0: PDMA will fetch the next TX/RX descriptor by adding 16-Byte 1: PDMA will fetch the next TX/RX descriptor by adding 32-Byte
7	BIG_ENDIAN	**Big endian** 0: PDMA will not do byte swapping for TX/RX packet header and payload 1: PDMA will do byte swapping for TX/RX packet header and payload
6	TX_WB_DDONE	0: Disable TX_DMA writing back DDONE into TXD 1: Enable TX_DMA writing back DDONE into TXD
5:4	PDMA_BT_SIZE	**The burst size of PDMA** 0: 4 DWORDs (16-bytes) 1: 8 DWORDs (32-bytes) 2: 16 DWORDs (64-bytes) 3: Reserved
3	RX_DMA_BUSY	0: RX_DMA is not busy 1: RX_DMA is busy
2	RX_DMA_EN	0: Disable RX_DMA (when disabled, RX_DMA will finish the current receiving packet, then stop) 1: Enable RX_DMA
1	TX_DMA_BUSY	0: TX_DMA is not busy 1: TX_DMA is busy
0	TX_DMA_EN	0: Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop) 1: Enable TX_DMA

1B100A08 PDMA_RST_IDX PDMA Reset Index 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0														RST_DRX_IDX1	RST_DRX_IDX0
Type	RO														WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1												RST_DTX_IDX3	RST_DTX_IDX2	RST_DTX_IDX1	RST_DTX_IDX0
Type	RO												WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:18	REV0	**Reserved**
17	RST_DRX_IDX1	**Write 1 to reset RX_DMA RX_IDX1 to 0**
16	RST_DRX_IDX0	**Write 1 to reset RX_DMA RX_IDX0 to 0**
15:4	REV1	**Reserved**

Bit(s)	Name	Description
3	RST_DTX_IDX3	**Write 1 to reset TX_DMA TX_IDX3 to 0**
2	RST_DTX_IDX2	**Write 1 to reset TX_DMA TX_IDX2 to 0**
1	RST_DTX_IDX1	**Write 1 to reset TX_DMA TX_IDX1 to 0**
0	RST_DTX_IDX0	**Write 1 to reset TX_DMA TX_IDX0 to 0**

1B100A0C DELAY_INT_CFG Delay Interrupt Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXDLY_INT_EN	TXMAX_PINT							TXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXDLY_INT_EN	RXMAX_PINT							RXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TXDLY_INT_EN	**Delay interrupt mechanism** 0: Disable TX delayed interrupt mechanism 1: Enable Tx delayed interrupt mechanism
30:24	TXMAX_PINT	**Specified Max. number of pended interrupts** When the number of pended interrupts is equal or greater than the value specified here or interrupt pending time reach the limit (see below), a final TX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt count check.
23:16	TXMAX_PTIME	**Specified Max. pended time** When the pending time is equal or greater than TXMAX_PTIME x 20us or the number of pended TX_DONE is equal or greater than TXMAX_PINT 9see above), a final TX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt time check.
15	RXDLY_INT_EN	0: Disable Rx delayed interrupt mechanism 1: Enable Rx delayed interrupt mechanism
14:8	RXMAX_PINT	**Specified Max. number of pended interrupts** When the number of pended interrupts is equal or greater than the value specified here or interrupt pending time reach the limit (see below), a final RX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt count check.
7:0	RXMAX_PTIME	**Specified Max. pended time** When the pending time is equal or greater than RXMAX_PTIME x 20us or the number of pended RX_DONE is equal or greater than RXMAX_PINT 9see above), a final RX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt time check.

1B100A10 FREEQ_THRES Free Queue Threshold 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1												FREEQ_THRES			

Type	RO												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:4	REV1	**Reserved**
3:0	FREEQ_THRES	**Rx free queue threshold** PDMA will stop DMA interface when left RX descriptors reach this threshold

1B100A20 INT_STATUS Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT	RING3_RX_DLY_INT	RING2_RX_DLY_INT	RING1_RX_DLY_INT	RXD_ERROR	ALT_RPLC_INT3	ALT_RPLC_INT2	ALT_RPLC_INT1	REV0	RX_DONE_INT3	RX_DONE_INT2	RX_DONE_INT1	RX_DONE_INT0
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	RO	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1												TX_DONE_INT3	TX_DONE_INT2	TX_DONE_INT1	TX_DONE_INT0
Type	RO												W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RX_COHERENT	**RX_DMA finds data coherent event while checking DDONE bit.**
30	RX_DLY_INT	**Summary of the whole PDMA Rx related interrupts.**
29	TX_COHERENT	**TX_DMA finds data coherent event while checking DDONE bit.**
28	TX_DLY_INT	**Summary of the whole PDMA Tx related interrupts.**
27	RING3_RX_DLY_INT	**Rx ring #3 packet receive interrupt**
26	RING2_RX_DLY_INT	**Rx ring #2 packet receive interrupt**
25	RING1_RX_DLY_INT	**Rx ring #1 packet receive interrupt**
24	RXD_ERROR	**Rx descriptor SDL0 error interrupt**
23	ALT_RPLC_INT3	**Auto-learn otg3 replacement interrupt**
22	ALT_RPLC_INT2	**Auto-learn otg2 replacement interrupt**
21	ALT_RPLC_INT1	**Auto-learn otg1 replacement interrupt**
20	REV0	**Reserved**
19	RX_DONE_INT3	**Rx ring #3 packet receive interrupt**
18	RX_DONE_INT2	**Rx ring #2 packet receive interrupt**
17	RX_DONE_INT1	**Rx ring #1 packet receive interrupt**
16	RX_DONE_INT0	**Rx ring #0 packet receive interrupt**
15:4	REV1	**Reserved**
3	TX_DONE_INT3	**Tx ring #3 packet transmit interrupt**
2	TX_DONE_INT2	**Tx ring #2 packet transmit interrupt**
1	TX_DONE_INT1	**Tx ring #1 packet transmit interrupt**
0	TX_DONE_INT0	**Tx ring #0 packet transmit interrupt**

1B100A28 INT_MASK Interrupt Mask 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT	RING3_RX	RING2_RX	RING1_RX	RXD_ERROR	ALT_RPLC	ALT_RPLC	ALT_RPLC_INT1	REV0	RX_DONE_INT3	RX_DONE_INT2	RX_DONE_INT1	RX_DON

					_DLY_INT	_DLY_INT	_DLY_INT		_INT3	_INT2						E_INT0
Type	RW	RW	RW	W1C	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1												TX_DONE_INT3	TX_DONE_INT2	TX_DONE_INT1	TX_DONE_INT0
Type	RW												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RX_COHERENT	**Interrupt enable for RX_DMA data coherent vent** 0: Disable interrupt 1: Enable interrupt
30	RX_DLY_INT	**Summary of the whole PDMA Rx related interrupts.** 0: Disable interrupt 1: Enable interrupt
29	TX_COHERENT	**Interrupt enable for TX_DMA data coherent vent** 0: Disable interrupt 1: Enable interrupt
28	TX_DLY_INT	**Summary of the whole PDMA Tx related interrupts.** 0: Disable interrupt 1: Enable interrupt
27	RING3_RX_DLY_INT	**Rx ring #3 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
26	RING2_RX_DLY_INT	**Rx ring #2 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
25	RING1_RX_DLY_INT	**Rx ring #1 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
24	RXD_ERROR	**Rx descriptor SDL0 error interrupt** 0: Disable interrupt 1: Enable interrupt
23	ALT_RPLC_INT3	**Auto-learn otg3 replacement interrupt** 0: Disable interrupt 1: Enable interrupt
22	ALT_RPLC_INT2	**Auto-learn otg2 replacement interrupt** 0: Disable interrupt 1: Enable interrupt
21	ALT_RPLC_INT1	**Auto-learn otg1 replacement interrupt** 0: Disable interrupt 1: Enable interrupt
20	REV0	**Reserved**
19	RX_DONE_INT3	**Rx ring #3 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
18	RX_DONE_INT2	**Rx ring #2 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
17	RX_DONE_INT1	**Rx ring #1 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
16	RX_DONE_INT0	**Rx ring #0 packet receive interrupt**

Bit(s)	Name	Description
		0: Disable interrupt 1: Enable interrupt
15:4	REV1	**Reserved** 0: Disable interrupt 1: Enable interrupt
3	TX_DONE_INT3	**Tx ring #3 packet transmit interrupt** 0: Disable interrupt 1: Enable interrupt
2	TX_DONE_INT2	**Tx ring #2 packet transmit interrupt** 0: Disable interrupt 1: Enable interrupt
1	TX_DONE_INT1	**Tx ring #1 packet transmit interrupt** 0: Disable interrupt 1: Enable interrupt
0	TX_DONE_INT0	**Tx ring #0 packet transmit interrupt** 0: Disable interrupt 1: Enable interrupt

1B100A40 PDMA_INT1_VEC_GRP0 PDMA Interrupt Status Group 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PDMA_INT1_VEC_GRP0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PDMA_INT1_VEC_GRP0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PDMA_INT1_VEC_GRP0	**Interrupt group 0 status, this information already "and" with "~PDMA_INT_GRP1 & ~PDMA_INT_GRP2"** Each bit definition is same as "INT_STATUS"

1B100A44 PDMA_INT1_VEC_GRP1 PDMA Interrupt Status Group 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PDMA_INT1_VEC_GRP1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PDMA_INT1_VEC_GRP1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PDMA_INT1_VEC_GRP1	**Interrupt group 1 status, this information already "and" with "PDMA_INT_GRP1"** Each bit definition is same as "INT_STATUS"

Bit(s)	Name	Description

1B100A48 PDMA_INT1_VEC_GRP2 PDMA Interrupt Status Group 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PDMA_INT1_VEC_GRP2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PDMA_INT1_VEC_GRP2															
Type	RO															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Name	Description
31:8	PDMA_INT1_VEC_GRP2	**Interrupt group 2 status, this information already "and" with "PDMA_INT_GRP2"** Each bit definition is same as "INT_STATUS"

1B100A50 PDMA_INT_GRP1 PDMA Interrupt Group 1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PDMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PDMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PDMA_INT_GRP1	**Interrupt group 1 assignment.** Each bit's definition is same as "INT_STATUS" 0: Leave to ADMA interrupt group 0, if (PDMA_INT_GRP1[n]==0 & PDMA_INT_GRP2[n]==0) 1: Assign to PDMA interrupt group 1

1B100A54 PDMA_INT_GRP2 PDMA Interrupt Group 2 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PDMA_INT_GRP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PDMA_INT_GRP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PDMA_INT_GRP2	**Interrupt group 2 assignment.** Each bit's definition is same as "INT_STATUS"

Bit(s)	Name	Description
		0: Leave to ADMA interrupt group 0, if (PDMA_INT_GRP1[n]==0 & PDMA_INT_GRP2[n]==0) 1: Assign to PDMA interrupt group 2

1B100A80 SCH_Q01_CFG Scheduler Configuration for Q0&Q1 5C004C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BKT_SIZE1	MAX_RATE_ULMT1	MAX_WEIGHT1		MIN_RATE_RATIO1		MAX_RATE1									
Type	RW	RW	RW		RW		RW									
Reset	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_BKT_SIZE0	MAX_RATE_ULMT0	MAX_WEIGHT0		MIN_RATE_RATIO0		MAX_RATE0									
Type	RW	RW	RW		RW		RW									
Reset	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_BKT_SIZE1	**Maximum bucket size** 0: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min. rate per 125us. 1: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min. rate per 125us + 2048 bytes.
30	MAX_RATE_ULMT1	**Maximum rate limitation** 0: the maximum rate limitation function for queue is enabled. The maximum rate for queue is defined by MAX_RATE. 1: the maximum rate limitation function for queue is disabled or unlimited. The scheduler would allocate bandwidth to queue based on MAX_WEIGHT.
29:28	MAX_WEIGHT1	**Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue** 2'b00 : 1023 bytes 2'b01 : 2047 bytes 2'b10 : 4095 bytes 2'b11: 8191 bytes
27:26	MIN_RATE_RATIO1	**Define the guaranteed Min rate based on MAX_RATE** 2'b00 : MIN_RATE3 = MAX_RATE3 2'b01 : MIN_RATE3 = 1/2 MAX_RATE3 2'b10 : MIN_RATE3 = 1/4 MAX_RATE3 2'b11 : MIN_RATE3 = 0
25:16	MAX_RATE1	**Define the limited Max rate for queue if MAX_RATE_ULMT is 0.** The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : 512 * 4 bytes/125us = 16.384M bytes/sec or 131Mbps
15	MAX_BKT_SIZE0	**Maximum bucket size** 0: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min. rate per 125us.

Bit(s)	Name	Description
		1: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min. rate per 125us + 2048 bytes.
14	MAX_RATE_ULMT0	**Maximum rate limitation** 0: the maximum rate limitation function for queue is enabled. The maximum rate for queue is defined by MAX_RATE. 1: the maximum rate limitation function for queue is disabled or unlimited. The scheduler would allocate bandwidth to queue based on MAX_WEIGHT.
13:12	MAX_WEIGHT0	**Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue** 2'b00 : 1023 bytes 2'b01 : 2047 bytes 2'b10 : 4095 bytes 2'b11: 8191 bytes
11:10	MIN_RATE_RATIO0	**Define the guaranteed Min rate based on MAX_RATE** 2'b00 : MIN_RATE3 = MAX_RATE3 2'b01 : MIN_RATE3 = 1/2 MAX_RATE3 2'b10 : MIN_RATE3 = 1/4 MAX_RATE3 2'b11 : MIN_RATE3 = 0
9:0	MAX_RATE0	**Define the limited Max rate for queue if MAX_RATE_ULMT is 0.** The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : 512 * 4 bytes/125us = 16.384M bytes/sec or 131Mbps

1B100A84 SCH_Q23_CFG Scheduler Configuration for Q2&Q3 7C006C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BKT_SIZE3	MAX_RATE_ULMT3	MAX_WEIGHT3		MIN_RATE_RATIO3		MAX_RATE3									
Type	RW	RW	RW		RW		RW									
Reset	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_BKT_SIZE2	MAX_RATE_ULMT2	MAX_WEIGHT2		MIN_RATE_RATIO2		MAX_RATE2									
Type	RW	RW	RW		RW		RW									
Reset	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_BKT_SIZE3	**Maximum bucket size** 0: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min. rate per 125us. 1: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min. rate per 125us + 2048 bytes.
30	MAX_RATE_ULMT3	**Maximum rate limitation** 0: the maximum rate limitation function for queue is enabled. The maximum rate for queue is defined by MAX_RATE.

Bit(s)	Name	Description
		1: the maximum rate limitation function for queue is disabled or unlimited. The scheduler would allocate bandwidth to queue based on MAX_WEIGHT.
29:28	MAX_WEIGHT3	**Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue** 2'b00 : 1023 bytes 2'b01 : 2047 bytes 2'b10 : 4095 bytes 2'b11: 8191 bytes
27:26	MIN_RATE_RATIO3	**Define the guaranteed Min rate based on MAX_RATE** 2'b00 : MIN_RATE3 = MAX_RATE3 2'b01 : MIN_RATE3 = 1/2 MAX_RATE3 2'b10 : MIN_RATE3 = 1/4 MAX_RATE3 2'b11 : MIN_RATE3 = 0
25:16	MAX_RATE3	**Define the limited Max rate for queue if MAX_RATE_ULMT is 0.** The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : 512 * 4 bytes/125us = 16.384M bytes/sec or 131Mbps
15	MAX_BKT_SIZE2	**Maximum bucket size** 0: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min. rate per 125us. 1: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min. rate per 125us + 2048 bytes.
14	MAX_RATE_ULMT2	**Maximum rate limitation** 0: the maximum rate limitation function for queue is enabled. The maximum rate for queue is defined by MAX_RATE. 1: the maximum rate limitation function for queue is disabled or unlimited. The scheduler would allocate bandwidth to queue based on MAX_WEIGHT.
13:12	MAX_WEIGHT2	**Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue** 2'b00 : 1023 bytes 2'b01 : 2047 bytes 2'b10 : 4095 bytes 2'b11: 8191 bytes
11:10	MIN_RATE_RATIO2	**Define the guaranteed Min rate based on MAX_RATE** 2'b00 : MIN_RATE3 = MAX_RATE3 2'b01 : MIN_RATE3 = 1/2 MAX_RATE3 2'b10 : MIN_RATE3 = 1/4 MAX_RATE3 2'b11 : MIN_RATE3 = 0
9:0	MAX_RATE2	**Define the limited Max rate for queue if MAX_RATE_ULMT is 0.** The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : 512 * 4 bytes/125us = 16.384M bytes/sec or 131Mbps

1B101400 CDMQ_IG_CTRL CDM VLAN Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															

Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															UNTAG_EN	STAG_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
31:16	CDM_TPID	**Inserted VLAN TPID**
1	UNTAG_EN	**VLAN un-tag** Un-tag the egress packets which are transmitted from CDM 0: disable 1: The first 4-bytes VLAN tag after Source Address will be untagged
0	STAG_EN	**Special tag indication** Indicate that the received packets is carrying the special tag from CPU 0: no special tag inserted. 1: The first 2-byte after Source Address is the special tag.

1B101404 CDMQ_EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																UNTAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	UNTAG_EN	**VLAN un-tag** Un-tag the egress packets which are transmitted from CDM to CPU 0: disable 1: The first 4-bytes VLAN tag after Source Address will be untagged

1B101408 CDMQ_PPP_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_INS
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	**PPPoE Header Insertion**

Bit(s)	Name	Description
15:0	SESS_ID	**PPPoE Session ID**

1B101500 GDM2_IG_CTRL GDM Ingress Control 00717777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							INSV_EN	STAG_EN		GDM_ICS_EN	GDM_TCS_EN	GDM_UCS_EN	DROP_256B			STRP_CRC
Type							RW	RW		RW	RW	RW	RW			RW
Reset							0	0		1	1	1	0			1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MYMAC_DP				BC_DP				MC_DP				UN_DP			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1

Bit(s)	Name	Description
25	INSV_EN	**VLAN insertion** Insert Port VID on the received packets on the corresponding GDM port. 0: disable 1: Insert 4-byte VLAN tag after Source Address
24	STAG_EN	**Special tag indication** Indicate that the received packets is carrying the special tag from GDM port. 0: no special tag inserted. 1: The first 2-byte after Source Address is the special tag.
22	GDM_ICS_EN	**IPv4 header checksum error drop** 0: checksum error status reported on RX descriptor (IP4F) 1: checksum error packet will be dropped
21	GDM_TCS_EN	**TCP checksum error drop** 0: checksum error status reported on RX descriptor (L4F) 1: checksum error packet will be dropped
20	GDM_UCS_EN	**UDP checksum error drop** 0: checksum error status reported on RX descriptor (L4F) 1: checksum error packet will be dropped
19	DROP_256B	**A special mode to drop packets with payload > 256-bytes** 1'b0: Drop packets according to the standard Ethernet frame length limitation. 1'b1: Drop packets with payload > 256 bytes
16	STRP_CRC	**GDM RX CRC Stripping** 1'b: Disable GDM RX CRC stripping 1'b1: Enable GDM RX CRC stripping
15:12	MYMAC_DP	**MY_MAC frames destination port** 4'b0000 : PDMA 4'b0001 : GDM1 4'b0010 : GDM2 4'b0011 : Reserved 4'b0100 : PPE 4'b0101 : QDMA 4'b0110 : Reserved 4'b0111 : Discard 4'b1xxx: Reserved
11:8	BC_DP	**Broadcast frame destination port** 4'b0000 : PDMA

Bit(s)	Name	Description
		4'b0001 : GDM1 4'b0010 : GDM2 4'b0011 : Reserved 4'b0100 : PPE 4'b0101 : QDMA 4'b0110 : Reserved 4'b0111 : Discard 4'b1xxx: Reserved
7:4	MC_DP	**Multicast frame destination port** 4'b0000 : PDMA 4'b0001 : GDM1 4'b0010 : GDM2 4'b0011 : Reserved 4'b0100 : PPE 4'b0101 : QDMA 4'b0110 : Reserved 4'b0111 : Discard 4'b1xxx: Reserved
3:0	UN_DP	**Other frame destination port** 4'b0000 : PDMA 4'b0001 : GDM1 4'b0010 : GDM2 4'b0011 : Reserved 4'b0100 : PPE 4'b0101 : QDMA 4'b0110 : Reserved 4'b0111 : Discard 4'b1xxx: Reserved

1B101504 GDM2_EG_CTRL GDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		UNTAG_EN	DIS_PAD	DIS_CRC				SHPR_EN	BK_SIZE							
Type		RW	RW	RW				RW	RW							
Reset		0	0	0				0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TK_TICK		TK_RATE													
Type	RW		RW													
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	UNTAG_EN	**VLAN un-tag** Un-tag the egress packets which are transmitted from GDM. 0: disable 1: The first 4-bytes VLAN tag after Source Address will be untagged
29	DIS_PAD	**GMAC Tx padding function** 1'b0: Enable GMAC Tx padding 1'b1: Disable GMAC Tx padding
28	DIS_CRC	**GMAC TX CRC generation** 1'b0: Enable GMAC Tx CRC generation

Bit(s)	Name	Description
		1'b1: Disable GMAC Tx CRC generation
24	SHPR_EN	**GDM output shaper enable** 1'b0: Disable 1'b1: Enable
23:16	BK_SIZE	**GDM output shaper bucket size.** This unit is 1K-byte
15	TK_TICK	**GDM shaper token period** 1'b0: GDM shaper add token every 1ms 1'b1: GDM shaper add token every 20us
13:0	TK_RATE	**GDM output shaper token rate** The unit is 8-Byte/ms or 8-Byte/20us according to TK_TICK.

1B101508 GDM2_MAC_LSB GDM MY_MAC Address LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MAC_ADR	**MY_MAC Address [31:0]**

1B10150C GDM2_MAC_MSB GDM MY_MAC Address MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	MAC_ADR	**MY_MAC Address [47:32]**

1B101510 GDM2_VLAN_GEN GDM VLAN Generation 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM_PRI			GDM_CFI	GDM_VID											
Type	RW			RW	RW											

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GDM_TPID	**Inserted VLAN TPID**
15:13	GDM_PRI	**Inserted PRI**
12	GDM_CFI	**Inserted CFI**
11:0	GDM_VID	**Inserted VLAN ID**

1B101514 GDM2_FILTER_CRTL GDM Filter Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													GDM_VIDF_EN	GMD_HASH_ALG	GDM_DAF_MODE	
Type													RW	RW	RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3	GDM_VIDF_EN	**GDM VLAN ID filter enable**
2	GMD_HASH_ALG	**Hash Algorithm setting** 0: Direct map - Using DA40 and DA 7~0 as hash key. Receive packet if corresponding bit is set. 1: CRC32 - Using 32 bit CRC bit 8~0 of DA as hash key. Receive packet if corresponding bit is set.
1:0	GDM_DAF_MODE	**Receive packet with DA Filter function** 0: Promiscuous mode - Receive all packets. 1: Filter packet by MAC_MAC/Broadcast/Hash table 2: Filter packet by MAC_MAC/Broadcast 3: Reserved

1B101518 GDM2_VIDF01 GDM VID Filter Control 01 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM2_VID1_VLD				GDM2_VID1											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM2_VID0_VLD				GDM2_VID0											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	GDM2_VID1_VLD	**VLAN ID #1 valid bit**
27:16	GDM2_VID1	**VLAN ID #1**
15	GDM2_VID0_VLD	**VLAN ID #0 valid bit**
11:0	GDM2_VID0	**VLAN ID #0**

1B10151C GDM2_VIDF23 GDM VID Filter Control 23 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM2_VID3_VLD				GDM2_VID3											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM2_VID2_VLD				GDM2_VID2											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	GDM2_VID3_VLD	**VLAN ID #3 valid bit**
27:16	GDM2_VID3	**VLAN ID #3**
15	GDM2_VID2_VLD	**VLAN ID #2 valid bit**
11:0	GDM2_VID2	**VLAN ID #2**

1B101600 CDMW_IG_CTRL CDM VLAN Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	CDM_TPID	**Inserted VLAN TPID**
0	STAG_EN	**Special tag indication** Indicate that the received packets is carrying the special tag from CPU 0: no special tag inserted. 1: The first 2-byte after Source Address is the special tag.

1B101604 CDMW_EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																UNTAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	UNTAG_EN	**VLAN un-tag** Un-tag the egress packets which are transmitted from CDM to CPU 0: disable 1: The first 4-bytes VLAN tag after Source Address will be untagged

1B101608 CDMW_PPP_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_INS
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	**PPPoE Header Insertion**
15:0	SESS_ID	**PPPoE Session ID**

1B101800 QTX_CFG_0 TX Queue #0, #(16 * n) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES.

1B101804 QTX_SCH_0 TX Queue #0, #(16 * n) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	TX_SCH_SEL	LEAKY_BK	BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Leaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3:16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** [Note] Rate control is calculated by 125MHz bus clock, please multiply by a factor when the bus clock is not 125MHz. 0: disable. When disable, shaper will always let the packet pass (infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** Value range: 0~127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable.** [Note] Rate control is calculated by 125MHz bus clock, please multiply by a factor when the bus clock is not 125MHz. 0: disable. When disable, shaper will always let the packet pass (infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** Value range: 0~127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps)

Bit(s)	Name	Description
		1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B101808 QTX_HEAD_0 TX Queue #0, #(16 * n) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10180C QTX_TAIL_0 TX Queue #0, #(16 * n) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101810 QTX_CFG_1 TX Queue #1, #(16 * n + 1) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**

Bit(s)	Name	Description
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES.

1B101814 QTX_SCH_1 TX Queue #1, #(16 * n + 1) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer the description of QTX_SCH_0, the same definition.**

1B101818 QTX_HEAD_1 TX Queue #1, #(16 * n + 1) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10181C QTX_TAIL_1 TX Queue #1, #(16 * n + 1) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101820 QTX_CFG_2 TX Queue #2, #(16 * n + 2) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES.

1B101824 QTX_SCH_2 TX Queue #2, #(16 * n + 2) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer the description of QTX_SCH_0, the same definition.**

1B101828 QTX_HEAD_2 TX Queue #2, #(16 * n + 2) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10182C QTX_TAIL_2 TX Queue #2, #(16 * n + 2) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101830 QTX_CFG_3 TX Queue #3, #(16 * n + 3) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B101834 QTX_SCH_3 TX Queue #3, #(16 * n + 3) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer the description of QTX_SCH_0, the same definition.**

1B101838 QTX_HEAD_3 TX Queue #3, #(16 * n + 3) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10183C QTX_TAIL_3 TX Queue #3, #(16 * n + 3) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101840 QTX_CFG_4 TX Queue #4, #(16 * n + 4) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

Bit(s)	Name	Description

1B101844 QTX_SCH_4 TX Queue #4, #(16 * n + 4) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer the description of QTX_SCH_0, the same definition.**

1B101848 QTX_HEAD_4 TX Queue #4, #(16 * n + 4) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10184C QTX_TAIL_4 TX Queue #4, #(16 * n + 4) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101850 QTX_CFG_5 TX Queue #5, #(16 * n + 5) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B101854 QTX_SCH_5 TX Queue #5, #(16 * n + 5) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer the description of QTX_SCH_0, the same definition.**

1B101858 QTX_HEAD_5 TX Queue #5, #(16 * n + 5) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10185C QTX_TAIL_5 TX Queue #5, #(16 * n + 5) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101860 QTX_CFG_6 TX Queue #6, #(16 * n + 6) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B101864 QTX_SCH_6 TX Queue #6, #(16 * n + 6) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer the description of QTX_SCH_0, the same definition.**

1B101868 QTX_HEAD_6 TX Queue #6, #(16 * n + 6) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10186C QTX_TAIL_6 TX Queue #6, #(16 * n + 6) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101870 QTX_CFG_7 TX Queue #7, #(16 * n + 7) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

Bit(s)	Name	Description

1B101874 QTX_SCH_7 TX Queue #7, #(16 * n + 7) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer the description of QTX_SCH_0, the same definition.**

1B101878 QTX_HEAD_7 TX Queue #7, #(16 * n + 7) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10187C QTX_TAIL_7 TX Queue #7, #(16 * n + 7) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101880 QTX_CFG_8 TX Queue #8, #(16 * n + 8) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B101884 QTX_SCH_8 TX Queue #8, #(16 * n + 8) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer the description of QTX_SCH_0, the same definition.**

1B101888 QTX_HEAD_8 TX Queue #8, #(16 * n + 8) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10188C QTX_TAIL_8 TX Queue #8, #(16 * n + 8) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101890 QTX_CFG_9 TX Queue #9, #(16 * n + 9) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B101894 QTX_SCH_9 TX Queue #9, #(16 * n + 9) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer the description of QTX_SCH_0, the same definition.**

1B101898 QTX_HEAD_9 TX Queue #9, #(16 * n + 9) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10189C QTX_TAIL_9 TX Queue #9, #(16 * n + 9) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B1018A0 QTX_CFG_10 TX Queue #10, #(16 * n + 10) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

Bit(s)	Name	Description

1B1018A4 QTX_SCH_10 TX Queue #10, #(16 * n + 10) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	Please refer the description of QTX_SCH_0, the same definition.

1B1018A8 QTX_HEAD_10 TX Queue #10, #(16 * n + 10) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	TX descriptor head pointer in Queue #

1B1018AC QTX_TAIL_10 TX Queue #10, #(16 * n + 10) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	TX descriptor tail pointer in Queue #

1B1018B0 QTX_CFG_11 TX Queue #11, #(16 * n + 11) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B1018B4 QTX_SCH_11 TX Queue #11, #(16 * n + 11) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer the description of QTX_SCH_0, the same definition.**

1B1018B8 QTX_HEAD_11 TX Queue #11, #(16 * n + 11) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

Bit(s)	Name	Description

1B1018BC QTX_TAIL_11 TX Queue #11, #(16 * n + 11) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B1018C0 QTX_CFG_12 TX Queue #12, #(16 * n + 12) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B1018C4 QTX_SCH_12 TX Queue #12, #(16 * n + 12) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer the description of QTX_SCH_0, the same definition.**

1B1018C8 QTX_HEAD_12 TX Queue #12, #(16 * n + 12) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B1018CC QTX_TAIL_12 TX Queue #12, #(16 * n + 12) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B1018D0 QTX_CFG_13 TX Queue #13, #(16 * n + 13) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES.

Bit(s)	Name	Description
7:0	SW_RESV_CNT	0: No reserved buffer 1: Buffer Reserved **Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B1018D4 QTX_SCH_13 TX Queue #13, #(16 * n + 13) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer the description of QTX_SCH_0, the same definition.**

1B1018D8 QTX_HEAD_13 TX Queue #13, #(16 * n + 13) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B1018DC QTX_TAIL_13 TX Queue #13, #(16 * n + 13) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B1018E0 QTX_CFG_14 TX Queue #14, #(16 * n + 14) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B1018E4 QTX_SCH_14 TX Queue #14, #(16 * n + 14) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer the description of QTX_SCH_0, the same definition.**

1B1018E8 QTX_HEAD_14 TX Queue #14, #(16 * n + 14) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B1018EC QTX_TAIL_14 TX Queue #14, #(16 * n + 14) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B1018F0 QTX_CFG_15 TX Queue #15, #(16 * n + 15) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B1018F4 QTX_SCH_15 TX Queue #15, #(16 * n + 15) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer the description of QTX_SCH_0, the same definition.**

1B1018F8 QTX_HEAD_15 TX Queue #15, #(16 * n + 15) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B1018FC QTX_TAIL_15 TX Queue #15, #(16 * n + 15) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101900 QRX_BASE_PTR_0 RX Ring #0 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	Point to the base address of RX Ring # (4-DW aligned address)

1B101904 QRX_MAX_CNT_0 RX Ring #0 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_MAX_CNT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	The maximum number of RXD count in RX Ring #

1B101908 QRX_CRX_IDX_0 RX Ring #0 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_CRX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	Point to the next RXD CPU wants to use

1B10190C QRX_DRX_IDX_0 RX Ring #0 DMA pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_DRX_IDX											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	Point to the next RXD DMA wants to use

1B101980 VQTX_TB_BASE_0 TX Virtual Queue Table #0 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_0	**Base address of TX Virtual Queue Table #0** This virtual queue table belongs to virtual queue group #0

1B101984 VQTX_TB_BASE_1 TX Virtual Queue Table #1 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_1	**Base address of TX Virtual Queue Table #1** This virtual queue table belongs to virtual queue group #1

1B101988 VQTX_TB_BASE_2 TX Virtual Queue Table #2 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_2	**Base address of TX Virtual Queue Table #2** This virtual queue table belongs to virtual queue group #2

1B10198C VQTX_TB_BASE_3 TX Virtual Queue Table #3 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_3	**Base address of TX Virtual Queue Table #3** This virtual queue table belongs to virtual queue group #3

1B101990 VQTX_TB_BASE_4 TX Virtual Queue Table #4 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_4	**Base address of TX Virtual Queue Table #4** This virtual queue table belongs to virtual queue group #4

1B101994 VQTX_TB_BASE_5 TX Virtual Queue Table #5 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_5	**Base address of TX Virtual Queue Table #5** This virtual queue table belongs to virtual queue group #5

1B101998 VQTX_TB_BASE_6 TX Virtual Queue Table #6 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_6															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_6	**Base address of TX Virtual Queue Table #6** This virtual queue table belongs to virtual queue group #6

1B10199C VQTX_TB_BASE_7 TX Virtual Queue Table #7 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_7	**Base address of TX Virtual Queue Table #7** This virtual queue table belongs to virtual queue group #7

1B1019F0 QDMA_PAGE QDMA Configuration Page 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													QTX_CFG_PAGE			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	QTX_CFG_PAGE	**Switch the page of per physical queue configuration registers** This setting will control following registers: QTX_CFG_*/QTX_SCH_*/QTX_HEAD_*/QTX_TAIL_*/RST_TX_IDX*/QDMA_DROP_PREC/FORCE_QUE 0: Mapping to physical queue #0~15, page n = 0 1: Mapping to physical queue #16~31, page n = 1 2: Mapping to physical queue #32~47, page n = 2 3: Mapping to physical queue #48~63, page n = 3 Others: Reserved

1B101A00 QDMA_INFO QDMA Information 000C0240

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV				INDEX_WIDTH											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_QUE_NUM							
Type									RO							
Reset									0	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	REV	**QDMA revision**
27:16	INDEX_WIDTH	**Ring index width**
7:0	TX_QUE_NUM	**TX queue number**

1B101A04 QDMA_GLO_CFG QDMA Global Configuration 40100450

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_2B_OFFSET	CSR_CLKGATE_BYP	BYTE_SWAP													
Type	RW	RW	RW													
Reset	0	1	0													
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DESC_32B_E	BIG_ENDIAN		QDMA_BT_SIZE		RX_DMA_BUSY	RX_DMA_EN	TX_DMA_BUSY	TX_DMA_EN
Type								RW	RW		RW		RO	RW	RO	RW
Reset								0	0		0	1	0	0	0	0

Bit(s)	Name	Description
31	RX_2B_OFFSET	**2-Byte offset** 0: Rx-buffer will be 4-byte offset 1: Rx-buffer will be 2-byte offset
30	CSR_CLKGATE_BYP	**Clock gated Bypass** 0: WDMA clock is gating as idle 1: WDMA clock is free-running
29	BYTE_SWAP	**Byte Swap** 0: QDMA will not do byte swapping for TX/RX packet descriptor 1: QDMA will do byte swapping for TX/RX packet descriptor
8	DESC_32B_E	**Enable 32-Byte RX Descriptor Length** 0: PDMA will fetch the next RX descriptor by adding 16-Byte 1: PDMA will fetch the next RX descriptor by adding 32-Byte
7	BIG_ENDIAN	**Big-endian** 0: QDMA will not do byte swapping for TX/RX packet header and payload 1: QDMA will do byte swapping for TX/RX packet header and payload
5:4	QDMA_BT_SIZE	**The burst size of QDMA** 0: 4 DWORDs (16-bytes) 1: 8 DWORDs (32-bytes) 2: 16 DWORDs (64-bytes) 3: 32 DWORDs (128-bytes)

Bit(s)	Name	Description
3	RX_DMA_BUSY	0: RX_DMA is not busy 1: RX_DMA is busy
2	RX_DMA_EN	0: Disable RX_DMA (when disabled, RX_DMA will finish the current receiving packet, then stop) 1: Enable RX_DMA
1	TX_DMA_BUSY	0: TX_DMA is not busy 1: TX_DNA is busy
0	TX_DMA_EN	0: Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop) 1: Enable TX_DMA

1B101A08 QDMA_RST_IDX QDMA Reset Index 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RST_SCH											RST_DRX_IDX1	RST_DRX_IDX0
Type				RW											RW	RW
Reset				0											0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RST_TX_IDX15	RST_TX_IDX14	RST_TX_IDX13	RST_TX_IDX12	RST_TX_IDX11	RST_TX_IDX10	RST_TX_IDX9	RST_TX_IDX8	RST_TX_IDX7	RST_TX_IDX6	RST_TX_IDX5	RST_TX_IDX4	RST_TX_IDX3	RST_TX_IDX2	RST_TX_IDX1	RST_TX_IDX0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	RST_SCH	**Write 1 to reset all token bucket of scheduler** Only valid when QTX_CFG_PAGE = 0
17	RST_DRX_IDX1	**Write 1 to reset RX_DMA RX_IDX1 to 0** Only valid when QTX_CFG_PAGE = 0
16	RST_DRX_IDX0	**Write 1 to reset RX_DMA RX_IDX0 to 0** Only valid when QTX_CFG_PAGE = 0
15	RST_TX_IDX15	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 15) to 0**
14	RST_TX_IDX14	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 14) to 0**
13	RST_TX_IDX13	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 13) to 0**
12	RST_TX_IDX12	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 12) to 0**
11	RST_TX_IDX11	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 11) to 0**
10	RST_TX_IDX10	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 10) to 0**
9	RST_TX_IDX9	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 9) to 0**
8	RST_TX_IDX8	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 8) to 0**
7	RST_TX_IDX7	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 7) to 0**
6	RST_TX_IDX6	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 6) to 0**
5	RST_TX_IDX5	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 5) to 0**

Bit(s)	Name	Description
4	RST_TX_IDX4	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 4) to 0**
3	RST_TX_IDX3	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 3) to 0**
2	RST_TX_IDX2	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 2) to 0**
1	RST_TX_IDX1	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 1) to 0**
0	RST_TX_IDX0	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 0) to 0**

1B101A0C QDMA_DELAY_INT Delay Interrupt Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RXDLY_INT_EN	RXMAX_PINT							RXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLS_DINT_EN	RLS_MAX_PINT							RLS_MAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RXDLY_INT_EN	0: Disable Rx delayed interrupt mechanism 1: Enable Rx delayed interrupt mechanism
30:24	RXMAX_PINT	**Specified Max. number of pended interrupts** When the number of pended interrupts is equal or greater than the value specified here or interrupt pending time reach the limit (see below), a final RX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt count check.
23:16	RXMAX_PTIME	**Specified Max. pended time** When the pending time is equal or greater than RXMAX_PTIME x 20us or the number of pended RX_DONE is equal or greater than RXMAX_PINT 9see above), a final RX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt time check.
15	RLS_DINT_EN	0: Disable RLS delayed interrupt mechanism 1: Enable RLS delayed interrupt mechanism
14:8	RLS_MAX_PINT	**Specified Max. number of pended interrupts** When the number of pended interrupts is equal or greater than the value specified here or interrupt pending time reach the limit (see below), a final RLS_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt count check.
7:0	RLS_MAX_PTIME	**Specified Max. pended time** When the pending time is equal or greater than RLS_MAX_PTIME x 20us or the number of pended RX_DONE is equal or greater than RLS_MAX_PINT (see above), a final RLS_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt time check.

1B101A10 QDMA_FC_THRES Flow Control Threshold 90904444

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	SW_DROP_FSTVQ_MODE		SW_DROP_MODE		SW_DROP_FSTVQ		SW_DROP_FFA	SW_DROP_EN	HW_DROP_FSTVQ_MODE		HW_DROP_MODE		HW_DROP_FSTVQ		HW_DROP_FFA	HW_DROP_EN
Type	RW		RW		RW		RW	RW	RW		RW		RW		RW	RW
Reset	1	0	0	1	0		0	0	1	0	0	1	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SHARE_SW_TH				SHARE_HW_TH				FREE_TH				RING_TH			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

Bit(s)	Name	Description
31:30	SW_DROP_FSTVQ_MODE	**SW drop condition on fullest virtual queue** If the corresponding PQ SW occupied queue depth over the SW_RESV_CNT, the en-queuing packet to fullest VQ will be drop depends on the usage of SW free-for-all buffer. 2'b00: FFA usage >= 0% 2'b01: FFA usage >= 25% 2'b10: FFA usage >= 50% 2'b11: FFA usage >= 75%
29:28	SW_DROP_MODE	**Drop Distribution Mode for SW Drop** Different drop probability when SW Free for All buffer usage (>75% / >50% / >25% / >0%) Drop Probability: 2'b00: 50%/25%/0%/0% 2'b01: 75%/50%/25%/0% 2'b10: 100%/75%/50%/25% 2'b11: 100%/100%/75%/50%
27	SW_DROP_FSTVQ	**SW drop en-queuing packet on fullest virtual queue, only take effect on the physical queues those binding with virtual queues.**
25	SW_DROP_FFA	**Flow Control Drop** QDMA asserts FC when FFA is equal to 0 and egress queue count is bigger than the reserved queue count. However, the de-assert condition is specified on this control bit. 0: QDMA de-assert FC when the egress queue count is less than the reserved queue count. 1: QDMA de-assert FC when FFA is bigger than 0 or the egress queue count is less than the reserved queue count.
24	SW_DROP_EN	**Enable Flow Control for SW buffer pool** QDMA drop packets when FFA is equal to 0 and the egress queue count is bigger than the reserved queue count.
23:22	HW_DROP_FSTVQ_MODE	**HW drop condition on fullest virtual queue** If the corresponding PQ SW occupied queue depth over the SW_RESV_CNT, the en-queuing packet to fullest VQ will be drop depends on the usage of HW free-for-all buffer. 2'b00: FFA usage >= 0% 2'b01: FFA usage >= 25% 2'b10: FFA usage >= 50% 2'b11: FFA usage >= 75%
21:20	HW_DROP_MODE	**Drop Distribution Mode for HW Drop** Different drop probability when HW Free for All buffer usage (>75% / >50% / >25% / >0%) Drop Probability: 2'b00: 50%/25%/0%/0% 2'b01: 75%/50%/25%/0% 2'b10: 100%/75%/50%/25%

Bit(s)	Name	Description
		2'b11: 100%/100%/75%/50%
19	HW_DROP_FSTVQ	**HW drop en-queuing packet on fullest virtual queue, only take effect on the physical queues those binding with virtual queues.**
17	HW_DROP_FFA	**Flow Control Drop** QDMA asserts FC when FFA is equal to 0 and the egress queue count is bigger than the reserved queue count. However, the de-assert condition is specified on this control bit. 0: QDMA de-assert FC when the egress queue count is less than the reserved queue count. 1: QDMA de-assert FC when FFA is bigger than 0 or the egress queue count is less than the reserved queue count.
16	HW_DROP_EN	**Enable Flow Control for HW buffer pool** QDMA drop packets when FFA is equal to 0 and the egress queue count is bigger than the reserved queue count.
15:12	SHARE_SW_TH	**SW Shared buffer threshold** QDMA will drop TX packets when the left shared buffer descriptors reach this threshold
11:8	SHARE_HW_TH	**HW Shared buffer threshold** QDMA will drop TX packets when the left shared buffer descriptors reach this threshold
7:4	FREE_TH	**Rx free buffer threshold** QDMA will pause RXDMA interface when the left free buffer descriptors reach this threshold
3:0	RING_TH	**Rx Ring threshold** QDMA will pause RXDMA interface when the left RX ring descriptors reach this threshold

1B101A14 QDMA_TX_SCH TX Scheduler Rate Control 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SCH2_MAX_WRR	SCH2_LEAKY_BK	SCH2_BUCKET_DEP		SCH2_RATE_EN	SCH2_RATE_MAN							SCH2_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCH1_MAX_WRR	SCH1_LEAKY_BK	SCH1_BUCKET_DEP		SCH1_RATE_EN	SCH1_RATE_MAN							SCH1_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31	SCH2_MAX_WRR	**Physical Queue arbitration mechanism between MIN and MAX rate** 0: Strict Priority 1: Weighted Round-Robin
30	SCH2_LEAKY_BK	**Leaky Bucket Select**
29:28	SCH2_BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3:16KB

Bit(s)	Name	Description
27	SCH2_RATE_EN	**TX SCH2 max. rate control enable**
26:20	SCH2_RATE_MAN	**Mantissa part of the max. rate control of the TX SCH2** Value range: 0~127
19:16	SCH2_RATE_EXP	**Exponent part of the max. rate control of the TX SCH2** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15	SCH1_MAX_WRR	**Physical Queue arbitration mechanism between MIN and MAX rate** 0: Strict Priority 1: Weighted Round-Robin
14	SCH1_LEAKY_BK	**Leaky Bucket Select**
13:12	SCH1_BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3:16KB
11	SCH1_RATE_EN	**TX SCH1 max. rate control enable**
10:4	SCH1_RATE_MAN	**Mantissa part of the max. rate control of the TX SCH1** Value range: 0~127
3:0	SCH1_RATE_EXP	**Exponent part of the max. rate control of the TX SCH2** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B101A18 QDMA_INT_STS Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	RLS_COHERENT	RLS_DLY_INT											RX_DONE_INT1	RX_DONE_INT0
Type	W1C	W1C	W1C	W1C											W1C	W1C
Reset	0	0	0	0											0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQDEP_DEQ_ERR1	VQDEP_DEQ_ERR0	VQDEP_ENQ_ERR1	VQDEP_ENQ_ERR0				FWD_FIFO_OV				QTX_REQ_EMP_VQ				RLS_DONE_INT
Type	W1C	W1C	W1C	W1C				W1C				W1C				W1C
Reset	0	0	0	0				0				0				0

Bit(s)	Name	Description
31	RX_COHERENT	**RX_DMA finds data coherent event while checking DDONE bit.**
30	RX_DLY_INT	**Summary of the whole QDMA Rx related interrupts.**
29	RLS_COHERENT	**TX_DMA finds data coherent event while checking DDONE bit.**
28	RLS_DLY_INT	**Summary of the whole QDMA TX related interrupts.**
17	RX_DONE_INT1	**Rx ring #1 packet receive interrupt**
16	RX_DONE_INT0	**Rx ring #0 packet receive interrupt**
15	VQDEP_DEQ_ERR1	**VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing.** A VQ not empty yet after de-queuing, but the remainder VQ_DEPTH >= 1
14	VQDEP_DEQ_ERR0	**VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing.** A VQ becomes empty after de-queuing but the remainder VQ_DEPTH = 0
13	VQDEP_ENQ_ERR1	**VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing.** A VQ been en-queued the first packet descriptor, but the VQ_DEPTH already >=1.
12	VQDEP_ENQ_ERR0	**VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing.** A VQ been en-queued a packet descriptor, but the VQ_DEPTH already full = 16'hffff.
8	FWD_FIFO_OV	**Forwarding engine FIFO overflow interrupt**
4	QTX_REQ_EMP_VQ	**QDMA TX request to transmit an empty VQ**
0	RLS_DONE_INT	**CPU release transmitted packet interrupt**

1B101A1C QDMA_INT_MASK Interrupt Mask 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	RLS_COHERENT	RLS_DLY_INT											RX_DONE_INT1	RX_DONE_INT0
Type	RW	RW	RW	RW											RW	RW
Reset	0	0	0	0											0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQDEP_DEQ_ERR1	VQDEP_DEQ_ERR0	VQDEP_ENQ_ERR1	VQDEP_ENQ_ERR0				FWD_FIFO_OV				QTX_REQ_EMP_VQ				RLS_DONE_INT
Type	RW	RW	RW	RW				RW				RW				RW
Reset	0	0	0	0				0				0				0

Bit(s)	Name	Description
31	RX_COHERENT	**Interrupt enable for RX_DMA data coherent vent** 0: Disable interrupt 1: Enable interrupt
30	RX_DLY_INT	**Summary of the whole QDMA Rx related interrupts.** 0: Disable interrupt 1: Enable interrupt
29	RLS_COHERENT	**Interrupt enable for TX_DMA data coherent vent** 0: Disable interrupt 1: Enable interrupt
28	RLS_DLY_INT	**Summary of the whole QDMA Tx related interrupts.**

Bit(s)	Name	Description
		0: Disable interrupt 1: Enable interrupt
17	RX_DONE_INT1	**Rx ring #1 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
16	RX_DONE_INT0	**Rx ring #0 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
15	VQDEP_DEQ_ERR1	**VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing.** A VQ not empty yet after de-queuing, but the remainder VQ_DEPTH >= 1 0: Disable interrupt 1: Enable interrupt
14	VQDEP_DEQ_ERR0	**VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing.** A VQ becomes empty after de-queuing but the remainder VQ_DEPTH = 0 0: Disable interrupt 1: Enable interrupt
13	VQDEP_ENQ_ERR1	**VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing.** A VQ been en-queued the first packet descriptor, but the VQ_DEPTH already >= 1. 0: Disable interrupt 1: Enable interrupt
12	VQDEP_ENQ_ERR0	**VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing.** A VQ been en-queued a packet descriptor, but the VQ_DEPTH already full = 16'hffff. 0: Disable interrupt 1: Enable interrupt
8	FWD_FIFO_OV	**Forwarding engine FIFO overflow interrupt** 0: Disable interrupt 1: Enable interrupt
4	QTX_REQ_EMP_VQ	**QDMA TX request to transmit an empty VQ**
0	RLS_DONE_INT	**CPU release transmitted packet interrupt** 0: Disable interrupt 1: Enable interrupt

1B101A20 QDMA_INT_GRP1 QDMA Interrupt Group 1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_GRP1	**Interrupt group 1 assignment.** Each bit's definition is same as "QDMA_INT_STS"

Bit(s)	Name	Description
		0: Leave to QDMA interrupt group 0, if (QDMA_INT_GRP1[n]==0 & QDMA_INT_GRP2[n]==0) 1: Assign to QDMA interrupt group 1

1B101A24 QDMA_INT_GRP2 QDMA Interrupt Group 2 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_GRP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_GRP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_GRP2	**Interrupt group 2 assignment.** Each bit's definition is same as "QDMA_INT_STS" 0: Leave to QDMA interrupt group 0, if (QDMA_INT_GRP1[n]==0 & QDMA_INT_GRP2[n]==0) 1: Assign to QDMA interrupt group 2

1B101A2C QDMA_DROP_PREC QDMA Drop by FFA Percentage Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SW_DROP_PREC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_DROP_PREC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SW_DROP_PREC	**QDMA SW Drop by FFA Percentage Control** QDMA drop packets based on the full percentage of Free-for-All [31:16] = [PQ#(16 * QTX_CFG_PAGE + 15) : PQ#(16 * QTX_CFG_PAGE + 0)] 0: Disable drop by FFA percentage 1: Enable drop by FFA percentage
15:0	HW_DROP_PREC	**QDMA HW Drop by FFA Percentage Control** QDMA drop packets based on the full percentage of Free-for-All [15:0] = [PQ#(16 * QTX_CFG_PAGE + 15) : PQ#(16 * QTX_CFG_PAGE + 0)] 0: Disable drop by FFA percentage 1: Enable drop by FFA percentage

1B101A40 QDMA_HRED1 QDMA HW RED Distribution - I FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	FFA_LOW_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFA_MIDDLE_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	FFA_LOW_UTIL	**Low Utilization of FFA on HW path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 25% probability.
15:0	FFA_MIDDLE_UTIL	**Middle Utilization of FFA on HW path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 50% probability.

1B101A44 QDMA_HRED2 QDMA HW RED Distribution - II FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVo															FFA_UTIL_SEL
Type	RW															RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFA_HIGH_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:17	REVo	**Reserved**
16	FFA_UTIL_SEL	**Manually Set FFA Utilization** When the bit is set, FFA Utilization will be configurable for user.
15:0	FFA_HIGH_UTIL	**High Utilization of FFA on HW path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 75% probability.

1B101A48 QDMA_SRED1 QDMA SW RED Distribution - I FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FFA_LOW_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFA_MIDDLE_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	FFA_LOW_UTIL	**Low Utilization of FFA on HW path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 25% probability.
15:0	FFA_MIDDLE_UTIL	**Middle Utilization of FFA on CPU path**

Bit(s)	Name	Description
		When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 50% probability.

1B101A4C QDMA_SRED2 QDMA SW RED Distribution - II FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVo															FFA_UTIL_SEL
Type	RW															RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFA_MIDDLE_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:17	REVo	**Reserved**
16	FFA_UTIL_SEL	**Manually Set FFA Utilization** When the bit is set, FFA Utilization will be configurable for user.
15:0	FFA_MIDDLE_UTIL	**High Utilization of FFA on CPU path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 75% probability.

1B101A70 QDMA_INT_STS_Go QDMA Interrupt Status Group 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_STS_Go															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_STS_Go															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_STS_Go	**Interrupt group o status, this information already "and" with "QDMA_INT_IMR"** Each bit definition is same as "QDMA_INT_STS"

1B101A74 QDMA_INT_STS_G1 QDMA Interrupt Status Group 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_STS_G1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_STS_G1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_STS_G1	**Interrupt group 1 status, this information already "and" with "QDMA_INT_IMR"** Each bit definition is same as "QDMA_INT_STS"

1B101A78 QDMA_INT_STS_G2 QDMA Interrupt Status Group 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_STS_G2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_STS_G2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_STS_G2	**Interrupt group 2 status, this information already "and" with "QDMA_INT_IMR"** Each bit definition is same as "QDMA_INT_STS"

1B101A80 VQTX_GLO TX Virtual Queue Global Configuration 000005EA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															VQTB_MIB_EN	
Type															RW	
Reset															0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_GQTUM															
Type	RW															
Reset	0	0	0	0	0	1	0	1	1	1	1	0	1	0	1	0

Bit(s)	Name	Description
17	VQTB_MIB_EN	**Configuration for the MIB packet/byte counter field of virtual queue table** 0: Disable MIB counter field, each virtual table entry is 16bytes 1: Enable MIB counter field, each virtual table entry extends to 32bytes, to record the amount of transmitted byte and packet count for each virtual queue
15:0	VQTX_GQTUM	**Amount of bytes a virtual queue is allowed to de-queue before the scheduler moves to the next virtual queue. Defaults to the MTU of the interface. The minimum value is 1.**

1B101A8C VQTX_INVLD_PTR TX Virtual Queue Invalid Pointer DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_INVLD_PTR															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_INVLD_PTR															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	VQTX_INVLD_PTR	**The pointer address indicates a invalid virtual queue head/tail pointer.** Either "VQHPTR" or "VQTPTR" of VQ table is equal to this invalid pointer VQTX_INVLD_PTR, which means there is no valid packet in this virtual queue.

1B101A90 VQTX_NUM Number of TX Virtual Queue Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		VQTX_NUM_7				VQTX_NUM_6				VQTX_NUM_5				VQTX_NUM_4		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VQTX_NUM_3				VQTX_NUM_2				VQTX_NUM_1				VQTX_NUM_0		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	VQTX_NUM_7	**Number of virtual queues in virtual queue group #7**
26:24	VQTX_NUM_6	**Number of virtual queues in virtual queue group #6**
22:20	VQTX_NUM_5	**Number of virtual queues in virtual queue group #5**
18:16	VQTX_NUM_4	**Number of virtual queues in virtual queue group #4**
14:12	VQTX_NUM_3	**Number of virtual queues in virtual queue group #3**
10:8	VQTX_NUM_2	**Number of virtual queues in virtual queue group #2**
6:4	VQTX_NUM_1	**Number of virtual queues in virtual queue group #1**
2:0	VQTX_NUM_0	**Number of virtual queues in virtual queue group #0** 0: disable virtual queue function 1: 32 2: 64 3: 128 4: 256 5: 512 6: 1024 7: reserved

1B101A98 VQTX_SCH TX Virtual Queue Schedule Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VQTX_SCH_7				VQTX_SCH_6				VQTX_SCH_5				VQTX_SCH_4	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name			VQTX_SCH_3				VQTX_SCH_2				VQTX_SCH_1				VQTX_SCH_0	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Name	Description
29:28	VQTX_SCH_7	**Virtual queues scheduling strategy for virtual queue group #7**
25:24	VQTX_SCH_6	**Virtual queues scheduling strategy for virtual queue group #6**
21:20	VQTX_SCH_5	**Virtual queues scheduling strategy for virtual queue group #5**
17:16	VQTX_SCH_4	**Virtual queues scheduling strategy for virtual queue group #4**
13:12	VQTX_SCH_3	**Virtual queues scheduling strategy for virtual queue group #3**
9:8	VQTX_SCH_2	**Virtual queues scheduling strategy for virtual queue group #2**
5:4	VQTX_SCH_1	**Virtual queues scheduling strategy for virtual queue group #1**
1:0	VQTX_SCH_0	**Virtual queues scheduling strategy for virtual queue group #0** 0: SFQ (packet base round robin) 1: DRR (deficit round robin) 2: Reserved 3: Reserved

1B101AA0 VQTX_HASH_CFG TX Virtual Queue Hash Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					HASH_PTB_MODE_EN_3	HASH_PTB_MODE_EN_2	HASH_PTB_MODE_EN_1	HASH_PTB_MODE_EN_0			HASH_ST_MODE					HASH_PTB_PRD
Type					RW	RW	RW	RW			RW					RW
Reset					0	0	0	0			0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_PTB_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27	HASH_PTB_MODE_EN_3	**Enable "Exclusive with CRC32" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PTB_PRD!=0.**
26	HASH_PTB_MODE_EN_2	**Enable "Exclusive with (B^(A&~C))" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PTB_PRD!=0.**
25	HASH_PTB_MODE_EN_1	**Enable "Exclusive with (A&B)|(~A&C)" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PTB_PRD!=0.**
24	HASH_PTB_MODE_EN_0	**Enable "Exclusive with HASH_SEED" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PTB_PRD!=0.**

Bit(s)	Name	Description
		(If HASH_PTB_MODE_EN_0~3 are all "0", hash will be forced on "Exclusive with HASH_SEED" mode.)
21:20	HASH_ST_MODE	**Hash scrambled mode selection, for static hash virtual queue index generating.** This field only valid when HASH_PTB_PRD=0 3: Exclusive with CRC32 2: Exclusive with (B^(A&~C)) 1: Exclusive with (A&B)|(~A&C) 0: Exclusive with HASH_SEED
16:0	HASH_PTB_PRD	**If HASH_PTB_PRD = 0, means operating in static hash mode, never changing the hash algorithm periodically.** Otherwise, operating in perturb hash mode when HASH_PTB_PRD != 0. HASH_PERTURB_PRD Indicates the period to change the hash algorithm for virtual queue index generating, in 1ms unit.

1B101AA4 VQTX_HASH_SD TX Virtual Queue Hash Seed 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_SD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_SD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	HASH_SD	**Hash seed for "Exclusive with HASH_SEED" mode.**

1B101AB0 VQTX_VLD_CFG TX Virtual Queue Valid Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_VLD_STRG_7				VQTX_VLD_STRG_6				VQTX_VLD_STRG_5				VQTX_VLD_STRG_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_VLD_STRG_3				VQTX_VLD_STRG_2				VQTX_VLD_STRG_1				VQTX_VLD_STRG_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	VQTX_VLD_STRG_7	**Virtual Queue Group #7: Virtual queue valid bit map starting slice number.**
27:24	VQTX_VLD_STRG_6	**Virtual Queue Group #6: Virtual queue valid bit map starting slice number.**
23:20	VQTX_VLD_STRG_5	**Virtual Queue Group #5: Virtual queue valid bit map starting slice number.**
19:16	VQTX_VLD_STRG_4	**Virtual Queue Group #4: Virtual queue valid bit map starting slice number.**
15:12	VQTX_VLD_STRG_3	**Virtual Queue Group #3: Virtual queue valid bit map starting slice number.**

Bit(s)	Name	Description
11:8	VQTX_VLD_STRG_2	**Virtual Queue Group #2: Virtual queue valid bit map starting slice number.**
7:4	VQTX_VLD_STRG_1	**Virtual Queue Group #1: Virtual queue valid bit map starting slice number.**
3:0	VQTX_VLD_STRG_0	**Virtual Queue Group #0: Virtual queue valid bit map starting slice number.** 1 VQ valid bit slice comprises 64 bit map. The amount of VQ valid slices for 1 VQ group depends on the setting of "VQTX_NUM_#", hardware will allocate VQ valid bit slices for each VQ group. 4'h0: VQ valid bit map starting from slice#0 4'h1: VQ valid bit map starting from slice#1 4'h15: VQ valid bit map starting from slice#15

1B101ABC QTX_MIB_IF TX Queue MIB Interface 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			MIB_RC_DIS	VQTX_MIB_EN				MIB_PQ_SHW_SEP			QTX_MIB_QID					
Type			RW	W1				RW			RW					
Reset			0	0				0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							QTX_MIB_VQID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	MIB_RC_DIS	**Disable the clear action during MIB reading** 0: After MIB reading done, the target MIB counter will be clear to 0 1: Keeps the value of target MIB counter after MIB reading
28	VQTX_MIB_EN	**Enable VQTB MIB read procedure** 0: After MIB accessing done, HW will clear this bit to 0 and put the result in VQTX_MIB_PCNT, VQTX_MIB_DPCNT, VQTX_MIB_BCNT0, VQTX_MIB_BCNT1 1: Enable MIB accessing procedure
24	MIB_PQ_SHW_SEP	**Separate the PQ's HW/SW MIB counter of QTX_MIB_PCNT and QTX_MIB_DPCNT** 0: Use whole 32bits as one MIB counter, which accumulates SW and HW packet count 1: Separate the SW and HW MIB counter
21:16	QTX_MIB_QID	**Physical queue ID for MIB accessing**
9:0	QTX_MIB_VQID	**Virtual queue ID for MIB accessing**

1B101AC0 VQTX_MIB_PCNT TX Virtual Queue MIB Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_PCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_PCNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_PCNT	**Packet count of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID.** Unavailable when VQTB_MIB_EN = 0

1B101AC4 VQTX_MIB_BCNTL TX Virtual Queue MIB Byte Count Low Bytes 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_BCNTH															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_BCNTH															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_BCNTH	**Byte count [31:0] of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID.** Unavailable when VQTB_MIB_EN = 0

1B101AC8 VQTX_MIB_BCNTH TX Virtual Queue MIB Byte Count High Bytes 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_BCNTL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_BCNTL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_BCNTL	**Byte count [63:32] of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID.** Unavailable when VQTB_MIB_EN = 0

1B101ACC VQTX_MIB_DPCNT TX Virtual Queue MIB Drop Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_DPCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_DPCNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_DPCNT	**Dropped packet count of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID.** Unavailable when VQTB_MIB_EN = 0

1B101AD0 QTX_MIB_PCNT TX Physical Queue MIB Forward Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_MIB_PCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_MIB_PCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_MIB_PCNT	**Accumulated forwarded packet count, according to QTX_MIB_QID.** If MIB_PQ_SHW_SEP = 1, this counter will be separated into two 16bits counter, [31:16] for software path, [15:0] for hardware path.

1B101AD4 QTX_MIB_DPCNT TX Physical Queue MIB Dropped Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_MIB_DPCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_MIB_DPCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_MIB_DPCNT	**Accumulated dropped packet count, according to QTX_MIB_QID.** If MIB_PQ_SHW_SEP = 1, this counter will be separated into two 16bits counter, [31:16] for software path, [15:0] for hardware path.

1B101AD8 QTX_MIB_BCNTL TX Physical Queue MIB Byte Count Low Bytes 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_MIB_BCNTL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_MIB_BCNTL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_MIB_BCNTL	**Accumulated forwarded byte count [31:0] of physical queue #QTX_MIB_QID.** Read QTX_MIB_BCNTL will not clear the value of QTX_MIB_BCNTL, QTX_MIB_BCNTL will be cleared by reading QTX_MIB_BCNTH when VQTB_MIB_RC_DIS=0.

1B101ADC QTX_MIB_BCNTH TX Physical Queue MIB Byte Count High Bytes 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													QTX_MIB_BCNTH			
Type													RO			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	QTX_MIB_BCNTH	**Accumulated forwarded byte count [35:32] of physical queue #QTX_MIB_QID** If VQTB_MIB_RC_DIS=0, read QTX_MIB_BCNTH will clear the value of QTX_MIB_BCNTH & QTX_MIB_BCNTL.

1B101B00 QTX_CTX_PTR TX Forward CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FWD_CTX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FWD_CTX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FWD_CTX_PTR	**TX forward chain CPU pointer**

1B101B04 QTX_DTX_PTR TX Forward DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FWD_DTX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FWD_DTX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FWD_DTX_PTR	**TX forward chain DMA pointer** When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

1B101B08 QTX_FWD_CNT TX Forward DMA Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACC_HW_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACC_SW_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ACC_HW_CNT	**Accumulated HW forwarded counter**
15:0	ACC_SW_CNT	**Accumulated SW forwarded counter**

1B101B10 QTX_CRX_PTR TX Release CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLS_CRX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLS_CRX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RLS_CRX_PTR	**TX release chain CPU pointer**

1B101B14 QTX_DRX_PTR TX Release DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLS_DRX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLS_DRX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RLS_DRX_PTR	**TX release chain DMA pointer** When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

1B101B18 QTX_RLS_CNT TX Release DMA Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACC_RLS_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ACC_RLS_CNT	**Accumulated TX released descriptor count**

1B101B20 QDMA_FQ_HEAD Free Page Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FQ_HEAD_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FQ_HEAD_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FQ_HEAD_PTR	**Free buffer head pointer** When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

1B101B24 QDMA_FQ_TAIL Free Page Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FQ_TAIL_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FQ_TAIL_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FQ_TAIL_PTR	**Free buffer tail pointer** When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

Bit(s)	Name	Description

1B101B28 QDMA_FQ_CNT Free Page Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SWFQ_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HWFQ_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SWFQ_CNT	**Free buffer on CPU Pool** Initial free buffer count on CPU pool when QDMA_GLO_CFG.TX_DMA_EN is de-asserted.
15:0	HWFQ_CNT	**Free buffer on HW Pool** Initial free buffer count on HW pool when QDMA_GLO_CFG.TX_DMA_EN is de-asserted.

1B101B2C QDMA_FQ_BLEN Free Page Buffer Length 08000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			FQ_BUF_BLEN													
Type			RW													
Reset			0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
29:16	FQ_BUF_BLEN	**Free buffer byte length** Configured free buffer length, QDMA RX will fetch the length info to decide the payload length on one descriptor/buffer.

1B101BC0 VQTX_0_3_BIND_QID QDMA Virtual Queue Group #0~3 to Physical Queue Binding 03020100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VQTX_3_BIND_QID								VQTX_2_BIND_QID					
Type			RW								RW					
Reset			0	0	0	0	1	1			0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			VQTX_1_BIND_QID								VQTX_0_BIND_QID					
Type			RW								RW					
Reset			0	0	0	0	0	1			0	0	0	0	0	0

Bit(s)	Name	Description
29:24	VQTX_3_BIND_QID	The Physical Queue Number which binds with Virtual queue group #3
21:16	VQTX_2_BIND_QID	The Physical Queue Number which binds with Virtual queue group #2
13:8	VQTX_1_BIND_QID	The Physical Queue Number which binds with Virtual queue group #1
5:0	VQTX_0_BIND_QID	The Physical Queue Number which binds with Virtual queue group #0

1B101BC4 VQTX_4_7_BIND_QID QDMA Virtual Queue Group #4~7 to Physical Queue Binding 07060504

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VQTX_7_BIND_QID								VQTX_6_BIND_QID					
Type			RW								RW					
Reset			0	0	0	1	1	1			0	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			VQTX_5_BIND_QID								VQTX_4_BIND_QID					
Type			RW								RW					
Reset			0	0	0	1	0	1			0	0	0	1	0	0

Bit(s)	Name	Description
29:24	VQTX_7_BIND_QID	The Physical Queue Number which binds with Virtual queue group #7
21:16	VQTX_6_BIND_QID	The Physical Queue Number which binds with Virtual queue group #6
13:8	VQTX_5_BIND_QID	The Physical Queue Number which binds with Virtual queue group #5
5:0	VQTX_4_BIND_QID	The Physical Queue Number which binds with Virtual queue group #4

1B101BE0 QTX_FC_SW_STS_0_31 Tx Queue#0~31 Software Path Flow Control Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_FC_SW_STS_0_31															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_FC_SW_STS_0_31															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_FC_SW_STS_0_31	**Tx Queue Software Path Flow Control Status** Each bit indicates the flow control decision on each physical queue's packet from software path. [0]: PQ#0 .... [31]: PQ#31 0: Packet could be en-queued 1: Current incoming packets will be dropped

Bit(s)	Name	Description

1B101BE4 QTX_FC_SW_STS_32_63 Tx Queue#32~63 Software Path Flow Control Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_FC_SW_STS_32_63															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_FC_SW_STS_32_63															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_FC_SW_STS_32_63	**Tx Queue Software Path Flow Control Status** Each bit indicates the flow control decision on each physical queue's packet from software path. [0]: PQ#32 .... [31]: PQ#63 0: Packet could be en-queued 1: Current incoming packets will be dropped

3.2 Giga bit-Media Access Controller (GMAC)

3.2.1 Introduction

The MAC sub-layer defines a medium-independent facility, built on the medium-dependent physical facility provided by the Physical Layer, and under the access-layer-independent LAN LLC sub-layer (or other MAC client). It is applicable to a general class of local area broadcast media suitable for use with the media access discipline known as Carrier Sense Multiple Access with Collision Detection (CSMA/CD).

3.2.2 Features

- Support MAC layer functions of IEEE 802.3 and Ethernet
- Support 10/100/1000 Mbps bit rates
- Support Half/Full duplex supported (1000Mbps Half Duplex Mode is not support)
- Support per port SGMII / RGMII / MII / TMII / revMII interface
- Automatic 32-bit CRC generation and checking
- Support inter-Frame Gap Shrink (96bits-->64bits)
- Report packet status (good, CRC error, alignment, oversize, undersize, other MIBs information)
- Support flow control and automatic generation of control frames in full duplex mode (IEEE 802.3x)
- Support collision detection and auto retransmission on collisions in half duplex mode (CSMA/CD protocol)
- Support EEE(Energy Efficient Ethernet) capability for full duplex mode (IEEE 802.3az)
- Support packet length up to 15K for jumbo frames application
- 2 port GMAC (port 1 for LAN, port 2 for WAN)
- Support PHY indirect-access by MDIO
- Support WOL (wake on LAN)

3.2.3 Register Definition

Module name: GMAC Base address: (+1b110000h)

Address	Name	Width	Register Function
1B110000	MAC_PPSC	32	PHY Polling and SMI Master Control
1B110004	MAC_PIAC	32	PHY Indirect Access Control

1B110000 MAC_PPSC PHY Polling and SMI Master Control 45000504

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PHY_AP_EN	PHY_PRE_EN	PHY_MDC_CFG						RESV0			MDC_TURBO	RESV1		EE_AN_EN	
Type	RW	RW	RW						RW			RW	RW		RW	
Reset	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV2		PHY_END_ADDR						RESV3			PHY_START_ADDR				

Type	RW			RW					RW				RW			
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
31	PHY_AP_EN	**PHY auto polling enable** Indicate all PHY's status will be updated to PHY's status registers by PHY polling process.
30	PHY_PRE_EN	**PHY preamble enable** Indicates SMI master will send preamble bits (32-bits) at each MDIO read/write transaction. [note] This bit will affect both PHY polling mode and PHY indirect access mode.
29:24	PHY_MDC_CFG	**PHY MDC clock configuration** Used to configure the divider N for MDC clock frequency. MDC clock is sourced from 12.5MHz system clock and divided by N. [note] MDC clock is gated or disabled when PHY_MDC_CFG is set to 0.
23:21	RESV0	**Reserved**
20	MDC_TURBO	**MDC clock Turbo mode** When this bit is set, MDC clock is sourced from 25MHz system clock and divided by PHY_MDC_CFG.
19:18	RESV1	**Reserved**
17:16	EE_AN_EN	**PHY EEE auto-polling enable**
15:13	RESV2	**Reserved**
12:8	PHY_END_ADDR	**PHY polling end address** Indicate the end of PHY address of PHY auto-polling process. [note] The difference between and start and end must be 1.
7:5	RESV3	**Reserved**
4:0	PHY_START_ADDR	**PHY polling start address** Indicate the start of PHY address of PHY auto-polling process.

1B110004 MAC_PIAC PHY Indirect Access Control 00090000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PHY_ACS_ST	RESV0	MDIO_REG_ADDR					MDIO_PHY_ADDR					MDIO_CMD		NMDIO_ST	
Type	W1C	RW	RW					RW					RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDIO_RW_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PHY_ACS_ST	**PHY access start** Start to indirect access PHY's register. While PHY's register access is complete, this bit will be self-cleared to 0. 0: Idle or indirect access complete 1: Start PHY access
30	RESV0	**Reserved**
29:25	MDIO_REG_ADDR	**Register Address (Clause 22) or Device Address (Clause 45)**
24:20	MDIO_PHY_ADDR	**PHY Address (Clause 22) or Port Address (Clause 45)**
19:18	MDIO_CMD	**MDIO command** 2'b00: Address (Clause 45)

Bit(s)	Name	Description
		2'b01: MDIO write 2'b10: MDIO read (Clause 22) / Read inc (Clause 45) 2'b11: MDIO read (Clause 45)
17:16	NMDIO_ST	**MDIO Start Field** 2'b00: Start (Clause 45) 2'b01: Start (Clause 22) other: Reserved
15:0	MDIO_RW_DATA	**MDIO Read/Write data** This is used as MDIO data field for read/write data access. When MDIO write command is activated, this is used as MDIO write data field. When MDIO read command is activated, this is used as MDIO read data field for read access only.

3.3 Serial Gigabit Media Independent Interface (SGMII)

3.3.1 Introduction

The SGMII is the interface between 10/100/1000/2500 Mbps PHY and Ethernet MAC, the spec is raised by Cisco in 1999, which is aims for pin reduction compare with the GMII. It uses 2 differential data pair for TX and RX with clock embedded bit stream to convey frame data and port ability information. The core leverages the 1000Base-X PCS and Auto-Negotiation from IEEE 802.3 specification (clause 36/37). This IP can support up to 3.125G baud for 2.5Gbps (proprietary 2500Base-X) data rate of MAC by overclocking.

3.3.2 Features

- Support 10/100/1000/2500 Mbps in full duplex mode and 10/100 Mbps in half duplex mode
- Support programmable Link timer
- Support I2C interface for accessing
- Support internal pattern generator with PRBS-7/ clock / user defined pattern for testing
- Support PCS/SERDES level loopback path in transmit/receive direction for system debugging

3.3.3 Register Definition

Module name: sgmii_reg Base address: (+1b128000h)

Address	Name	Width	Register Function
1B128000	PCS_CONTROL_1	32	C45 3.1
1B128004	PCS_DEVICE_IDENTIFIER	32	C45 3.3
1B128008	PCS_SPEED_ABILITY	32	C45 3.5
1B12800C	PACKAGE_PRESENT	32	C45 3.7
1B128010	PCS_STATUS_2	32	C45 3.8
1B128014	PCS_SCRATCH	32	
1B128018	PCS_LINK_TIMER	32	
1B12801C	PCS_DEC_ERROR_CNT	32	
1B128020	SGMII_MODE	32	
1B128024	SGMII_RESERVED	32	
1B12802C	SGMII_WO_REG_VALUE	32	
1B128034	SGMII_RESERVED_0	32	C45 3.2001
1B128040	SGMII_RW_0	32	
1B12804C	INTERRUPT_CONTROL_0	32	
1B128050	INTERRUPT_CONTROL_1	32	
1B128060	QPHY_SIG_DET_CTRL	32	QPHY signal detect threshold control
1B1280C4	PAT_GEN_CTRL_0	32	Pattern Gen control_0
1B1280C8	PAT_GEN_CTRL_1	32	Pattern Gen control_1
1B1280CC	PAT_GEN_CTRL_2	32	Pattern Gen control_2

Address	Name	Width	Register Function
1B1280D0	PAT_GEN_CTRL_3	32	Pattern Gen control_3
1B1280E8	QPHY_PWR_STATE_CTRL	32	QPHY power state control
1B1280EC	QPHY_WRAP_CTRL	32	QPHY wrapper control
1B1280F0	I2C_CTRL	32	I2C interface control

1B128000 PCS_CONTROL_1 C45 3.1 00001140

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		SGMII_AN_EXPANSION_CLR							SGMII_PCS_FAULT		SGMII_AN_COMPLETE		SGMII_AN_ABILITY	SGMII_LINK_STATUS		
Type		WO							RO		RO		RO	RO		
Reset		0							0		0		0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SGMII_AN_ENABLE		SGMII_ISOLATE	SGMII_AN_RESTART									
Type				RW		RW	WO									
Reset				1		0	0									

Bit(s)	Name	Description
30	SGMII_AN_EXPANSION_CLR	**Page_Receive flag clear** 1'b0 : no effect 1'b1 : reset @SGMII_AN_EXPANSION_12_0[1] to 0
23	SGMII_PCS_FAULT	**SGMII fault condition detection** 1'b0 : No fault condition detected 1'b1 : Fault condition detected (txfifo_full or rxfifo_empty)
21	SGMII_AN_COMPLETE	**AN complete** 1'b0 : AN not complete 1'b1 : when @SGMII_AN_ENABLE=1, @SGMII_SW_RESET=0 and an_done is synchronized from rx_mii_ck to csr_ck
19	SGMII_AN_ABILITY	**Auto-Negotiation ability** 1'b0 : PHY is not able to perform Auto-Negotiation 1'b1 : PHY is able to perform Auto-Negotiation
18	SGMII_LINK_STATUS	**Signal link_status** 1'b0 : when loss of sync 1'b1 : when acquire sync (if SGMII_AN_ENABLE = 1, it will check if SGMII_AN_COMPLETE = 1 as well)
12	SGMII_AN_ENABLE	**Auto-negotiation enable** 1'b0 : disable 1'b1 : enable
10	SGMII_ISOLATE	**SGMII software reset** 1'b0 : no effect 1'b1 : reset SGMII design
9	SGMII_AN_RESTART	**Auto-negotiation restart (self clear)** 1'b0 : no effect 1'b1 : restart auto-negotiation

1B128004 PCS_DEVICE_IDENTIFIER C45 3.3 4D544950

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SGMII_PHY_IDENTIFIER_REG3															
Type	RO															
Reset	0	1	0	0	1	1	0	1	0	1	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGMII_PHY_IDENTIFIER_REG2															
Type	RO															
Reset	0	1	0	0	1	0	0	1	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
31:16	SGMII_PHY_IDENTIFIER_REG3	**Version tag of SGMII**
15:0	SGMII_PHY_IDENTIFIER_REG2	**Version tag of SGMII**

1B128008 PCS_SPEED_ABILITY C45 3.5 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SGMII_PARTNER_ABILITY_15_11					SGMII_PARTNER_ABILITY_10	SGMII_PARTNER_ABILITY_9	SGMII_PARTNER_ABILITY_8	SGMII_PARTNER_ABILITY_7	SGMII_PARTNER_ABILITY_6	SGMII_PARTNER_ABILITY_5	SGMII_PARTNER_ABILITY_4	SGMII_PARTNER_ABILITY_3	SGMII_PARTNER_ABILITY_2	SGMII_PARTNER_ABILITY_1	SGMII_PARTNER_ABILITY_0
Type	RO					RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGMII_DEV_ABILITY_15	SGMII_ANACK	SGMII_DEV_ABILITY_13_4										SGMII_DEV_ABILITY_3	SGMII_DEV_ABILITY_2	SGMII_DEV_ABILITY_1	SGMII_DEV_ABILITY_0
Type	RW	RO	RW										RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:27	SGMII_PARTNER_ABILITY_15_11	**link partner's advertised ability, bit 15 to 11**
26	SGMII_PARTNER_ABILITY_10	**link partner's advertised ability, bit 10**
25	SGMII_PARTNER_ABILITY_9	**link partner's advertised ability, bit 9**
24	SGMII_PARTNER_ABILITY_8	**link partner's advertised ability, bit 8**
23	SGMII_PARTNER_ABILITY_7	**link partner's advertised ability, bit 7**
22	SGMII_PARTNER_ABILITY_6	**link partner's advertised ability, bit 6**
21	SGMII_PARTNER_ABILITY_5	**link partner's advertised ability, bit 5**
20	SGMII_PARTNER_ABILITY_4	**link partner's advertised ability, bit 4**
19	SGMII_PARTNER_ABILITY_3	**link partner's advertised ability, bit 3**
18	SGMII_PARTNER_ABILITY_2	**link partner's advertised ability, bit 2**
17	SGMII_PARTNER_ABILITY_1	**link partner's advertised ability, bit 1**
16	SGMII_PARTNER_ABILITY_0	**link partner's advertised ability, bit 0**
15	SGMII_DEV_ABILITY_15	**local device's advertised ability, bit 15**
14	SGMII_AN_ACK	**ACK to link partner's auto-negotiation**
13:4	SGMII_DEV_ABILITY_13_4	**local device's advertised ability, bit 13 to 4**
3	SGMII_DEV_ABILITY_3	**local device's advertised ability, bit 3**
2	SGMII_DEV_ABILITY_2	**local device's advertised ability, bit 2**
1	SGMII_DEV_ABILITY_1	**local device's advertised ability, bit 1**
0	SGMII_DEV_ABILITY_0	**local device's advertised ability, bit 0 (1 indicating SGMII mode)**

Bit(s)	Name	Description

1B12800C PACKAGE_PRESENT C45 3.7 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGMII_AN_EXPANSION_15	SGMII_AN_EXPANSION_14	SGMII_AN_EXPANSION_13	SGMII_AN_EXPANSION_12_0												
Type	RO	RO	RO	RO												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15	SGMII_AN_EXPANSION_15	AN expansion register bit 15, always 0
14	SGMII_AN_EXPANSION_14	AN expansion register bit 14, always 0
13	SGMII_AN_EXPANSION_13	AN expansion register bit 13, always 0
12:0	SGMII_AN_EXPANSION_12_0	AN expansion register bit 12 to 0, bit 12 to 2 are always 11'd1, bit 1 is 0 when AN entering restart state (high priority) or is 1 when receive link partner's page cycle (medium priority) or is 0 when @SGMII_AN_EXPANSION_CLR is 1

1B128010 PCS_STATUS_2 C45 3.8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SGMII_TX_FAULT_LATCH	SGMII_RX_FAULT_LATCH										
Type					RO	RO										
Reset					0	0										

Bit(s)	Name	Description
11	SGMII_TX_FAULT_LATCH	indicate TXFIFO full event
10	SGMII_RX_FAULT_LATCH	indicate RXFIFO empty event

1B128014 PCS_SCRATCH 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SGMII_DEV_VERSION															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGMII_SCRATCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SGMII_DEV_VERSION	**device version, always 16'd1**
15:0	SGMII_SCRATCH	**scratch register, reserved**

1B128018 PCS_LINK_TIMER 00098968

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SGMII_LINK_TIMER			
Type													RW			
Reset													1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGMII_LINK_TIMER															
Type	RW															
Reset	1	0	0	0	1	0	0	1	0	1	1	0	1	0	0	0

Bit(s)	Name	Description
19:0	SGMII_LINK_TIMER	**Programmable link timer, delay time = SGMII_LINK_TIMER*2*(SGMII : 8ns / HSGMII : 3.2ns)**

1B12801C PCS_DEC_ERROR_CNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGMII_DEC_ERROR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SGMII_DEC_ERROR_CNT	**decode error count, reset when @SGMII_ISOLATE=1 or @SGMII_SW_RESET=1, increase when character error or disparity error**

1B128020 SGMII_MODE 3112001B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SGMII_SEND_A	SGMII_CODE_S	SGMII_CODE_S	SGMII_REMOT			SGMII_IF_MODE_5_0					

					N_ERROR_EN	SYNC_SET_EN	SYNC_SET_VAL	E_FAULT_DIS								
Type					RW	RW	RW	RW			RW					
Reset					0	0	0	0			0	1	1	0	1	1

Bit(s)	Name	Description
11	SGMII_SEND_AN_ERROR_EN	**Remote fault control during AN** 1'b0 : don't send remote fault when capability is not match 1'b1 : send remote fault when capability is not match
10	SGMII_CODE_SYNC_SET_EN	**Manually set code_sync enable bit** 1'b0 : disable 1'b1 : enable
9	SGMII_CODE_SYNC_SET_VAL	**Manually set code_sync value when SGMII_CODE_SYNC_SET_EN = 1** 1'b0 : sync loss 1'b1 : sync acquired
8	SGMII_REMOTE_FAULT_DIS	**Update control of Remote Fault** 1'b0 : tx_config_reg[13:12] = 10 when SGMII_DEV_ABILITY_13_4[9:8] is 10, tx_config_reg[13:12] = 01 when remaining in link fail state, tx_config_reg[13:12] = 11 when remaining in AN error state, and tx_config_reg[13:12] = 00 when normal state. Priority of all above states are from high to low. 1'b1 : tx_config_reg[13:12] is from SGMII_DEV_ABILITY_13_4[9:8] (sw control totally)
5:0	SGMII_IF_MODE_5_0	**Interface mode** [0] : need to set 1, do not change [1] : enable of advertising speed and duplex by AN [3:2] : force speed setting when [1] = 0, 2'b00 : 10Mbps / 2'b01 : 100Mbps / 2'b10 : 1Gbps / 2'b11 : reserved [4] : force duplex setting when [1] = 0, 1'b0 : full duplex / 1'b1 : half duplex [5] : reserved

1B128024 SGMII_RESERVED 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SGMII_RESERVED_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGMII_RESERVED_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SGMII_RESERVED_REG	**reserved registers**

1B12802C SGMII_WO_REG_VALUE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SGMII_RO_SW_RESET	SGMII_RO_AN_RESTART	SGMII_RO_AN_EXPANSIO	SGMII_RO_LINK_RST

															N_CLR	
Type													RO	RO	RO	RO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
19	SGMII_RO_SW_RESET	**Read only signal for debug**
18	SGMII_RO_AN_RESTART	**Read only signal for debug**
17	SGMII_RO_AN_EXPANSION_CLR	**Read only signal for debug**
16	SGMII_RO_LINK_RST	**Read only signal for debug**

1B128034 SGMII_RESERVED_0 C45 3.2001 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SGMII_SW_RESET
Type																WO
Reset																0

Bit(s)	Name	Description
0	SGMII_SW_RESET	**SGMII design reset** 1'b0 : no effect 1'b1 : reset

1B128040 SGMII_RW_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		SGMII_PCS_DEC_ERROR_CNT_READ_LATCH														
Type		RW														
Reset		0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
30	SGMII_PCS_DEC_ERROR_CNT_READ_LATCH	**Latch current decode error count to SGMII_DEC_ERROR_CNT for read** 1'b0 : no effect 1'b1 : latch

1B12804C INTERRUPT_CONTROL_0 FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INTS_MASK															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INTS_CLEAR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	INTS_MASK	**Interrupt mask** [15] : link up [14] : link down [13] : AN done [12] : re AN [11] : tx basepage [10] : rx basepage [9] : tx nextpage [8] : rx nextpage [7] : remote fault [6] : coding error [5] : tx fifo ptr error [4] : rx fifo ptr error [3] : reserved [2] : reserved [1] : reserved [0] : reserved
15:0	INTS_CLEAR	**Interrupt clear (self-clear)** [15] : link up [14] : link down [13] : AN done [12] : re AN [11] : tx basepage [10] : rx basepage [9] : tx nextpage [8] : rx nextpage [7] : remote fault [6] : coding error [5] : tx fifo ptr error [4] : rx fifo ptr error [3] : reserved [2] : reserved [1] : reserved [0] : reserved

1B128050 INTERRUPT_CONTROL_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INTS_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31:16	INTS_STATUS	**Interrupt Status** [15] : link up [14] : link down [13] : AN done [12] : re AN [11] : tx basepage [10] : rx basepage [9] : tx nextpage [8] : rx nextpage [7] : remote fault [6] : coding error [5] : tx fifo ptr error [4] : rx fifo ptr error [3] : reserved [2] : reserved [1] : reserved [0] : reserved

1B128060 QPHY_SIG_DET_CTRL QPHY signal detect threshold control 40120005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FRC_SIG_DET	SIG_DET_CR														
Type	RW	RW														
Reset	0	1														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	FRC_SIG_DET	**PCS's signal_detect input force mode** 1'b0 : disable 1'b1 : enable
30	SIG_DET_CR	**Control PCS's signal_detect input value if FRC_SIG_DET = 1** 1'b0 : signal not detected 1'b1 : signal detected

1B1280C4 PAT_GEN_CTRL_0 Pattern Gen control_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UDP_DATA_15_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								BIST_ERR	BIST_RUN	BIST_OK	PRBS_INJERR	RENEW_MODE	PRBS_MODE		PRBS_CHECK	PRBS_EN
Type								RO	RO	RO	RW	RW	RW		RW	RW
Reset								0	0	0	0	0	0		0	0

Bit(s)	Name	Description
31:16	UDP_DATA_15_0	**User define pattern [15:0]**
8	BIST_ERR	**BIST Error flag (error bit received)**
7	BIST_RUN	**BIST Run flag (Pattern generate and check period)**
6	BIST_OK	**BIST OK flag (no error bit received)**
5	PRBS_INJERR	**PRBS pattern error bits injection** 1'b0 : TX send PRBS pattern normally 1'b1 : TX send specific pattern 20'h5a5a5
4	RENEW_MODE	**Mode of Next PRBS golden pattern generation for check** 1'b0 : using first RX data to polynomial LFSR 1'b1 : using every RX data to polynomial LFSR
3:2	PRBS_MODE	**Type of pattern for generation** 2'b00 : PRBS-7 2'b01 : User define pattern 2'b10 : Clock pattern 2'b11 : No used
1	PRBS_CHECK	**Start to calculate PRBS error count enable** 1'b0 : no active 1'b1 : active
0	PRBS_EN	**Pattern Gen enable** 1'b0 : disable 1'b1 : enable

1B1280C8 PAT_GEN_CTRL_1 Pattern Gen control_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UDP_DATA_47_16															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UDP_DATA_47_16															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	UDP_DATA_47_16	**User define pattern [47:16]**

1B1280CC PAT_GEN_CTRL_2 Pattern Gen control_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UDP_DATA_79_48															
Type	RW															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UDP_DATA_79_48															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	UDP_DATA_79_48	**User define pattern [79:48]**

1B1280D0 PAT_GEN_CTRL_3 Pattern Gen control_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIST_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BIST_ERR_CNT	**PRBS error count**

1B1280E8 QPHY_PWR_STATE_CTRL QPHY power state control 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PHYA_PWD				
Type												RW				
Reset												1				

Bit(s)	Name	Description
4	PHYA_PWD	**Power down SERDES totally** 1'b0 : QPHY is under power on state 1'b1 : QPHY is under power down state

1B1280EC QPHY_WRAP_CTRL QPHY wrapper control 00000500

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name										TBI_RX_DISABLE	TBI_TX_DISABLE	PCS_R2T_LOOPBACK	QPHY_R2T_LOOPBACK	PCS_T2R_LOOPBACK	RX_BIT_POLARITY	TX_BIT_POLARITY
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	TBI_RX_DISABLE	**TBI interface of RX data disable** 1'b0 : enable RX data 1'b1 : disable RX data
5	TBI_TX_DISABLE	**TBI interface of TX data disable** 1'b0 : enable TX data 1'b1 : disable TX data
4	PCS_R2T_LOOPBACK	**PCS level RX loopback to TX enable** 1'b0 : disable 1'b1 : enable
3	QPHY_R2T_LOOPBACK	**PMA level RX loopback to TX enable** 1'b0 : disable 1'b1 : enable
2	PCS_T2R_LOOPBACK	**PCS level TX loopback to RX enable** 1'b0 : disable 1'b1 : enable
1	RX_BIT_POLARITY	**RX bit polarity control** 1'b0 : normal 1'b1 : inversed
0	TX_BIT_POLARITY	**TX bit polarity control** 1'b0 : normal 1'b1 : inversed

1B1280F0 I2C_CTRL I2C interface control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															I2C_MODE	I2C_MODE_CR_CTRL_SEL
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	I2C_MODE	**CR accessing source control when I2C_MODE_CR_CTRL_SEL = 1** 1'b0 : form AXI bus 1'b1 : from external I2C
0	I2C_MODE_CR_CTRL_SEL	**CR accessing source control** 1'b0 : depend on test_mode by strap to decide CR access form AXI bus(0) or external I2C(1) 1'b1 : depend on I2C_MODE to decide CR access form AXI bus(0) or external I2C(1)

Bit(s)	Name	Description

Module name: sgmii_reg_phya Base address: (+1b12a000h)

Address	Name	Width	Register Function
1B12A028	OFFSETX28H	32	ANA RG_ Control Signals III

1B12A028 OFFSETX28H ANA RG_ Control Signals III 00014813

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_TPHY_SPEED			
Type													RW			
Reset													0	0		

Bit(s)	Mnemonic	Name	Description
3:2		RG_TPHY_SPEED	**Speed select** 2'b00: 1.25G bps (SGMII 1G) 2'b01: 3.125G bps (SGMII 2.5G)