



FLIK

**World's First
Portable Accelerator
for Your Laptop!**



Terasic Overview

World Leading FPGA-Based Product Designer & Manufacturer

Terasic is the leading developer and provider for FPGA-based hardware & complex system solution. With twenty years of experience in developing high-end solutions for the industrial and FPGA system markets, our team provides the first-class design-to-order services for high speed boards and custom rugged system solutions to help our customers achieve their demanding applications in High Performance Computing, High Frequency Trading, network processing, radar detection, instrumentation, etc.

Headquartered in Hsinchu, Taiwan, the silicon valley of Asia and the cradle of invention and creativity, Terasic boasts an extensive product portfolio from COTS of PCIe boards, high speed boards, FMC & HSMC daughter cards for networking & video processing to cost-friendly educational & development kits widely used by today's college education and worldwide research institutes.

Our technical coverage:

- FPGA board design & layout
- Firmware & Drivers
- Signal integrity analysis
- SoC application
- OpenCL BSP porting & support
- OpenVINO and OPAAE Support

Terasic is Intel's official global service provider for OpenCL™ BSP Service

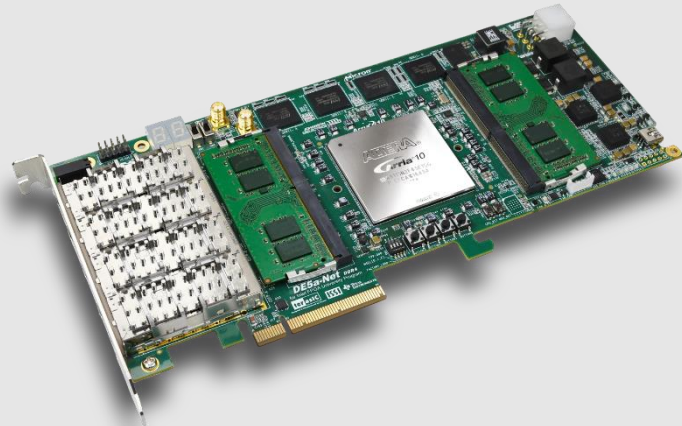


FPGA Design
Solutions Network
Platinum

As Intel certified service provider for OpenCL-related services & development, Terasic also provides customized service to meet the exact needs of our client.

- Support OpenCL™ HPC, SoC, and Networking BSPs.
- Customize FPGA Board and OpenCL BSP.
- Terasic FPGA Board integrate Customized IPs.
- Upgrade OpenCL BSP to the latest version.
- Modify hardware of Terasic FPGA Board, example: Memory Size

Terasic platforms support Intel FPGA Acceleration Hub



Dynamically Allocate Intel® FPGAs for Workload Optimization

Enhanced End-User Experience

Focus on System Architecture

Fast-Track Your Performance

Workload Optimization with Less Effort

Common Developer Interface for Intel® FPGA Data Center Products

Decrease server TCO, simplify management

Rack-Level Solutions

User Applications

Industry Standard Software Frameworks

Acceleration Libraries

Intel® Developer Tools

(Intel Quartus® Prime, Intel FPGA SDK for OpenCL™, Intel Parallel Studio XE)

Acceleration Environment

(Intel Acceleration Engine with OPAE Technology, FPGA Interface Manager (FIM))

OS & Virtualization Environment



Intel® Hardware



OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission by Khronos. Some names pending final approval and may change in the future.

Terasic platforms support Intel OpenVINO™ Toolkit

OpenVINO 2020 R1 version is now available on Terasic Stratix 10, and Arria 10 boards and Starter Platform for OpenVINO™ toolkit.

Demonstrations:

- Face Detection
- Emotion Recognition
- Age and Gender Recognition
- Head Pose Estimation
- Object Detection
- Object Segmentation
- Person Re-identification
- Vehicle Detection





Product Features

FLIK – FPGA Client Innovation Kit



Major Specs and Interfaces

- Arria 10 FPGA Board with Thunderbolt 3 connection
- Kit Features:
 - Arria 10 GX 1150K
 - Two DDR4 x64 Data Bus for 8GB total
 - PCIe Gen 3 x4 via Type-C Thunderbolt 3 interface
 - Board Management Controller includes Power, Temperature, Fan, and LED Control

FLIK Layout



Laser Engraved Logo
with Polished Surface

Fingerprint-resistant
Aluminum Alloy Chassis



Cellular Metal Filter

Plating and Shining

RGB LED Status Bar

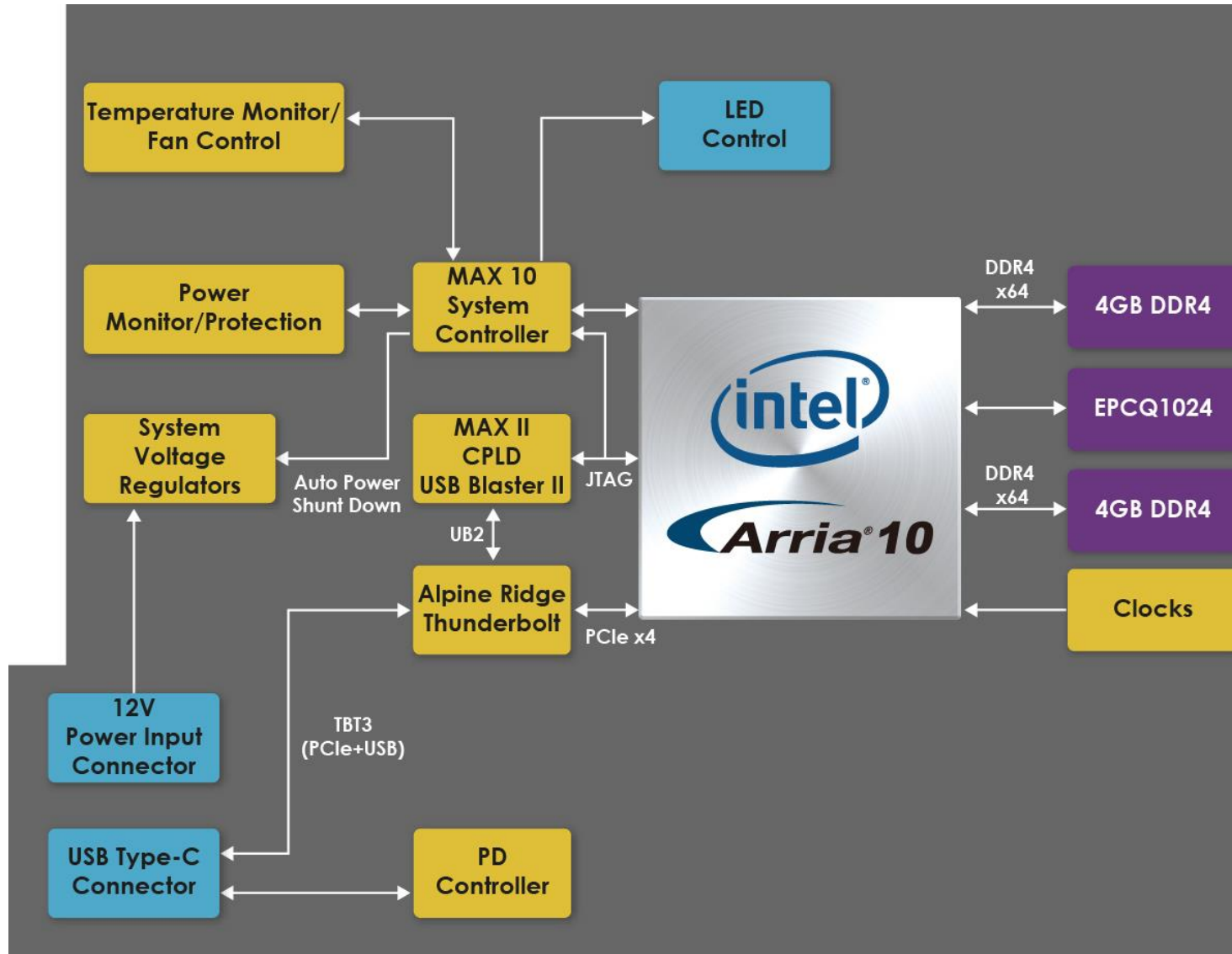


Anode Treatment with
Sandblasting Process

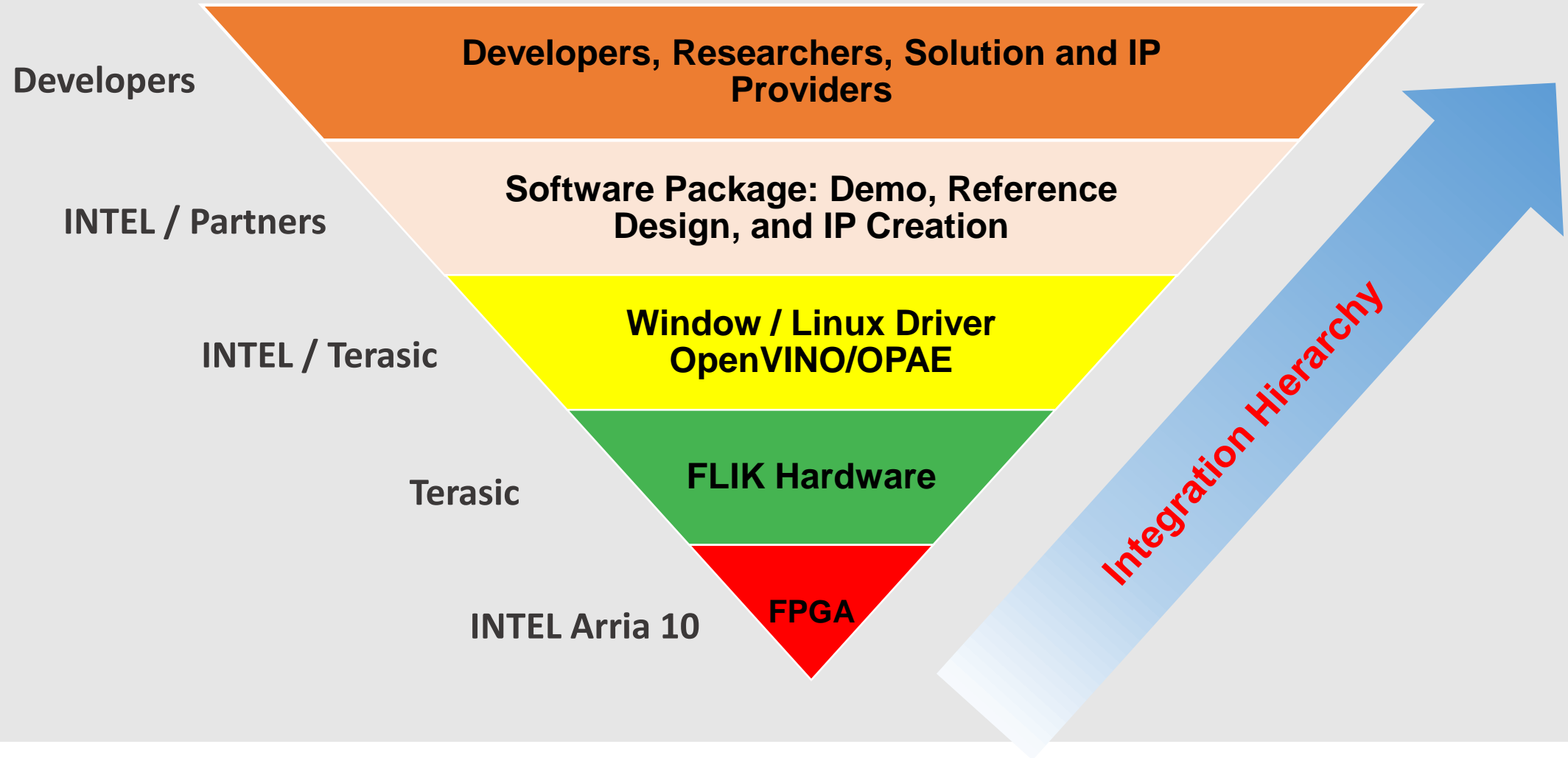
DC 12V Power

Thunderbolt 3 Port
Support 40Gbps Bandwidth

Block Diagram



Goal of FLIK: An integrated System for Global Developers for AI and FPGA Acceleration



Hardware

Package

Preparation

Chassis and ID Look

Thickness increased from 0.5mm to 0.8mm –
Done by Intel and Terasic

Board Manufacture

Design circuitry has been validated and verified –
Done by Terasic

Accessories

Includes power supply and Thunderbolt cable –
Done by Terasic

Package Design

Package / Box Design – Done by Terasic and
approved by INTEL

Software

Contents

1

Pre-programmed Power-on
Self-test Suite

2

OpenVINO Toolkit Demos

3

OPAE Enablement with Examples
(working in progress)

4

OpenCL for Windows 10

5

Adobe Premiere Pro Plugin

1. Pre-programmed Power-on Self-test Suite

- FPGA Boot from EPCQL1024 to see the board is powered up correctly
- Thunderbolt Link Status to check if a Thunderbolt cable is connected or disconnected
- DMA Access between Host PC and DDR4 on FLIK via PCIe Gen3 x4 up to 32Gbps
- Read/Write Data Transfer between FPGA and Two Bank 4GB DDR4@2133 MT/S (1066MHz)
- Power and Temperature Monitor to keep tracking power consumption and the temperature of FPGA and hotspots such as power modules

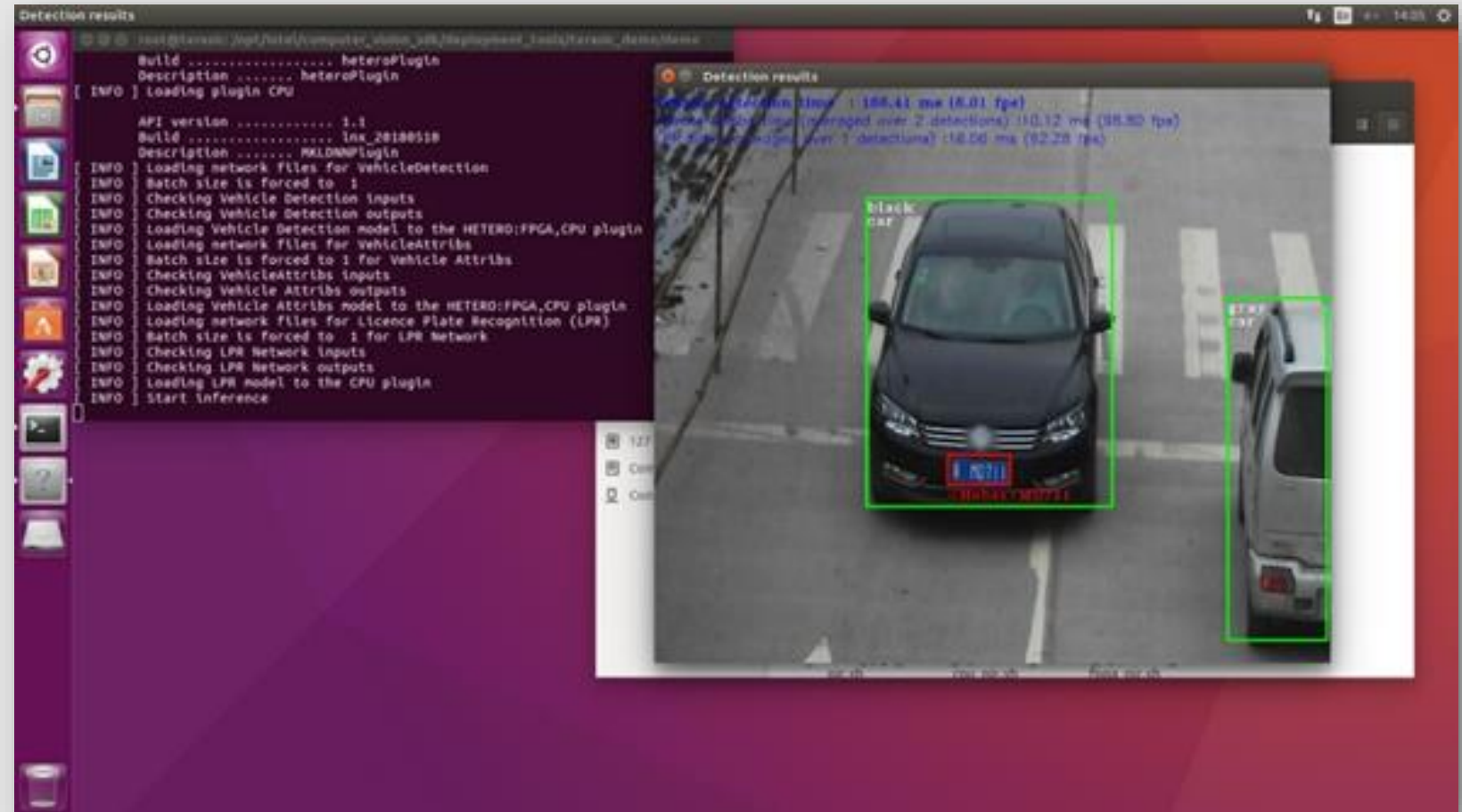
Performance between FLIK and CPU

OpenVINO Benchmark Application Demo

	Arria 10 FPGA	6th Gen i7 series CPU
Latency	2.00 ms	6.82 ms
Throughput	647.23 FPS	243.09 FPS

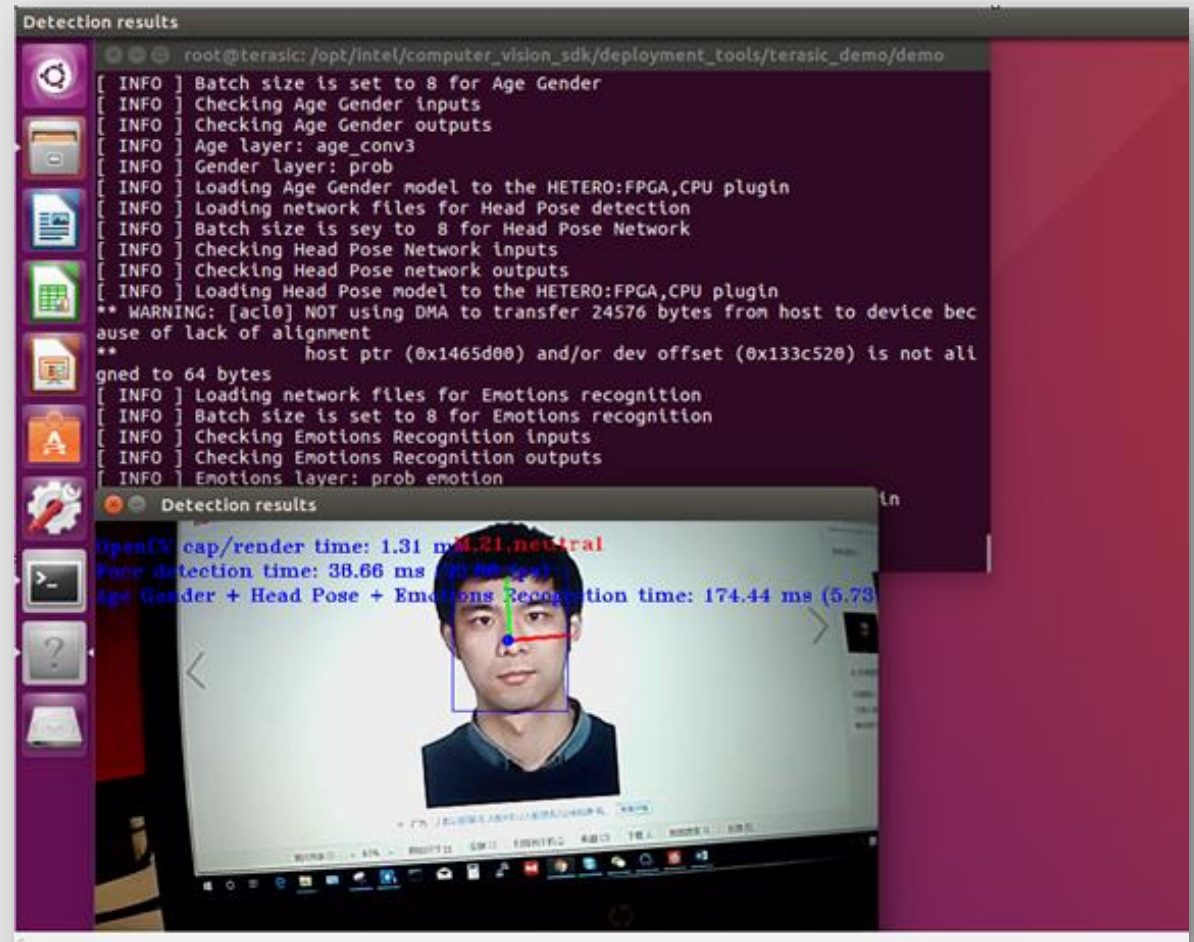
2. Demos for OpenVINO™ ToolKit on FLIK (1/3)

- Security Barrier – This demo can recognize the car, car license number and its location by using the three models.



2. OpenVINO™ ToolKit Demos on FLIK (2/3)

- Face detection - This demo used four models and it can recognize human face position in the figure. It can also judge the human gender, age, expression, and head gesture according to the human face.



```
Detection results
root@terasic: /opt/intel/computer_vision_sdk/deployment_tools/terasic_demo/demo
[ INFO ] Batch size is set to 8 for Age Gender
[ INFO ] Checking Age Gender inputs
[ INFO ] Checking Age Gender outputs
[ INFO ] Age layer: age_conv3
[ INFO ] Gender layer: prob
[ INFO ] Loading Age Gender model to the HETERO:FPGA,CPU plugin
[ INFO ] Loading network files for Head Pose detection
[ INFO ] Batch size is set to 8 for Head Pose Network
[ INFO ] Checking Head Pose Network inputs
[ INFO ] Checking Head Pose network outputs
[ INFO ] Loading Head Pose model to the HETERO:FPGA,CPU plugin
** WARNING: [acl0] NOT using DMA to transfer 24576 bytes from host to device because of lack of alignment
** host ptr (0x1465d00) and/or dev offset (0x133c520) is not alligned to 64 bytes
[ INFO ] Loading network files for Emotions recognition
[ INFO ] Batch size is set to 8 for Emotions recognition
[ INFO ] Checking Emotions Recognition inputs
[ INFO ] Checking Emotions Recognition outputs
[ INFO ] Emotions layer: prob emotion

OpenCL cap/render time: 1.31 ms, neutral
Face detection time: 38.66 ms (5.73)
Age Gender + Head Pose + Emotions Recognition time: 174.44 ms (5.73)
```

The screenshot shows a terminal window with a list of log messages from the OpenVINO toolkit. The messages include information about batch sizes, model loading, and a warning about DMA usage. Below the terminal, a video player displays a video of a man's face. The video player has overlaid text showing performance metrics: 'OpenCL cap/render time: 1.31 ms, neutral', 'Face detection time: 38.66 ms (5.73)', and 'Age Gender + Head Pose + Emotions Recognition time: 174.44 ms (5.73)'. The video frame shows a blue bounding box around the man's face and red lines indicating head pose.

2. OpenVINO™ ToolKit Demos on FLIK (3/3)

- GoogleNet – This demo can recognize the target object by using GoogleNetV2, the object tags are shown in figure below:

The image displays a Linux desktop environment with several windows. On the left, a terminal window shows the output of the OpenVINO demo, including API version (1.1), build number (11653), and inference results for a chair. The results list the number of proposals found for various classes, with 'chair' having 185 proposals. In the center, a video player window shows a chair with a red bounding box and the label 'chair 0.94'. The video player also displays performance metrics: 'OpenCV call time: 0.44 ms', 'Wallclock time (SYNC, press Tab): 35', and 'Detection time: 348.57 ms (2.87 fps)'. On the right, a file manager window shows a directory containing various shell scripts, including '04_GoogleNetV2_FPGA_camera.sh'.

Rank	Object
1	aeroplane
2	bicycle
3	bird
4	boat
5	bottle
6	bus
7	car
8	cat
9	chair
10	cow
11	diningtable
12	dog
13	horse
14	motorbike
15	person
16	pottedplant
17	sheep
18	sofa
19	train
20	tvmonitor

```
Detection results
root@terasic: /opt/intel/computer_vision_sdk/deployment_tools/terasic_demo/demo
API version ..... 1.1
Build ..... 11653
[ INFO ] Parsing input parameters
[ INFO ] Reading input
[ INFO ] Loading plugin

API version ..... 1.1
Build ..... heteroPlugin
Description ..... heteroPlugin
[ INFO ] Loading network files
[ INFO ] Batch size is forced to 1.
[ INFO ] Checking that the inputs are as the sample expects
[ INFO ] Checking that the outputs are as the sample expects
[ INFO ] Loading model to the plugin
[ INFO ] Start inference
Only 191 proposals found
Only 157 proposals found
Only 111 proposals found
Only 150 proposals found
Only 185 proposals found
Only 174 proposals found
Only 192 proposals found
Only 170 proposals found
```

OpenCV call time: 0.44 ms
Wallclock time (SYNC, press Tab): 35
Detection time: 348.57 ms (2.87 fps)

chair 0.94

3. OPAE Enablement with Examples for Intel Acceleration Stack

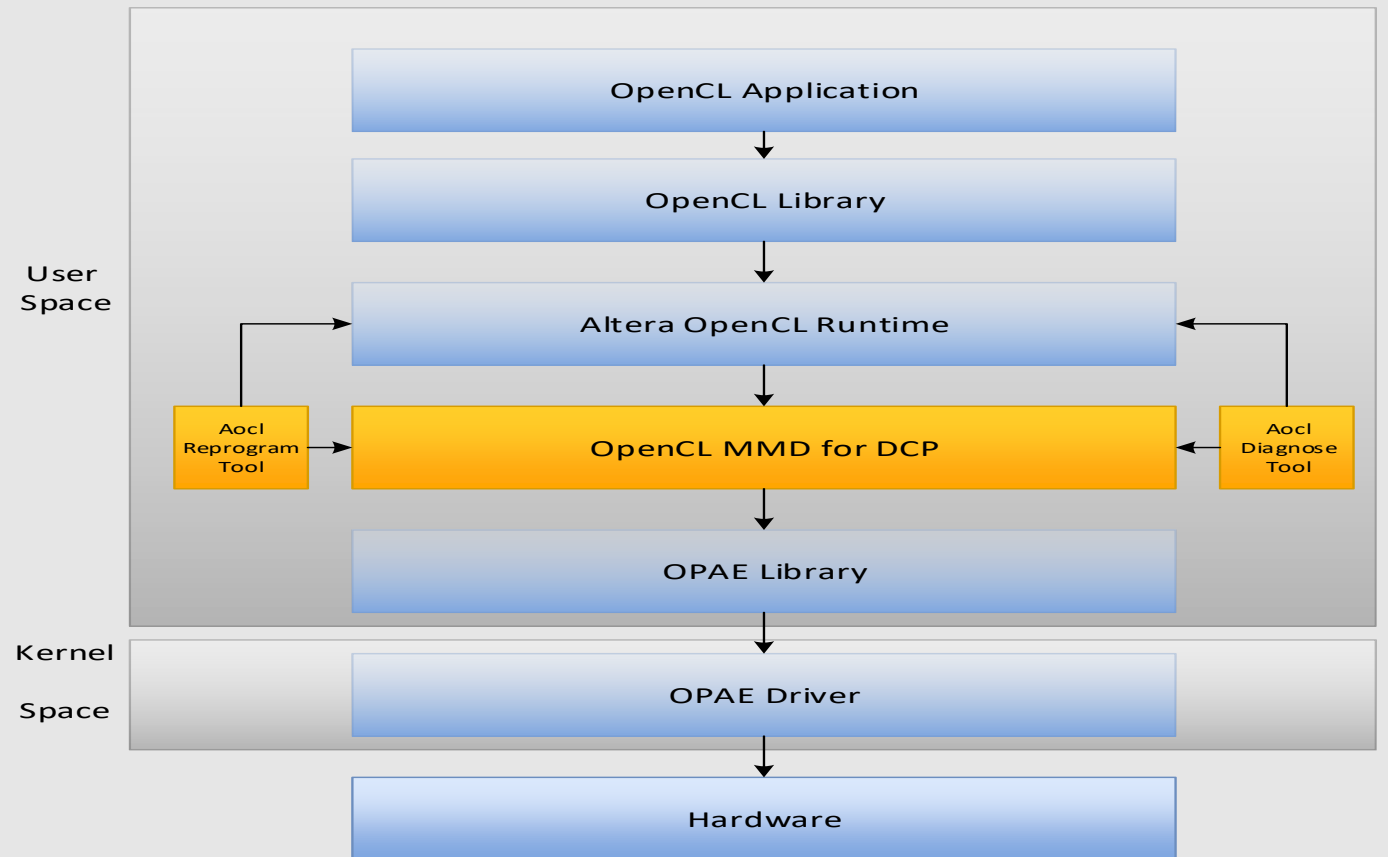
- The direct memory access (DMA) AFU test transfers data from host memory to FPGA-attached local memory (**dma_afu**)
- **hello_intr_afu** demonstrates the user interrupt feature in ASE
- **hello_mem_afu** demonstrates an AFU that builds a simple state machine to access memory
- **nlb_mode_0_stp** is a CCI-P system demonstrating the memory copy test.
- **nlb_mode_3** is a native loopback (NLB) test implements a loopback from TX to RX

4. OpenCL for Windows 10

One of the expectations for FLIK is for application developers to use SDK APIs and libraries to communicate with the FPGA OpenCL based IP.

Additional SDK can be built on top of OpenCL for FPGA development. For examples,

- Deep Learning SDK implementing CNNs,
- Intel's Computer Vision SDK (CVSDK),
- Microsoft's Machine Learning (ML) SDK.



5. FLIK's benchmark for Adobe Encoder

Terasic is working closely with IBEX. The goal is to productize Adobe Premiere Pro Plugin on FLIK.

Current Performance:

The Adobe Premiere Pro plugin can accelerate different codecs in the FPGA. This IP gives over 3X performance improvement when encoding video with FPGA (FLIK) vs a 12 core Xeon CPU.

The End