

FLIK

Getting Started Guide



FPGA

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Chapter 1

Overview

This chapter provides an overview of the FLIK and installation guide.

1.1 General Description

With the rapidly-rising demand in today's AI and compute-intensive applications, Terasic's FLIK (FPGA Client Innovation Kit) is a compact, all-in-one, adaptable accelerator purpose-design to accelerate critical workloads such as data analysis, deep learning, and machine learning algorithms directly on laptops or everything portable! With a form factor slightly larger than a 2.5" external hard drive. It can be placed vertically or horizontally to blend into various size-demanding environment.

FLIK takes advantage of the powerful Intel Arria 10 FPGA to enable higher speed data processing. The kit is armed with 8GB DDR4-2133 on-board memory, providing around 4GB data transfer via PCIe Gen 3 interface between FPGA and laptops or host PC via Thunderbolt™ 3 port. Also, with a form factor slightly larger than a 2.5" external hard drive and closely packed in an aluminum body with advanced thermal solution, FLIK takes care of the heat dissipation dynamically and is adaptable to various size-demanding environment.

FLIK fully supports Intel Open VINO™ toolkit, Intel Acceleration Stack, and OpenCL in both Linux and Windows versions. Our clients can achieve highest computing performance, adaptability and lowest cost across broadest range of AI and deep learning workloads.

1.2 Package Content

Figure 1-1 shows the package content of the FLIK kit.



Figure 1-1 FLIK Kit Content

1.3 FLIK View

Figure 1-2 shows the front and rear views of the FLIK. There are five color LED in front panel. The five color LED indicate the status of FLIK. **Table 1-1** shows the LED indication meanings. There are a thunderbolt 3 port and a 12V DC input Jack on the rear of FLIK.



Figure 1-2 FLIK View

Table 1-1 Front Color LED Indication

Front Color LED	Description
Green	FLIK is power on but not connected to Host PC.
Dark Blue	FLIK is just connected to the Host PC
Light Blue and Dark Blue	FLIK is connected to the Host PC and show the power consumption status. More Light Blue means more power is consumed.
Red	FPGA power is shut down due to over temperature.
Orange	FPGA power is shut down due to power consumption exceeds expectation.
Gray	FPGA power is shut down due to FPGA power consumption exceeds expectation.
Yellow	FLIK is disconnected and will be auto shutdown in 60 seconds.

1.4 Block Diagram

Figure 1-3 shows the block diagram of the FLIK board.

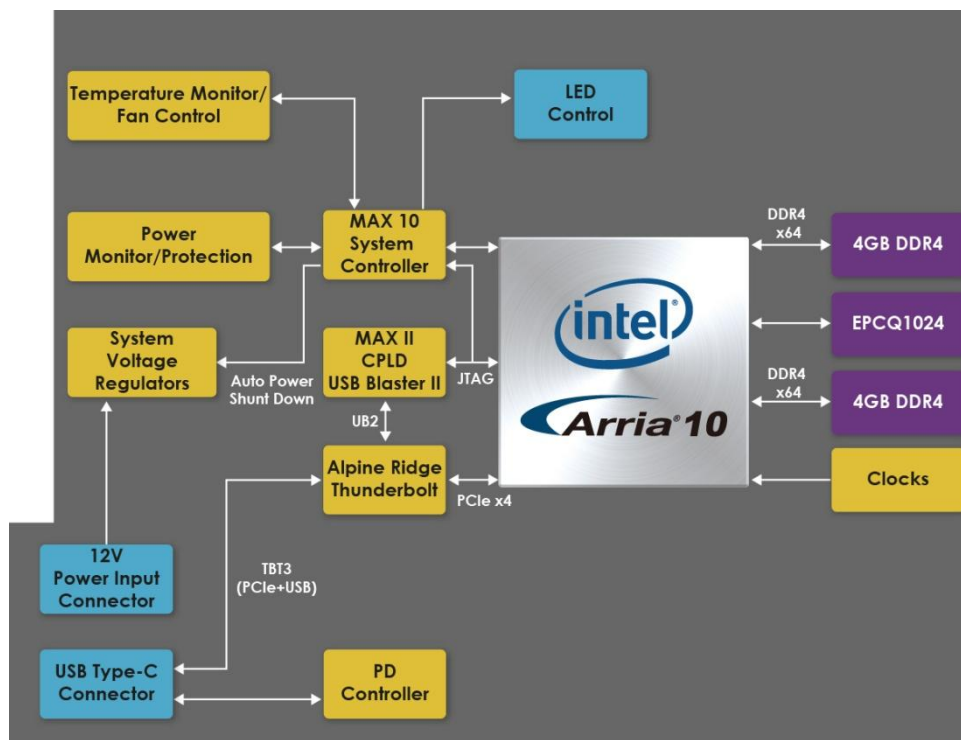


Figure 1-3 Block diagram of the FLIK

1.5 Key Features

The following hardware is implemented on the FLIK board:

■ FPGA

- Intel Arria ® 10 FPGA 10AX115N3F40E2SG

■ FPGA Configuration

- On-Board USB Blaster II via Thunderbolt 3 Port
- AS x4 configuration via QSPI Flash

■ Clock System

- 50MHz and 100MHz Oscillators
- Programmable clock generators Si5340

■ Memory

- Two Independent DDR4 banks, 4GB 1066MHz for each.
- 1024Mb QSPI Flash

■ Communication Ports

- Thunderbolt 3 Port x1
- PCIe Gen3x4 via Thunderbolt 3 Port
- USB Blaster II port via Thunderbolt 3 Port

■ System Monitor and Control

- FPGA Temperature Monitor
- Board Temperature Monitor
- Power Monitor
- Auto Fan Speed Control
- Auto Shutdown when temperature or power are abnormal.
- LED Indication

■ Power Source

- 12V DC Input

1.6 Software Package and Manual

The FLIK Kit includes three software packages, as shown in **Table 1-2**. The software packages are prepared for C/C++, OpenCL, and RTL developers. **Table 1-3** shows the documents provided by the FLIK Kit. The table also recommends manuals that developers should study.

Table 1-2 Software Packages

Software Package	Required Programming Skill for FPGA
OpenVINO BSP	C/C++
OpenCL BSP	OpenCL
RTL Example Designs	RTL Coding

Table 1-3 Software Packages

Manual\Developer	OpenVINO Developer	OpenCL Developer	RTL Developer
Quick Stat Guide	√	√	√
Getting Started Guide (Windows or Linux)	√	√	√
OpenVINO Development Guide	√		
OpenCL User Manual		√	
RTL Development Guide			√

1.7 Power On FLIK

There is no power SWITCH on FLIK. Plug in 12V DC to FLIK will directly power on the FLIK (See **Figure 1-4**). When FLIK is power on without connected to the Host PC, the Font Panel Color LED is Green as shown in **Figure 1-5**.



Figure 1-4 Plug the DC 12V power to the FLIK



Figure 1-5 RGB Status LED when Power up

1.8 Power Monitor Utility

The FLIK Kit includes a Power Monitor Software which can be used to monitor the power and temperature status of the FLIK, as shown in **Figure 1-6**. For more detailed information, please check [Chapter 4 : Power Monitor Setup](#).

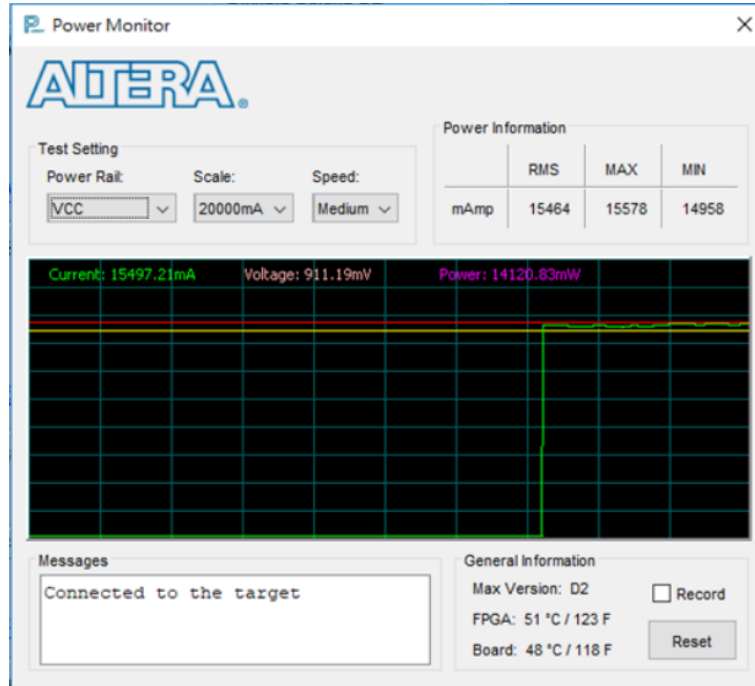


Figure 1-6 Power Monitor

1.9 Function Test Guide

To perform function test on FLIK, users need to setup thunderbolt 3 first. For detail, refer to Chapter 2 in this document. For OpenVINO developers, they need to install OpenVINO Software. For detail, refer to Chapter 3 in this document.

Chapter 2

Thunderbolt 3 Setup

Thunderbolt 3 is unique communication path between the Host PC and FLIK. As shown in **Figure 2-1**, the FLIK use thunderbolt3 port to connect the PCIe and USB Blaster II interface to the FPGA. For the OpenCL and OpenVINO applications with the Intel FPGA, the PCIe bus is the main interface for communicating and transferring data with the host PC. The thunderbolt3 port on the FLIK allows the user to build such connection for the FPGA and the host PC via a thunderbolt3 cable. In addition, the thunderbolt3 on the FLIK also provides an USB interface to connect to the USB Blaster II circuit on the board, providing a JTAG interface for the user to program the FPGA or configuration device through the host PC.

Therefore, a host PC equipped with thunderbolt 3 port is required to work with the FLIK. This chapter will show user how to setup thunderbolt 3 connection between the Host PC and the FLIK for the first time. The windows OS is present in this chapter. For Linux OS, please refer to the *Linux Getting start guide*.

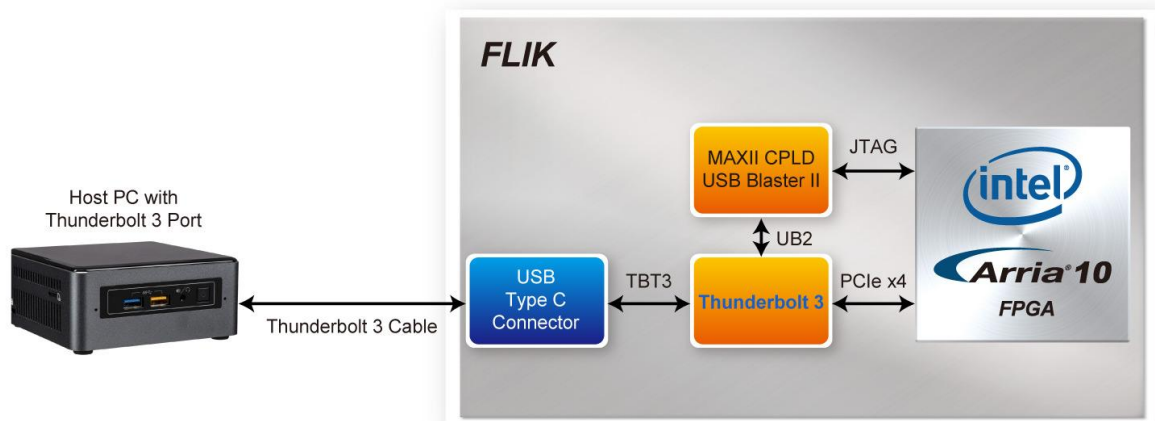


Figure 2-1 The Thunderbolt interface of the FLIK

2.1 Hardware Requirement

- A Host PC with Thunderbolt 3 Port is required to perform FLIK function Tests.
The PC should be:
 - Built-in Thunderbolt 3 Port or with Thunderbolt3 Card Installed.
 - Windows/Linux Installed
 - Thunderbolt 3 driver installed
- A FLIK kit
- A Thunderbolt 3 Cable as shown in **Figure 2-2**



Figure 2-2 Thunderbolt 3 Cable

2.2 Thunderbolt 3 Test

Below shows the procedure when the FLIK is first time to plug into the thunderbolt 3 port of the Host PC.

1. Make sure your Host PC had installed Thunderbolt 3 Driver.
2. Plug 12V DC to FLIK to power on the FLIK.
3. Connect FLIK and host PC by a Thunderbolt 3 cable.



Figure 2-3 Plug the Thunderbolt 3 cable to the FLIK

4. When the host pc connects to the FLIK with Thunderbolt 3 cable for the first time. Windows should detect a Thunderbolt Device and you will see a “New Thunderbolt device has been connected” message appear in the bottom right corner of your screen as shown in **Figure 2-4**. Click the message to approve the device.

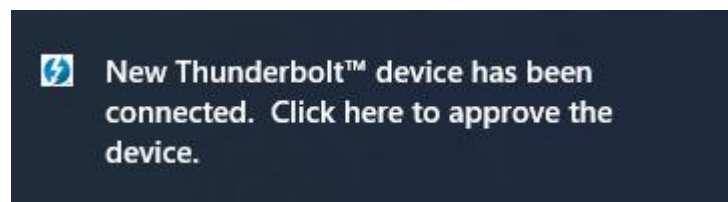


Figure 2-4 New Thunderbolt devices have been attached" message

Note, if this message does not appear, user can reconnect the thunderbolt 3 cable between the FLIK and Host PC or power off and on the FLIK. If the message still doesn't appear, please confirm that driver of the Thunderbolt 3 has been properly installed on the host PC.

5. A Thunderbolt Dialog window will appear as shown in **Figure 2-5** or **Figure 2-6**.

Select "Always Connected" and click OK button.

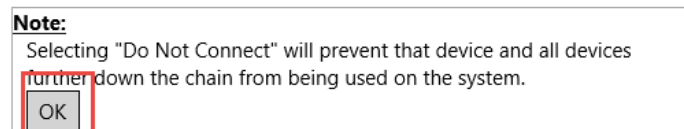
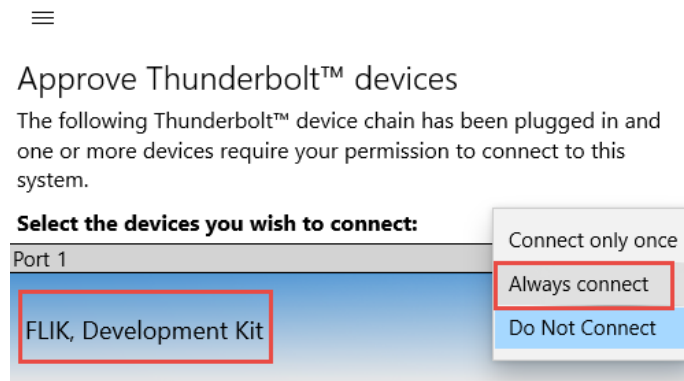


Figure 2-5 Approve Thunderbolt device window

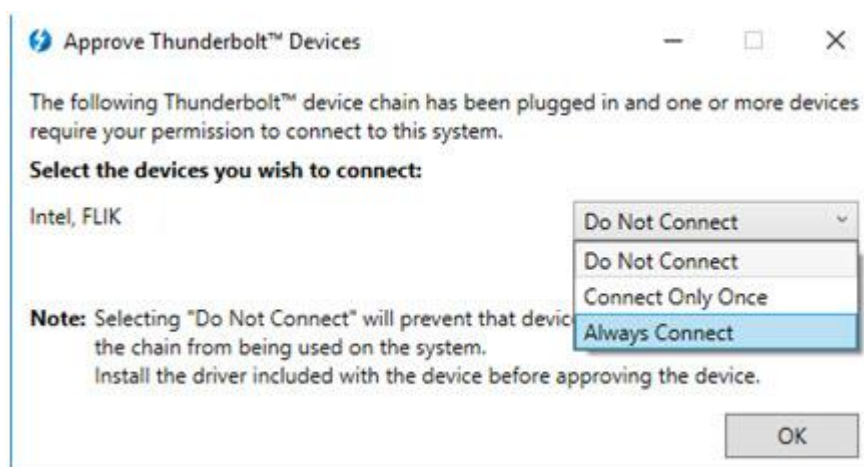


Figure 2-6 Approve Thunderbolt device window

6. Open the "Device Manager" in the Windows and you will see the "PCI Device"

and "Unknown device" on the "Other devices" item (See **Figure 2-7**). It shows that the PCIe device and USB Blaster II circuit on the FLIK are correctly detected by the host PC. The following chapter will show how to install the drivers for these two devices.

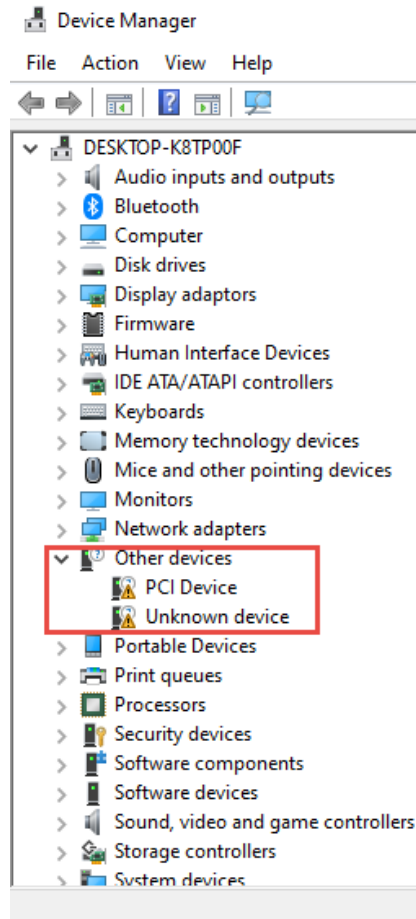


Figure 2-7 Host PC detects the PCIe and USB Blaster II function in the FLIK

Chapter 3

OpenVINO Setup for Windows

OpenVINO is a high-level development kit. Users can accelerate the computing by high-level C/C++ language rather than low-level RTL coding. This chapter introduces how to install OpenVINO run-time environment and how to performance OpenCL demo on **Windows 10**. Before setup the OpenVINO, please make sure the thunderbolt3 driver is installed on the Host PC.

3.1 OpenVINO Installer/Demo Package

First, users need to download the OpenVINO BSP for windows "FLIK_OpenVINO2019R1_windows.zip" from the link: <http://flik.terasic.com/cd>.

OpenVINO 2019 R1





Title	Version	Size(KB)	Date Added	Download
OpenVINO BSP for Windows	1.0 		2019-11-27	
OpenVINO BSP for Linux	1.0 		2019-11-27	

Figure 3-1 OpenVINO BSP for Windows

Then, uncompress the.zip file into your Host PC. There are two folders in the compressed file.

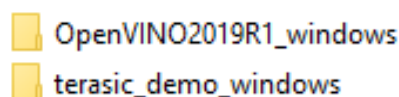


Figure 3-2 Contents of the demo package

The "OpenVINO2019R1_windows" folder has the relevant file for installing OpenVINO tool kit in the window. The "terasic_demo_windows" folder contains demo

examples for using OpenVINO with the FLIK.

3.2 Install FLIK OpenVINO Runtime Environment

1. Install required Microsoft Visual Studio runtime library : [Visual Studio 2017 Redistributable Package](#)

Visual Studio 2015, 2017 and 2019

Download the [Microsoft Visual C++ Redistributable for Visual Studio 2015, 2017 and 2019](#). The following updates are the latest supported Visual C++ redistributable packages for Visual Studio 2015, 2017 and 2019. Included is a baseline version of the Universal C Runtime see [MSDN](#) for details.

- x86: [vc_redist.x86.exe](#)
- x64: [vc_redist.x64.exe](#)
- ARM64: [vc_redist.arm64.exe](#)

Figure 3-3 Web site of the Visual Studio 2017 Redistributable Package

2. Open the folder “**OpenVINO2019R1_windows**” you just extracted (section 3.1). Before install the drive of the FLIK and setup associated environment, please open and read the “**Intel OBL Commercial Use License.pdf**” for Software License Agreement.
3. Go to the path “**/OpenVINO2019R1_windows/FLIK-Windows-Install_19.2**” and execute “**1-SetBootOptions.bat**” as an Administration to enable test-signed code and device driver signing of the windows, as shown in **Figure 3-4** and **Figure 3-5**.

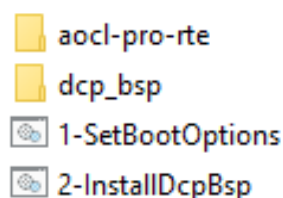


Figure 3-4 The FLIK-Windows-Install folder

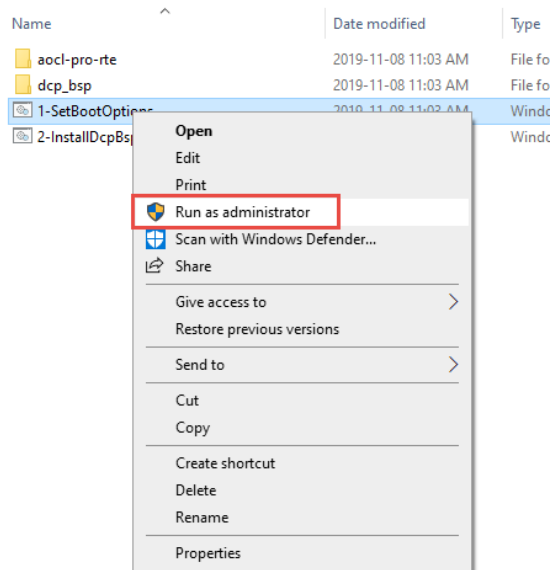


Figure 3-5 Run 1-SetBootOptions.bat as administrator

- When the batch file is executed, please **reboot the system** to enable the settings.

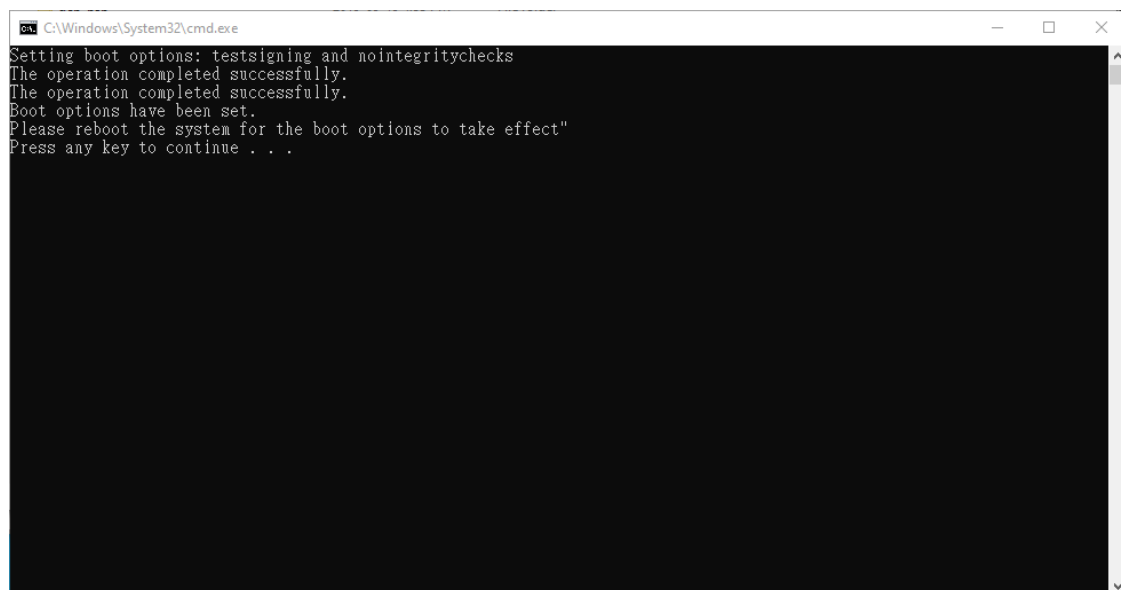


Figure 3-6 1-SetBootOptions.bat is executed

- After Reboot Windows, open **“Command Prompt”** and run as **“administrator”**.

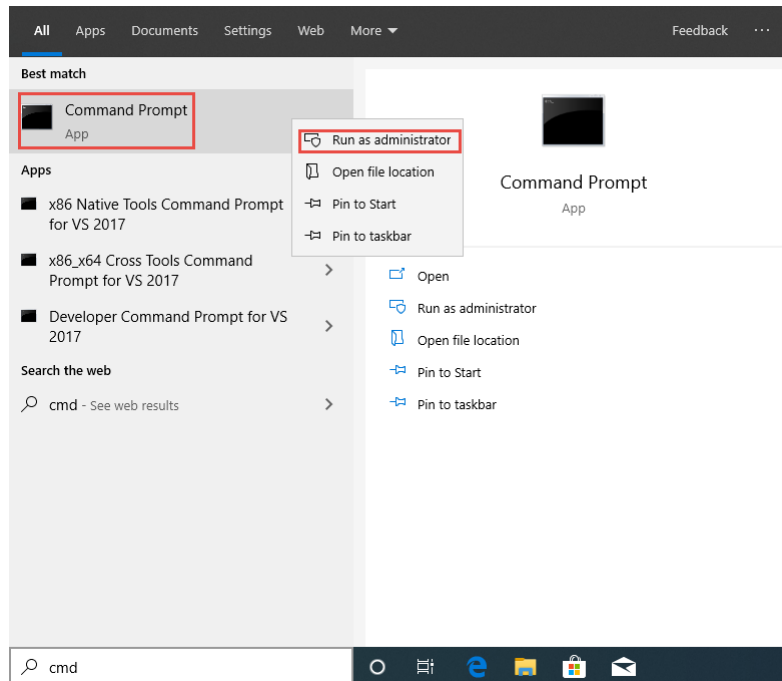


Figure 3-7 Open Command Prompt

6. Go to the folder “FLIK-Windows-Install_19.2” and execute “**2-InstallDcpBsp.bat**”.
It will start to install Intel Runtime Environment for OpenCL.

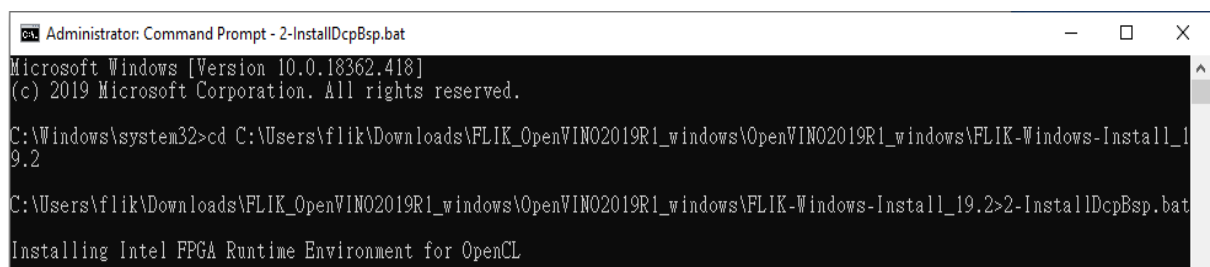


Figure 3-8 Run “2-InstallDcpBsp.bat” as administrator

7. Press “y” when ask to install FLIK device driver.

```
Administrator: Command Prompt - 2-InstallDcpBsp.bat
C:\Users\flik\Downloads\FLIK_OpenVINO2019R1_windows\OpenVINO2019R1_windows\FLIK-Windows-Install_19.2\.\dcp_bsp\windows64
\driver\opaaccel.sys
C:\Users\flik\Downloads\FLIK_OpenVINO2019R1_windows\OpenVINO2019R1_windows\FLIK-Windows-Install_19.2\.\dcp_bsp\windows64
\driver\opaedevic.cat
C:\Users\flik\Downloads\FLIK_OpenVINO2019R1_windows\OpenVINO2019R1_windows\FLIK-Windows-Install_19.2\.\dcp_bsp\windows64
\driver\opaedevic.inf
C:\Users\flik\Downloads\FLIK_OpenVINO2019R1_windows\OpenVINO2019R1_windows\FLIK-Windows-Install_19.2\.\dcp_bsp\windows64
\driver\opaedevic.sys
C:\Users\flik\Downloads\FLIK_OpenVINO2019R1_windows\OpenVINO2019R1_windows\FLIK-Windows-Install_19.2\.\dcp_bsp\windows64
\driver\uninstall.bat
C:\Users\flik\Downloads\FLIK_OpenVINO2019R1_windows\OpenVINO2019R1_windows\FLIK-Windows-Install_19.2\.\dcp_bsp\windows64
\lib\intel_opae_mmd.lib
C:\Users\flik\Downloads\FLIK_OpenVINO2019R1_windows\OpenVINO2019R1_windows\FLIK-Windows-Install_19.2\.\dcp_bsp\windows64
\libexec\diagnose.exe
C:\Users\flik\Downloads\FLIK_OpenVINO2019R1_windows\OpenVINO2019R1_windows\FLIK-Windows-Install_19.2\.\dcp_bsp\windows64
\libexec\flash.bat
C:\Users\flik\Downloads\FLIK_OpenVINO2019R1_windows\OpenVINO2019R1_windows\FLIK-Windows-Install_19.2\.\dcp_bsp\windows64
\libexec\flash.pl
C:\Users\flik\Downloads\FLIK_OpenVINO2019R1_windows\OpenVINO2019R1_windows\FLIK-Windows-Install_19.2\.\dcp_bsp\windows64
\libexec\FpgaLib.dll
C:\Users\flik\Downloads\FLIK_OpenVINO2019R1_windows\OpenVINO2019R1_windows\FLIK-Windows-Install_19.2\.\dcp_bsp\windows64
\libexec\install.bat
C:\Users\flik\Downloads\FLIK_OpenVINO2019R1_windows\OpenVINO2019R1_windows\FLIK-Windows-Install_19.2\.\dcp_bsp\windows64
\libexec\program.exe
C:\Users\flik\Downloads\FLIK_OpenVINO2019R1_windows\OpenVINO2019R1_windows\FLIK-Windows-Install_19.2\.\dcp_bsp\windows64
\libexec\uninstall.bat
28 File(s) copied
Installing FLIK device drivers
Do you want to setup PCD with for all users (requiring administrative privileges) [y/n]?
```

Figure 3-9 Install FLIK device driver

8. Then, a Device Driver Installation Wizard window will appear. Click “**Next**” to install the driver.

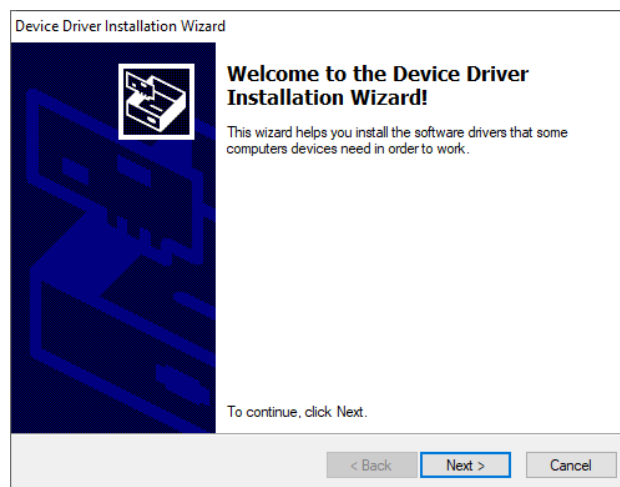


Figure 3-10 Device Driver Installation Wizard

When a Windows Security dialog appears, please select “**Install this driver software anyway**” option (This may appear twice).

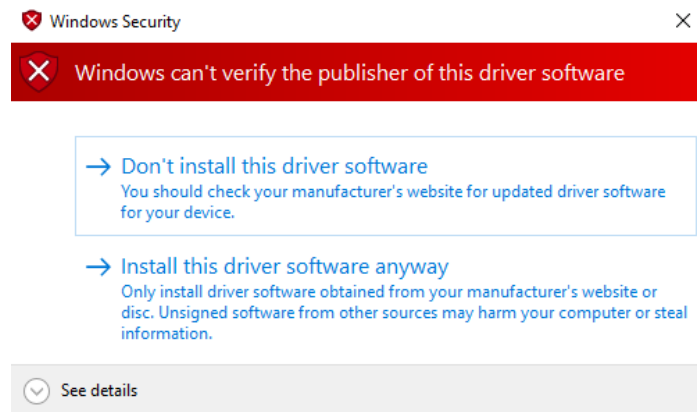


Figure 3-11 Windows Security Dialog

After finish install the device driver, press any key to finish the whole setups.

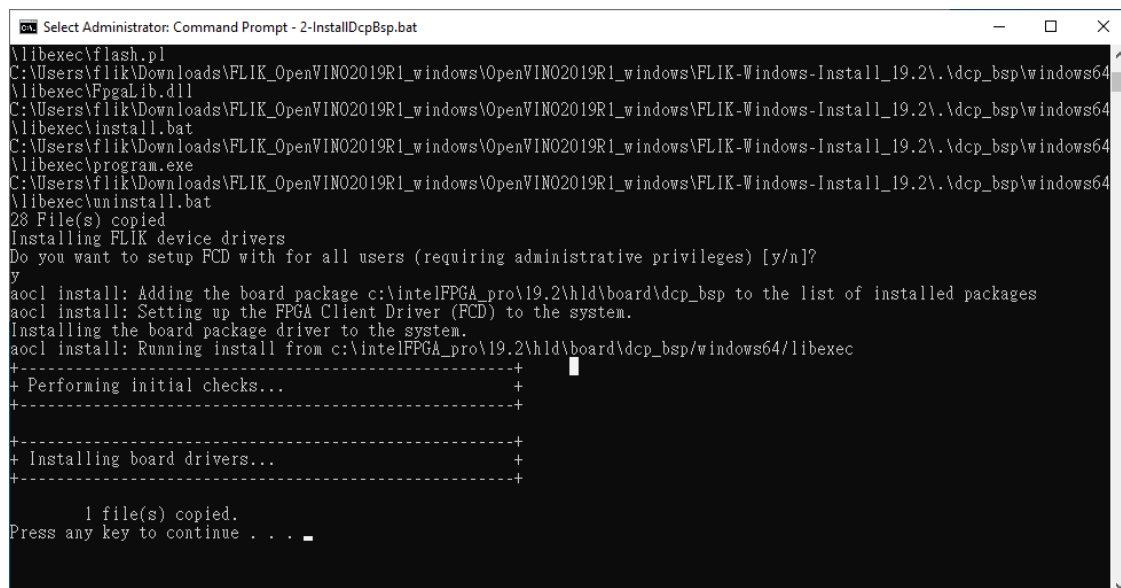


Figure 3-12 Windows Security Dialog

9. Make sure the "C:\intelFPGA_pro\19.2\aclrte-windows64\board\dcp_bsp" which is generated by the installer is existed.
10. Plug 12V DC power to FLIK to power on the FLIK.
11. Connect FLIK to your Host PC via Thunderbolt 3 cable. Make sure you have set up the Thunderbolt 3 port for FLIK and your host PC as described in the Chapter 2
12. Open "**Device Manager**" on your host PC and expand the "**Accelerators**", "**FPGA Opaeaccel Device**" and "**FPGA PF Device**" should be list. That shows the driver of the PCIe hardware in the FLIK has been installed on your Host PC.

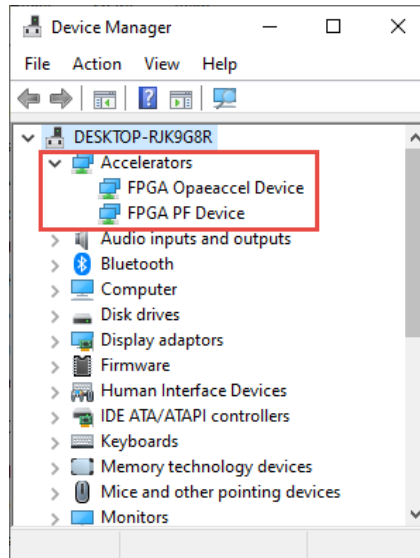


Figure 3-13 System device in Device Manager

13. Open **Command Prompt(CMD)** in the Windows.

14. Go to the folder “C:\intelFPGA_pro\19.2\aclrte-windows64\board\dcg_bsp\bringup”

Note : If the path: "C:\IntelFPGA_pro\19.2\aclrte-windows64\board\ dcg_bsp\" does not exist on the user's host PC, please copy the path from the OpenVINO BSP for windows (path: \FLIK_OpenVINO2019R1_windows\OpenVINO2019R1_windows\FLIK-Windows-Install_19.2 \dcg_bsp) to the specified directory.

15. Execute “InitRuntimeEnv.bat”

```

Microsoft Windows [Version 10.0.18362.418]
(c) 2019 Microsoft Corporation. All rights reserved.

C:\Users\flik>cd C:\IntelFPGA_pro\19.2\aclrte-windows64\board\dcg_bsp\bringup
C:\intelFPGA_pro\19.2\aclrte-windows64\board\dcg_bsp\bringup>InitRuntimeEnv.bat
INTELFPGAOCLESDKROOT is set to "C:\intelFPGA_pro\19.2\aclrte-windows64". Using that.
aoc was not found, but aocl was found. Assuming only RTE is installed.
AOCL_BOARD_PACKAGE_ROOT is set to C:\intelFPGA_pro\19.2\aclrte-windows64\board\dcg_bsp. Using that.

VisualStudio's link.exe is not on the path. Guessing its location.
Cannot find VisualStudio installation by looking at the environment.
If VisualStudio is installed, use VisualStudio Command Prompt to set all
required environment variables.

Adding C:\intelFPGA_pro\19.2\aclrte-windows64\bin to PATH
Adding C:\intelFPGA_pro\19.2\aclrte-windows64\windows64\bin to PATH
Adding C:\intelFPGA_pro\19.2\aclrte-windows64\host\windows64\bin to PATH
Adding C:\intelFPGA_pro\19.2\aclrte-windows64\board\dcg_bsp\windows64\bin to PATH
C:\intelFPGA_pro\19.2\aclrte-windows64\board\dcg_bsp\bringup>_

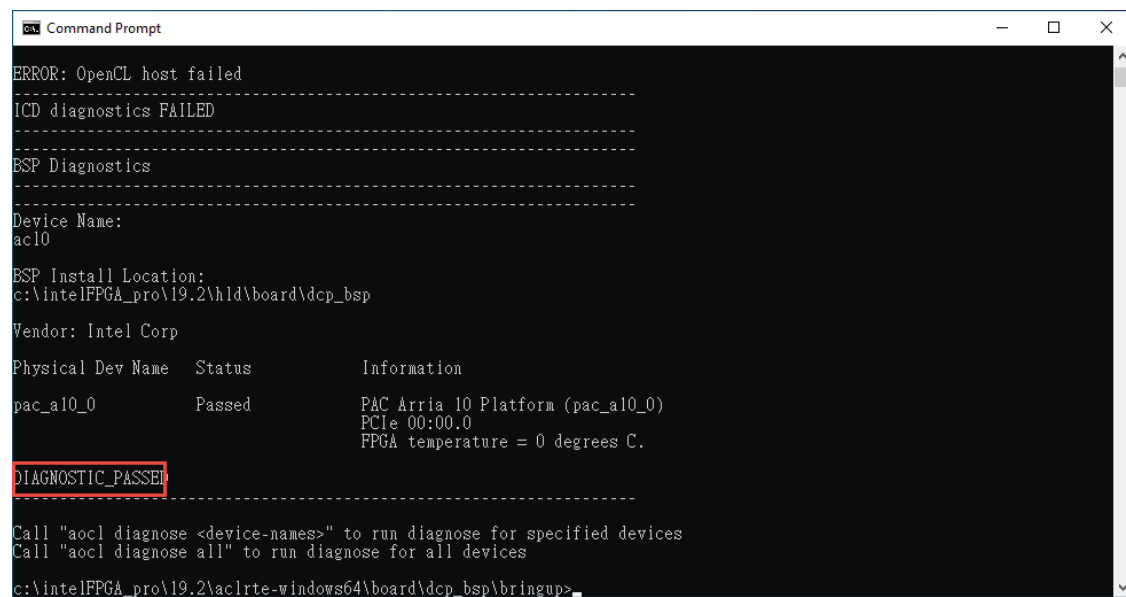
```

Figure 3-14 run InitRuntimeEnv.bat

16. Run the simple diagnostic utility: **"aocl diagnose"**.

The aocl diagnose command is useful to query the available PCIe device in a system. It will report device information and identifies issues.

There is a diagnose report on the command shell as shown in below. IF the command returns "DIAGNOSTIC_PASSED", it shows that the hardware configuration is successful.



```
Command Prompt
ERROR: OpenCL host failed
-----
ICD diagnostics FAILED
-----
BSP Diagnostics
-----
Device Name:
acl0
BSP Install Location:
c:\intelFPGA_pro\19.2\hld\board\dcu_bsp
Vendor: Intel Corp
Physical Dev Name   Status      Information
pac_a10_0           Passed      PAC Arria 10 Platform (pac_a10_0)
                                   PCIe 00:00.0
                                   FPGA temperature = 0 degrees C.
DIAGNOSTIC_PASSED
-----
Call "aocl diagnose <device-names>" to run diagnose for specified devices
Call "aocl diagnose all" to run diagnose for all devices
c:\intelFPGA_pro\19.2\aclrte-windows64\board\dcu_bsp\bringup>
```

Figure 3-15 run InitRuntimeEnv.bat

17. The user can also do the test for the individual device connected to the host PC.

The command is: `aocl diagnose <device_name>`. If the host pc is connected to only one device, <device_name> is usually named "acl0". So after entering the `aocl diagnose acl0` command, the memory transfer test will start and the test result will be returned.

Please execute **"aocl diagnose acl0"**

There is a diagnose report on the command shell as shown in **Figure 3-16**. If the command returns **"DIAGNOSTIC_PASSED"**, it shows that the hardware configuration is successful. User can go to section 3.4 for further setting steps.

```

Command Prompt
2097152 1459.38 1604.43 904.10 1445.22
4194304 1627.23 1781.63 1211.56 1616.27
8388608 1771.02 1928.06 1506.85 1764.32
16777216 1913.53 1960.76 1664.54 1910.09
33554432 2030.06 2070.89 1941.52 2028.06
67108864 2025.86 2043.30 1997.04 2024.47
134217728 2113.97 2189.73 2043.28 2113.51
268435456 2128.47 2128.47 2128.47 2128.47

Reading 262144 KBs with block size (in bytes) below:

Block Size Avg      Max      Min      End-End (MB/s)
524288 1416.43 1567.85 750.05 1356.04
1048576 1251.97 1530.77 658.32 1227.87
2097152 1426.71 1605.17 1261.60 1412.84
4194304 1463.88 1657.17 1373.52 1455.65
8388608 1977.14 2076.85 1358.48 1970.07
16777216 2289.12 2354.80 1827.50 2284.78
33554432 2577.27 2601.72 2516.08 2575.64
67108864 2546.61 2693.05 2418.17 2545.31
134217728 2718.57 2737.84 2699.57 2718.10
268435456 2617.36 2617.36 2617.36 2617.36

Write top speed = 2189.73 MB/s
Read top speed = 2737.84 MB/s
Throughput = 2463.79 MB/s

DIAGNOSTIC_PASSED

c:\intel\FPGA_pro\19.2\aclrte-windows64\board\dcu_bsp\bringup>

```

Figure 3-16 aocl diagnose passed

3.3 Install FLIK OpenVINO Toolkit

Below is the procedure to install OpenVINO Toolkit and perform OpenVINO face detection demo.

1. Go to folder “OpenVINO2019R1_windows”
2. Execute “python-3.6.5-amd64.exe”. Remember to check “Add Python 3.6 to PATH” as shown in Figure 3-17.

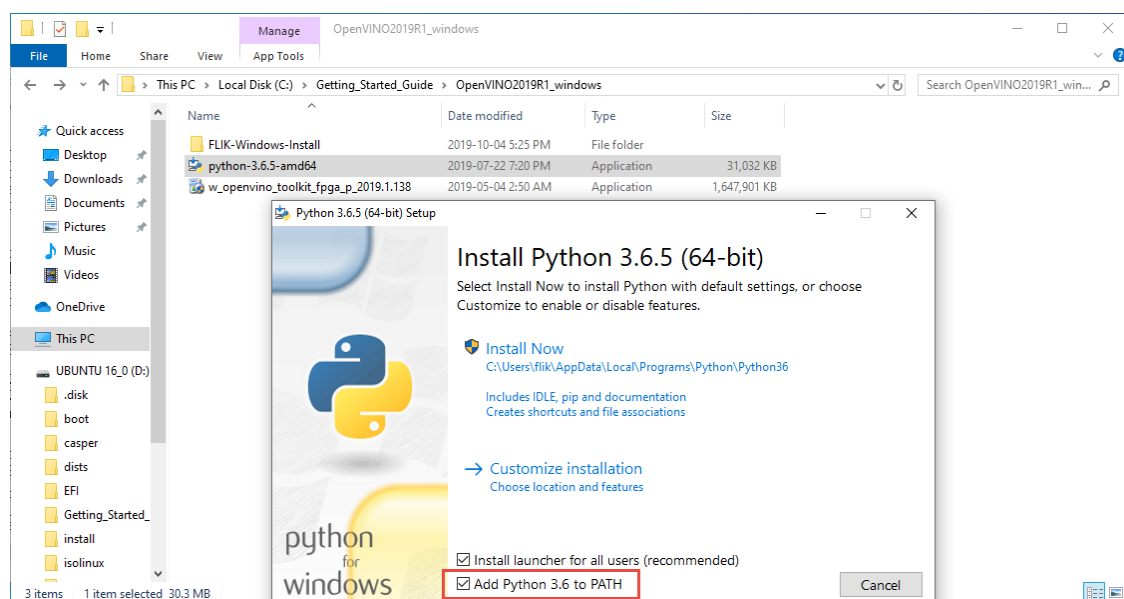


Figure 3-17 Install the Python 3.6

3. Go to folder “**OpenVINO2019R1_windows**”
4. Execute “**w_openvino_toolkit_fpga_p_2019.1.138.exe**” to install Intel Distribution of OpenVINO toolkit for Windows.

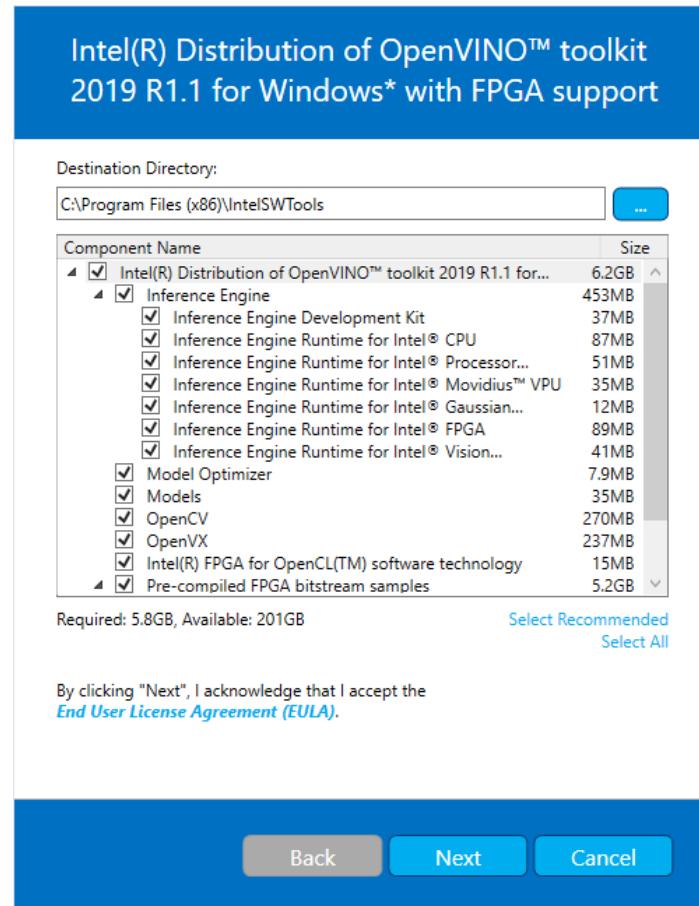
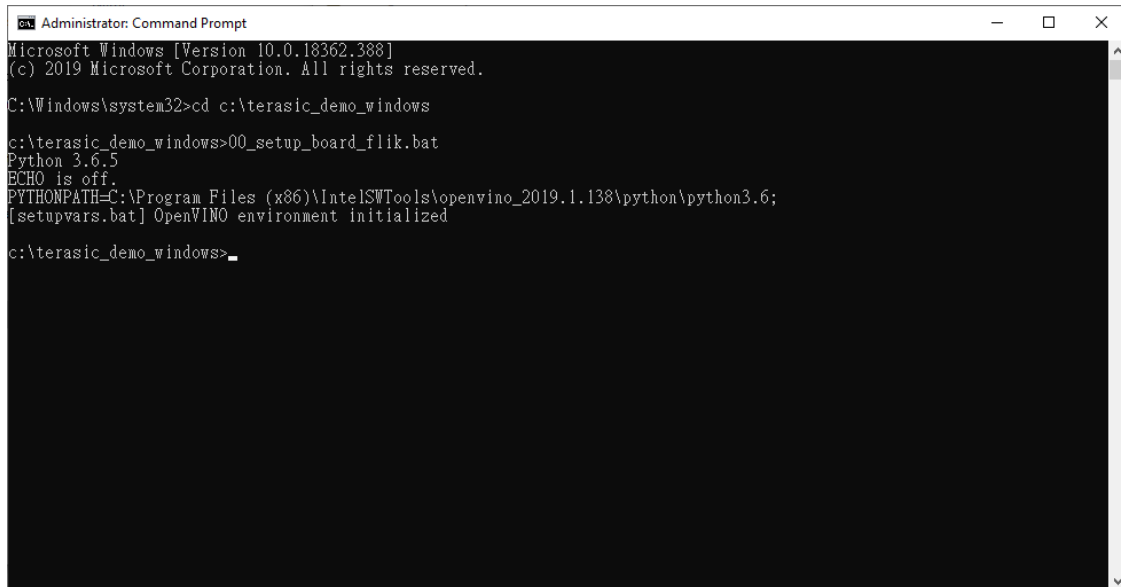


Figure 3-18 Install the OpenVINO toolkit

5. Go to the OpenVINO Demo Package folder “**terasic_demo_windows**” in your host PC (See section 3.1).
6. Execute “**00_setup_board_flik.bat**” for setting the Intel FPGA RTE for OpenCL Pro edition user environment variables.



```
Administrator: Command Prompt
Microsoft Windows [Version 10.0.18362.388]
(c) 2019 Microsoft Corporation. All rights reserved.

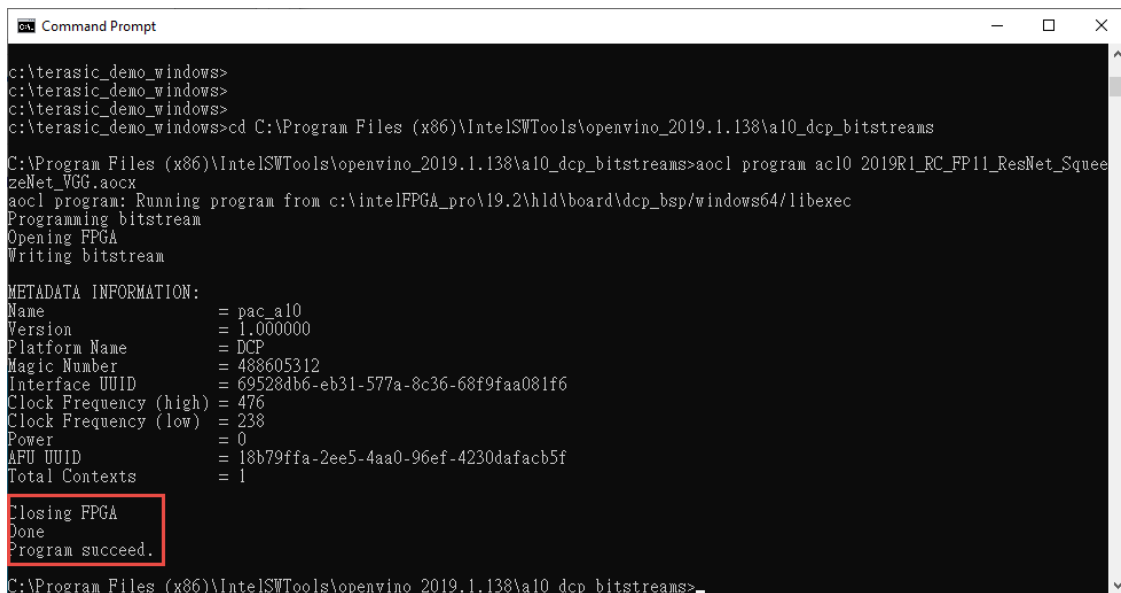
C:\Windows\system32>cd c:\terasic_demo_windows

c:\terasic_demo_windows>00_setup_board_flik.bat
Python 3.6.5
ECHO is off.
PYTHONPATH=C:\Program Files (x86)\IntelSWTools\openvino_2019.1.138\python\python3.6;
[setupvars.bat] OpenVINO environment initialized

c:\terasic_demo_windows>
```

Figure 3-19 Execute "00_setup_board_flik.bat"

7. Go to folder :
"C:\Program Files (x86)\IntelSWTools\openvino_2019.1.138\ai0_dcp_bitstreams"
8. Execute
"aocl program acl0 2019R1_RC_FP11_ResNet_SqueezeNet_VGG.aocx" to
program the demo bitstream file into the FPGA. Check the command returns
"Program succeed" for download finish.



```
Command Prompt

c:\terasic_demo_windows>
c:\terasic_demo_windows>
c:\terasic_demo_windows>
c:\terasic_demo_windows>cd C:\Program Files (x86)\IntelSWTools\openvino_2019.1.138\ai0_dcp_bitstreams

C:\Program Files (x86)\IntelSWTools\openvino_2019.1.138\ai0_dcp_bitstreams>aocl program acl0 2019R1_RC_FP11_ResNet_Squee
zeNet_VGG.aocx
aocl program: Running program from c:\intelFPGA_pro\19.2\hld\board\dcp_bsp\windows64\libexec
Programming bitstream
Opening FPGA
Writing bitstream

METADATA INFORMATION:
Name                = pac_a10
Version             = 1.000000
Platform Name       = DCP
Magic Number        = 488605312
Interface UUID      = 69528db6-eb31-577a-8c36-68f9faa081f6
Clock Frequency (high) = 476
Clock Frequency (low) = 238
Power               = 0
AFU UUID            = 18b79ffa-2ee5-4aa0-96ef-4230dafac5f
Total Contexts      = 1

Closing FPGA
Done
Program succeed.

C:\Program Files (x86)\IntelSWTools\openvino_2019.1.138\ai0_dcp_bitstreams>
```

Figure 3-20 Program the demo bitstream file into the FLIK

9. Return to folder "terasic_demo_windows"

10. Execute “04_face_detection.bat fpga video” to run the face detection demo.

```
Administrator: Command Prompt - 04_face_detection.bat fpga video
c:\terasic_demo_windows>
c:\terasic_demo_windows>
c:\terasic_demo_windows>
c:\terasic_demo_windows>
c:\terasic_demo_windows>
c:\terasic_demo_windows>
c:\terasic_demo_windows>04_face_detection.bat fpga video
target_device= HETERO:FPGA,CPU
target_precision="FP16"
target_image_path="c:\terasic_demo_windows\pic_video\people.mp4"
Get allparam ok
InferenceEngine:
    API version ..... 1.6
    Build ..... 23780
[ INFO ] Parsing input parameters
[ INFO ] Reading input
[ INFO ] Loading plugin HETERO:FPGA,CPU

    API version ..... 1.6
    Build ..... heteroPlugin
    Description ..... heteroPlugin
[ INFO ] Loading network files for Face Detection
[ INFO ] Batch size is set to 1
[ INFO ] Checking Face Detection network inputs
[ INFO ] Checking Face Detection network outputs
[ INFO ] Loading Face Detection model to the HETERO:FPGA,CPU plugin
Event (Type = 0x1, Handle = 0x0000000000000858, Flags = 0x0) successfully registered.
Event (Type = 0x1, Handle = 0x000000000000085C, Flags = 0x0) successfully registered.
```

Figure 3-21 Execute face_detection demo

11. You will see the face detection as shown in Figure 3-22.

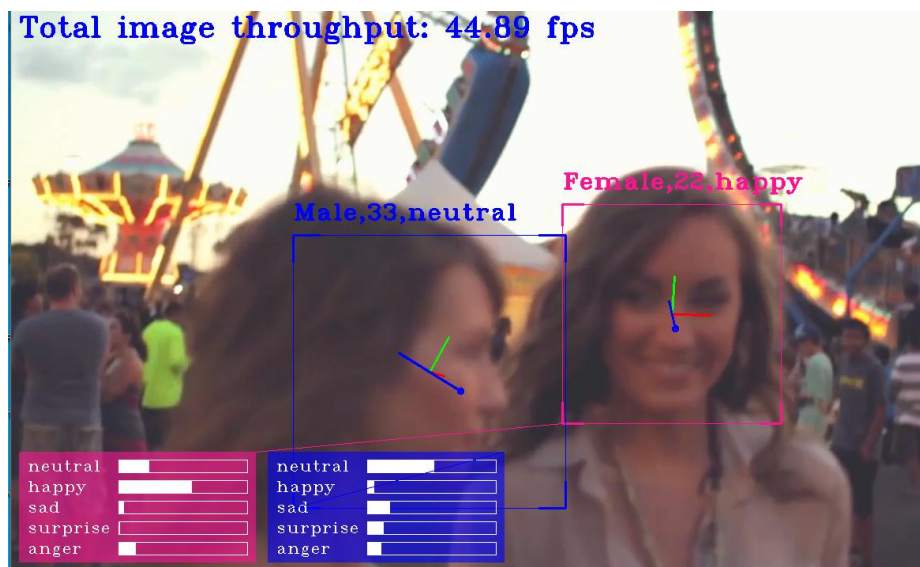


Figure 3-22 face detection demo

Chapter 4

Power Monitor Setup

Power Monitor is a GUI software utility which is designed to monitor the power and temperature status of the FLIK. It communicates with the FLIK via the USB Blaster II connection of the FLIK. The USB Blaster II connection is established base on the Thunderbolt 3 connection. Users can skip this chapter if they are not interested with the Power Monitor.

4.1 Software Requirements

■ **Quartus Programmer**

To use the power monitor, user first needs to download and install the Quartus programmer software. This software can set the environment settings for the host pc and install the USB Blaster II driver at the same time.

Here is the procedure to install the Quartus Programmer and setup the USB Blaster II:

1. The Quartus Prime Programmer is available on <http://fpgasoftware.intel.com/> as shown in **Figure 4-1**.

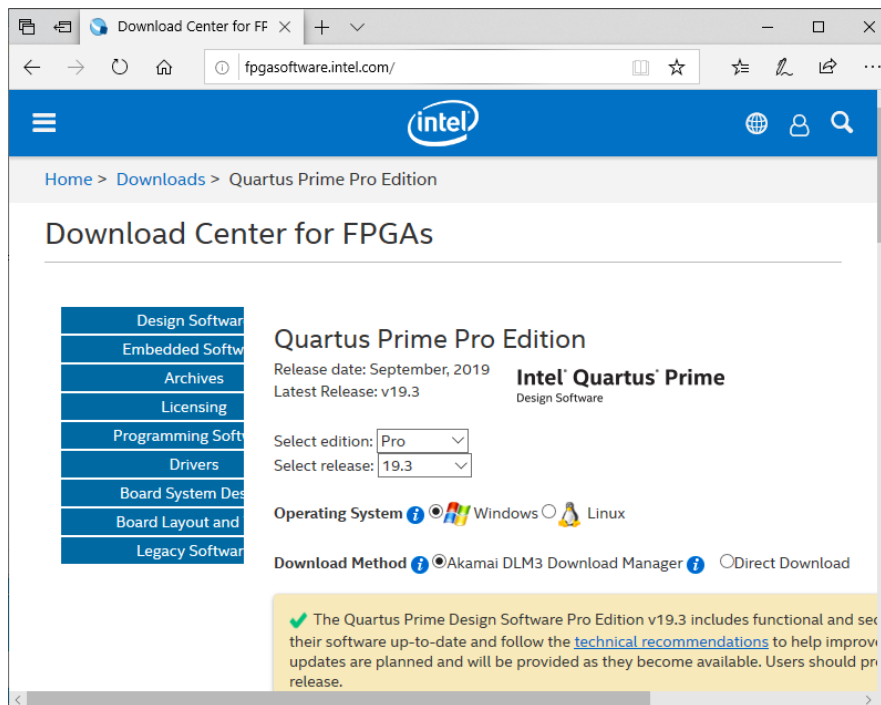


Figure 4-1 Download Center for FPGAs

2. As shown in **Figure 4-2**, set the “Select edition” to **Standard** and set “Select release” to **18.1**. (In order to properly execute the power monitor, please install 18.1 standard version)

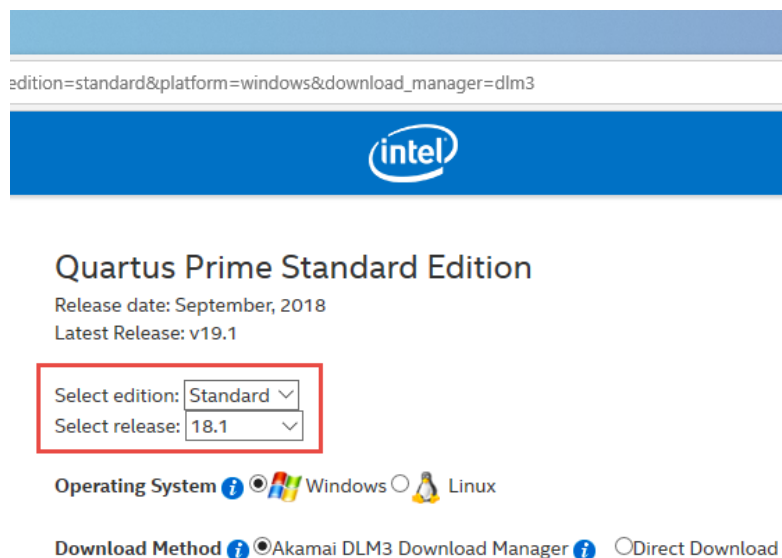


Figure 4-2 Select Quartus edition and release

3. In the same page, select the “Additional Software” Tab, check “Quartus Prime

Programmer and Tools” and click the “Download Selected Files”

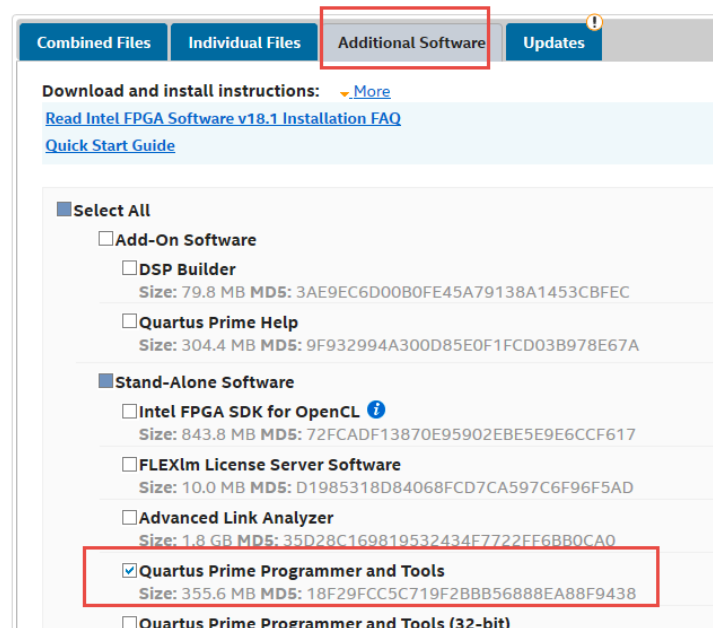


Figure 4-3 Select Stand-Alone software

4. Follow the instruction to install the Quartus programmer.

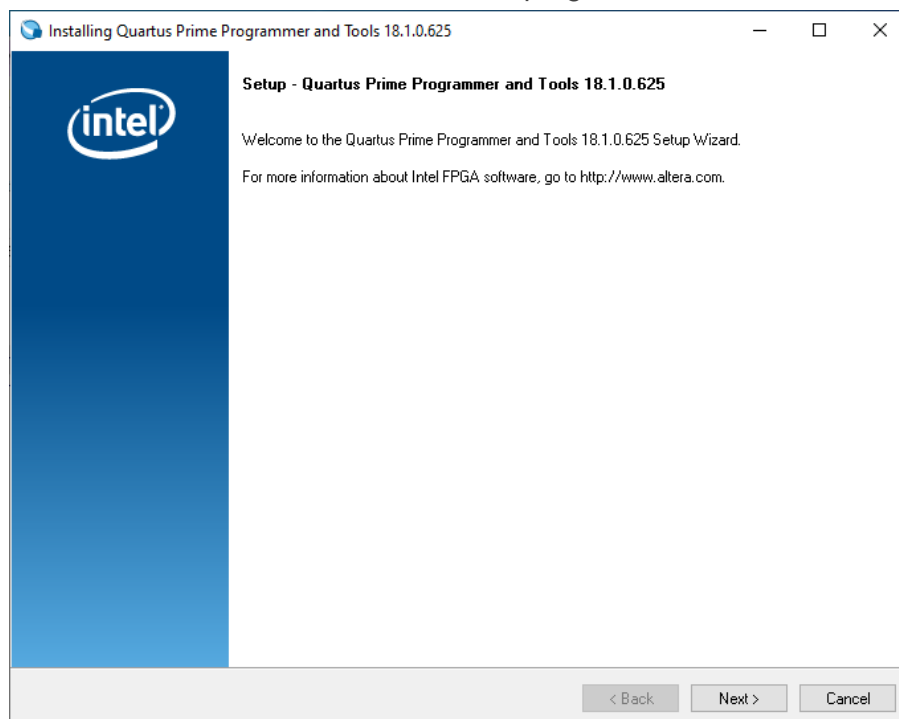


Figure 4-4 Install Quartus Programmer

5. In the last step of the installation, please check “Launch USB Blaster II driver

installation” to install USB Blaster II.

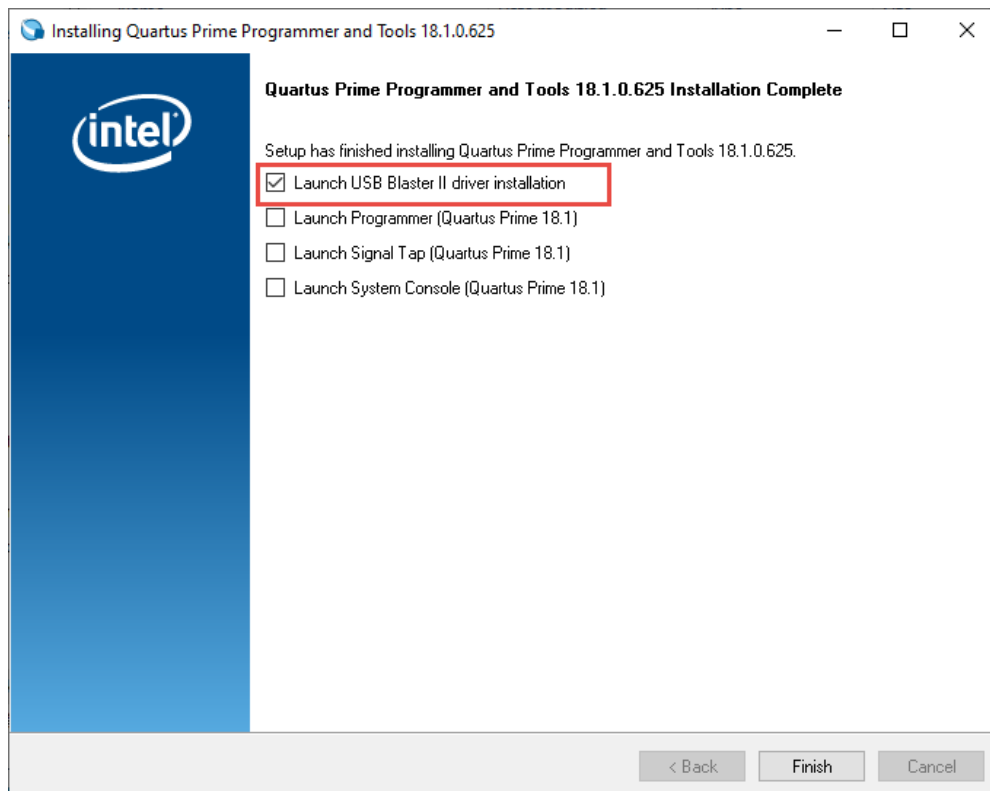


Figure 4-5 Select Launch USB Blaster II driver installation

6. See **Figure 4-6** ,follow the instructions to install the USB Blaster II driver on your host PC

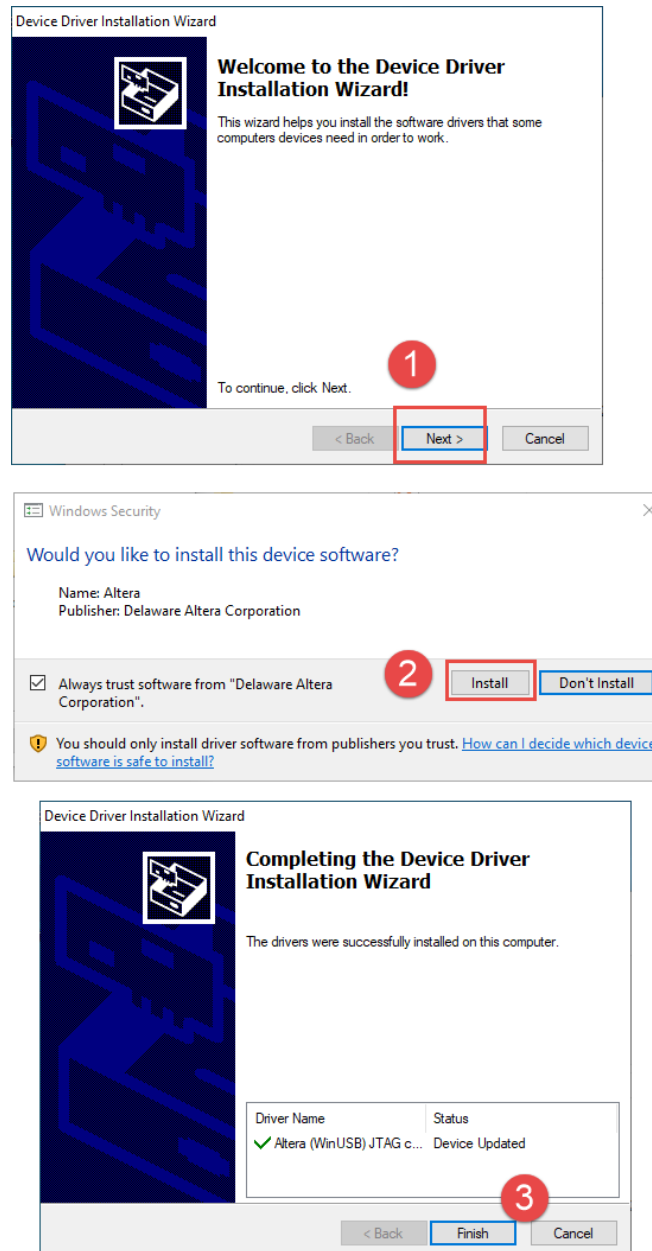


Figure 4-6 Install USB Blaster II driver

7. Plug the 12V DC to FLIK to power on the FLIK.
8. Connect FLIK to PC Thunderbolt 3 port by a Thunderbolt 3 cable.
9. Open the “Device Manager”, you should see a “**JTAG cables**” device and it contains the Altera USB-Blaster II hardware device. That means the USB Blaster II driver is install correctly on your host PC.

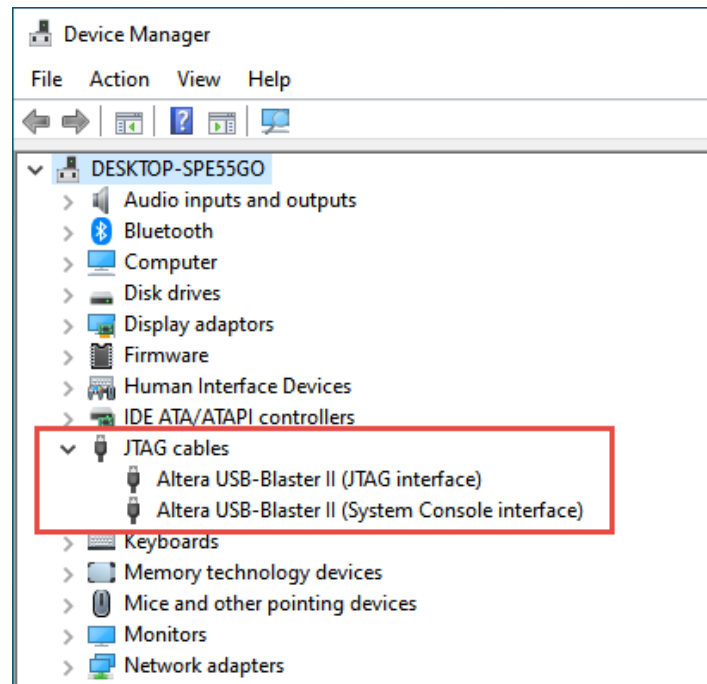


Figure 4-7 Verify USB Blaster II device

■ Microsoft Visual C++ 2010 Redistributable Package for Windows

In addition to the Quartus Programmer, since Power Monitor software is a 32-bit software, users also need to download and install the Microsoft Visual C++ 2010 Redistributable Package for Windows x86 version. It can be downloaded from the link: <https://www.microsoft.com/en-us/download/details.aspx?id=5555>

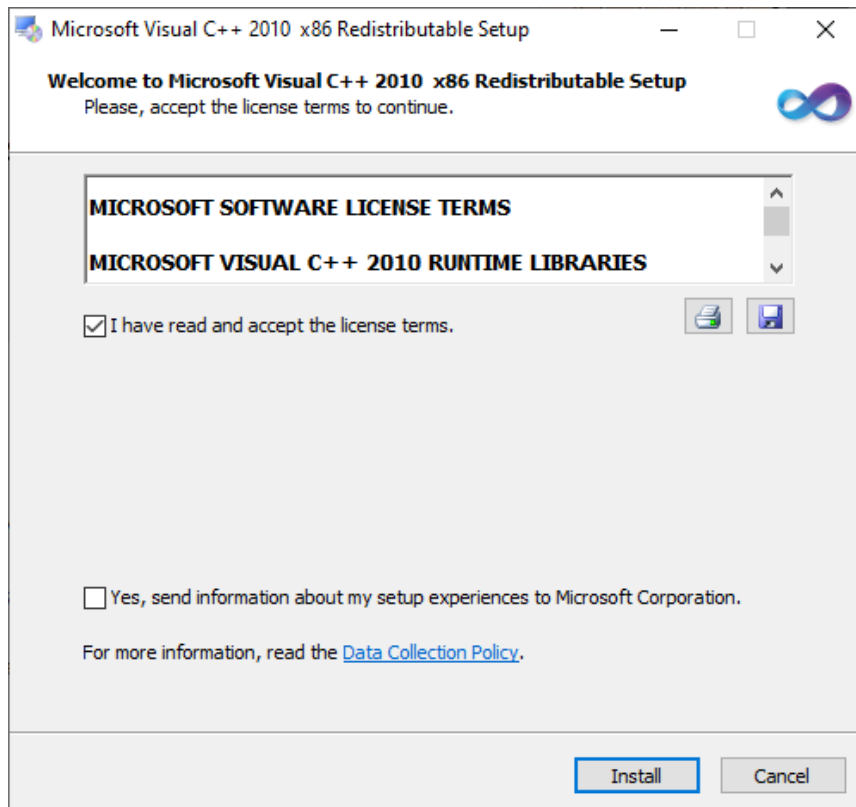


Figure 4-8 Install the Microsoft Visual C++ 2010 Redistributable Package

4.2 Power Monitor Utility

The FLIK Kit Includes a Power Monitor Software Utility which can be used monitor the FLIK Power Status and Temperature information. The software “*flik_power_monitor.zip*” is available from the link: <http://flik.terasic.com/cd>.

Tools

Title	Version	Size(KB)	Date Added	Download
FLIK Power Monitor		1628	2019-12-25	

Figure 4-9 Power monitor utility

Here is the procedure to launch the Power Monitor Utility.

1. Make sure the Power Monitor is downloaded and copy to the Host PC.
2. Make sure the Quartus Prime Programmer is downloaded and installed.
3. Plug 12V DC power to FLIK to power on the FLIK.
4. Connect FLIK to PC Thunderbolt 3 port by a Thunderbolt 3 cable.

5. Launch Power Monitor. A GUI will appear as shown in **Figure 4-10**.

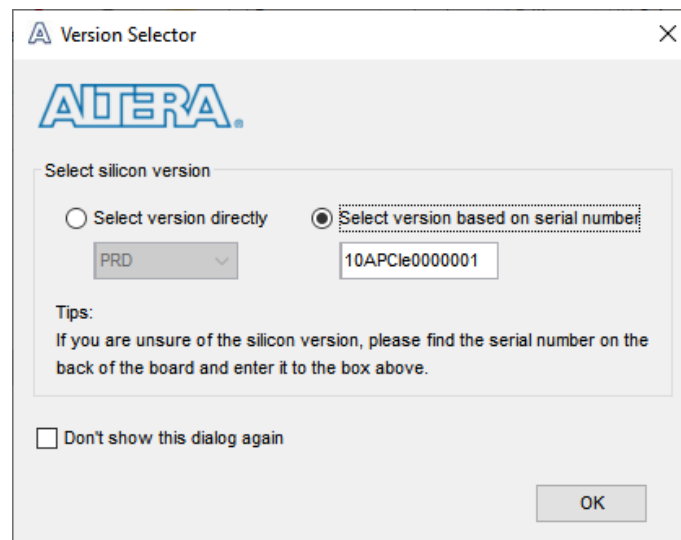


Figure 4-10 Power Monitor Screen

6. In the dialog, Power Status and FPGA/Board Temperature are shown on the GUI.

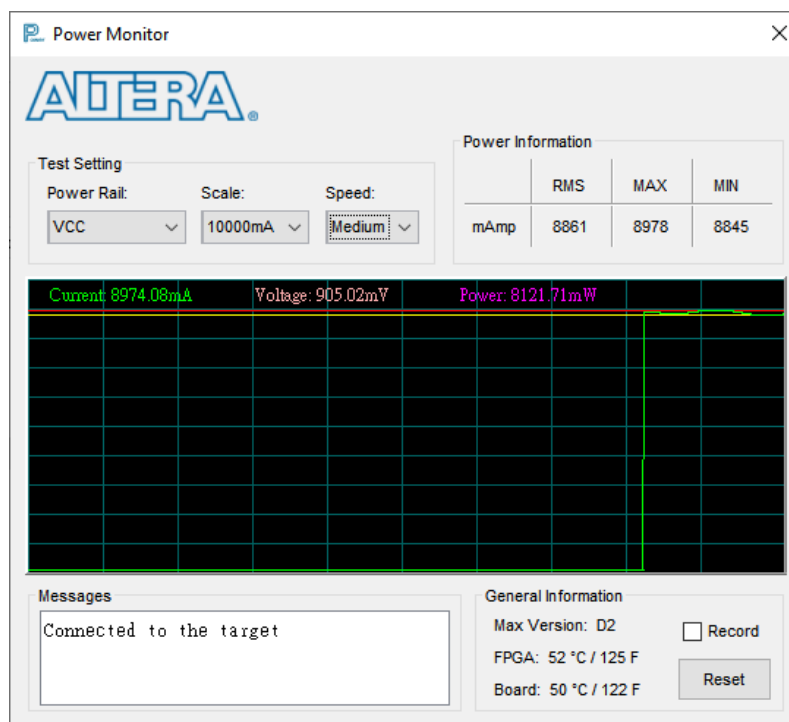


Figure 4-11 Power Monitor Screen Shoot

Additional Information

4.3 Getting Help

Here are the addresses where you can get help if you encounter problems:

■ Terasic Technologies

9F., No.176, Sec.2, Gongdao 5th Rd,
East Dist, HsinChu City, Taiwan, 30070

Email: support@terasic.com

Web: www.terasic.com

FLIK Web: flik.terasic.com

■ Revision History

Date	Version	Changes
2019.09	First publication	
2020.01	V1.1	Modify section 3.1 and 4.2