

Foot1
F1
Foot2
F2
Foot3
F3
Foot4
F4

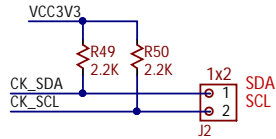
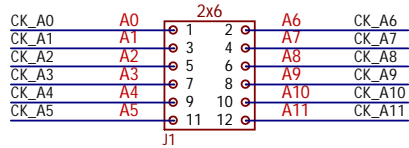
PYNQ Digilent Inc. Xilinx Texas Instruments CE ROHS Chinese ROHS

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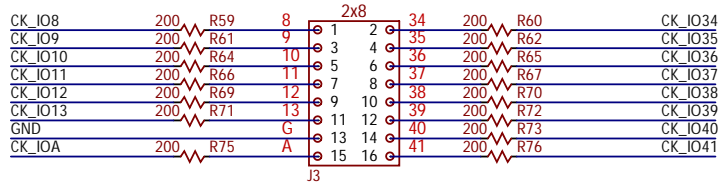
Circuit PMODs, User I/O
Doc# 6003-500-017
Engineer GTM
Author DL
Date 8/10/16
Sheet# 1 out of 13



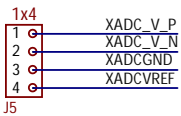
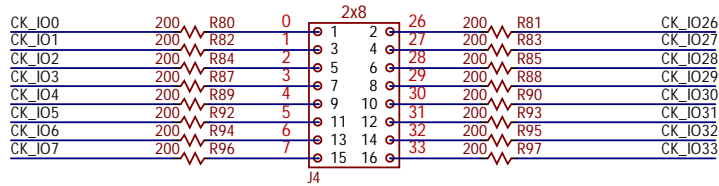
ANALOG



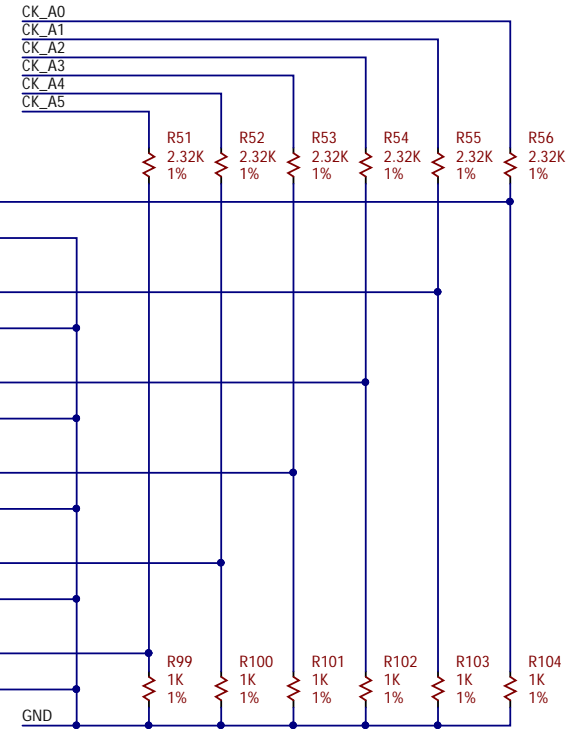
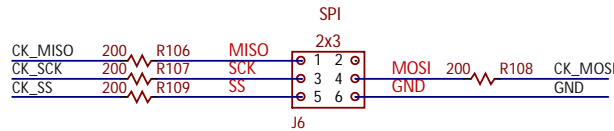
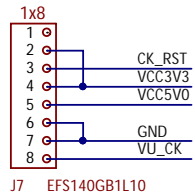
IOH



IOL



POWER

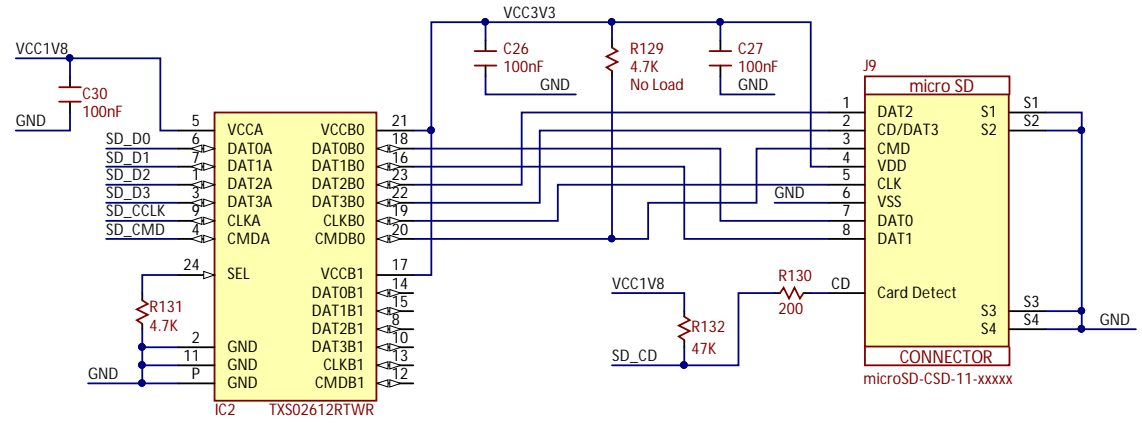
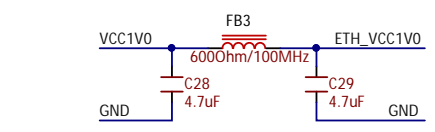
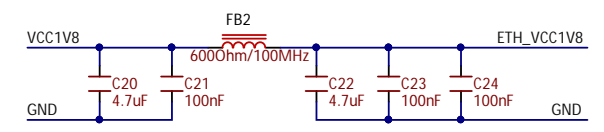
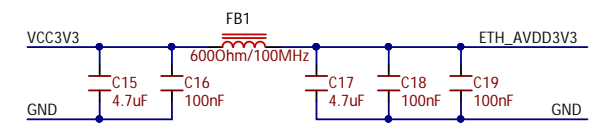
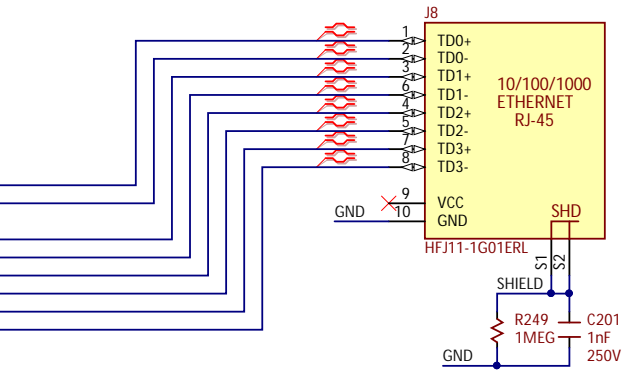
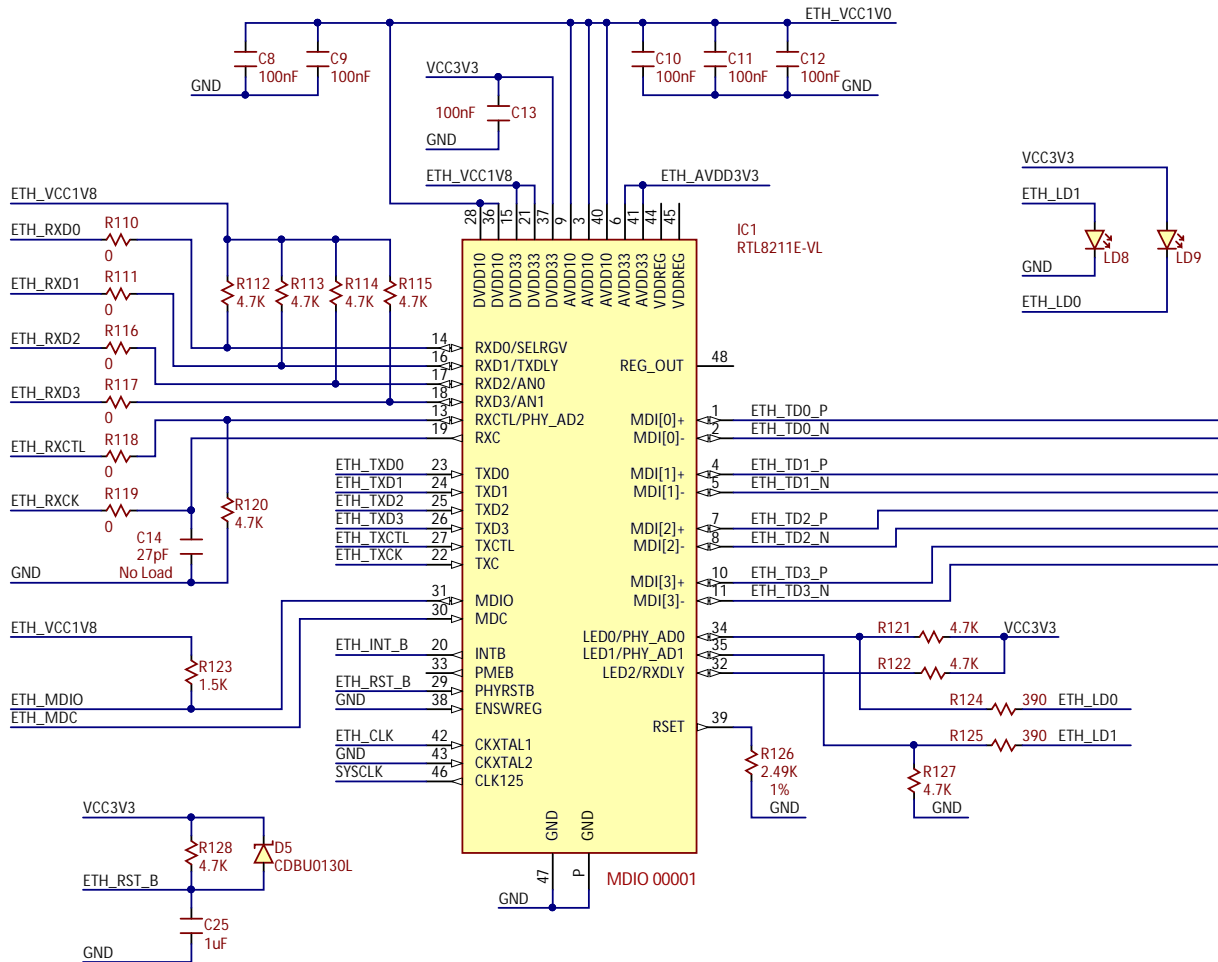


Note: Terminate N signals next to Analog Header

Title		Rev
PYNQ-Z1		C.0
Circuit		Copyright 2016
CHiPKIT IO		
Doc#	6003-500-017	
Engineer	GTM	
Author	DL	
Date	8/10/16	
Sheet#	2 out of 13	



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Title		Rev
PYNQ-Z1		C.0
Circuit		Ethernet and SD Card
Doc#		6003-500-017
Engineer		GTM
Author		DL
Date		8/10/16
Sheet#		3 out of 13
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A

B

C

D

A

B

C

D

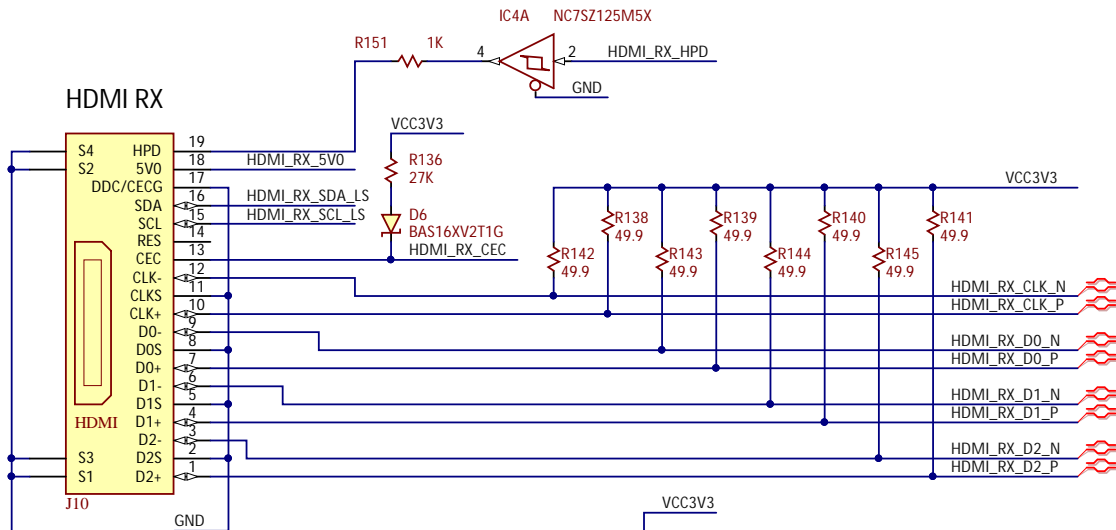
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2

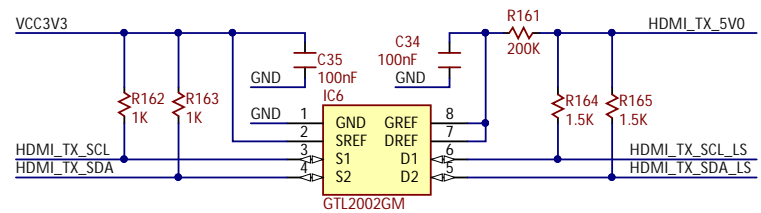
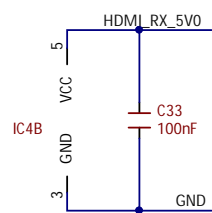
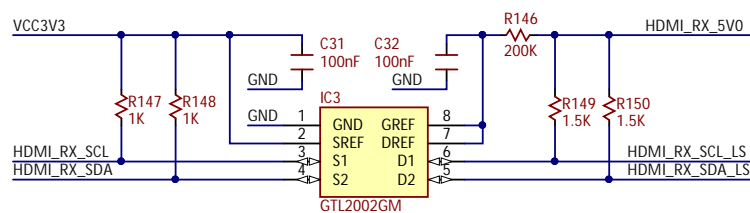
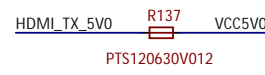
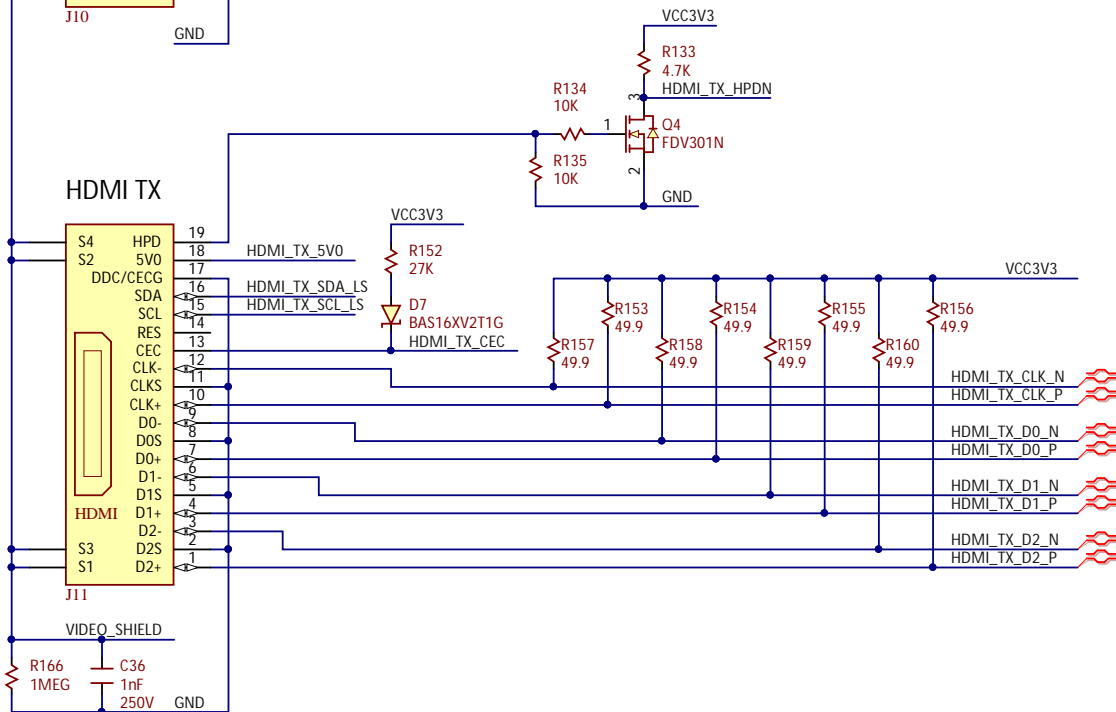
3

4

HDMI RX



HDMI TX



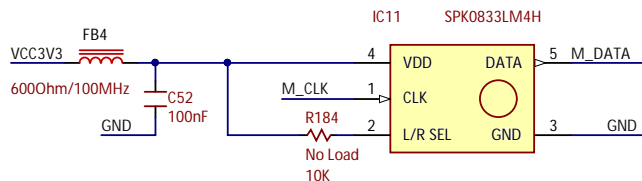
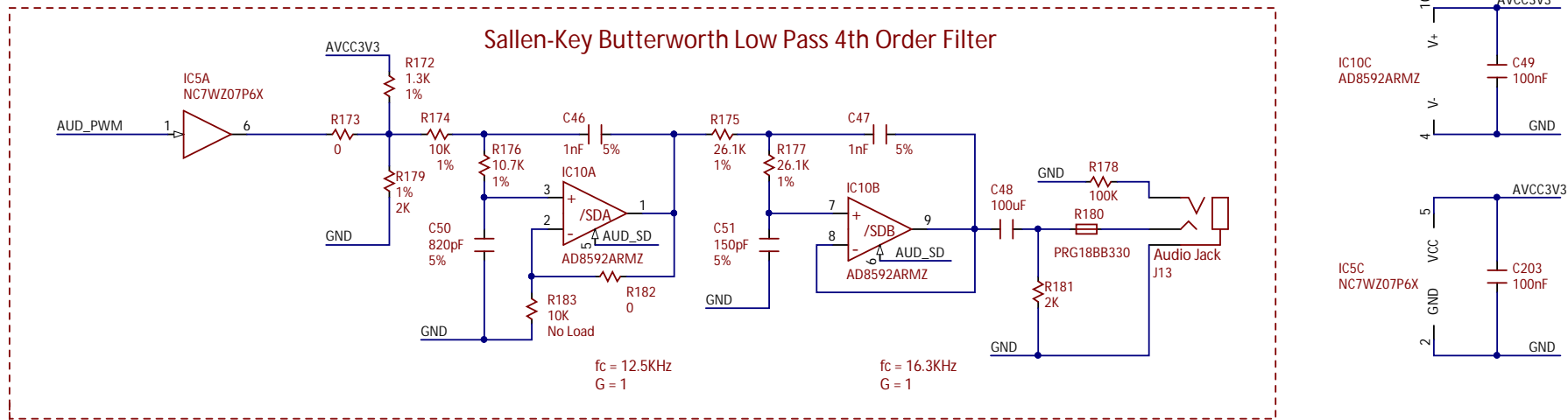
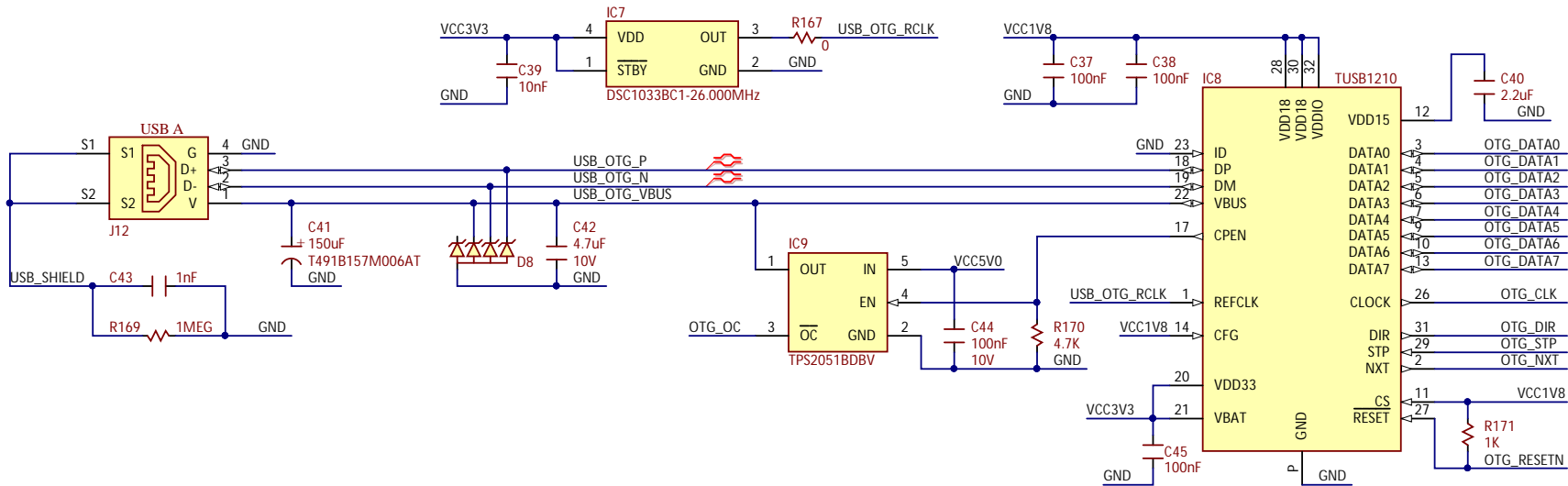
Title PYNQ-Z1		Rev C.0 Copyright 2016
Circuit HDMI	Doc# 6003-500-017	 A National Instruments Company
Engineer GTM	Author DL	
Date 8/10/16	Sheet# 4 out of 13	

1

2

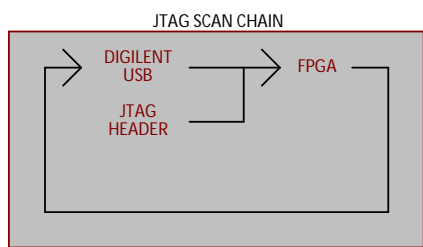
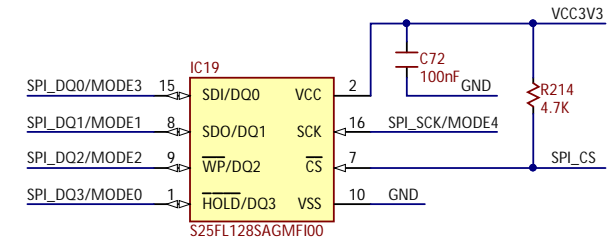
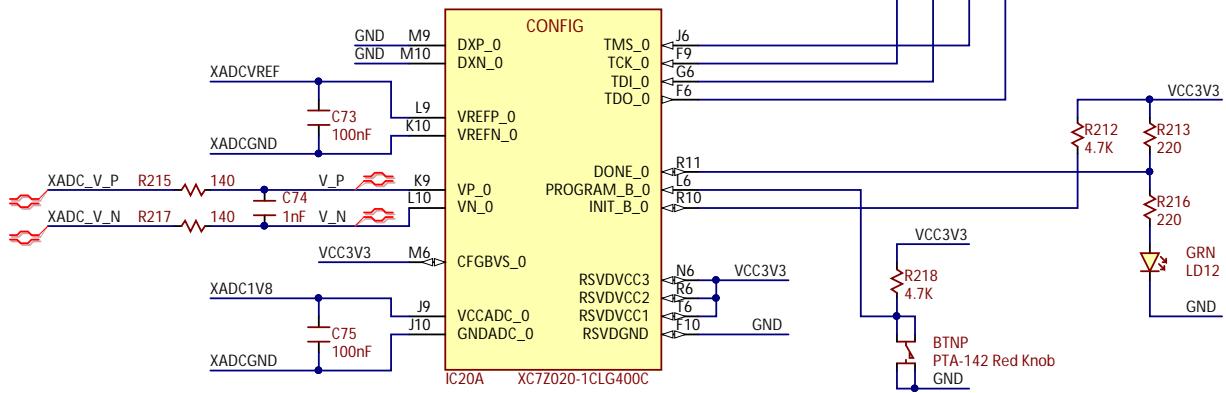
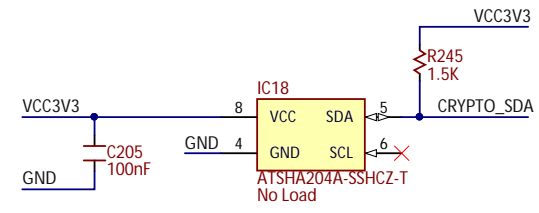
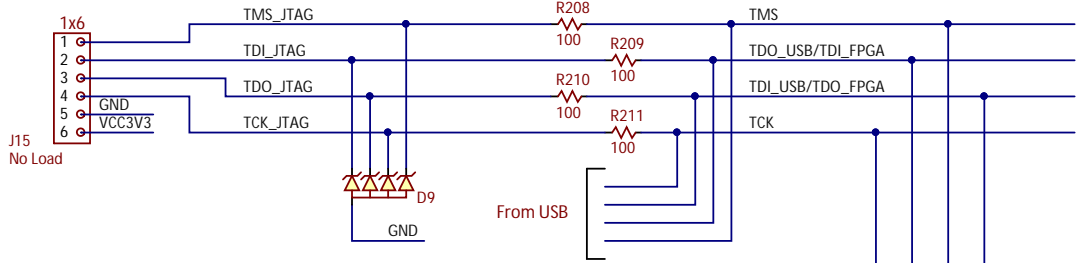
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4

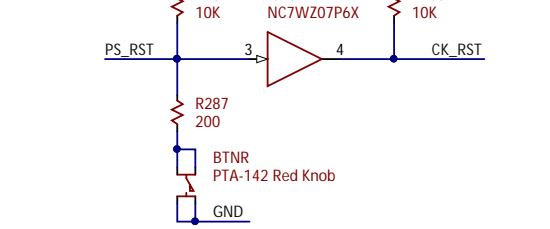
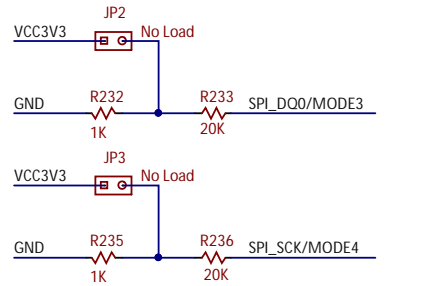
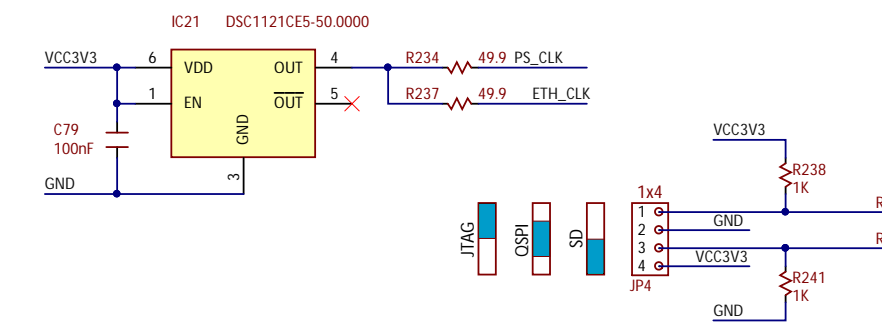
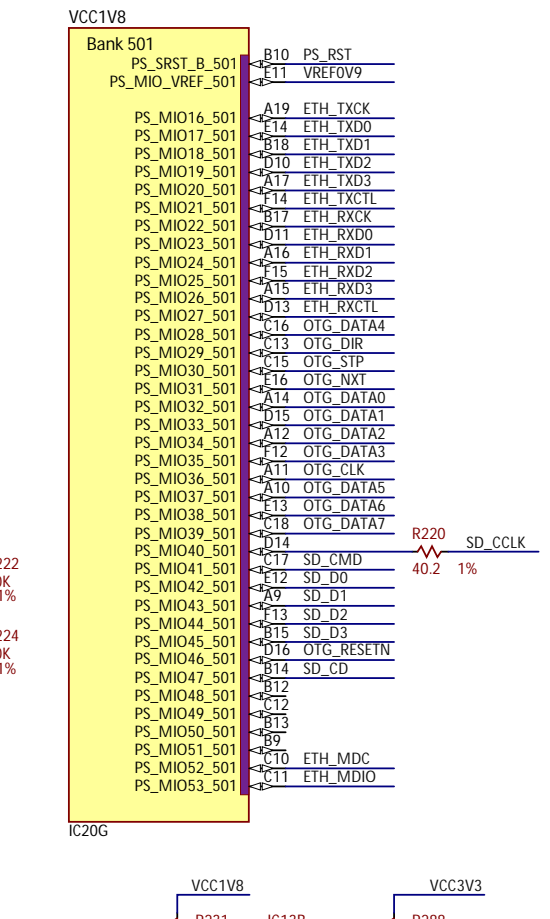
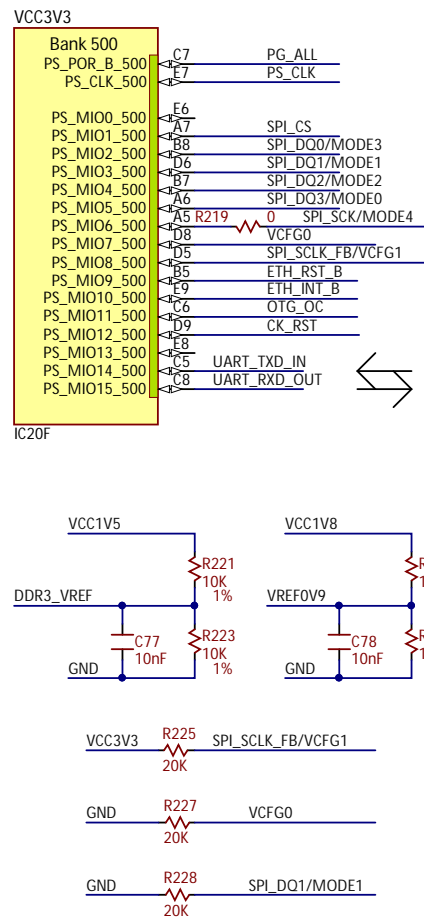
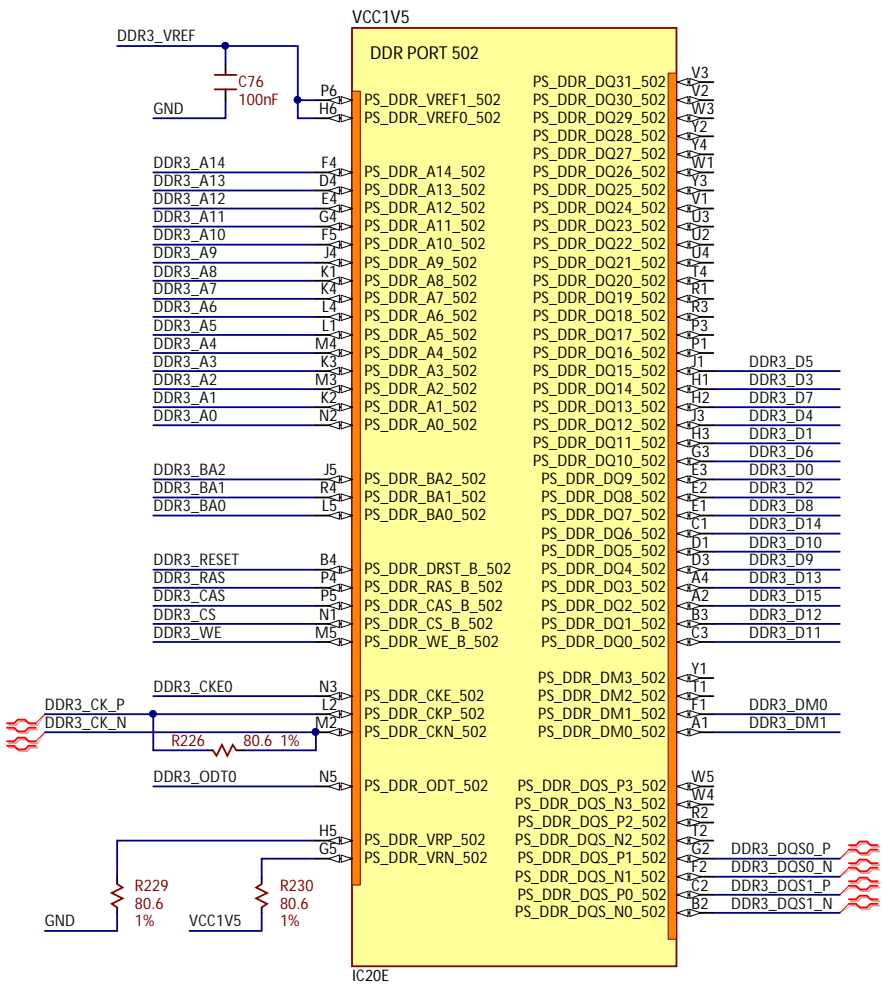


Title		Rev
PYNQ-Z1		C.0
Circuit		USB HOST, MIC, Audio Out
Doc#		6003-500-017
Engineer		GTM
Author		DL
Date		8/10/16
Sheet#		5 out of 13
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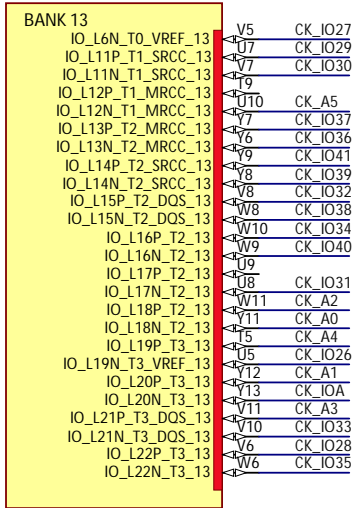
Title		Rev
PYNQ-Z1		C.0
Circuit		Copyright 2016
FPGA Configuration, Flash		
Doc#	6003-500-017	
Engineer	GTM	
Author	DL	
Date	8/10/16	
Sheet#	7 out of 13	



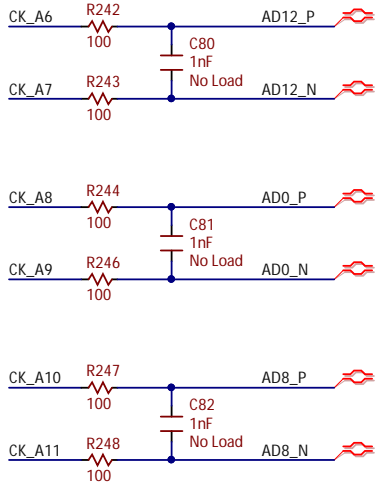
Title PYNQ-Z1		Rev C.0 Copyright 2016
Circuit DDR and MIO Banks		
Doc#	6003-500-017	
Engineer	GTM	
Author	DL	
Date	8/10/16	
Sheet#	8 out of 13	



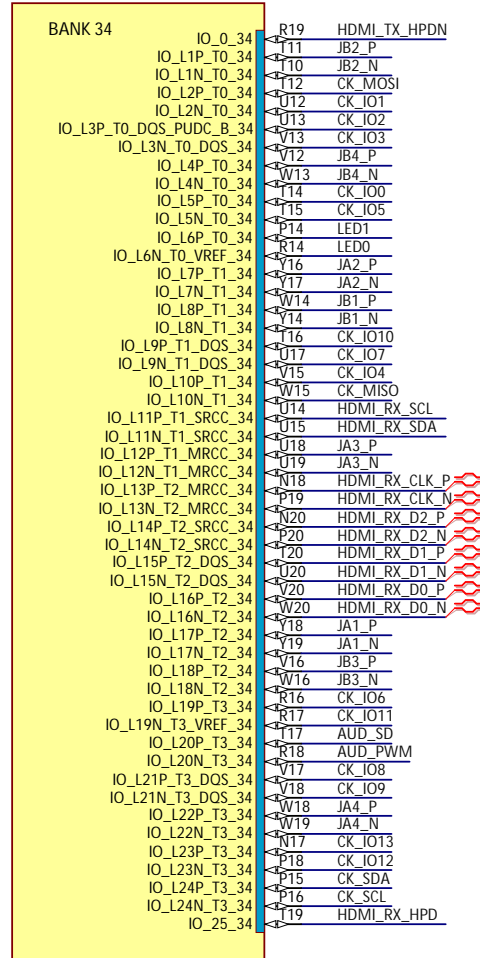
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IC20B

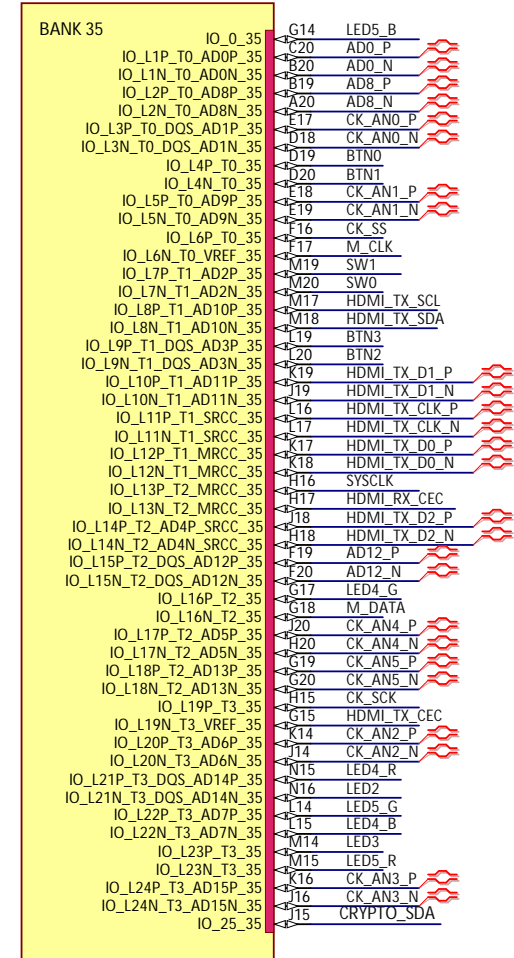


VCC3V3



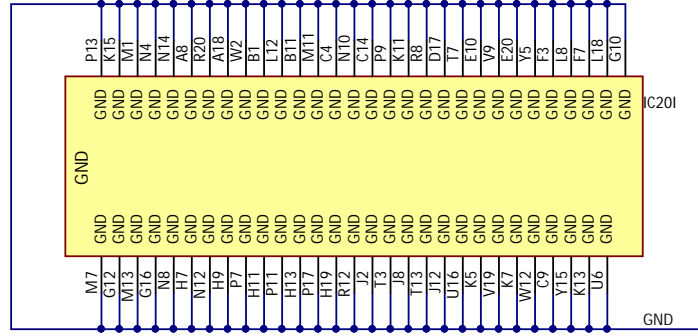
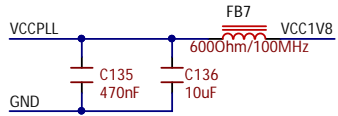
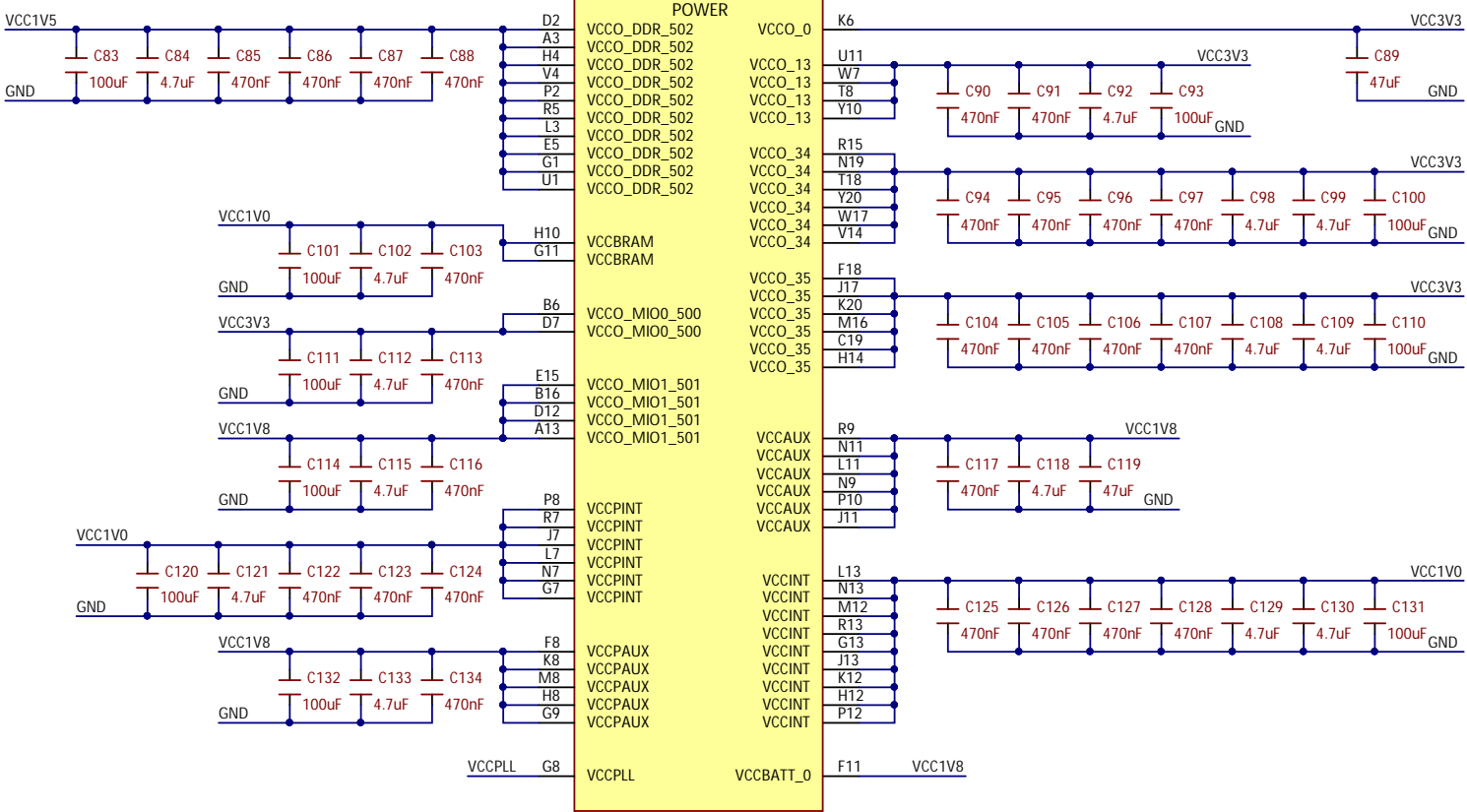
IC20C

VCC3V3

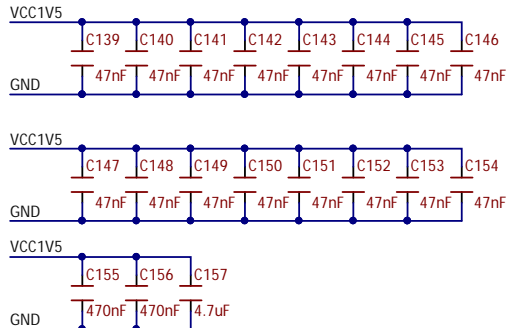
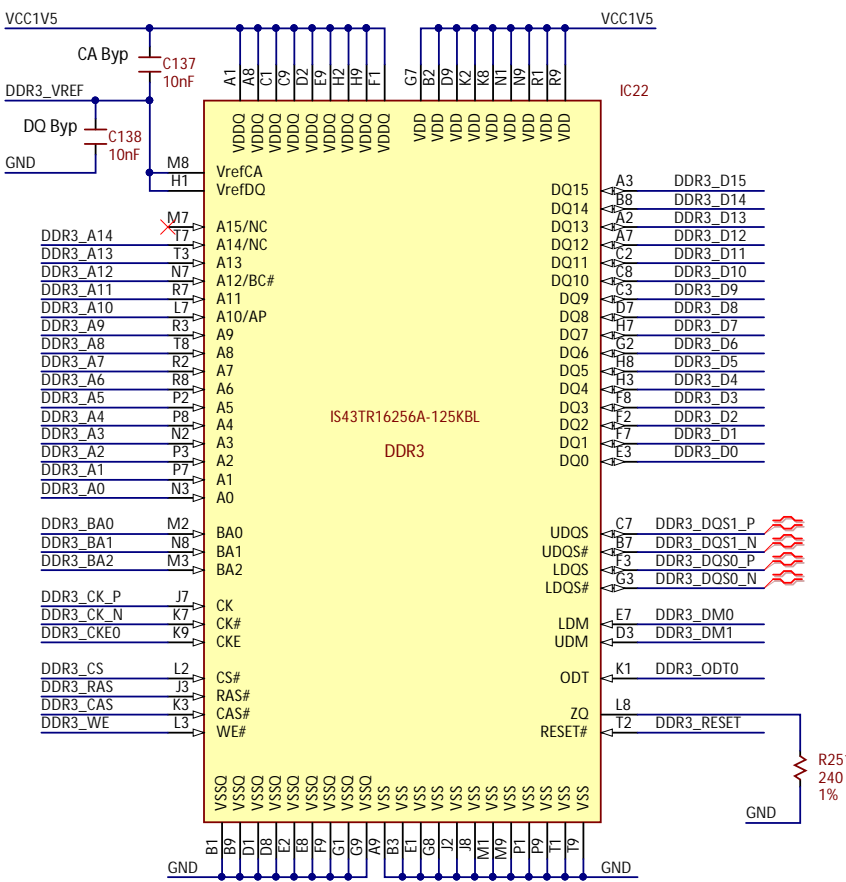


IC20D

Title		Rev	
PYNQ-Z1		C.0	
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Circuit	FPGA Banks, Anti Alias Filters		
Doc#	6003-500-017		
Engineer	GTM		
Author	DL		
Date	8/10/16		
Sheet#	9 out of 13		

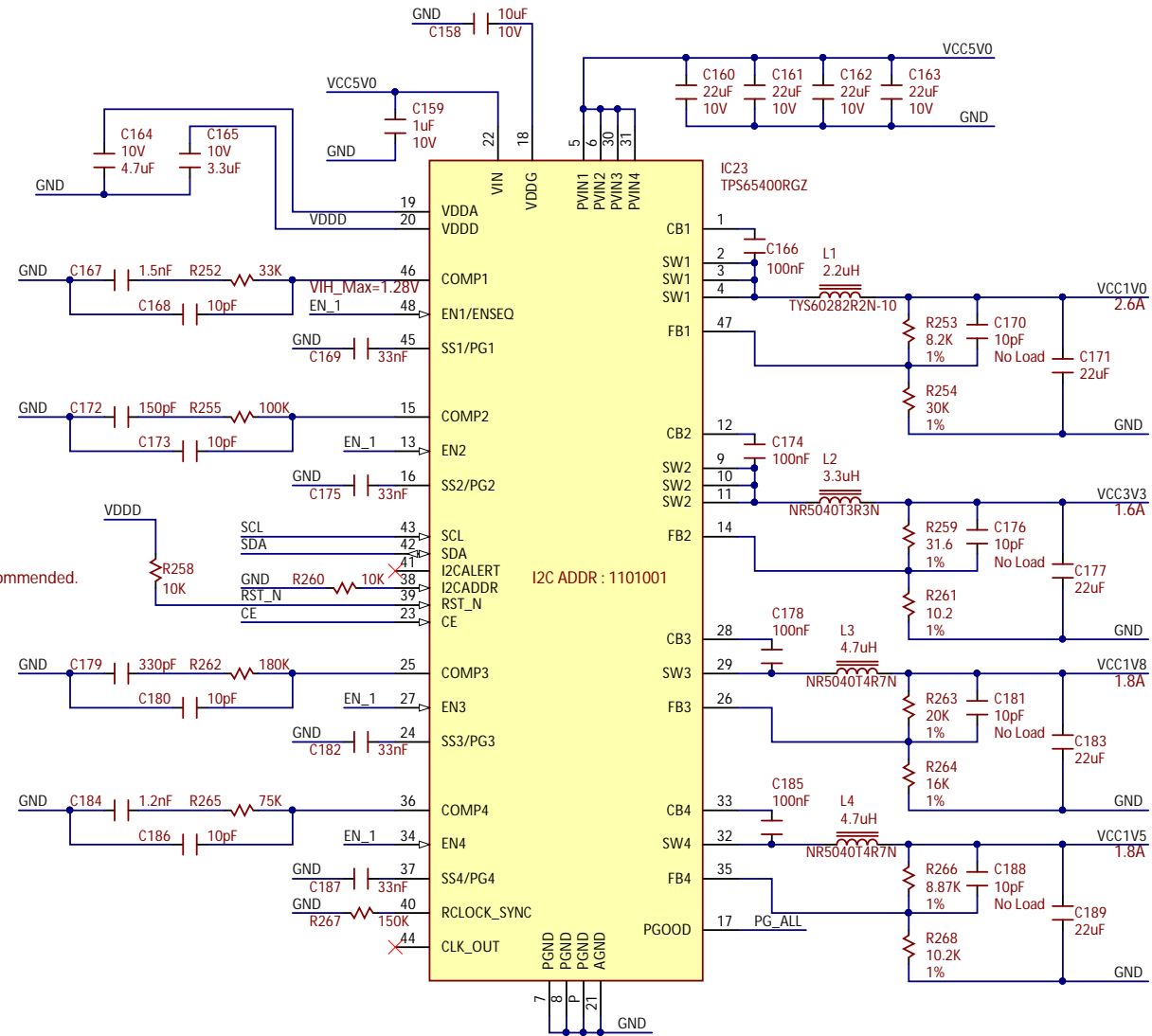
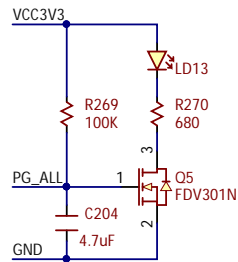
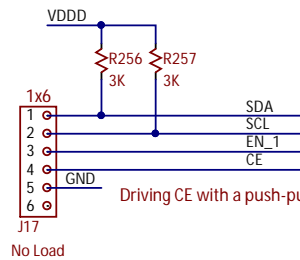


Title PYNQ-Z1		Rev C.0 Copyright 2016
Circuit FPGA Power	Doc# 6003-500-017	 A National Instruments Company
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Date 8/10/16	Sheet# 10 out of 13	



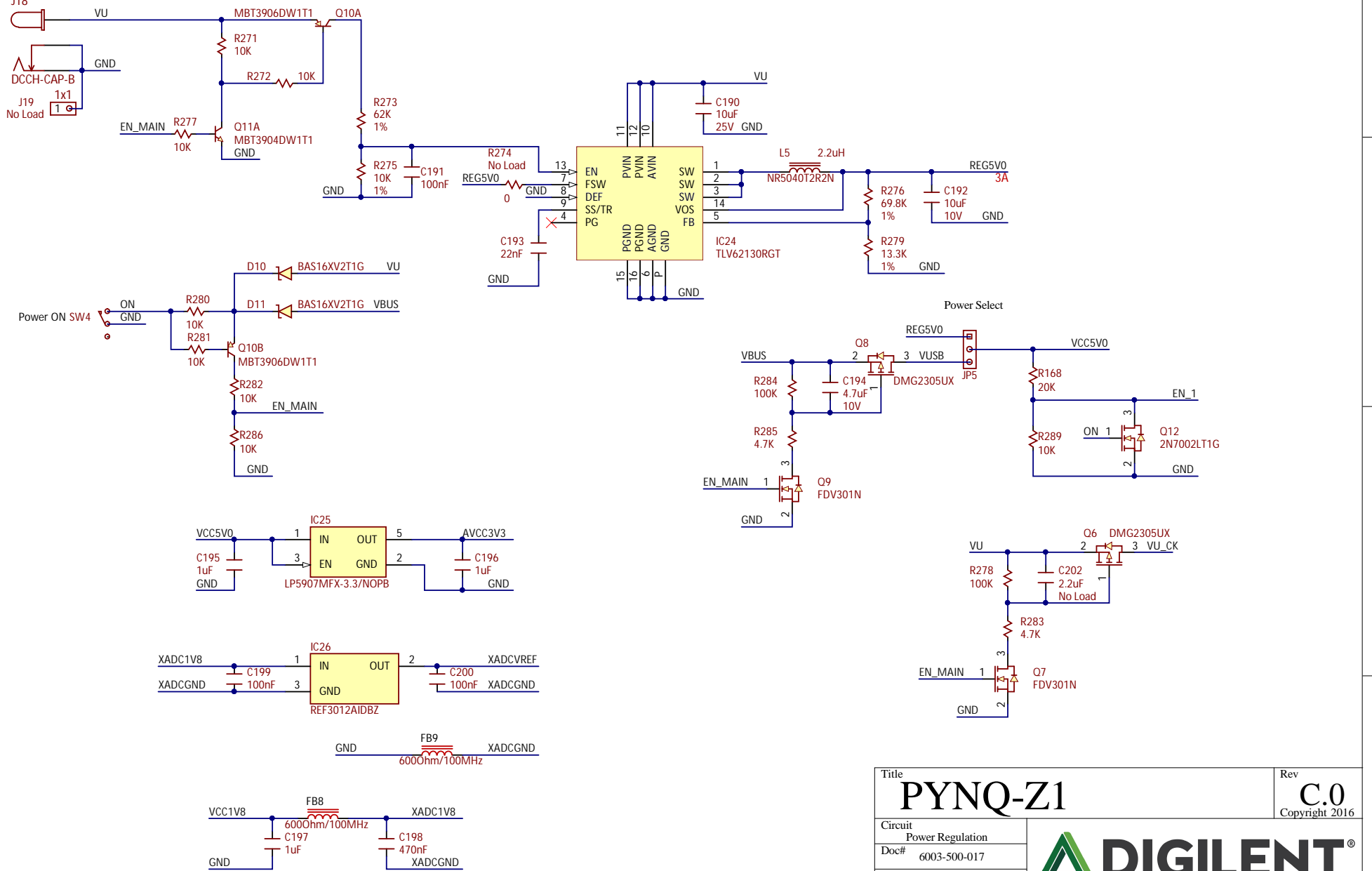
Title PYNQ-Z1		Rev C.0 Copyright 2016
Circuit DDR3 Memory	Doc# 6003-500-017	 A National Instruments Company
Engineer GTM	Author DL	
Date 8/10/16	Sheet# 11 out of 13	

1. VCC1V0
2. VCC1V8
3. VCC1V5
4. VCC3V3



Title PYNQ-Z1		Rev C.0 Copyright 2016
Circuit Power Regulation		
Doc# 6003-500-017		
Engineer GTM		
Author DL		
Date 8/10/16		
Sheet# 12 out of 13		
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Note: Input Voltage 7-15V.



Title PYNQ-Z1		Rev C.0
Circuit Power Regulation		Copyright 2016
Doc#	6003-500-017	
Engineer	GTM	
Author	DL	
Date	8/10/16	
Sheet#	13 out of 13	

