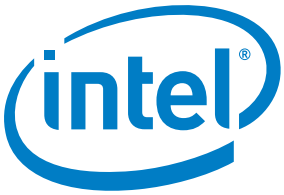

# Intel® Quark™ microcontroller D2000

## Pin Connectivity

*December 2015*

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# Revision History

| Date | Revision | Description |
|---|---|---|
| December 2015 | 001 | Initial release |

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# 1.0 Introduction

The Intel™ Quark® microcontroller D2000 is an ultra-low power Intel Architecture (IA) SoC that integrates an Intel® Quark™ processor core with on-die volatile and non-volatile storage and I/O interfaces into a single system-on-chip solution. This document outlines the pin map coordinates for the Intel™ Quark® microcontroller D2000.

## 1.1 Terminology

**Table 1. Terminology**

| Term | Description |
|---|---|
| ADC | Analog-to-Digital Converter |
| CRB | Customer Reference Board |
| I2C | Inter-Integrated Circuit |
| JTAG | Joint Test Action Group |
| QFN | Quad Flat No-Leads |
| SoC | System on Chip |
| SPI | Serial Peripheral Interface |



# 2.0 System Assumptions

## 2.1 General Assumptions

This section covers general Intel™ Quark® microcontroller D2000 module and Customer Reference Board (CRB) system topology and interface connectivity assumptions.

# 3.0 Pins and Package Information

The Intel™ Quark® microcontroller D2000 is delivered in a 6 mm x 6 mm Quad Flat No-Leads (QFN) package.

## 3.1 SoC Attributes

- Package parameters: 6 mm x 6 mm (QFN)
- Pin Count: 40

All units: mm

Tolerances if not specified:

- .X: ± 0.1
- .XX: ± 0.05
- Angles: ± 1.0 degrees

## 3.2 Pin Multiplexing

The SoC has 15 dedicated pins + 1 QFN GND plane and 25 functional pins which can be configured as GPIO (GPIO[24:0]) or other functions (I2C/UART/SPI/JTAG). There are two major I/O modes: user mode and test mode. In user mode, each pin can be individually configured in one of the four user modes (FUNC 0/1/2/3). By default, after power-on-reset (RST_N) or cold reset, the SoC comes up in user mode 0 function (FUNC0). SoC firmware and software enable the platform-specific configuration by programming the respective I/O pad control registers. Test mode is selected through JTAG interface wherein pins take the test mode functions as defined.

Out of 25 functional pins, 19 pins are double bonded to analog input pads and digital pads while 6 pins are digital only pads. All analog pads (AI[18:0]) are specified with respect to AVDD, and all digital pads are specified with respect to IOVDD. The analog inputs (AI) are connected to an ADC or comparators inside the SoC. AI[5:0] are connected to a fast response/high performance comparator, and AI[18:6] are connected to a slow response/low power comparator. Any wake-capable analog inputs are connected only to any of AI[18:6] and not to AI[5:0].

Gray shaded I/Os are dedicated I/Os and not pin multiplexed.

## Table 2. Pin Multiplexing

| Pin Number | User Mode 0 | User Mode 1 | User Mode 2 | User Mode 3 |
|---|---|---|---|---|
| VSS | GND | GND | GND | GND |
| 27 | PVDD | PVDD | PVDD | PVDD |
| 40 | AVDD | AVDD | AVDD | AVDD |
| 12 | IOVDD | IOVDD | IOVDD | IOVDD |
| 28 | VSENSE | VSENSE | VSENSE | VSENSE |
| 25 | GSENSE | GSENSE | GSENSE | GSENSE |
| 26 | LX | LX | LX | LX |
| 29 | VREN | VREN | VREN | VREN |
| 17 | DVDD | DVDD | DVDD | DVDD |
| 30 | RST_N | RST_N | RST_N | RST_N |
| 22 | RTC_XTALI | RTC_XTALI | RTC_XTALI | RTC_XTALI |
| 23 | RTC_XTALO | RTC_XTALO | RTC_XTALO | RTC_XTALO |
| 19 | HYB_XTALI | HYB_XTALI | HYB_XTALI | HYB_XTALI |
| 20 | HYB_XTALO | HYB_XTALO | HYB_XTALO | HYB_XTALO |
| 1 | AR | AR | AR | AR |
| 31 | GPIO0 | AI0 | SPI_M_SS0 | DBG_VISA0 |
| 32 | GPIO1 | AI1 | SPI_M_SS1 | DBG_VISA1 |
| 33 | GPIO2 | AI2 | SPI_M_SS2 | DBG_VISA2 |
| 34 | GPIO3 | AI3 | SPI_M_SS3 | DBG_VISA3 |
| 35 | GPIO4 | AI4 | RTC_CLK_OUT | DBG_VISA4 |
| 36 | GPIO5 | AI5 | SYS_CLK_OUT | DBG_VISA5 |
| 37 | GPIO6 | AI6 | I2C_SCL | DBG_VISA6 |
| 38 | GPIO7 | AI7 | I2C_SDA | DBG_VISA7 |
| 39 | GPIO8 | AI8 | SPI_S_SCLK | DBG_VISA8 |
| 11 | GPIO9 | AI9 | SPI_S_SDIN | DBG_VISA9 |

| Pin Number | User Mode 0 | User Mode 1 | User Mode 2 | User Mode 3 |
|---|---|---|---|---|
| 2 | GPIO10 | AI10 | SPI_S_SDOUT | DBG_VISA10 |
| 3 | GPIO11 | AI11 | SPI_S_SCS | DBG_VISA11 |
| 4 | GPIO12 | AI12 | UART_A_TXD | DBG_VISA12 |
| 5 | GPIO13 | AI13 | UART_A_RXD | DBG_VISA13 |
| 6 | GPIO14 | AI14 | UART_A_RTS/UART_A_DE | DBG_VISA14 |
| 7 | GPIO15 | AI15 | UART_A_CTS/UART_A_RE | DBG_VISA15 |
| 8 | GPIO16 | AI16 | SPI_M_SCLK | DBG_VISA16 |
| 9 | GPIO17 | AI17 | SPI_M_TXD | DBG_VISA17 |
| 10 | GPIO18 | AI18 | SPI_M_RXD | - |
| 18 | TDO | GPIO19 | PWM0 | - |
| 13 | TRST_N | GPIO20 | UART_B_TXD | - |
| 14 | TCK | GPIO21 | UART_B_RXD | - |
| 15 | TMS | GPIO22 | UART_B_RTS/UART_B_DE | - |
| 16 | TDI | GPIO23 | UART_B_CTS/UART_B_RE | - |
| 21 | GPIO24 | LPD_SIG_OUT | PWM1 | - |

- All analog I/Os (AI[18:0]/ADC[18:0]) are specified with respect to the AVDD rail.
- All digital I/Os are 3.3V tolerant.
- All digital I/Os include configurable drive strength namely low-drive (12 mA) and high-drive (16 mA) modes. By default, all digital I/Os come up in low-drive mode.
- All digital I/Os include a configurable pull-up with the pull-up disabled by default, except for F_20, F_22, F_23 (TRST_N, TMS, TDI) where the pull-up is enabled by default.

UART_A/B_CTS (input) or UART_A/B_RE (output) is available based on the UART mode of operation (RS232 or RS485) configurable in the respective UART controller, similarly for UART_A/B_RTS (output) or UART_A/B_DE (output). The default is RS232. FW can choose to enable the input direction and output direction for CTS/RE pins, and hardware will control the output enable of these pins based on RS232 or RS485 mode of operation if these pins are configured for UART function.

The JTAG interface is enabled by default (user mode 0) to assist in debug as well as embedded flash programming.

The F_25 pad is not bonded to any pin. This pad (mapped as pin 25 for pinmux configuration in the System Control Subsystem) is configured by FW in input disabled mode (Input Enable = 0; User mode 3 which makes Output Enable disabled).

DVDD_2 and DVDD are identical and are connected to the same source.

## 3.3 Alphabetical Pin Listing

### Table 3. Alphabetical Pin Listing

| Pin Number | User Mode 0 | User Mode 1 | User Mode 2 | User Mode 3 |
|---|---|---|---|---|
| 1 | AR | AR | AR | AR |
| 2 | GPIO10 | AI10 | SPI_S_SDOUT | DBG_VISA10 |
| 3 | GPIO11 | AI11 | SPI_S_SCS | DBG_VISA11 |
| 4 | GPIO12 | AI12 | UART_A_TXD | DBG_VISA12 |
| 5 | GPIO13 | AI13 | UART_A_RXD | DBG_VISA13 |
| 6 | GPIO14 | AI14 | UART_A_RTS/ UART_A_DE | DBG_VISA14 |
| 7 | GPIO15 | AI15 | UART_A_CTS/ UART_A_RE | DBG_VISA15 |
| 8 | GPIO16 | AI16 | SPI_M_SCLK | DBG_VISA16 |
| 9 | GPIO17 | AI17 | SPI_M_TXD | DBG_VISA17 |
| 10 | GPIO18 | AI18 | SPI_M_RXD | - |
| 11 | GPIO9 | AI9 | SPI_S_SDIN | DBG_VISA9 |
| 12 | IOVDD | IOVDD | IOVDD | IOVDD |
| 13 | TRST_N | GPIO20 | UART_B_TXD | - |
| 14 | TCK | GPIO21 | UART_B_RXD | - |
| 15 | TMS | GPIO22 | UART_B_RTS/ UART_B_DE | - |
| 16 | TDI | GPIO23 | UART_B_CTS/ UART_B_RE | - |

| Pin Number | User Mode 0 | User Mode 1 | User Mode 2 | User Mode 3 |
|---|---|---|---|---|
| 17 | DVDD | DVDD | DVDD | DVDD |
| 18 | TDO | GPIO19 | PWM0 | - |
| 19 | HYB_XTALI | HYB_XTALI | HYB_XTALI | HYB_XTALI |
| 20 | HYB_XTALO | HYB_XTALO | HYB_XTALO | HYB_XTALO |
| 21 | GPIO24 | LPD_SIG_OUT | PWM1 | - |
| 22 | RTC_XTALI | RTC_XTALI | RTC_XTALI | RTC_XTALI |
| 23 | RTC_XTALO | RTC_XTALO | RTC_XTALO | RTC_XTALO |
| 24 | DVDD_2 | DVDD_2 | DVDD_2 | DVDD_2 |
| 25 | GSENSE | GSENSE | GSENSE | GSENSE |
| 26 | LX | LX | LX | LX |
| 27 | PVDD | PVDD | PVDD | PVDD |
| 28 | VSENSE | VSENSE | VSENSE | VSENSE |
| 29 | VREN | VREN | VREN | VREN |
| 30 | RST_N | RST_N | RST_N | RST_N |
| 31 | GPIO0 | AI0 | SPI_M_SS0 | DBG_VISA0 |
| 32 | GPIO1 | AI1 | SPI_M_SS1 | DBG_VISA1 |
| 33 | GPIO2 | AI2 | SPI_M_SS2 | DBG_VISA2 |
| 34 | GPIO3 | AI3 | SPI_M_SS3 | DBG_VISA3 |
| 35 | GPIO4 | AI4 | RTC_CLK_OUT | DBG_VISA4 |
| 36 | GPIO5 | AI5 | SYS_CLK_OUT | DBG_VISA5 |
| 37 | GPIO6 | AI6 | I2C_SCL | DBG_VISA6 |
| 38 | GPIO7 | AI7 | I2C_SDA | DBG_VISA7 |
| 39 | GPIO8 | AI8 | SPI_S_SCLK | DBG_VISA8 |
| 40 | AVDD | AVDD | AVDD | AVDD |
| VSS | GND | GND | GND | GND |

## Figure 1. Mechanical Drawing of Package