AN3093
Application note

ALTAIR05T-800 5 W wide range CV-CC optoless adapter demonstration board

1 Introduction

This application note describes the demonstration board of the all primary-sensing switching regulator ALTAIR05T-800 and presents the results of its bench evaluation. The board implements a 5 W (5 V / 1 A) wide range mains battery charger with constant voltage/constant current.

The ALTAIR05T-800 combines a high-performance low-voltage PWM controller chip and an 800 V, avalanche rugged power MOSFET in the same package.

The PWM chip is a quasi-resonant (QR) current mode controller IC specifically designed for QR ZVS (zero-voltage switching at switch turn-on) flyback converters.

The device is capable of providing constant output voltage (CV) and constant output current (CC) regulation using primary sensing feedback. This eliminates the need for the optocoupler, the secondary voltage reference, as well as the current sensor, while maintaining very accurate regulation.

Additionally, it is possible to compensate the voltage drop of the output cable, so as to improve CV regulation on the externally accessible terminals.

Extremely low consumption under no-load conditions is ensured thanks to a controlled burst mode operation that, along with the built-in high-voltage startup circuit and the low operating current of the device, helps minimize residual input consumption. Although an auxiliary winding is required in the transformer to correctly perform CV/CC regulation, the chip is capable of powering itself directly from the rectified mains. This is useful especially during CC regulation, where the flyback voltage generated by the winding drops. However, if ultra low no-load input consumption is required to comply with the most stringent energy saving recommendations, then the device needs to be powered via the auxiliary winding.

Figure 1. Demonstration board picture

Contents

1 Introduction 1

2 Test board: design and evaluation 5

3 Efficiency and no-load measurements 11

3.1 Standby optimization: tips for reducing standby consumption 12

Design optimization 13

3.2 Five star charger energy rating 14

4 Typical board waveforms 15

5 V-I output characteristics and cable drop compensation 19

6 Conclusion 22

Appendix A Modes of operation 23

A.1 Constant voltage operation 23

A.2 Constant current operation 24

A.3 Current comparator speed 25

A.4 Cable drop compensation block 26

Revision history 28

List of tables

Table 1. ALTAIR05T-800 demonstration board: electrical specification 5
Table 2. ALTAIR05T-800 demonstration board: bill of material 7
Table 3. ALTAIR05T-800 demonstration board: transformer characteristics 9
Table 4. Efficiency at 115 V_{AC} 11
Table 5. Efficiency at 230 V_{AC} 11
Table 6. Standby consumption 12
Table 7. Document revision history 28

List of figures

Figure 1. Demonstration board picture . . . 1
Figure 2. Electrical schematic . . . 6
Figure 3. PCB: top side and through-hole components(1) . . . 8
Figure 4. PCB: bottom side and SMD components(1) . . . 8
Figure 5. Electrical schematic . . . 9
Figure 6. Side view . . . 9
Figure 7. Bottom side view . . . 10
Figure 8. PCB hole dimensions . . . 10
Figure 9. Efficiency vs. output power . . . 12
Figure 10. No-load consumption score chart . . . 14
Figure 11. Normal operation at full load, at 115 V_{AC} and 230 V_{AC} . . . 16
Figure 12. Normal operation in CC mode with V_{OUT} = 3 V, at 115 V_{AC} and 230 V_{AC} . . . 16
Figure 13. Short-circuit at 115 V_{AC} and 230 V_{AC} . . . 17
Figure 14. Normal operation at no-load, at 115 V_{AC} and 230 V_{AC} . . . 17
Figure 15. Startup at no-load, at 115 V_{AC} and 230 V_{AC} . . . 18
Figure 16. Startup at full load, at 115 V_{AC} and 230 V_{AC} . . . 18
Figure 17. Output characteristic at 115 V_{AC} . . . 19
Figure 18. Output characteristic at 230 V_{AC} . . . 20
Figure 19. Output characteristic without cable drop compensation: R_{CABLE} = 0.32 Ω and R_5 = 10 kΩ . . . 20
Figure 20. Output characteristic with cable drop compensation: R_{CABLE} = 0.32 Ω and R_5 = 10 kΩ . . . 21
Figure 21. Voltage control principle: internal schematic . . . 23
Figure 22. Current control principle . . . 24
Figure 23. Constant current operation: switching cycle waveforms . . . 25
Figure 24. Feed-forward compensation: internal schematic . . . 26
Figure 25. CDC compensation: external configuration . . . 27

2 Test board: design and evaluation

A 5 W battery charger demonstration board based on ALTAIR05T-800 is now presented.

Table 1 summarizes the electrical specifications of the application. *Table 2* provides the bill of materials and *Table 3* lists the transformer specifications. The electrical schematic is shown in *Figure 2* and the PCB layout in *Figure 3* and *Figure 4*.

Table 1. ALTAIR05T-800 demonstration board: electrical specification

Parameter	Value
Input voltage range (V_{IN})	90 - 265 V_{AC}
Mains frequency (f_L)	50 - 60 Hz
Maximum (rated) output power	5 W
Output	V_{OUT} = 5 V ± 5% I_{OUT} = 0 to 1 A ± 7% V_{ripple} < 100 mV
Minimum switching frequency in normal mode	70 kHz
Target average efficiency (at P_{OUT} = 5 W, V_{IN} = 90 - 264 V_{AC})	> 70%(1)
Maximum input power in standby	< 100 mW(2)

1. Compliant with the EPA 2.0 standard for low voltage devices (V_{OUT} < 6, I_{OUT} > 0.55 A).
2. Compliant with the European Code of Conduct, adapter for mobile handheld battery-driven applications, starting from 1st January 2011.

Figure 2. Electrical schematic

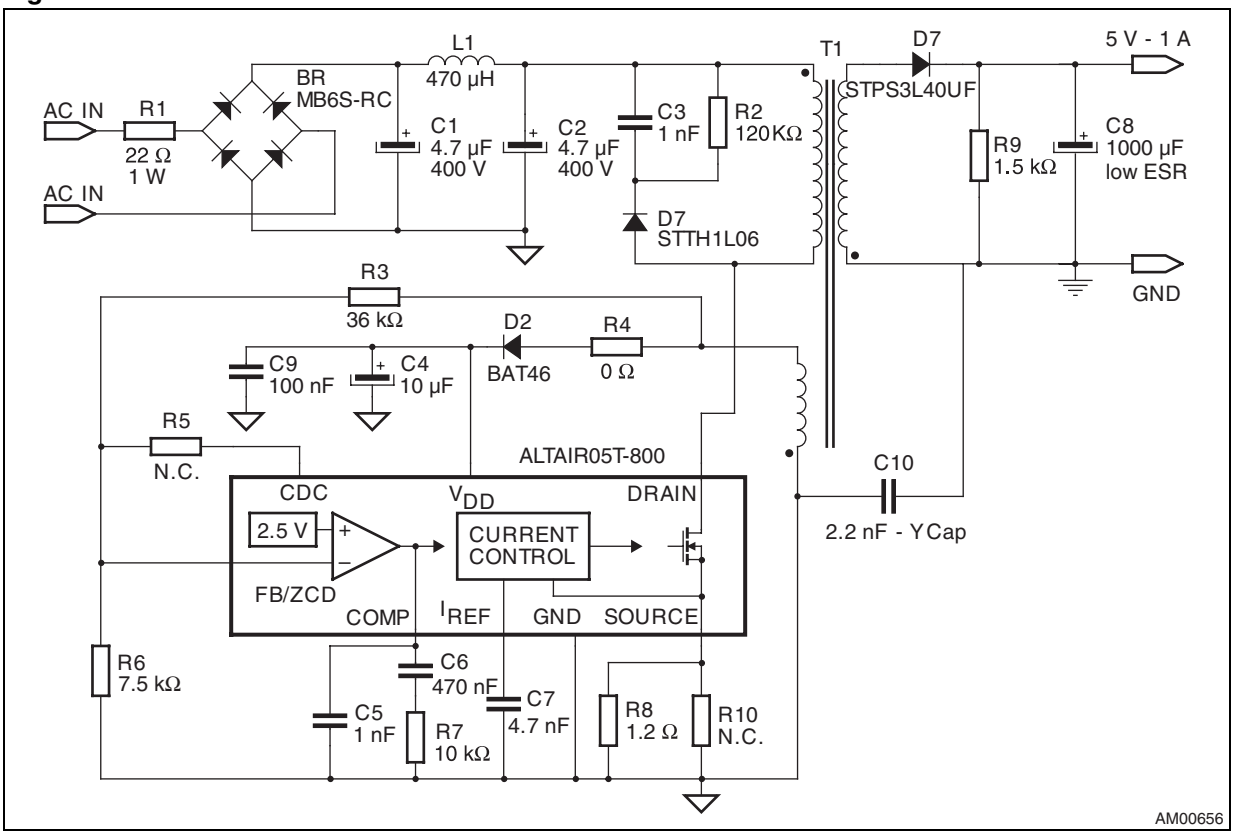
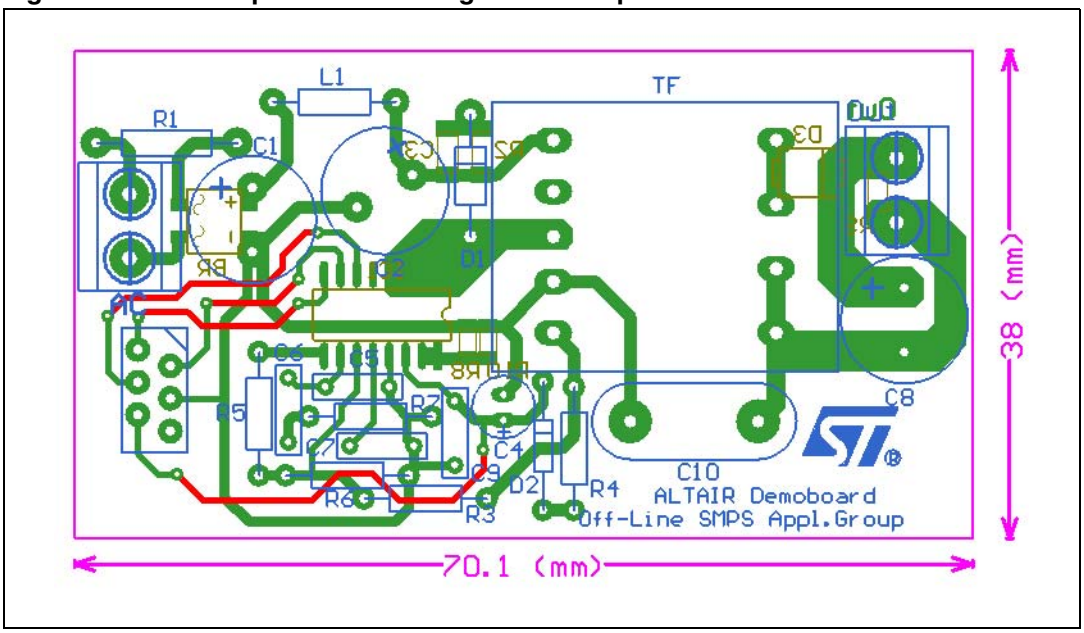


Table 2. ALTAIR05T-800 demonstration board: bill of material(1)

Reference	Part	Description	Note
R1		22 Ω - 1 W	Axial flame proof
R2		120 kΩ SMD (1206)	
R3		36 kΩ	1% tolerance
R4		0 Ω	
R5		Not connected	See *Section A.4: Cable drop compensation block*
R6		7.5 kΩ	1% tolerance
R7		10 kΩ	
R8		1.2 Ω	1% tolerance
R9		1.5 kΩ	
C1, C2		4.7 µF 400 V electrolytic	
C3		1 nF - 500 V XR7	
C4		10 µF - 35 V electrolytic	
C5		1 nF - 25 V	
C6		470 nF - 25 V	
C7		4.7 nF - 25 V	
C8	B41889A4108M	1000 µF - 16 V electrolytic	Epcos
C9		100 nF - 25 V	
C10	Y1- capacitor	2.2 nF - 230 V	
D1	STTH1L06	Ultra fast high voltage diode	STMicroelectronics
D2	BAT46	Small signal Schottky diode	STMicroelectronics
D3	STPS3L40UF	Power Schottky diode	STMicroelectronics
L1	B78108S1474J	470 µH axial inductor	Epcos
BR	MB6S RC	Input bridge rectifier	
TF	1335.0032 rev.1	Flyback transformer	Magnetica®
IC	ALTAIR05T-800	Primary switching regulator	STMicroelectronics

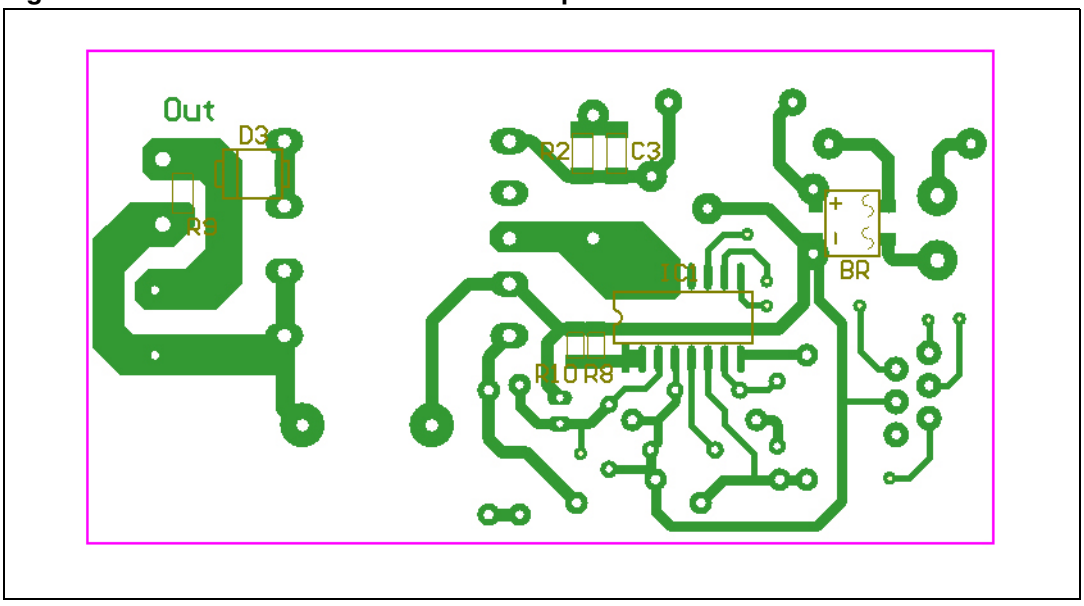
1. If not otherwise specified, all resistors are 5%, 1/4 W.

Figure 3. PCB: top side and through-hole components(1)



1. Layout is not to scale.

Figure 4. PCB: bottom side and SMD components(1)



1. Layout is not to scale.

Table 3. ALTAIR05T-800 demonstration board: transformer characteristics

Name	Value
Manufacturer	Magnetica
Part number	1335.0032 rev. 1
Core	E16/5
Primary inductance	2.2 mH ± 15%
Air gap	0.18 mm
Leakage inductance	66 µH max.
Primary to secondary turn ratio	13.9 ± 5%
Primary to auxiliary turn ratio	5 ± 5%
Primary saturation current	0.4 A_P max. (B_{SAT} = 0.35 T)
Insulation primary to secondary	4 kV

Figure 5. Electrical schematic

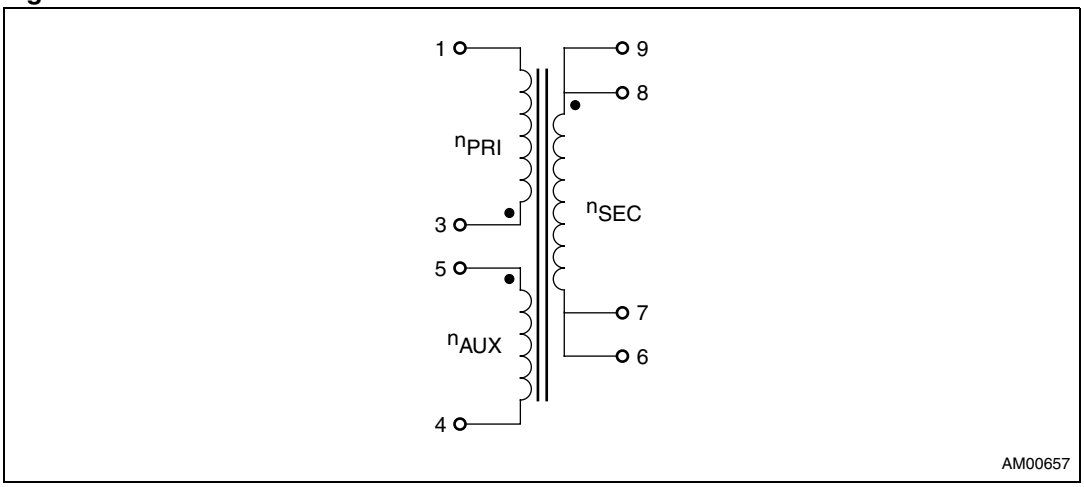


Figure 6. Side view

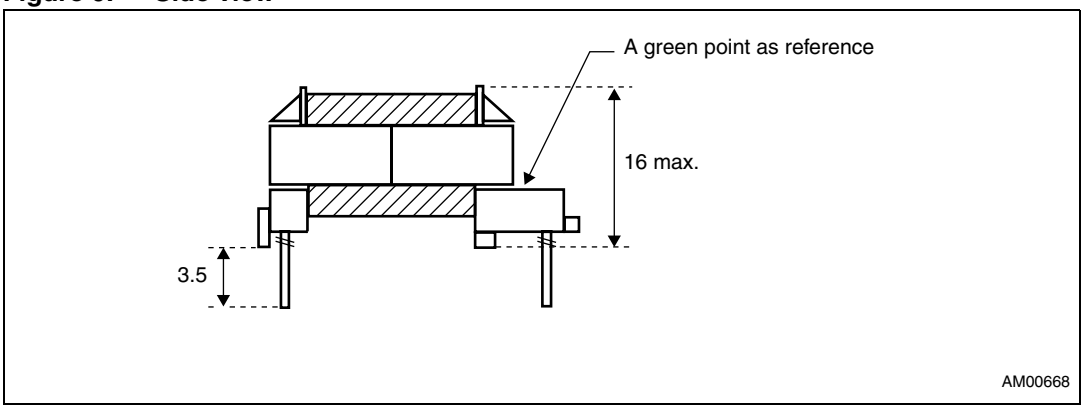


Figure 7. Bottom side view

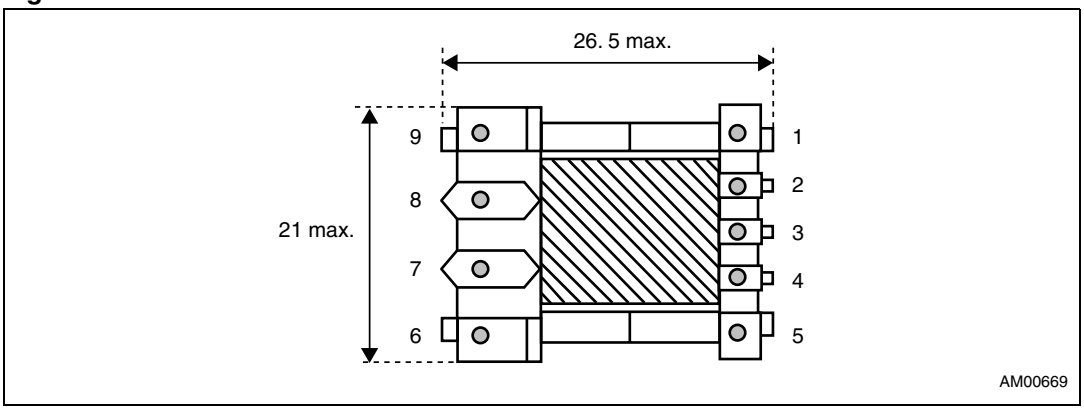
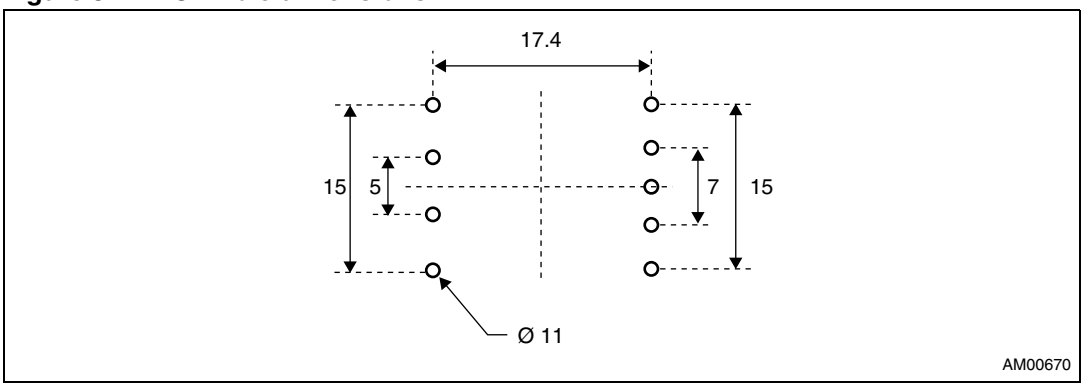


Figure 8. PCB hole dimensions



3 Efficiency and no-load measurements

The efficiency of the converter has been measured in different load and line voltage conditions.

According to the Energy Star average active mode testing efficiency method, the efficiency measurements have been performed at 25%, 50% and 75% and 100% of the rated output power, at both 115 V_{AC} and 230 V_{AC}.

Table 4 and *Table 5* show the results.

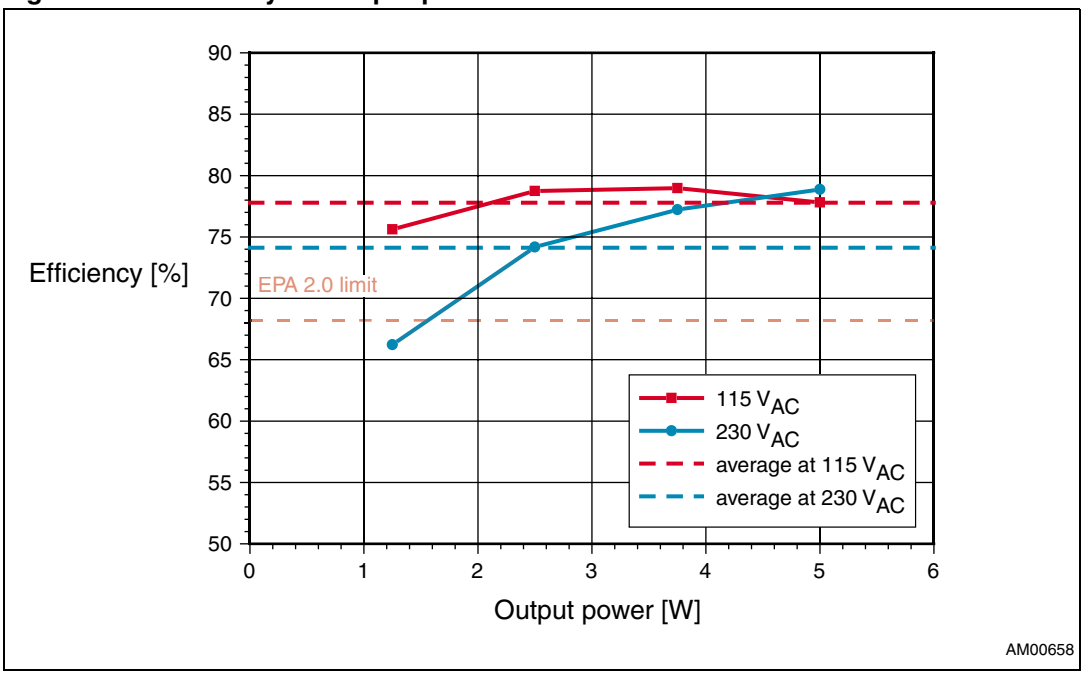
Table 4. Efficiency at 115 V_{AC}

Load [%]	I_{OUT} [A]	V_{OUT} [V]	P_{OUT} [W]	P_{IN} [W]	Efficiency [%]
25	0.25	4.97	1.243	1.643	75.62
50	0.5	4.97	2.485	3.156	78.74
75	0.75	4.97	3.728	4.72	78.97
100	1	4.98	4.980	6.4	77.81
Average efficiency					77.79

Table 5. Efficiency at 230 V_{AC}

Load [%]	I_{OUT} [A]	V_{OUT} [V]	P_{OUT} [W]	P_{IN} [W]	Efficiency [%]
25	0.25	4.98	1.245	1.88	66.22
50	0.5	4.97	2.485	3.349	74.18
75	0.75	4.98	3.735	4.838	77.22
100	1	4.99	4.99	6.326	78.88
Average efficiency					74.12

Figure 9. Efficiency vs. output power



This adapter complies with the new EPA 2.0 standard for low voltage devices (V_{OUT} < 6, I_{OUT} > 0.55 A). The minimum required efficiency for a 5 W SMPS is 68.2%. This value should be calculated as the average of the efficiency at 25%, 50%, 75% and 100% of the rated load.

The input power without load has also been measured and as indicated in *Table 6*, for both 115 V_{AC} and 230 V_{AC}.

The proposed adapter using the ALTAIR05T-800 meets the most restrictive worldwide standards for efficiency and power consumption at no-load (European Code of Conduct, adapter for mobile handheld battery-driven applications, starting from 1st January 2011: < 150 mW).

Table 6. Standby consumption

V_{IN} [V]	P_{IN} [mW]
115 V_{AC}	54 mW
230 V_{AC}	75 mW

3.1 Standby optimization: tips for reducing standby consumption

When light loaded or in no-load condition, most of the losses are switching losses, which are almost proportional to the switching frequency. It should be considered that even if no external load is connected to the power supply, some power needs to be processed in order to sustain the operation of the ALTAIR05T-800 and some is also dissipated on the bleeder resistor at the secondary side.

Basically, when the converter switches to burst mode operation, the lower the load, the lower the average switching frequency. So, the burst mode operation of the ALTAIR05T-800

significantly reduces the average switching frequency of the converter, when light loaded or completely no-loaded.

As the output voltage is sensed through the auxiliary winding just at the end of the secondary demagnetization, rendering the IC is blind to the output voltage between one switching cycle and the next, the switching frequency cannot be reduced below the minimum restart time, $T_{RESTART}$, fixed at 500 µs (typical value).

Let's calculate the minimum input power consumption when the IC works at minimum restart frequency:

Equation 1

$$P_{IN(MIN)} = \frac{1}{2} \times L_P \times \left(\frac{V_{SENSE_M}}{R_{SENSE}} \right)^2 \times \frac{1}{T_{RESTART}}$$

where (V_{SENSE_M}/R_{SENSE}) is the peak drain current during burst mode (V_{SENSE_M} = 140 mV internally defined).

Neglecting the losses through the input bridge rectifier, the input capacitor leakage current losses and the conduction losses, the primary side losses can be calculated as follows:

Equation 2

$$P_{PRI} = P_{BIAS} + P_{SW} + P_{SNUBBER}$$

where $P_{BIAS} = V_{CC} \times I_Q$ is the consumption of the IC (the quiescent current, I_Q, is 1 mA typical value), P_{SW} represents the switching losses and $P_{SNUBBER}$ are the losses through the RCD snubber connected to the drain.

If $P_{IN(MIN)} > P_{PRI}$, the residual energy is transferred to the secondary side and it must be dissipated through a dummy load in order to avoid an increase in the output voltage. In this case, the bleeder resistor can be calculated as following:

Equation 3

$$R_{BLEEDER} \leq \frac{V_{OUT}^2}{\left[\frac{1}{2} \times L_P \times \left(\frac{V_{SENSE_M}}{R_{SENSE}} \right)^2 \times \frac{1}{T_{RESTART}} \right] - P_{PRI}}$$

However, if $P_{IN(MIN)} = P_{PRI}$ the dummy load can be removed.

Since most of the time P_{PRI} is lower than $P_{IN(MIN)}$, the above consideration shows that input power reduction can be achieved by reducing *Equation 1* so that the $R_{BLEDEER}$ can be increased in accordance with *Equation 3*.

Design optimization

The sense resistor R_{SENSE} sets the constant current value together with transformer's primary-to-secondary turn ratio (see *Section A.2*), but also defines the minimum input power consumption according to *Equation 4*.

A proper design can help reduce the energy per switching cycle transferred to the secondary and, consequently, no-load consumption. This can be done by increasing R_{SENSE} as much as possible and consequently, increasing the transformer's reflected voltage, in order to achieve the CC setpoint according to *Equation 4*. Other design considerations should be taken into account in designing the transformer.

For the purpose of reducing the switching losses, some consideration should also be given to the transformer. The primary parasitic capacitance causes switch-on losses as it is fast-charged each time the MOSFET is turned on and the charging current dissipates energy within the MOSFET itself. Reducing this capacitance as low as possible, this type of loss is minimized.

With reference to *Equation 1*, it is clear that a reduction of the $P_{IN(MIN)}$ can be achieved by reducing, as much as possible, the primary inductance of the transformer (L_P), (according to other design considerations also).

In this case the energy per cycle sent to the secondary side is reduced, which means that the bleeder resistor value increases, thus reducing the dissipation of the dummy load.

3.2 Five star charger energy rating

To help save energy, in November 2008 the world's five largest mobile phone makers announced their own five star energy rating system to help consumers more easily identify the most energy-efficient chargers.

The new rating system shows how much energy each charger uses when left plugged in. Chargers are labeled with ratings from five stars for the most efficient chargers (≤0.03 W), to zero stars for those using the most energy in no-load mode (> 0.5 W).

Figure 10. No-load consumption score chart

As shown in *Table 6*, the charger presented here meets the "**four star rating**".

By optimizing the design, based on suggestions provided in *Section 3.1*, the input power consumption can be reduced. Also, if a higher output voltage in no-load can be accepted, the bleeder resistor value can be increased a bit more than the minimum value in *Equation 3*, thus achieving a further reduction in no-load consumption and helping to meet the "**five star rating**".

4 Typical board waveforms

Drain voltage and current waveforms were reported for the two nominal input voltages and for the minimum and the maximum voltage of the converter input operating range. *Figure 11* shows the drain current and the drain voltage waveforms at nominal input voltages and full load.

In order to simulate this mode of operation, the electronic load has been set in CV mode at 3 V, so that this voltage is imposed on the charger's output from the E-load: the charger is forced to enter CC mode, thus regulating the output current at its nominal value. *Figure 12* shows the typical waveforms during CC mode.

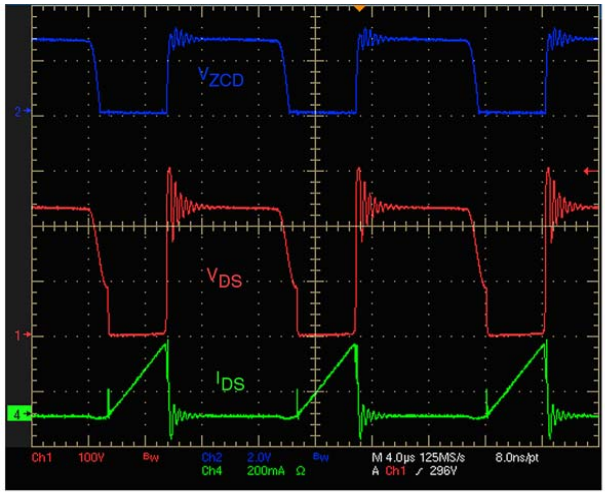
The CC mode loop is able to regulate even when the output voltage falls to zero, thanks to the self-supply capability of the IC. This is especially important when the output connector is shorted. In this case, the current is still maintained close to the nominal value, thus eliminating hiccup mode and reducing the secondary peak current.

Moreover, the CC mode technique eliminates the need for overload protection. In fact, maximum output power is achieved on the corner point between CV mode and CC mode, and coincides with the full load condition. *Figure 13* shows the typical waveforms during short-circuit at nominal input voltage.

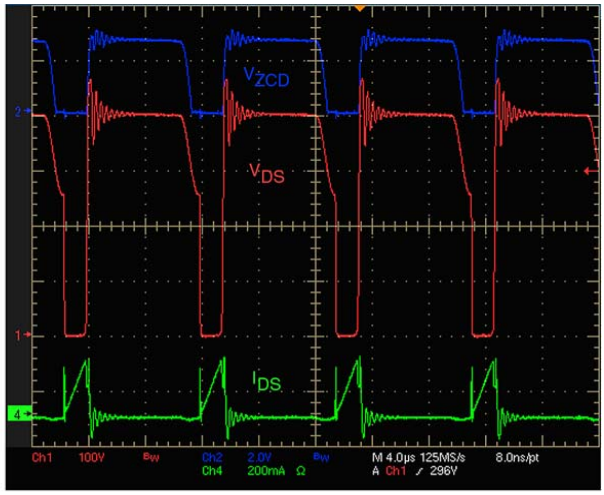
As described in *Section 3*, at low load the OC enters in burst mode, reducing the switching frequency down to a minimum fixed value: *Figure 14* shows the typical waveforms during no-load conditions at both 115 V_{AC} and 230 V_{AC} circuit at nominal input voltage.

Figure 15 and *Figure 16* show the charger startup in both no-load and full load conditions and nominal input voltage: the maximum drain-source voltage is well below the BV_{DSS} of the IC and the output voltage overshoot is always below 5.3 V.

Figure 11. Normal operation at full load, at 115 V_{AC} and 230 V_{AC}

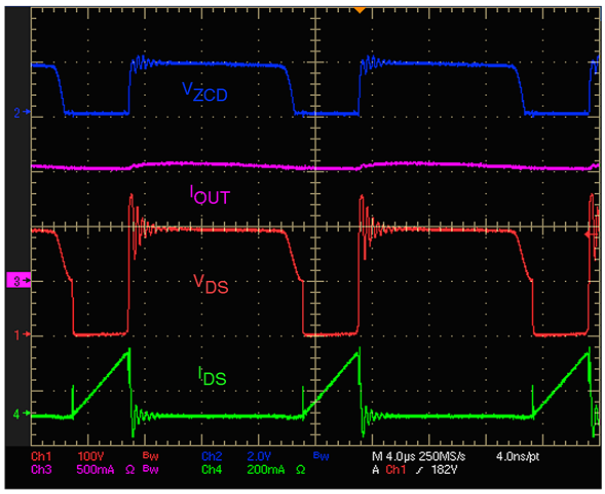


Ch1 (max.): 302.8 V
Ch1 (freq.): 75 kHz
Ch4 (max.): 269.6 mA
M: 4.0 µs / div.

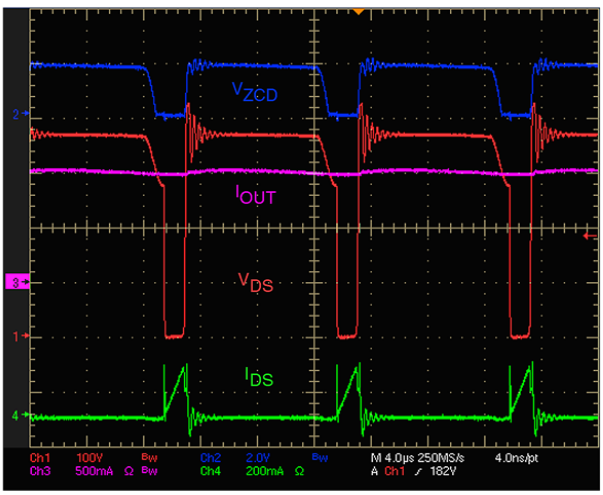


Ch1 (max.): 463.2 V
Ch1 (freq.): 104.3 kHz
Ch4 (max.): 206.4 mA
M: 4.0 µs / div.

Figure 12. Normal operation in CC mode with V_{OUT} = 3 V, at 115 V_{AC} and 230 V_{AC}

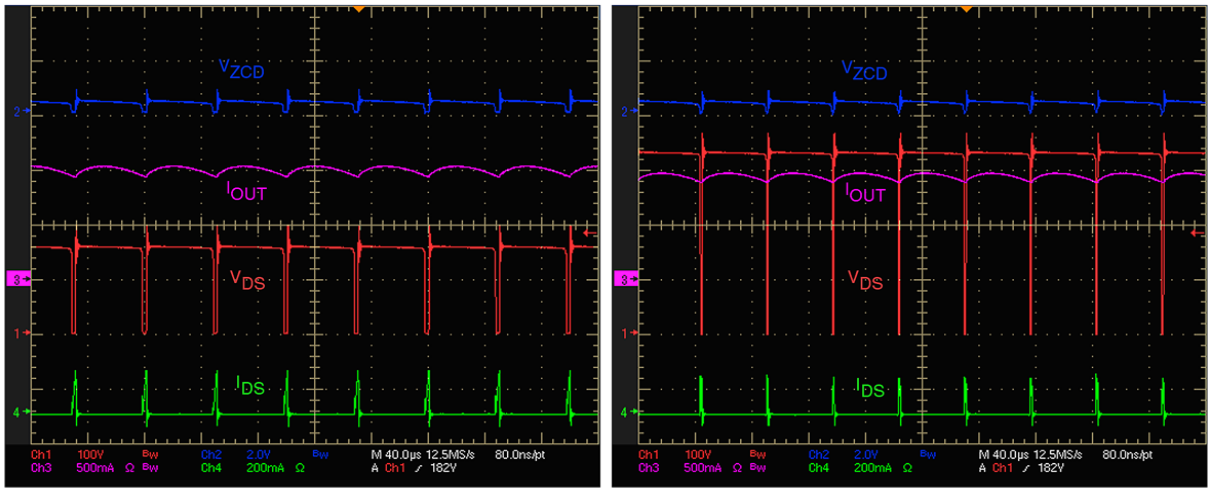


Ch1 (max.): 255.2 V
Ch1 (freq.): 61.79 kHz
Ch3 (mean): 1.04 A
Ch3 (Pk-Pk): 80 mA
Ch4 (max.): 238.4 mA
M: 4.0 µs / div.



Ch1 (max.): 424.8 V
Ch1 (freq.): 82.28 kHz
Ch3 (mean): 1.002 A
Ch3 (Pk-Pk): 72 mA
Ch4 (max.): 192.0 mA
M: 4.0 µs / div.

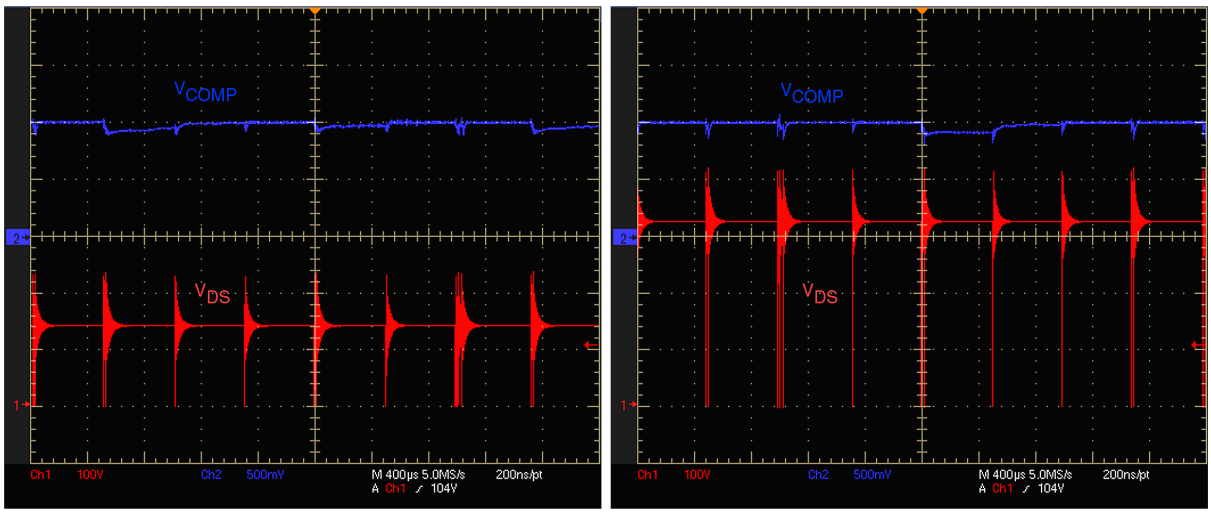
Figure 13. Short-circuit at 115 V_{AC} and 230 V_{AC}



Ch1 (max.): 195.6 V
Ch1 (freq.): 20.08 kHz
Ch3 (mean): 996.4 mA
Ch3 (Pk-Pk): 105.2 mA
Ch4 (max.): 149.9 mA
M: 40.0 µs / div.

Ch1 (max.): 364.8 V
Ch1 (freq.): 21.5 kHz
Ch3 (mean): 938.6 mA
Ch3 (Pk-Pk): 91.95 mA
Ch4 (max.): 134.2 mA
M: 40.0 µs / div.

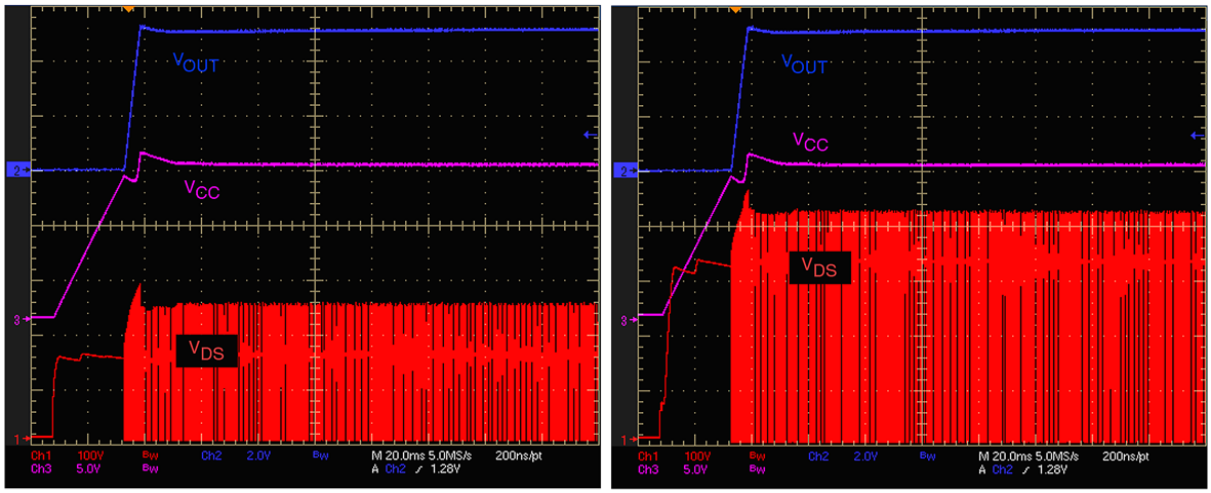
Figure 14. Normal operation at no-load, at 115 V_{AC} and 230 V_{AC}



Ch1 (freq.): 2.08 kHz
Ch2 (max.): 1.05 V
Ch2 (min.): 896 mV
M: 400.0 µs / div.

Ch1 (freq.): 2.08 kHz
Ch2 (max.) (blue): 1.08 V
Ch2 (min.) (blue): 892 mV
M: 400.0 µs / div.

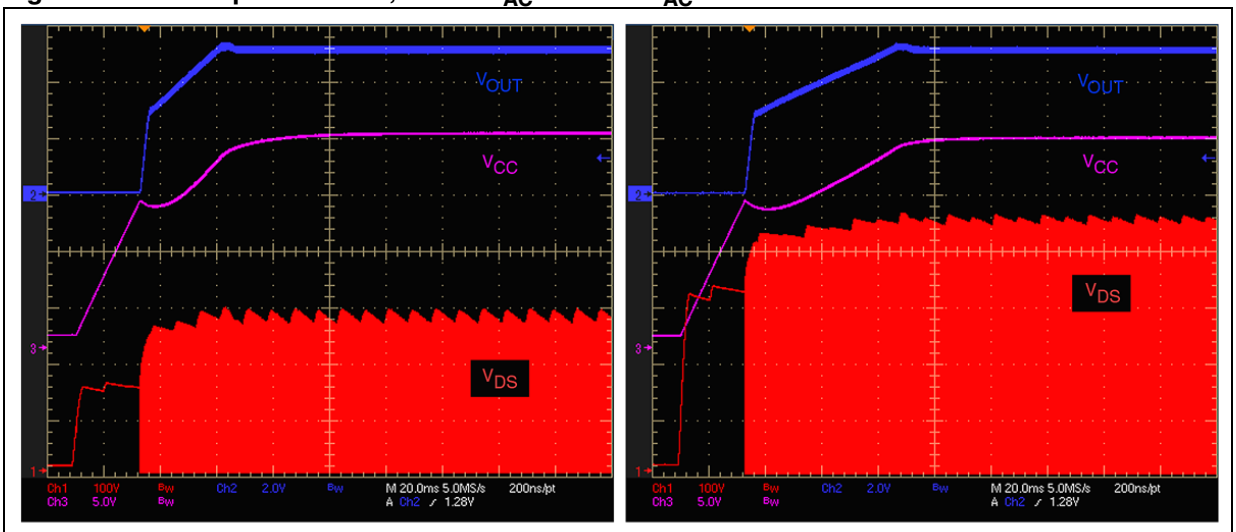
Figure 15. Startup at no-load, at 115 V_{AC} and 230 V_{AC}



Ch1 (max.): 282 V
Ch2 (max.): 5.28 V
Ch3 (mean): 14.2 V
M: 20.0 ms / div.

Ch1 (max.): 454 V
Ch2 (max.): 5.27 V
Ch3 (mean): 14.4 V
M: 20.0 ms / div.

Figure 16. Startup at full load, at 115 V_{AC} and 230 V_{AC}



Ch1 (max.): 290 V
Ch2 (max.): 5.29 V
Ch3 (mean): 18.1 V
M: 20.0 ms / div.

Ch1 (max.): 458 V
Ch2 (max.): 5.28 V
Ch3 (mean): 18.2 V
M: 20.0 ms / div.

5 V-I output characteristics and cable drop compensation

Figure 17 and *Figure 18* show the V-I output characteristics at the PCB output connector, measured at 115 V_{AC} and 230 V_{AC} mains input voltage.

Thanks to the self-supply of the ALTAIR05T-800, the output current can be regulated even with an output voltage close to zero.

The IC is also equipped with a cable compensation function that compensates the output voltage drop when a long cable is used, so ideally zero-load regulation can be achieved even at the end of the cable.

Figure 19 shows the load regulation in CV mode when the CDC function is not used: the voltage is tightly regulated at the end of the PCB connector, whereas at the end of the cable it decreases proportionally to the output current.

Conversely, in *Figure 20* the effect of the cable drop compensation is shown. The CV setpoint is increased proportionally to the output current, in order to compensate the voltage drop across the cable and maintaining the regulation at the end of the cable almost constant.

Figure 17. Output characteristic at 115 V_{AC}

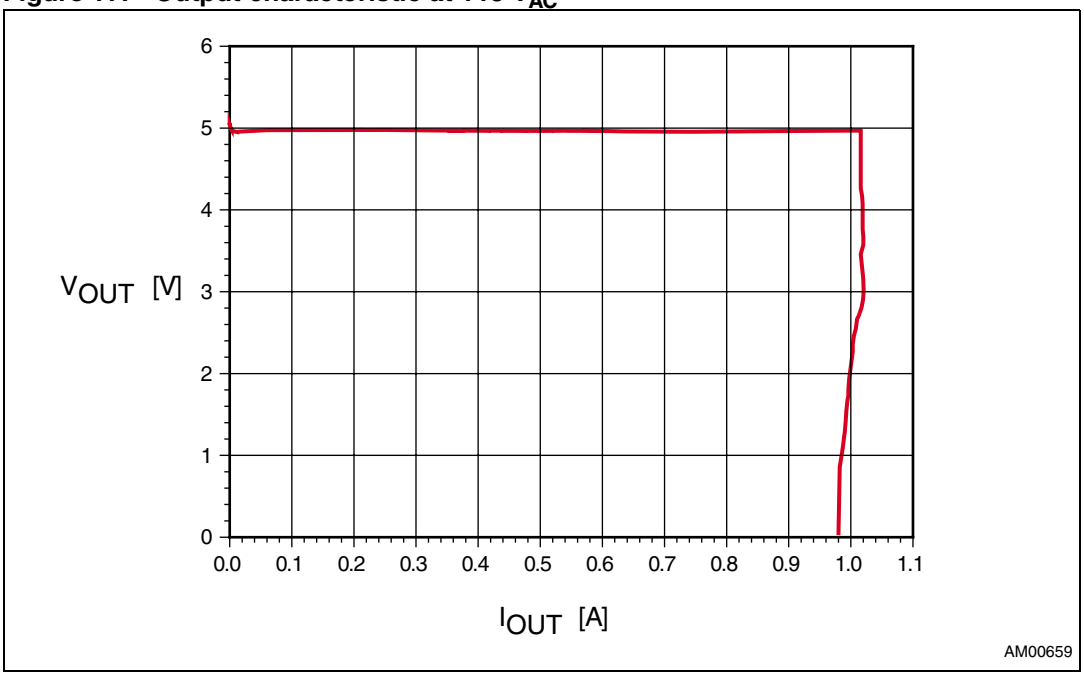


Figure 18. Output characteristic at 230 V_{AC}

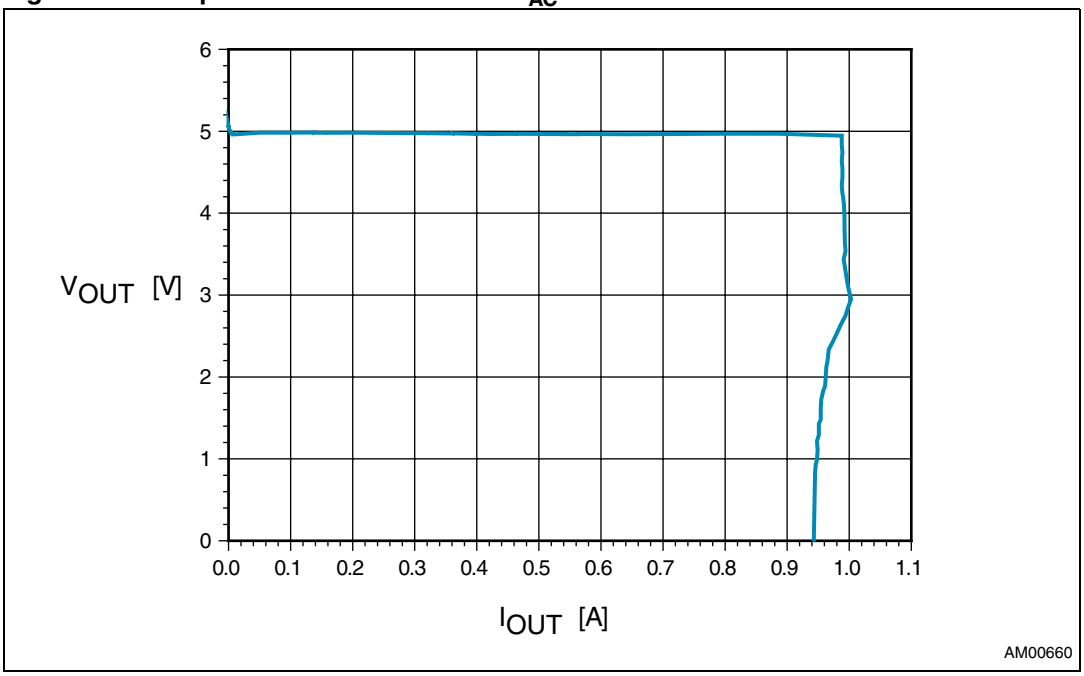


Figure 19. Output characteristic without cable drop compensation: R_{CABLE} = 0.32 Ω and R_5 = 10 kΩ

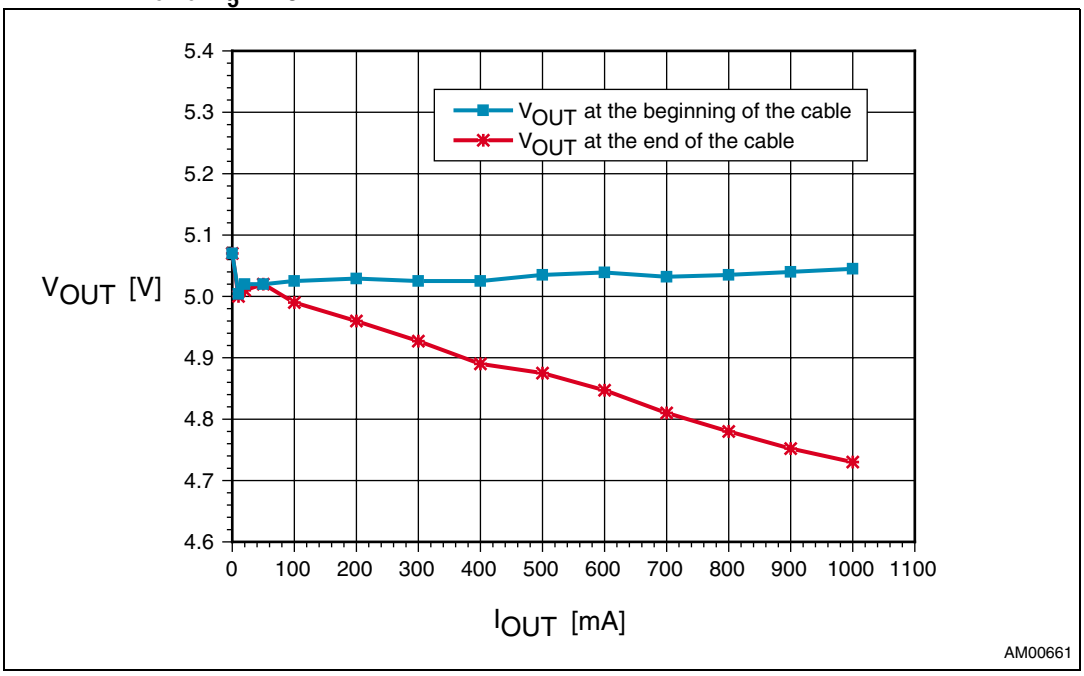
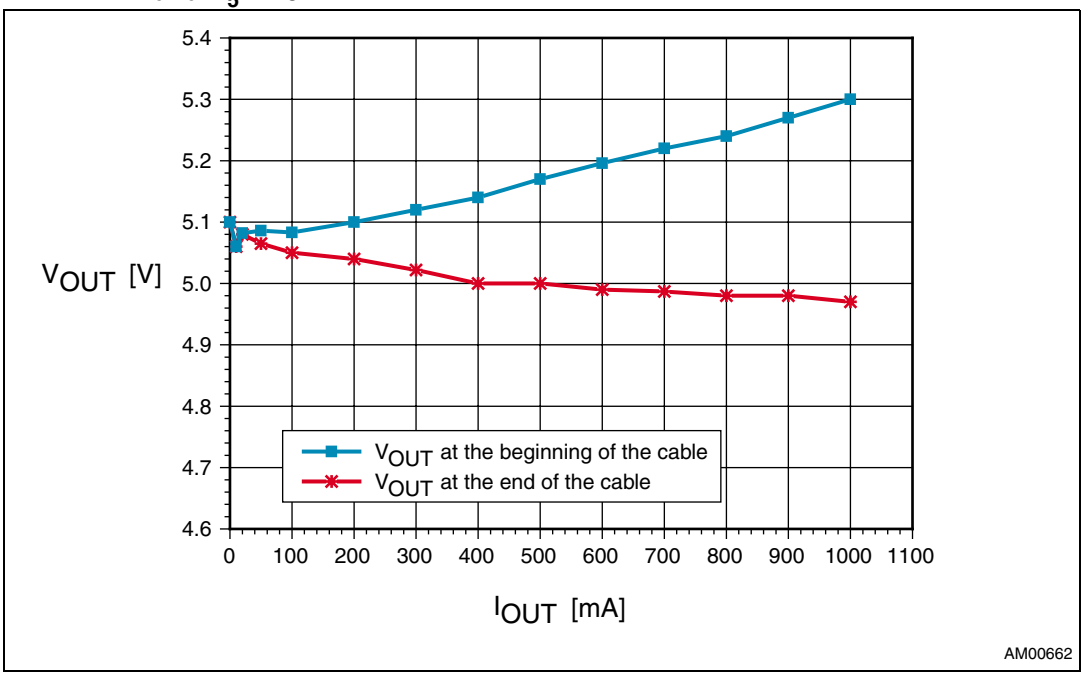


Figure 20. Output characteristic with cable drop compensation: R_{CABLE} = 0.32 Ω and R_5 = 10 kΩ



6 Conclusion

A 5 W CV-CC optoless adapter demonstration board using the ALTAIR05T-800 device was presented and the results show that very good performance can be obtained using this new device.

The unique “all-primary sensing” feedback for both constant voltage and constant current eliminates the need for the optocoupler, the secondary voltage reference, as well as the current sensor, making the IC suitable for AC-DC chargers for mobile phones and other portable equipment, as well as any adapter requiring tight tolerance from both CV and CC regulation.

The ALTAIR05T-800 is capable of meeting the most restrictive worldwide standards for efficiency and power consumption at no-load.

The embedded protection features of this new device and the 800 V power section considerably increase the safety and reliability of the end product.

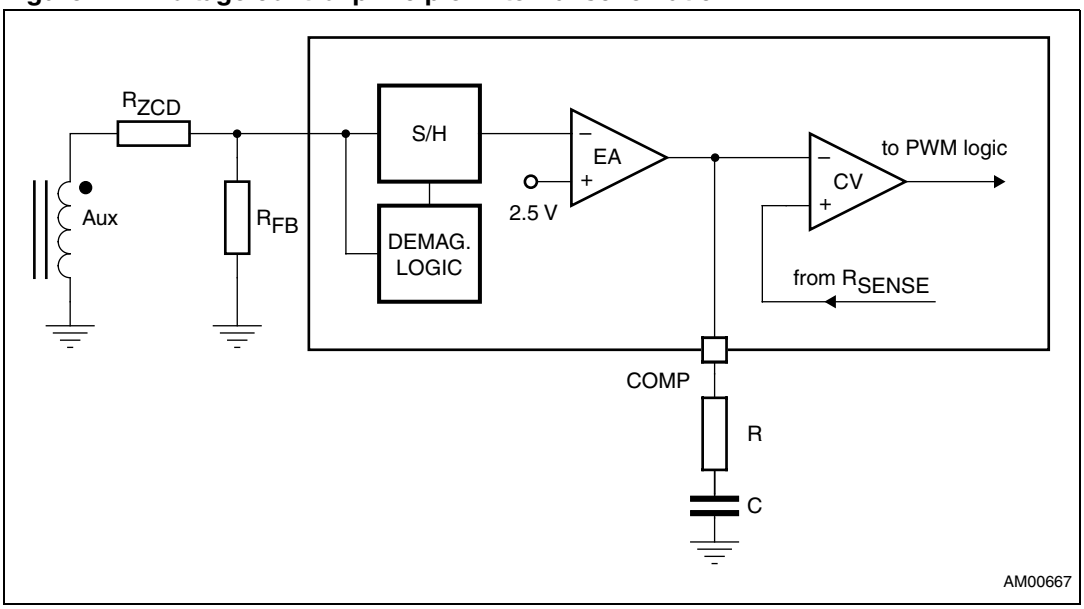
Appendix A Modes of operation

A.1 Constant voltage operation

The IC is specifically designed to work in primary regulation and the output voltage is sensed through a voltage partition of the auxiliary winding, just before the auxiliary rectifier diode.

Figure 21 shows the internal schematic of the constant voltage mode and the external connections.

Figure 21. Voltage control principle: internal schematic



In order to achieve a tight output regulation, the signal on the ZCD/FB pin is sampled and held at the end of the transformer demagnetization to obtain an accurate image of the output voltage, and it is compared with the error amplifier internal reference.

The internal error amplifier delivers an output current proportional to the voltage imbalance of the two outputs: the output generates the control voltage that is compared with the voltage across the sense resistor, thus modulating the cycle-by-cycle peak drain current.

The output voltage can be set by choosing R_{FB} according to *Equation 4*:

Equation 4

$$R_{FB} = \frac{V_{REF}}{\frac{n_{AUX}}{n_{SEC}} \times V_{OUT} - V_{REF}} \times R_{ZCD}$$

Where n_{SEC} and n_{AUX} are the secondary and auxiliary number of turns, respectively.

The R_{ZCD} value can be defined based on the application parameters and can be calculated according to *Equation 6*.

A.2 Constant current operation

Figure 22 presents the principle used for controlling the average output current of the flyback converter.

The output voltage of an auxiliary winding is used by a demagnetization block to generate the control signal for the MOSFET switch Q1. A resistor (R) in series with it absorbs the current V_C/R, where V_C is the voltage developed by capacitor C_{REF}.

The flip-flop's output is high, as long as the transformer delivers current on the secondary side (*Figure 23*).

If the value of the capacitor (C) is sufficiently high to consider the voltage V_C as constant, and the system works in DCM (this is the case because the IC is in QR mode), it is possible to obtain the equation:

Equation 5

$$I_{OUT} = \frac{n}{2} \times \frac{V_{CREF}}{R_{SENSE}}$$

Where *n* is the primary-to-secondary turn ratio and $V_{CREF} = I_{REF} \times R$.

Equation 5 shows that the average output current no longer depends on input or output voltage, nor on the transformer inductance values. The parameters defining the output current are the transformer ratio n and the sense resistor R_{SENSE}, while the current reference voltage V_{CREF} (equal to $I_{REF} \times R$) is internally defined.

Figure 22. Current control principle

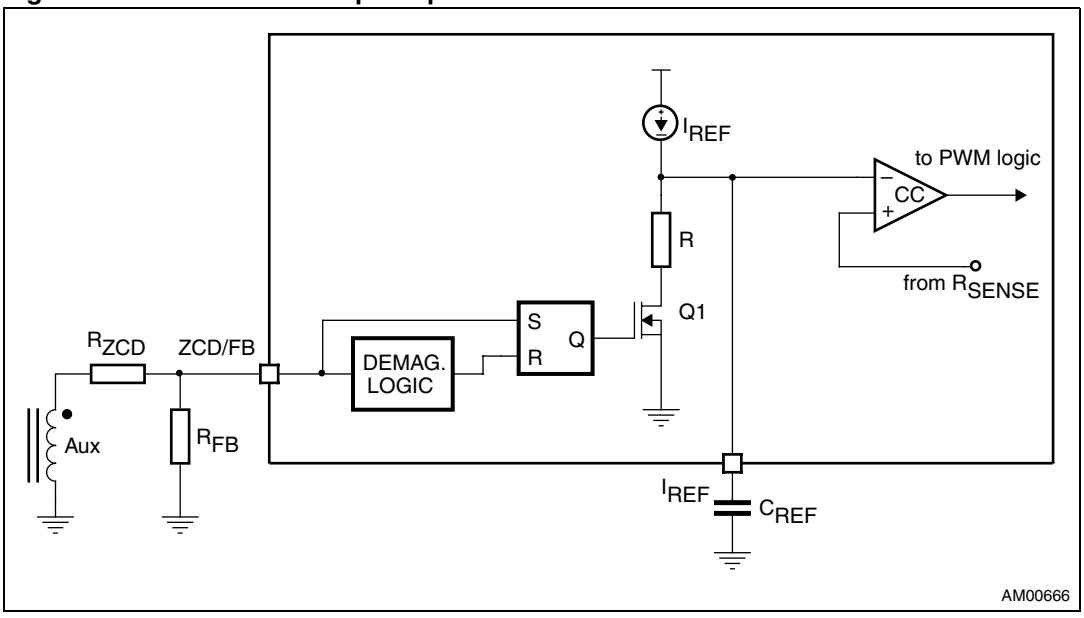
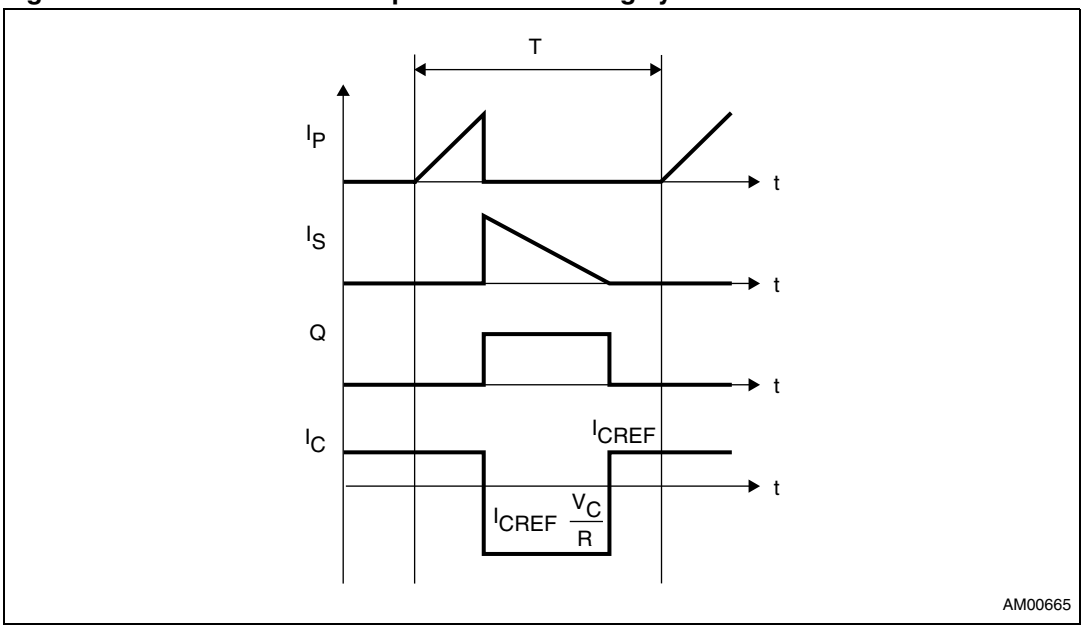


Figure 23. Constant current operation: switching cycle waveforms



A.3 Current comparator speed

The propagation delay of the internal current comparator used in the CC control block causes the MOSFET to be switched off with a peak current higher than the theoretical value: this current overshoot is dependent on the input voltage and introduces an error in the calculated CC setpoint, rendering *Equation 5* no longer valid.

In order to make the cycle-by-cycle current limitation and the CC setpoint almost independent of the input voltage, a feed-forward function has been implemented, according the schematic in *Figure 24*.

During the MOSFET's ON-time, the current sourced from the ZCD/FB pin is mirrored inside the “feed-forward logic” block to provide the feed-forward current, I_{FF}.

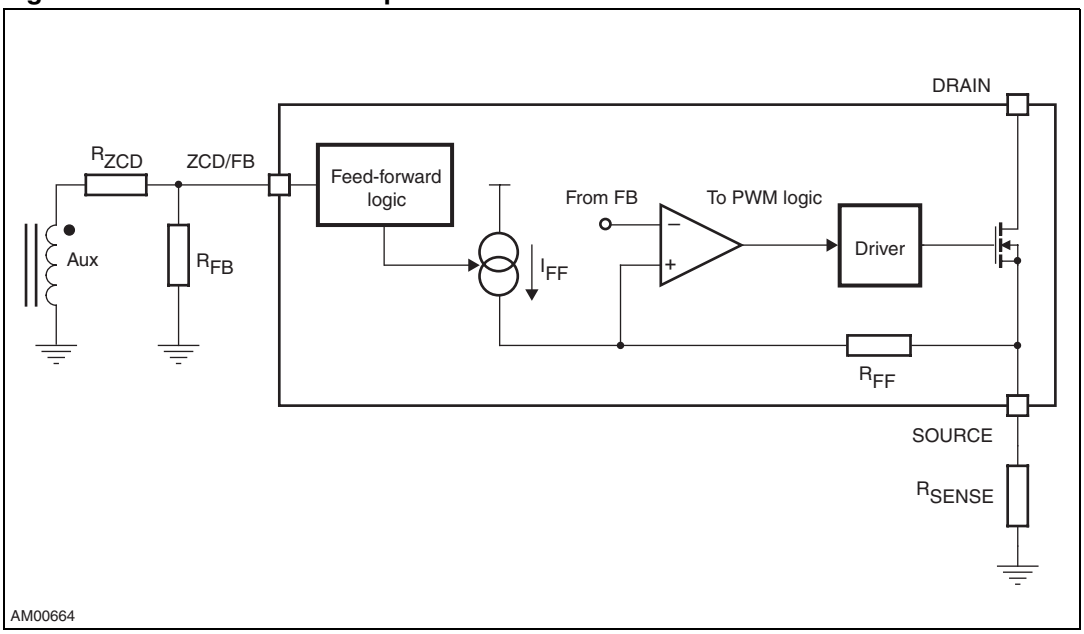
This feed-forward current is proportional to the input voltage and provides an offset on the current sense to compensate the propagation delay of the current comparator.

In order to achieve full compensation, the R_{ZCD} resistor should be selected based on the following equation:

Equation 6

$$R_{ZCD} = \frac{n_{AUX}}{n_{PRI}} \times \frac{L_P \times R_{FF}}{T_d \times R_{SENSE}}$$

Figure 24. Feed-forward compensation: internal schematic



A.4 Cable drop compensation block

The cable drop compensation (CDC) function is used to compensate the voltage drop across an output cable. In fact, the voltage on the end of the cable is lower than that at the beginning, depending on the output current level. This voltage drop may not be acceptable, especially in applications where tight voltage regulation is required and a long output cable is used.

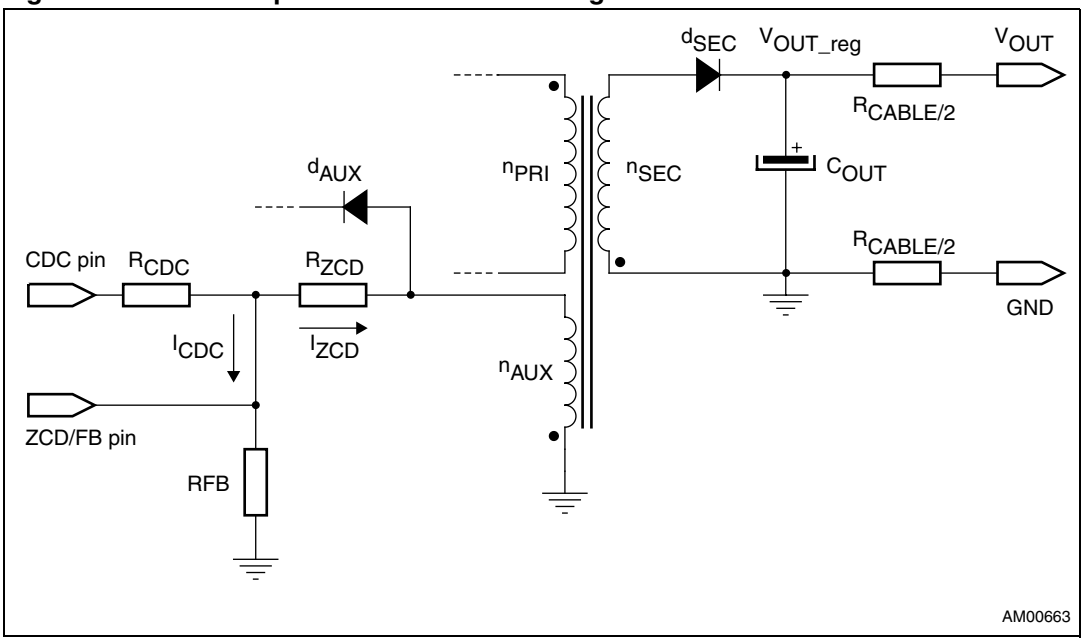
The CDC is a voltage source which provides, during constant voltage mode regulation, a voltage on the CDC pin lower than 2.5 V by an amount proportional to the output current.

According to *Figure 25*, by connecting an appropriate resistor between this pin and the ZCD/FB pin, the CV setpoint is increased proportionally to I_{OUT}, so that the output at the end of the cable is almost constant. The R_{CDC} value can be calculated using *Equation 7*:

Equation 7

$$R_{CDC} = \frac{2}{n} \times \frac{n_{SEC}}{n_{AUX}} \times \frac{R_{SENSE} \times R_{ZCD}}{R_{CABLE}}$$

Figure 25. CDC compensation: external configuration



In *Equation 7*, R_{CABLE} is the total resistance of the output cable.

The CDC block acts as a second-order correction and creates a positive feedback that can impact overall system stability. To avoid any issues that could render the loop unstable, the CV setpoint time response must be much lower than the main control signal. For this reason, the CDC block is designed with a time response of a few tens of milliseconds.

Revision history

Table 7. Document revision history

Date	Revision	Changes
11-Jan-2011	1	Initial release.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2011 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com