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Z-turn Lite

- ➢ *667MHz Xilinx XC7Z007S or XC7Z010 ARM Cortex-A9 Processor with Xilinx 7-series FPGA logic*
- ➢ *512MB DDR3 SDRAM (2 x 256MB, 32-bit), 4GB eMMC Flash, 16MB QSPI Flash*
- ➢ *Micro USB2.0 OTG, 1 x 10/100/1000M Ethernet, TF, Debug UART, JTAG...*
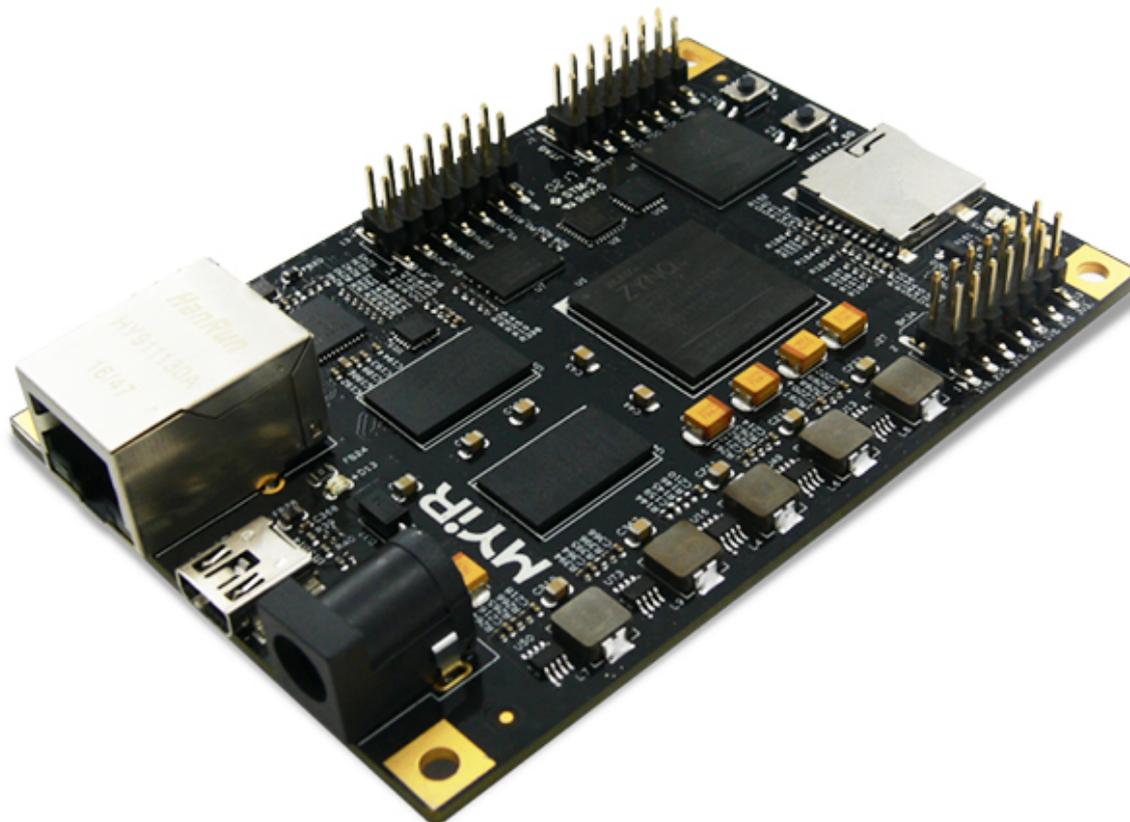- ➢ *Ready-to-Run Linux Single Board Computer*

Figure 1-1 Z-turn Lite

The **Z-turn Lite** is an ultra-cost-effective lite version of MYIR's **Z-turn board**. It is built around 667MHz Xilinx **Zynq-7007S** SoC which is among the new Zynq Z-7000S family with a Single-core **ARM Cortex-A9** processor and integrated Artix-7 Field Programmable Gate Array (**FPGA**) logic. The **Zynq-7010** Dual-core **ARM Cortex-A9** MPCore processor can also be compatible to be used on this board. It is a minimal and compact system of **Xilinx Z-7007S** or **Z-7010** SoC and provides numerous pending configuration of PL resources. It is an excellent reference design and evaluation board for development based on **Xilinx Zynq-7000** series SoCs.

The **Z-turn Lite** takes full features of the **Zynq Z-7007S** or **Z-7010** all programmable SoC.   It is equipped with **512MB DDR3**, **4GB eMMC Flash**, **16MB QSPI Flash** and a set of peripherals including **Micro USB OTG, 10/100/1000Mbps Ethernet**, **TF**, **JTAG**, **Debug UART**, etc. Additionally, there is one **120 position connector socket** on the rear of the board to bring out as many as IO signals for user extensions.

The **Z-turn Lite** is capable of running Linux operating system and provided with **Linux 3.15.0** SDK, the kernel and many drivers are in source code. The **Z-turn Lite Kit** is delivered with complete accessories including one micro USB cable, one Ethernet cable, one 4GB TF card, one USB-to-UART cable, one 5V power adapter and product disk which enables you to start the development quickly when getting the board out-of-the-box.

Hardware Specification

The **Zynq®-7000 All Programmable SoC** (AP SoC) family integrates the software programmability of an ARM®-based processor with the hardware programmability of an FPGA, enabling key analytics and hardware acceleration while integrating CPU, DSP, ASSP, and mixed signal functionality on a single device. Consisting of single-core Zynq-7000S and dual-core Zynq-7000 devices, the Zynq-7000 family is the best price to performance-per-watt, fully scalable SoC platform for your unique application requirements.

Zynq-7000S

Zynq-7000S devices feature a single-core ARM Cortex™-A9 processor mated with 28nm Artix®-7 based programmable logic, representing the lowest cost entry point to the scalable Zynq-7000 platform. It includes Zynq Z-7007S, Z-7012S and Z-7014S which target smaller embedded designs. Available with 6.25Gb/s transceivers and outfitted with commonly used hardened peripherals, the Zynq-7000S delivers cost-optimized system integration ideal for industrial IoT applications such as motor control and embedded vision.
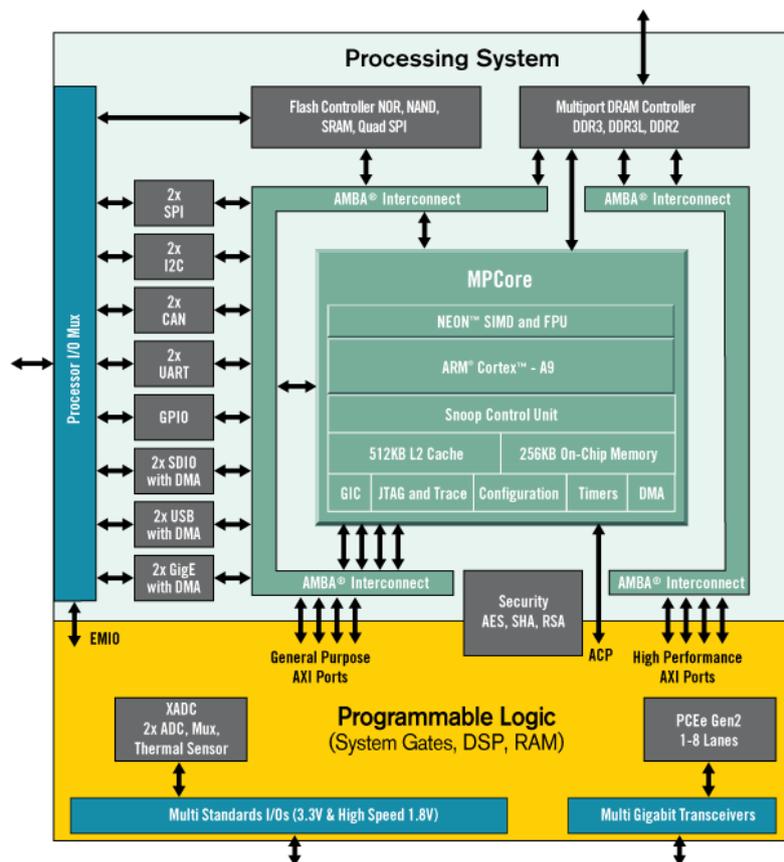

Figure 1-2 Zynq Z-7000S SoC Device Block Diagram

Zynq-7000

Zynq-7000 devices are equipped with dual-core ARM Cortex-A9 processors integrated with 28nm Artix-7 or Kintex®-7 based programmable logic for excellent performance-per-watt and maximum design flexibility. With up to 6.6M logic cells and offered with transceivers ranging from 6.25Gb/s to 12.5Gb/s, Zynq-7000 devices enable highly differentiated designs for a wide range of embedded applications including multi-camera drivers assistance systems and 4K2K Ultra-HDTV.
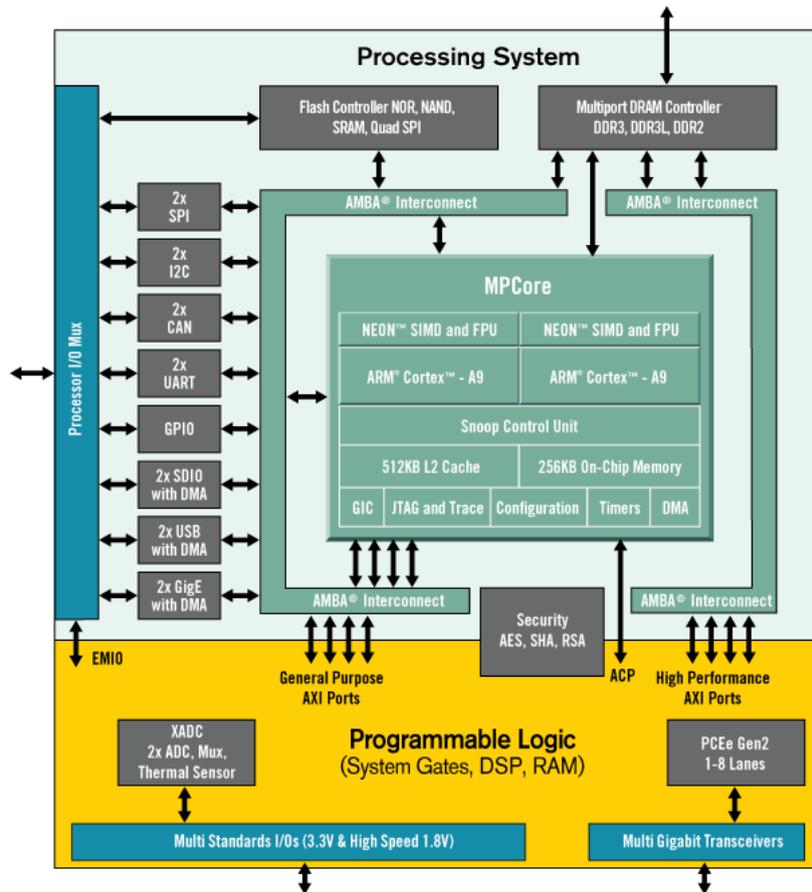

Figure 1-3 Zynq Z-7000 SoC Device Block Diagram

Zynq®-7000 All Programmable SoC Family

		Cost-Optimized Devices						Mid-Range Devices			
	Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Processing System (PS)	Processor Core	Single-Core ARM® Cortex™-A9 MPCore™ Up to 766MHz			Dual-Core ARM Cortex-A9 MPCore Up to 866MHz			Dual-Core ARM Cortex-A9 MPCore Up to 1GHz[1]			
	Processor Extensions	NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per processor									
	L1 Cache	32KB Instruction, 32KB Data per processor									
	L2 Cache	512KB									
	On-Chip Memory	256KB									
	External Memory Support[2]	DDR3, DDR3L, DDR2, LPDDR2									
	External Static Memory Support[2]	2x Quad-SPI, NAND, NOR									
	DMA Channels	8 (4 dedicated to PL)									
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO									
	Peripherals w/ built-in DMA[2]	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO									
	Security[3]	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot									
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts									
Programmable Logic (PL)	7 Series PL Equivalent	Artix®-7	Artix-7	Artix-7	Artix-7	Artix-7	Artix-7	Kintex®-7	Kintex-7	Kintex-7	Kintex-7
	Logic Cells	23K	55K	65K	28K	74K	85K	125K	275K	350K	444K
	Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Total Block RAM	1.8Mb	2.5Mb	3.8Mb	2.1Mb	3.3Mb	4.9Mb	9.3Mb	17.6Mb	19.1Mb	26.5Mb
	(# 36Kb Blocks)	(50)	(72)	(107)	(60)	(95)	(140)	(265)	(500)	(545)	(755)
	DSP Slices	66	120	170	80	160	220	400	900	900	2,020
	PCI Express®	—	Gen2 x4	—	—	Gen2 x4	—	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC[2]	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs									
	Security[3]	AES & SHA 256b Decryption & Authentication for Secure Programmable Logic Config									
Speed Grades	Commercial	-1			-1			-1			-1
	Extended	-2			-2,-3			-2,-3			-2
	Industrial	-1, -2			-1, -2, -1L			-1, -2, -2L			-1, -2, -2L

Notes:
1. 1 GHz processor frequency is available only for -3 speed grades for devices in flip-chip packages. See DS190, *Zynq-7000 All Programmable SoC Overview* for details.
2. Z-7007S and Z-7010 in CLG225 have restrictions on PS peripherals, memory interfaces, and I/Os. Please refer to UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual* for more details.
3. Security block is shared by the Processing System and the Programmable Logic.

Figure 1-4 Zynq *Z-7000 and Z-7000S SoC Device Table*

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The Z-turn Lite is based on the Xilinx Zynq-7007S or Zynq-7010 SoC and the hardware specification is listed in following table1-1:

Item	Features
SoC	Xilinx XC7Z007S-1CLG400C (Zynq-7007S) or XC7Z010-1CLG400C (Zynq-7010) - ARM® Cortex™-A9 MPCore processor 667MHz single-core processor (up to 766MHz, for XC7Z007S) 667MHz dual-core processor (up to 866MHz, for XC7Z010) - Integrated Artix-7 class FPGA subsystem with 23K logic cells, 14,400 LUTs, 66DSP slices (for XC7Z007S) with 28K logic cells, 17,600 LUTs, 80 DSP slices (for XC7Z010) - NEON™ & Single / Double Precision Floating Point for each processor - Supports a Variety of Static and Dynamic Memory Interfaces
Memory	512MB DDR3 SDRAM (2 x 256MB, 32-bit)
Storage	4GB eMMC Flash 16MB QSPI Flash TF card interface
Communications	1 x 10/100/1000M Ethernet 1 x Micro USB2.0 OTG
Input and Output	1 x 2.54mm pitch 14-pin JTAG interface 1 x 0.5mm pitch 120 Position Connector Socket for Expansion interface 1 x 2.54mm pitch 4-pin Debug UART interface
Others	2 x Buttons (1x Reset, 1 x User) 5 x LEDs - 1 x User LED - 1 x FPGA configuration indicator - 1 x FPGA initialization indicator - 1 x Power indicator - 1 x USB overcurrent indicator
Dimensions	91mm x 63mm (10-layer PCB design)
Power supply	DC 5V/2A
Temp.	0~70 Celsius
Power consumption	8W

Table 1-1 Z-turn Lite Hardware Specification

MYIR TECH LIMITED
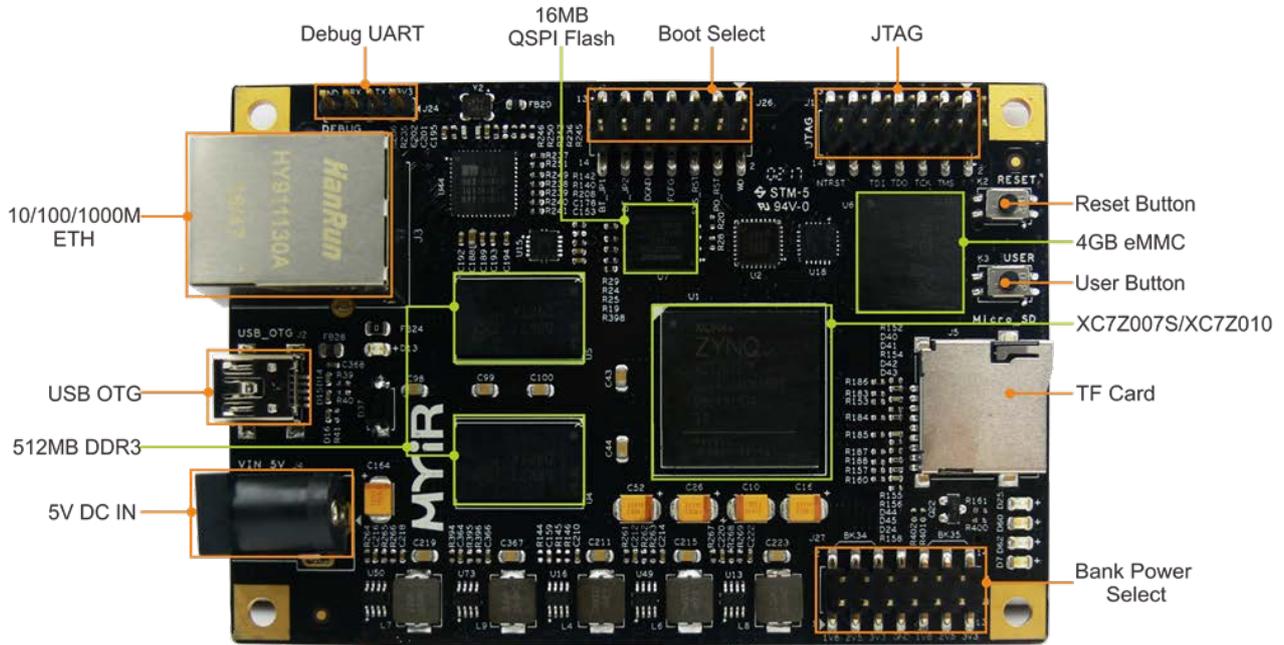
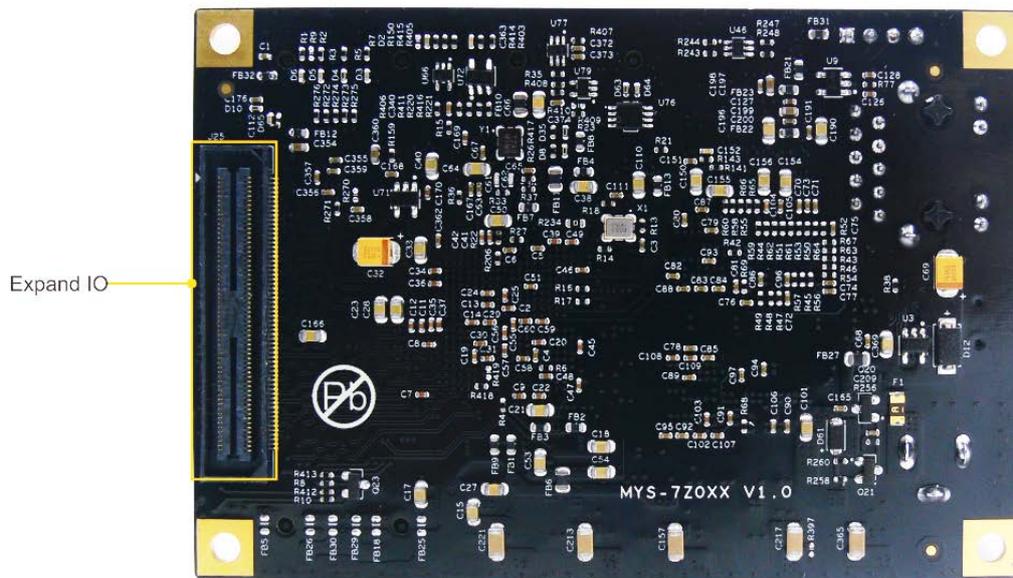www.myirtech.com

Figure 1-3 Z-turn Lite (Top-view)
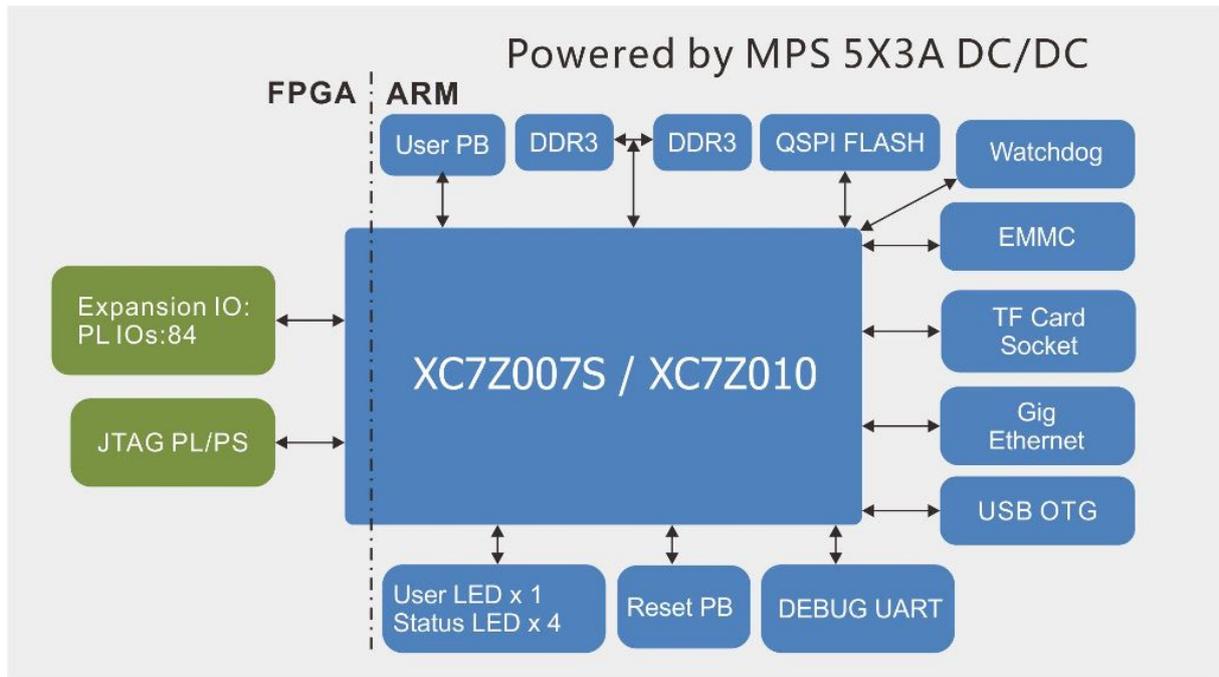

Figure 1-4 Z-turn Lite (Bottom-view)

Figure 1-5 Z-turn Lite Function Block Diagram

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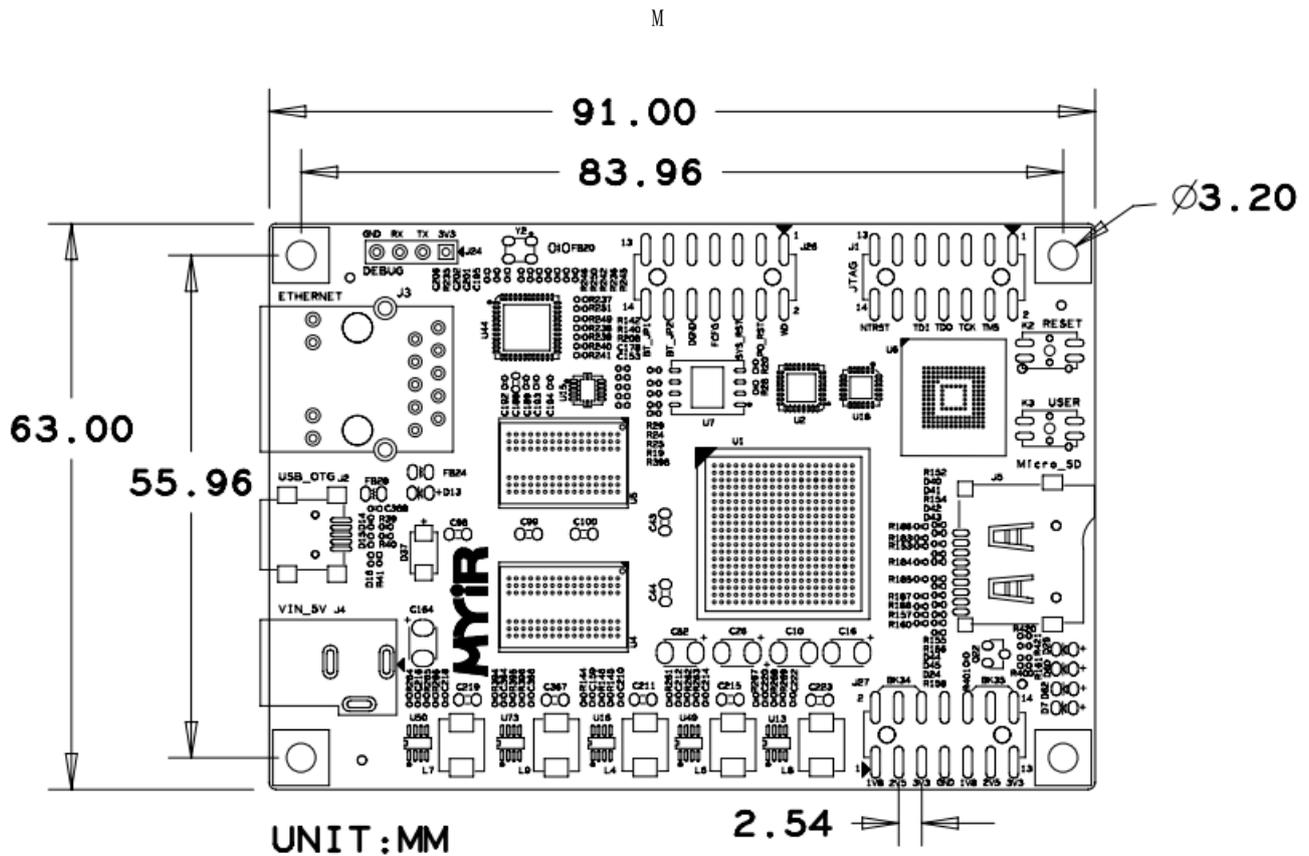*Figure 1-6 Z-turn Lite Dimension Chart*

Software Features

Item	Features	Description	Remark
Cross compiler	gcc 4.6.1	gcc version 4.6.1 (SourceryCodeBench Lite 2011.09-50)	
Boot program	BOOT.BIN	First boot program including FSBL, bitstream and u-boot	Source code provided
Linux Kernel	Linux 3.15.0	Customized kernel for Z-turn Lite Board	Source code provided
Drivers	USB OTG	USB OTG driver	Source code provided
	Ethernet	Gigabit Ethernet driver	Source code provided
	MMC/SD/TF	MMC/SD/TF card driver	Source code provided
	Button	Button driver	Source code provided
	UART	UART driver	Source code provided
	LED	LED driver	Source code provided
	GPIO	GPIO driver	Source code provided
	Watchdog	Watchdog driver	Source code provided
File System	Ramdisk	Ramdisk system image	

Table 1-2 Software Features of Z-turn Lite

Order Information

Item	Part No.	Packing List
Z-turn Lite	MYS-7Z007S-C-S	➢ One Z-turn Lite (for Zynq-7007S) ➢ One product disk ➢ One 4GB TF card
	MYS-7Z010-L-C-S	➢ One Z-turn Lite (for Zynq-7010) ➢ One product disk ➢ One 4GB TF card
Z-turn Lite Kit	MYS-7Z007S-C	➢ One Z-turn Lite (for Zynq-7007S) ➢ One 1.5m cross Ethernet cable ➢ One 1.2m Micro USB2.0 cable ➢ One MY-UART012U USB-to-UART cable ➢ One 4GB TF card ➢ One 5V/2A Power adapter ➢ One product disk (including user manual, schematic in PDF format, datasheets and software package)
	MYS-7Z010-L-C	➢ One Z-turn Lite (for Zynq-7010) ➢ One 1.5m cross Ethernet cable ➢ One 1.2m Micro USB2.0 cable ➢ One MY-UART012U USB-to-UART cable ➢ One 4GB TF card ➢ One 5V/2A Power adapter ➢ One product disk (including user manual, schematic in PDF format, datasheets and software package)

MYiR™

MYIR Tech Limited
Room 1306, Wensheng Center, Wenjin Plaza, North Wenjin Road, Luohu District,
Shenzhen, China 518020
E-mail: sales@myirtech.com
Phone: +86-755-22984836
Fax: +86-755-25532724
Website: http://www.myirtech.com