UM2248
User manual

Evaluation board with STM32L4R9AI MCU

Introduction

The STM32L4R9I-EVAL board is designed as complete demonstration and development platform for the STMicroelectronics Arm® Cortex®-M4 core-based STM32L4R9AI microcontroller with four I²C buses, three SPI and six USART ports, CAN port, two SAI ports, 12-bit ADC, 12-bit DAC, internal 640-Kbyte SRAM and 2-Mbyte Flash memory, two Octo-SPI memory interfaces, touch-sensing capability, USB OTG FS port, LCD-TFT controller, MIPI® DSI host controller, flexible memory controller (FMC), 8- to 14-bit camera interface and JTAG debugging support.

The STM32L4R9I-EVAL, shown in *Figure 3*, *Figure 4*, and *Figure 5*, is used as a reference design for user application development before porting to the final product.

The full range of hardware features on the board helps the user to evaluate all the peripherals (USB, USART, digital microphones, ADC and DAC, TFT LCD, MIPI DSI display, LDR, SRAM, NOR Flash memory device, Octo-SPI Flash memory device, microSD™ card, sigma-delta modulators, CAN transceiver, EEPROM) and develop applications. Extension headers allow easy connection of a daughterboard or wrapping board for a specific application.

An ST-LINK/V2-1 is integrated on the board, as the embedded in-circuit debugger and programmer for the STM32 MCU and the USB virtual COM port bridge.

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1 Features

- STM32L4R9AII6 Arm-based microcontroller with 2 Mbytes of Flash memory and 640 Kbytes of RAM in a UFBGA169 package
- 1.2” 390x390 pixels MIPI DSI round LCD
- 4.3” 480x272 pixels TFT LCD with RGB mode
- Two ST-MEMS digital microphones
- 8-Gbyte microSD card bundled
- 16-Mbit (1 M x 16 bit) SRAM device
- 128-Mbit (8 M x 16 bit) NOR Flash memory device
- 512-Mbit Octo-SPI Flash memory device with double transfer rate (DTR) support
- 64-Mbit Octo-SPI SRAM memory device with HyperBus interface support
- EEPROM supporting 1 MHz I²C-bus communication speed
- Reset and wake-up / tamper buttons
- Joystick with four-way controller and selector
- Touch-sensing button
- Light-dependent resistor (LDR)
- Potentiometer
- Coin battery cell for power backup
- Board connectors:
  - Two jack outputs for stereo audio headphone with independent content
  - Slot for microSD card supporting SD and SDHC
  - TFT LCD standard connector
  - MIPI DSI display standard connector
  - EXT_I2C connector supports I²C bus
  - RS-232 port configurable for communication or MCU flashing
  - USB OTG FS Micro-AB port
  - CAN 2.0A/B-compliant port
  - Connector for ADC input and DAC output
  - JTAG/SWD connector
  - ETM trace debug connector
  - User interface through USB virtual COM port
  - Embedded ST-LINK/V2-1 debug and flashing facility
  - TAG connector
  - STDC14 connector
  - PMOD connector
- Board expansion connectors:
  - Motor-control connector
  - Extension connector for daughterboard
- Flexible power-supply options: power jack, ST-LINK/V2-1 USB connector, USB OTG FS connector, daughterboard
- On-board ST-LINK/V2-1 debugger/programmer with USB re-enumeration capability:

mass storage, virtual COM port and debug port

- Microcontroller supply voltage: fixed 3.3 V or adjustable range from 1.71 V to 3.6 V
- MCU current consumption measurement circuit
- Access to comparator and operational amplifier of STM32L4R9AII6
- Comprehensive free software libraries and examples available with the STM32Cube package
- Support of a wide choice of integrated development environments (IDEs) including IAR™, Keil®, GCC-based IDEs

arm

2 Product marking

Evaluation tools marked as “ES” or “E” are not yet qualified and therefore not ready to be used as reference design or in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples tools as reference design or in production.

“E” or “ES” marking examples of location:

- On the targeted STM32 that is soldered on the board (for illustration of STM32 marking, refer to the STM32 datasheet “Package information” paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck or silk-screen printed on the board.

This board features a specific STM32 device version which allows the operation of any stack or library. This STM32 device shows a “U” marking option at the end of the standard part number and is not available for sales.

3 System requirements

- Windows® OS (XP, 7, 8, 10) or Linux® or macOS®
- USB Type-A to Macro-B cable

4 Development toolchains

- Arm® Keil®: MDK-ARM™ (a)
- IAR™: EWARM(a)
- GCC-based IDEs (free AC6: SW4STM32, Atollic® TrueSTUDIO® (a) and others)

a. On Windows only

5 Demonstration software

The demonstration software, included in the STM32Cube package corresponding to on-board MCU, is preloaded in the STM32 Flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation are available from *www.st.com*.

6 Ordering information

To order the evaluation board based on the STM32L4R9AII6 MCU, use the order code STM32L4R9I-EVAL.

7 Delivery recommendations

Before the first use, make sure that, no damage occurred to the board during shipment and no socketed components are loosen in their sockets or fallen into the plastic bag.

In particular, pay attention to the following components:

1. microSD card in its CN8 receptacle
2. DSI display MB1314 daughterboard in its CN16 connector

For product information related with STM32L4R9AII6 microcontroller, visit *www.st.com* website.

8 Technology partners

MACRONIX: 512-Mbit Octo-SPI Flash, part number MX25LM51245GXDI00

9 Hardware layout and configuration

The STM32L4R9I-EVAL board is designed around STM32L4R9AII6 target microcontroller in UFBGA 169-pin package. *Figure 1* illustrates STM32L4R9AII6 connections with peripheral components. *Figure 2* shows the location of main components on the evaluation board. *Figure 3*, *Figure 4*, and *Figure 5* are the three images showing the STM32L4R9I-EVAL board top view with round DSI display, top view with TFT LCD, and bottom view.

Figure 1. STM32L4R9I-EVAL hardware block diagram

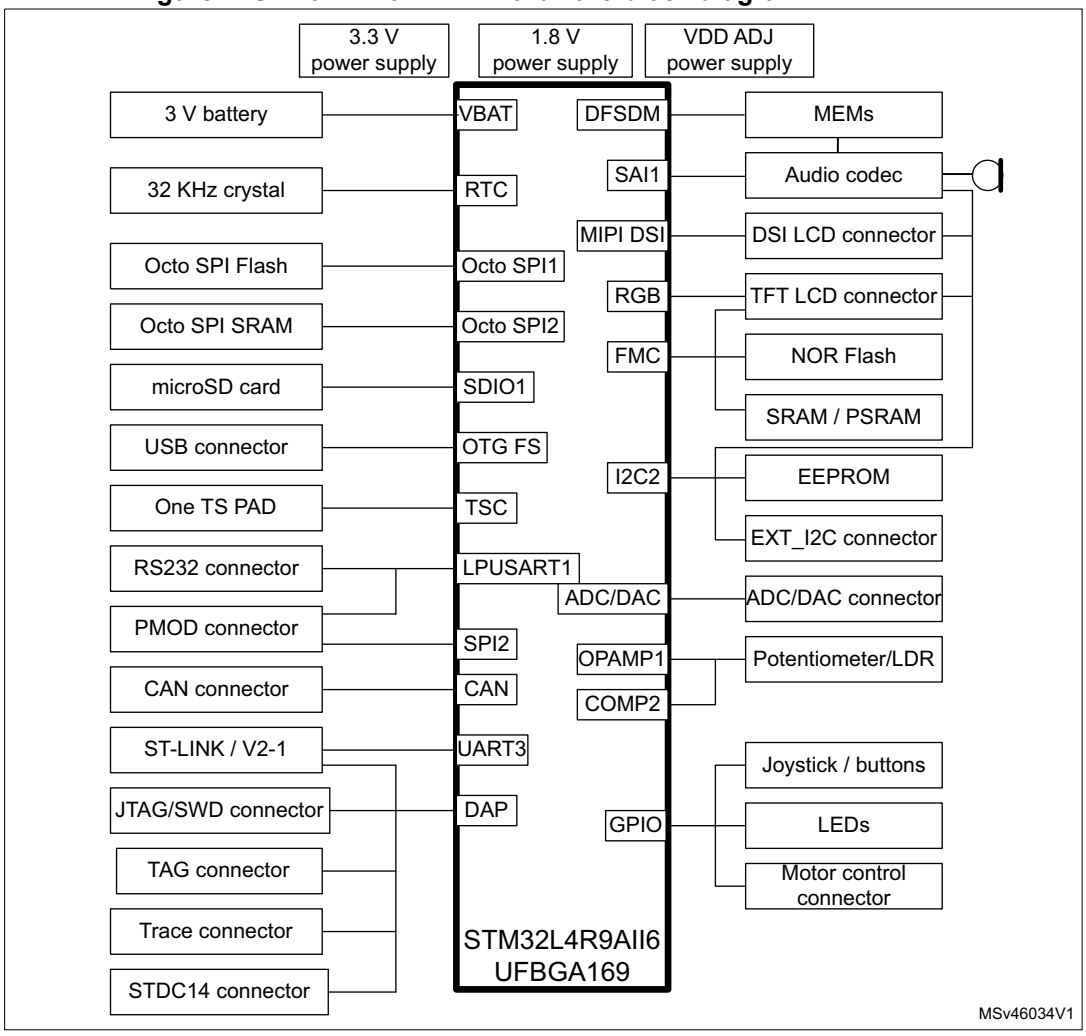
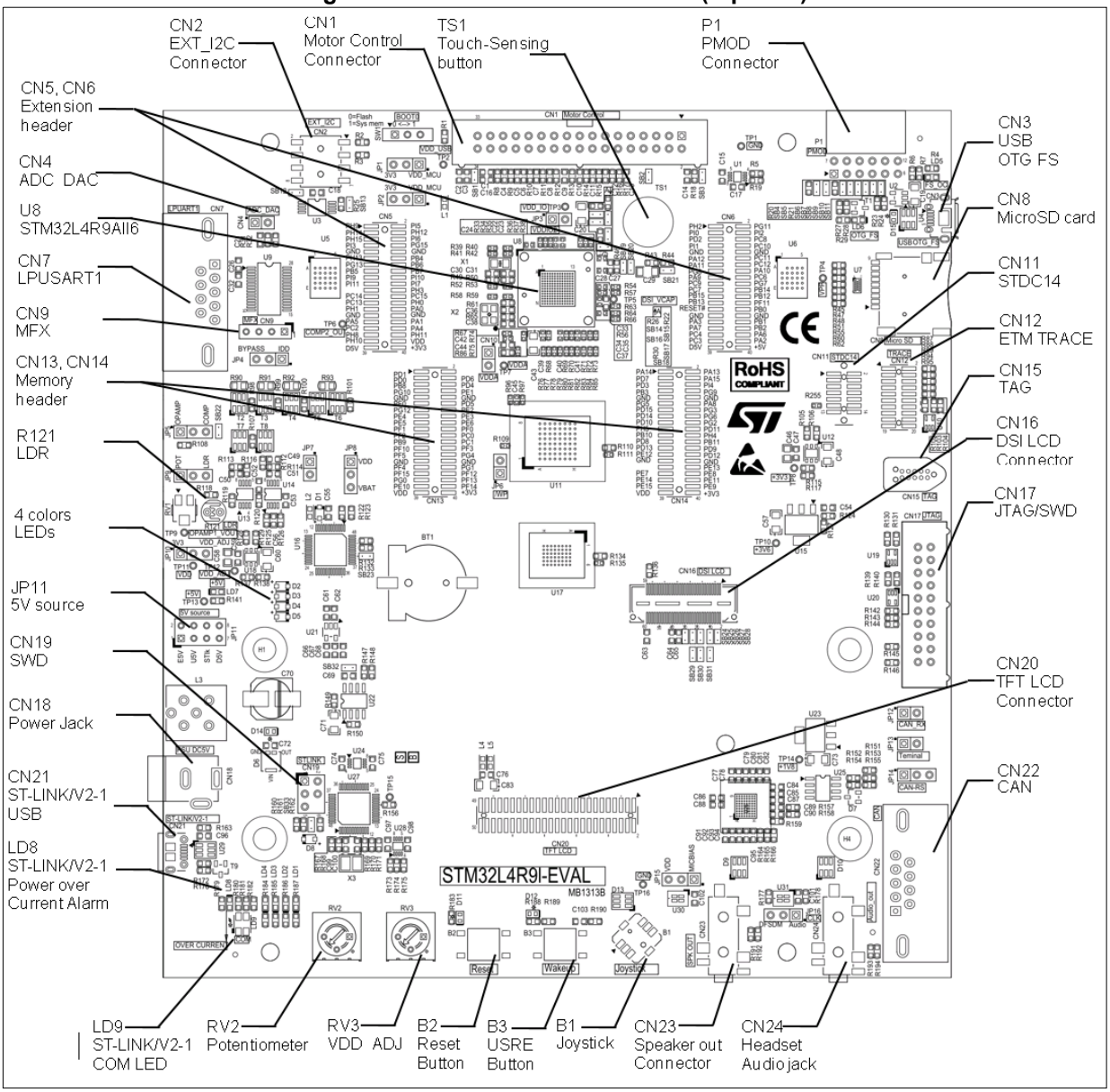
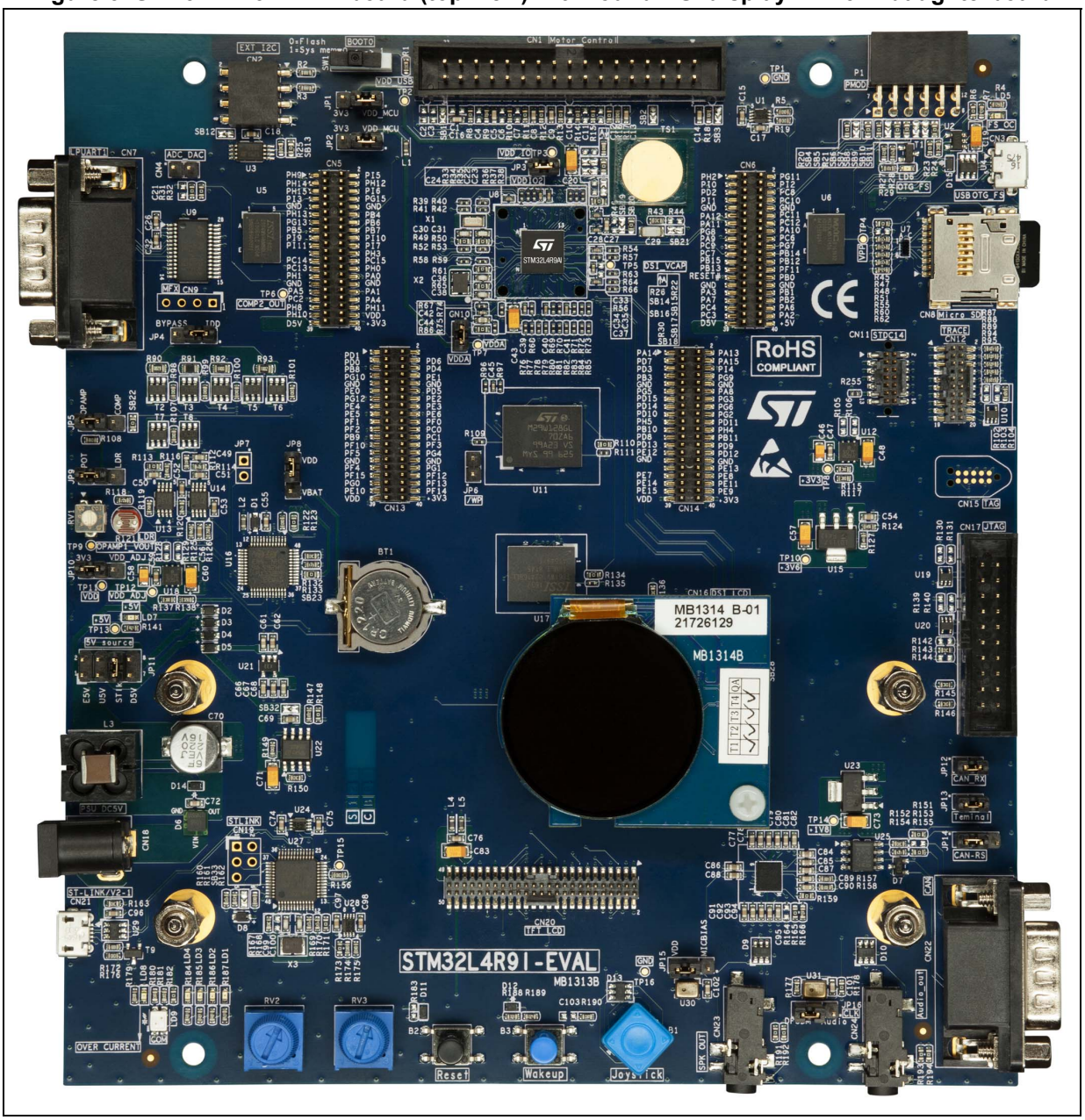


Figure 2. STM32L4R9I-EVAL board (top side)



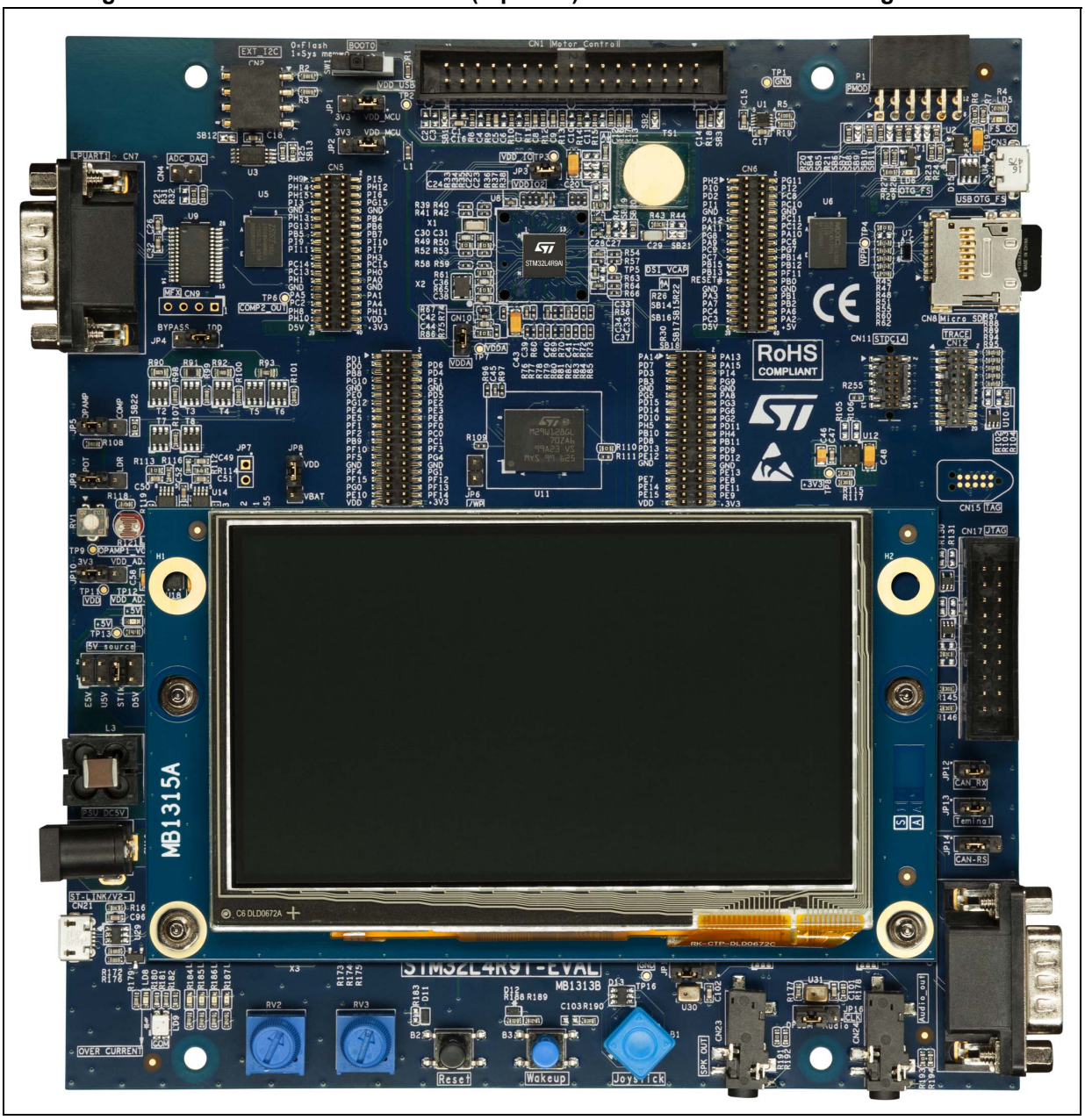
9.1 STM32L4R9I-EVAL board views

Figure 3. STM32L4R9I-EVAL board (top view) with round DSI display MB1314 daughterboard



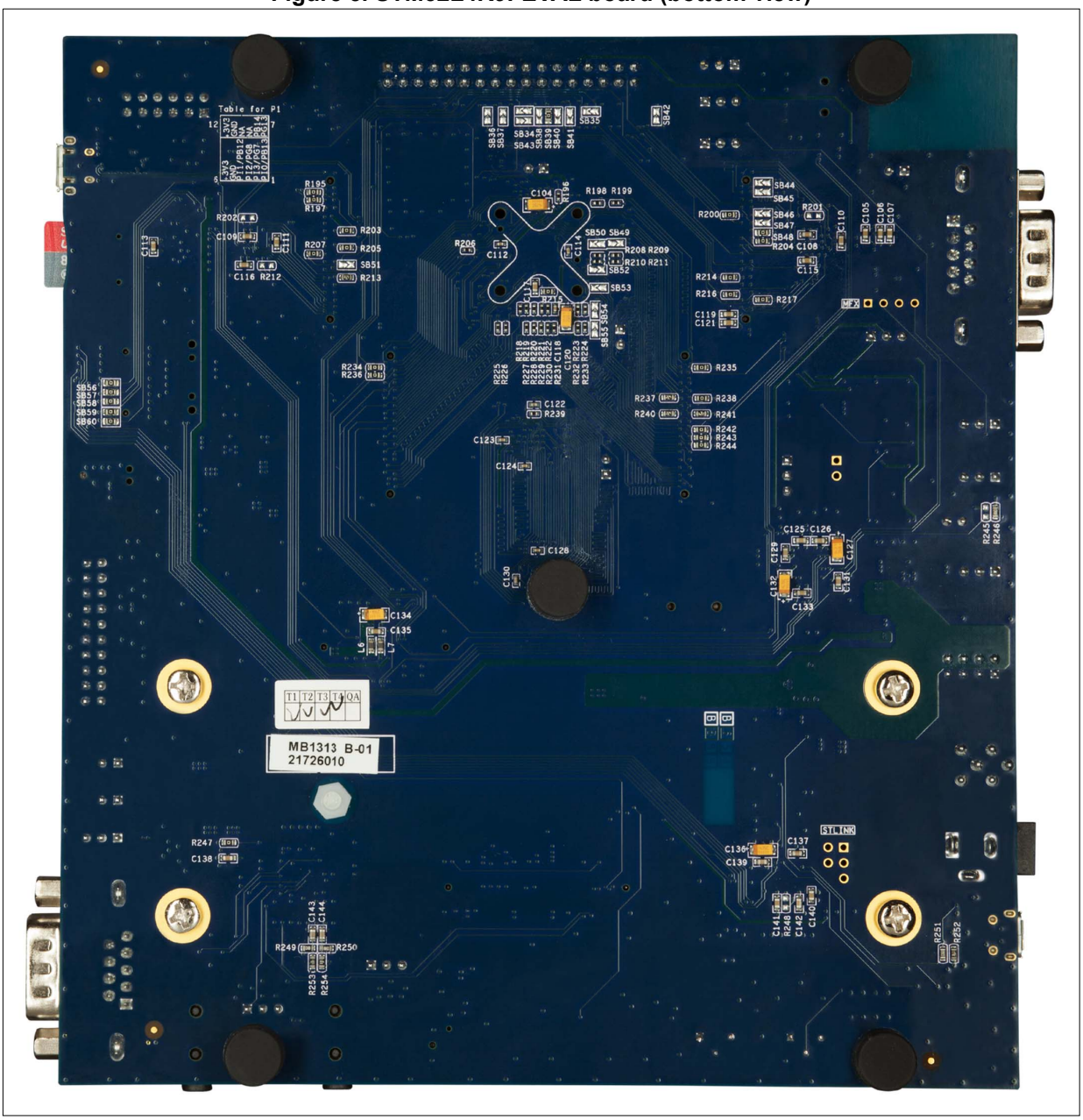
Picture is not contractual

Figure 4. STM32L4R9I-EVAL board (top view) with TFT LCD MB1315 daughterboard



Picture is not contractual

Figure 5. STM32L4R9I-EVAL board (bottom view)



Picture is not contractual

9.2 Mechanical dimensions

Figure 6. MB1313 STM32L4R9I-EVAL board

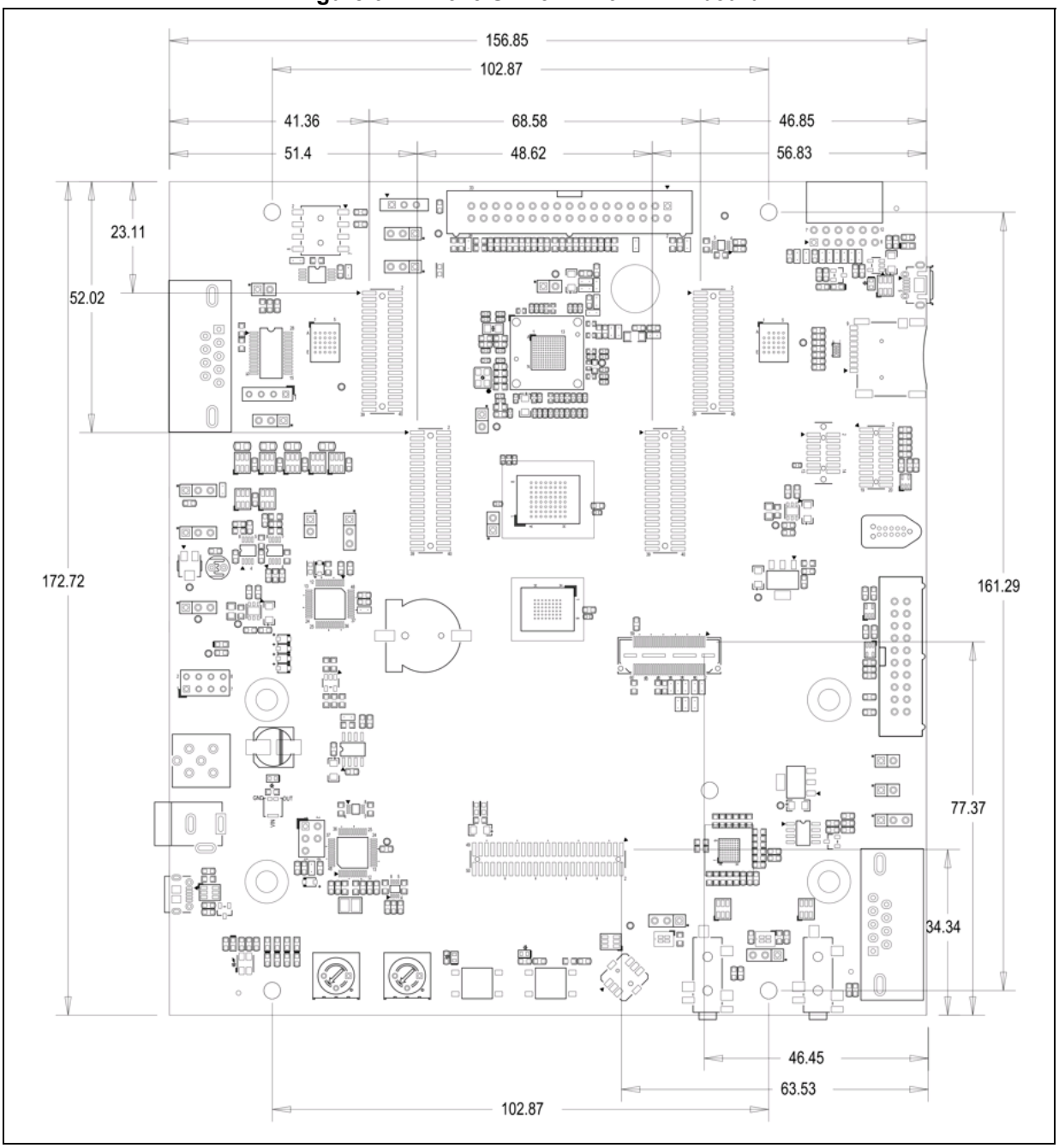
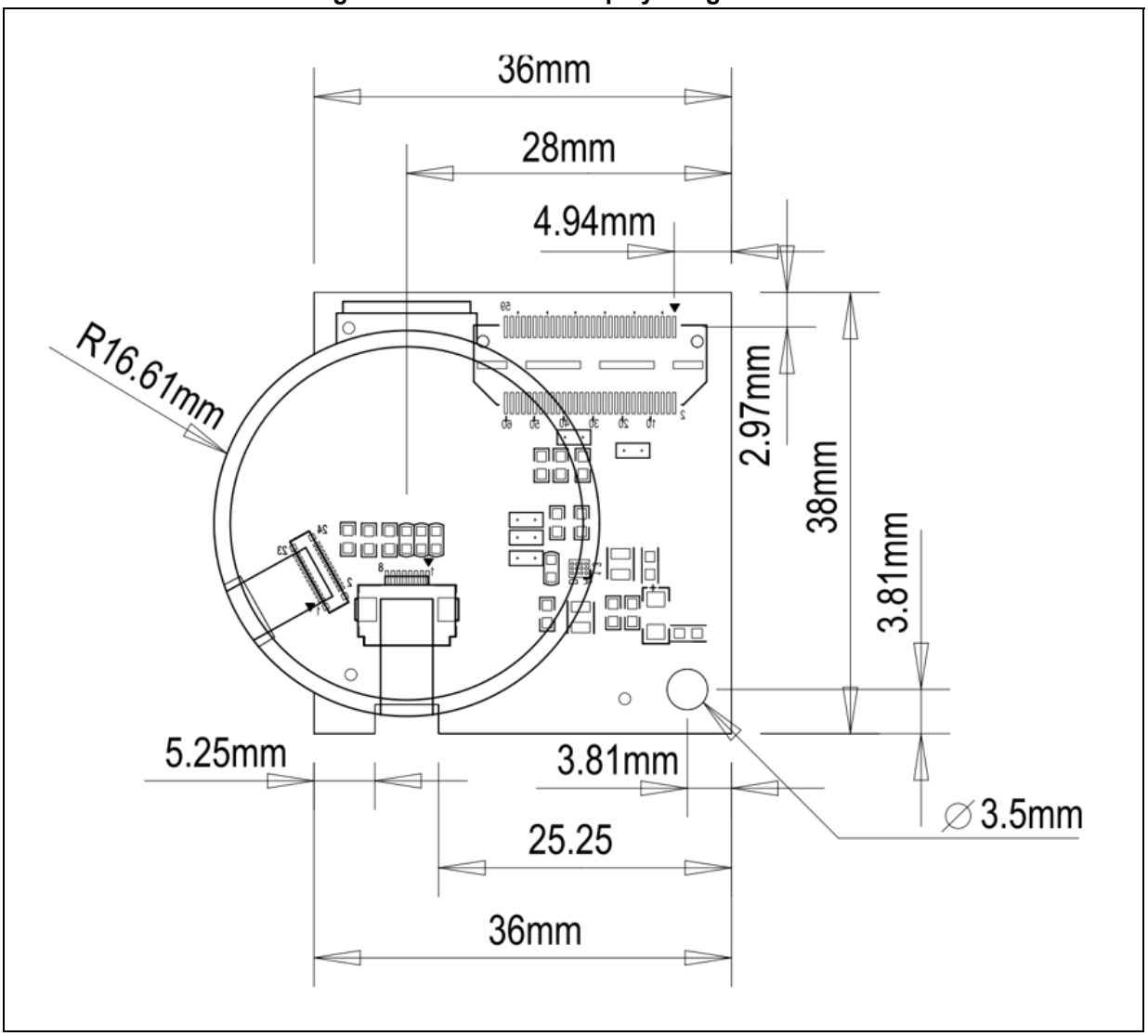


Figure 7. MB1314 DSI display daughterboard



9.3 ST-LINK/V2-1

ST-LINK/V2-1 facility for debug and flashing of STM32L4R9AII6, is integrated on the STM32L4R9I-EVAL board.

Compared to ST-LINK/V2 stand-alone tool available from STMicroelectronics, ST-LINK/V2-1 offers new features and drops some others.

New features:

- USB software re-enumeration
- Virtual COM port interface on USB
- Mass storage interface on USB
- USB power management request for more than 100mA power on USB

Features dropped:

- SWIM interface

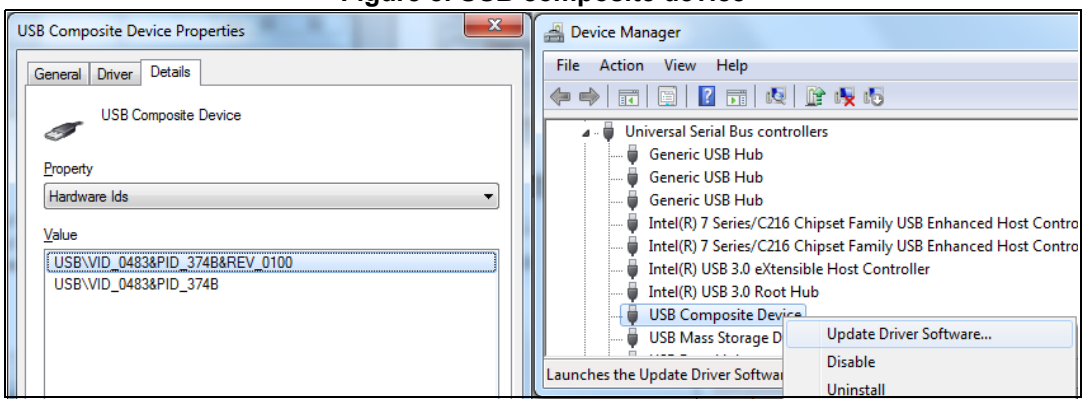
The USB connector CN21 is usable to power STM32L4R9I-EVAL regardless of the ST-LINK/V2-1 facility use for debugging or for flashing STM32L4R9AII6. This holds also when ST-LINK/V2 stand-alone tool is connected to CN12 or CN17 or CN11 or CN15 connector and used for debugging or flashing STM32L4R9AII6. *Section 9.5* provides more detail on powering STM32L4R9I-EVAL.
For full detail on both versions of the debug and flashing tool, the stand-alone ST-LINK/V2 and the embedded ST-LINK/V2-1, refer to *www.st.com*.

9.3.1 Drivers

Before connecting STM32L4R9I-EVAL to a Windows (XP, 7, 8 10) PC via USB, a driver for ST-LINK/V2-1 must be installed. It is available from *www.st.com*.

In case the STM32L4R9I-EVAL board is connected to the PC before installing the driver, the Windows device manager may report some USB devices found on STM32L4R9I-EVAL as “Unknown”. To recover from this situation, after installing the dedicated driver downloaded from *www.st.com*, the association of “Unknown” USB devices found on STM32L4R9I-EVAL to this dedicated driver must be updated in the device manager manually. It is recommended to proceed using USB Composite Device line, as shown in *Figure 8*.

Figure 8. USB composite device



9.3.2 ST-LINK/V2-1 firmware upgrade

For its own operation, ST-LINK/V2-1 employs a dedicated MCU with Flash memory. Its firmware determines ST-LINK/V2-1 functionality and performance. The firmware may evolve during the life span of STM32L4R9I-EVAL to include new functionality, fix bugs or support new target microcontroller families. It is therefore recommended to keep ST-LINK/V2-1 firmware up to date. The latest version is available from *www.st.com*.

9.4 ETM trace

The connector CN12 is available to output trace signals used for debug. By default, the evaluation board is configured such that, STM32L4R9AII6 signals PE2, PE5 and PE6 are not connected to trace outputs Trace_CK, Trace_D2, and Trace_D3 of CN12. They are used for other functions.

Table 1 shows the setting of configuration elements to shunt PE2, PE5 and PE6 MCU ports to CN12 connector, to use them as debug trace signals.

Table 1. Setting of configuration elements for trace connector CN12

Element	Setting	Configuration
R53 SB56	R53 in SB56 open	Default setting. PE2 connected to memory address line A23.
	R53 out SB56 closed	PE2 connected to Trace_CK on CN12. A23 pulled down.
R209 SB59	R209 in SB59 open	Default setting. PE5 connected to memory address line A21.
	R209 out SB59 closed	PE5 connected to Trace_D2 on CN12. A21 pulled down.
R211 SB60	R211 in SB60 open	Default setting. PE6 connected to memory address line A22.
	R211 out SB60 closed	PE6 connected to Trace_D3 on CN12. A22 pulled down.

Warning: Enabling the CN12 trace outputs through hardware modifications described in *Table 1* results in reducing the memory address bus width to 20 address lines and so the addressable space to 1 Mwords of 16 bits. As a consequence, the on-board SRAM and NOR Flash memory usable capacity is reduced to 16 Mbits.

9.5 Power Supply

The STM32L4R9I-EVAL board is designed to be powered from 5 V DC power source. It incorporates a precise polymer Zener diode (Poly-Zen) protecting the board from damage due to wrong power supply. One of the following four 5 V DC power inputs is usable with an appropriate board configuration:

- Power jack CN18, marked PSU_DC5V on the board. A jumper must be placed in E5V location of JP11. The positive pole is on the center pin as illustrated in *Figure 20*.
- Micro-B USB receptacle CN21 of ST-LINK/V2-1, provides up to 500mA to the board. Offering enumeration feature described in *Section 9.5.1*.
- Micro-AB USB receptacle CN3 of USB OTG interface, marked USB OTG_FS on the board, supplies up to 500mA to the board.
- Pin 39 of CN5 and Pin 39 of CN6 extension connectors for custom daughterboard, marked D5V on the board.

No external power supply is provided with the board.

LD7 red LED turns on when the voltage on the power line marked as +5 V is present. All supply lines required for the operation of the components on STM32L4R9I-EVAL are derived from that +5 V line.

Table 2 describes the setting of all jumpers related with powering STM32L4R9I-EVAL and extension board. VDD_MCU is STM32L4R9AII6 digital supply voltage line. It is possible to drive the boards with either fixed 3.3 V or with an adjustable voltage regulator controlled by RV3 potentiometer and producing a range of voltages between 1.71 V and 3.6 V.

9.5.1 Supplying the board through ST-LINK/V2-1 USB port

To power STM32L4R9I-EVAL in this way, the USB host (a PC) gets connected with the STM32L4R9I-EVAL board's Micro-B USB receptacle, via a USB cable. This event starts the USB enumeration procedure. In its initial phase, the host's USB port current supply capability is limited to 100 mA. It is enough because only ST-LINK/V2-1 part of STM32L4R9I-EVAL draws power at that time. If the solder bridge SB33 is open, the U22 ST890 power switch is set to OFF position, which isolates the remainder of STM32L4R9I-EVAL from the power source. In the next phase of the enumeration procedure, the host PC informs the ST-LINK/V2-1 facility of its capability to supply up to 300 mA of current. If the answer is positive, the ST-LINK/V2-1 sets the U22 ST890 switch to ON position to supply power to the remainder of the STM32L4R9I-EVAL board. If the PC USB port is not capable of supplying up to 300 mA of current, the CN18 power jack is available to supply the board.

Should a short-circuit occur on the board, the ST890 power switch protects the USB port of the host PC against a current demand exceeding 600 mA, In such an event, the LD8 LED lights on.

The STM32L4R9I-EVAL board is also supply-able from a USB power source not supporting enumeration, such as a USB charger, as shown in *Table 2*. ST-LINK/V2-1 turns the ST890 power switch ON regardless of enumeration procedure result and passes the power unconditionally to the board.

The LD7 red LED turns on whenever the whole board is powered.

9.5.2 Using ST-LINK/2-1 along with powering through CN18 power jack

If the board requires more than 300 mA of supply current, this cannot be provided by host PC connected to ST-LINK/2-1 USB port, used for debugging or flashing STM32L4R9AII6. In such a case, the board is supplied through CN18 (marked PSU_DC5V on the board).

To do this, it is important to power the board before connecting it with the host PC, which requires the following sequence to be respected:

1. Set the jumper in JP11 header in E5V position
2. Connect the external 5 V power source to CN18
3. Check the red LED LD7 is turned on
4. Connect host PC to USB connector CN21

In case the board demands more than 300 mA and the host PC is connected via USB before the board is powered from CN18, there is a risk of the following events to occur, in the order of severity:

1. The host PC is capable of supplying 300 mA (the enumeration succeeds) but it does not incorporate any over-current protection on its USB port. It is damaged due to over-current.
2. The host PC is capable of supplying 300 mA (the enumeration succeeds) and it has a built-in over-current protection on its USB port, limiting or shutting down the power out of its USB port when the excessive current demand from STM32L4R9I-EVAL is detected. This causes an operating failure to STM32L4R9I-EVAL.
3. The host PC is not capable of supplying 300 mA (the enumeration fails) so ST-LINK/V2-1 does not supply the remainder of STM32L4R9I-EVAL from its USB port VBUS line.

Table 2. Power supply related jumpers settings

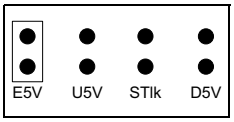
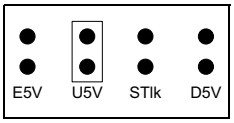
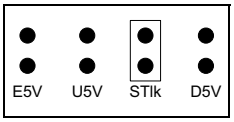
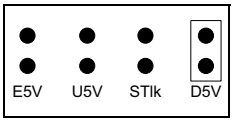
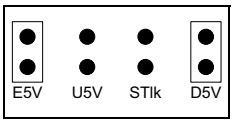
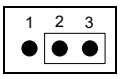
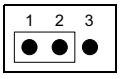
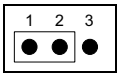
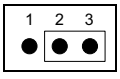
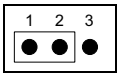
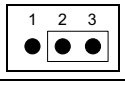
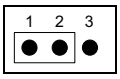
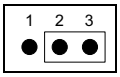
Jumper / solder bridge	Setting	Configuration
JP11 Power source selector		STM32L4R9I-EVAL is supplied through CN18 power jack (marked PSU_DC5V). CN5 and CN6 extension connectors do not pass the 5 V of STM32L4R9I-EVAL to daughterboard.
		STM32L4R9I-EVAL is supplied through CN3 Micro-AB USB connector. CN5 and CN6 extension connectors do not pass the 5 V of STM32L4R9I-EVAL to daughterboard.
		Default setting. STM32L4R9I-EVAL is supplied through CN21 Micro-B USB connector. CN5 and CN6 extension connectors do not pass the 5 V of STM32L4R9I-EVAL to daughterboard.
		STM32L4R9I-EVAL is supplied through pin 39 of CN5 and pin 39 of CN6 extension connectors.
		STM32L4R9I-EVAL is supplied through CN18 power jack. CN5 and CN6 extension connectors pass the 5 V of STM32L4R9I-EVAL to daughterboard. Make sure to disconnect from the daughterboard, any power supply that may generate conflict with the power supply on CN18 power jack.
JP8 Vbat connection		Vbat is connected to battery.
		Default setting. Vbat is connected to VDD.
JP10 VDD_MCU connection		Default setting. VDD_MCU (VDD terminals of STM32L4R9AII6) is connected to fixed +3.3 V.
		VDD_MCU is connected to voltage in the range from +1.71 V to +3.6 V, adjustable with potentiometer RV3.
JP1 VDD_USB connection		Default setting. VDD_USB (VDDUSB terminal of STM32L4R9AII6) is connected with VDD_MCU.
		VDD_USB is connected to +3.3 V.

Table 2. Power supply related jumpers settings (continued)

Jumper / solder bridge	Setting	Configuration
JP2 VDDA connection		Default setting. VDDA terminal of STM32L4R9AII6 is connected with VDD_MCU.
		VDDA terminal of STM32L4R9AII6 is connected to +3.3 V.
JP3 VDD_IO connection		Default setting. VDD_IO (VDDIO2 terminals of STM32L4R9AII6) is connected with VDD_MCU.
		VDD_IO is open.
SB33 Powering through USB of ST-LINK/V2-1	SB33 Off	Default setting. Micro-B USB connector CN21 of ST-LINK/V2-1 is usable to supply power to the STM32L4R9I-EVAL board remainder, depending on host PC USB port's powering capability declared in the enumeration.
	SB33 On	Micro-B USB connector CN21 of ST-LINK/V2-1 supplies power to the STM32L4R9I-EVAL board remainder. Setting for powering the board through CN21 using USB charger.(1)

1. On all ST-LINK/V2-1 boards, the target application is now able to run even if the STLINK/V2-1 is either not connected to an USB host, or is powered through a USB charger (or through a not-enumerating USB host).

9.6 Clock references

Two clock references are available on STM32L4R9I-EVAL for STM32L4R9AII6 microcontroller.

- 32.768 kHz crystal X1, for embedded RTC
- 25 MHz crystal X2, for mail clock generator

The main clock generation is possible via an internal RC oscillator, disconnected by removing resistors R61 and R65 when internal RC clock is used.

Table 3. X1 crystal related solder bridge settings

Solder bridge	Setting	Configuration
SB50	Open	Default setting. PC14 OSC32_IN terminal is not routed to extension connector CN5. X1 is used as clock reference.
	Closed	PC14 OSC32_IN is routed to extension connector CN5. Resistor R50 must be removed, for X1 quartz circuit not to disturb clock reference or source on daughterboard.

Table 3. X1 crystal related solder bridge settings (continued)

Solder bridge	Setting	Configuration
SB49	Open	Default setting. PC15 OSC32_OUT terminal is not routed to extension connector CN5. X1 is used as clock reference.
	Closed	PC15 OSC32_OUT is routed to extension connector CN5. Resistor R49 must be removed, for X1 quartz circuit not to disturb clock reference on daughterboard.

Table 4. X2 crystal related solder bridge settings

Solder bridge	Setting	Configuration
SB52	Open	Default setting. PH0 OSC_IN terminal is not routed to extension connector CN5. X2 is used as clock reference.
	Closed	PH0 OSC_IN is routed to extension connector CN5. Resistor R61 must be removed, in order not to disturb clock reference or source on daughterboard.
SB53	Open	Default setting. PH1 OSC_OUT terminal is not routed to extension connector CN5. X2 is used as clock reference.
	Closed	PH1 OSC_OUT is routed to extension connector CN5. Resistor R65 must be removed, in order not to disturb clock reference or source on daughterboard.

9.7 Reset sources

The reset signal of STM32L4R9I-EVAL board is active low.

Sources of reset are listed below:

- reset button B2
- JTAG/SWD connector CN17, ETM trace connector CN12, STDC14 connector CN11 and TAG connector CN15 (reset from debug tools)
- reset through extension connector CN6 pin 27 (reset from daughterboard)
- embedded ST-LINK/V2-1

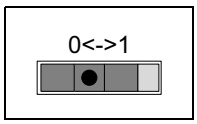
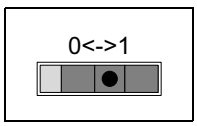
9.8 Boot option

After reset, the STM32L4R9AII6 MCU boot is available from the following embedded memory locations:

- main (user, non-protected) Flash memory
- system (protected) Flash memory
- RAM, for debugging

The boot option is configured by setting switch SW1 (BOOT) and the boot base address programmed in the nBOOT1, nBOOT0 and nSWBOOT0 of FLASH_OPTR option bytes.

Table 5. Boot selection switch

Switch	Setting	Description
SW1		Default setting. BOOT0 line is tied low. STM32L4R9AII6 boots from main Flash memory or system memory.
		BOOT0 line is tied high. STM32L4R9AII6 boots from system Flash memory (nBOOT1 bit of FLASH_OPTR register is set high) or from RAM (nBOOT1 is set low).

9.8.1 Bootloader limitations

Boot from system Flash memory results in executing bootloader code stored in the system Flash memory protected against writing and erasing. This allows in-system programming (ISP), that is, flashing the STM32 user Flash memory. It also allows writing data into RAM. The data come in via one of communication interfaces such as USART, SPI, I2C bus, USB or CAN.

Bootloader version is identified by reading the Bootloader ID at the address 0x1FFF6FFE: the content is 0x91 for bootloader V9.1 and 0x92 for V9.2.

The STM32L4R9AII6 part soldered on the STM32L4R9I-EVAL main board is marked with a date code corresponding to its date of manufacturing. STM32L4R9AII6 parts with a date code prior or equal to week 37 of 2017 are fitted with bootloader V9.1 affected by the limitations to be worked around, as described hereunder. Parts with the date code starting from week 38 of 2017 contain bootloader V9.2 in which the limitations no longer exist.

To locate the visual date code information on the STM32L4R9II6 package, refer to its datasheet (DS12023) available at *www.st.com*, section Package Information. Date code related portion of the package marking takes Y WW format, where Y is the last digit of the year and WW is the week. For example, a part manufactured in week 38 of 2017 bares the date code 7 38.

There is also another mean to identify the need for workaround: before opening the blister of the Discovery Kit, just check the back side of the blister. At the bottom left side, if the reference number is equal or higher than 32L4R9IDISCO/ 02-0, it means the bootloader version is V9.2 and there is no need to apply workaround. Any other inferior number like 01-0 will need the workaround.

Bootloader ID for the bootloader V9.1 is 0x91.

The following limitation exists in the bootloader V9.1:

Some user Flash memory data get corrupted when written via SPI interface

Description:

During bootloader SPI Write Flash operation, some random 64-bits (2 double-words) may be left blank at 0xFF

Workarounds:

WA1: add a delay between sending Write command and its ACK request. Its duration should be the duration of the 256-Byte Flash write time.

WA2: read back after each write operation (256 bytes or at end of user code flashing) and in case of error start write again.

WA3: Using bootloader, load a patch code in RAM to write in Flash memory through same Write Memory write protocol as bootloader (code provided by ST). The patch code is available for download from *www.st.com* website with a readme.txt file containing usage instructions.

9.9 Audio

A codec connected to STM32L4R9AII6 SAI interface supports DSAI port TDM feature. This offers STM32L4R9AII6 the capability to simultaneously stream two independent stereo audio channels to two separate stereo analog audio outputs.

There are two digital microphones on STM32L4R9I-EVAL board.

9.9.1 Digital microphones

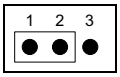
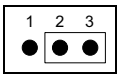
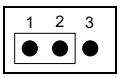
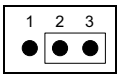
U30 and U31 on STM32L4R9I-EVAL board are MP34DT01TR MEMS digital omnidirectional microphones providing PDM (pulse density modulation) outputs. To share the same data line, their outputs are interlaced. The combined data output of the microphones is directly routed to STM32L4R9AII6 terminals, thanks to the integrated input digital filters. The microphones are supplied with programmable clock generated directly by STM32L4R9AII6.

As an option, the microphones is connected to U26, Wolfson audio codec device, WM8994. In that configuration, U26 also supplies the PDM clock to the microphones.

Regardless of where the microphones are routed to, STM32L4R9AII6 or WM8994, their power supplier is either VDD or MICBIAS1 output of the WM8994 codec device.

Table 6 shows settings of all jumpers associated with the digital microphones on the board.

Table 6. Digital microphone-related jumper settings

Jumper	Setting	Configuration
JP16		PDM clock for digital microphones comes from WM8994 codec.
		Default setting. PDM clock for digital microphones comes from STM32L4R9AII6.
JP15		Power supply of digital microphones is generated by WM8994 codec.
		Default setting. Power supply of digital microphones is V_{DD}.

9.9.2 Headphones outputs

The STM32L4R9I-EVAL board potentially drives two sets of stereo headphones. Identical or different stereo audio content are played back in each set of headphones. STM32L4R9AII6 sends up to two independent stereo audio channels, via its SAI1 TDM port, to the WM8994 codec device. The codec device converts the digital audio stream to stereo analog signals. It then boosts them for direct drive of headphones connecting to 3.5 mm stereo jack receptacles on the board, CN24 for Audio-output1 and CN23 for Audio_output2.

The CN23 jack takes its signal from the output of the WM8994 codec device intended for driving an amplifier for loudspeakers. A hardware adaptation is incorporated on the board to make it compatible with a direct headphone drive. The adaptation consists of coupling capacitors blocking the DC component of the signal, attenuator and anti-pop resistors. The loudspeaker output of the WM8994 codec device must be configured by software in linear mode called “class AB” and not in switching mode called “class D”.

The I²C-bus address of WM8994 is 0b0011 010x.

9.9.3 Limitations in using audio features

Due to the share of some terminals of STM32L4R9AII6 by multiple peripherals, the following limitations apply in using the audio features:

- If the SAI1_MCLKA and SAI1_FSA are used as part of SAI1 port, it cannot be used as CAN peripheral.
- If the SAI1_SDB is used as part of SAI1 port, it cannot be used as Comp2_OUT signal.
- If the SAI1 port of STM32L4R9AII6 is used for streaming audio to the WM8994 codec IC, STM32L4R9AII6 cannot control the motor.
- If the digital microphones are attached to STM32L4R9AII6, control the motor cannot be driven.

9.10 USB OTG FS port

The STM32L4R9I-EVAL board supports USB OTG full-speed (FS) communication. The USB OTG connector CN3 is Micro-AB type.

9.10.1 STM32L4R9I-EVAL used as USB device

When a “USB host” connection to the CN3 Micro-AB USB connector of STM32L4R9I-EVAL is detected, the board starts behaving as “USB device”. Depending on the powering capability of the USB host, the board potentially takes power from VBUS terminal of CN3. In the board schematic diagrams, the corresponding power voltage line is called U5V.

Section 9.5 provides information on how to set associated jumpers for this powering option. The resistor R23 must be left open to prevent STM32L4R9I-EVAL from sourcing 5 V to VBUS terminal, which would cause conflict with the 5 V sourced by the USB host. This may happen if the MFX_GPIO6 is controlled by the software of the MFX MCU such that, it enables the output of U2 power switch.

9.10.2 STM32L4R9I-EVAL used as USB host

When a “USB device” connection to the CN3 Micro-AB USB connector is detected, the STM32L4R9I-EVAL board starts behaving as “USB host”. It sources 5 V on the VBUS

terminal of CN3 Micro-AB USB connector to power the USB device. For this to happen, the STM32L4R9AII6 sets the U2 power switch STMPS2151STR to ON state. The LD6 green LED marked OTG_FS indicates that the peripheral is supplied from the board. The LD5 red LED marked FS_OC lights up if over-current is detected. The resistor R23 must be closed to allow the MFX_GPIO6 from MFX MCU to control the U2 power switch.

In any other STM32L4R9I-EVALpowering option, the resistor R23 must be open, to avoid accidental damage caused to an external USB host.

9.10.3 Limitations in using USB OTG FS port

The USB OTG FS port operation is exclusive with motor control

9.10.4 Operating voltage

The USB-related operating supply voltage of STM32L4R9AII6 (VDD_USB line) must be within the range from 3.0 V to 3.6 V.

9.11 RS232 port

The STM32L4R9I-EVAL board offers one RS-232 communication port. The RS-232 communication port uses the DB9 male connector CN7. RX, TX, RTS and CTS signals of LPUSART1 port of STM32L4R9AII6 are routed to CN7.

9.11.1 Operating voltage

The RS-232 operating supply voltage of STM32L4R9AII6 (VDD line) must be within the range from 1.71 V to 3.6 V.

9.12 microSD card

The CN8 slot for microSD card is routed to STM32L4R9AII6 SDIO port, accepting SD (up to 2 Gbytes) and SDHC (up to 32 Gbytes) cards. One 8-Gbyte microSD card is delivered as part of STM32L4R9I-EVAL. The card insertion switch is routed to the MFX_GPIO5 of MFX MCU port.

9.12.1 Limitations

Due to the share of SDIO port, the following limitations apply:

- The microSD card cannot be operated simultaneously with motor control.
- The microSD card cannot be operated for 4 bits date when SDIO_D1 and SDIO_D2 used as Trace_D0 and Trace_D1 signals.

9.12.2 Operating voltage

The supply voltage for STM32L4R9I-EVAL microSD card operation must be within the range from 2.7 V to 3.6 V.

9.13 Motor control

The CN1 connector is designed to receive a motor-control (MC) module. *Table 7* shows the assignment of CN1 and STM32L4R9AII6 terminals.

Table 7 also lists the modifications to be made on the board versus its by-default configuration. See *Section 9.13.1* for further details.

Table 7. Motor-control terminal and function assignment

Motor-control connector CN1		STM32L4R9AII6 microcontroller			
Terminal	**Terminal name**	**Port name**	**Function**	**Alternate function**	**Board modifications for enabling motor control**
1	Emergency Stop	PI4	TIM8_BKIN	-	Close SB3. Remove R234.
2	GND	-	GND	-	-
3	PWM_1H	PC6	TIM8_CH1	-	Close SB21. Remove R44 or no daughterboard.
4	GND	-	GND	-	-
5	PWM_1L	PH13	TIM8_CH1N	-	Close SB46. Remove R186.
6	GND	-	GND	-	-
7	PWM_2H	PC7	TIM8_CH2	-	Close SB19. Open SB20. Remove R46 or no daughterboard.
8	GND	-	GND	-	-
9	PWM_2L	PH14	TIM8_CH2N	-	Close SB44. Remove R185.
10	GND	-	GND	-	-
11	PWM_3H	PC8	TIM8_CH3	-	Close SB2. Remove R195.
12	GND	-	GND	-	-
13	PWM_3L	PH15	TIM8_CH3N	-	Close SB45. Remove R184.
14	Bus Voltage	PC4	ADC1_IN13	-	Close SB55. Remove R75.
15	PhaseA current+	PC0	ADC1_IN1	-	Close SB36. Remove R242.
16	PhaseA current-	-	GND	-	-

Table 7. Motor-control terminal and function assignment (continued)

Motor-control connector CN1		STM32L4R9AII6 microcontroller			
Terminal	**Terminal name**	**Port name**	**Function**	**Alternate function**	**Board modifications for enabling motor control**
17	PhaseB current+	PC1	ADC1_IN2	-	Close SB37. Remove R244.
18	PhaseB current-	-	GND	-	-
19	PhaseC current+	PC2	ADC1_IN3	-	Close SB43. Remove R217.
20	PhaseC current-	-	GND	-	-
21	ICL Shutout	PG9	GPIO	-	Close SB34. Remove R236.
22	GND	-	GND	-	-
23	Dissipative Brake	PG13	GPIO	-	Close SB47. Remove SB29 and no board on PMOD connector.
24	PFC ind. curr.	PA0	ADC1_IN5	-	Close SB38 Remove R214 and SB39
25	+5V	-	+5V	-	-
26	Heatsink Temp.	PA1	ADC1_IN6	-	Close SB40. Remove R216.
27	PFC Sync	PB14	TIM15_CH1	-	Close SB41. Remove R207 and no board on PMOD connector.
28	+3.3V	-	+3.3V	-	-
29	PFC PWM	PB15	TIM15_CH2	-	Close SB51. Remove R187.
30	PFC Shutdown	PA9	TIM15_BKIN	-	Close SB35. Remove R203.
31	Encoder A	PB6	TIM4_CH1	ADC12_IN	Close SB14. Remove SB15 and SB16. Remove R26 or no daughterboard.
32	PFC Vac	PC3	ADC1_IN4	-	Close SB54. Remove R67.

Table 7. Motor-control terminal and function assignment (continued)

Motor-control connector CN1		STM32L4R9AII6 microcontroller			
Terminal	Terminal name	Port name	Function	Alternate function	Board modifications for enabling motor control
33	Encoder B	PB7	TIM4_CH2	ADC12_IN	Close SB17. Remove SB18. Remove R30 or no daughterboard.
34	Encoder Index	PB8	TIM4_CH3	ADC12_IN	Close SB42. Remove R235 and open JP12.

9.13.1 Board modifications to enable motor control

Figure 9 (top side) and *Figure 10* (bottom side) illustrate the board modifications listed in *Table 7*, required for the operation of motor control. Red color denotes a component to be removed. Green color denotes a component to be fitted.

9.13.2 Limitations

Motor-control operation is exclusive with Octo-SPIP1 Flash memory device, audio codec, potentiometer, LDR, microSD card, LED1 to LED4 drive, MEMS, MFX, PMOD, USB OTG_FS, TFT LCD connector, DSI display connector and touch sensing.

Figure 9. PCB top-side rework for motor control

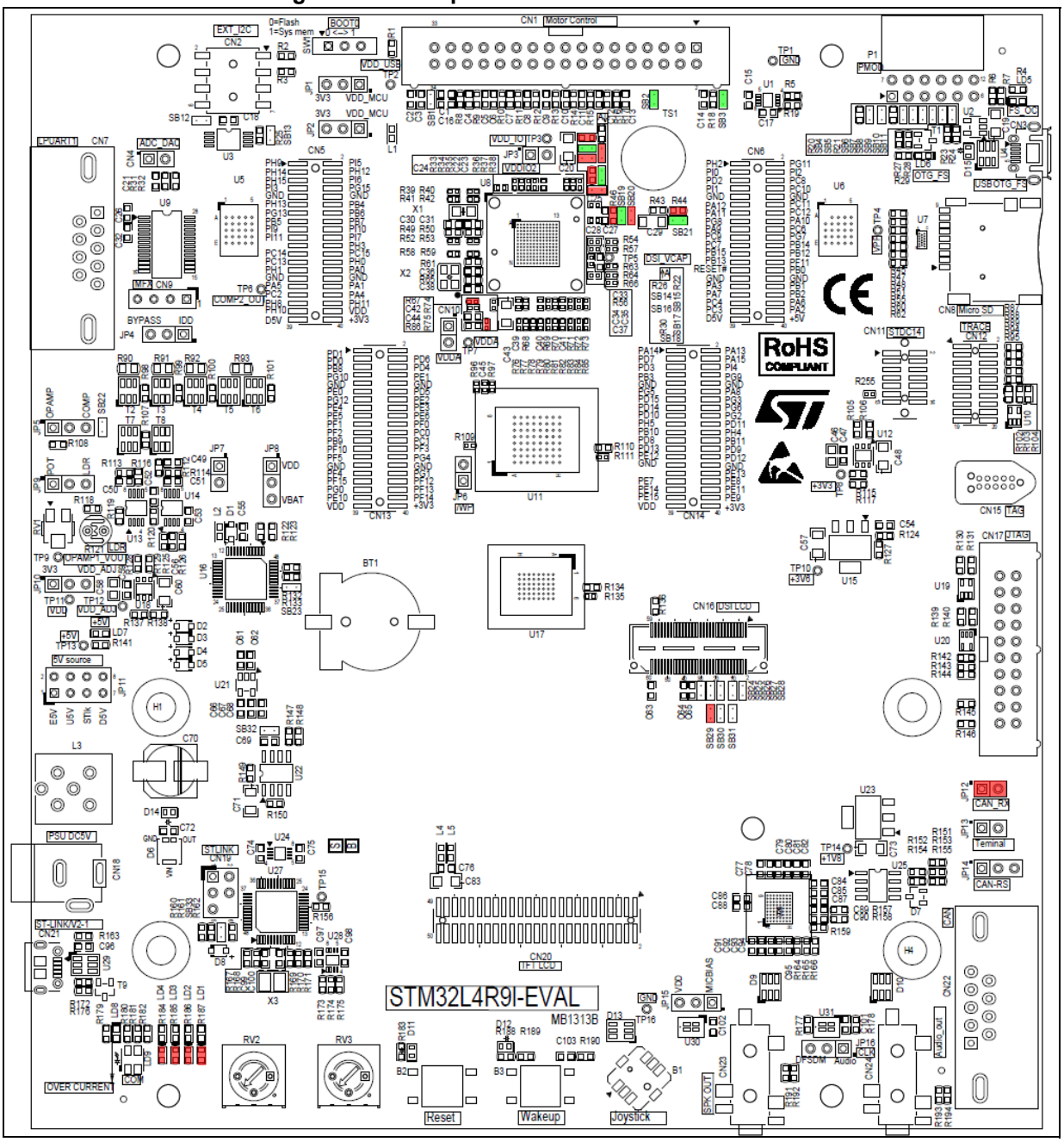
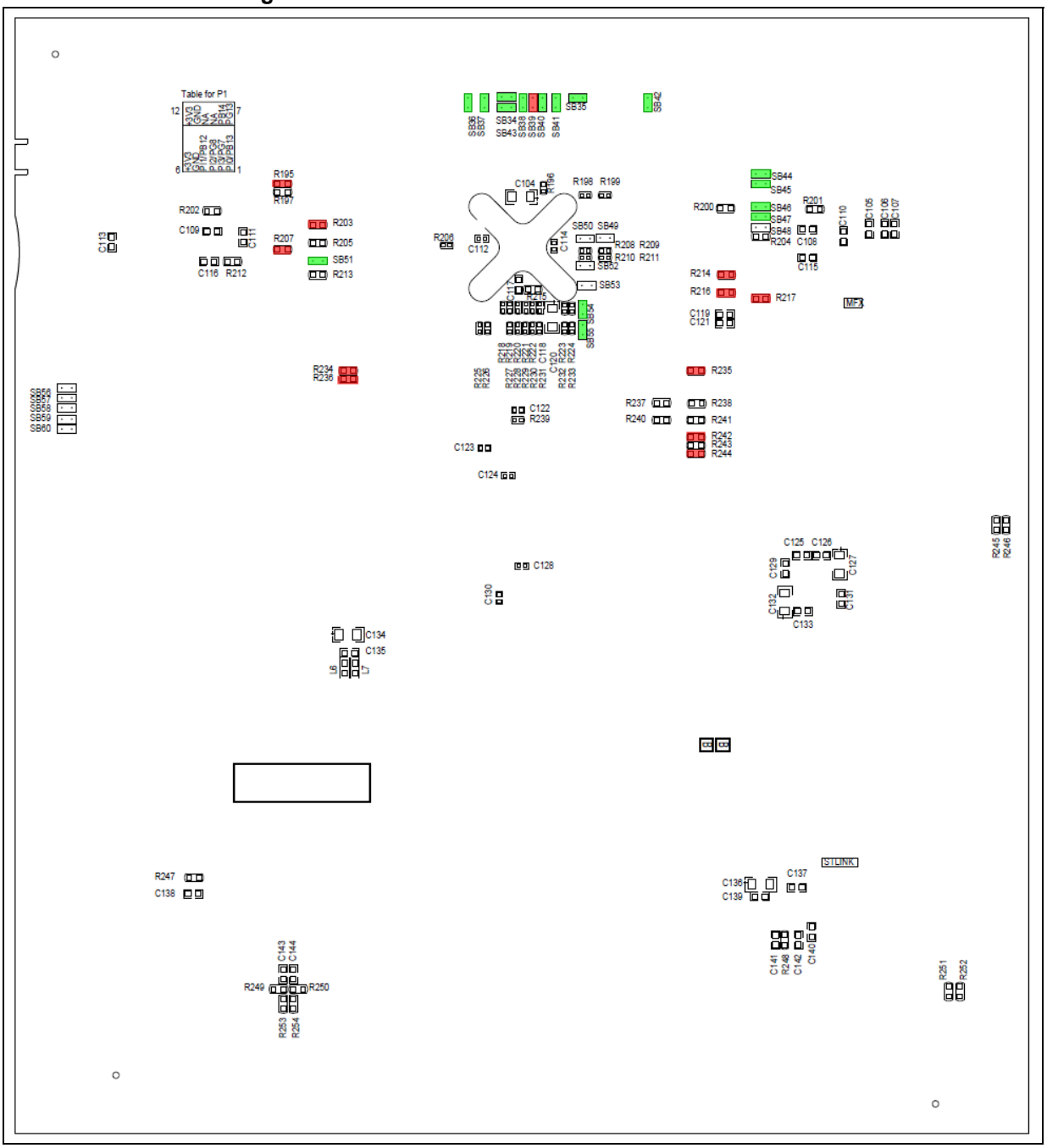


Figure 10. PCB bottom-side rework for motor control



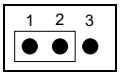
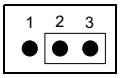
9.14 CAN

The STM32L4R9I-EVAL board supports one CAN2.0A/B channel compliant with CAN specification. The CN22 DB9 male connector is available as CAN interface.

A 3.3 V CAN transceiver is fitted between the CN22 connector and the CAN controller port of STM32L4R9AII6.

The JP14 jumper selects one of high-speed, standby and slope control modes of the CAN transceiver. The JP13 jumper allows to integrate a CAN termination resistor. The JP12 is used to connected CAN transceiver avoiding unknown signals from CAN transceiver.

Table 8. CAN related jumpers

Jumper	Setting	Configuration
JP14		Default setting. CAN transceiver operates in high-speed mode.
		CAN transceiver is in standby mode.
JP13		Default setting. Termination resistor fitted on CAN physical link.
		No termination resistor on CAN physical link.
JP12		Default setting. CAN_TX is not used for CAN transceiver.
		CAN_TX is used from STM32L4R9AII6 termina.l

9.14.1 Limitations

CAN operation is exclusive with Audio codex and MC operation.

9.14.2 Operating voltage

The supply voltage for STM32L4R9I-EVAL CAN operation must be within the range from 3.0 V to 3.6 V.

9.15 Extension connectors CN5, CN6, CN13 and CN14

The CN5, CN6, CN13 and CN14 headers complement to give access to all GPIOs of the STM32L4R9AII6 microcontroller. In addition to GPIOs, the following signals and power supply lines are also routed on CN5 or CN6 or CN13 or CN14:

- GND
- +5 V
- +3.3 V
- D5V
- VDD
- RESET#
- Clock terminals PC14-OSC32_IN, PC15-OSC32_OUT, PH0-OSC_IN, PH1-OSC_OUT

Each header has two rows of 20 pins, with 1.27 mm pitch and 2.54 mm row spacing. For extension modules, SAMTEC RSM-120-02-L-D-xxx and SMS-120-x-x-D are recommendable as SMD and through-hole receptacles, respectively (x is a wild card).

9.16 User LEDs

Four general-purpose color LEDs (LD1, LD2, LD3, LD4) are available as light indicators. Each LED is in light-emitting state with low level of the corresponding ports of STM32L4R9AII6.

And the four LEDs are exclusive with MC operation.

9.17 Physical input devices

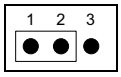
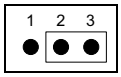
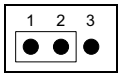
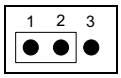
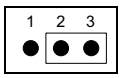
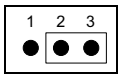
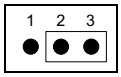
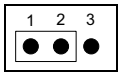
The STM32L4R9I-EVAL board provides a number of input devices for physical human control, listed below:

- four-way joystick controller with select key (B1)
- wake-up/ tamper button (B3)
- reset button (B2)
- 10 kΩ potentiometer (RV2)
- light-dependent resistor, LDR (R121)

The potentiometer and the light-dependent resistor are mutually exclusively rout-able to either PB4 or to PA0 port of STM32L4R9AII6. *Table 9* depicts the setting of associated configuration jumpers.

As illustrated in the schematic diagram in *Figure 30*, the PB4 port is routed, in the STM32L4R9AII6, to the non-inverting input of comparator Comp2. The PA0 is routed to non-inverting input of operational amplifier OpAmp1.

Table 9. Port assignment for control of physical input devices

Jumper	Setting	Routing
JP9		Potentiometer is routed to pin PB4 o fSTM32L4R9AII6.
JP5		
JP9		Default setting. Potentiometer is routed to pin PA0 of STM32L4R9AII6.
JP5		
JP9		LDR is routed to pin PB4 of STM32L4R9AII6.
JP5		
JP9		LDR is routed to pin PA0 of STM32L4R9AII6.
JP5		

9.17.1 Limitations

The potentiometer and the light-dependent resistor are exclusive with MFX, Audio codex, OctoSPIP1, Debugging connector and MC operation. They are mutually exclusive.

9.18 Operational amplifier and comparator

9.18.1 Operational amplifier

STM32L4R9AII6 provides two on-board operational amplifiers, one of which, OpAmp1, is made accessible on STM32L4R9I-EVAL. OpAmp1 has its inputs and its output routed to I/O ports PA0, PA1 and PA3, respectively. The non-inverting input PA0 is accessible on the terminal 1 of the JP5 jumper header. On top of the possibility of routing either of the potentiometer or LDR to PA0, an external source is also connectible to it, using the terminal 1 of JP5.

The PA3 output of the operational amplifier is accessible on test point TP9. Refer to the schematic diagram in *Figure 30.*

The gain of OpAmp1 is determined by the ratio of the variable resistor RV1 and the resistor R246, as shown in the following equation:

Gain = 1 + RV1 / R246

With the RV1 ranging from 0 to 10 kΩ and R246 being 1 kΩ, the gain varies from 1 to 11.

The R108 resistor in series with PA0 is beneficial for reducing the output offset.

Table 10 shows the configuration elements and their settings allowing to access the OpAmp1 function.

Table 10. Configuration elements related with OpAmp1

Element	Setting	Configuration
SB39 SB38 R214	SB38 open SB39 closed R214 out	OpAmp1_INP is routed to pin PA0 of STM32L4R9AII6.
	SB38 open SB39 closed R214 in	Default setting. PA0 port of STM32L4R9AII6 is routed to MFX_IRQ_OUT or motor control signal.
	SB38 closed SB39 open R214 out	PA0 port of STM32L4R9AII6 is routed to motor control signal.
R216 SB40	R216 in SB40 open	Default setting. OpAmp1_INM is routed to pin PA1 of STM32L4R9AII6.
	R216 out SB40 closed	PA1 port of STM32L4R9AII6 is routed to motor control signal.
R215 R221	R215 in R221 out	OpAmp1_VOUT is routed to pin PA3 of STM32L4R9AII6.
	R215 out R221 in	Default setting. OpAmp1_VOUT is not routed to pin PA3 of STM32L4R9AII6. PA3 port of STM32L4R9AII6 is routed to OctoSPI1_CLK.

9.18.2 Comparator

STM32L4R9AII6 provides two on-board comparators, one of which, Comp2, is made accessible on STM32L4R9I-EVAL. Comp2 has its non-inverting input and its output routed to I/O ports PB4 and PB5, respectively. The input is accessible on the terminal 3 of the JP5 jumper header. On top of the possibility of routing either the potentiometer or LDR to PB4, an external source is connectible to it, using the terminal 3 of JP5.

The PB5 output of the comparator is accessible on test point TP6. Refer to the schematic diagram in *Figure 30*.

Table 11 shows the configuration elements and their settings allowing to access the Comp2 function.

Table 11. Configuration elements related with Comp2

Element	Setting	Configuration
R200 SB22	R200 out SB22 closed	Default setting. Comp2_INP is routed to pin PB4 of STM32L4R9AII6.
	R200 in SB22 open	PB4 port of STM32L4R9AII6 is routed to TRST signal.

Table 11. Configuration elements related with Comp2 (continued)

Element	Setting	Configuration
R204 SB48	R204 out SB48 open	Comp2_OUT is routed to pin PB5 of STM32L4R9AII6.
	R204 in SB48 closed	Default setting. Comp2_OUT is not routed to pin PB4 of STM32L4R9AII6. PB4 port of STM32L4R9AII6 is routed to SAI1_SDB.

9.18.3 Limitations

The OpAmp1 is exclusive with MFX, OctoSPIP1, and MC operation.

The Comp2 is exclusive with Debugging connector and SAI1.

9.19 Analog input, output, VREF

STM32L4R9AII6 provides on-board analog-to-digital converter, ADC and digital-to-analog converter, DAC. The port PA4 is configurable to operate either as ADC input or as DAC output. PA4 is routed to the two-way header CN4 allowing to fetch signals to or from PA4 or to ground it by fitting a jumper into CN4.

Parameters of the ADC input low-pass filter formed with R31 and C21 are adjustable by replacing these components according to application requirements. Similarly, parameters of the DAC output low-pass filter formed with R32 and C21 are modifiable by replacing these components according to application requirements.

The VREF+ terminal of STM32L4R9AII6 is used as reference voltage for both ADC and DAC. By default, it is routed to VDDA through a jumper fitted into the two-way header CN10. The jumper is removable and an external voltage applied to the terminal 1 of CN10, for specific purposes.

9.20 SRAM device

IS61WV102416BLL, a 16-Mbit static RAM (SRAM), 1 M x 16 bit, is fitted on the STM32L4R9I-EVAL main board, in U17 position. The STM32L4R9I-EVAL main board, as well as the addressing capabilities of FMC, allow hosting SRAM devices up to 64 Mbytes. This is the reason why the schematic diagram in *Figure 26* mentions several SRAM devices.

The SRAM device is attached to the 16-bit data bus and accessed with FMC. The base address is 0x6000 0000, corresponding to NOR/SRAM1 bank1. The SRAM device is selected with FMC_NE1 chip select. FMC_NBL0 and FMC_NBL1 signals allow selecting 8-bit and 16-bit data word operating modes.

By removal of R134, a zero-ohm resistor, the SRAM is deselected and the STM32L4R9AII6 ports PD7, PE0 and PE1 corresponding to FMC_NE1, FMC_NBL0 and FMC_NBL1 signals, respectively, are usable for other application purposes.

Table 12. SRAM chip select configuration

Resistor	Fitting	Configuration
R134	In	Default setting. SRAM chip select is controlled with FMC_NE1
	Out	SRAM is deselected. FMC_NE1 is freed for other application purposes.

9.20.1 Limitations

The SRAM addressable space is limited if some or all of A21 FMC address lines is shunted to the CN12 connector for debug trace purposes. In such a case, the disconnected addressing inputs of the SRAM device are pulled down by resistors. *Section 9.4* provides information on the associated configuration elements.

9.20.2 Operating voltage

The SRAM device operating voltage is in the range from 2.4 V to 3.6 V.

9.21 NOR Flash memory device

M29W128GL70ZA6E, a 128-Mbit NOR Flash memory, 8 M x16 bit, is fitted on the STM32L4R9I-EVAL main board, in U11 position. The STM32L4R9I-EVAL main board, as well as the addressing capabilities of FMC, allow hosting M29W256GL70ZA6E, a 256-Mbit NOR Flash memory device. This is the reason why the schematic diagram in *Figure 26* mentions both devices.

The NOR Flash memory device is attached to the 16-bit data bus and accessed with FMC. The base address is 0x6800 0000, corresponding to NOR/SRAM2 bank1. The NOR Flash memory device is selected with FMC_NE3 chip select signal. 16-bit data word operation mode is selected by a pull-up resistor connected to BYTE terminal of NOR Flash memory. The jumper JP6 is dedicated for write protect configuration.

By default, the FMC_NWAIT signal is not routed to RB port of the NOR Flash memory device, and, to know its ready status, its status register is polled by the demo software fitted in STM32L4R9I-EVAL. This is modifiable with configuration elements, as shown in *Table 13*.

Table 13. NOR Flash memory related jumper

Jumper	Setting	Configuration
JP6		Default setting. NOR Flash memory write is enabled.
		NOR Flash memory write is inhibited. Write protect is activated.

9.21.1 Limitations

The NOR Flash memory device's addressable space is limited if some or all of A21, A22 and A23 FMC address lines are shunted to the CN12 connector for debug trace purposes. In such

a case, the disconnected addressing inputs of the NOR Flash memory device are pulled down by resistors. *Section 9.4* provides information on the associated configuration elements.

9.21.2 Operating voltage

NOR Flash memory operating voltage must be in the range from 1.65 V to 3.6 V.

9.22 EEPROM

M24128-DFDW6TP, a 128-Kbit I²C-bus EEPROM device, is fitted on the main board of STM32L4R9I-EVAL, in U3 position. It is accessed with I²C-bus lines I2C2_SCL and I2C2_SDA of STM32L4R9AII6. It supports all I²C-bus modes with speeds up to 1 MHz. The base I²C-bus address is 0xA0. Write-protecting the EEPROM is possible through opening the SB13 solder bridge. By default, SB13 is closed and writing into the EEPROM enabled.

9.22.1 Operating voltage

The M24128-DFDW6TP EEPROM device's operating voltage must be in the range from 1.7 V to 3.6 V

9.23 EXT_I2C connector

EXT_I2C CN2 connected to I²C bus daughterboard is possible. MFX_GPIO8 of MFX MCU provides EXT_RSET signal, and solder bridge SB12 is used to connector +5 V power supply for daughterboard.

9.24 Octo-SPI Flash memory device

MX25LM51245GXDI00, a 512-Mbit Octo-SPI Flash memory device, is fitted on the STM32L4R9I-EVAL main board, in U6 position. It allows evaluating STM32L4R9AII6 Octo-SPI interface.

MX25LM51245GXDI00 operates in single transfer rate (STR) or double transfer rate (DTR) mode.

Table 14 shows the configuration elements and their settings allowing to access the Octo-SPI Flash memory device.

Table 14. Configuration elements related with Octo-SPI Flash device

Element	Setting	Configuration
R221 R215	R221 in R215 out	Default setting. OctoSPI1_CLK is available at Octo-SPI Flash memory device.
	R221 out R215 in	OctoSPI1_CLK is not available at Octo-SPI Flash memory device. PA3 port of STM32L4R9AII6 is routed to OpAmp1_Vout signal.

Table 14. Configuration elements related with Octo-SPI Flash device (continued)

Element	Setting	Configuration
R67 SB54	R67 in SB54 open	Default setting. OctoSPI1_IO6 data line is available at Octo-SPI Flash memory device.
	R67 out SB54 closed	OctoSPI1_IO6 is not available at Octo-SPI Flash memory device. PC3 port of SSTM32L4R9AII6 is routed to motor control signal.
R75 SB55	R75 in SB55 open	Default setting. OctoSPI1_IO7 data line is available at Octo-SPI Flash memory device.
	R75 out SB55 closed	OctoSPI1_IO7 is not available at Octo-SPI Flash memory device. PC4 port of STM32L4R9AII6 is routed to motor control signal.

9.24.1 Limitations

Octo-SPI Flash memory device operation is exclusive with OpAmp1 and with motor control.

9.24.2 Operating voltage

Voltage of Octo-SPI Flash memory device MX25LM51245GXDI00 is in the range of 2.7 V to 3.6 V.

9.25 Octo-SPI DRAM device

IS66WVH8M8BLL-100BLI, a 64-Mbit self-refresh dynamic RAM (DRAM) device with a HyperBus interface, is fitted on the STM32L4R9I-EVAL main board, in U5 position. It allows evaluating STM32L4R9AII6 Octo-SPI interface.

9.25.1 Operating voltage

Voltage of Octo-SPI DRAM device IS66WVH8M8BLL-100BLI is in the range of 2.7 V to 3.6 V.

9.26 Touch-sensing button

The STM32L4R9I-EVAL board supports a touch sensing button based on either RC charging or on charge-transfer technique. The latter is enabled, by default.

The touch sensing button is connected to PC6 port of STM32L4R9AII6 and the related charge capacitor is connected to PC7.

An active shield is designed in the layer 2 of the main PCB, under the button footprint. It allows reducing disturbances from other circuits to prevent from false touch detections.

The active shield is connected to PB6 port of STM32L4R9AII6 through the resistor R22. The related charge capacitor is connected to PB7.

Table 15 shows the configuration elements related with the touch sensing function. Some of them serve to enable or disable its operation. However, most of them serve to optimize the

touch sensing performance, by isolating copper tracks to avoid disturbances due to their antenna effect.

Table 15. Touch-sensing-related configuration elements

Element	Setting	Configuration
R44	In	PC6 port is routed to CN6 connector for daughterboard. This setting is not good for robustness of touch sensing.
	Out	Default setting. PC6 port is cut from CN6.
SB21	Open	Default setting. PC6 is not routed to motor control.
	Closed	PC6 is routed to motor control. This setting is not good for robustness of touch sensing.
R46	In	PC7 port is routed to CN6 connector for daughterboard. This setting is not good for robustness of touch sensing.
	Out	Default setting. PC7 port is cut from CN6.
SB19	Open	Default setting. PC7 is not routed to motor control.
	Closed	PC7 is routed to motor control. This setting is not good for robustness of touch sensing.
SB20	Open	PC7 is not routed to sampling capacitor. Touch sensing cannot operate.
	Closed	Default setting. PC7 is routed to sampling capacitor. Touch sensing available.
R26	In	PB6 port is routed to CN5 connector for daughterboard. This setting is not good for robustness of touch sensing.
	Out	Default setting. PB6 port is cut from CN5.
SB14	Open	Default setting. PB6 is not routed to motor control.
	Closed	PB6 is routed to motor control. This setting is not good for robustness of touch sensing.
SB15	Open	PB6 is not routed to active shield under the touch sensing button. This setting is not good for robustness of touch sensing.
	Closed	Default setting. PB6 is routed to active shield under the touch sensing button. This setting is not good for robustness of touch sensing.
SB16	Open	Default setting. PB6 is not routed to CN16 DSI display connector.
	Closed	PB6 is routed to CN16 DSI display connector. This setting is not good for robustness of touch sensing.

Table 15. Touch-sensing-related configuration elements (continued)

Element	Setting	Configuration
R30	In	PB7 port is routed to CN5 connector for daughterboard. This setting is not good for robustness of touch sensing.
	Out	Default setting. PB7 port is cut from CN5.
SB17	Open	Default setting. PB7 is not routed to motor control.
	Closed	PB7 is routed to motor control. This setting is not good for robustness of touch sensing.
SB18	Open	PB7 is not routed to sampling capacitor of the active shield under the touch sensing button. This setting is not good for robustness of touch sensing.
	Closed	Default setting. PB6 is routed to sampling capacitor of the active shield under the touch sensing button. This setting is not good for robustness of touch sensing.

9.26.1 Limitations

Touch sensing button is exclusive with DSI display connector, motor-control and daughterboard connector.

9.27 MFX MCU

The MFX MCU is used as MFX (multi function expander) and IDD measurement.

The MFX circuit on STM32L4R9I-EVAL board acts as IO-expander. The communication interface between MFX and STM32L4R9AII6 is I2C2 bus. The signals connected to MFX are listed in *Table 16*.

Table 16. MFX signals

Pin number of MFX	Pin name of MFX	MFX functions	Function of STM32L4R9AII6	Direction (for MFX)	Terminal device
15	PA5	MFX_GPIO5	uS_Detect	Input	microSD
16	PA6	MFX_GPIO6	USB _PSON	Output	USB_FS
17	PA7	MFX_GPIO7	USB_OVRCR	Input	USB_FS
18	PB0	MFX_GPIO0	JOY_SEL	Input	Joystick
19	PB1	MFX_GPIO1	JOY_DOWN	Input	Joystick
20	PB2	MFX_GPIO2	JOY_LEFT	Input	Joystick
26	PB13	MFX_GPIO13	-	-	-
27	PB14	MFX_GPIO14	-	-	-
28	PB15	MFX_GPIO15	-	-	-

Table 16. MFX signals (continued)

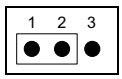
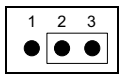
Pin number of MFX	Pin name of MFX	MFX functions	Function of STM32L4R9AII6	Direction (for MFX)	Terminal device
29	PA8	MFX_GPIO8	EXT_RESET	Output	EXT_I2C
30	PA9	MFX_GPIO9	DSI_RST	Output	DSI LCD
31	PA10	MFX_GPIO10	-	-	-
32	PA11	MFX_GPIO11	LCD_DISP	Output	TFT LCD
33	PA12	MFX_GPIO12	LCD_RST	Output	TFT LCD
39	PB3	MFX_GPIO3	JOY_RIGHT	Input	Joystick
40	PB4	MFX_GPIO4	JOY_UP	Input	Joystick

9.28 IDD measurement

STM32L4R9AII6 has a built-in circuit allowing to measure its own current consumption (IDD) in Run and Low-power modes, except for Shutdown mode. It is strongly recommended that the MCU supply voltage (VDD_MCU line) does not exceed 3.3 V. This is because there are components on STM32L4R9I-EVAL supplied from 3.3 V that communicate with the MCU through I/O ports. Voltage exceeding 3.3 V on the MCU output port may inject current into 3.3 V-supplied peripheral I/Os and false the MCU current consumption measurement.

Table 17 shows settings of jumper associated with the IDD measurement on the board.

Table 17. IDD measurement related jumper setting

Jumper	Setting	Configuration
JP4		Default setting. STM32L4R9AII6 has a built-in circuit allowing to measure its own current consumption.
		IDD measurement is not available, bypass mode only for STM32L4R9AII6 VDD_MCU power supply.

9.29 DSI display (MIPI) connector

The CN16 connector is designed to connect DSI display daughterboard. MB1314 daughterboard is available to mount on STM32L4R9I-EVAL board. *Table 18* shows the assignment of CN16 and STM32L4R9AII6 terminals.

Table 18. DSI display module connector CN16

Pin No.	Description	Pin connection	Pin No.	Description	Pin connection
1	GND	-	2	-	-
3	DSI_CK_P	-	4	DSI_INT	PC2
5	DSI_CK_N	-	6	GND	-

Table 18. DSI display module connector CN16 (continued)

Pin No.	Description	Pin connection	Pin No.	Description	Pin connection
7	GND	-	8	RFU	GND
9	DSI_D0_P	-	10	RFU	GND
11	DSI_D0_N	-	12	GND	-
13	GND	-	14	RFU	GND
15	DSI_D1_P	-	16	RFU	GND
17	DSI_D1_N	-	18	GND	-
19	GND	-	20	-	-
21	BLVDD (5 V)	-	22	SPI_CS	PG12
23	BLVDD (5 V)	-	24	SPI_CLK/UART_CK	PI1/PG13
25	-	-	26	SPI_SDI/UART_TX	PI3/PB6
27	BLGND	-	28	SPI_DCX	PI2
29	BLGND	-	30	-	-
31	-	-	32	-	-
33	-	-	34	-	-
35	SCLK/MCLK	PA8	36	3.3 V	-
37	LRCLK	PB9	38	VDD	-
39	I2S_DATA	PC1	40	I2C_SDA	PH5
41	-	-	42	-	-
43	SWIRE	PG6	44	I2C_SCL	PH4
45	CEC_CLK	NA	46	-	-
47	CEC	NA	48	-	-
49	DSI_TE	PF11	50	-	-
51	-	-	52	-	-
53	DSI_BL_CTRL	PB14	54	-	-
55	-	-	56	-	-
57	DSI_RST	MFX_GPIO9	58	-	-
59	-	-	60	1.8 V	-

9.29.1 Limitations

The DSI display module connector signal INT is used both for TFT LCD and DSI display connector.

9.30 TFT LCD (RGB and FMC mode) connector

The 50-pin 1.27 mm-pitch female connector CN20 is designed to connect TFT LCD daughterboard, supporting RGB and FMC modes. MB1315 daughterboard is available to

mount on STM32L4R9I-EVAL board with RGB mode. *Table 19* shows the assignment of CN20 and STM32L4R9AII6 terminals.

Table 19. TFT LCD module connector CN20

Pin No.	RGB mode description	FMC mode description	Pin connection	Pin No.	RGB mode description	FMC mode description	Pin connection
1	GND	GND	-	2	GND	GND	-
3	R0	-	PE2	4	G0	-	PF14
5	R1	RS(A19)	PE3	6	G1	-	PF15
7	R2	D12	PE15	8	G2	D6	PE9
9	R3	D13	PD8	10	G3	D7	PE10
11	R4	D14	PD9	12	G4	D8	PE11
13	R5	D15	PD10	14	G5	D9	PE12
15	R6	-	PD11	16	G6	D10	PE13
17	R7	-	PD12	18	G7	D11	PE14
19	GND	GND	-	20	GND	GND	-
21	B0	-	PE4	22	DE	TE	PF11
23	B1	-	PF13	24	LCD_DSIP	-	MFX_ GPIO11
25	B2	D0	PD14	26	HSYNC	-	PE0
27	B3	D1	PD15	28	VSYNC	-	PE1
29	B4	D2	PD0	30	GND	GND	-
31	B5	D3	PD1	32	PCLK	-	PD3
33	B6	D4	PE7	34	GND	GND	-
35	B7	D5	PE8	36	RST#	RST#	MFX_ GPIO12
37	GND	GND	-	38	SDA	SDA	PH5
39	INT	INT	PC2	40	SCL	SCL	PH4
41	-	RS	PE2	42	-	NOE	PD4
43	BL_CTRL	BL_CTRL	PA5	44	-	NWE	PD5
45	BL+5 V	BL+5 V	-	46	-	CS	PG12
47	BLGND	BLGND	-	48	VDD	VDD	-
49	BLGND	BLGND	-	50	+3.3 V	+3.3 V	-

9.30.1 Limitations

The TFT LCD module connector supports RGB mode or FMC mode only on the same time. The signal INT is used both for TFT LCD and DSI display connector. When RGB mode TFT LCD used, STM32L4R9AII6 cannot access SRAM and NOR Flash memory on board.

9.31 PMOD connector

The standard PMOD connector P1 is available on STM32L4R9I-EVAL board to support flexibility in small form factor application. The PMOD connector is implemented the PMOD type 2A and 4A on STM32L4R9I-EVAL board.

Table 20. PMOD connector P1

Pin number	Description	Pin number	Description
1	SS/CTS (PI0/PB13)	7	INT (PG13)
2	MOSI/TXD (PI3/PG7)	8	RESET (PB14)
3	MISO/RXD (PI2/PG8)	9	-
4	SCK/RTS (PI1/PB12)	10	-
5	GND	11	GND
6	3.3 V	12	3.3 V

9.32 MB1314 DSI display board

MB1314 is DSI display daughterboard which are available to mount on STM32L4R9I-EVAL board via connector CN1. GVO IEG1120TB103GF-001 is selected for round LCD with one data lane, 390x390 resolution, 24 bpp with capacitive touch panel (FocalTech FT3x67 driver). *Table 21* shows MB1314 board connector CN1 pin function description.

Table 21. MB1314 board connector CN1 pin function description

Pin number	Description	Pin number	Description
1	GND	2	-
3	DSI_CK_P	4	DSI_INT
5	DSI_CK_N	6	GND
7	GND	8	RFU
9	DSI_D0_P	10	RFU
11	DSI_D0_N	12	GND
13	GND	14	RFU
15	RFU	16	RFU
17	RFU	18	GND
19	GND	20	-
21	BLVDD (5 V)	22	RFU
23	BLVDD (5 V)	24	RFU
25	-	26	RFU
27	BLGND	28	RFU
29	BLGND	30	-
31	-	32	-

Table 21. MB1314 board connector CN1 pin function description (continued)

Pin number	Description	Pin number	Description
33	-	34	-
35	RFU	36	3.3 V
37	RFU	38	VDD
39	RFU	40	I2C_SDA
41	-	42	-
43	SWIRE	44	I2C_SCL
45	RFU	46	-
47	RFU	48	-
49	DSI_TE	50	-
51	-	52	-
53	DSI_BL_CTRL	54	-
55	-	56	-
57	DSI_RST	58	-
59	-	60	RFU

Warning: Permanent Image sticking may occur if AMOLED displays same image for an extended period of time.

9.33 MB1315 TFT LCD board

MB1315 is TFT LCD daughterboard supporting RGB mode, available to mount on STM32L4R9I-EVAL board via connector CN1.

The 4.3” TFT LCD is used LCD RK043FN48H-CT672B with capacitive touch panel which only supports 3.3 V power and interface. So a level shifter SN74LVC16T245DGGR is requested on TFT RGB LCD daughterboard to support wide power supply range. *Table 22* shows MB1315 board connector CN1 pin function description.

Table 22. MB1315 board connector CN1 pin function description

Pin number	Description	Pin number	Description
1	GND	2	GND
3	R0	4	G0
5	R1	6	G1
7	R2	8	G2
9	R3	10	G3
11	R4	12	G4

Table 22. MB1315 board connector CN1 pin function description (continued)

Pin number	Description	Pin number	Description
13	R5	14	G5
15	R6	16	G6
17	R7	18	G7
19	GND	20	GND
21	B0	22	DE
23	B1	24	LCD_DSIP
25	B2	26	HSYNC
27	B3	28	VSYNC
29	B4	30	GND
31	B5	32	PCLK
33	B6	34	GND
35	B7	36	RST#
37	GND	38	SDA
39	INT	40	SCL
41	-	42	-
43	BL_CTRL	44	-
45	BL+5 V	46	-
47	BLGND	48	VDD
49	BLGND	50	+3.3 V

10 Connectors

10.1 Motor-control connector CN1

Figure 11. Motor-control connector CN1 (top view)

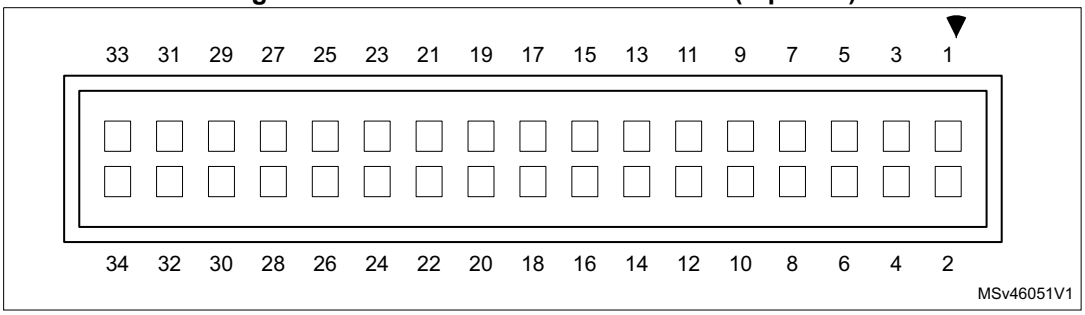


Table 23. Motor-control connector CN1

Description	Pin of STM32L4R9AII6	Pin number of CN1	Pin number of CN1	Pin of STM32L4R9AII6	Description
Emergency STOP	PI4	1	2	-	GND
PWM_1H	PC6	3	4	-	GND
PWM_1L	PH13	5	6	-	GND
PWM_2H	PC7	7	8	-	GND
PWM_2L	PH14	9	10	-	GND
PWM_3H	PC8	11	12	-	GND
PWM_3L	PH15	13	14	PC4	BUS VOLTAGE
CURRENT A	PC0	15	16	-	GND
CURRENT B	PC1	17	18	-	GND
CURRENT C	PC2	19	20	-	GND
ICL Shutout	PG9	21	22	-	GND
DISSIPATIVE BRAKE	PG13	23	24	PA0	PCD Ind. Current
+5 V power	-	25	26	PA1	Heatsink temperature
PFC SYNC	PB14	27	28	-	3.3 V power
PFC PWM	PB15	29	30	PA9	PFC Shut Down
Encoder A	PB6	31	32	PC3	PFC Vac
Encoder B	PB7	33	34	PB8	Encoder Index

10.2 External I²C connector CN2

Figure 12. EXT_I2C connector CN2 (front view)

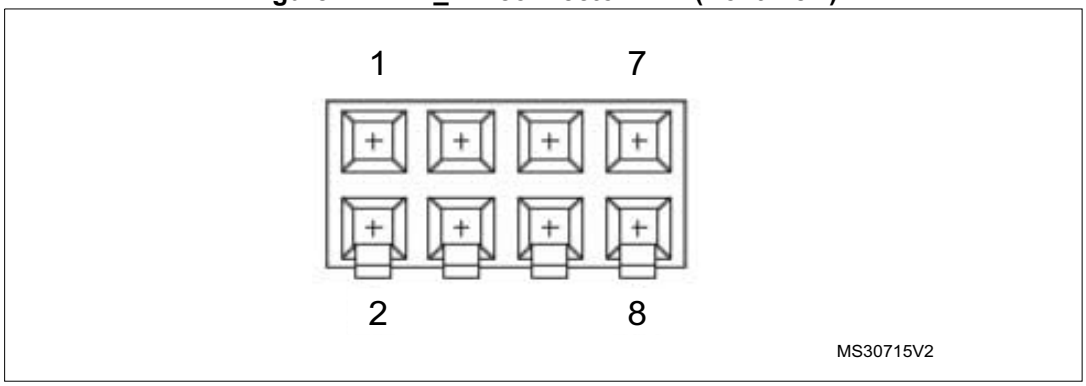


Table 24. EXT_I2C connector CN2

Pin number	Description	Pin number	Description
1	I2C1_SDA (PH5)	5	VDD
2	NC	6	NC
3	I2C_SCL (PH4)	7	GND
4	EXT_RESET (MFX_GPIO8)	8	NC

10.3 USB OTG FS Micro-AB connector CN3

Figure 13. USB OTG FS Micro-AB connector CN3 (Front view)

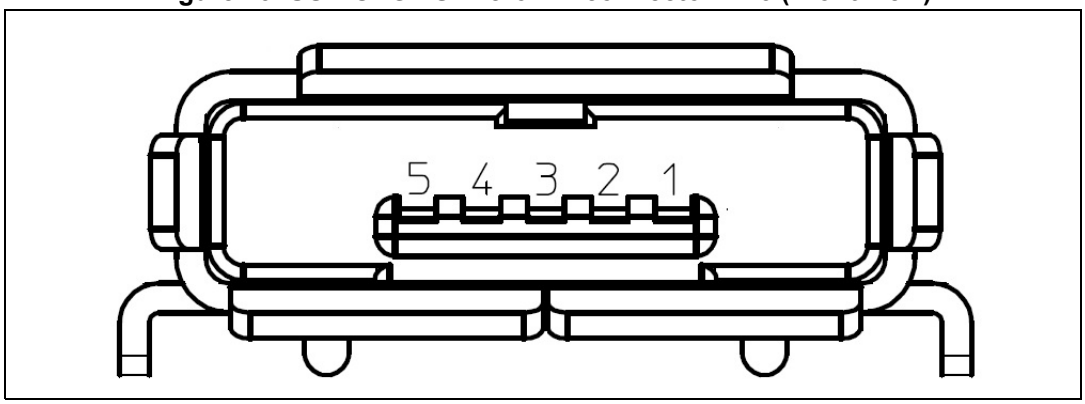


Table 25. USB OTG FS Micro-AB connector CN3

Pin number	Description	Pin number	Description
1	VBUS (PA9)	4	ID (PA10)
2	DM (PA11)	5	GND
3	DP (PA12)	-	-

10.4 Analog input-output connector CN4

Figure 14. Analog input-output connector CN4 (top view)

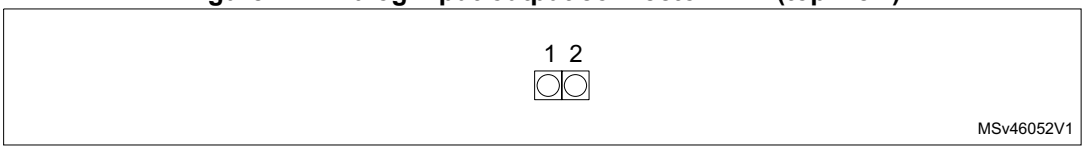


Table 26. Analog input-output connector CN4

Pin number	Description	Pin number	Description
1	GND	2	Analog input-output PA4

10.5 Extension connectors CN5, CN6, CN13 and CN14

All GPIO signals from STM32L4R9AII6 are connected to extension connectors CN5, CN6, CN13 and CN14. Extension connectors CN13 and CN14 is also used for FMC device.

Table 27. Daughter board extension connector CN5

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
1	PH9	OCTO-SPI2_IO4	Remove the U5.
3	PH14	LED3, MC	Remove R185, open SB44.
5	PH15	LED4, MC	Remove R184, open SB45.
7	PI3	SPI2_MOSI	No connection for CN16 and P1.
9	GND	-	-
11	PH13	LED2, MC	Remove R186, open SB46.
13	PG13	PMOD_INT, USART1_CK, MC	Open SB29, SB47. No connection for P1.
15	PB5	SAI1_SDB, Comp2_OUT	Remove R204, open SB48.
17	PI9	OCTO-SPI2_IO2	Remove the U5.
19	PI11	OCTO-SPI2_IO0	Remove the U5.
21	NC	-	-
23	PC14	OSC32_IN	Remove R50, close SB50.
25	PC13	Wakeup	Remove R188.
27	PH1	OSC_OUT	Remove R65, close SB53.
29	GND	-	-
31	PA5	TFT LCD_BL_CTRL	No connection for CN20.
33	PC2	DSI LCD_INT, TFT LCD_INT, MC	Remove R217, open SB43.
35	PH8	OCTO-SPI2_IO3	Remove the U5.

Table 27. Daughter board extension connector CN5 (continued)

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
37	PH10	OCTO-SPI2_IO5	Remove the U5.
39	D5V	-	-
2	PI5	OCTO-SPI2_NCS	Remove the U5.
4	PH12	OCTO-SPI2_IO7	Remove the U5.
6	PI6	OCTO-SPI2_CLK	Remove the U5.
8	PG15	OCTO-SPI2_DQS	Remove the U5.
10	GND	-	-
12	PB4	Comp2_INP, TRST	Remove R200, open SB22.
14	PB6	TS_SHIELD, USART1_TX, MC	Closed R26, open SB14, SB16 and SB15.
16	PB7	TS_SHIELD_CS, MC	Closed R30, open SB17 and SB18.
18	PI10	OCTO-SPI2_IO1	Remove the U5.
20	PI7	-	-
22	PH3	BOOT0	Remove R1.
24	PC15	OSC32_OUT	Remove R49, close SB49.
26	PH0	OSC_IN	Remove R61, close SB52.
28	PA0	MFX_IRQ_OUT, OpAmp1_INP, MC	Remove R214, open SB38 and SB39.
30	GND	-	-
32	PA1	OpAmp1_INM, MC	Remove R216, open SB40.
34	PA4	ADC_DAC	Remove R32.
36	PH11	OCTO-SPI2_IO6	Remove the U5.
38	VDD	-	-
40	+3V3	-	-

Table 28. Daughter board extension connector CN6

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
1	PH2	OCTO-SPI1_IO4	Remove the U6.
3	PI0	SPI2_NSS	No connection for P1.
5	PD2	SDIO1_CMD	Remove R55, no SD card insert.
7	PI1	SPI2_SCK	No connection for CN16 and P1.
9	GND	-	-
11	PA12	USB OTG_DP	No connection for the CN3.
13	PA11	USB OTG_DM	No connection for the CN3.

Table 28. Daughter board extension connector CN6 (continued)

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
15	PG8	LPUART1_RX	Remove the U9.
17	PA9	VBUS_FS, MC	Remove R203, open SB35.
19	PC9	SDIO1_D1, Trace_D0	Remove R205, open SB57.
21	PC7	TS_KEY_CS, MC	Closed R46, open SB19 and SB20.
23	PB15	LED1, MC	Remove R187, open SB51.
25	PB13	LPUART1_CTS	Remove the U9.
27	RESET#	-	-
29	GND	-	-
31	PA3	OpAmp1_VOUT, OCTO-SPI1_CLK	Remove R221, R215.
33	PA7	OCTO-SPI1_IO2	Remove the U6.
35	PC4	OCTO-SPI1_IO7, MC	Remove R75, open SB55.
37	PC3	OCTO-SPI1_IO6, MC	Remove R67, open SB54.
39	D5V	-	-
2	PG11	OCTO-SPI1_IO5	Remove the U6.
4	PI2	SPI2_MISO	No connection for CN16 and P1.
6	PC8	SDIO1_D0, MC	Remove R195, open SB2.
8	PC10	SDIO1_D2, Trace_D1	Remove R197, open SB58.
10	GND	-	-
12	PC11	SDIO1_D3	Remove R60, no SD card insert.
14	PC12	SDIO1_CLK	no SD card insert.
16	PA10	USB OTG_ID	No connection for the CN3.
18	PC6	TS_KEY, MC	Closed R44, open SB21.
20	PG7	LPUART1_TX	Remove R19 and U1.
22	PB14	DSI LCD_BL_CTRL, PMOD_RST, MC	Remove R207, open SB41. No connection for P1.
24	PB12	LPUART1_RTS	Remove R5 and U1.
26	PF11	DSI LCD_TE, TFT LCD_DE	No connection for CN16 and CN20.
28	PB0	OCTO-SPI1_IO1	Remove the U6.
30	GND	-	-
32	PB1	OCTO-SPI1_IO0	Remove the U6.
34	PB2	OCTO-SPI1_DQS	Remove the U6.
36	PA6	OCTO-SPI1_IO3	Remove the U6.

Table 28. Daughter board extension connector CN6 (continued)

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
38	PA2	OCTO-SPI1_NCS	Remove the U6.
40	+5V	-	-

Table 29. Daughter board extension connector CN13

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
1	PD1	FMC_D3	-
3	PD0	FMC_D2	-
5	PB8	SAI1_MCLKA, CAN_RX, MC	Remove R235, open SB42 and JP12.
7	PG10	FMC_NE3	-
9	GND	-	-
11	PE0	FMC_NBL0	-
13	PG12	FMC_NE4, SPI	Remove R238, open SB26.
15	PE4	FMC_A20	-
17	PE5	FMC_A21	Keep the CN12 open.
19	PF1	FMC_A1	-
21	PF2	FMC_A2	-
23	PB9	SAI1_FSA, CAN_TX	Remove R243, R247.
25	PF10	DFSDM_CLK	Open JP16.
27	PF5	FMC_A5	-
29	GND	-	-
31	PF4	FMC_A4	-
33	PF15	FMC_A9	-
35	PG0	FMC_A10	-
37	PE10	FMC_D7	-
39	VDD	-	-
2	NC	-	-
4	PD6	FMC_NWAIT	-
6	PD4	FMC_NOE	-
8	PE1	FMC_NBL1	-
10	GND	-	-
12	PD5	FMC_NWE	-
14	PE2	FMC_A23	Keep the CN12 open.
16	PE3	FMC_A19	-

Table 29. Daughter board extension connector CN13 (continued)

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
18	PE6	FMC_A22	Keep the CN12 open.
20	PF0	FMC_A0	-
22	PC0	DFSDM, MC	Remove R242, open SB36.
24	PC1	SAI1, MC	Remove R244, open SB37.
26	PF3	FMC_A3	-
28	PG4	FMC_A14	-
30	GND	-	-
32	PG1	FMC_A11	-
34	PF12	FMC_A6	-
36	PF13	FMC_A7	-
38	PF14	FMC_A8	-
40	+3V3	-	-

Table 30. Daughter board extension connector CN14

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
1	PA14	JTAG_TCK/SWCLK	Do not use the CN11, CN12, CN15, CN17 for debug connecto.r
3	PD7	FMC_NE1	-
5	PD3	TFT LCD_CLK	No connection for CN20.
7	PB3	JTAG_TDO/SWO	Do not use the CN11, CN12, CN15, CN17 for debug connector.
9	GND	-	-
11	PG5	FMC_A15	-
13	PD15	FMC_D1	-
15	PD14	FMC_D0	-
17	PD10	FMC_D15	-
19	PH5	I2C2_SDA	Remove R2.
21	PB10	UART3_TX	Remove R173, no connection for the CN11.
23	PD8	FMC_D13	-
25	PD13	FMC_A18	-
27	PE12	FMC_D9	-
29	GND	-	-
31	NC	-	-
33	PE7	FMC_D4	-

Table 30. Daughter board extension connector CN14 (continued)

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
35	PE14	FMC_D11	-
37	PE15	FMC_D12	-
39	VDD	-	-
2	PA13	JTAG_TMS/SWDIO	Do not use the CN11, CN12, CN15, CN17 for debug connector.
4	PA15	JTAG_TDI	Do not use the CN11, CN12, CN15, CN17 for debug connector.
6	PI4	Audio_INT, MC	Remove R234, open SB3.
8	PG9	MFX_WAKUP, MC	Remove R236, open SB34.
10	GND	-	-
12	PA8	SAI1_SCKA	Remove the U26.
14	PG3	FMC_A13	-
16	PG6	DSI LCD_SWIRE	No connection for the CN16.
18	PG2	FMC_A12	-
20	PD11	FMC_A16	-
22	PH4	I2C2_SCL	Remove R3.
24	PB11	UART3_RX	Remove R171, no connection for the CN11.
26	PD9	FMC_D14	-
28	PD12	FMC_A17	-
30	GND	-	-
32	PE13	FMC_D10	-
34	PE8	FMC_D5	-
36	PE11	FMC_D8	-
38	PE9	FMC_D6	-
40	+3V3	-	-

10.6 RS232 connector CN7

Figure 15. RS232 D-sub male connector (front view)

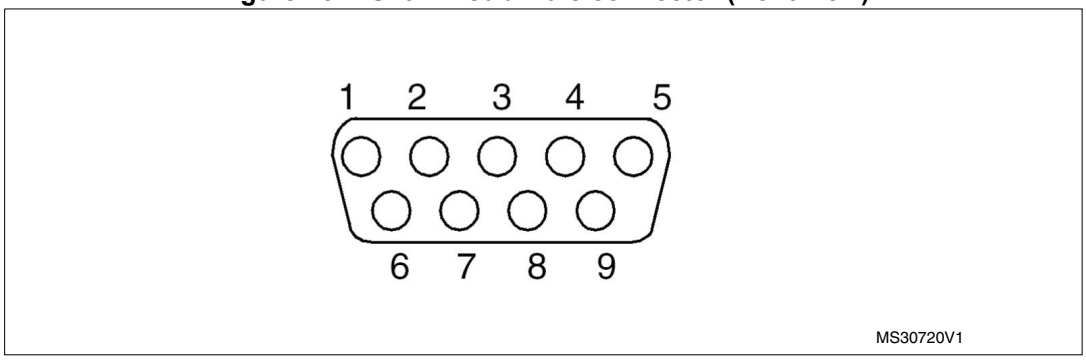


Table 31. RS232 D-sub male connector

Pin number	Description	Pin number	Description
1	NC	6	NC
2	RS232_RX (PG8)	7	RS232_RTS (PB12)
3	RS232_TX (PG7)	8	RS232_CTS (PB13)
4	NC	9	NC
5	GND	-	-

10.7 microSD connector CN8

Figure 16. microSD connector CN8 (top view)

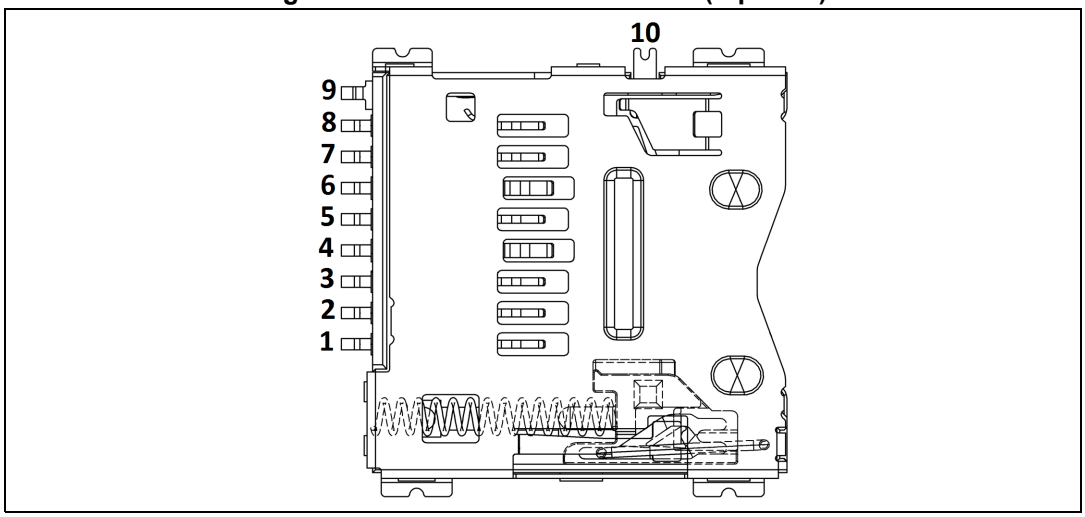


Table 32. microSD connector CN8

Pin number	Description	Pin number	Description
1	SDIO_D2 (PC10)	6	Vss/GND
2	SDIO_D3 (PC11)	7	SDIO_D0 (PC8)
3	SDIO_CMD (PD2)	8	SDIO_D1 (PC9)
4	VDD	9	GND
5	SDIO_CLK (PC12)	10	MicroSDcard_detect (MFX GPIO15)

10.8 MFX programming connector CN9

The connector CN9 is used only for embedded MFX (multi function expander) programming during board manufacture. It is not populated by default and not for end user.

10.9 STDC14 connector CN11

Figure 17. STDC14 debugging connector CN11 (top view)

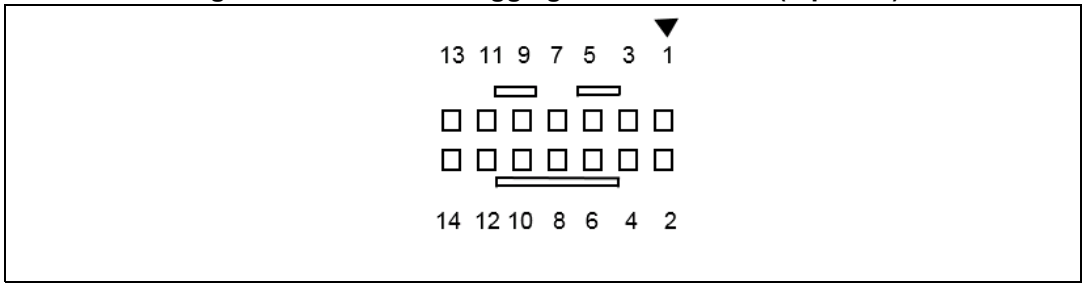


Table 33. STDC14 debugging connector CN11

Terminal	Function / MCU port	Terminal	Function / MCU port
1	-	2	-
3	VDD	4	SWDIO/TMS (PA13)
5	GND	6	SWDCLK/TCK (PA14)
7	GND	8	SWO/TDO (PB3)
9	KEY	10	TDI (PA15)
11	GND	12	RESET#
13	VCP_RX (PB11)(1)	14	VCP_TX (PB10)(1)

1. Due to discrepancies between port terminal and sheet symbol, VCP_RX and VCP_TX are not connected to MCU

10.10 Trace debugging connector CN12

Figure 18. ETM trace debugging connector CN12 (Top view)

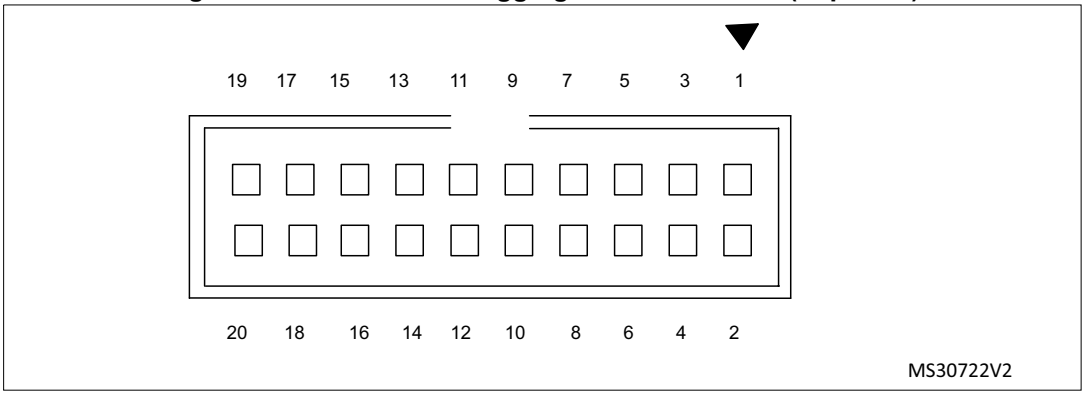


Table 34. Trace debugging connector CN12

Pin number	Description	Pin number	Description
1	+3.3 V	2	TMS/PA13
3	GND	4	TCK/PA14
5	GND	6	TDO/PB3
7	KEY	8	TDI/PA15
9	GND	10	RESET#
11	GND	12	Trace_CLK/PE2
13	GND	14	Trace_D0/PE3 or SWO/PB3
15	GND	16	Trace_D1/PE4 or nTRST/PB4
17	GND	18	Trace_D2/PE5
19	GND	20	Trace_D3/PE6

10.11 TAG connector CN15

Table 35. TAG debugging connector CN15

Terminal	Function / MCU port	Terminal	Function / MCU port
1	VDD	2	SWDIO/TMS (PA13)
3	GND	4	SWDCLK/TCK (PA14)
5	GND	6	SWO/TDO (PB3)
7	NC	8	TDI (PA15)
9	TRST (PB4)	10	RESET#

10.12 DSI display connector CN16 (MIPI)

A TFT color LCD with MIPI DSI interface board is mounted on CN16. Refer to *Section 9.29* for detail.

10.13 JTAG connector CN17

Figure 19. JTAG/SWD debugging connector CN17 (Top view)

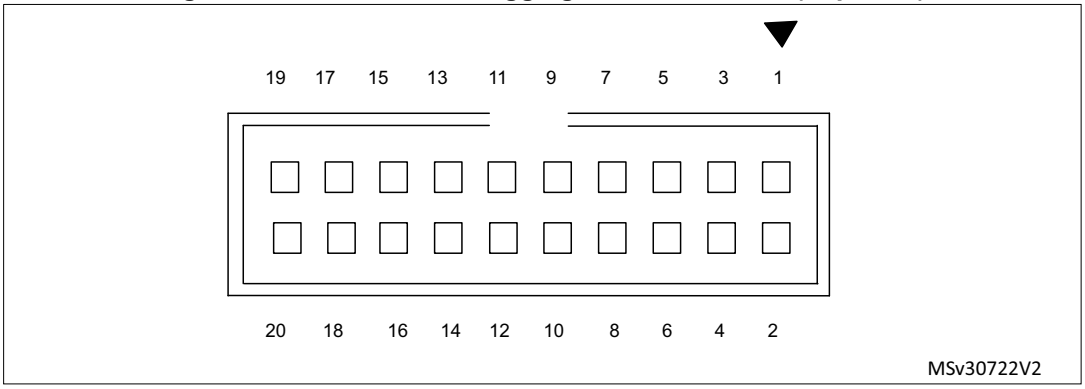


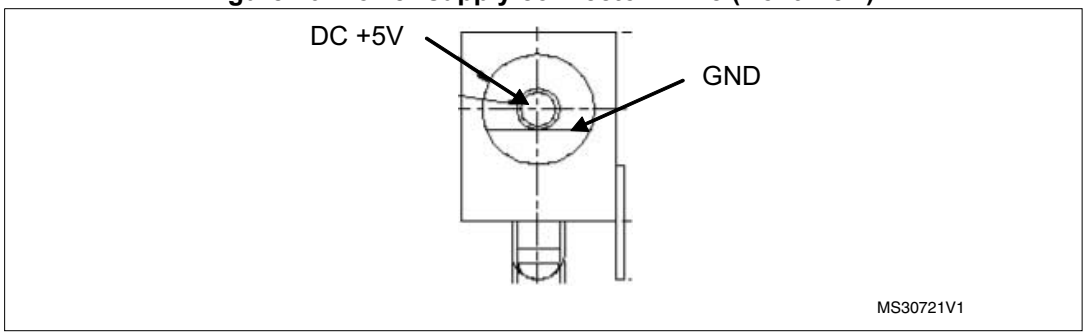
Table 36. JTAG/SWD debugging connector CN17

Pin number	Description	Pin number	Description
1	VDD power	2	VDD power
3	PB4	4	GND
5	PA15	6	GND
7	PA13	8	GND
9	PA14	10	GND
11	NC	12	GND
13	PB3	14	GND
15	RESET#	16	GND
17	-	18	GND
19	-	20	GND

10.14 Power connector CN18

The STM32L4R9I-EVAL board is power-able with a DC 5 V power supply via the external power supply jack (CN18) shown in *Figure 20*. The central pin of CN18 must be positive.

Figure 20. Power-supply connector CN18 (front view)



10.15 ST-LINK/V2-1 programming connector CN19

The connector CN19 is used only for embedded ST-LINK/V2-1 programming during board manufacturing. It is not populated by default and not for end users.

10.16 TFT LCD connector CN20 (RGB)

A TFT-color LCD board is mounted on CN20. Refer to *Section 9.30* for details.

10.17 ST-LINK/V2-1 USB Micro-B connector CN21

The USB connector CN21 is used to connect on board ST-LINK/V2-1 facility to a PC for programming and debugging purposes.

Figure 21. USB Micro-B connector CN21 (front view)

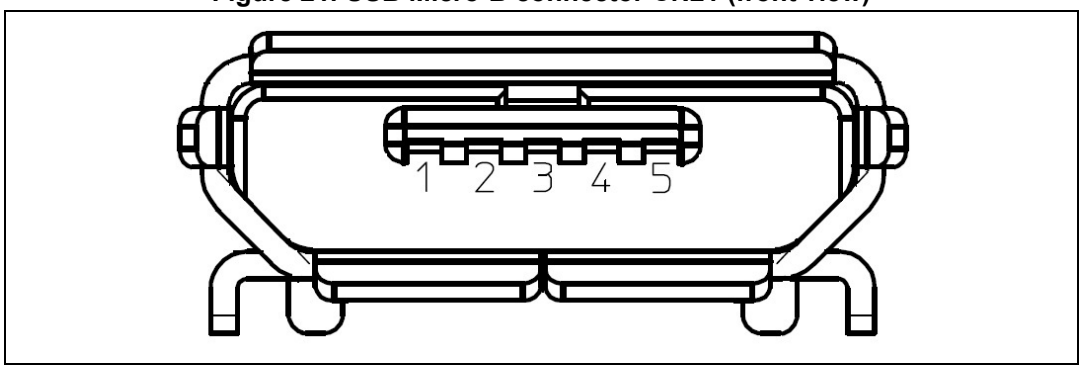


Table 37. USB Micro-B connector CN21 (front view)

Pin number	Description	Pin number	Description
1	VBUS (power)	4	GND

Table 37. USB Micro-B connector CN21 (front view) (continued)

Pin number	Description	Pin number	Description
2	DM	5	Shield
3	DP	-	-

10.18 CAN D-type male connector CN22

Figure 22. CAN D-type 9-pin male connector CN22 (front view)

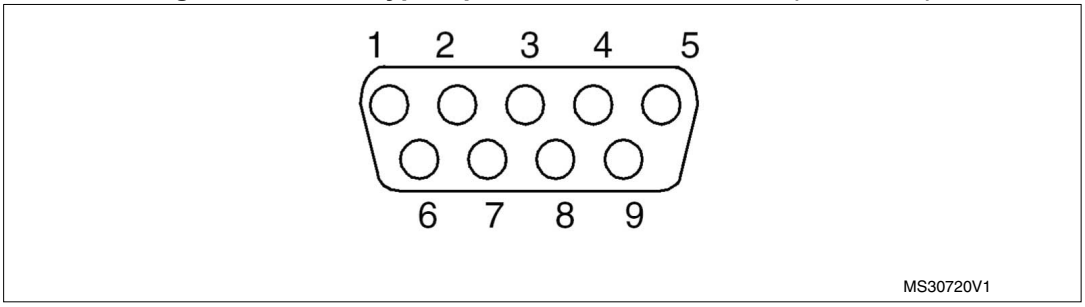


Table 38. CAN D-type 9-pin male connector CN22

Pin number	Description	Pin number	Description
1,4,8,9	NC	7	CANH
2	CANL	3,5,6	GND

11 Electrical schematics

This section provides design schematics for the STM32L4R9I-EVAL key features to help users to implement these features in application designs.

This section includes:

- Overall schematics for the STM32L4R9I-EVAL, see *Figure 23*
- STM32L4R9I-EVAL MCU, see *Figure 24*
- Power supply, see *Figure 25*
- SRAM and NOR Flash memory devices and TFT LCD, see *Figure 26*
- Audio codec device, see *Figure 27*
- DSI display connector, see *Figure 28*
- Physical control peripherals, microSD card and EEPROM, see *Figure 29*
- Analog input and output, Touch-sensing device, see *Figure 30*
- ST-LINK/V2-1, see *Figure 31*
- IDD measurement, see *Figure 32*
- JTAG and trace debug connectors, see *Figure 33*
- Motor control connector, see *Figure 34*
- USB_OTG_FS port, see *Figure 35*
- USART and CAN transceiver, PMOD connector, see *Figure 36*
- Octo-SPI Flash memory device, see *Figure 37*
- Extension connector, see *Figure 38*

Figure 23. Overall schematics for the STM32L4R9I-EVAL

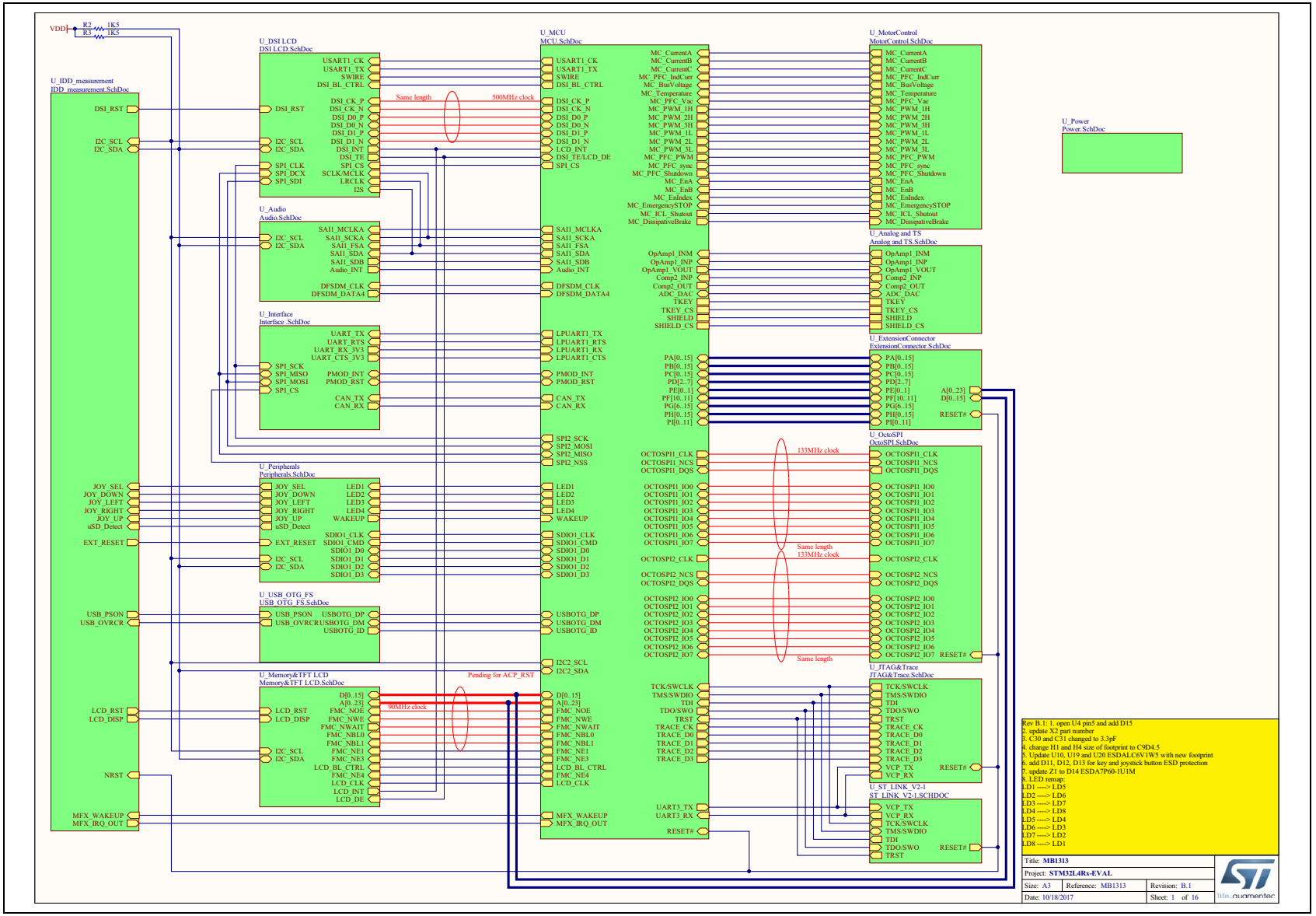


Figure 24. STM32L4R9I-EVAL MCU

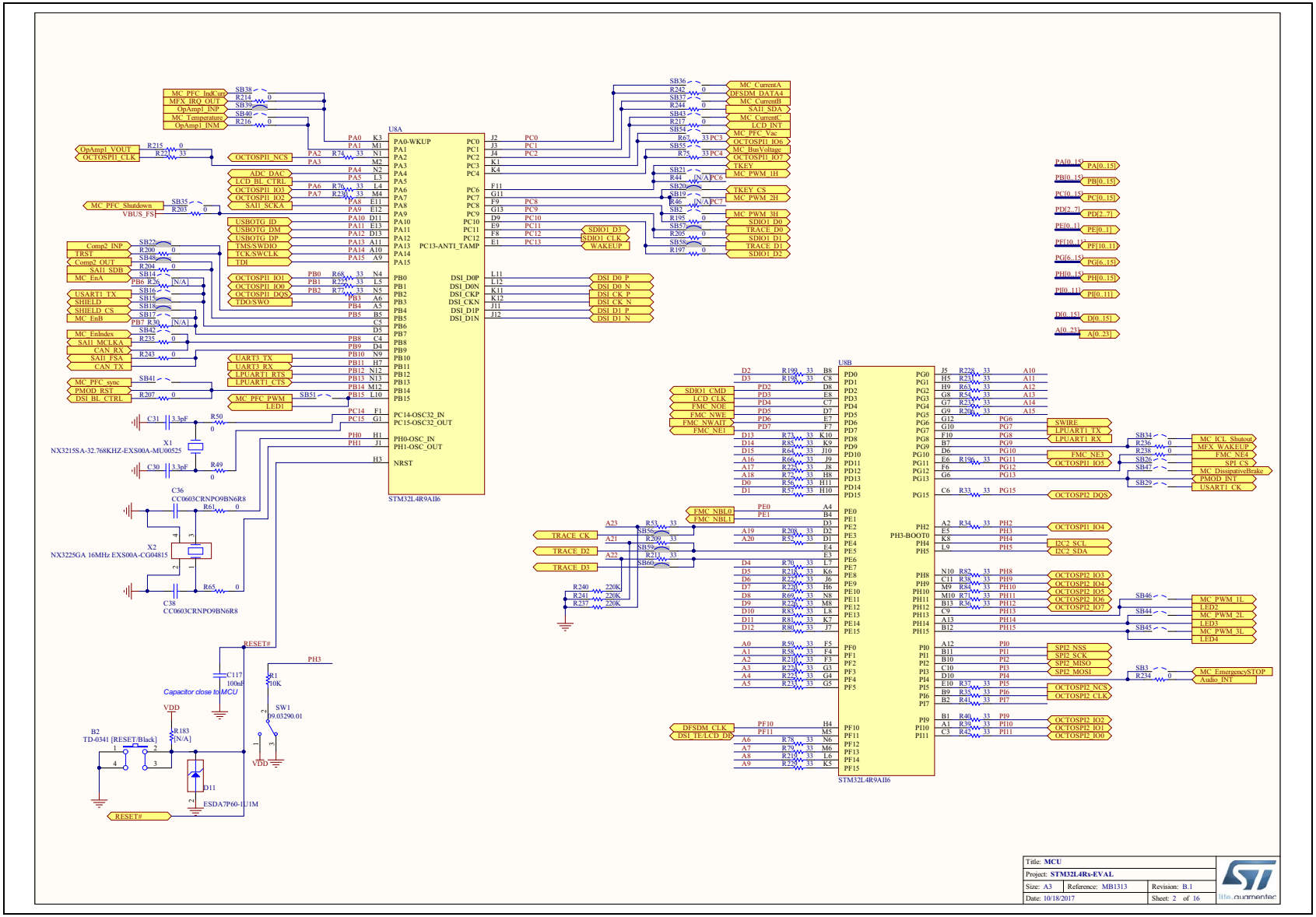


Figure 25. Power supply

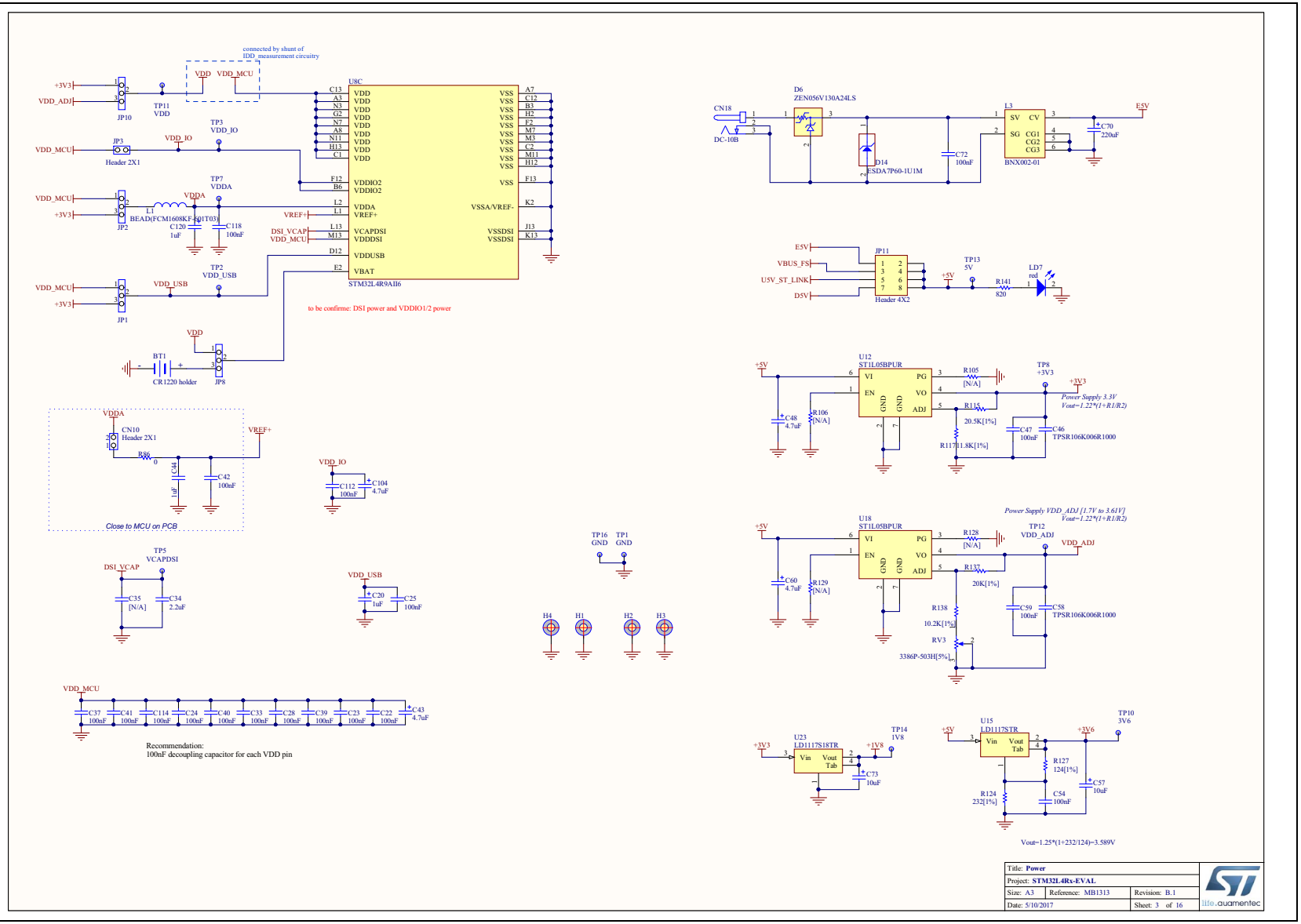


Figure 26. SRAM and NOR Flash memory devices and TFT LCD

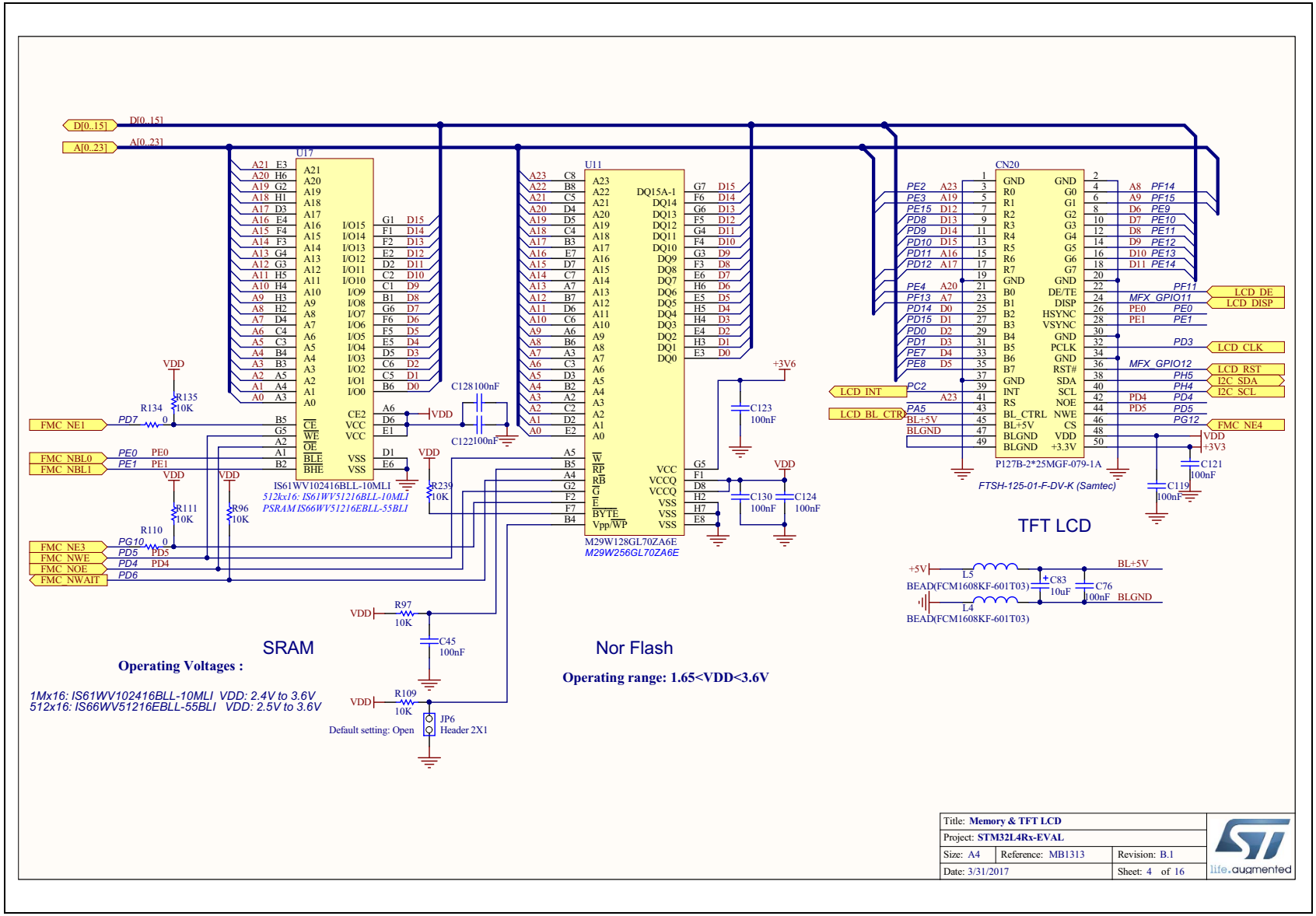


Figure 27. Audio codec device

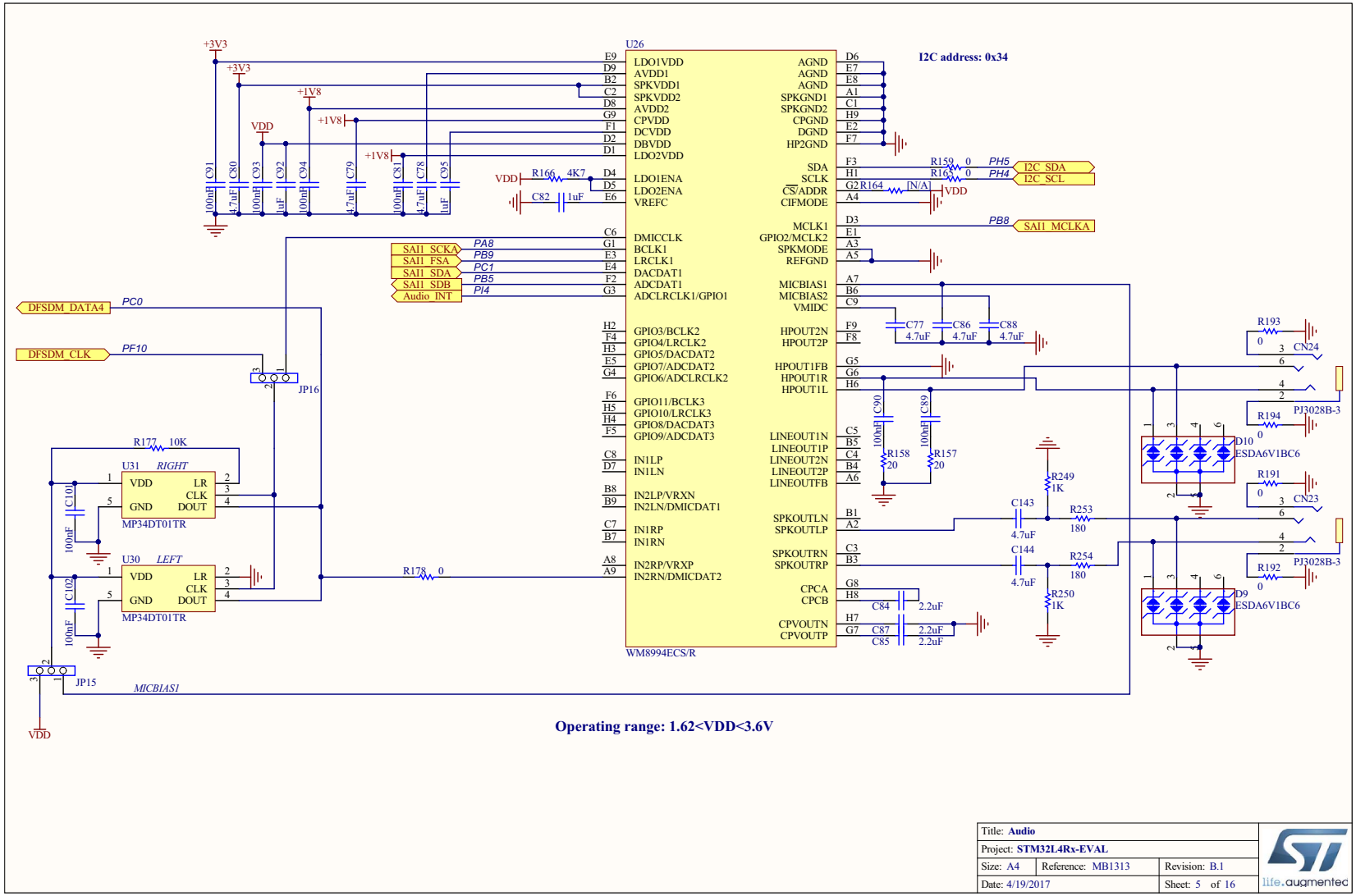


Figure 28. DSI display connector

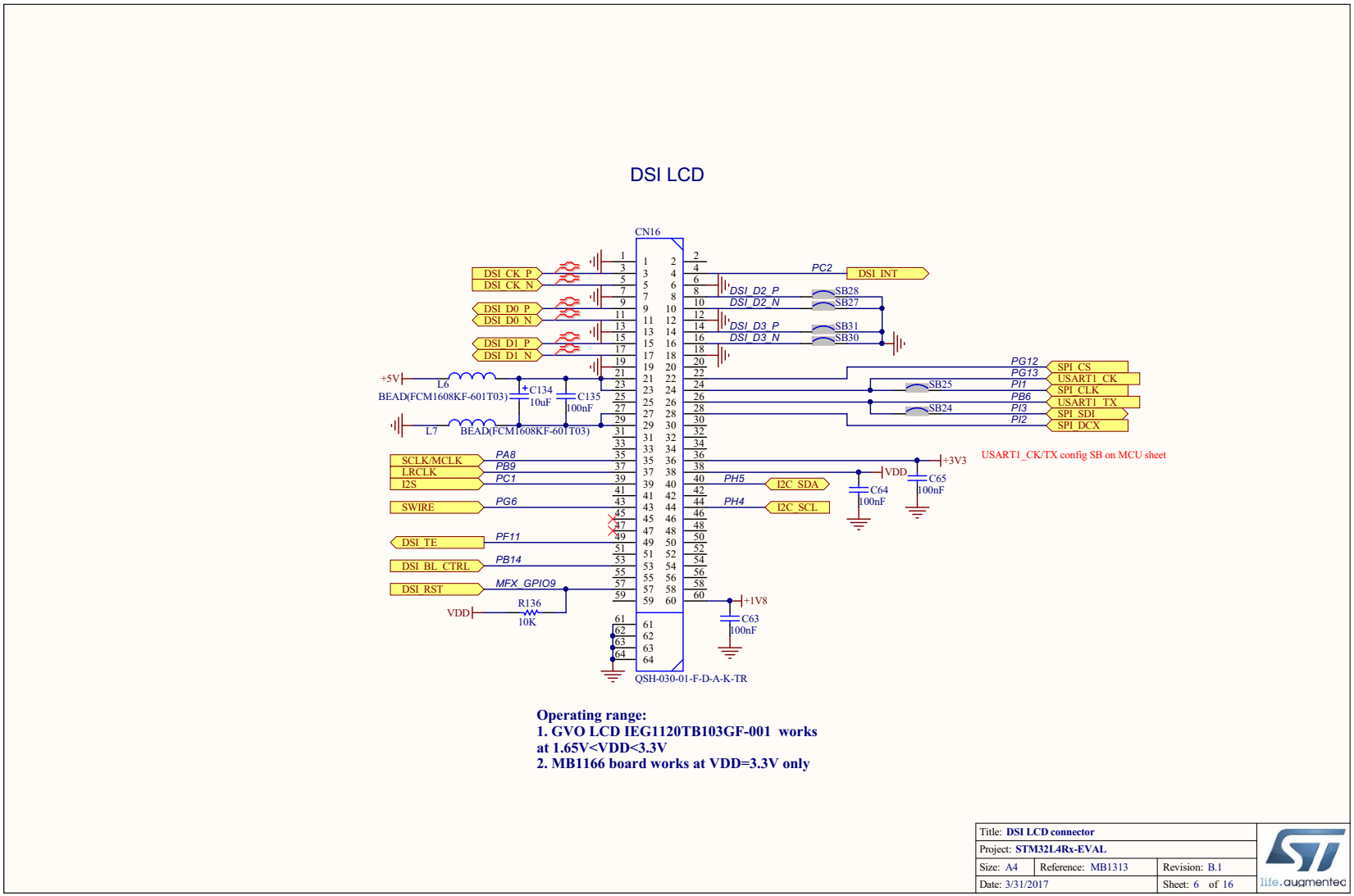


Figure 29. Physical control peripherals, microSD card and EEPROM

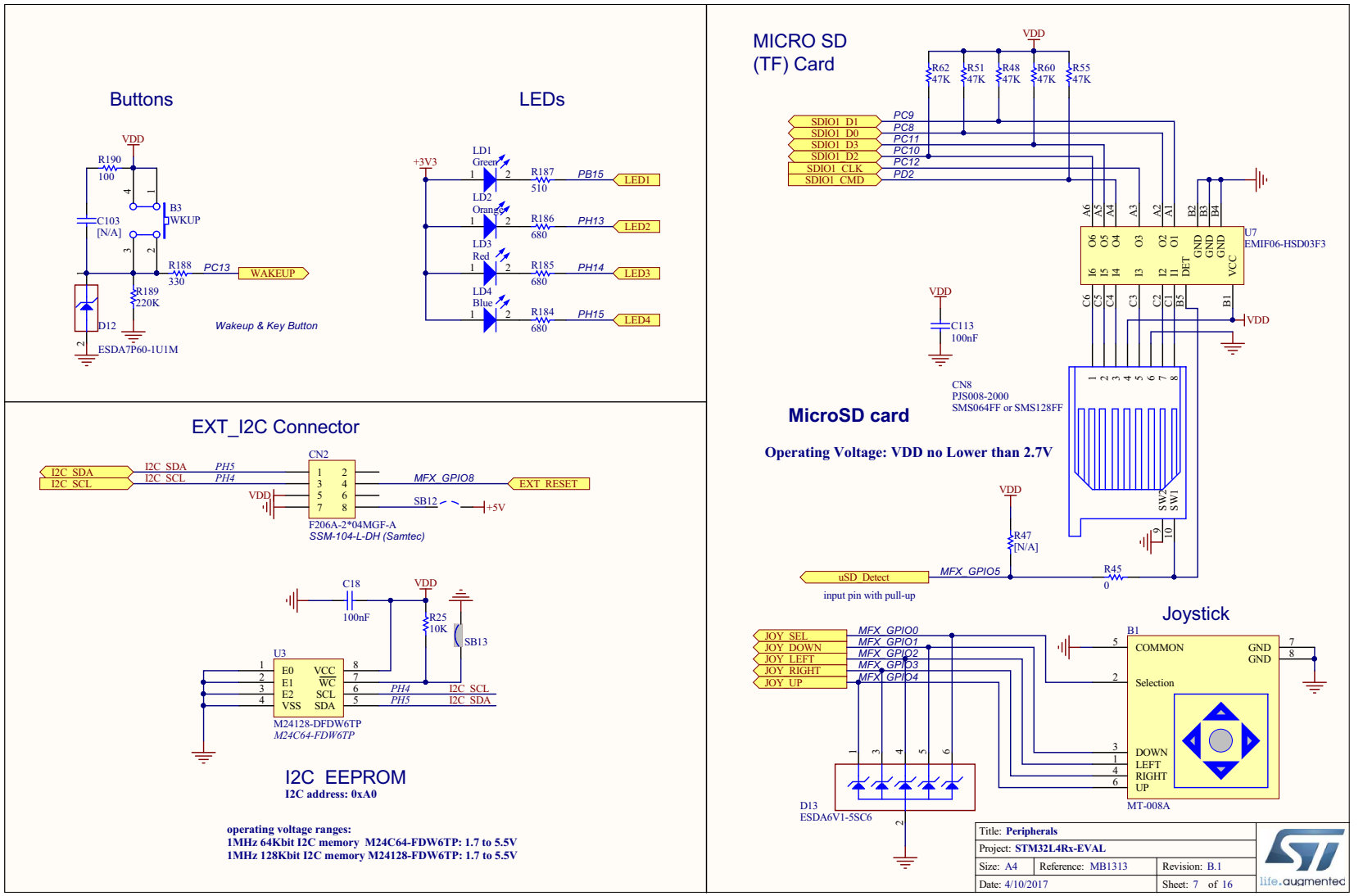


Figure 30. Analog input and output and touch-sensing device

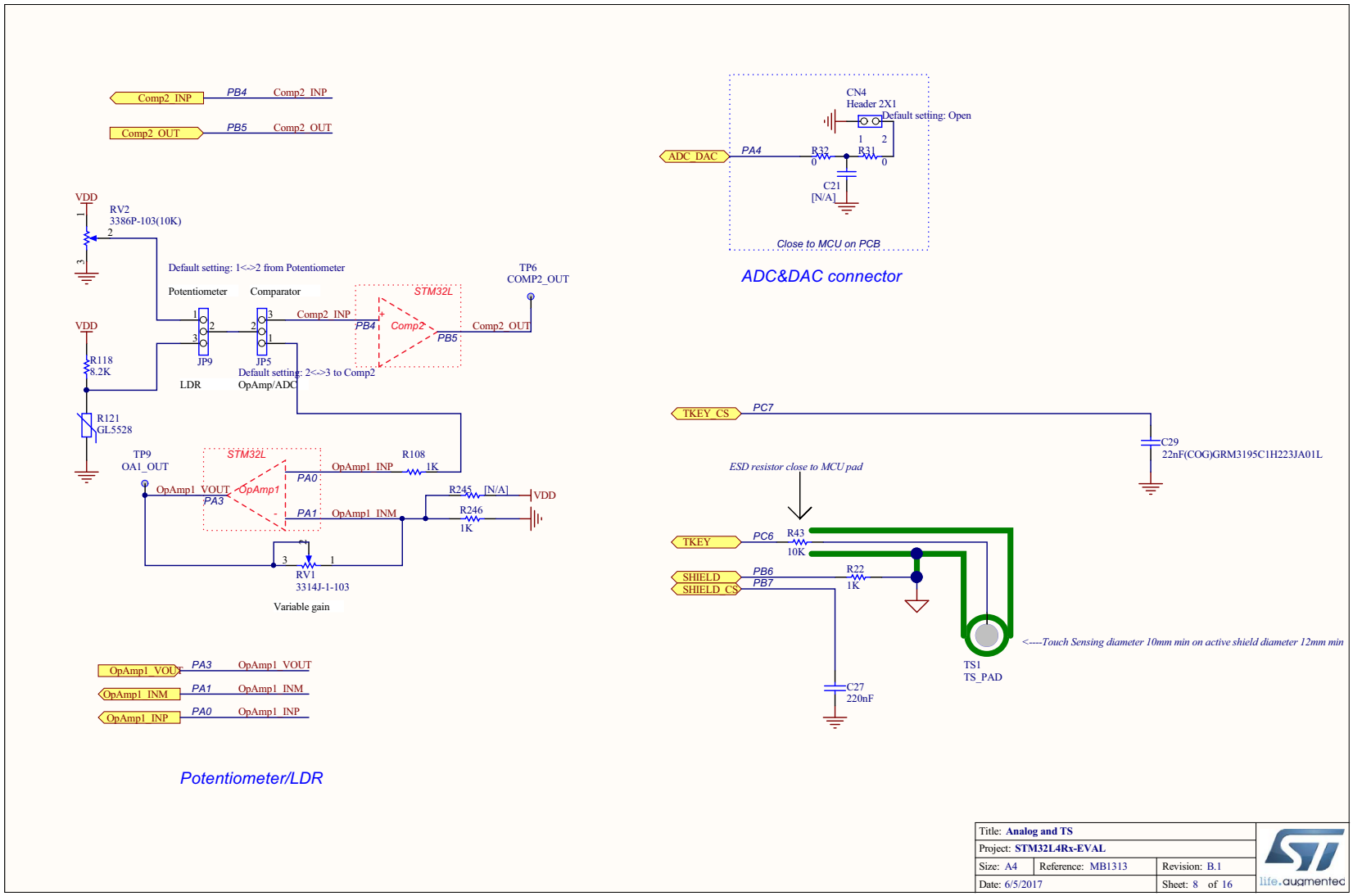


Figure 31. ST-LINK/V2-1

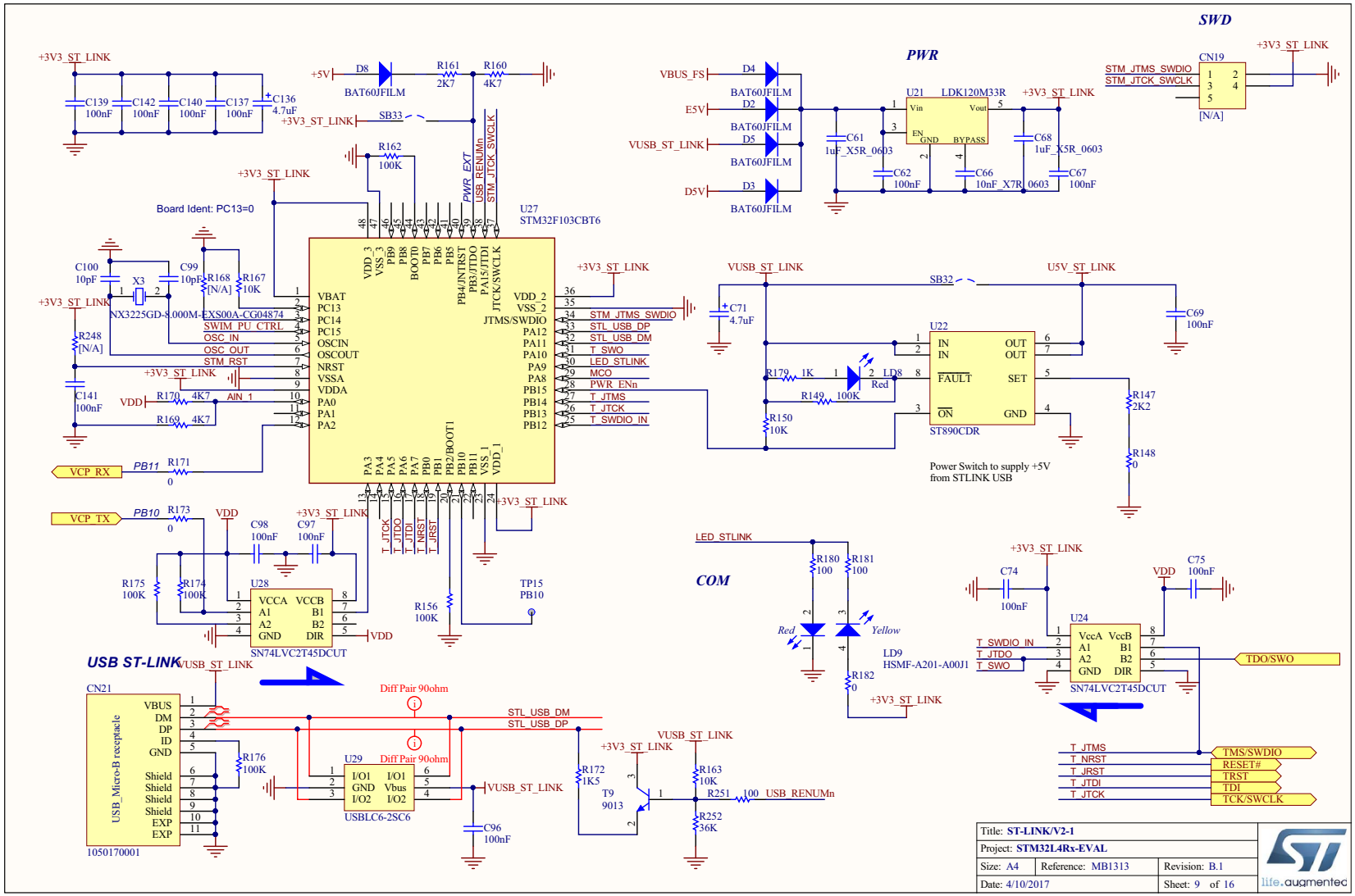


Figure 32. IDD measurement

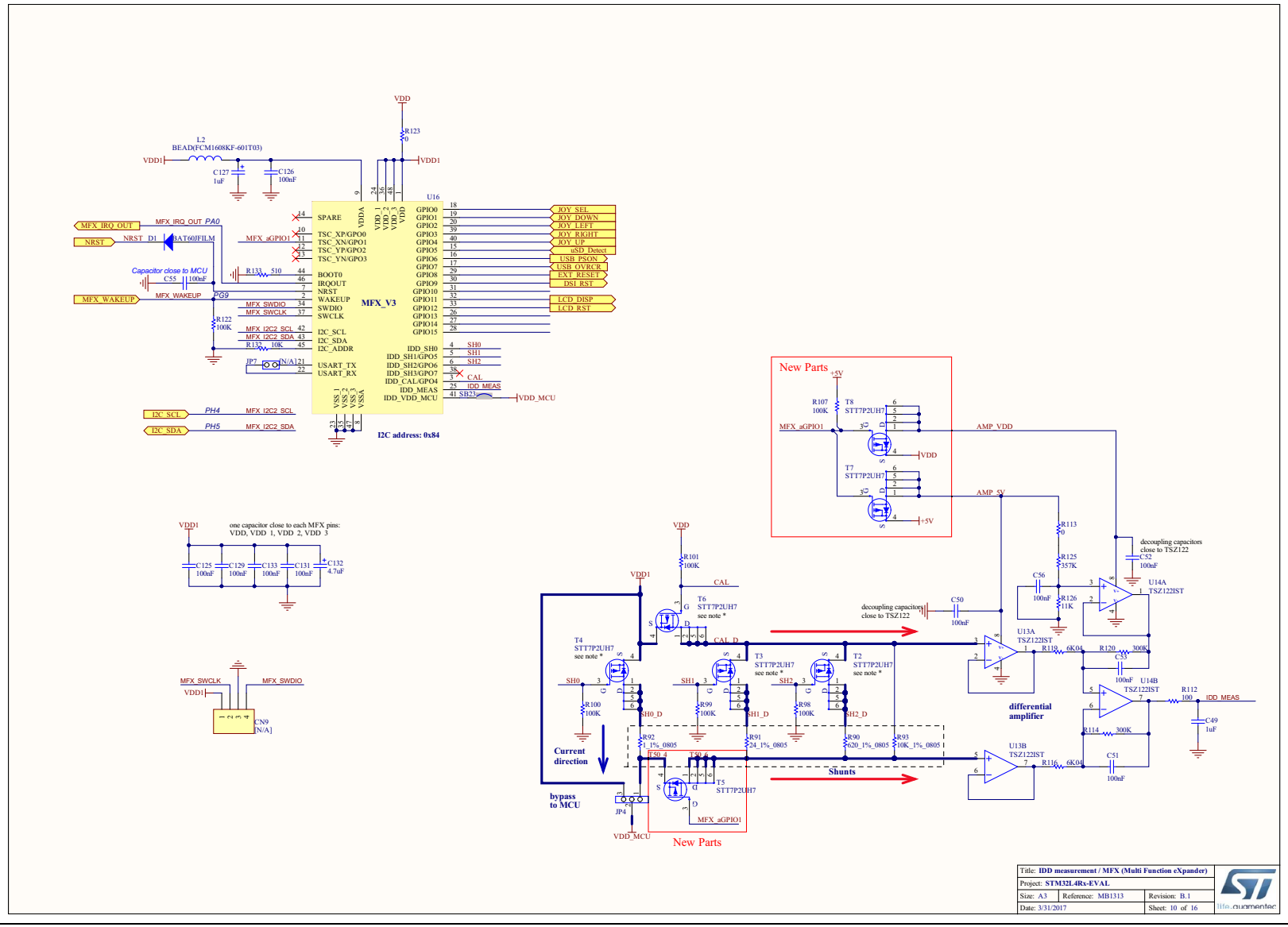


Figure 33. JTAG and trace debug connectors

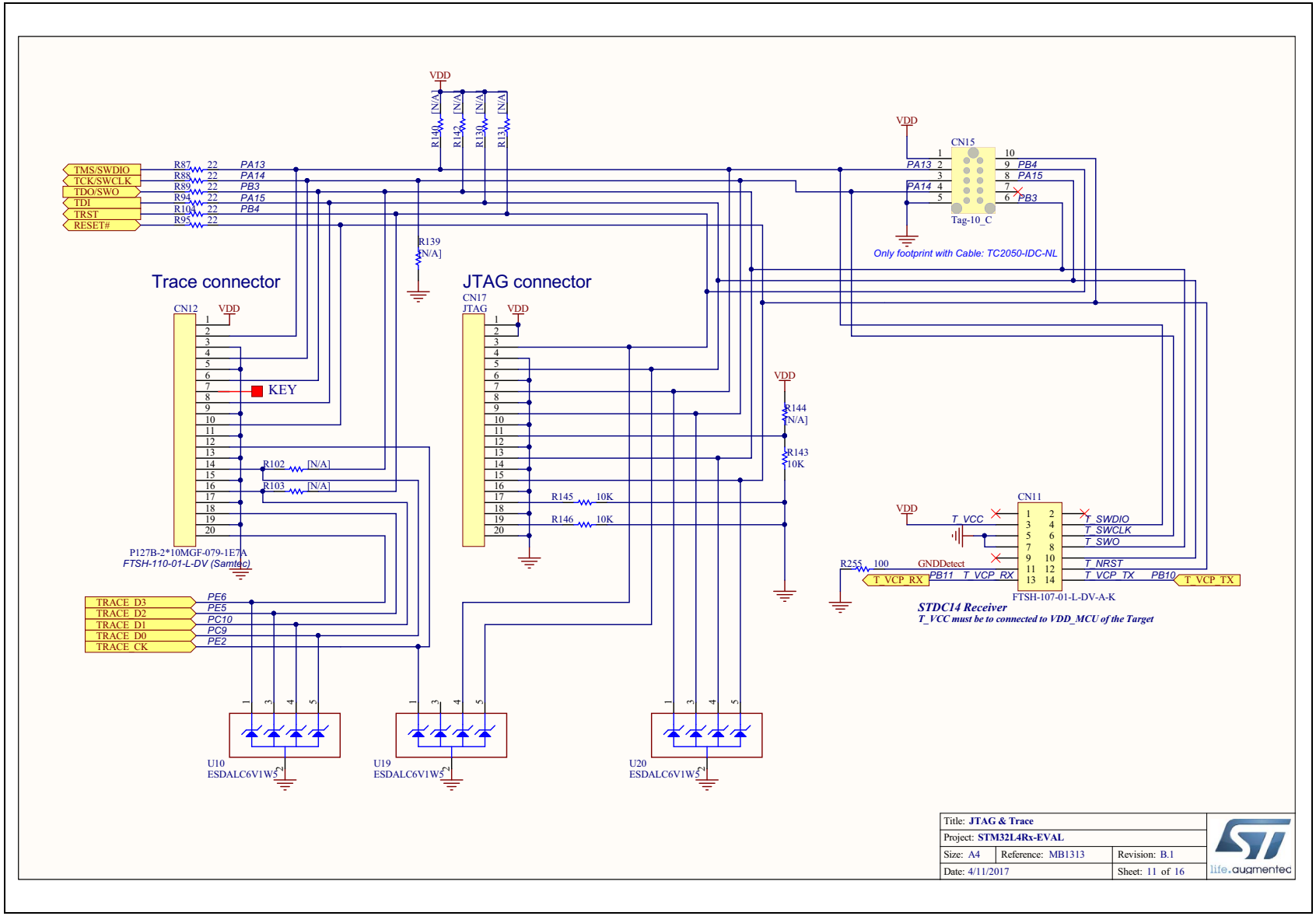


Figure 34. Motor-control connector

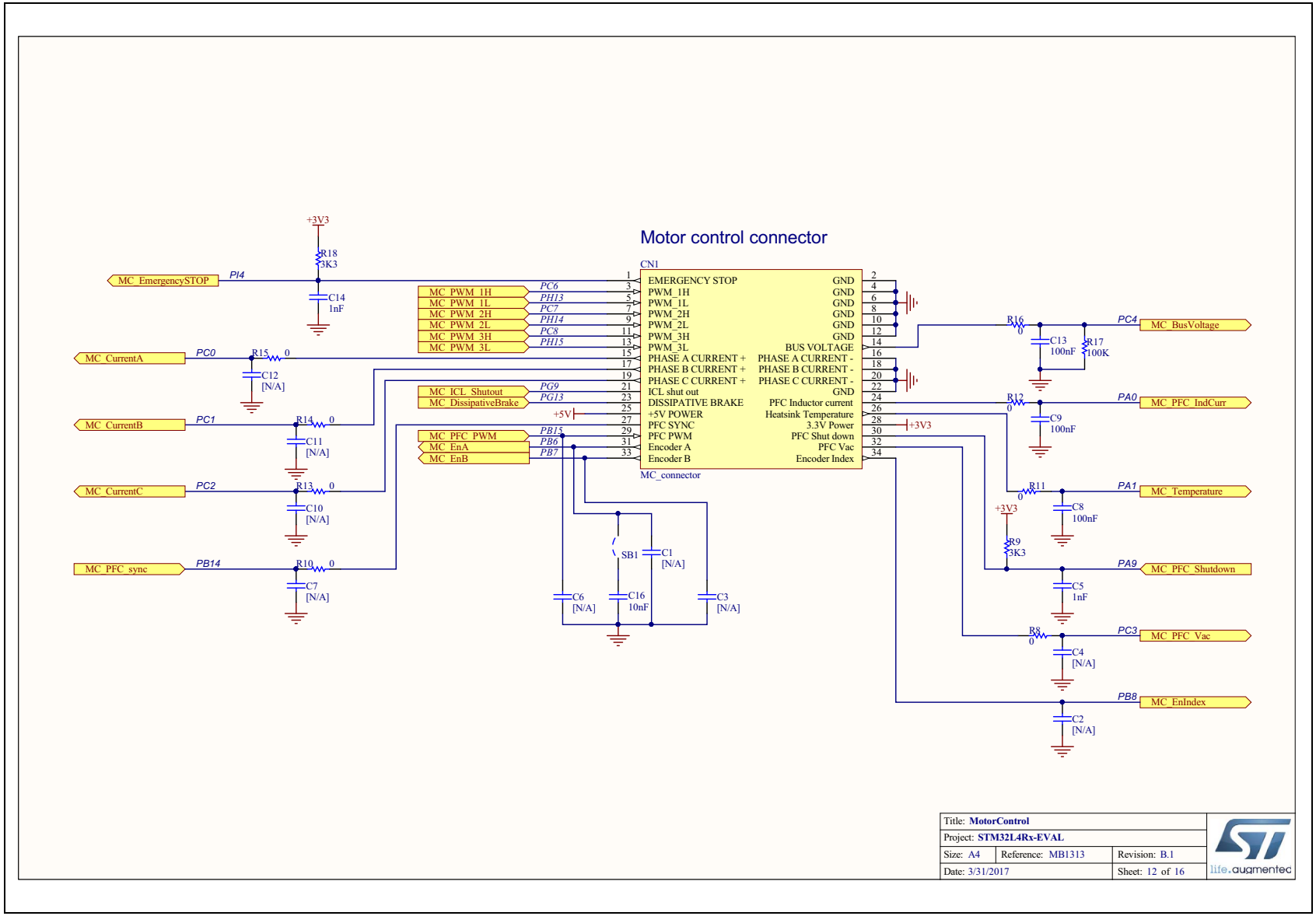


Figure 35. USB OTG FS port

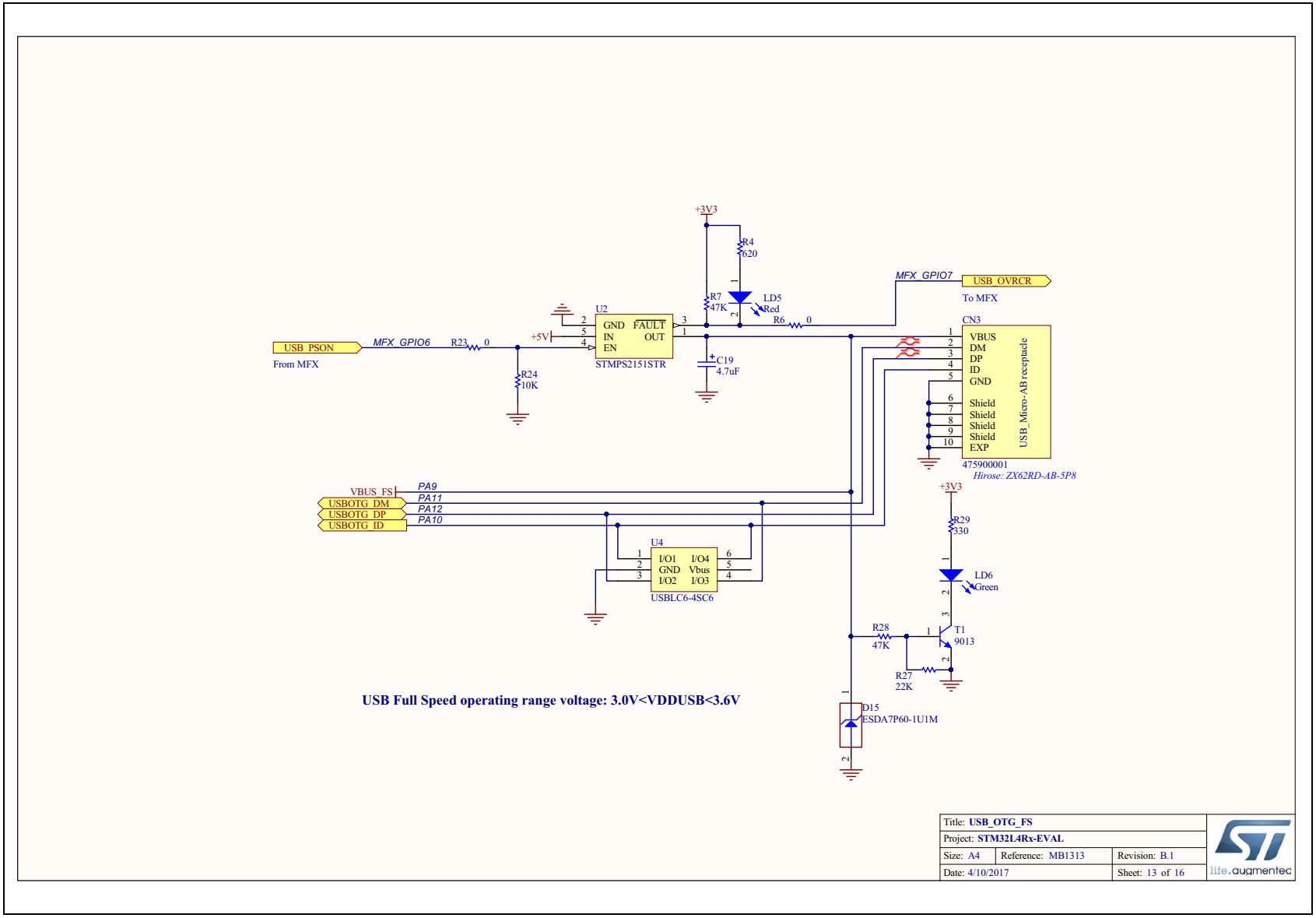


Figure 36. USART, CAN transceiver and PMOD connector

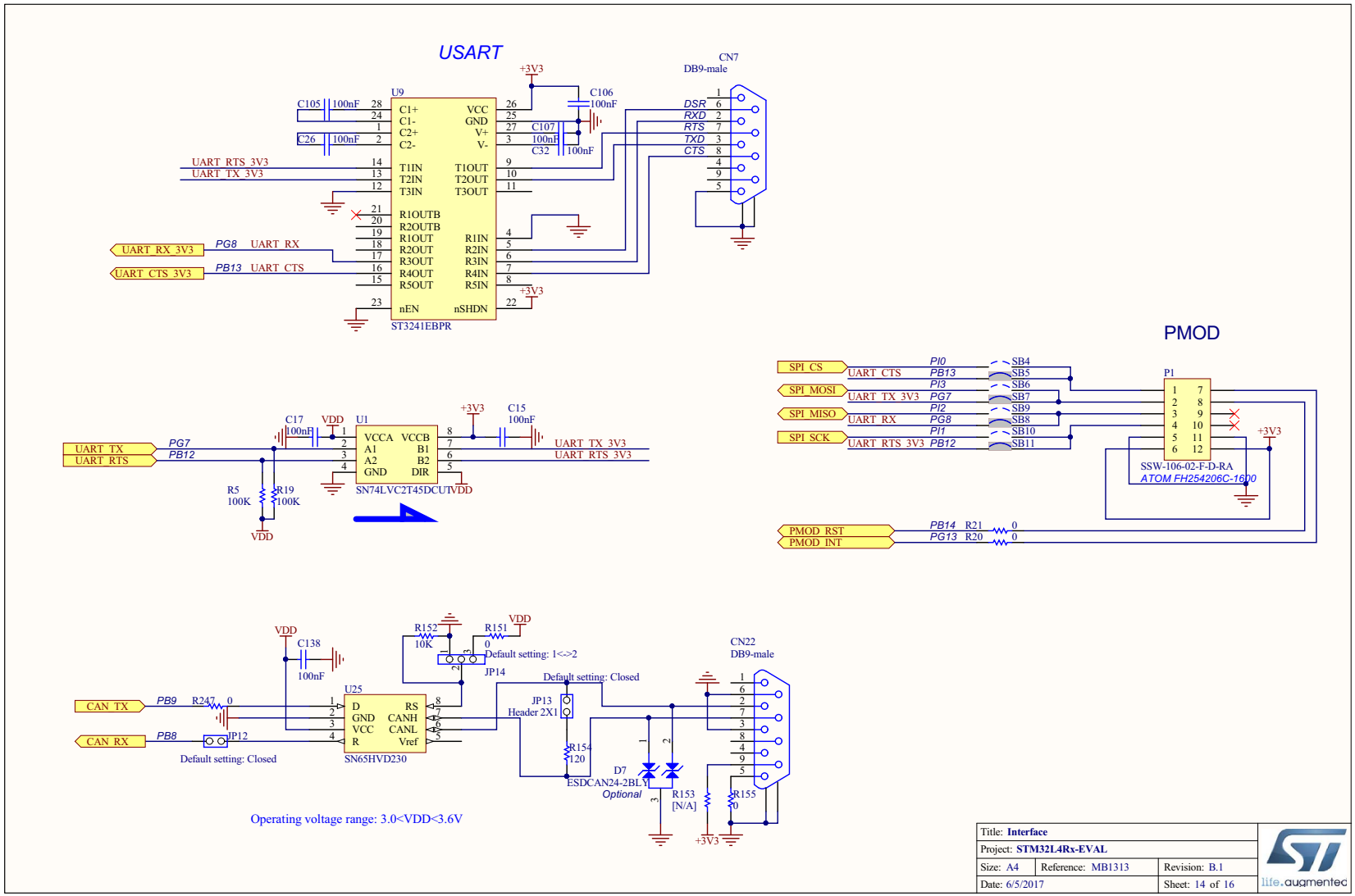


Figure 37. Octo-SPI Flash memory device

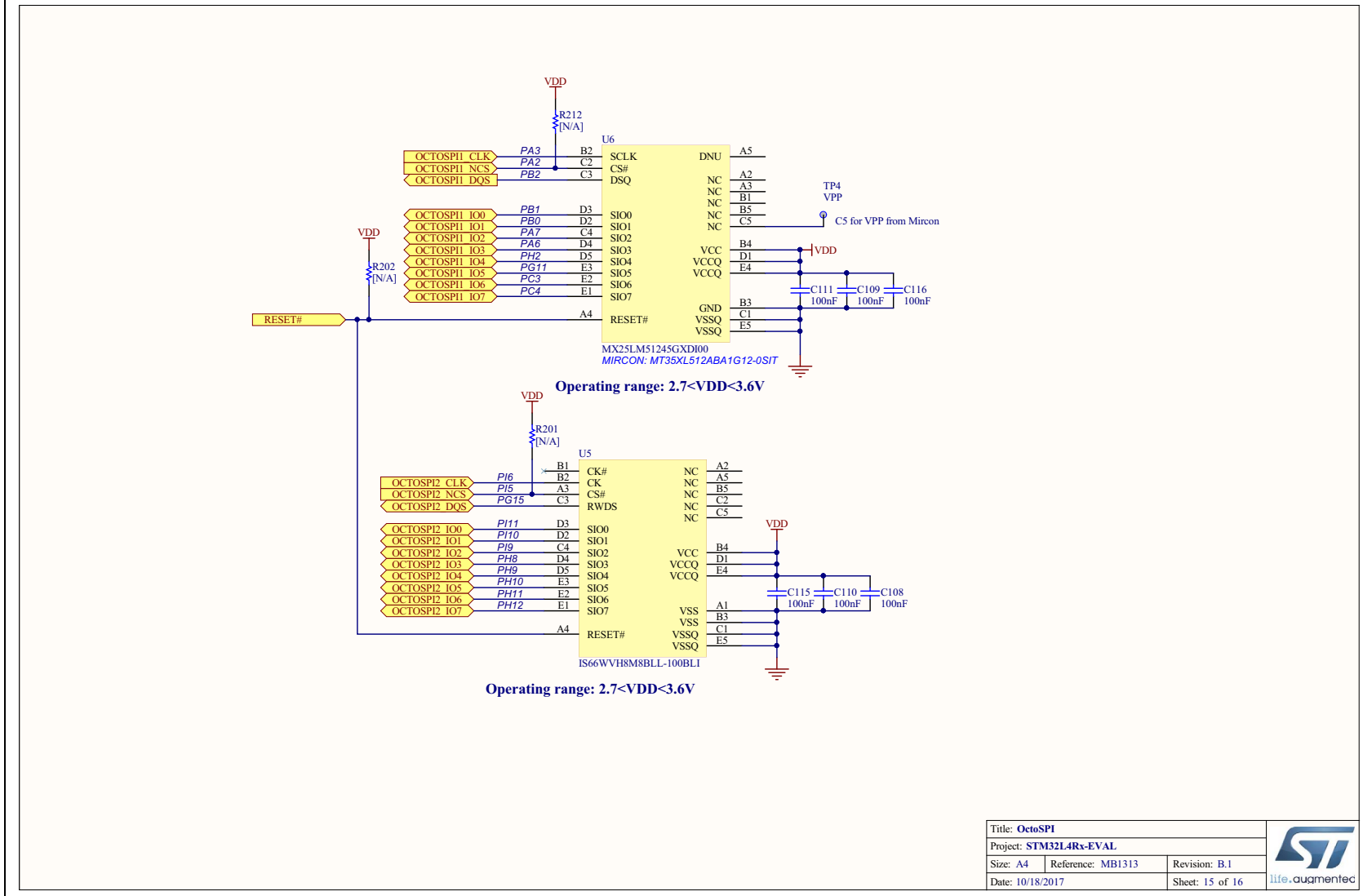
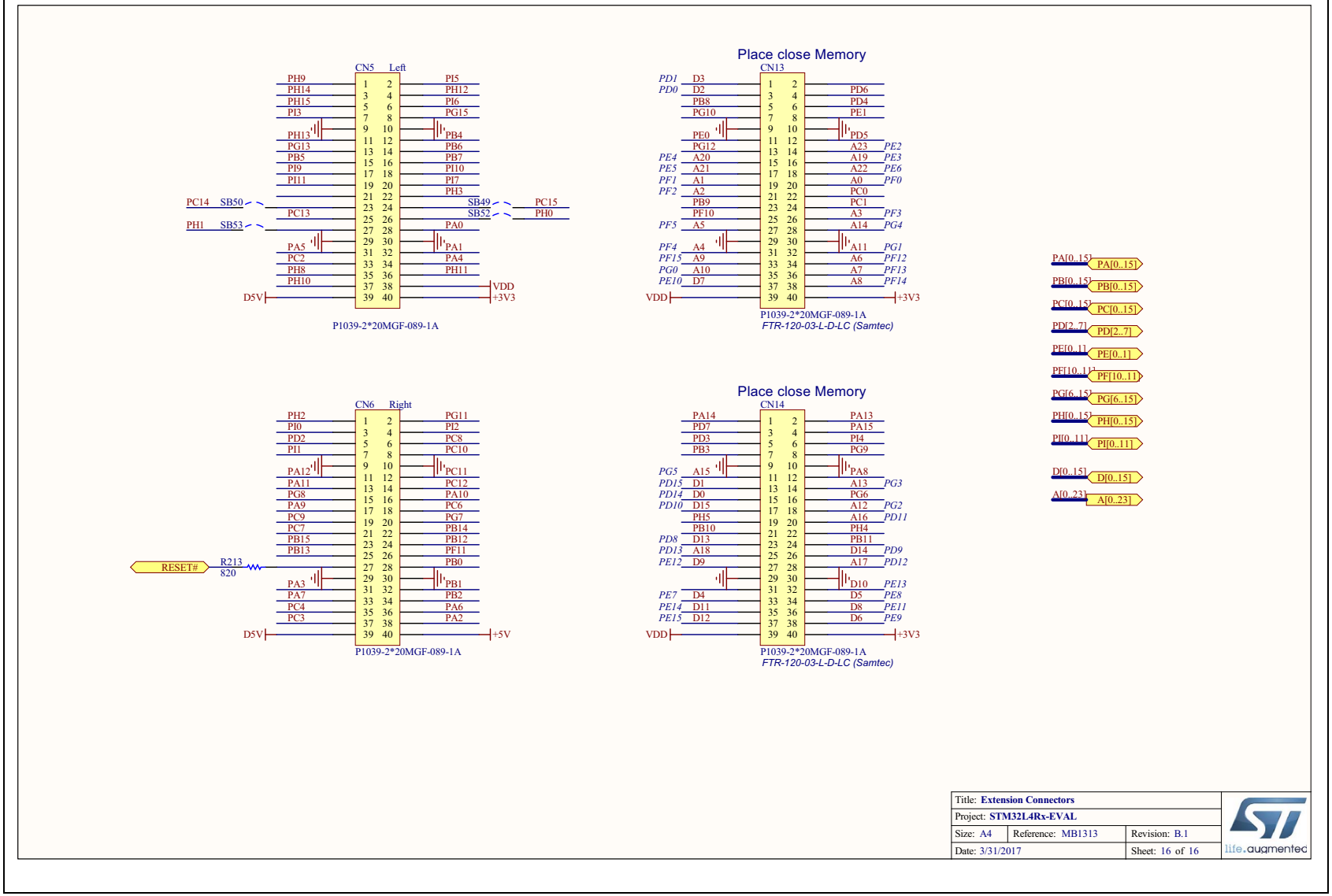


Figure 38. Extension connectors



Appendix A I/O assignment

Table 39. STM32L4R9I-EVAL I/O assignment

Primary key	UFBGA 169 DSI	Pin name	Pinout assignment	RGB LCD with FMC mode	Motor-control connector
1	K12	DSI_CKN	-	-	-
2	K11	DSI_CKP	-	-	-
3	L12	DSI_D0N	-	-	-
4	L11	DSI_D0P	-	-	-
5	J12	DSI_D1N	-	-	-
6	J11	DSI_D1P	-	-	-
7	L13	VCAPDSI	-	-	-
8	[L13]	VDD12DSI	-	-	-
9	[L13]	VDD12DSI	-	-	-
10	J13	VSSDSI	-	-	-
11	K13	VSSDSI	-	-	-
12	H3	NRST	NRST	-	-
13	K3	PA0	OPAMP1_VINP || MFX_IRQ_OUT	-	PFC ind. Curr.
14	M1	PA1	OPAMP1_VINM	-	Heatsink Temp.
15	N1	PA2	OCTOSPIP1_NCS	-	-
16	M2	PA3	OCTOSPIP1_ CLK || OPAMP1_VOUT	-	-
17	N2	PA4	ADC/DAC	-	-
18	L3	PA5	LCD_BL_CTRL	-	-
19	L4	PA6	OCTOSPIP1_IO3	-	-
20	M4	PA7	OCTOSPIP1_IO2	-	-
21	E11	PA8	SAI1_SCK_A	-	-
22	E12	PA9	OTG_FS_VBUS	-	PFC shutdown
23	D11	PA10	OTG_FS_ID	-	-
24	E13	PA11	OTG_FS_DM	-	-
25	D13	PA12	OTG_FS_DP	-	-
26	A11	PA13	JTMS/SWDIO	-	-
27	A10	PA14	JTCK/SWCLK	-	-
28	A9	PA15	JTDI	-	-
29	N4	PB0	OCTOSPIP1_IO1	-	-
30	L5	PB1	OCTOSPIP1_IO0	-	-
31	N5	PB2	OCTOSPIP1_DQS	-	-

Table 39. STM32L4R9I-EVAL I/O assignment (continued)

Primary key	UFBGA 169 DSI	Pin name	Pinout assignment	RGB LCD with FMC mode	Motor-control connector
32	A6	PB3	JTDO/TRACESWO	-	-
33	A5	PB4	NJTRST || COMP2_INP	-	-
34	B5	PB5	SAI1_SD_B || COMP2_OUT	-	-
35	C5	PB6	TSC_G2_IO3 || USART1_TX	-	Encoder A
36	D5	PB7	TSC_G2_IO4	-	Encoder B
37	C4	PB8	SAI1_MCLK_A || CAN1_RX	-	Encoder Index
38	D4	PB9	SAI1_FS_A || CAN1_TX	-	-
39	N9	PB10	UART3_TX	-	-
40	H7	PB11	UART3_RX	-	-
41	N12	PB12	LPUART1_RTS_DE	-	-
42	N13	PB13	LPUART1_CTS	-	-
43	M12	PB14	PMOD_RST/DSI_BL_CTRL	-	PFC sync
44	L10	PB15	LED1	-	PFC PWM
45	J2	PC0	DFSDM1_DATIN4	-	PhaseA Current+
46	J3	PC1	SAI1_SD_A	-	PhaseB Current+
47	J4	PC2	LCD_INT	-	PhaseC Current+
48	K1	PC3	OCTOSPIP1_IO6	-	PFC Vac
49	K4	PC4	OCTOSPIP1_IO7	-	Bus Voltage
50	F11	PC6	TSC_G4_IO1	-	MC_PWM_1H
51	G11	PC7	TSC_G4_IO2	-	MC_PWM_2H
52	F9	PC8	uSD1_D0	-	MC_PWM_3H
53	G13	PC9	uSD1_D1 || TRACED0	-	-
54	D9	PC10	uSD1_D2 || TRACED1	-	-
55	E9	PC11	uSD1_D3	-	-
56	F8	PC12	uSD1_CK	-	-
57	E1	PC13	TAMP1/WKUP2	-	-
58	F1	PC14-OSC32_IN	OSC32_IN	-	-
59	G1	PC15-OSC32_OUT	OSC32_OUT	-	-
60	B8	PD0	FMC_D2	LCD_B4	-
61	C8	PD1	FMC_D3	LCD_B5	-
62	D8	PD2	uSD1_CMD	-	-
63	E8	PD3	-	LCD_CLK	-
64	C7	PD4	FMC_NOE	LCD_NOE	-

Table 39. STM32L4R9I-EVAL I/O assignment (continued)

Primary key	UFBGA 169 DSI	Pin name	Pinout assignment	RGB LCD with FMC mode	Motor-control connector
65	D7	PD5	FMC_NWE	LCD_NWE	-
66	E7	PD6	FMC_NWAIT	LCD_DE	-
67	F7	PD7	FMC_NE1	-	-
68	K10	PD8	FMC_D13	LCD_R3	-
69	K9	PD9	FMC_D14	LCD_R4	-
70	J10	PD10	FMC_D15	LCD_R5	-
71	J9	PD11	FMC_A16	LCD_R6	-
72	J8	PD12	FMC_A17	LCD_R7	-
73	H8	PD13	FMC_A18	-	-
74	H11	PD14	FMC_D0	LCD_B2	-
75	H10	PD15	FMC_D1	LCD_B3	-
76	A4	PE0	FMC_NBL0	LCD_HSYNC	-
77	B4	PE1	FMC_NBL1	LCD_VSYNC	-
78	D3	PE2	FMC_A23 || TRACECK	LCD_R0	-
79	D2	PE3	FMC_A19	LCD_R1	-
80	D1	PE4	FMC_A20	LCD_B0	-
81	E4	PE5	FMC_A21 || TRACED2	-	-
82	E3	PE6	FMC_A22 || TRACED3	-	-
83	L7	PE7	FMC_D4	LCD_B6	-
84	K6	PE8	FMC_D5	LCD_B7	-
85	J6	PE9	FMC_D6	LCD_G2	-
86	H6	PE10	FMC_D7	LCD_G3	-
87	N8	PE11	FMC_D8	LCD_G4	-
88	M8	PE12	FMC_D9	LCD_G5	-
89	L8	PE13	FMC_D10	LCD_G6	-
90	K7	PE14	FMC_D11	LCD_G7	-
91	J7	PE15	FMC_D12	LCD_R2	-
92	F5	PF0	FMC_A0	-	-
93	F4	PF1	FMC_A1	-	-
94	F3	PF2	FMC_A2	-	-
95	G3	PF3	FMC_A3	-	-
96	G4	PF4	FMC_A4	-	-
97	G5	PF5	FMC_A5	-	-
98	H4	PF10	DFSDM1_CKOUT	-	-

Table 39. STM32L4R9I-EVAL I/O assignment (continued)

Primary key	UFBGA 169 DSI	Pin name	Pinout assignment	RGB LCD with FMC mode	Motor-control connector
99	M5	PF11	DSI_TE/LCD_DE	-	-
100	N6	PF12	FMC_A6	-	-
101	M6	PF13	FMC_A7	LCD_B1	-
102	L6	PF14	FMC_A8	LCD_G0	-
103	K5	PF15	FMC_A9	LCD_G1	-
104	J5	PG0	FMC_A10	-	-
105	H5	PG1	FMC_A11	-	-
106	H9	PG2	FMC_A12	-	-
107	G8	PG3	FMC_A13	-	-
108	G7	PG4	FMC_A14	-	-
109	G9	PG5	FMC_A15	-	-
110	G12	PG6	SWIRE	-	-
111	G10	PG7	LPUART1_TX	-	-
112	F10	PG8	LPUART1_RX	-	-
113	B7	PG9	MFX_WAKEUP	-	ICL shutout
114	D6	PG10	FMC_NE3	-	-
115	E6	PG11	OCTOSPIP1_IO5	-	-
116	F6	PG12	SPI_CS	LCD_NE4	-
117	G6	PG13	PMOD_INT/ USART1_CK	-	Dissipative Brake
118	C6	PG15	OCTOSPIP2_DQS	-	-
119	H1	PH0-OSC_IN	OSC_IN	-	-
120	J1	PH1-OSC_OUT	OSC_OUT	-	-
121	A2	PH2	OCTOSPIP1_IO4	-	-
122	E5	PH3-BOOT0	-	-	-
123	K8	PH4	I2C2_SCL	-	-
124	L9	PH5	I2C2_SDA	-	-
125	N10	PH8	OCTOSPIP2_IO3	-	-
126	C11	PH9	OCTOSPIP2_IO4	-	-
127	M9	PH10	OCTOSPIP2_IO5	-	-
128	M10	PH11	OCTOSPIP2_IO6	-	-
129	B13	PH12	OCTOSPIP2_IO7	-	-
130	C9	PH13	LED2	-	MC_PWM_1L
131	A13	PH14	LED3	-	MC_PWM_2L
132	B12	PH15	LED4	-	MC_PWM_3L

Table 39. STM32L4R9I-EVAL I/O assignment (continued)

Primary key	UFBGA 169 DSI	Pin name	Pinout assignment	RGB LCD with FMC mode	Motor-control connector
133	A12	PI0	SPI2_NSS	-	-
134	B11	PI1	SPI2_SCK	-	-
135	B10	PI2	SPI2_MISO	-	-
136	C10	PI3	SPI2_MOSI	-	-
137	D10	PI4	Audio_INT	-	MC_EmergencySTOP
138	E10	PI5	OCTOSPIP2_NCS	-	-
139	B9	PI6	OCTOSPIP2_CLK	-	-
140	B2	PI7	-	-	-
141	B1	PI9	OCTOSPIP2_IO2	-	-
142	A1	PI10	OCTOSPIP2_IO1	-	-
143	C3	PI11	OCTOSPIP2_IO0	-	-
144	E2	VBAT	-	-	-
145	N11	VDD	-	-	-
146	H13	VDD	-	-	-
147	C1	VDD	-	-	-
148	A3	VDD	-	-	-
149	C13	VDD	-	-	-
150	N3	VDD	-	-	-
151	G2	VDD	-	-	-
152	N7	VDD	-	-	-
153	A8	VDD	-	-	-
154	M13	VDDDSI	-	-	-
155	L2	VDDA	-	-	-
156	F12	VDDIO2	-	-	-
157	B6	VDDIO2	-	-	-
158	D12	VDDUSB	-	-	-
159	L1	VREF+	-	-	-
160	K2	VREF-	-	-	-
161	A7	VSS	-	-	-
162	C2	VSS	-	-	-
163	H12	VSS	-	-	-
164	M11	VSS	-	-	-
165	B3	VSS	-	-	-

Table 39. STM32L4R9I-EVAL I/O assignment (continued)

Primary key	UFBGA 169 DSI	Pin name	Pinout assignment	RGB LCD with FMC mode	Motor-control connector
166	C12	VSS	-	-	-
167	H2	VSS	-	-	-
168	F2	VSS	-	-	-
169	M7	VSS	-	-	-
170	M3	VSS	-	-	-
171	F13	VSS	-	-	-

Revision history

Table 40. Document revision history

Date	Revision	Changes
18-Aug-2017	1	Initial version
25-Oct-2017	2	Added: STM32L4R9I-EVAL board bottom view in *Figure 5* Bootloader limitation in *Chapter 9.8.1* Warning on AMOLED display in *Chapter 9.32* Updated: Cover views *Figure 3* and *Figure 4* moved to *Section 9.1* *Table 27* and *Table 39* alternative function removed *Figure 23*, *Figure 24*, and *Figure 37* in *Electrical schematics*