ESP-PSRAM32
Datasheet

Version 1.1

About This Guide

This document introduces the specifications of ESP-PSRAM32. The document is structured as follows:

Chapter	Title	Content
Chapter 1	Introduction	Overview of this datasheet.
Chapter 2	Package Type and Pin Configuration	Introduction to pin layout and pin description of ESP-PSRAM32.
Chapter 3	Power-up Initialization	Introduction to the power-up initialization timing.
Chapter 4	Interface Description	Provides information about address space, page length, drive strength, power-on status and commands.
Chapter 5	Operations in SPI Mode	Introduction to operations in SPI mode.
Chapter 6	Operations in QPI Mode	Introduction to operations in QPI mode.
Chapter 7	Reset Operation	Introduction to reset operation.
Chapter 8	Set Burst Length Operation	Introduction to set burst length operation.
Chapter 9	Input/Output Timing	Provides information on input/output timing.
Chapter 10	Electrical Specifications	Provides electrical specifications.
Chapter 11	Package Information	Provides package information.
Chapter 12	Ordering Information	Provides ordering information of ESP-PSRAM32.
Appendix A	Device Marking Convention	Provides information about device marking of ESP-PSRAM32.

Release Notes

Date	Version	Release notes
2017.06	V1.0	First release.
2017.08	V1.1	Updated Table 11-1 Package Dimensions.

Table of Contents

1. Introduction

This document provides the specifications of ESP-PSRAM32, which is a 1.8V 32-Mbit of SPI/QPI (serial/quad parallel interface) Pseudo SRAM device. This RAM is configurable as 1-bit input and output separately or 4-bit I/O common interface. This device also has Pseudo-SRAM features. All of the necessary refresh operations are taken care by the device itself.

The table below lists ordering information of ESP-PSRAM32.

Table 1-1. Ordering Information of ESP-PSRAM32

Product density	Package type	Temperature	Product carrier	Green code	Operating Voltage	Read/Write Operation Mode	SPI mode
32 Mbit	SOP8-150 mil	Extended (-25°C ~ +85°C)	Tube	RoHS Compliant Package and Green/Reach Package	1.8V	1 KB Pages	Standard/ Quad SPI

2. Pin Description

ESP-PSRAM32 is offered in an 8-pin SOP8 150 mil. Figure 2-1 shows the pin layout.

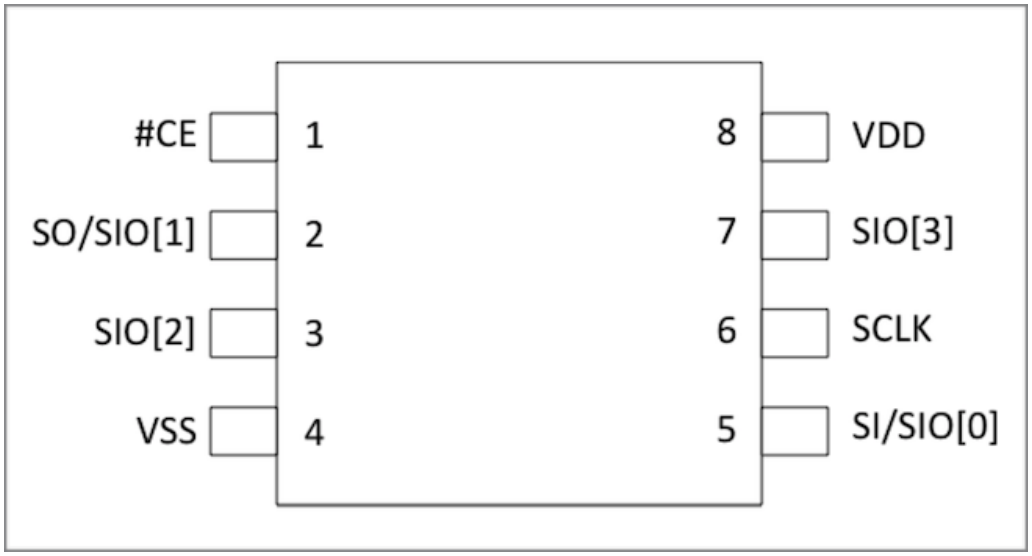

Figure 2-1.Pin Layout of ESP-PSRAM32

Table 2-1. Pin Description of ESP-PSRAM32

Pin	Signal Type	SPI Mode	QPI Mode
VDD	Power	Core power supply, 1.8V.	
VSS	Ground	Core supply ground	
CE#	Input	Chip select signal, active low. When CE# input is high, the memory will be in standby status.	
CLK	Output	Clock signal	
SI/SIO[0]	I/O	Serial input	I/O[0]
SO/SIO[1]	I/O	Serial output	I/O[1]
SIO[3:2]	I/O	(I/O[3:2]*)	I/O[3:2]

> 📖 ***Note:***
>
> Fast quad read access and quad write access in SPI mode will use SIO[3:2].

3. Power-up Initialization

The SPI/QPI includes an on-chip voltage sensor used to start the self-initialization process. When VDD reaches a stable level at above the minimum VDD, the device will need 150 µs to complete its self-initialization process. From the beginning of power ramp to the end of the 150-µs period, CLK should remain LOW, CE# should remain HIGH (to track VDD within 200 mV) and SI/SO/SIO[3:0] should remain LOW.

After the 150-µs period, the device requires at least one clock during CE# high to properly reset. The device will then be ready for normal operation.

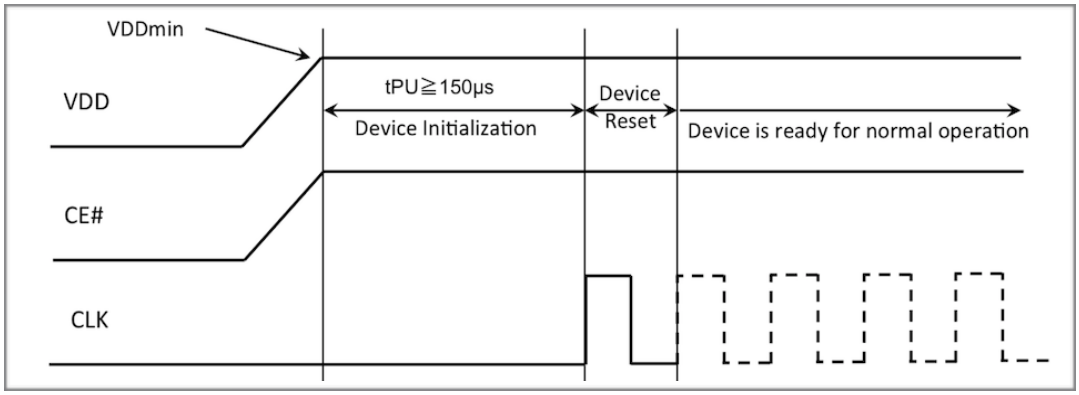

Figure 3-1. Power-up Initialization Timing

4. Interface Description

4.1. Address Space

SPI/QPI PSRAM device is byte-addressable. 32M device is addressed with A*21:0+.

4.2. Page Length

Read and write operations are always in wrap mode within 1 KB.

4.3. Drive Strength

The device powers up in 1/2 driver strength (50Ω).

4.4. Power-on Status

The device powers up in SPI Mode.

At least one clock pulse of CE# high is needed before beginning any operations.

4.5. Command/Address Latching Truth

The device recognizes the following commands specified by the various input methods.

Table 4-1. Commands Recognized by ESP32-PSRAM

Command	Code	SPI Mode (QE=0)					QPI Mode (QE=1)				
		Cmd	Add	Wait Cycle	DIO	MAX Freq.	Cmd	Add	Wait Cycle	DIO	MAX Freq.
Read	0x03	S	S	0	S	33	N/A				
Fast Read	0x0B	S	S	8	S	104	Q	Q	4	Q	84
Fast Read Quad	0xEB	S	Q	6	Q	104	Q	Q	6	Q	104
Write	0x02	S	S	0	S	104	Q	Q	0	Q	104
Quad Write	0x38	S	Q	0	Q	104	the same as 0x02				
Enter Quad Mode	0x35	S	-	-	-	104	N/A				
Exit Quad Mode	0xF5	N/A					Q	-	-	-	104
Reset Enable	0x66	S	-	-	-	104	Q	-	-	-	104
Reset	0x99	S	-	-	-	104	Q	-	-	-	104

Command	Code	SPI Mode (QE=0)					QPI Mode (QE=1)				
		Cmd	Add	Wait Cycle	DIO	MAX Freq.	Cmd	Add	Wait Cycle	DIO	MAX Freq.
Set Burst Length	0xC0	S	-	-	-	104	Q	-	-	-	104
Read ID	0x9F	S	S	0	S	104	N/A				

4.6. Command Termination

All reads and writes must be followed immediately by a clock pulse of CE# high in order to terminate the activated word line for the reads and writes, and set the device into standby status. Failure in doing so will block internal refresh operations until the device is notified of the termination of the read and write word line.

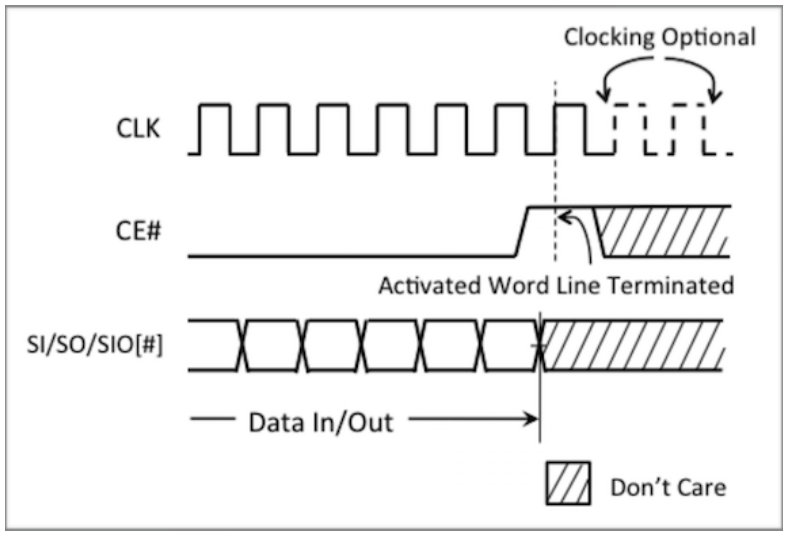

Figure 4-1. Command Termination

5. Operations in SPI Mode

The device enters SPI mode on power-up by default but can also be switched into QPI mode.

5.1. SPI Read Operations

For all reads, data will be available for tACLK after the falling edge of CLK. SPI reads can be done in three ways:

- 0x03: Serial CMD, Serial IO, slow frequency
- 0x0B: Serial CMD, Serial IO, fast frequency
- 0xEB: Serial CMD, Quad IO, fast frequency

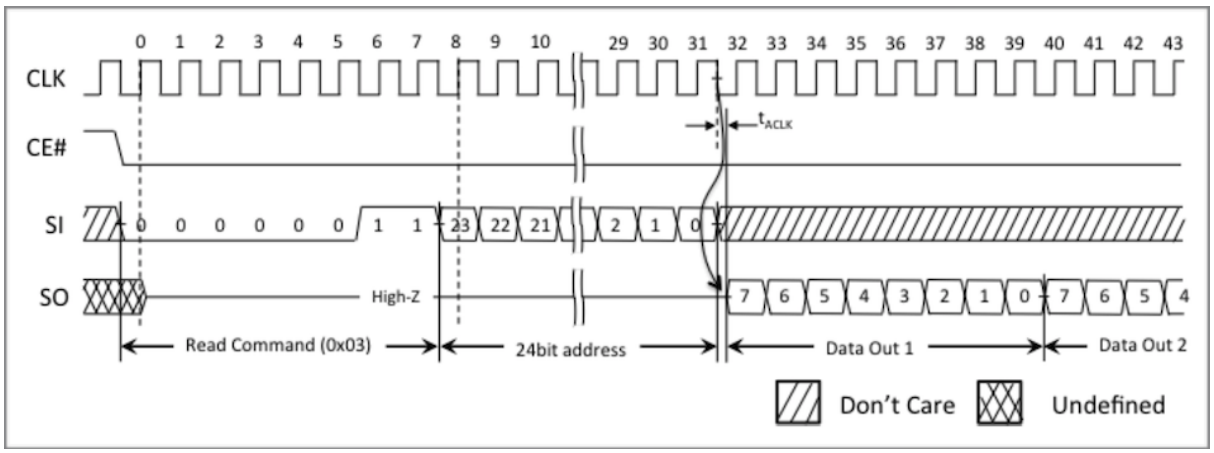

Figure 5-1. SPI Read 0x03 (Max frequency: 33 MHz)

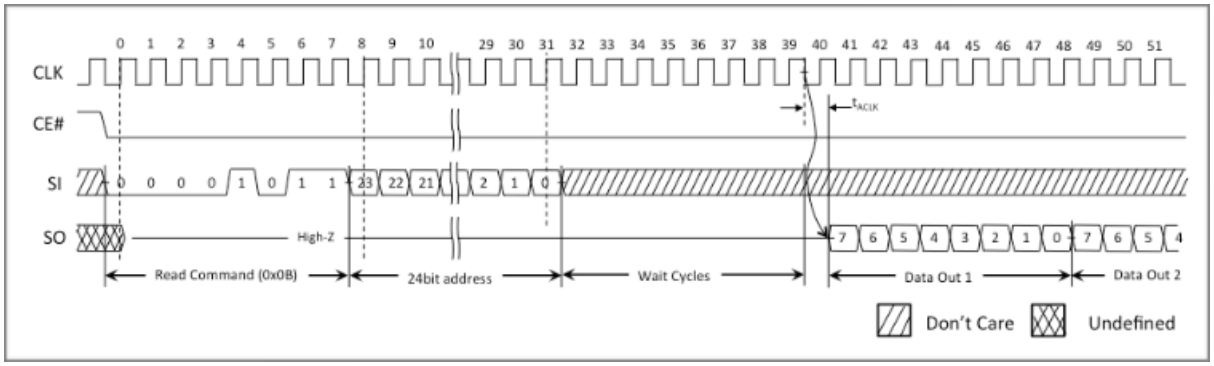

Figure 5-2. SPI Read 0x0B (Max frequency: 104 MHz)

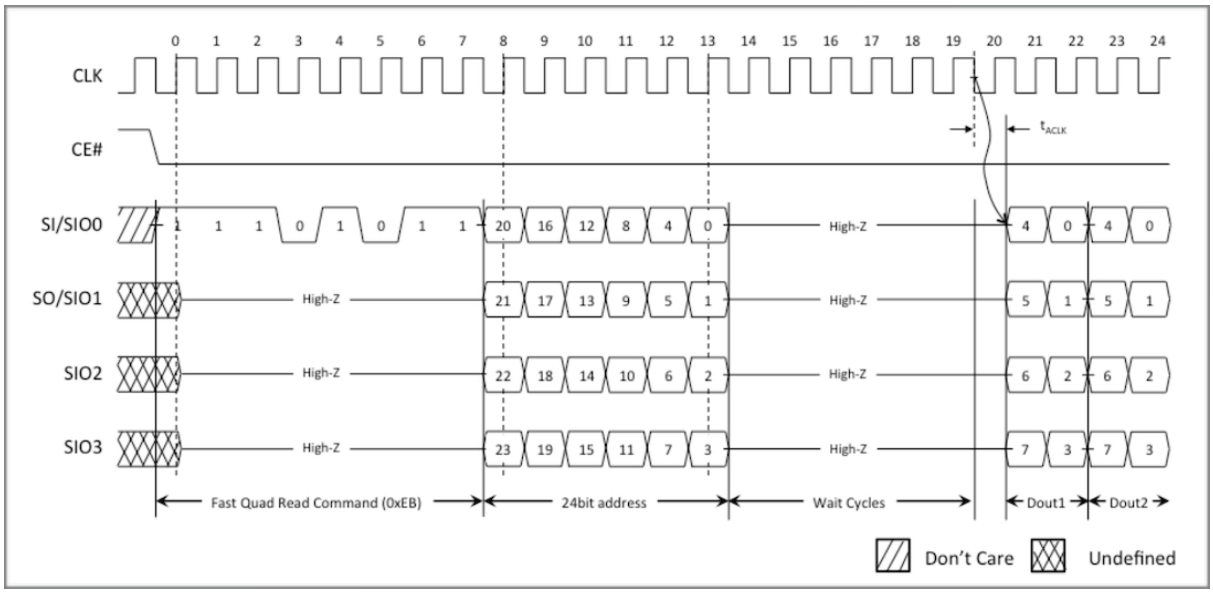

Figure 5-3. SPI Fast Quad Read 0xEB (Max frequency: 104 MHz)

5.2. SPI Write Operations

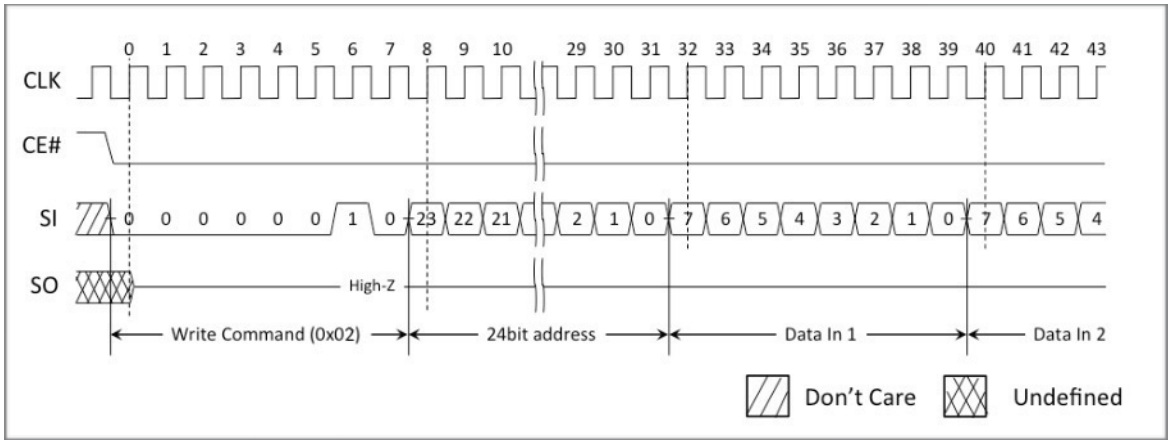

Figure 5-4. SPI Write Command 0x02

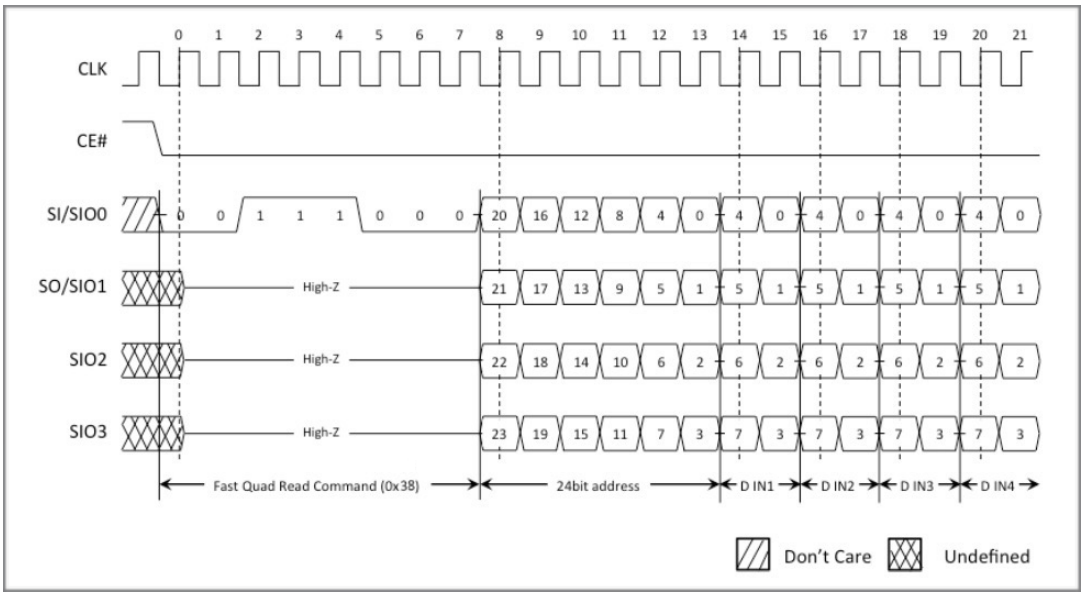

Figure 5-5. SPI Quad Write Command 0x38

5.3. QPI Mode

This command switches the device into quad IO mode.

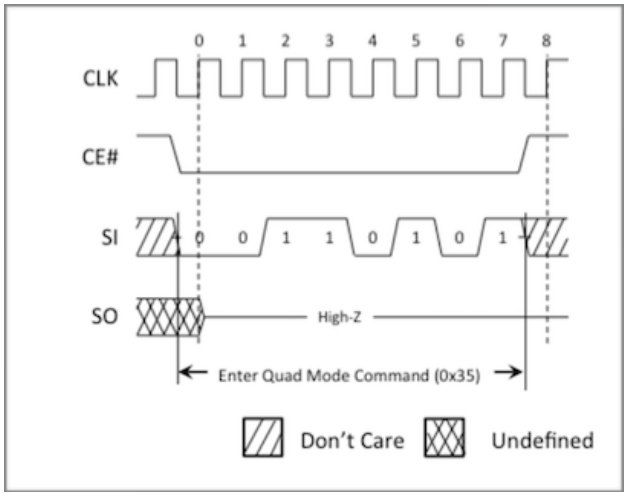

Figure 5-6. Quad Mode Enable 0x35

5.4. SPI Read ID Operation

This command is similar to Fast Read. But it has no wait cycles and the device outputs EID value instead of data.

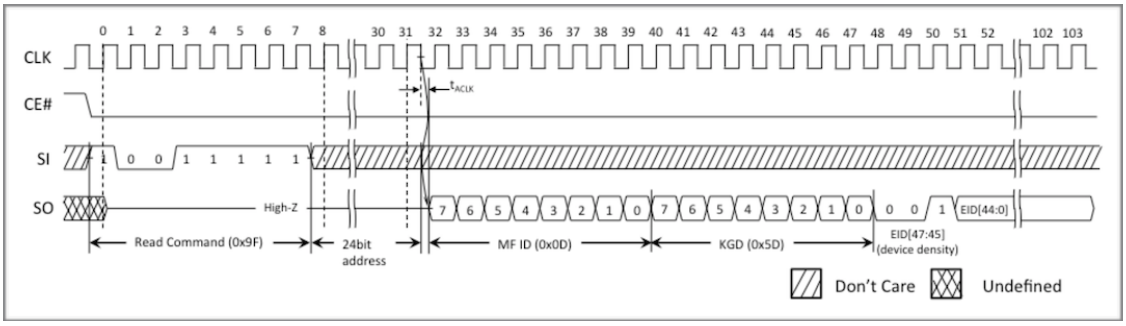

Figure 5-7. SPI Read ID 0x9F (Available Only in SPI Mode)

Table 5-1. Known Good Die (KGD)

KDG[7:0]	Known Good Die Register
0x5D	Pass
0x55	Fail

> 📖 ***Note:***
>
> Default value on this register is (0x55=fail). After the all tests passed then programed as (0x5D= PASS) in manufacturing process.

6. Operations in QPI Mode

6.1. QPI Read Operations

For all reads, data will be available for tACLK after the falling edge of CLK. QPI reads can be done in two ways:

1. 0x0B: Quad CMD, Quad IO, slow frequency
2. 0xEB: Quad CMD, Quad IO, fast frequency

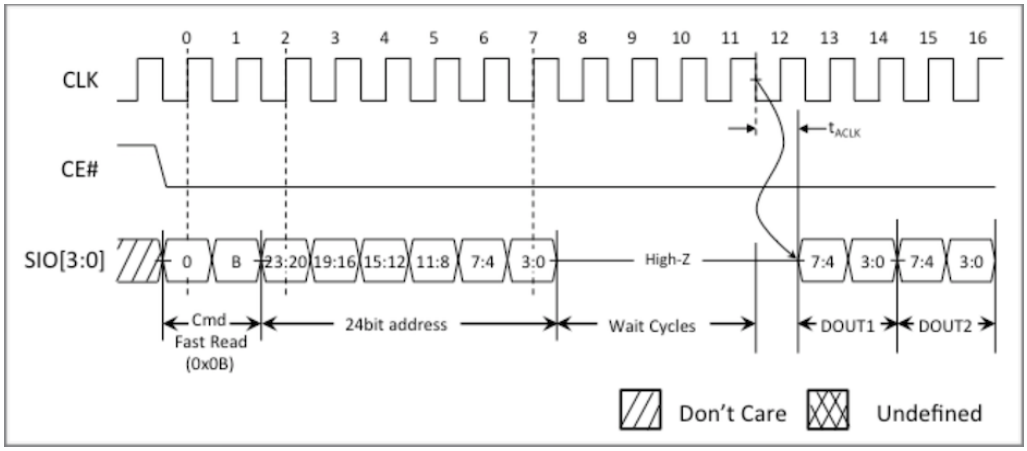

Figure 6-1. QPI Fast Read 0x0B (Max Frequency: 84 MHz)

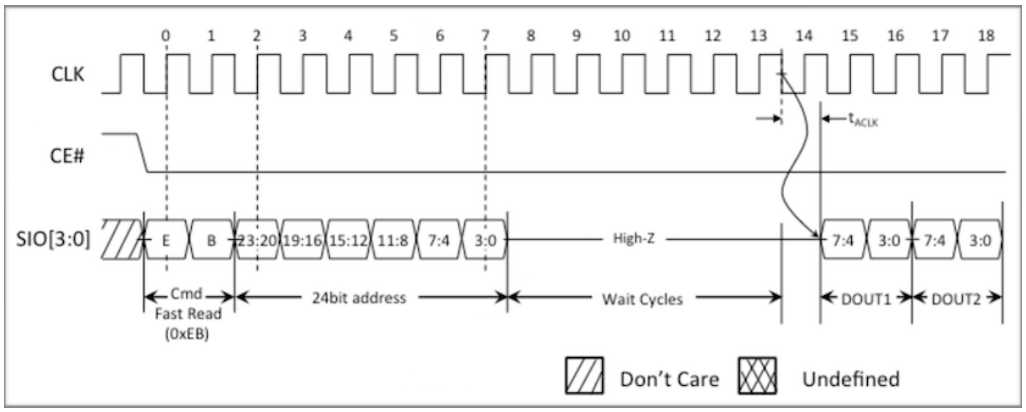

Figure 6-2. QPI Fast Read 0xEB (Max Frequency: 104 MHz)

6.2. QPI Write Operations

QPI write command can be input as 0x02 or 0x38. It has nothing to do with clock frequency.

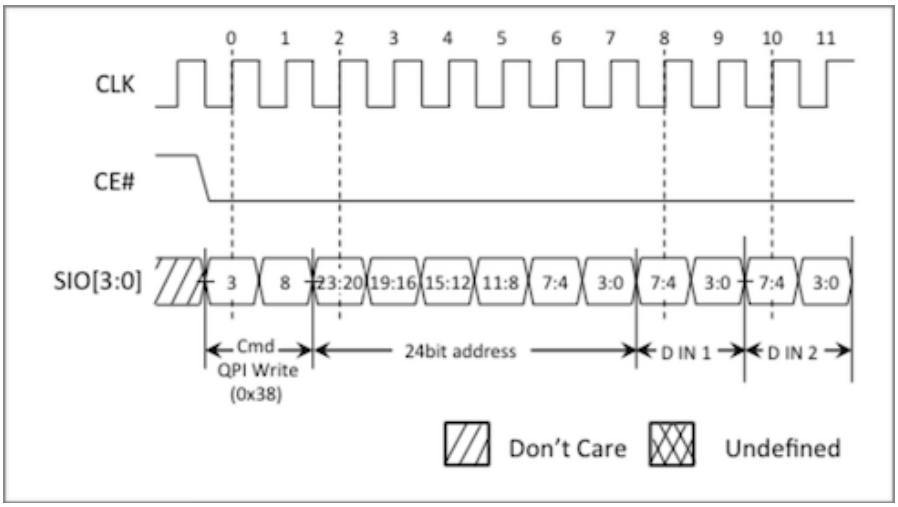

Figure 6-3. QPI Write 0x02 or 0x38

6.3. QPI Quad Mode Exit Operation

This command will switch the device back into serial IO mode.

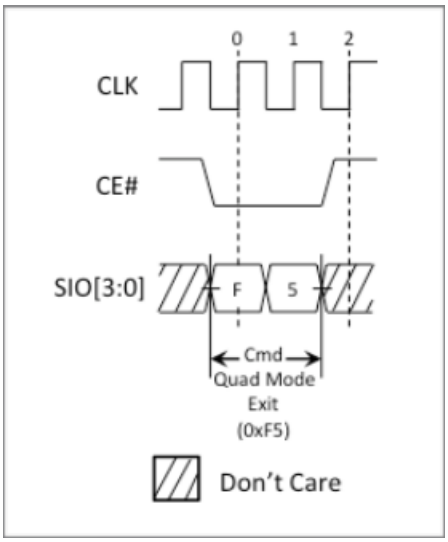

Figure 6-4. Quad Mode Exit 0xF5 (Only Available in QPI Mode)

7. Reset Operation

The reset operation is used as a system (software) reset that puts the device in SPI standby mode, which is also the default mode after power-up. This operation consists of two commands: Reset Enable (RSTEN) and Reset (RST).

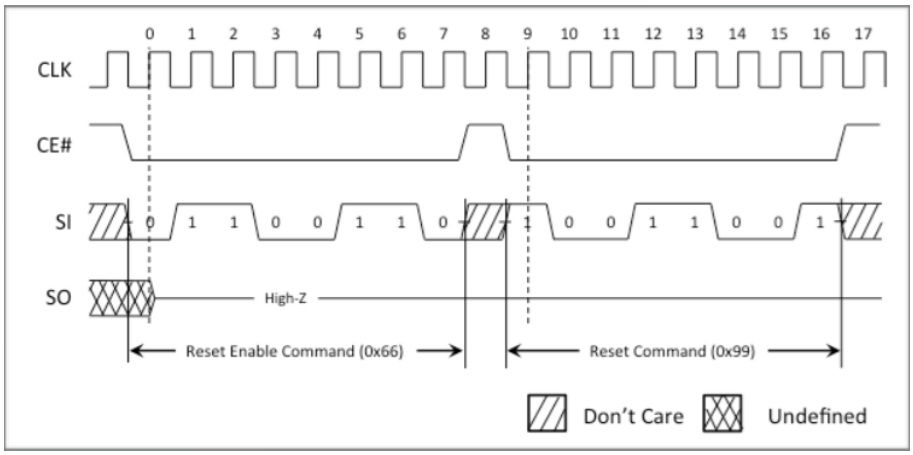

Figure 7-1. SPI Reset

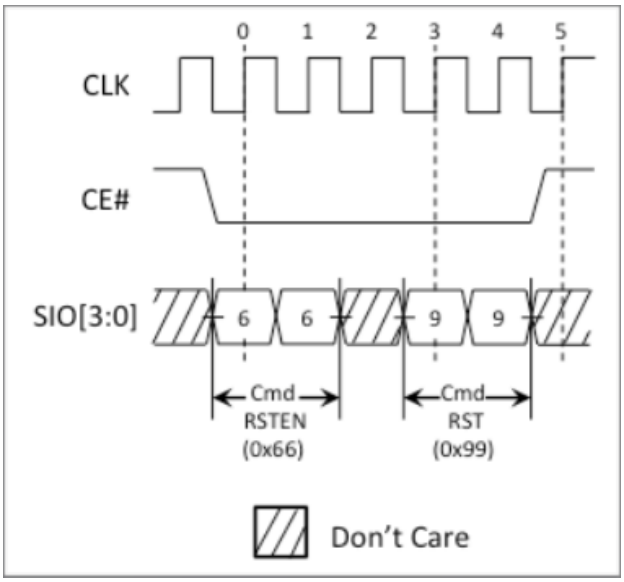

Figure 7-2. QPI Reset

The reset operation requires the `Reset Enable` command to be followed by the `Reset` command. Any command other than the `Reset` command after the `Reset Enable` command will disable the `Reset Enable` procedure.

8. Set Burst Length Operation

The set burst length operation toggles the device's burst length wrap between 1024 and 32. The default burst length is 1024.

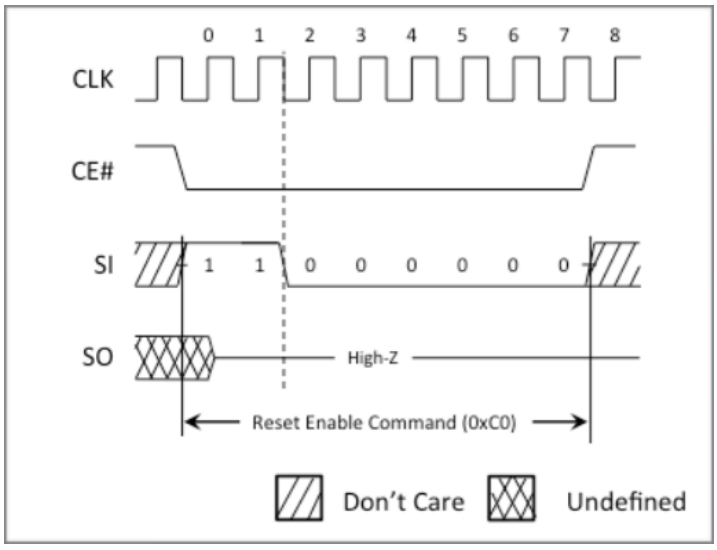

Figure 8-1. SPI Set Burst Length 0xC0

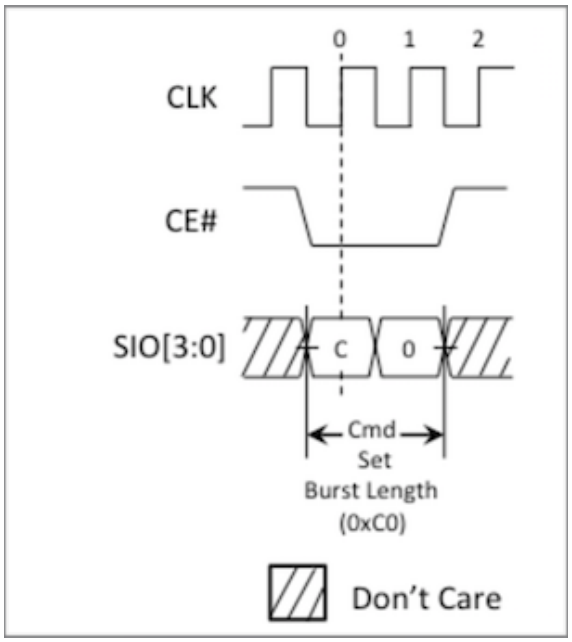

Figure 8-2. QPI Set Burst Length 0xC0

9. Input/Output Timing

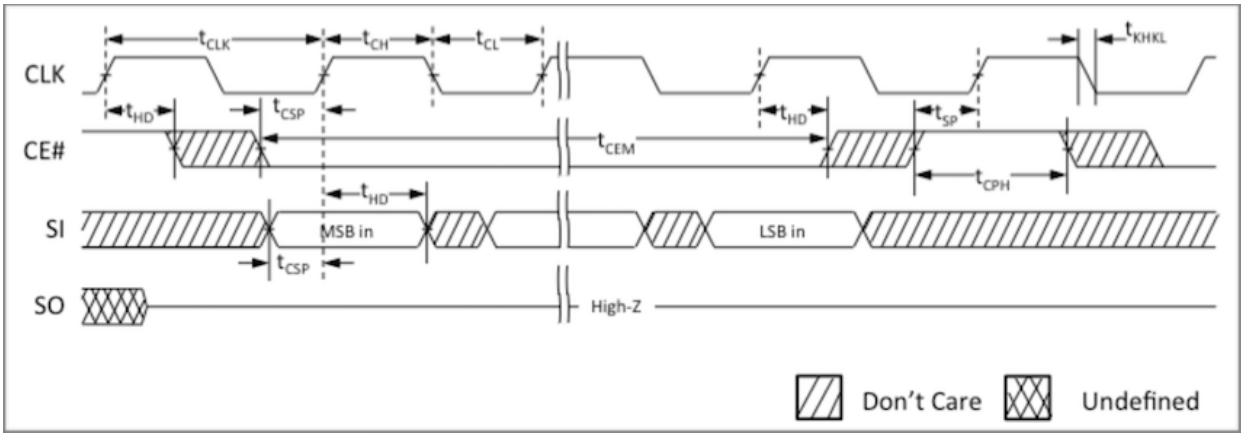

Figure 9-1. Input Timing

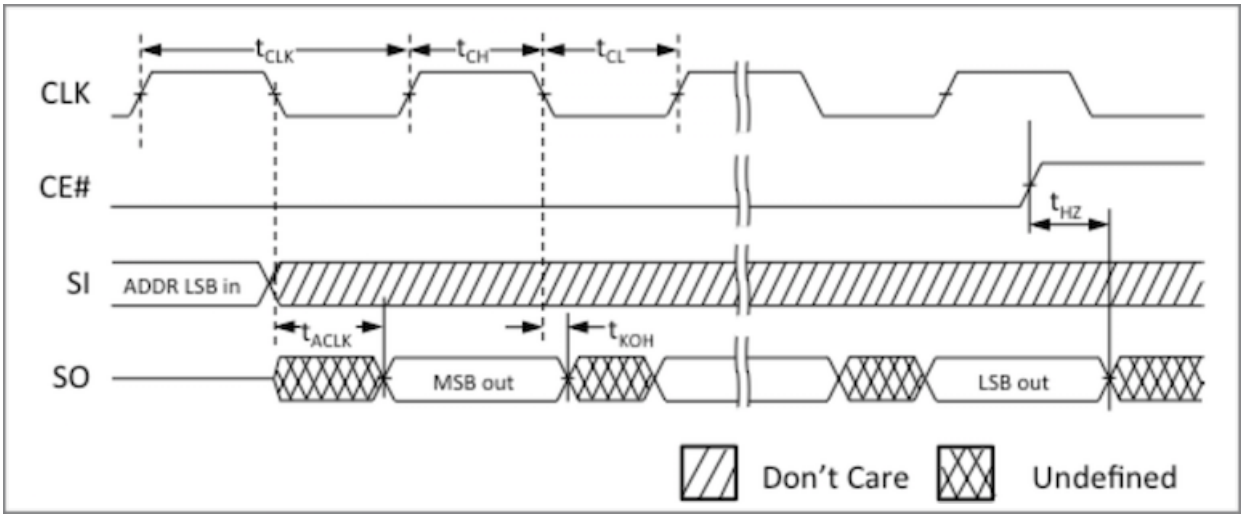

Figure 9-2. Output Timing

10. Electrical Specifications

10.1. Absolute Maximum Ratings

Table 10-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit	Notes
VT	Voltage to any ball except VDD relative to VSS	-0.3 to VDD + 0.3	V	-
VDD	Voltage on VDD supply relative to VSS	-0.2 to +2.45	V	-
TSTG	Storage Temperature	–55 to +150	°C	1

📖 ***Note:***

Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

⚠ ***Notice:***

Exposing the device to stress above the listed absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits specified in this document.

10.2. Operating Condition

Table 10-2. Operating Temperature

Parameter	Min	Max	Unit
Operating temperature (standard)	-25	85	°C

10.3. DC Characteristics

Table 10-3. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
VDD	Supply voltage	1.62	1.98	V	-
VIH	Input high voltage	VDD - 0.4	VDD+0.2	V	-
TIL	Input low voltage	-0.2	0.4	V	1
VOH	Output high voltage (IOH=0.2 mA)	0.8 VDD	-	V	-
VOL	Output low voltage (IOL=0.2 mA)	-	0.2 VDD	V	-
ILI	Input leakage current	-	1	mA	-

Symbol	Parameter	Min	Max	Unit	Notes
VDD	Supply voltage	1.62	1.98	V	-
ILI	Input leakage current	-	1	mA	-
ILO	Output leakage current	-	1	mA	-
ICC	Read/Write	-	25	mA	-
ISB	Standby current	-	50	µA	*typical

10.4. AC Characteristics

Table 10-4. Read/Write Timing

Symbol	Parameter	Min	Max	Unit	Notes
t_{CLK}	CLK period—SPI Read (0x5D)	30.3	-	ns	33 MHz
	CLK period—QPI Fast Read (0x0B)	11.9			84 MHz
	CLK period—QPI Fast Read (the other operations)	9.6			104 MHz
t_{CH}/t_{CL}	Clock high/low width	0.45	0.55	t_{CLK}	-
t_{KHKL}	Clock rise or fall time	-	1.5	ns	-
t_{CPH}	CE# high between subsequent burst operations	1	-	t_{CLK}	-
t_{CEM}	CE# low pulse width	-	4	µs	-
t_{CSP}	CE# setup time to CLK rising edge	3	-	ns	-
t_{SP}	Setup time to active CLK edge	2.5	-		-
t_{HD}	Hold time from active CLK edge	2	-		-
t_{HZ}	Chip disable to DQ output high–Z	-	7	ns	-
t_{ACLK}	CLK to output delay	-	7		-
t_{KOH}	Data hold time from clock falling edge	1.5	-		-

11. Package Information

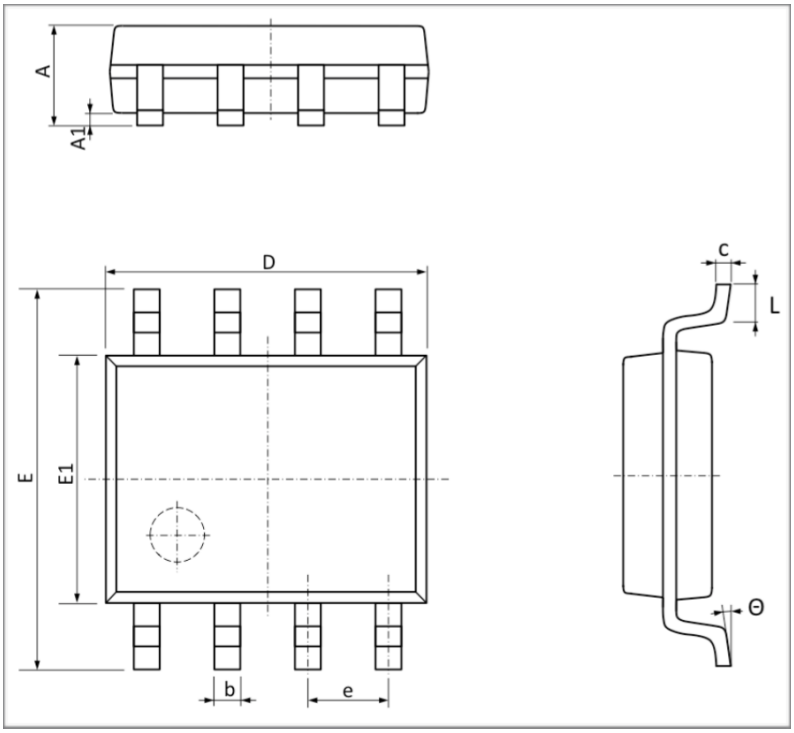

Figure 11-1. Package Diagram

Table 11-1. Package Dimension (Unit: mm)

Symbol	Min	Max
A	1.35	1.75
A1	0.05	0.10
b	0.35	0.47
c	0.15	0.25
D	4.75	5.05
E1	3.80	4.00
E	5.80	6.20
e	1.27 (TYP.)	
L	0.40	0.80
Θ	0°	8°

A. Appendix–Device Marking Convention

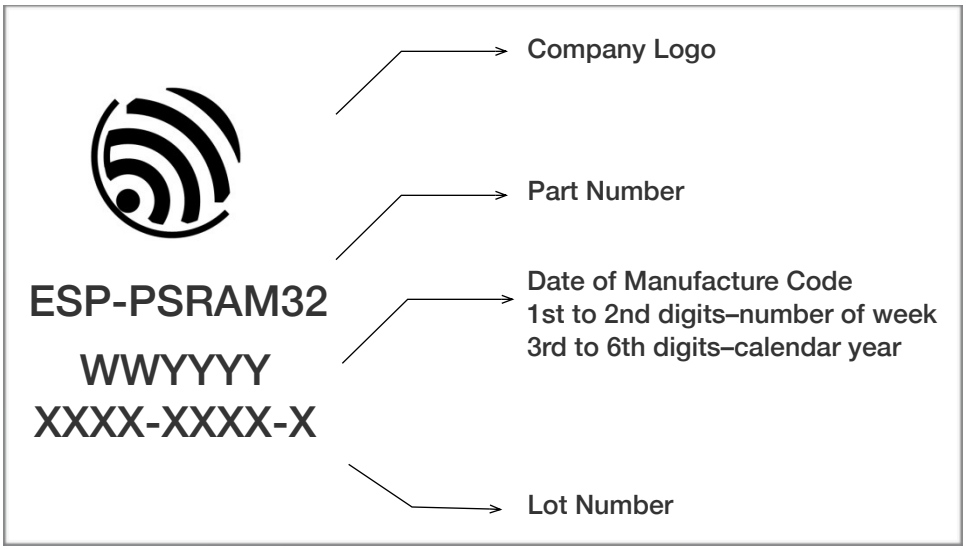

Figure A-1. Device Marking of ESP-PSRAM32

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