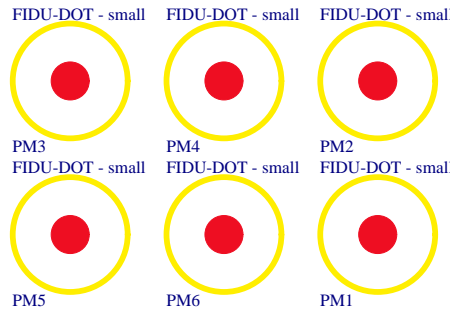
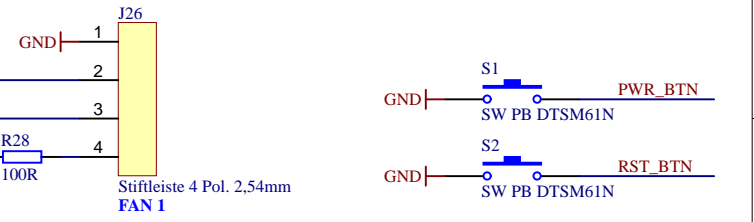
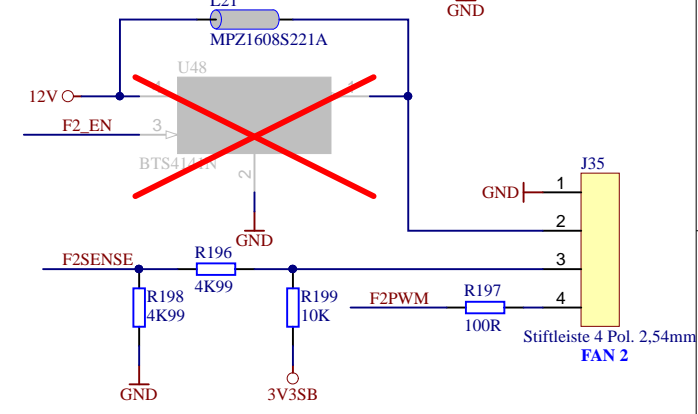
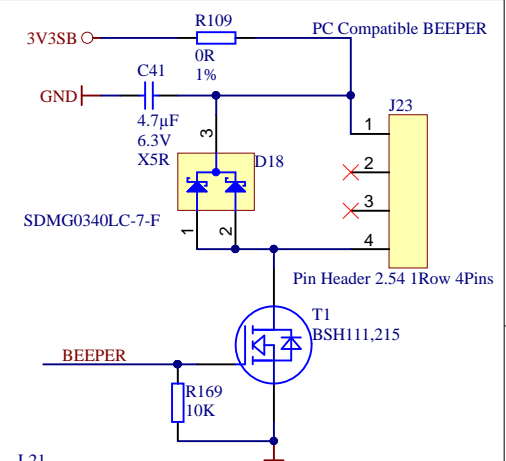
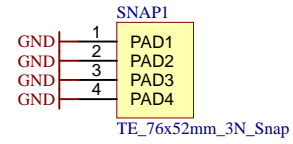
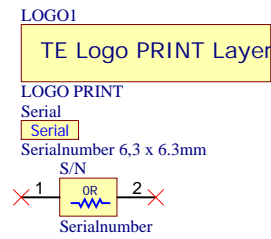
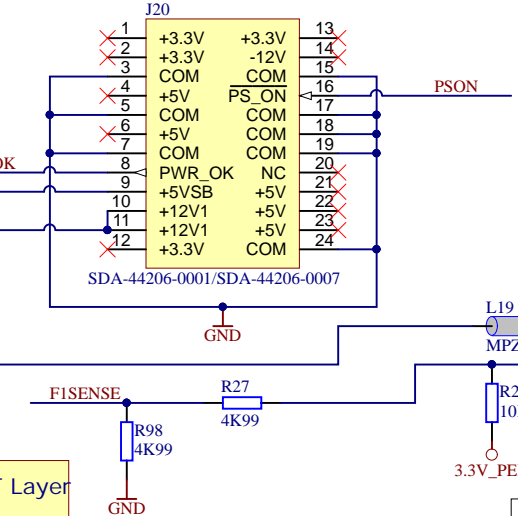
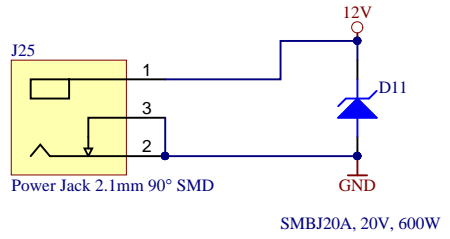
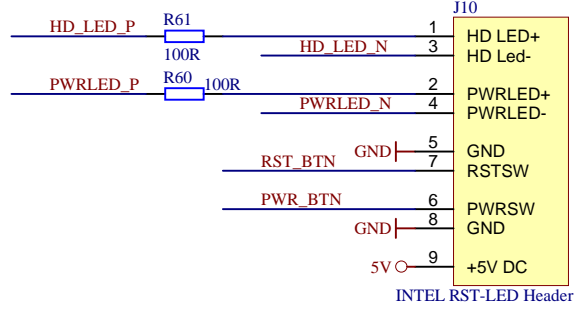


- U_B2B
B2B.schdoc
- U_USB3-HUB
USB3-HUB.SchDoc
- U_PClE
PClE.schdoc
- U_SFP
SFP.schdoc
- U_SC
SC.schdoc
- U_SC2
SC2.schdoc
- U_PMOD
PMODE.schdoc
- U_XMOD
XMOD.schdoc
- U_Power_1
Power_1.schdoc
- U_Power_2
Power_2.schdoc
- U_Power_3
Power_3.schdoc
- U_Power_4
Power_4.schdoc
- U_FMC
FMC.SchDoc
- U_FMC PWR
FMC PWR.SchDoc
- U_FMC MISC
FMC_MISC.SchDoc
- U_RC
Revision_Changes.SchDoc
- U_DP_PS
DP_PS.schdoc
- U_SATA
SATA.schdoc
- U_USB-CONN
USB-CONN.schdoc
- U_USB
USB.schdoc
- U_USB-PHY
USB-PHY.SchDoc
- U_ETH-PHY
ETH-PHY.SchDoc
- U_I2C_system
I2C_system.schdoc
- U_CLK
CLK.schdoc
- U_CLK_MUX
CLK_MUX.schdoc
- U_SD
SD.schdoc
- U_EMMC
eMMC.SchDoc
- U_FIREFLY
FireFly.SchDoc
- U_MISC
MISC.schdoc
- U_Audio
Audio.SchDoc
- U_BD
BD.SchDoc

INTEL Reset/LED Pinout



Title: TEBF0808 - Mini-ITX Top Sheet		
A4	Number: TEBF0808 TEBF0808	Rev. 04
Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page1 of 36
Filename: TEBF0808.schdoc		

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A

A

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D

D

U_J1
 J1.schdoc
 U_J2
 J2.schdoc
 U_J3
 J3.schdoc
 U_J4
 J4.schdoc



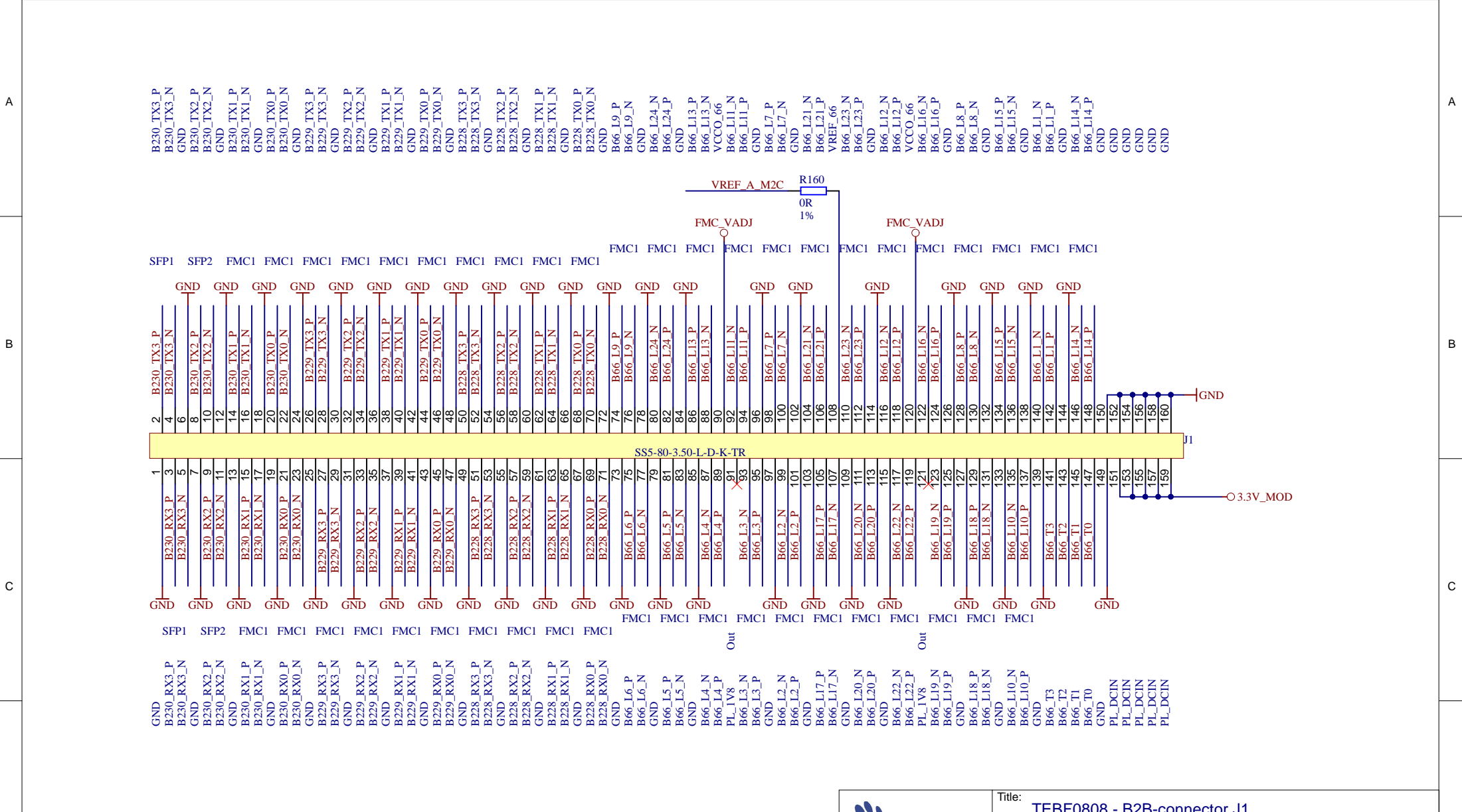
Title: TEBF0808 - B2B-connectors		
A4	Number: TEBF0808 TEBF0808	Rev. 04
Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page 2 of 36
Filename: B2B.schdoc		


1

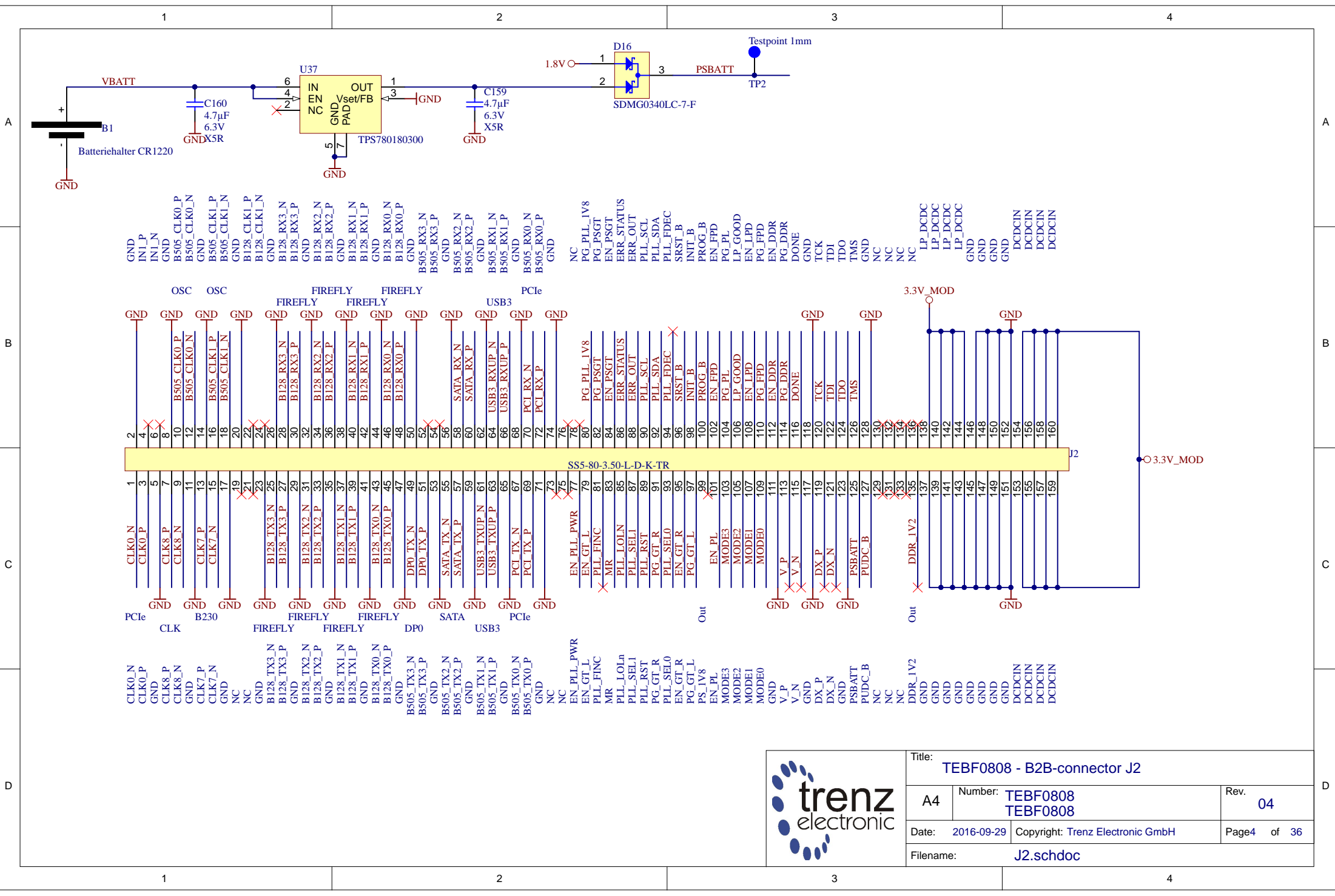
2

3

4



			Title: TEBF0808 - B2B-connector J1	
			A4 Number: TEBF0808 TEBF0808	Rev. 04
Date: 2016-09-29		Copyright: Trenz Electronic GmbH		Page 3 of 36
Filename: J1.schdoc				



Title: TEBF0808 - B2B-connector J2		
A4	Number: TEBF0808 TEBF0808	Rev. 04
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Filename: J2.schdoc		

A
B
C
D

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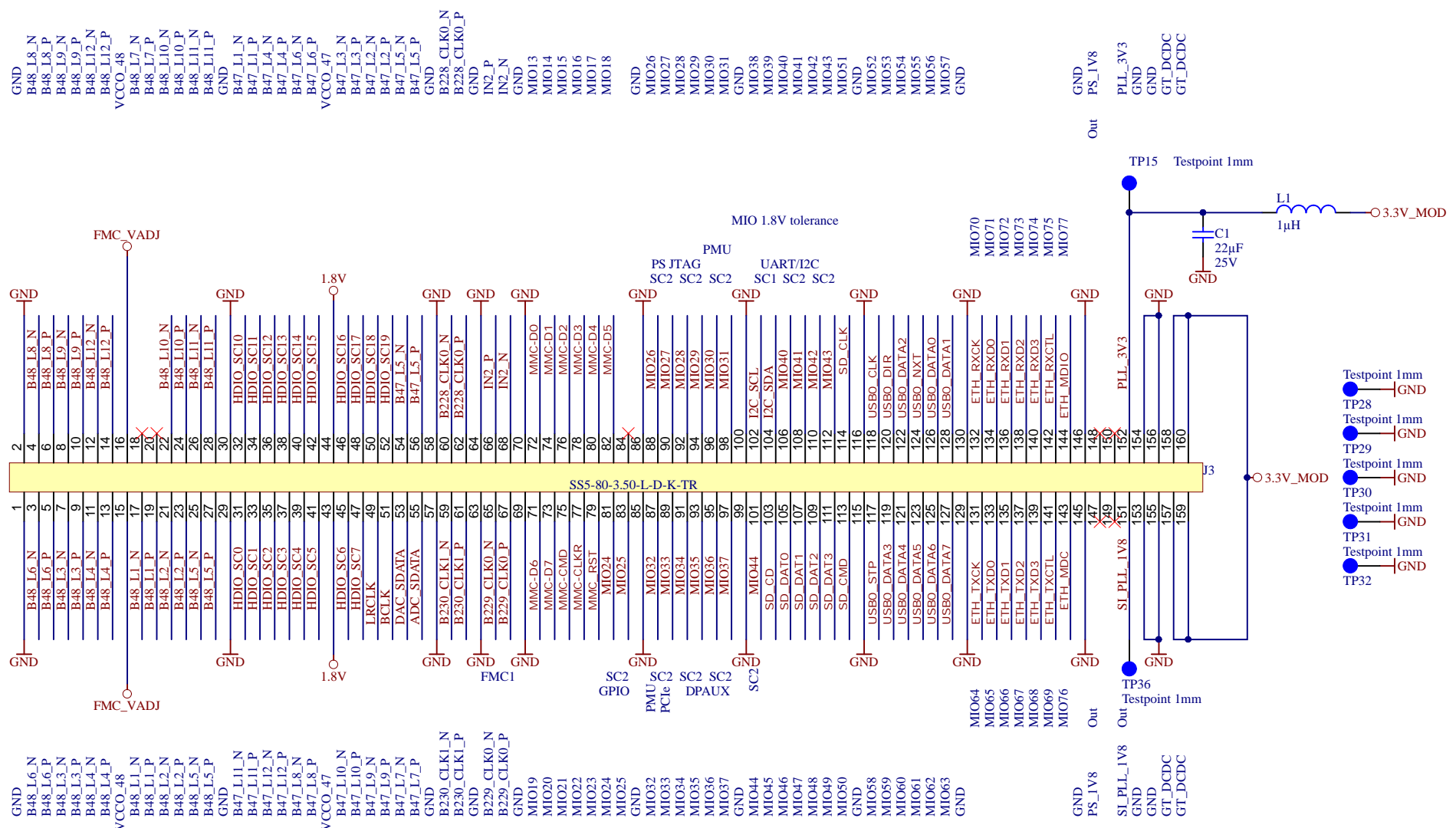
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1

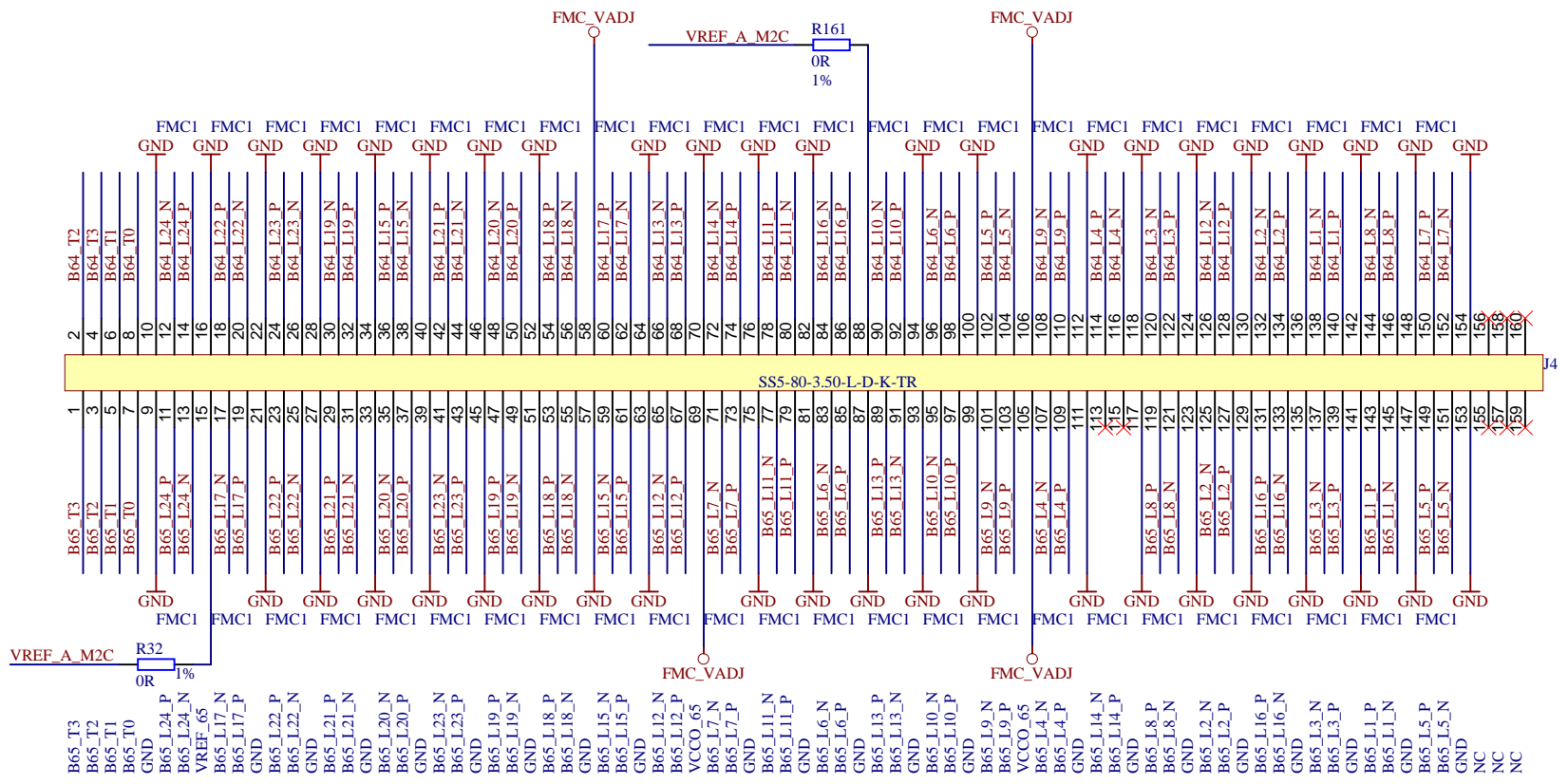
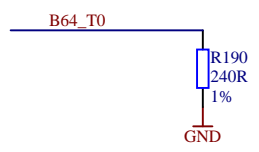
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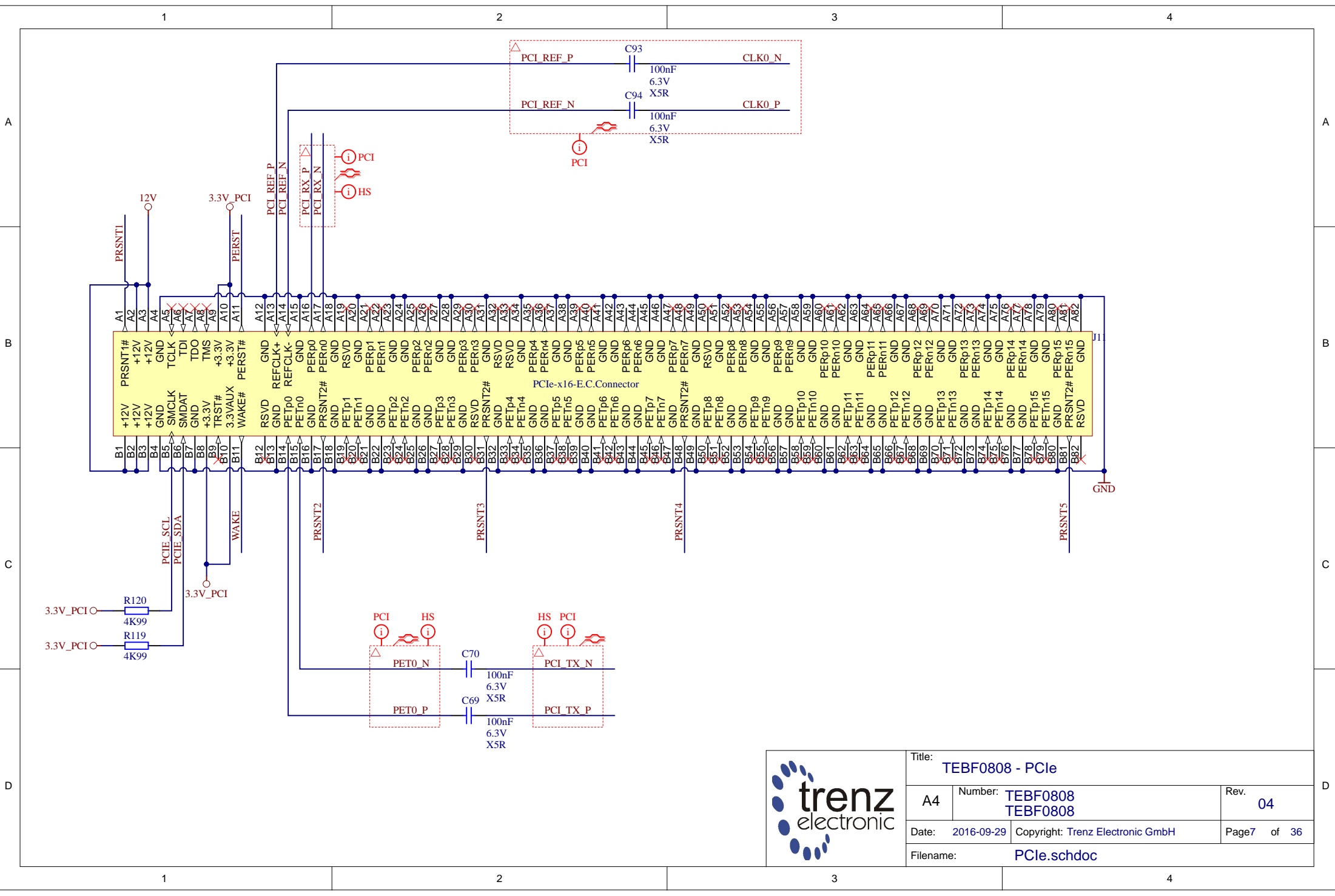
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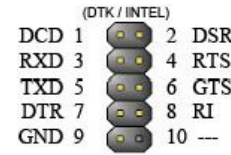
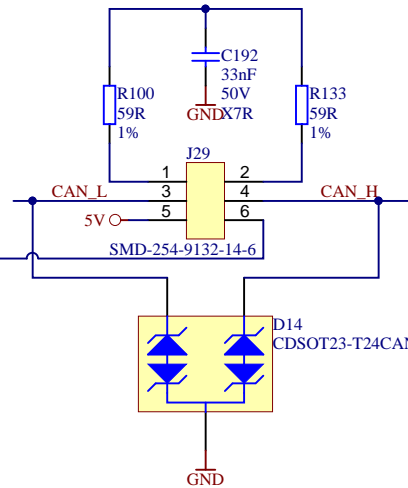
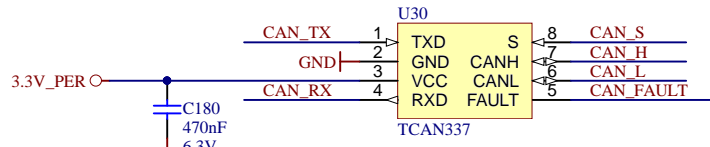
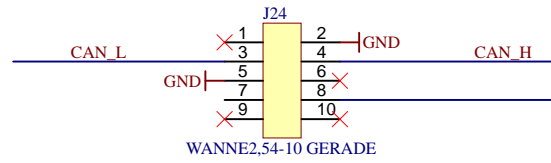
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A4	Number: TEBF0808 TEBF0808	Rev. 04
Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page5 of 36
Filename: J3.schdoc		



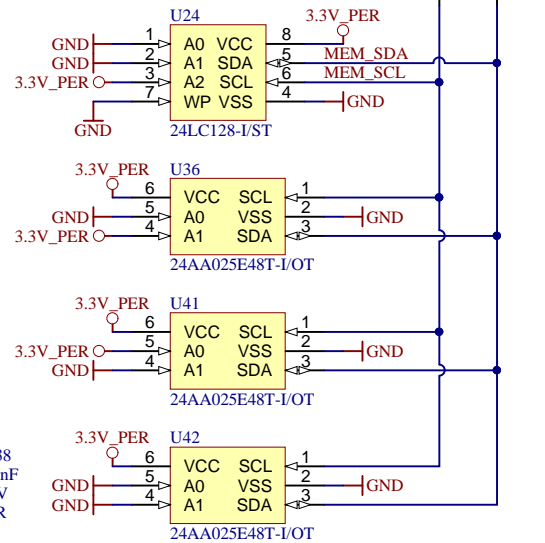
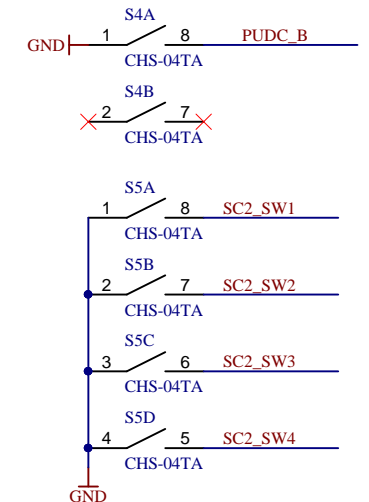
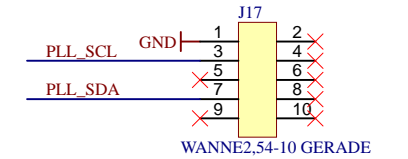
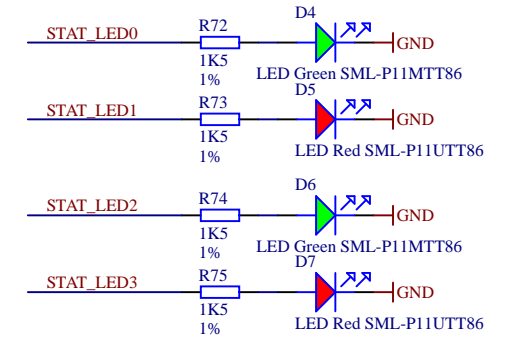
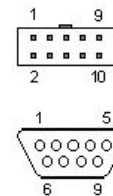
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A4	Number: TEBF0808 TEBF0808	Rev. 04
Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page6 of 36
Filename: J4.schdoc		



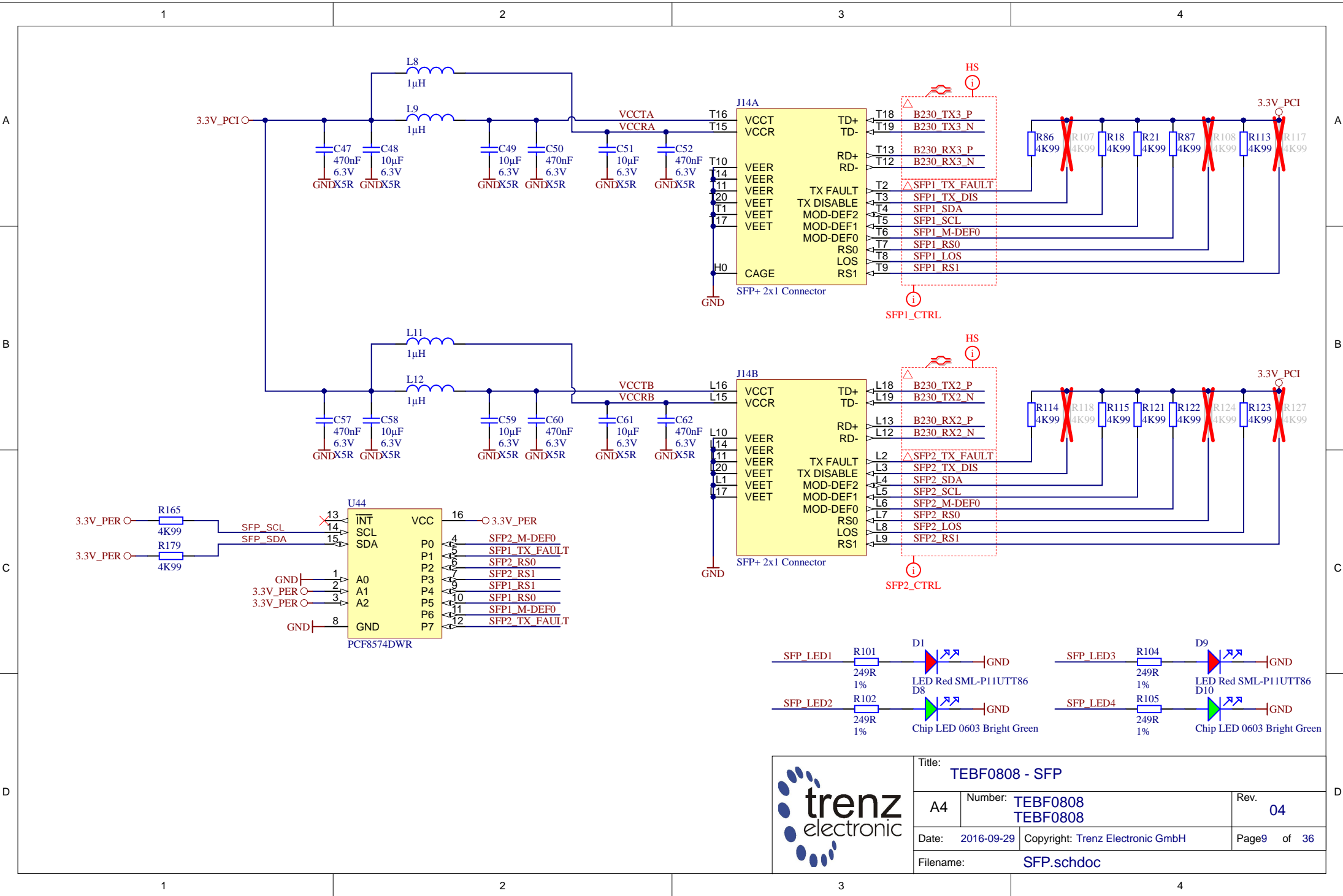
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A4	Number: TEBF0808 TEBF0808	Rev. 04
Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page 7 of 36
Filename: PCIe.schdoc		




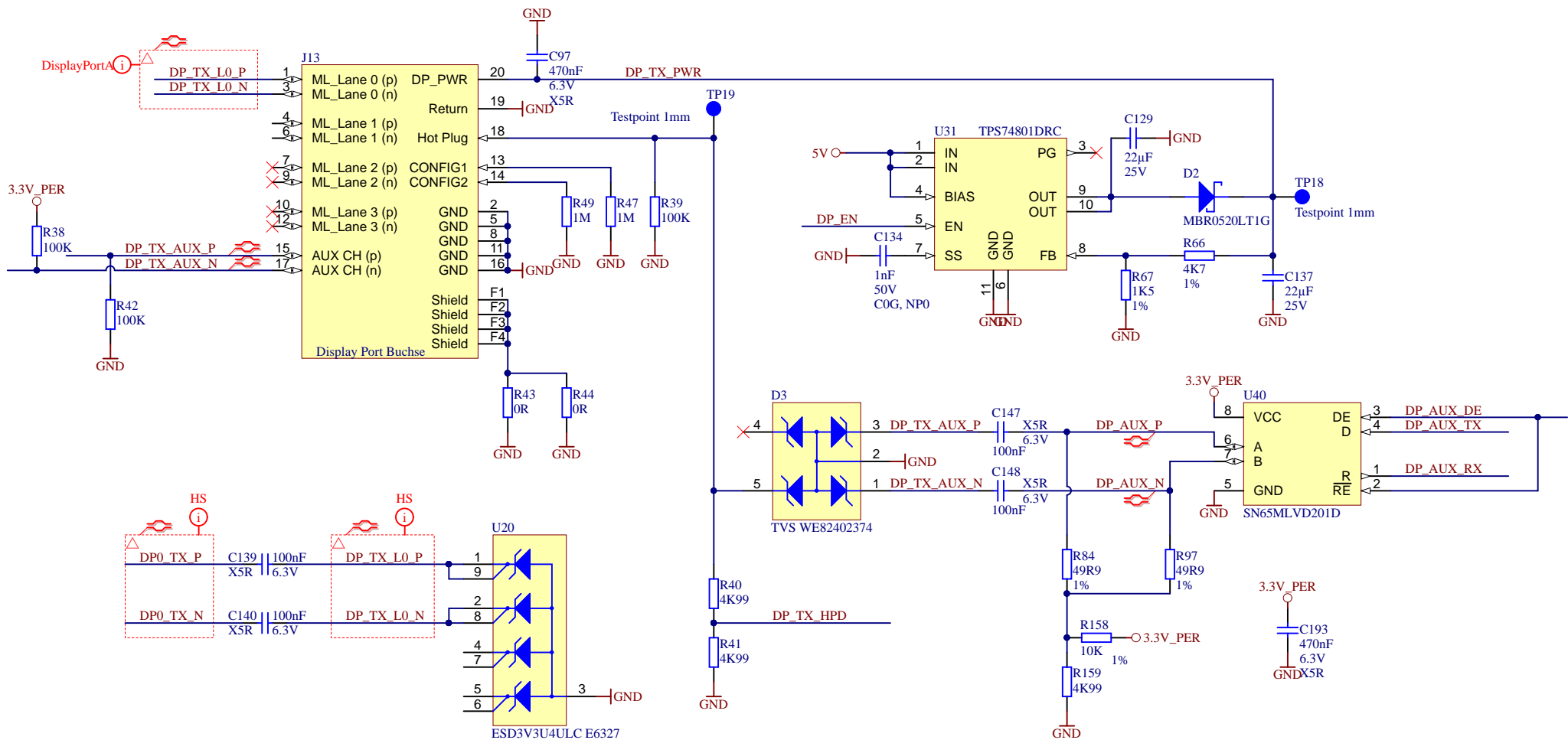
- 1 - 1
- 2 - 3
- 3 - 5
- 4 - 7
- 5 - 9
- 6 - 2
- 7 - 4
- 8 - 6
- 9 - 8
- 10 --



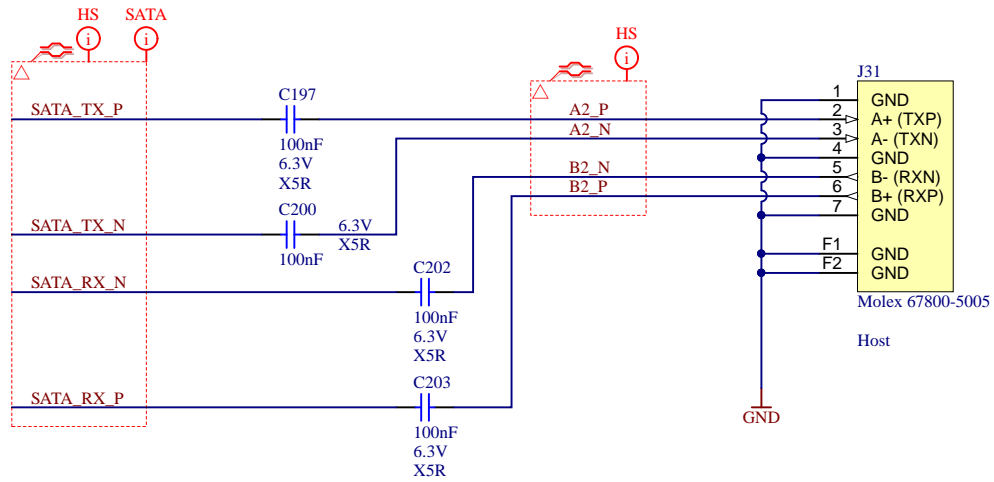
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A4	Number: TEBF0808 TEBF0808	Rev. 04
Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page 8 of 36
Filename: MISC.schdoc		




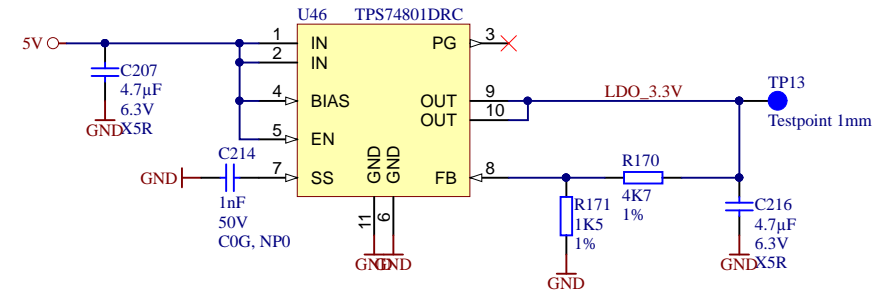
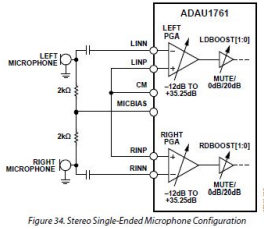
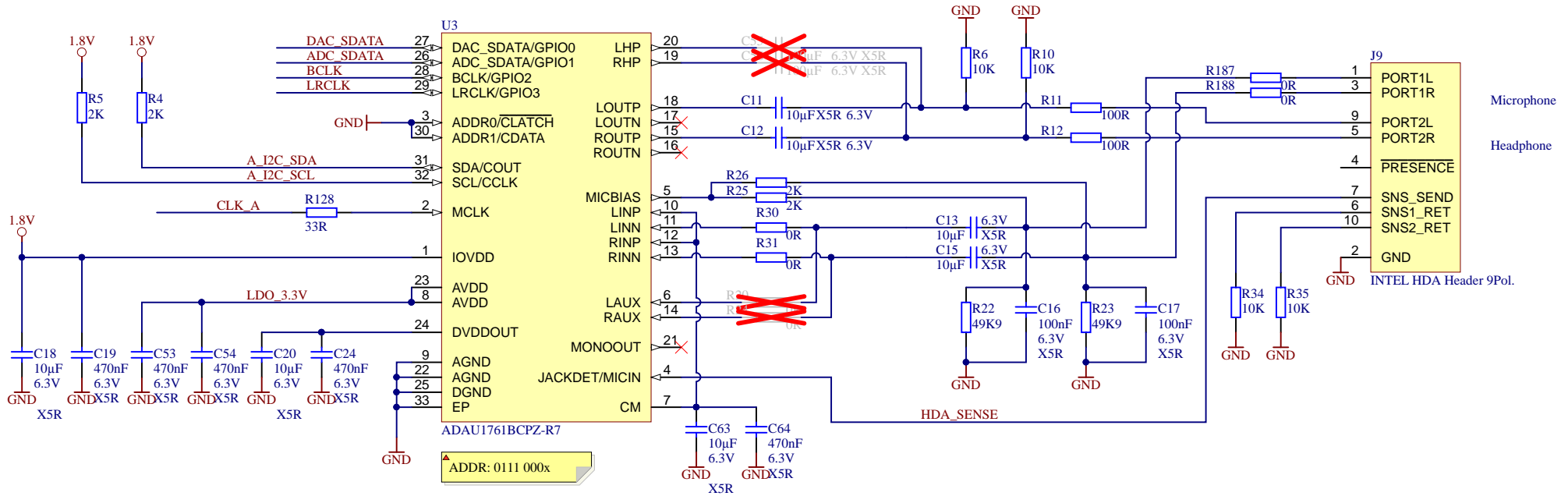
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	A4	Number: TEBF0808 TEBF0808
	Date: 2016-09-29	Copyright: Trenz Electronic GmbH
	Filename: SFP.schdoc	Rev. 04
		Page 9 of 36



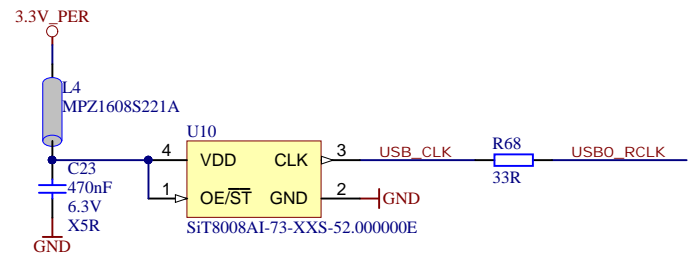
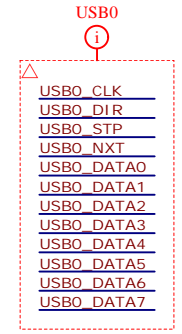
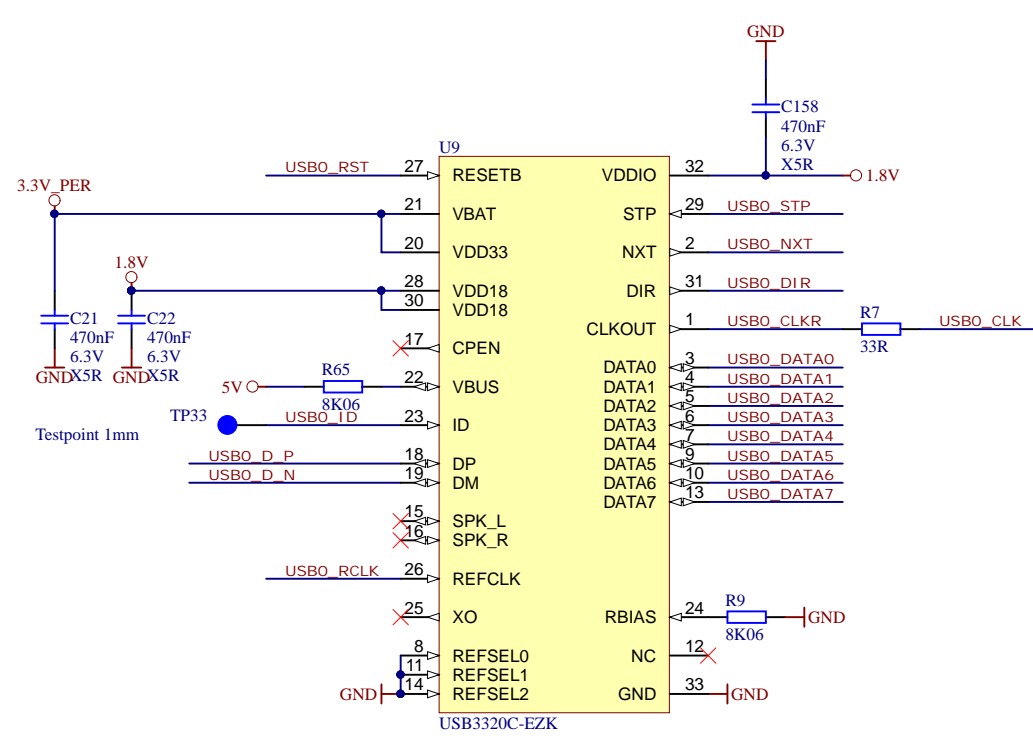
Title: TEBF0808 - DisplayPort		
A4	Number: TEBF0808 TEBF0808	Rev. 04
Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page 10 of 36
Filename: DP_PS.schdoc		



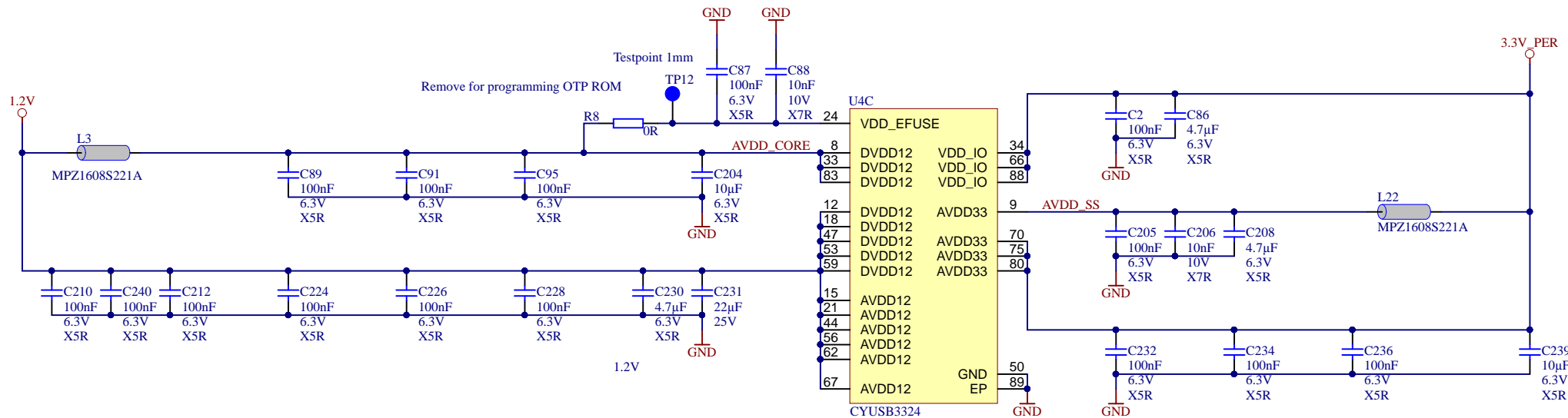
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	A4	Number: TEBF0808 TEBF0808	Rev. 04
	Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page 11 of 36
	Filename: SATA.schdoc		



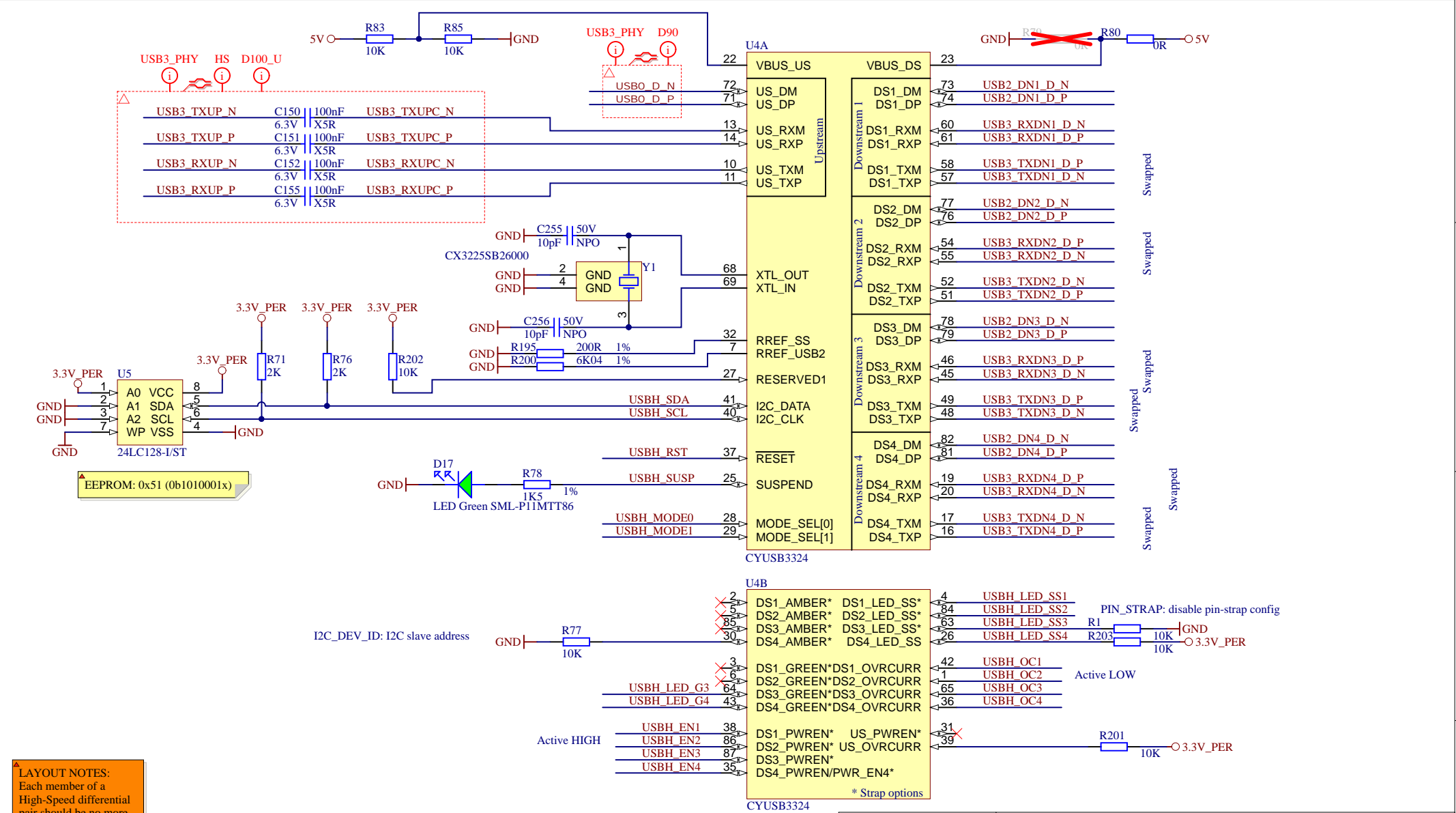
	Title: TEBF0808 - Audio	
	A4	Number: TEBF0808 TEBF0808
	Date: 2016-09-29	Rev. 04
	Copyright: Trenz Electronic GmbH	Page 12 of 36
Filename: Audio.SchDoc		



Title: TEBF0808 - USB		
A4	Number: TEBF0808 TEBF0808	Rev. 04
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Filename: USB-PHY.SchDoc		



Title: TEBF0808 - USB		
A4	Number: TEBF0808 TEBF0808	Rev. 04
Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page 14 of 36
Filename: USB.schdoc		



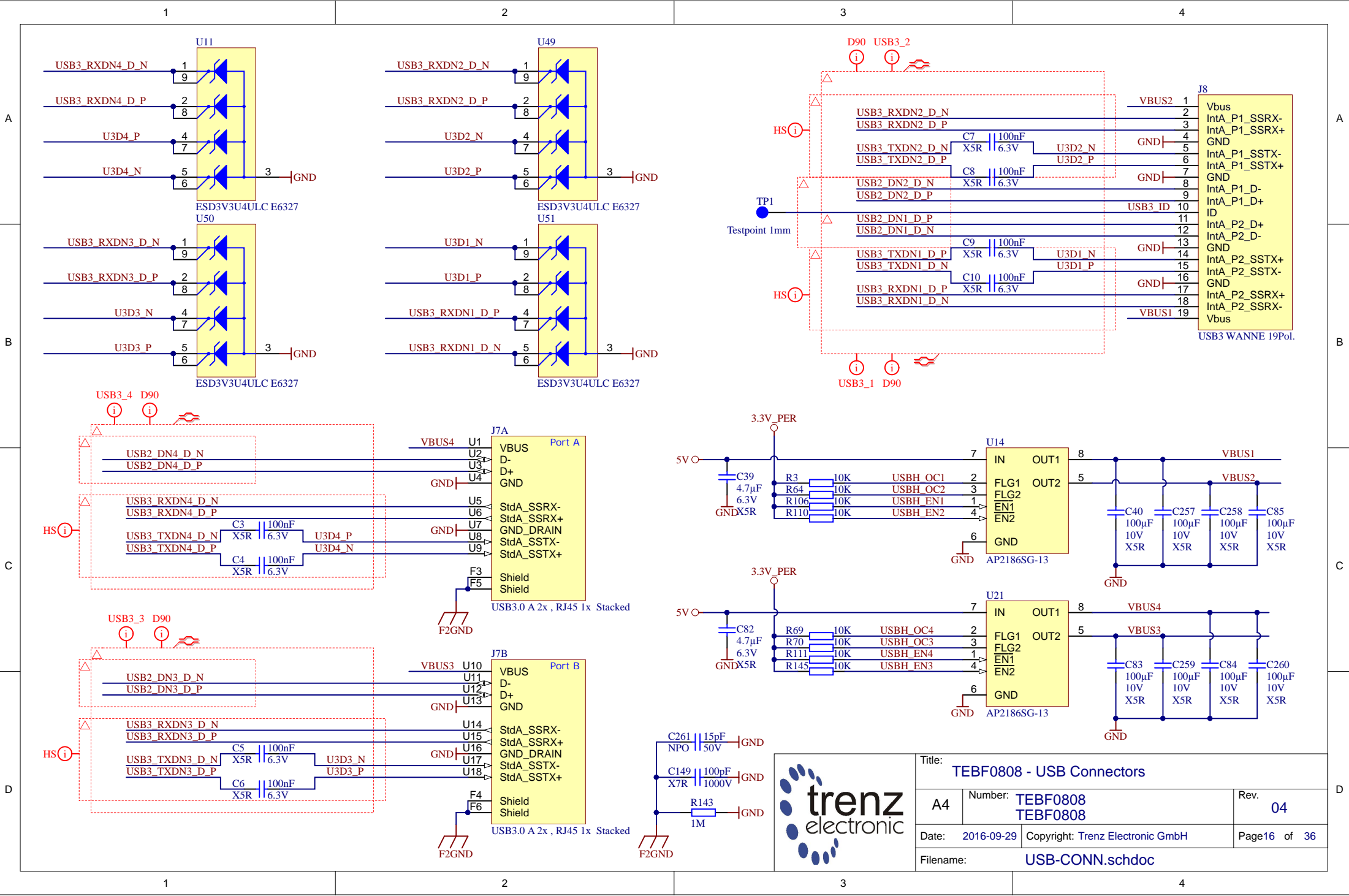
LAYOUT NOTES:
 Each member of a High-Speed differential pair should be no more than 1.25 mm
 Each member of a SuperSpeed differential pair should be no more than 0.13 mm

RESETN pin should be held LOW until both supplies become stable.

CLK: 0x60 (or 0x58)



Title: TEBF0808 - USB		
A4	Number: TEBF0808 TEBF0808	Rev. 04
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Filename: USB3-HUB.SchDoc		



Title: TEBF0808 - USB Connectors		
A4	Number: TEBF0808 TEBF0808	Rev. 04
Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page 16 of 36
Filename: USB-CONN.schdoc		

1

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A

A

B

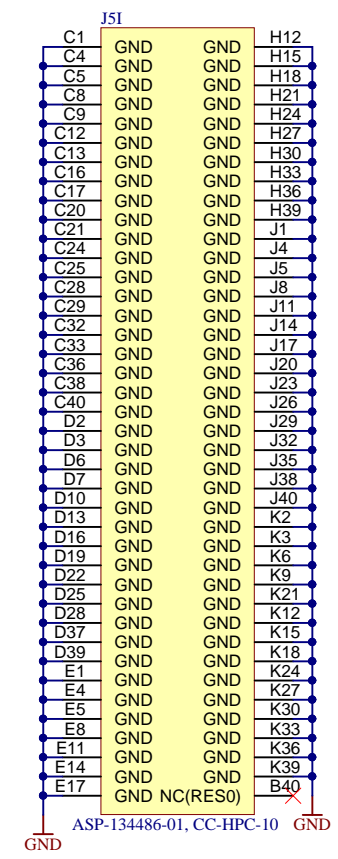
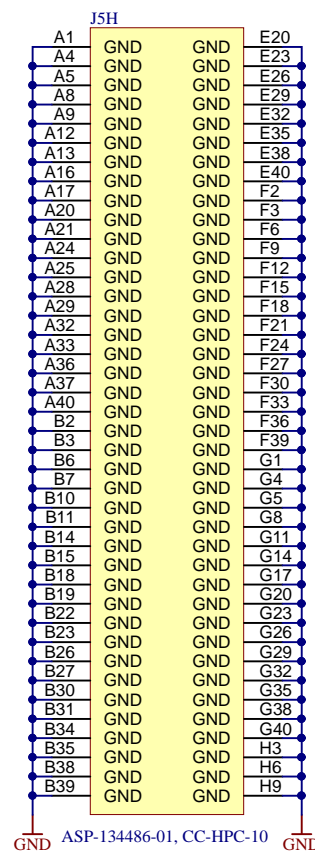
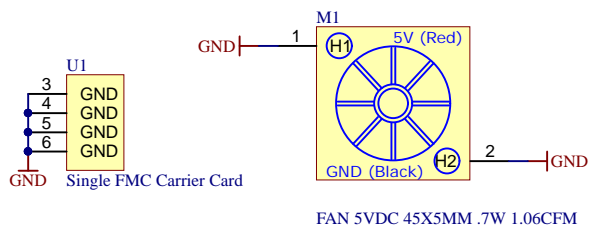
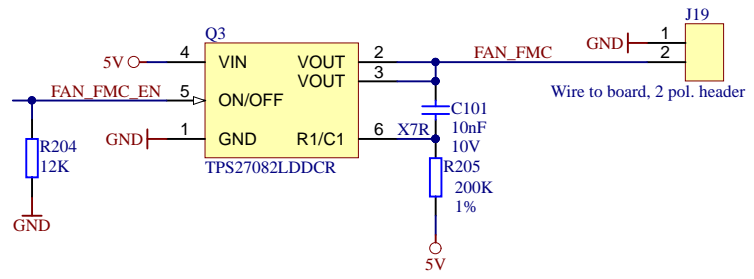
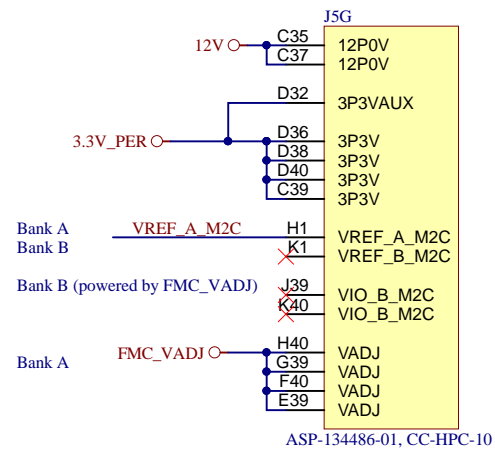
B

C

C

D

D



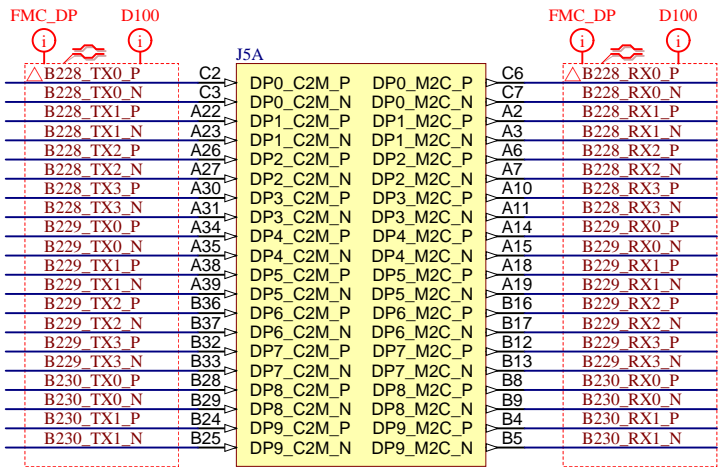
Title: TEBF0808 - FMC		
A4	Number: TEBF0808 TEBF0808	Rev. 04
Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page 17 of 36
Filename: FMC PWR.SchDoc		

1

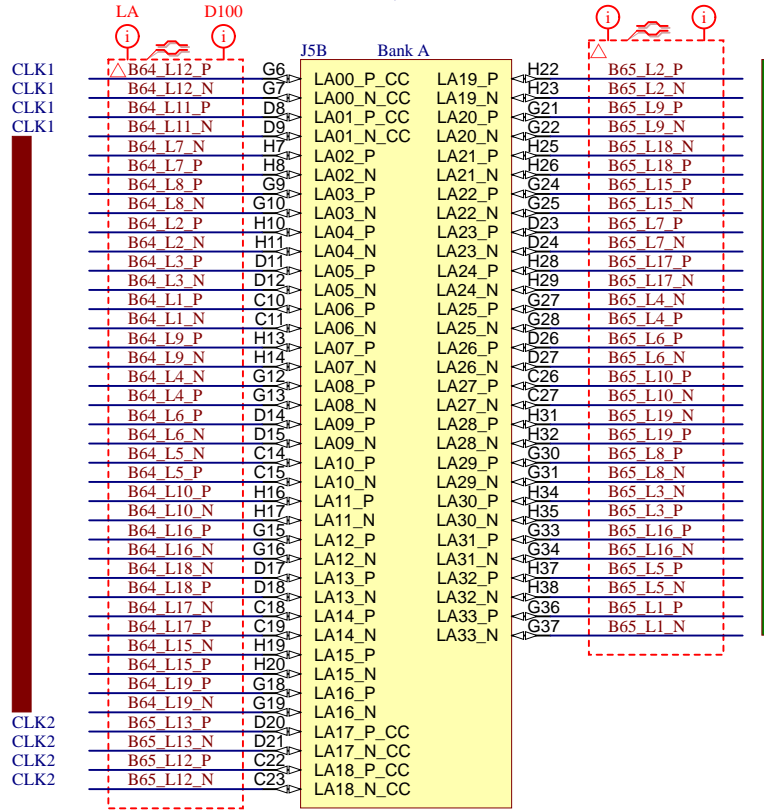
2

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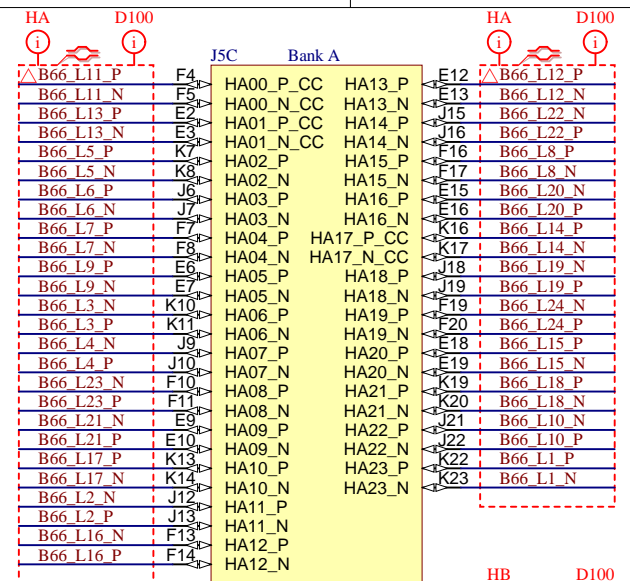
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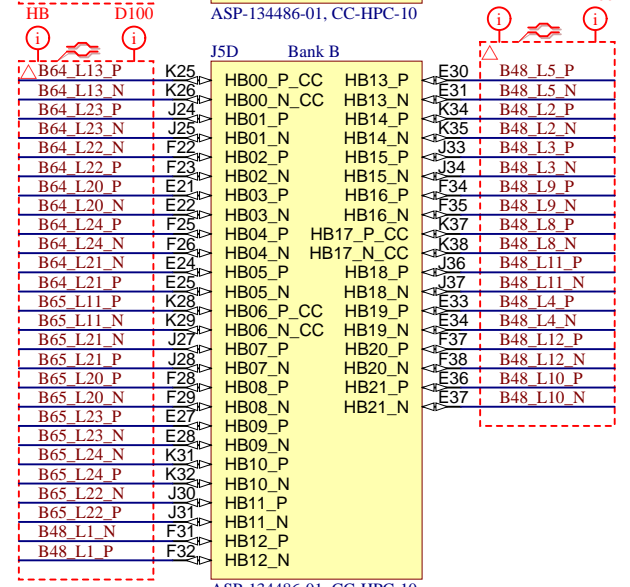
ASP-134486-01, CC-HPC-10



ASP-134486-01, CC-HPC-10



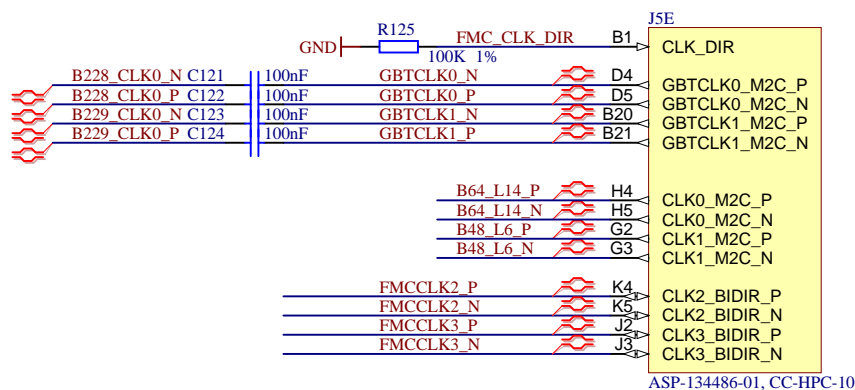
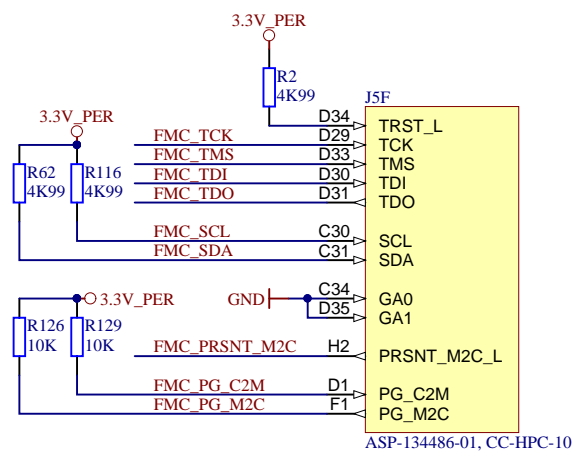
ASP-134486-01, CC-HPC-10



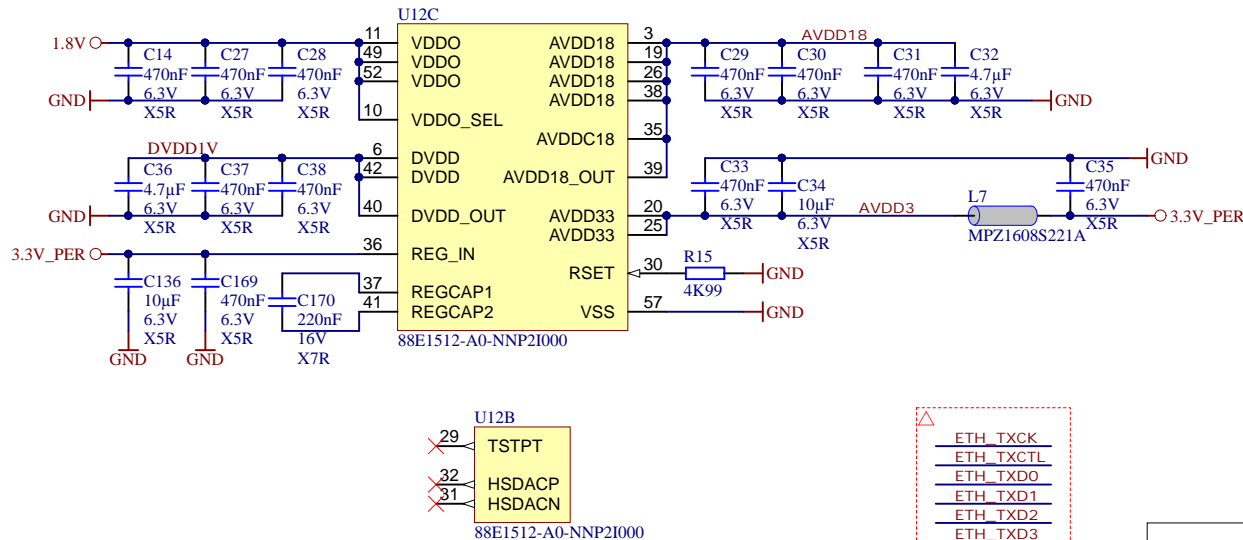
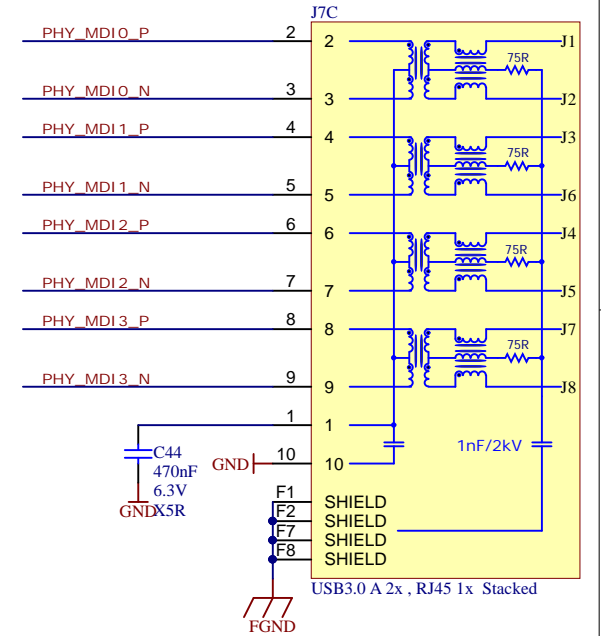
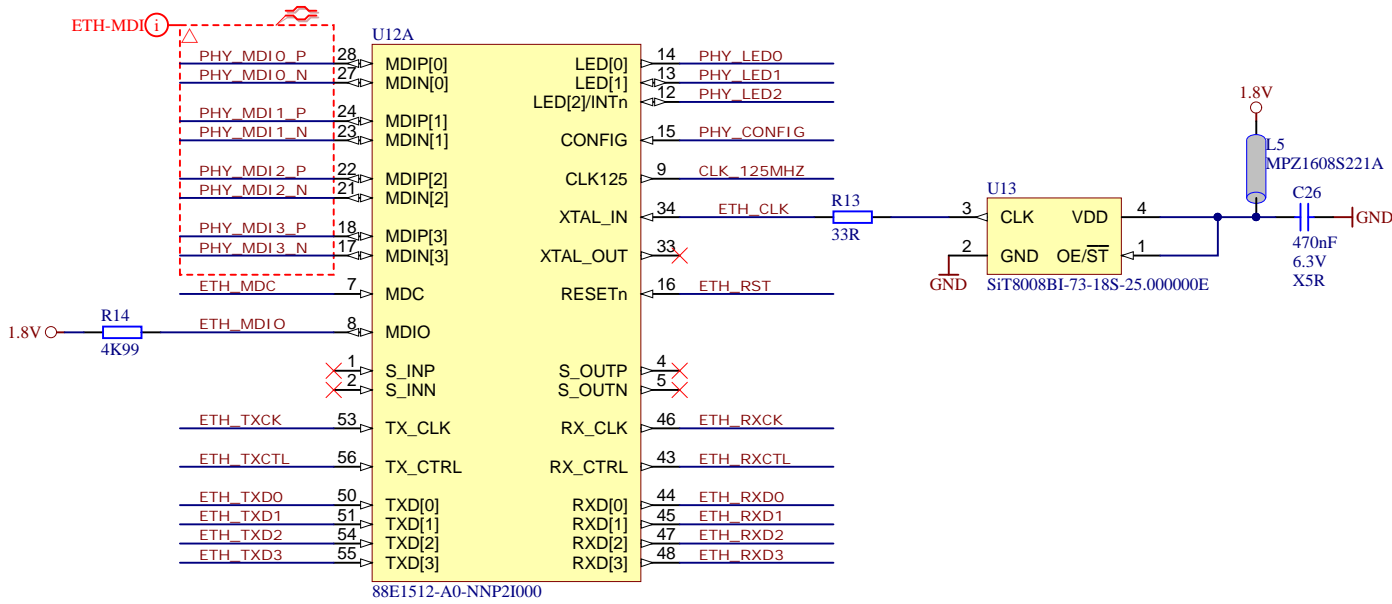
ASP-134486-01, CC-HPC-10



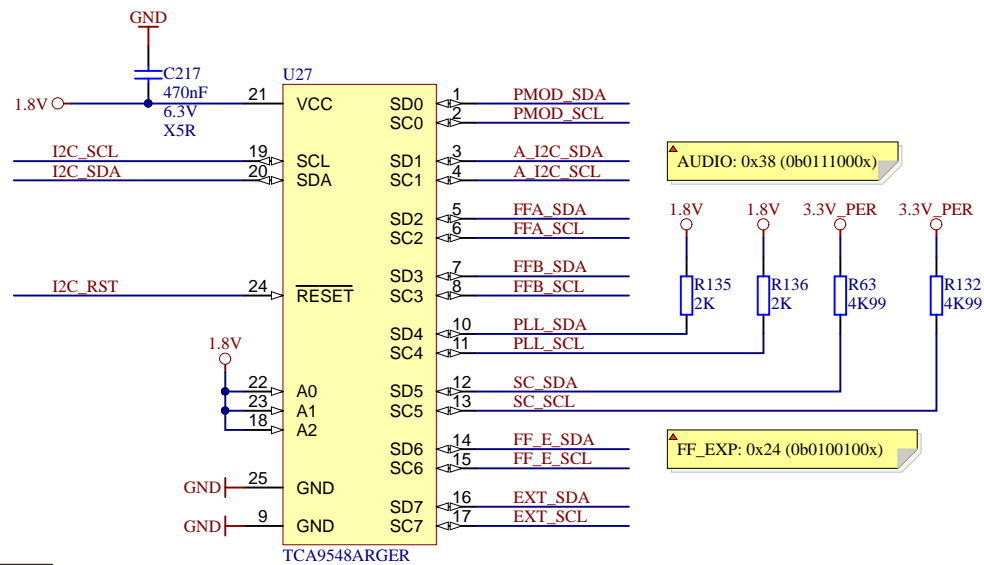
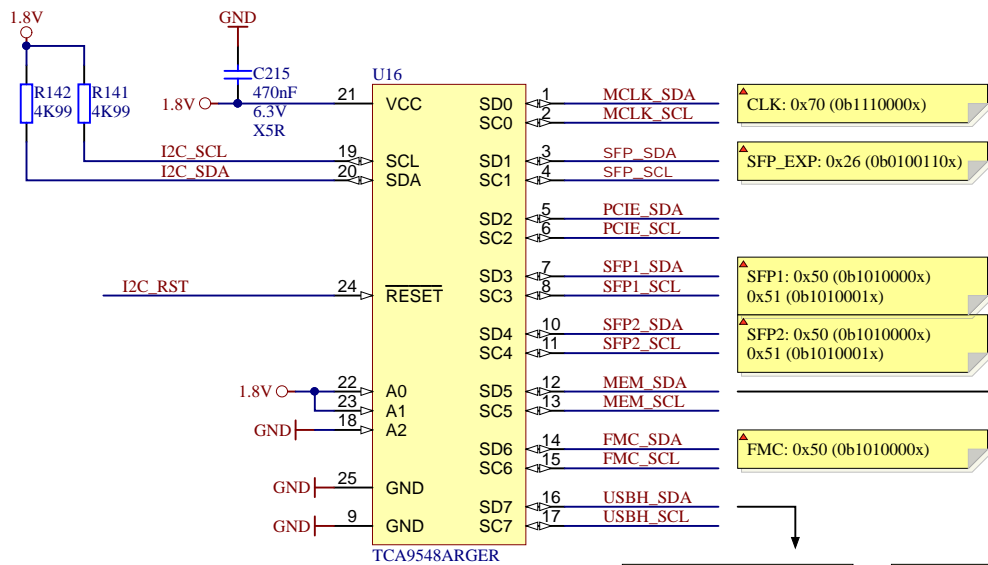
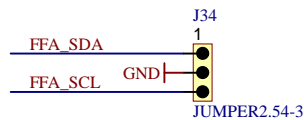
Title: TEBF0808 - FMC		
A4	Number: TEBF0808 TEBF0808	Rev. 04
Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page 18 of 36
Filename: FMC.SchDoc		



	Title: TEBF0808 - FMC		
	A4	Number: TEBF0808 TEBF0808	Rev. 04
	Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page 19 of 36
	Filename: FMC_MISC.SchDoc		



			Title: TEBF0808 - ETHERNET	
			A4	Number: TEBF0808 TEBF0808
Date: 2016-09-29		Copyright: Trenz Electronic GmbH		Rev. 04
Filename: ETH-PHY.SchDoc			Page 20 of 36	



ADDR: 0x73 (0b1110011x)

USB:

EEPROM: 0x51 (0b1010001x)

EEPROM: 0x50 (0b1010000x)

EEPROM: 0x51 (0b1010001x)

EEPROM: 0x52 (0b1010010x)

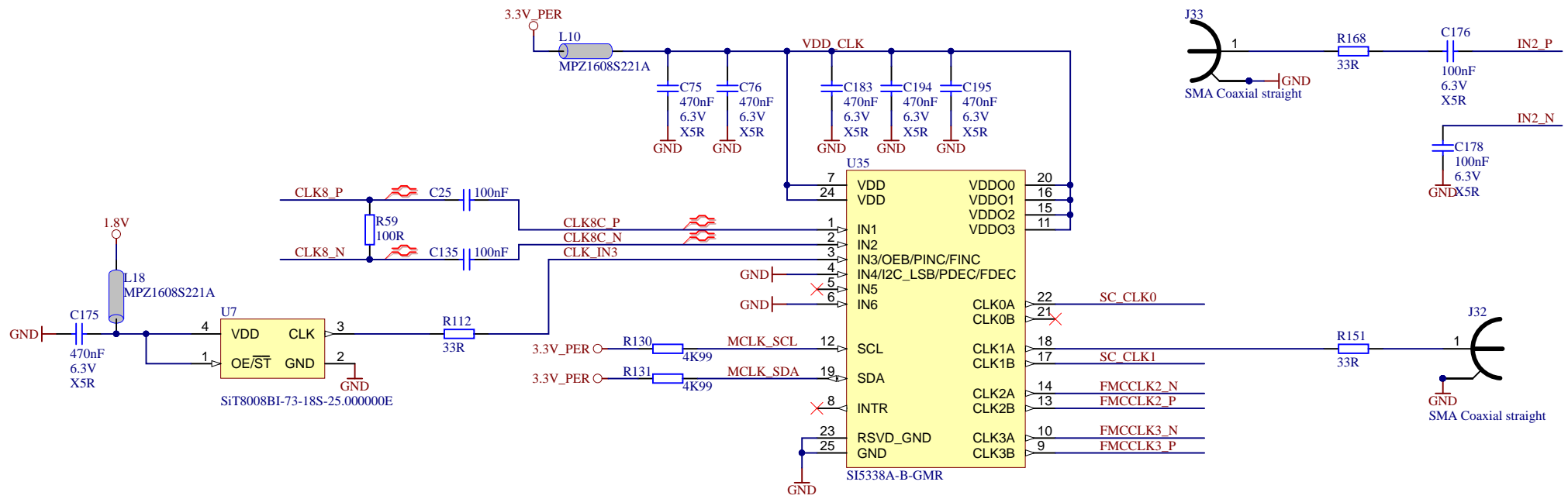
EEPROM: 0x53 (0b1010100x)


EXP: 0x27 (0b0100111x)

ADDR: 0x77 (0b1110111x)



Title: TEBF0808 - I2C System		
A4	Number: TEBF0808 TEBF0808	Rev. 04
Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page 21 of 36
Filename: I2C_system.schdoc		



	Title: TEBF0808 - CLK		
	A4	Number: TEBF0808 TEBF0808	Rev. 04
	Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page22 of 36
	Filename: CLK.schdoc		

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A

A

B

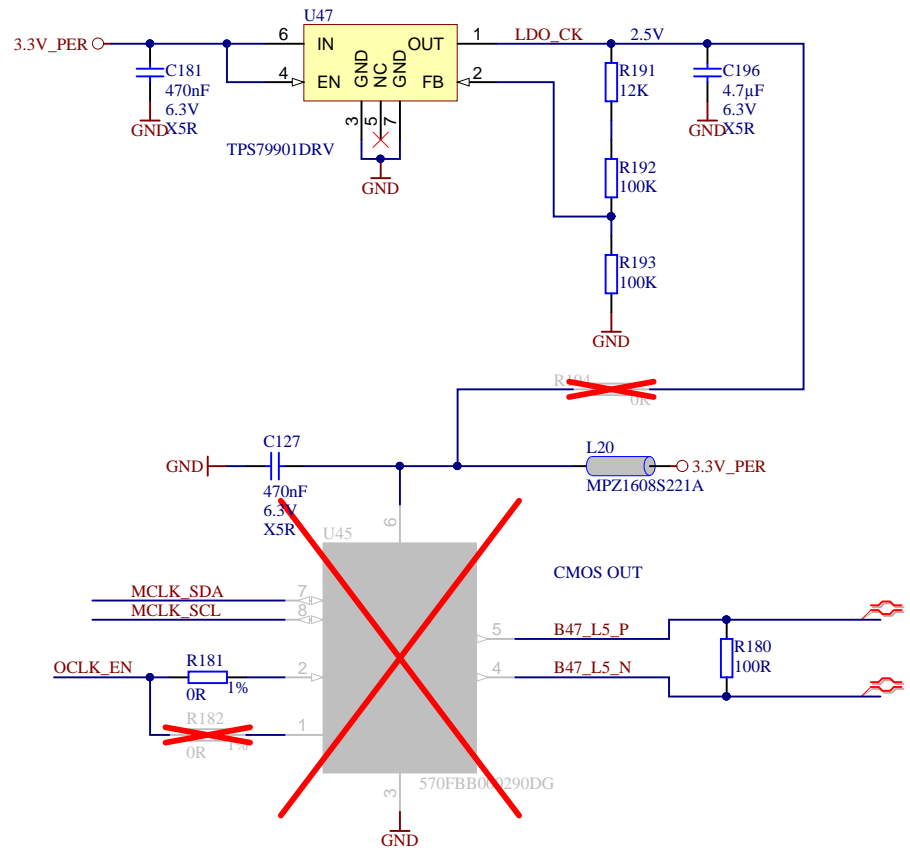
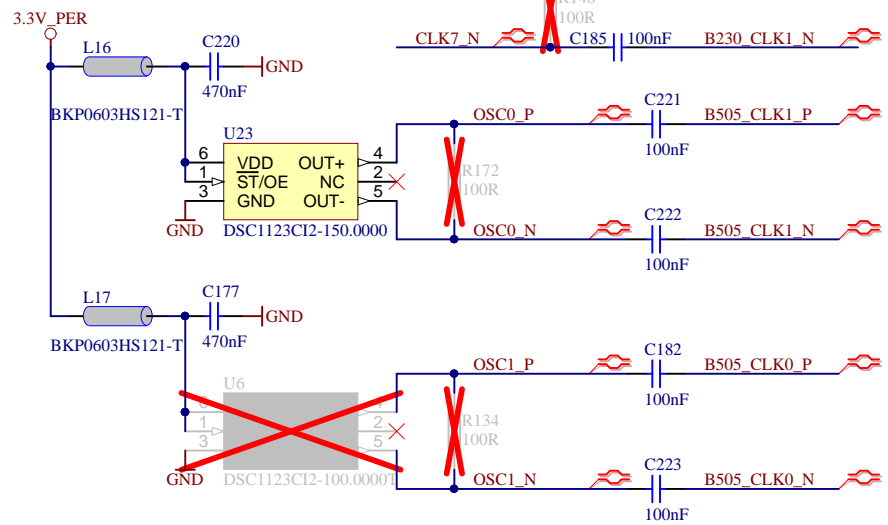
B

C

C

D

D



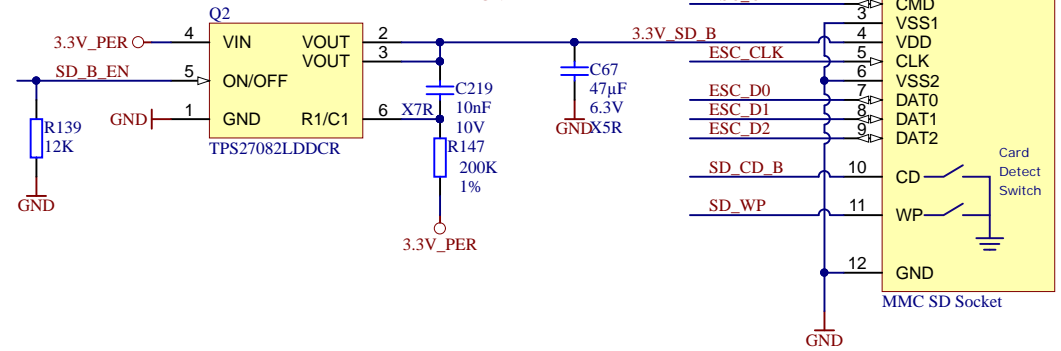
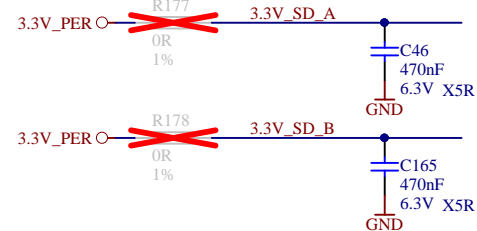
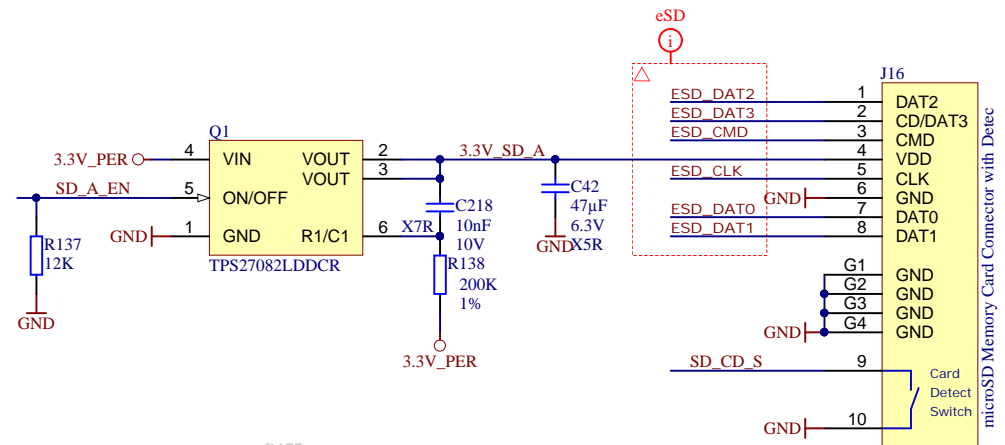
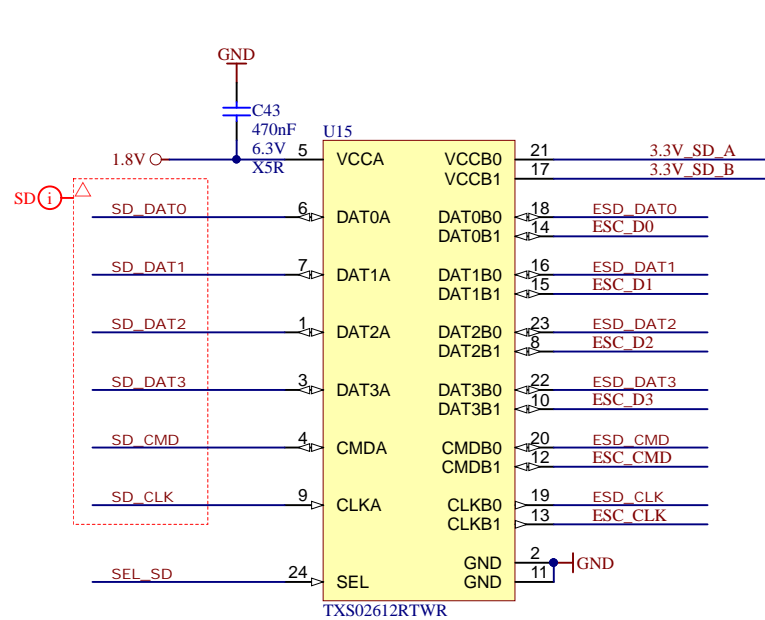
Title: TEBF0808 - CLK		
A4	Number: TEBF0808 TEBF0808	Rev. 04
Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page23 of 36
Filename: CLK_MUX.schdoc		

1

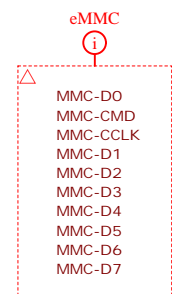
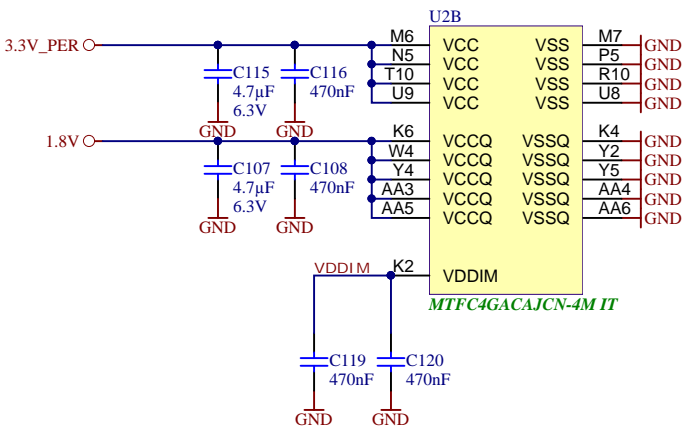
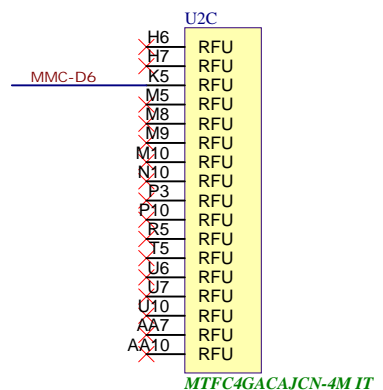
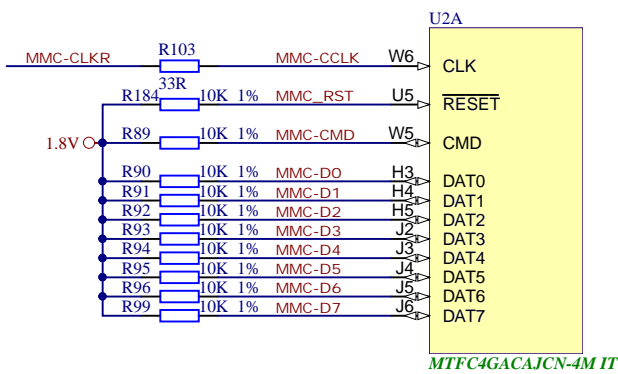
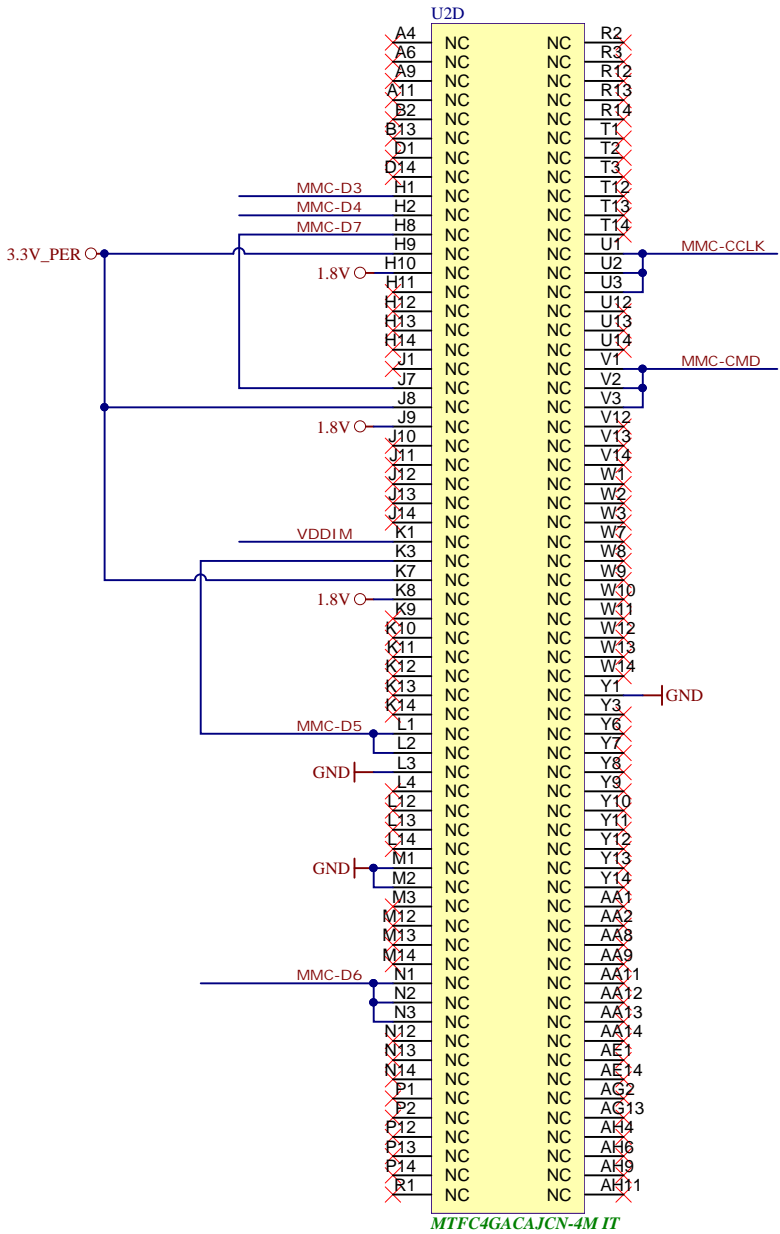
2

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4



	Title: TEBF0808 - SD	
	A4	Number: TEBF0808 TEBF0808
	Date: 2016-09-29	Copyright: Trenz Electronic GmbH
	Filename: SD.schdoc	
	Rev. 04	Page24 of 36



LAYOUT NOTES:
Signal trace length skew constraints
- Mismatch within DAT0DAT7 < 250 mil
- CLK to DAT0-7 mismatch < 250 mil
- CLK to CMD mismatch < 250 mil
- CLK to RST_N mismatch < 1000 mil



Title: TEBF0808 - eMMC		
A4	Number: TEBF0808 TEBF0808	Rev. 04
Date: 2016-09-29	Copyright: Trenz Electronic GmbH	Page 25 of 36
Filename: eMMC.SchDoc		

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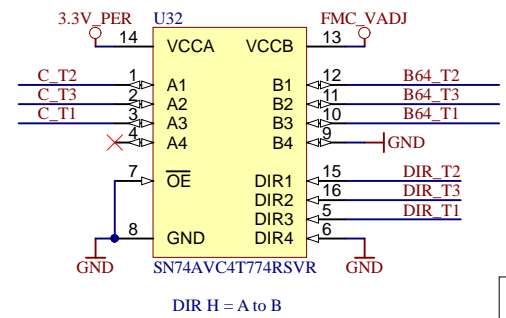
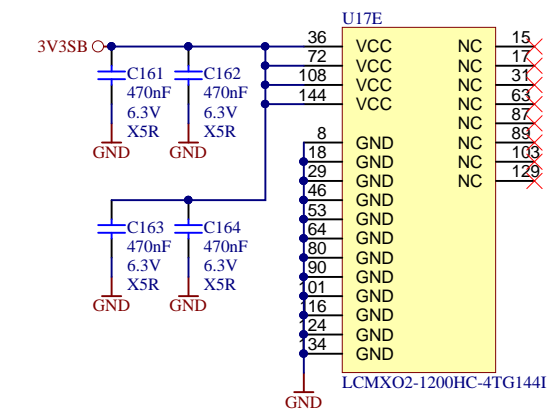
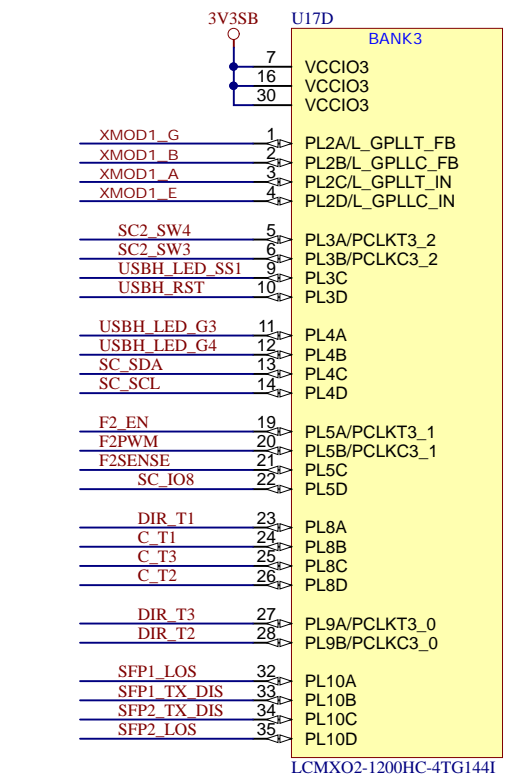
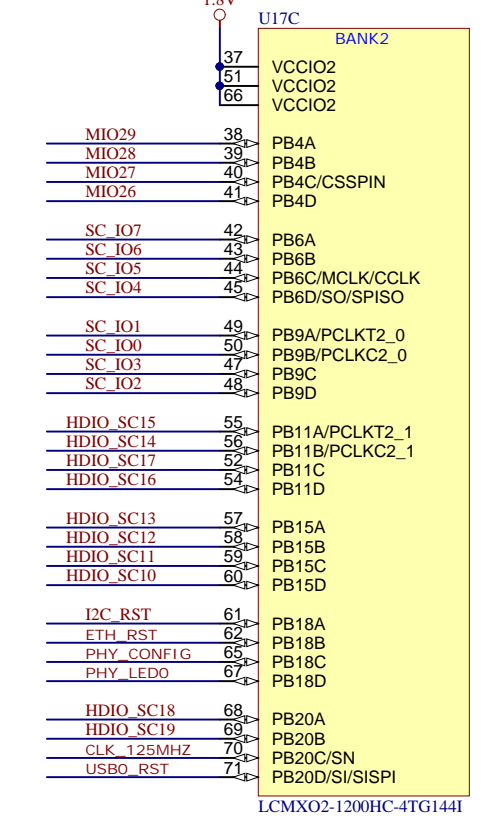
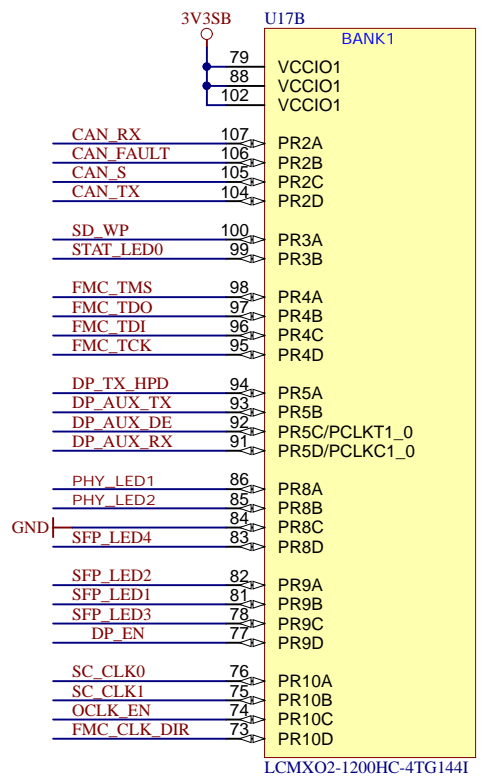
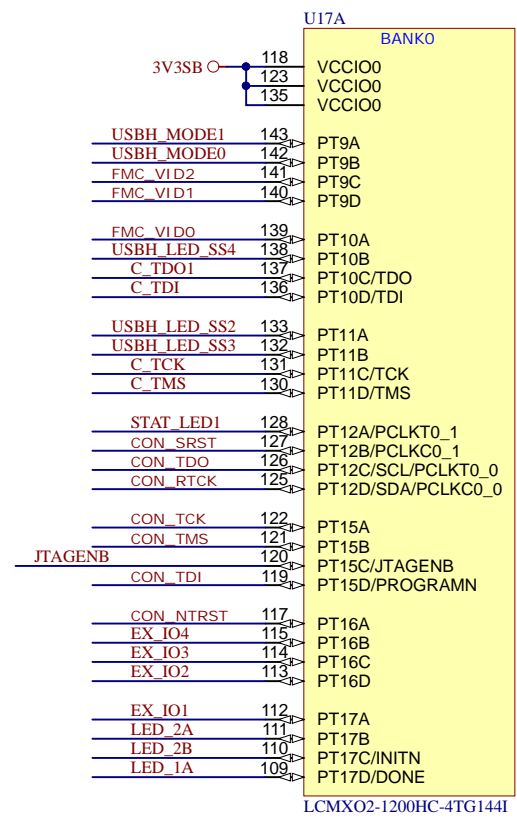
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Pin 84 PR8C "GND": REV04



Title: TEBF0808 - CPLD		
A4	Number: TEBF0808 TEBF0808	Rev. 04
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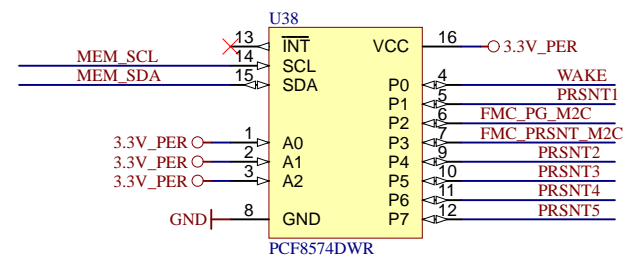
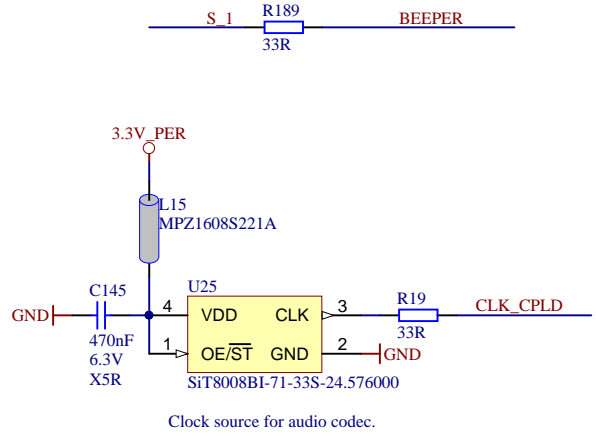
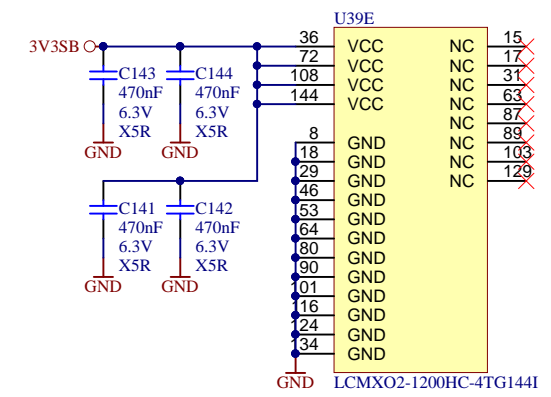
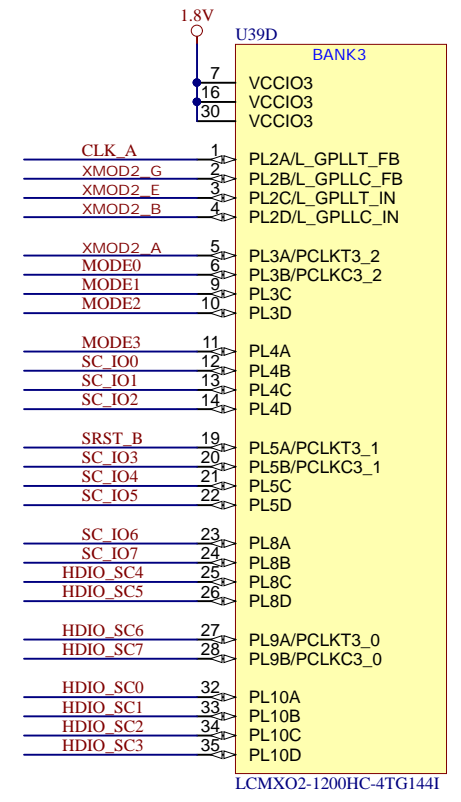
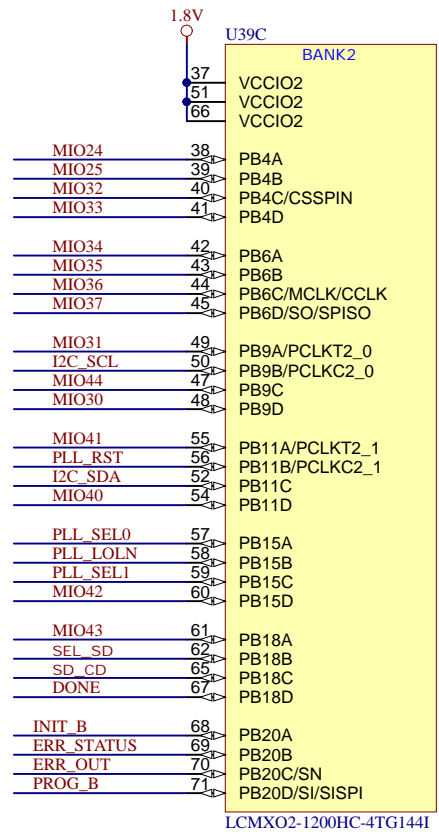
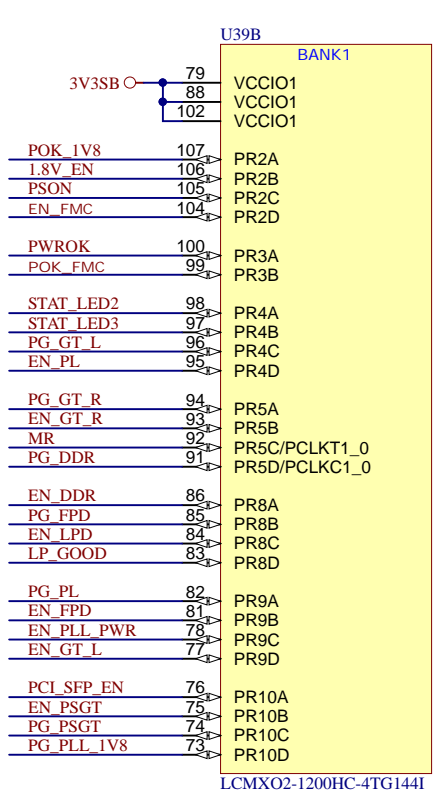
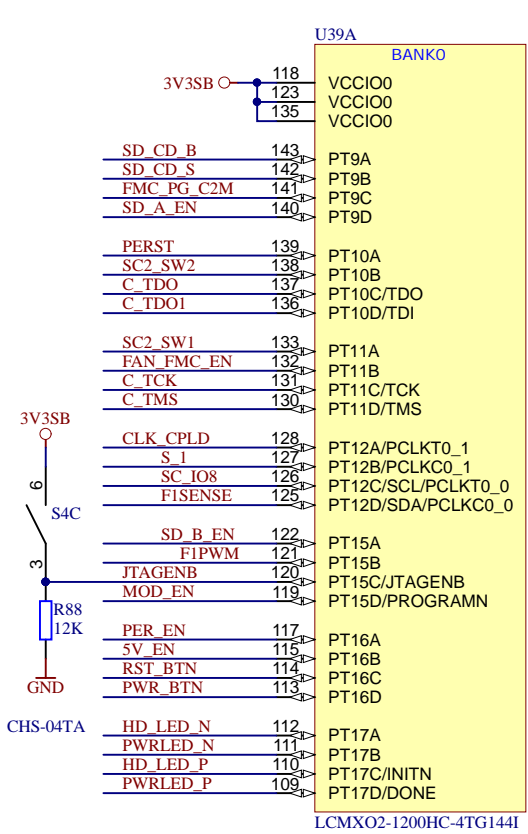
B

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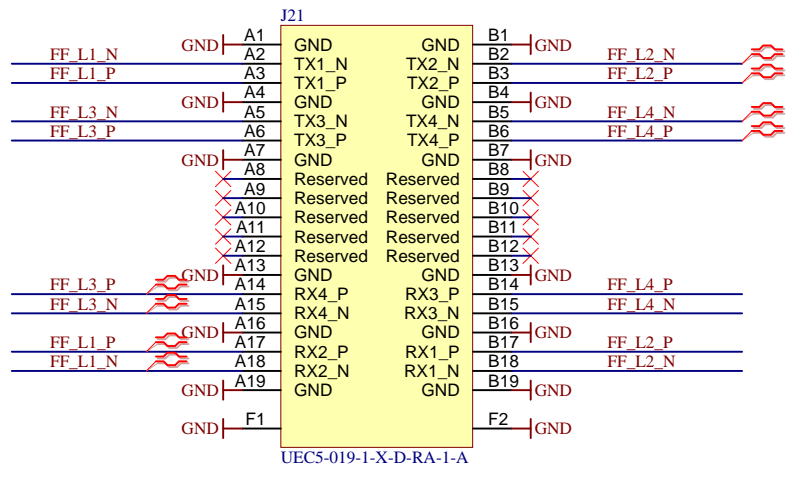
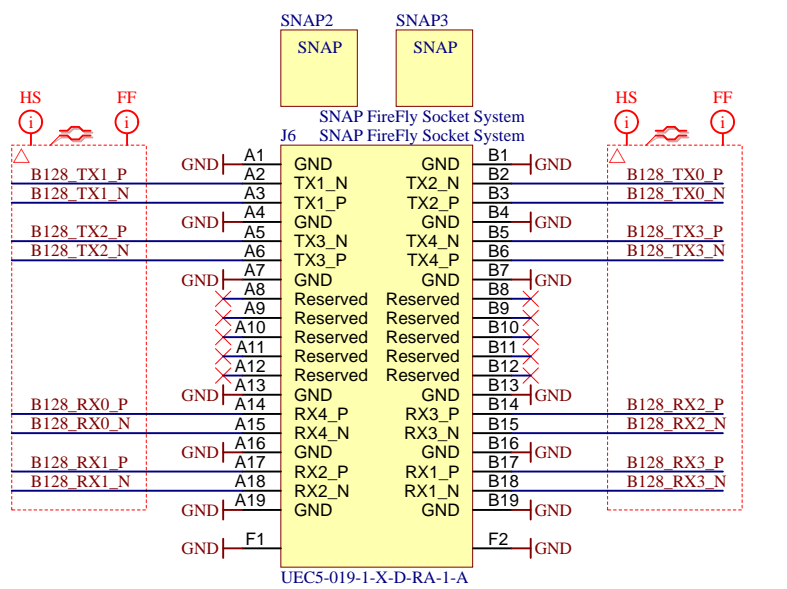
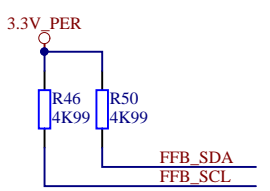
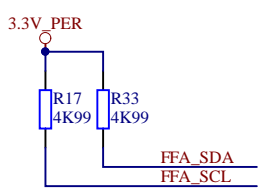
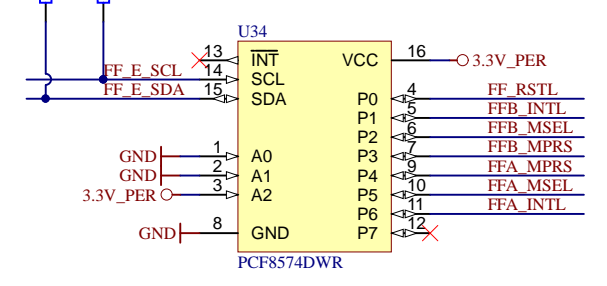
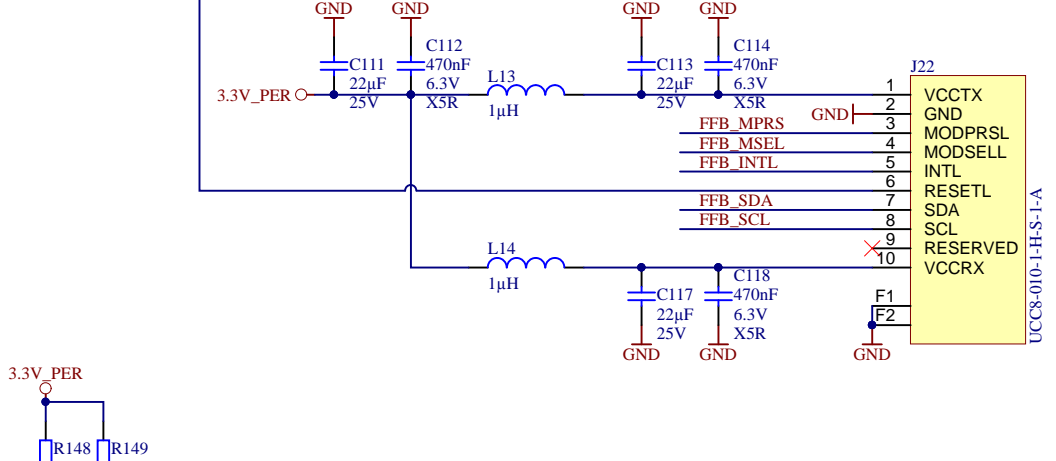
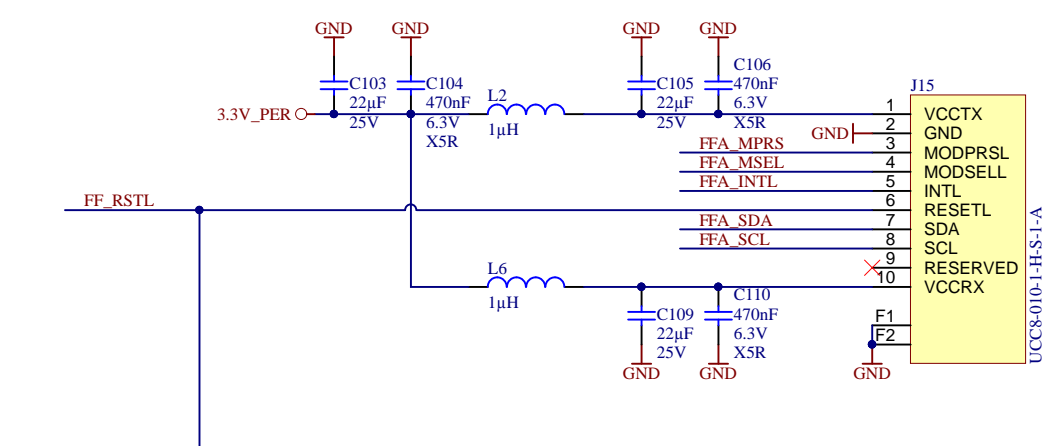
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Title: TEBF0808 - CPLD_2		
A4	Number: TEBF0808 TEBF0808	Rev. 04
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Filename: SC2.schdoc		



Title: TEBF0808 - FireFly		
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Filename: FireFly.SchDoc		

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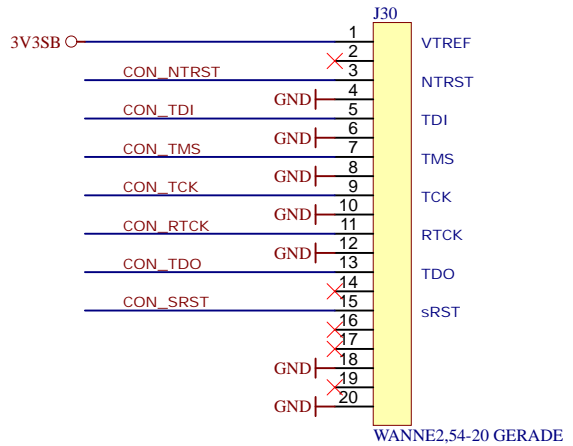
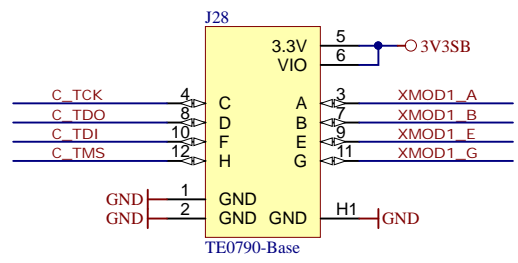
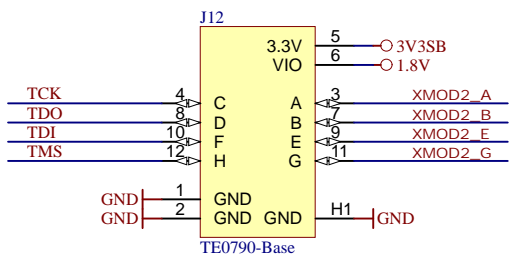
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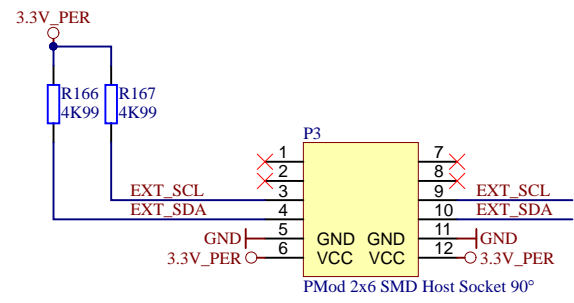
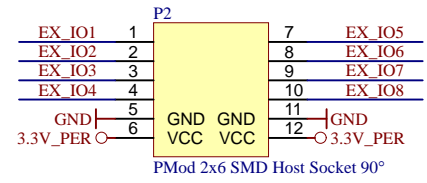
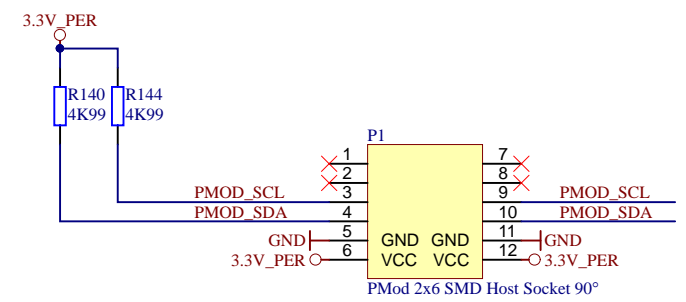
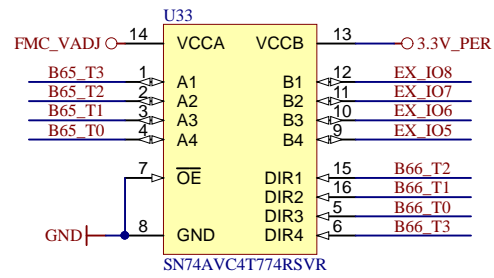
Title: TEBF0808 - XMOD JTAG		
A4	Number: TEBF0808 TEBF0808	Rev. 04
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Filename: XMOD.schdoc		

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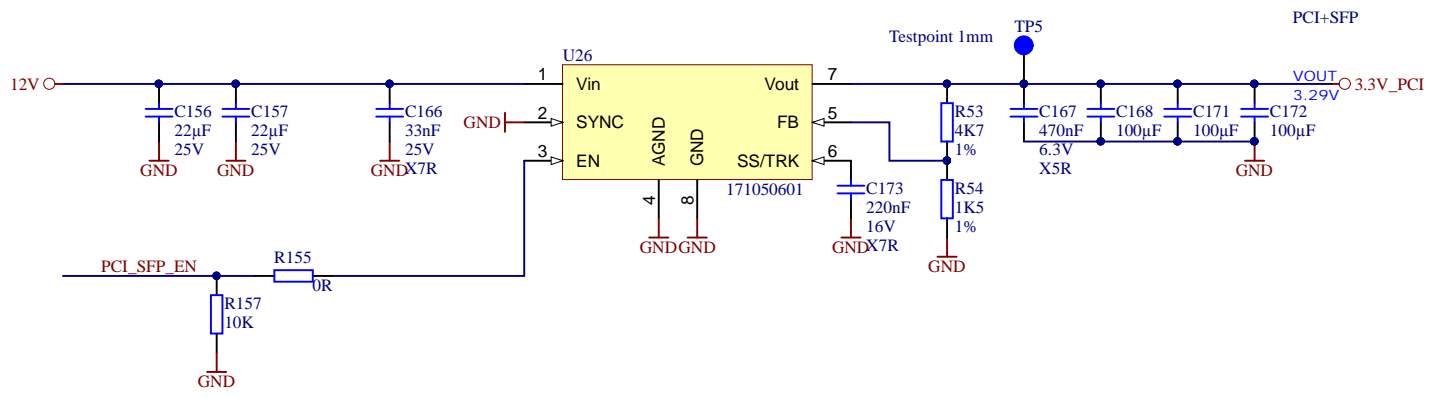
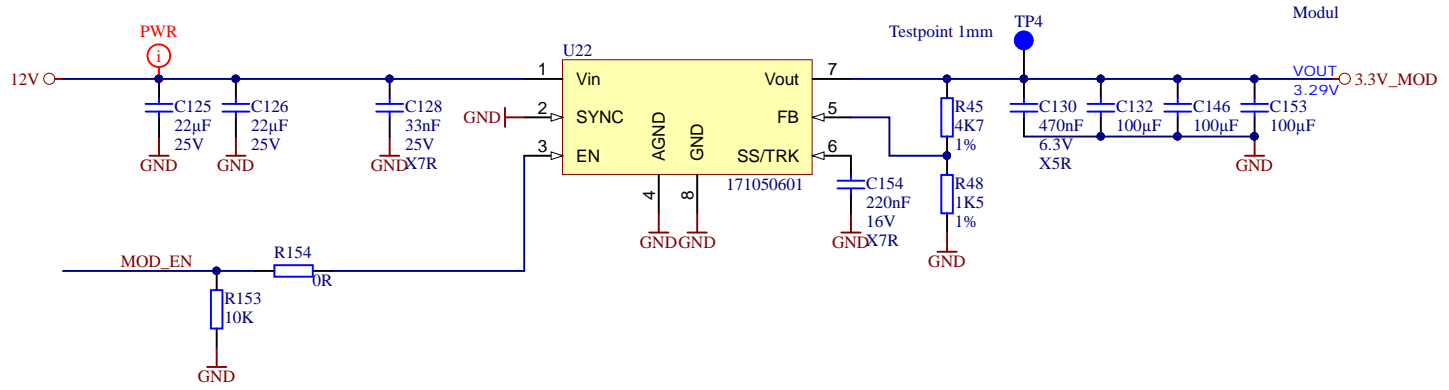
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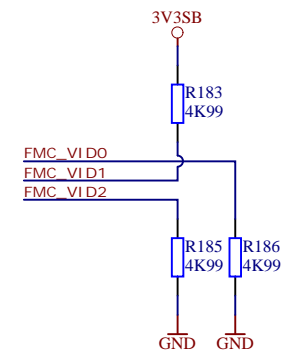
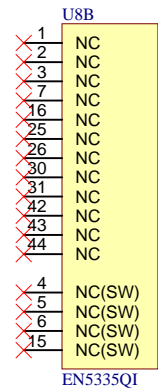
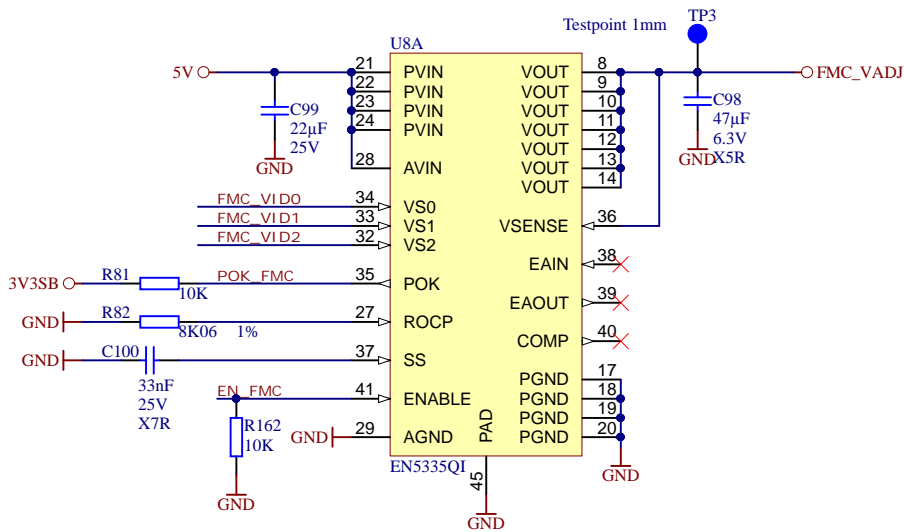
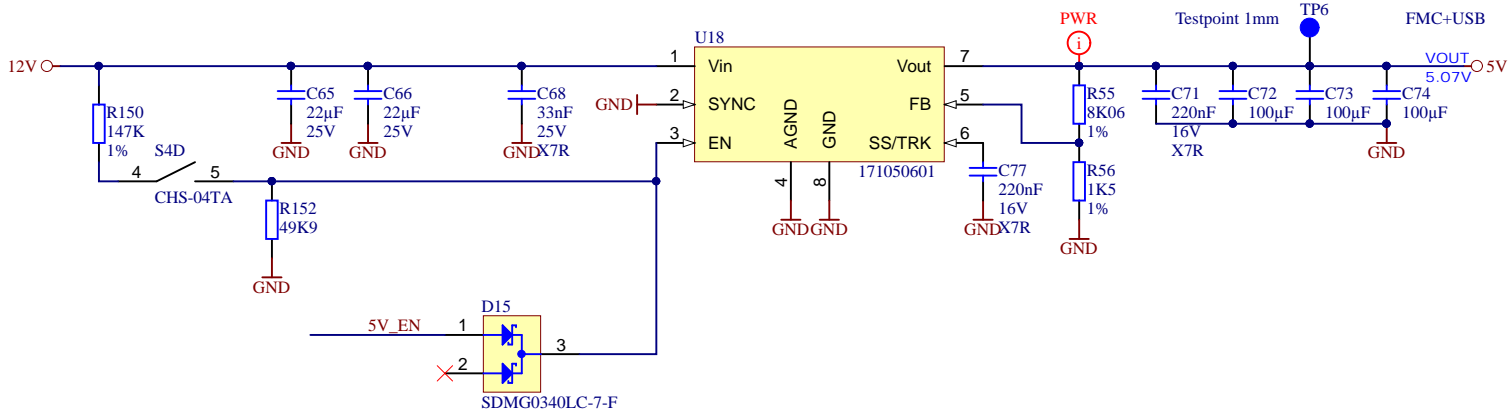
4



	Title: TEBF0808 - MISC		
	A4	Number: TEBF0808 TEBF0808	Rev. 04
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	Filename: PMODE.schdoc		



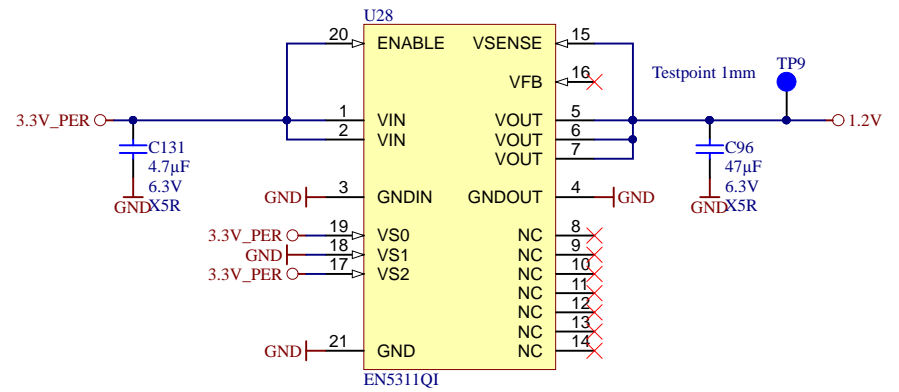
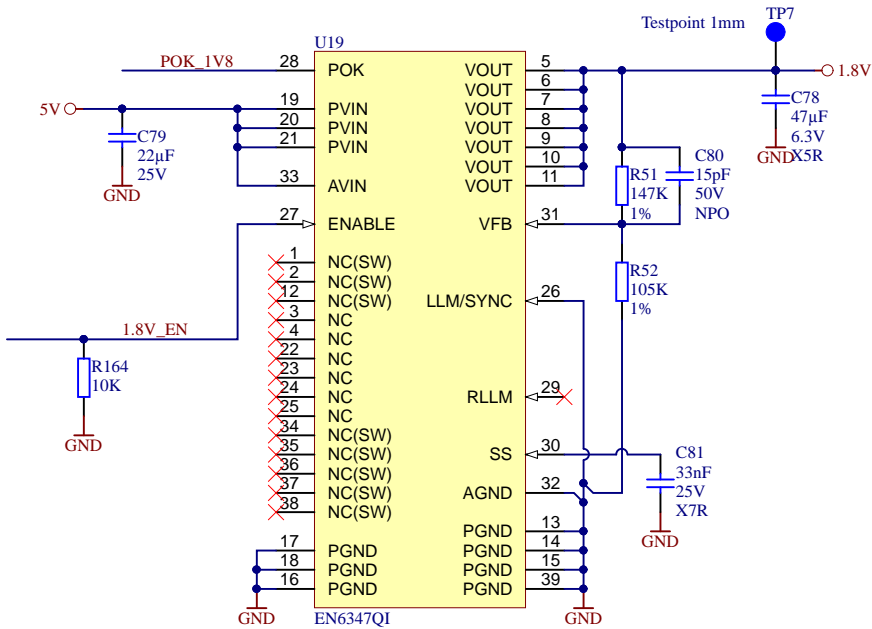
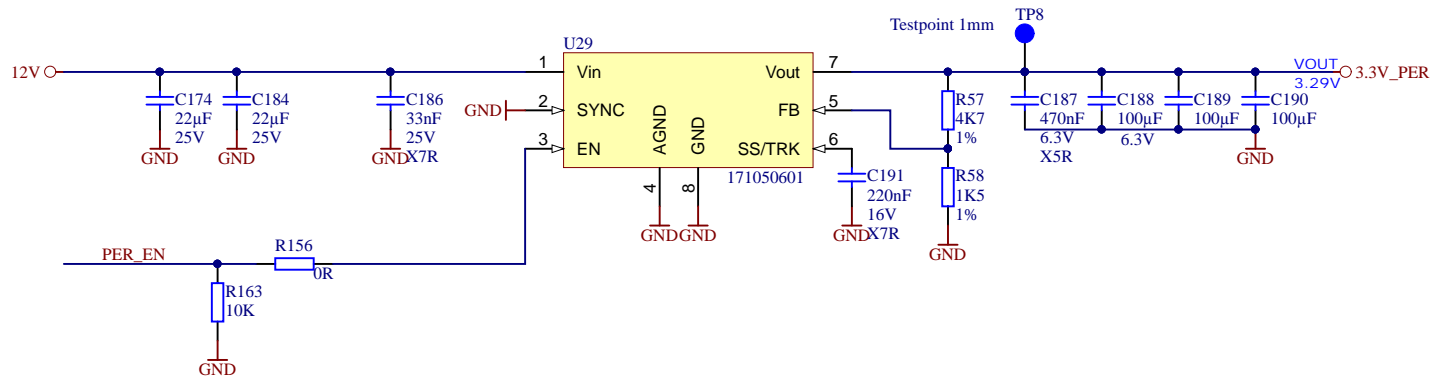
Title: TEBF0808 - Power		
A4	Number: TEBF0808 TEBF0808	Rev. 04
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Filename: Power_1.schdoc		




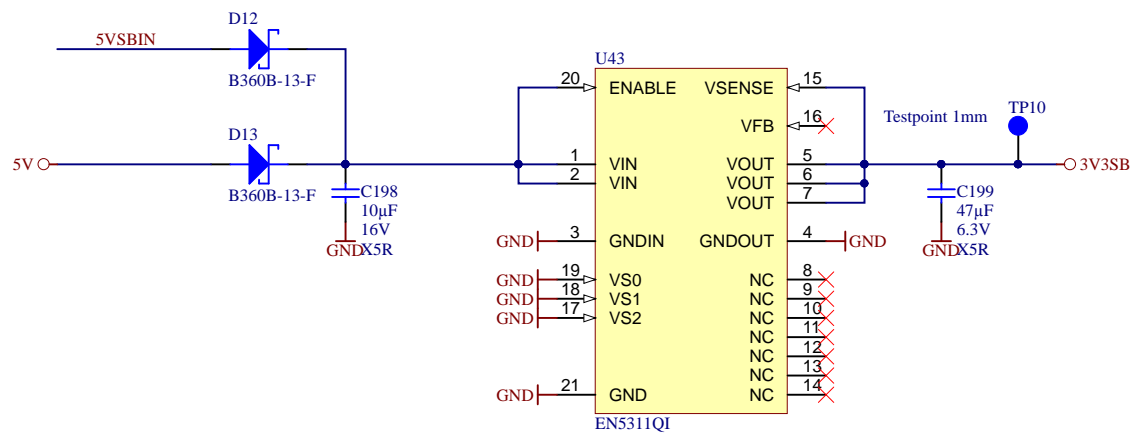
VS2 | VS1 | VS0 | Output Voltage


0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V

Title: TEBF0808 - Power		
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		Title: TEBF0808 - Power	
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		Title: TEBF0808 - Power	
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Filename: Power_4.schdoc			

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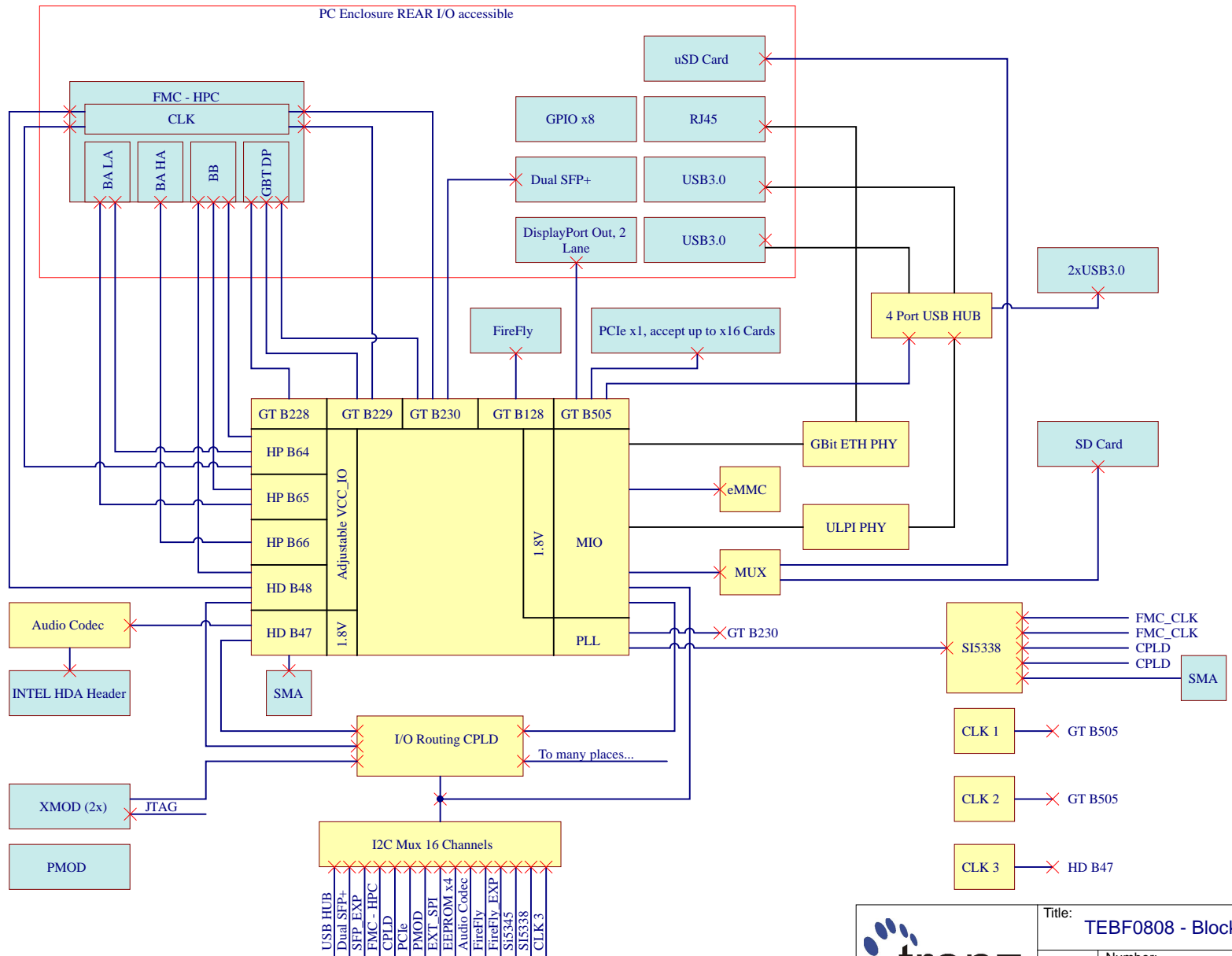
C

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PC Enclosure REAR I/O accessible



- USB HUB
- Dual SFP+
- SFP_EXP
- FMC - HPC
- CPLD
- PMOD
- EXT_SPI
- EEPROM x4
- Audio Codec
- FireFly
- FireFly_EXP
- SI5338
- CLK 3

Title: TEBF0808 - Block Diagram		
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Filename: BD.SchDoc		



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REV03

- 1) Added 2.5V option for clock source U45
- 2) Net B64_T0 terminated via 240 Ohm resistor to GND.
- 3) Nets B64_T1..T3 connected to CPLD
- 4) Nets SFP#_LOS and SFP#TX_DIS connected to CPLD (# = 1..2)
- 5) Added 4-pin connector for FAN2 (12V). Added high side switch like option for FAN without control signals.
- 6) Added net SC_IO8 between CPLD1 and CPLD2 (Bank 3V3_SB)
- 7) Deleted USB3.0 port (J18)
- 8) Port USB2.0 replaced to USB3.0 (J8, front panel)
- 9) Replaced USB HUB USB5537B to CYUSB3324 (U4)

REV04:

- 1) P and N lanes swapped in FMC clock signal pairs B228_CLK0 and B229_CLK0
- 2) Added additional FAN connector (J35)
- 3) New control circuit for external beeper
- 4) Layout and routing improvements

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	Title: TEBF0808 - Revision history		
	A4	Number: TEBF0808 TEBF0808	Rev. 04
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	Filename: Revision_Changes.SchDoc		

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