0.5 Inch OLED Display Specification

Product Outline

Item	Unit	(typ.) Specification(typ.)
Product	-	OLED display unit
Number of dots	-	60×32
Color	-	White
Substrate outside	mm	15.3×10.2
Total of thickness	mm	0.935(typ.) 1.035(max.)
Visible area(WxH)	mm	12.5×7.2
Active area(WxH)	mm	11.25×5.986 (0.50inch)
Dot pitch(WxH)	mm	0.188×0.188
Product weight	g	**0.34**(typ.) **0.38** (max.)
I OLED driver IC	-	LD7032 / LDT
Interface	-	(SPI / I2C) Serial(SPI / I2C)

Absolute Maximum Rating

Items		Symbol	Min	Max	Unit
(Ta=25℃) Supply Voltage	Drive System	VCC_C	-0.3	18.0	V
	Logic System	VDD	-0.3	3.63	V
	Interface System				
Input Voltages		Vin	-0.3	VDD+0.3	V
Operating Temperature		Topr	-20	+70	℃
Storage Temperature		Tstg	-30	+80	℃

Electrical Characteristics

1 Permissible Range of Operating Voltages

(1) Power Voltages

	Symbol	Min	Typ	Max	Unit
Drive System Power Voltage	VCC_C	14.0	15.0	16.0	V
Logic System Power Voltage Interface System Power Voltage	VDD	2.9	3.0	3.1	V

(2) Input Voltages

	Symbol	Min	Typ	Max	Unit
(High) Input High Level Voltage	VIH	VDD×0.8	-	VDD	V
(Low) Input Low Level Voltage	VIL	0.0	-	VDD×0.2	V

Current Consumption

	Symbol	MIN	TYP	MAX	Unit
All-Dots-On Mode Drive System Power Current	IH1	-	6.3	7.6	mA
All-Dots-On Mode Logic System Power Current	IDD1	-	0.12	0.18	mA
Stand-by Mode	IH2	-	-	10	μA
Stand-by Mode	IDD2	-	-	10	μA

High Humidity Storage

Store a test sample at +60 +/- 2°C and 90% RH in a constant temperature bath for 240+12/-0 hours.
Then, leave the sample at ambient temperature and humidity for 2 to 4 hours.
After these procedures, the luminance and color coordinates measured for the dot-matrix area shall meet the following criteria:

- Luminance change rate: within +/- 10% of the initial measurement
- Color coordinates change x: within +/- 0.03 of the initial measurement
  y: within +/- 0.03 of the initial measurement

Also, irregularities shall not be found for the display or the appearance of the entire OLED unit.

Low Temperature Operation (for Functionality)

Operate a test sample at -20 +/- 3°C in a constant temperature bath for 240+12/-0 hours.
Then, leave the sample at ambient temperature and humidity for 2 to 4 hours.
After these procedures, the luminance and color coordinates measured for the dot-matrix area shall meet the following criteria:

- Luminance change rate: within +/- 10% of the initial measurement
- Color coordinates change x: within +/- 0.03 of the initial measurement
  y: within +/- 0.03 of the initial measurement

Also, irregularities shall not be found for the display or the appearance of the entire OLED unit.

High Temperature Operation (for Functionality)

Operate a test sample at +70 +/- 2°C in a constant temperature bath for 240+12/-0 hours.
Then, leave the sample at ambient temperature and humidity for 2 to 4 hours.
After these procedures, the luminance and color coordinates measured for the dot-matrix area shall meet the following criteria:

- Luminance change rate: within +/- 20% of the initial measurement
- Color coordinates change x: within +/- 0.03 of the initial measurement
  y: within +/- 0.03 of the initial measurement

Also, irregularities shall not be found for the display or the appearance of the entire OLED unit.

High Temperature Humidity Operation (for Functionality)

Operate a test sample at +60 +/- 2°C and 90% RH in a constant temperature bath for 240+12/-0 hours.
Then, leave the sample at ambient temperature and humidity for 2 to 4 hours.
After these procedures, the luminance and color coordinates measured for the dot-m area shall meet the following criteria:

- Luminance change rate: within +/- 20% of the initial measurement
- Color coordinates change x: within +/- 0.03 of the initial measurement
  y: within +/- 0.03 of the initial measurement

Also, irregularities shall not be found for the display or the appearance of the entire OLED unit.

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Endurance Tests

1 Operating Life

Operate a test sample in the All-Dots-On Mode under the standard condition.
After this operation, the luminance and color coordinates measured for the dot-matrix area shall meet:
The time for luminance to decrease in half shall be 3500 hours or more.
Also, irregularities shall not be found for the display or the appearance of the entire OLED unit.

2 Electrostatic Discharge

Connect the ground terminal of the electrostatic discharge simulator to a metal-based earthing board and a test sample.
Place the test sample on the insulating plate set up on the board and make the simulator's electrode contact the test sample surface (i.e., another terminal). When the test sample is not energized, place positive and negative voltages between the ground terminal and the other terminal (once for possitive and negative respectively) under the testing conditions shown below:

＜Machine Model＞	- Discharge R: 0 Ω
	- Charge C: 200pF +/- 5%
	- Voltage: 0.2kV
＜Human Body Model＞	- Discharge R: 1500 Ω
	- Charge C: 100pF +/- 5%
	- Voltage: 1.0kV

After these procedures:
- The luminance and color coordinates measured for the dot-matrix area shall be in the range of their initial optical characteristics.
- Irregularities shall not be found for the display or the appearance of the entire OLED unit.

15. IO Interfaces

Pin No.	Pin Name	IO	Functions
1	IXS	I	SPI/I2C H : I2C(Slave address : 0110000b), L : SPI
2	D0（SCL)	I/O	Serial clock input
3	D1（SI)	I/O	Serial data input
4	A0	I	Switch data or command
5	CSB	I	Chip Select(Active Low), When IXS=H,CSB must be Low
6	RSTB	I	Reset terminal
7	VDD		Power supply for analog and digital
8	IREF	O	Resistor terminal for reference current
9	VCC_C		High voltage power supply for driving circuits
10	VCC_R		Cathode voltage power supply for driving circuits
11	VSS		GND

2.1 Power ON Setting

	初期状態 Initial state ※		
1. VDD ON	VDD ON		
2.	Wait	max.100ms	
3. CSB Disable	CSB="H"		
4.	Wait	min.0μs	
5. VCC_C ON	VCC_C ON		
6.	Wait	After stabilizing VCC_C, wait min.1μs.	
7. Reset Release	RSTB="H"		
8.	Wait	min.0.1μs	

※ **Initial state:**
VDD=VCC_C=0V
RSTB=CSB=A0="L"
D0=D1="Hi-z"

When transiting from Power ON to Display ON, the waiting time between Reset Release and Display ON shall be more than 1.1ms.

Refer to "16.2.3 Power ON/OFF Sequence" for the timing details.

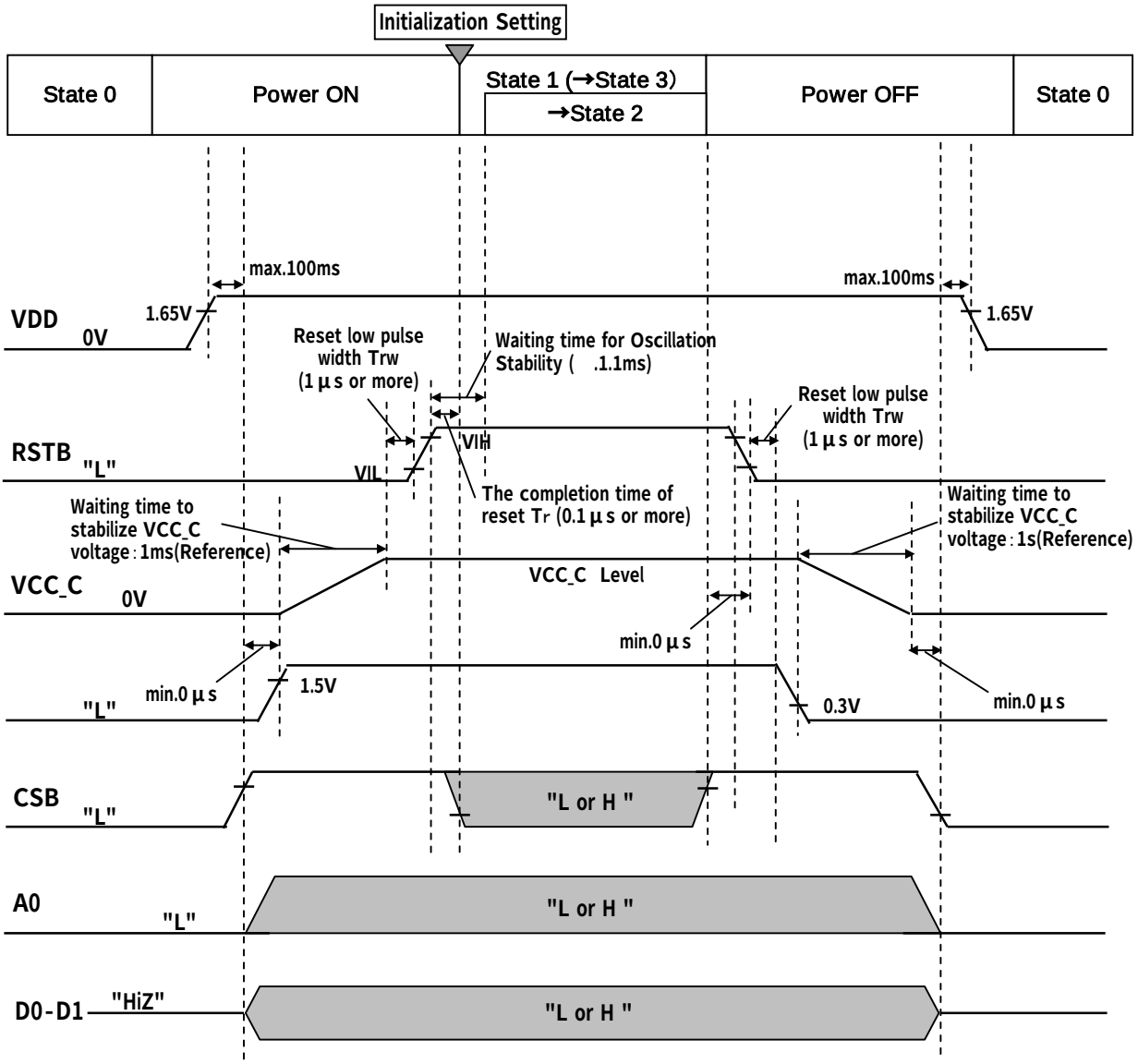
Power OFF Setting

1. CSB Disable	CSB="H"		
2.	Wait	min.0μs	
3. Reset	RSTB="L"		
4.	Wait	min.1μs	
5. VCC_C OFF	VCC_C OFF		
6.	Wait	Waiting time to stabilize VCC_C	No need in the case of ⑦
7. CSB Enable	CSB="L"		
8. VDD OFF	VDD OFF		
	Initial state ※		

Initial state:
VDD=VCC_C=0V
RSTB=CSB=A0="L"
D0=D1="Hi-z"

Refer to "16.2.3 Power ON/OFF Sequence" for the timing details.

16.2.3 Power ON/OFF Sequence



NOTES: - If VDD is turned on but nothing is displayed, the OLED unit shall be put into State 1 or State 3.
- When VDD is turned on or off, the following conditions shall be met:
RSTB=CSB=A0= "L" D0=D1= "Hi-z"

16.3 Initialization

16.3.1 Initialization Setting

"○○"x"△△"

→

Command writing guide

″○○″ : Command address (1Byte)

″△△″ : Parameter or Data (1 ~ 4Byte)

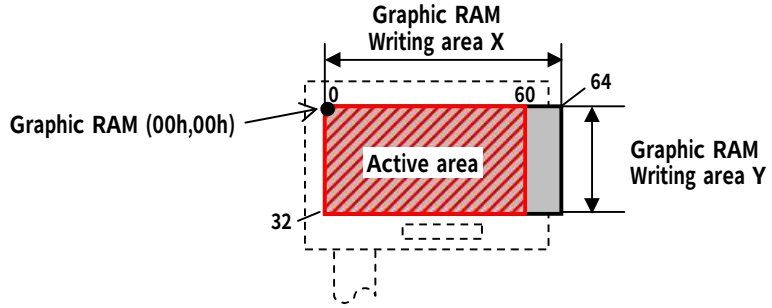
	Value		Name
1. DDISPON/OFF	02 x 00	*1	Dot Matrix Display ON/OFF
2. DSTBYON/OFF	14 x 01	*1	Dot Matrix Display Stand-by ON/OFF
3. DFRAME	1A x 04	*2	Dot Matrix Frame Rate
4. WriteDirection	1D x 00	*1	Graphics Memory Writing Direction.
5. DispDirection	09 x 00	*1	Display Direction
6. DispSizeX	30 x 003B		Display Size X
7. DispSizeY	32 x 001F		Display Size Y
8. XDispStart	38 x 00	*1	Display Start Address X
9. YDispStart	39 x 00	*1	Display Start Address Y
10. XBoxAdrStart	34 x 00	*1	Data Reading/Writing Box X start
11. XBoxAdrEnd	35 x 07		Data Reading/Writing Box X end
12. YBoxAdrStart	36 x 00	*1	Data Reading/Writing Box Y start
13. YBoxAdrEnd	37 x 1F		Data Reading/Writing Box Y end
14. PeakWidth	10 x 00	*2	Peak Pulse Width Set
15. PeakDelay	16 x 00	*1*2	Peak Pulse Delay Set
16. DotCurrent	12 x **50**	*2	Dot Matrix Current Set
17. PreC_Width	18 x 03	*2	Pre-Charge Width Set
18. PreC_Select	44 x 02	*1*2	Pre-Charge Mode Set
19. Row_Overlap	48 x 03	*2	Row overlap
20. RowScan	17 x 00	*1*2	Row Scan
21. ScanMode	13 x 00	*1*2	Row Scan Sequence Setting
22. Data_Reverse	1C x 00	*1	Data_Reverse
23. VCC_R_SEL	3F x 11	*2	Set Internal Regulator for Row Scan
24. VDD_SEL	3D x **00**	*2	VDD Selection
25. S_SLeepTimer	C0 x 00	*1	Screen Saver Command
26. S_SleepStart	C2 x 00	*1	Screen Saver Command
27. S_StepTimer	C3 x 00	*1	Screen Saver Command
28. S_StepUnit	C4 x 00	*1	Screen Saver Command
29. S_Condition	CC x 00	*1	Screen Saver Command
30. S_Start/Stop	CD x 00	*1	Screen Saver Command
31. S_Select	CE x 02	*1	Screen Saver Command
32. DataRW	08 x		
33. Graphic RAM Data	[00～FF]		Image Data *3
↓ ↓	↓		
288. ↓	[00～FF]		

*1:It is the same as a default value.

*2:Please do not change the value.

*3:Please send the image data sized 64 x 32 pixels.

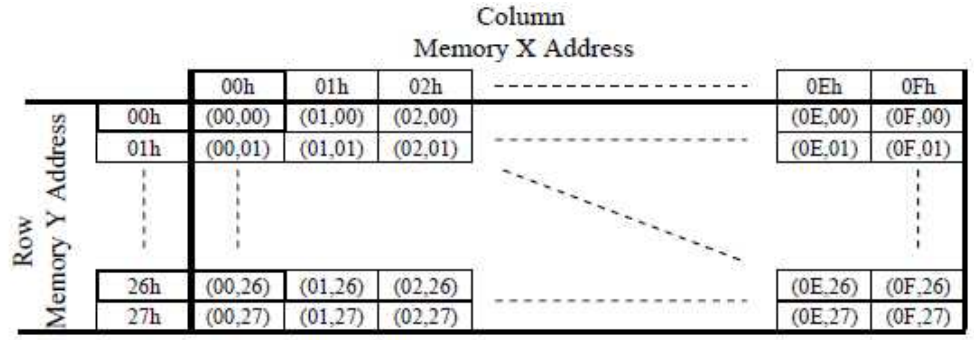
Refer to "LD7032 Function Manual" for the details.



3.2 Image Writing

Dot Memory Map

The size of the Graphic RAM is 128x64 bits. One bit indicates one pixcel.
The address toward the direction of X is set every 8bits and the direction of Y is set every 1bit.

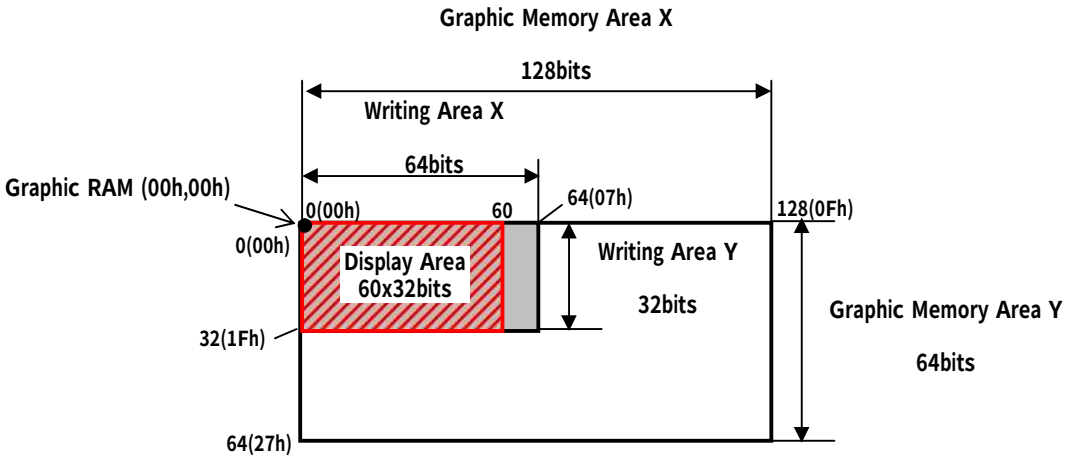


Memory Size = 16 x 8Bit x 40 = 5,120 Bit

Dot Memory Map(LD7032)

Image Data Writing

If the size of display is 60x32 pixels, the image data sized 64x32 pixels needs to be sent because the address toward the direction of X is set every 8bits.
4x32 pixels are not shown on the display.



4 Display ON/OFF Setting

4.1 Display ON

1. STANDBY_OFF	14x00	
2.	Wait	min.0μs
3. DataRW	08 x	
4. Graphic RAM Data	[00～FF]	※
↓ ↓	↓	
259. ↓	[00～FF]	
260. Display ON	02x01	

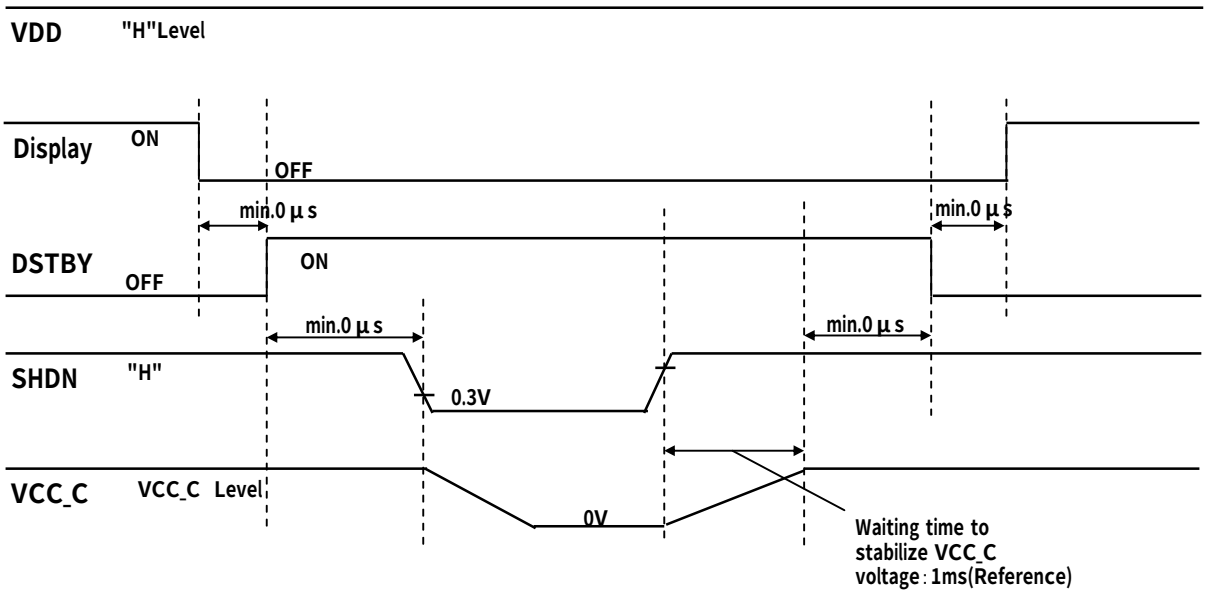
Unnecessary when not rewriting the image.

4.2 Display OFF

1. Display OFF	02x00	
2.	Wait	min.0ms
3. DSTBYON/OFF	14x01	

4.3 Display ON/OFF Sequence

State 2	Display OFF	State 1	VCC_C OFF	State 3	VCC_C ON	State 1	Display ON	State 2



5 Changing The Display Setting

5.1 Image Rewriting

1. DataRW	08 x
2. Graphic RAM Data	[00～FF]
↓ ↓	↓
257. ↓	[00～FF]

16.5.2 Screen Saver Setting

Screen Saver ON】

1. S_StepTimer	C3x[00～FF]
2. S_StepUnit	C4x[01 or 02]
3. S_Condition	CCx[01 or 02]
4. S_Start/Stop	CDx01

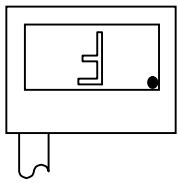
Screen Saver OFF】

1. S_Start/Stop	CDx00

16.5.3 Reverse Display 180°

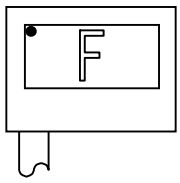
When reversing display 180°】

1. XDispStart	38x04
2. WriteDirection	1Dx0B
3. DataRW	08 x
4. Graphic RAM Data	[00～FF]
↓ ↓	↓
259. ↓	[00～FF]



When restoring 180° reversed display】

1. XDispStart	38x00
2. WriteDirection	1Dx00
3. DataRW	08 x
4. Graphic RAM Data	[00～FF]
↓ ↓	↓
259. ↓	[00～FF]



Reversing display 180° is enabled in only State 1 or State 3.

17. Interface Characteristics/Timing

Interface Characteristics

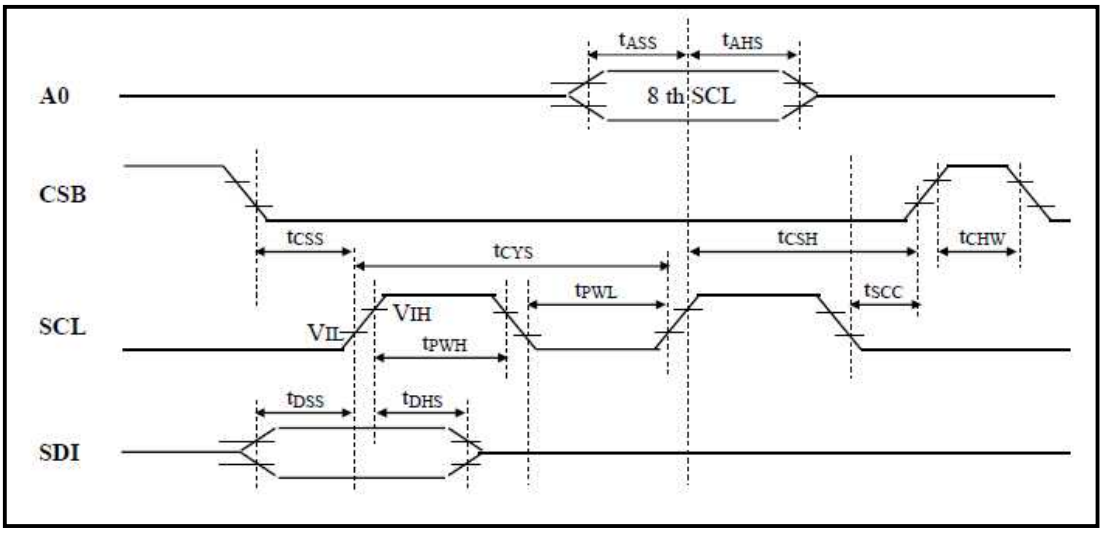
Serial Interface

(Ta=25℃, VSS=0V, VDD=1.65– 3.5V)

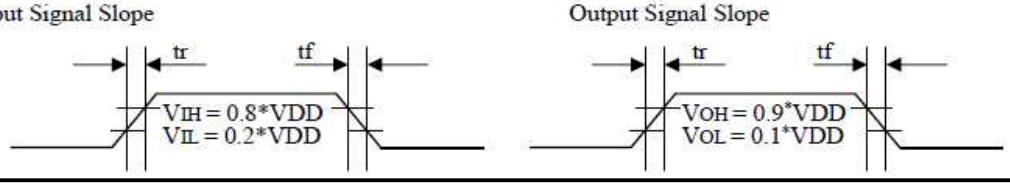
Parameter	Symbol	Related Pins	Specification MIN	Specification MAX	Unit
Serial clock cycle	t_{CYS}	SCL (D0)	66	-	
High pulse width	t_{PWH}		20	-	ns
Low pulse width	t_{PWL}		20	-	
A0 setup time	t_{ASS}	A0	15	-	ns
A0 hold time	t_{AHS}		25	-	
Data setup time	t_{DSS}	SDI (D1)	20	-	ns
Data hold time	t_{DHS}		20	-	
Chip select setup time	t_{CSS}	CSB	20	-	
Chip select hold time	t_{CSH}		50	-	ns
Chip select high pulse width	t_{CSW}		50	-	
SCL to Chip Select	t_{SCC}	SCL(D0), CSB	15	-	ns

(Ta=25℃, VSS=0V, VDD=1.65– 3.5V)

Parameter	Symbol	Related Pins	Specification MIN	Specification MAX	Unit
Serial clock cycle	t_{CYS}	SCL (D0)	150	-	
High pulse width	t_{PWH}		60	-	ns
Low pulse width	t_{PWL}		60	-	
A0 setup time	t_{ASS}	A0	50	-	ns
A0 hold time	t_{AHS}		60	-	
Data setup time	t_{DSS}	SDI (D1)	60	-	ns
Data hold time	t_{DHS}		60	-	
Chip select setup time	t_{CSS}	CSB	60	-	
Chip select hold time	t_{CSH}		100	-	ns
Chip select high pulse width	t_{CSW}		100	-	
SCL to Chip Select	t_{SCC}	SCL(D0), CSB	40	-	ns



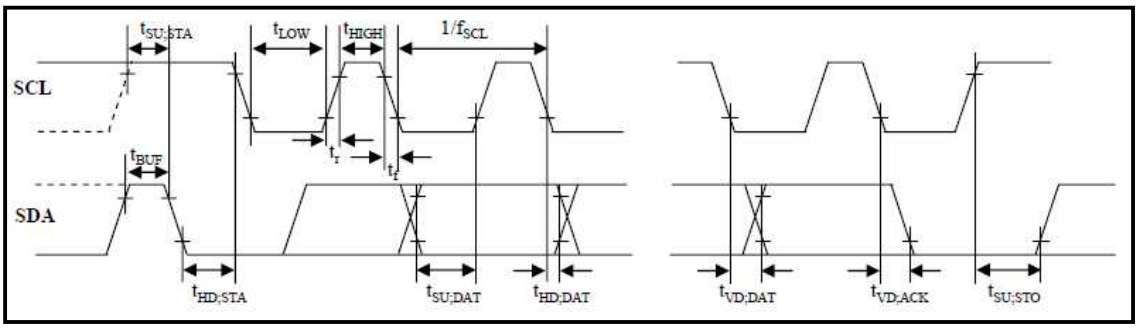
NOTE : The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.



I2C Interface

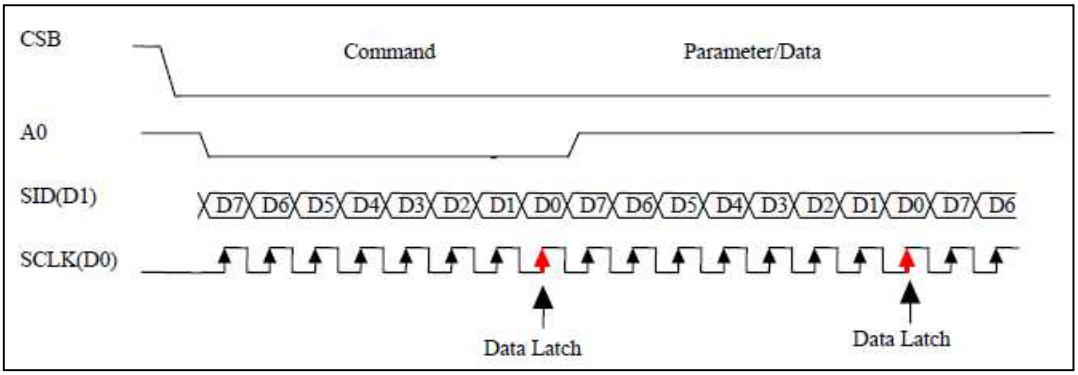
(Ta=25℃, VSS=0V, VDD=1.65– 3.5V)

Parameter	Symbol	Standard mode		Fast mode		UNIT
		MIN	MAX	MIN	MAX	
SCL clock frequency	f_{scl}	0	100	0	400	kHz
bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	us
hold time (repeated) START condition	$t_{HD;STA}$	4.0	-	0.6	-	us
set-up time form a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	us
set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	us
data set-up time	$t_{SU;DAT}$	0.25	-	0.1	-	us
data hold time	$t_{HD;DTA}$	0	-	0	-	ns
data valid acknowledge time	$t_{VD;ACK}$	0.3	3.45	0.1	0.9	us
data valid time	$t_{VD;DAT}$	0.3	-	0.5	-	us
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	us
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	us
fall time of both SDA and SCL signals	t_f	-	0.3	-	0.3	us
rise time of both SDA and SCL signals	t_r	-	1.0	-	0.3	us
pulse width of spikes that must be suppressed by the input filter	t_{SP}	0	50	0	50	ns



2.2 Interface Timing

8Bit Serial Interface



I2C Interface

Slave Address : 0 1 1 0 0 0 0 b

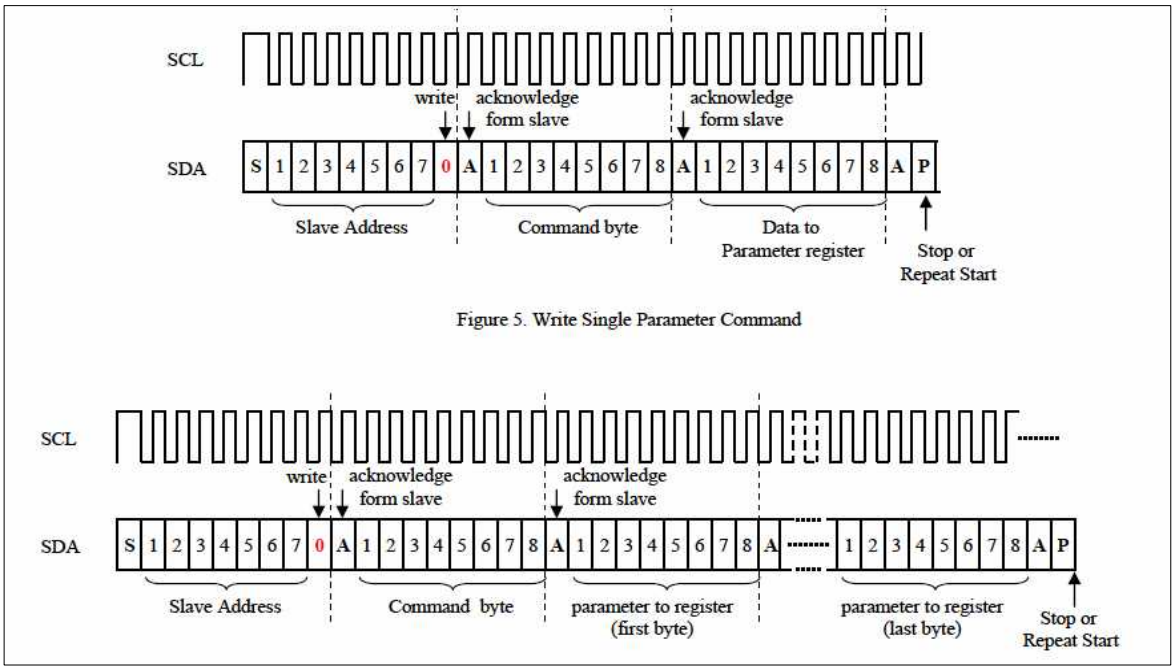
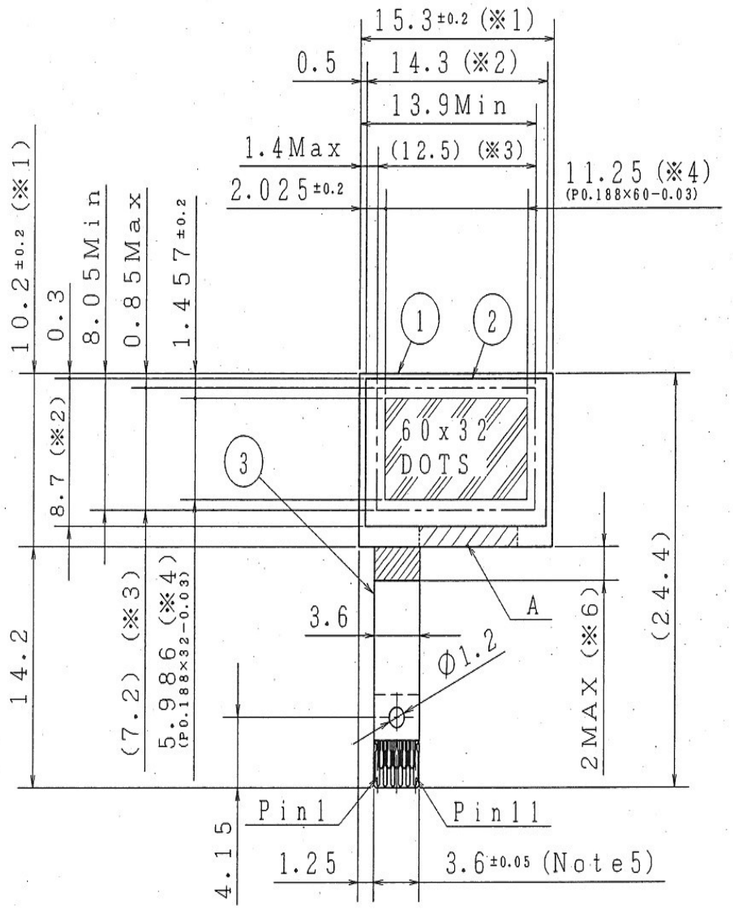
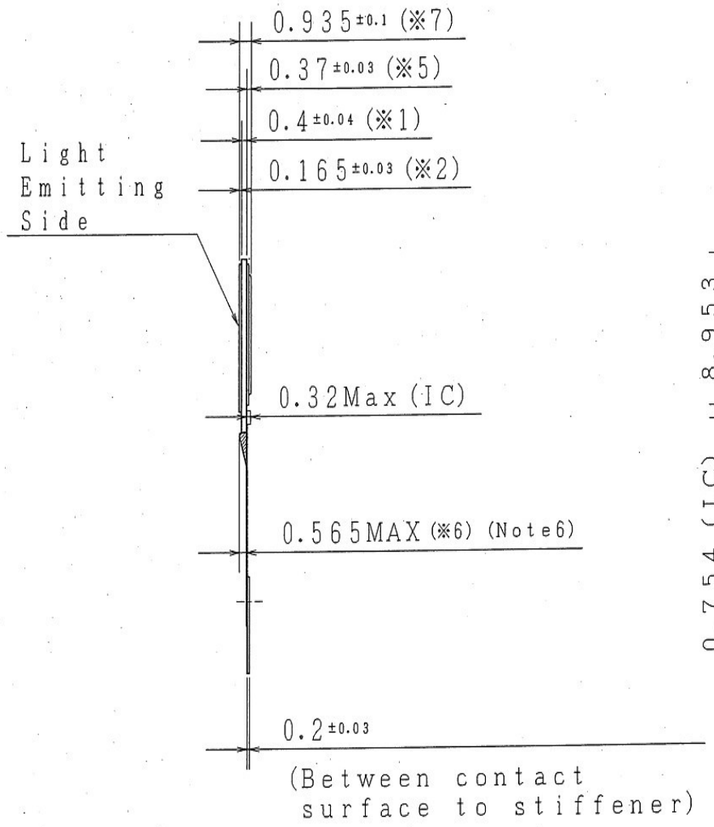
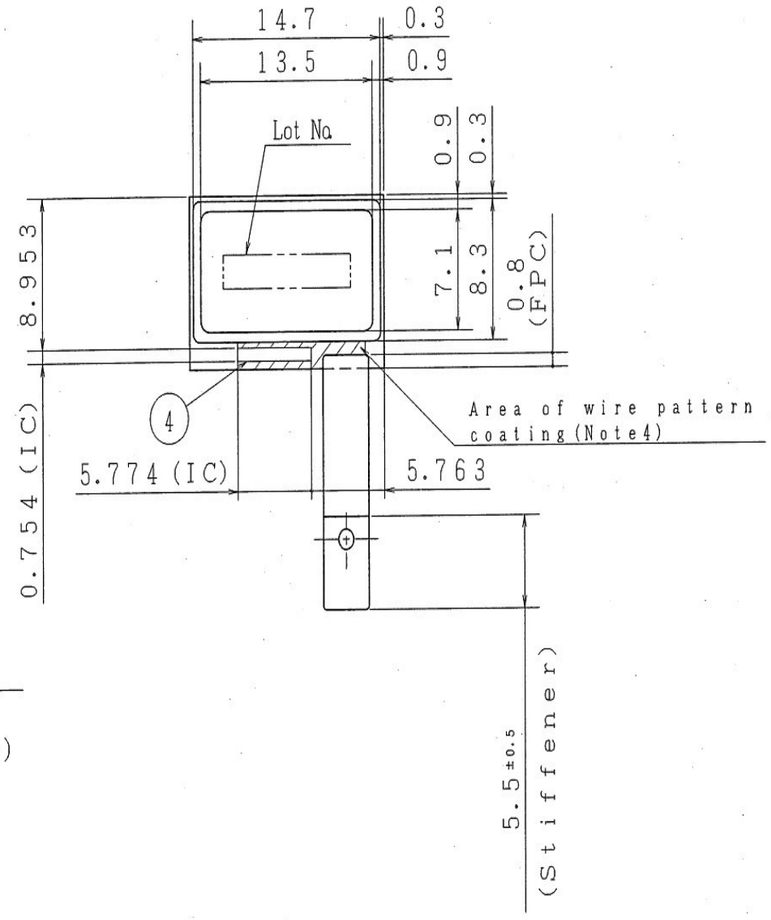


Figure 5. Write Single Parameter Command

MRK	DATE	PNO	REVISION RECORD	DR.	MRK	DATE	PNO	REVISION RECORD	DR.
1					5				
2					6				
3					7				
4					8				

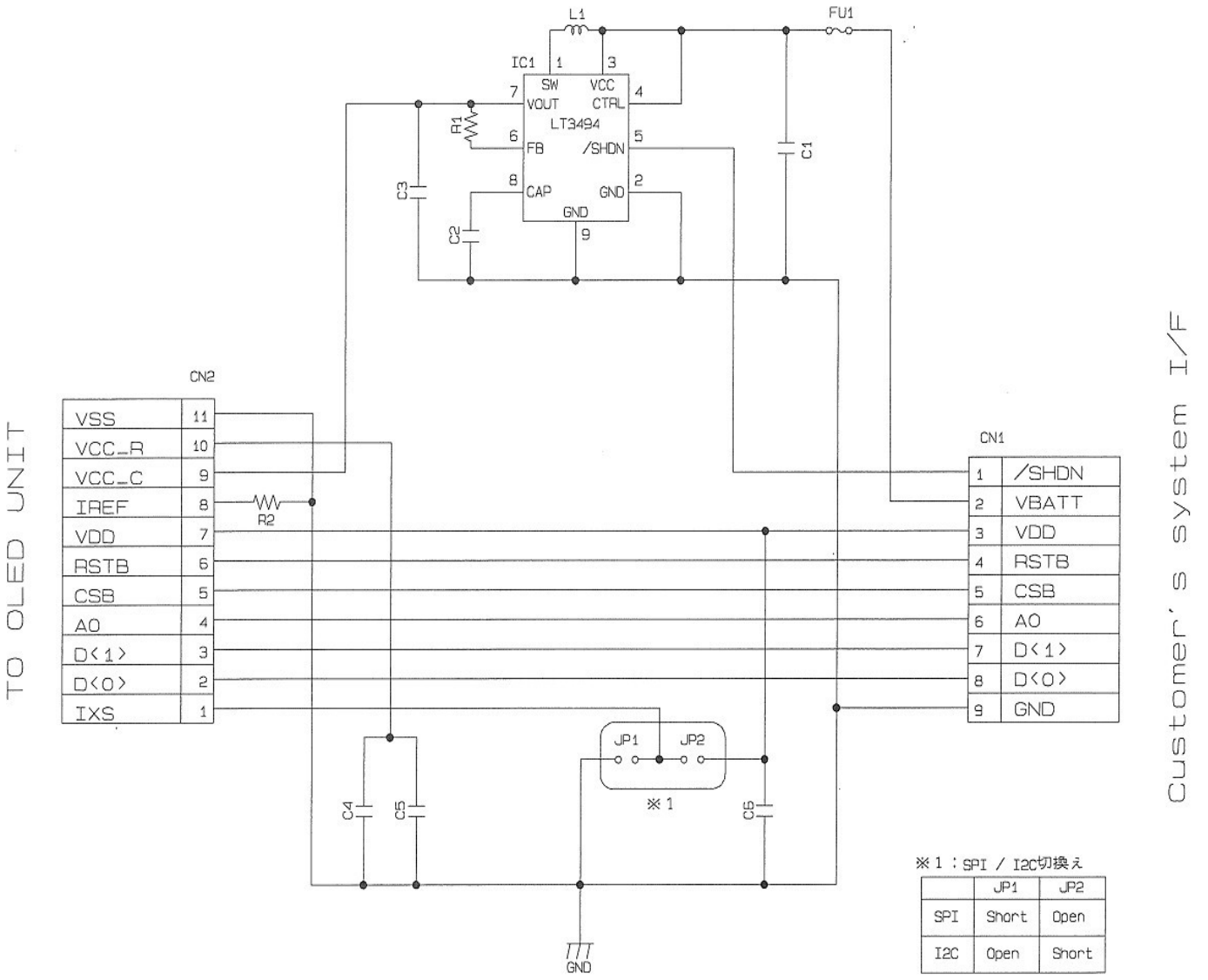






MRK	DATE	PNo	REVISION RECORD	DR	MRK	DATE	PNo	REVISION RECORD	DR
1					5				
2					6				
3					7				
4					8				

Serial(SPI/I2C) I/F



※1：SPI / I2C切換え

	JP1	JP2
SPI	Short	Open
I2C	Open	Short

PARTS NAME	PARTS ID	PARTS No	SUPPLIER	Characteristic	Note
Resistor	R1	-	-	1.8MΩ ±1% 1.0×0.5 t=0.35	
Resistor	R2	-	-	39KΩ ±0.5% 1.0×0.5 t=0.35	
Ceramic Capacitor	C1	-	-	10uF/6.3V 2.0×1.25 t=0.85	
Ceramic Capacitor	C2	-	-	0.22uF/25V 1.6×0.8 t=0.8	
Ceramic Capacitor	C3	-	-	2.2uF/25V 2.0×1.25 t=0.85	
Tantalum Capacitor	C4	ESVA1E105M	NEC-TOKIN	1.0uF/25V 2.0×1.25 t=0.85	
Ceramic Capacitor	C5	-	-	0.1uF/25V 1.0×0.5 t=0.5	
Ceramic Capacitor	C6・C7	-	-	0.1uF/6.3V 1.0×0.5 t=0.5	
Fuse	FU1	KAB5002 2501 NA29	MATSUO	0.25A 1.6×0.8 t=0.45	
Coil	L1	NR3012T150M	TAIYO YUDEN	15uH 440mA 3.0×3.0 t=1.2	
I C	IC1	LT3494EDDB	LINEAR TECHNOLOGY	3.0×2.0 t=0.75	
Connector	CN2	6296 / 6843	KYOCERA CONNECTOR PRODUCTS	0.3mm Pitch	11Pin