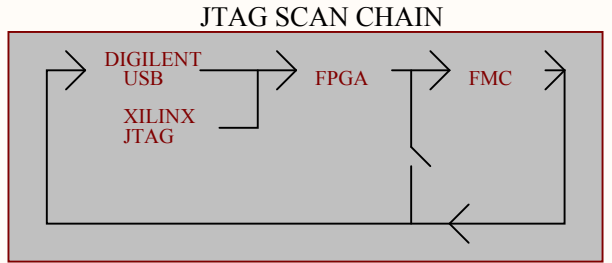
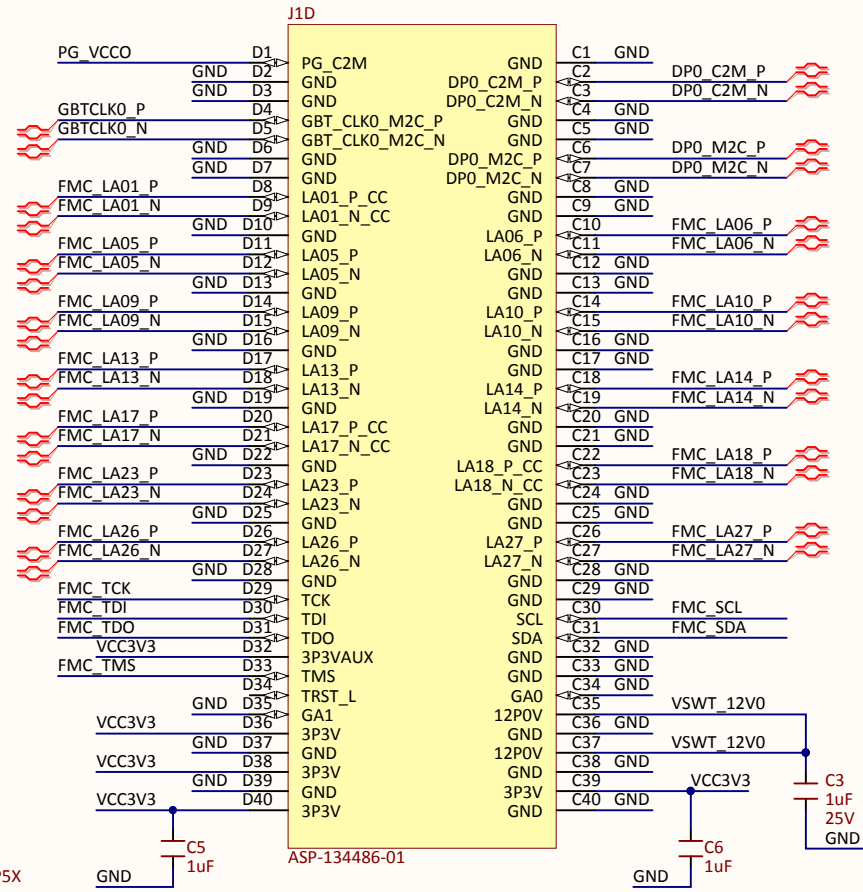
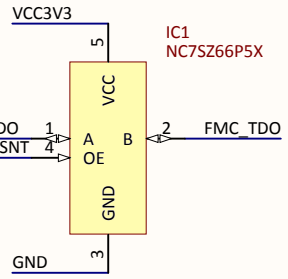
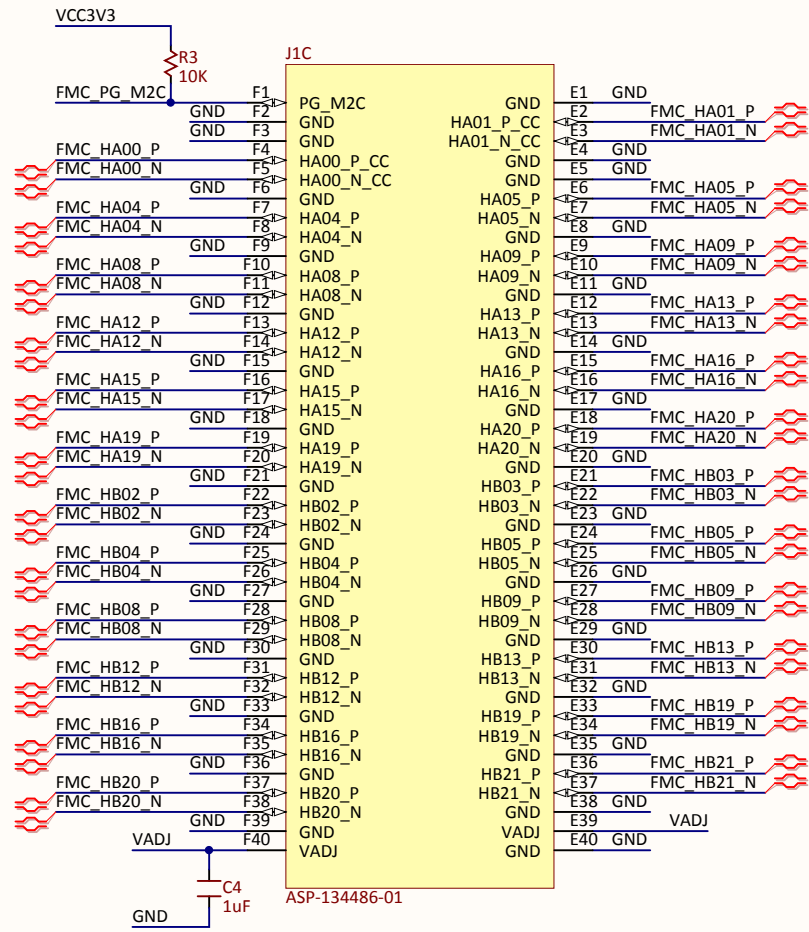


- SHIELD F Foot F1
- SHIELD F Foot F2
- SHIELD F Foot F3
- SHIELD F Foot F4
- SHIELD F5 Heatsink

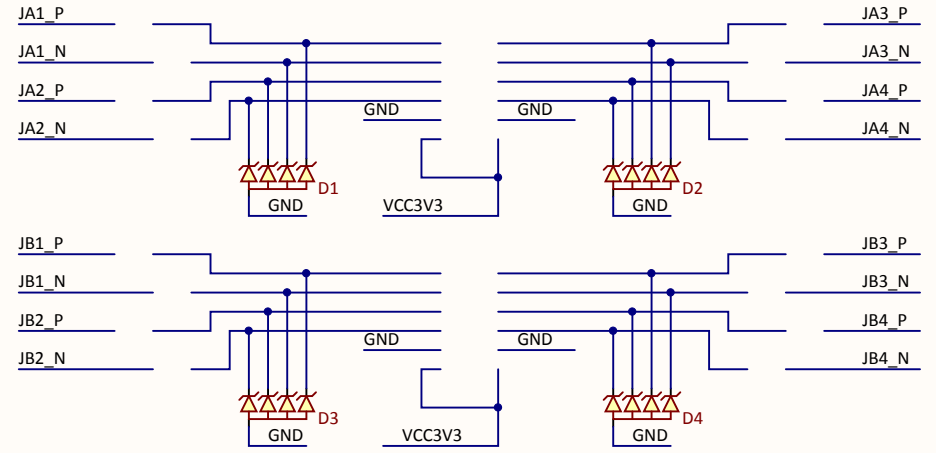
- CE
- ROHS
- Xilinx
- Genesys2
- Digilent Inc.
- Linear Tech
- Chinese ROHS

Malico MBF31035-24P + Sunon MC30101V1-0000-G99

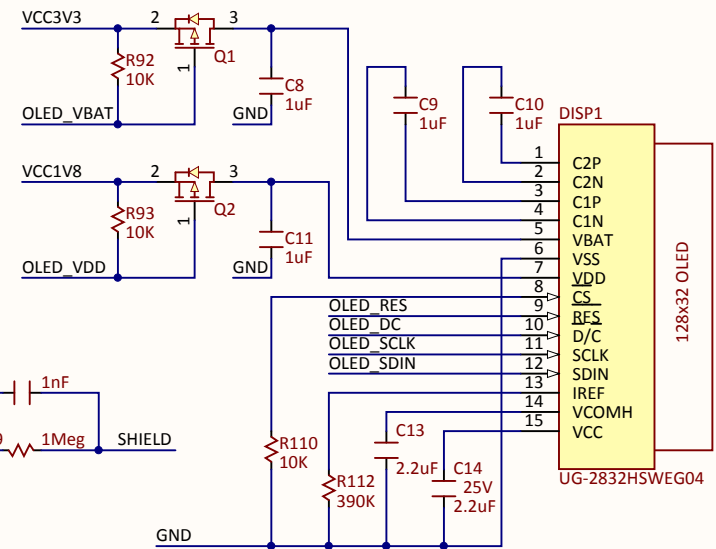
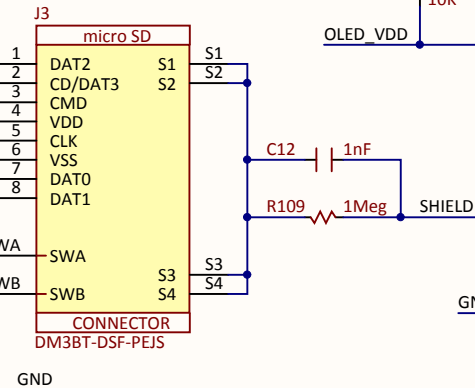
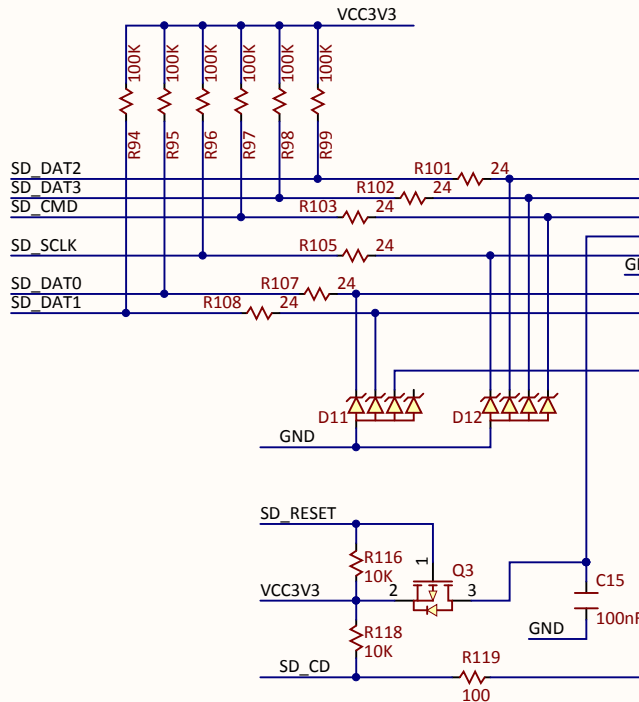
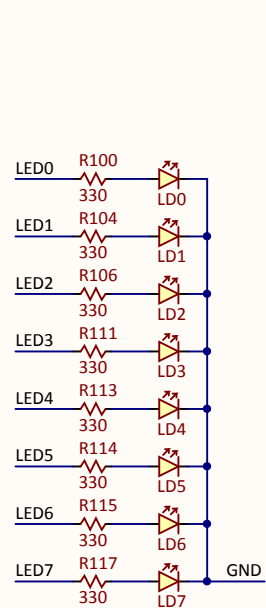
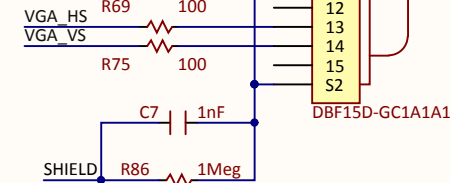
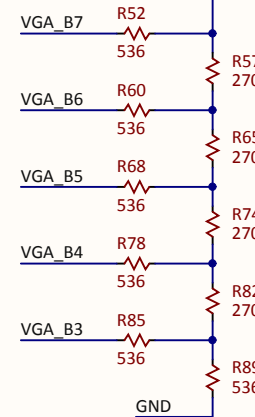
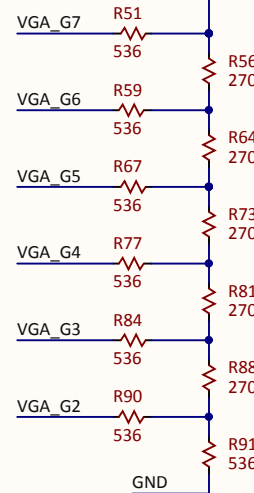
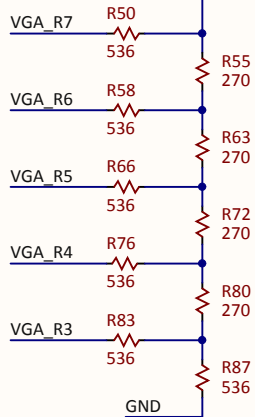
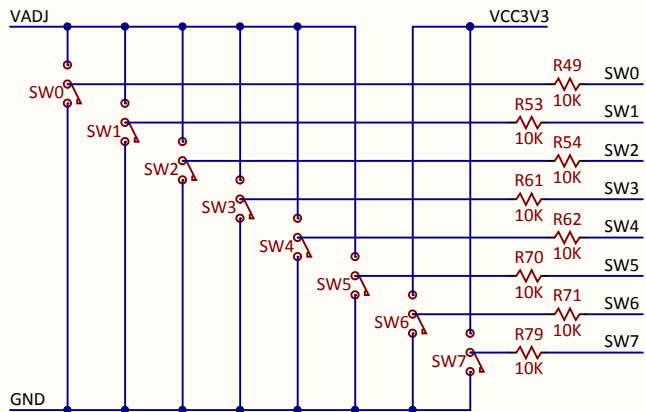
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|--------------------|---------------|----------------|--|
| Title | | Rev | |
| <h1>Genesys 2</h1> | | <h1>H.1</h1> | |
| | | Copyright 2015 | |
| Circuit | FMC CONNECTOR | | |
| Doc# | 500-300 | | |
| Engineer | EG | | |
| Author | DL | | |
| Date | 7/17/2015 | | |
| Sheet# | 1 out of 22 | | |



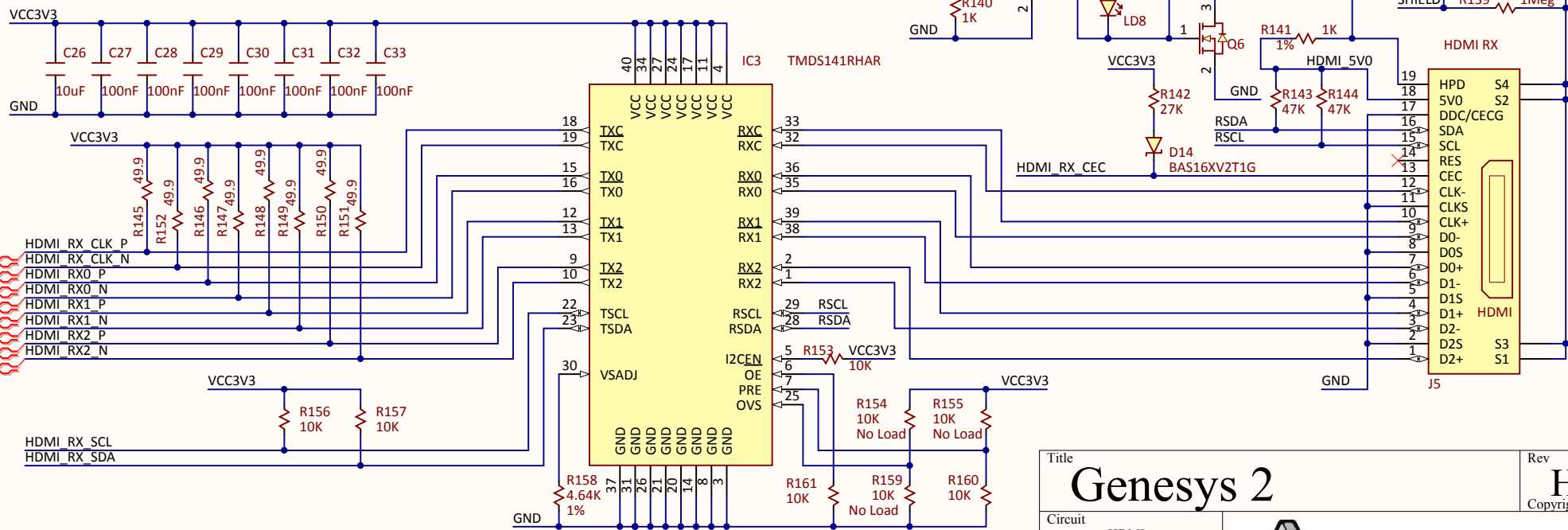
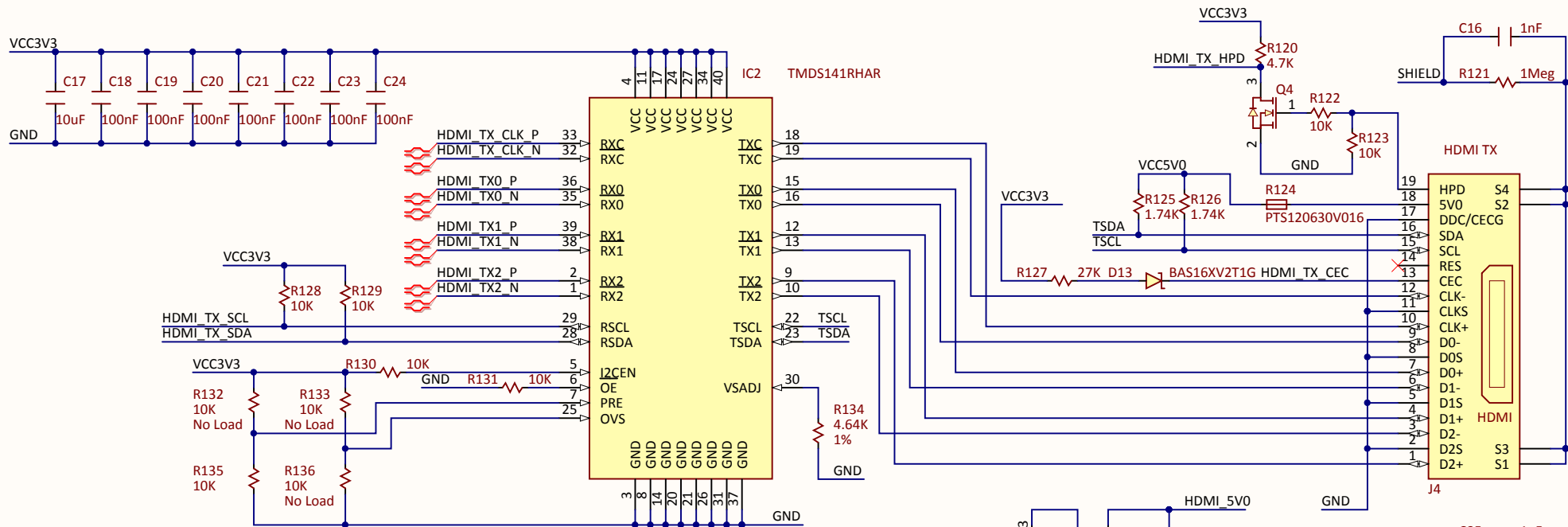
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|------------------|-------------|----------------|
| Title | | Rev |
| Genesys 2 | | H.1 |
| Circuit | | Copyright 2015 |
| FMC CONNECTOR | | |
| Doc# | 500-300 | |
| Engineer | EG | |
| Author | DL | |
| Date | 7/17/2015 | |
| Sheet# | 2 out of 22 | |




| | | |
|---------------------------|-------------|-------------------------------------|
| Title Genesys 2 | | Rev H.1 Copyright 2015 |
| Circuit | | |
| Doc# | 500-300 | |
| Engineer | EG | |
| Author | DL | |
| Date | 7/17/2015 | |
| Sheet# | 3 out of 22 | |

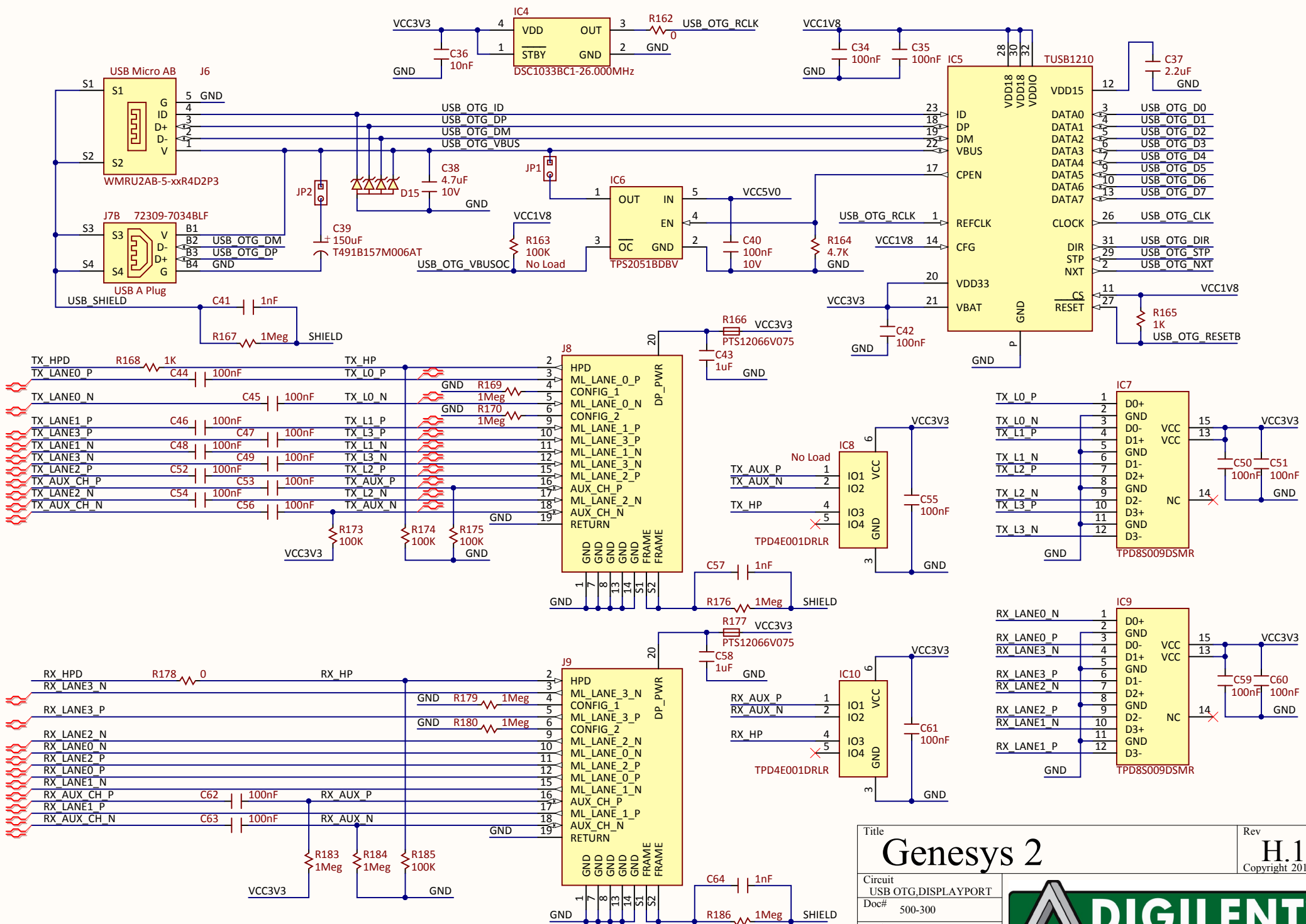


| | | |
|---------------------|-------------|----------------|
| Title | | Rev |
| Genesis 2 | | H.1 |
| Circuit | | Copyright 2015 |
| VGA, OLED, SD, GPIO | | |
| Doc# | 500-300 | |
| Engineer | EG | |
| Author | DL | |
| Date | 7/17/2015 | |
| Sheet# | 4 out of 22 | |




| | | | |
|-----------|-------------|----------------|--|
| Title | | Rev | |
| Genesys 2 | | H.1 | |
| Circuit | | Copyright 2015 | |
| HDMI | | | |
| Doc# | 500-300 | | |
| Engineer | EG | | |
| Author | DL | | |
| Date | 7/17/2015 | | |
| Sheet# | 5 out of 22 | | |



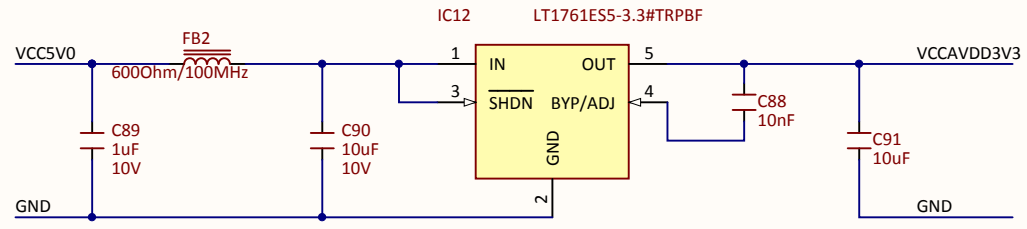
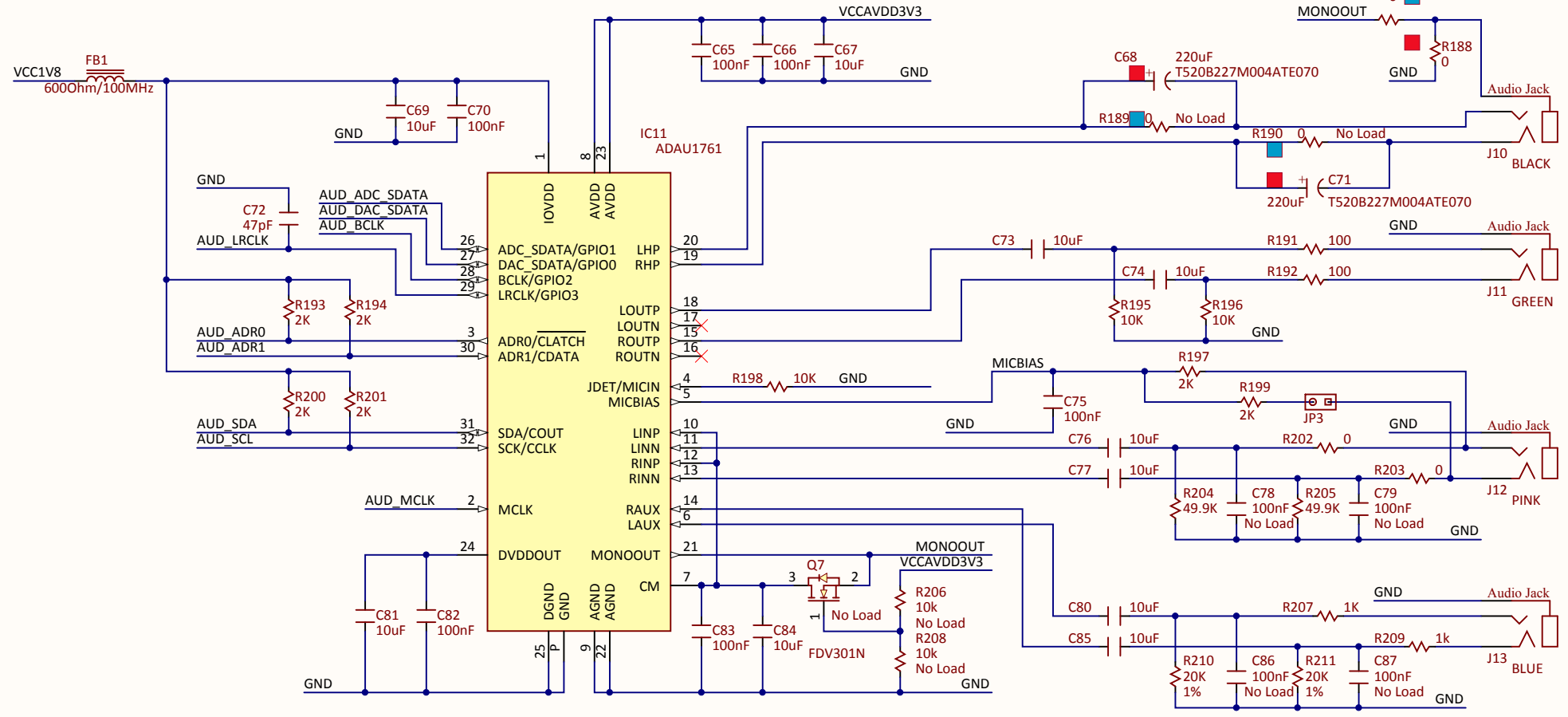


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|--------------------|--|---------------------|--|
| Title | | Rev | |
| <h1>Genesis 2</h1> | | <h1>H.1</h1> | |
| Circuit | | USB OTG.DISPLAYPORT | |
| Doc# | | 500-300 | |
| Engineer | | EG | |
| Author | | DL | |
| Date | | 7/17/2015 | |
| Sheet# | | 6 out of 22 | |




DIGILENT
BEYOND THEORY

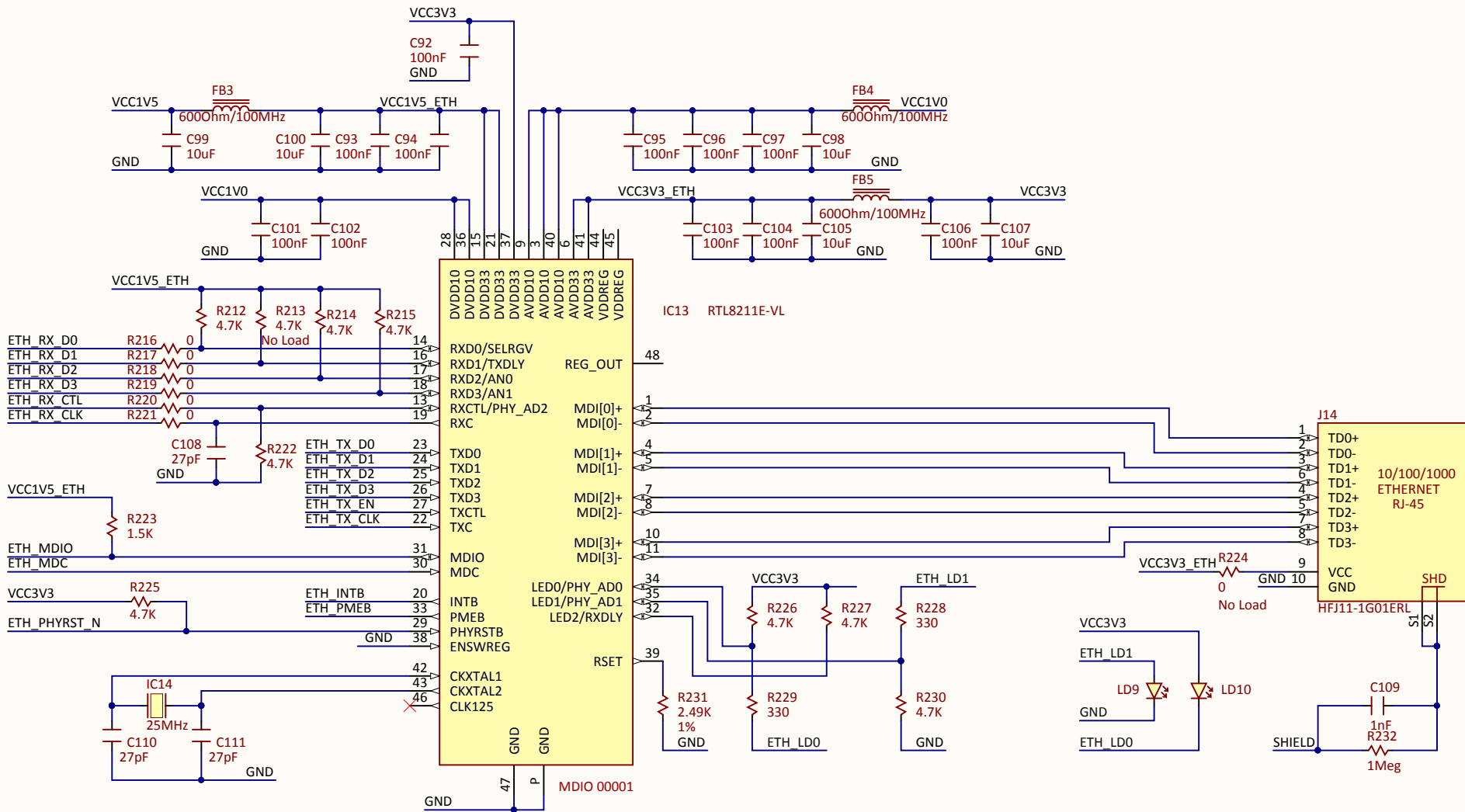
NOTE: Load No Load
 Capless Headphone ■ ■
 AC-Coupled Headphone ■ ■




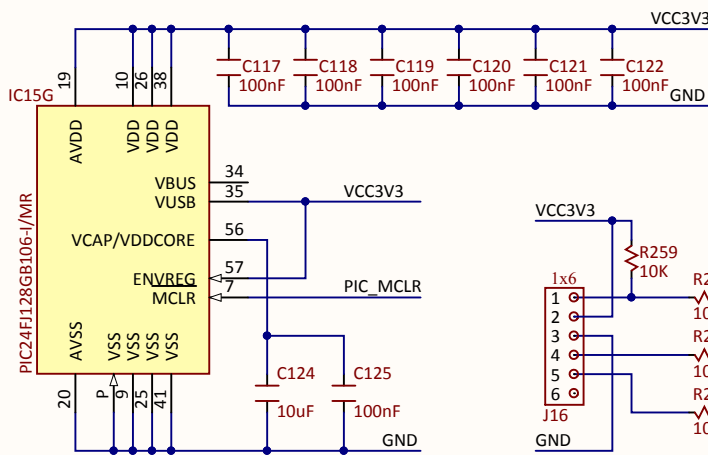
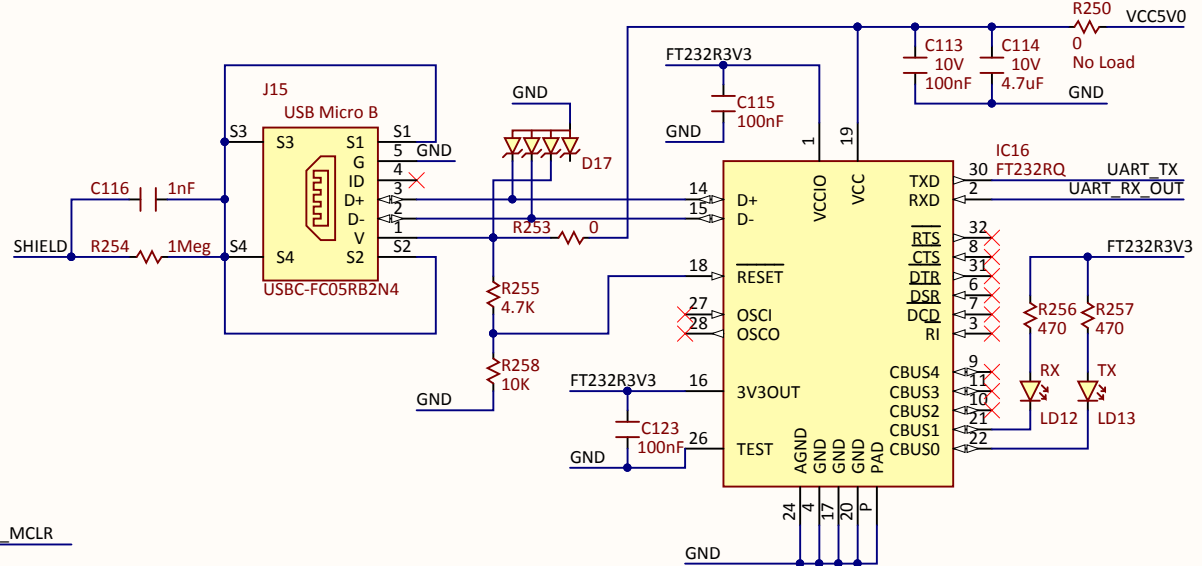
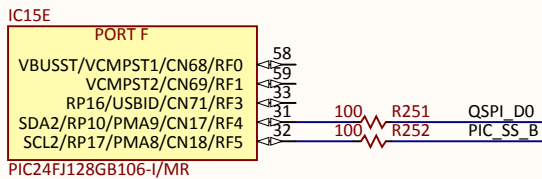
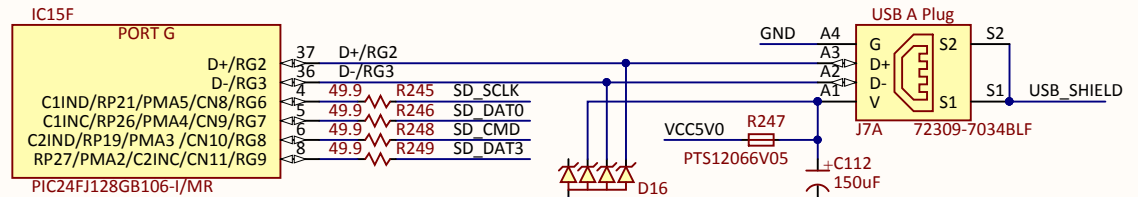
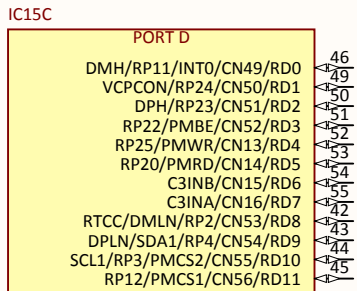
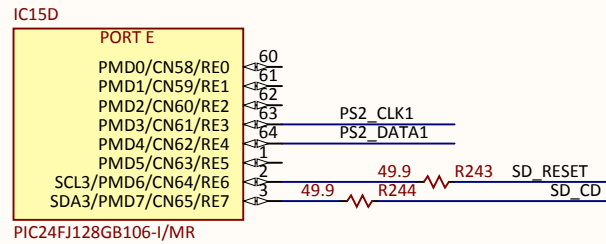
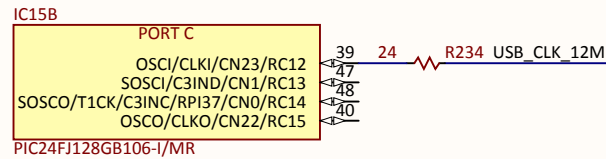
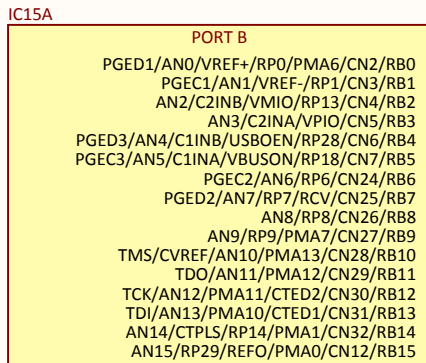
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| Title | | Rev | |
| <h1>Genesis 2</h1> | | <h1>H.1</h1> | |
| | | Copyright 2015 | |
| Circuit | AUDIO | | |
| Doc# | 500-300 | | |
| Engineer | EG | | |
| Author | DL | | |
| Date | 7/17/2015 | | |
| Sheet# | 7 out of 22 | | |



DIGILENT
BEYOND THEORY

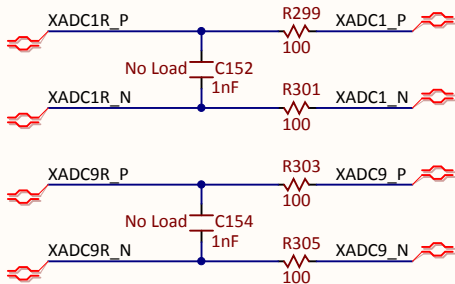
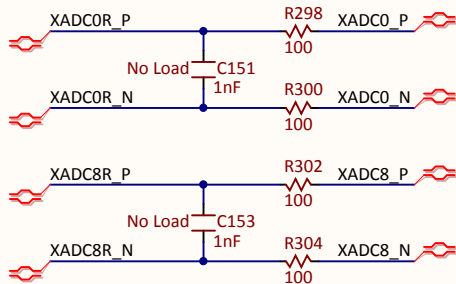
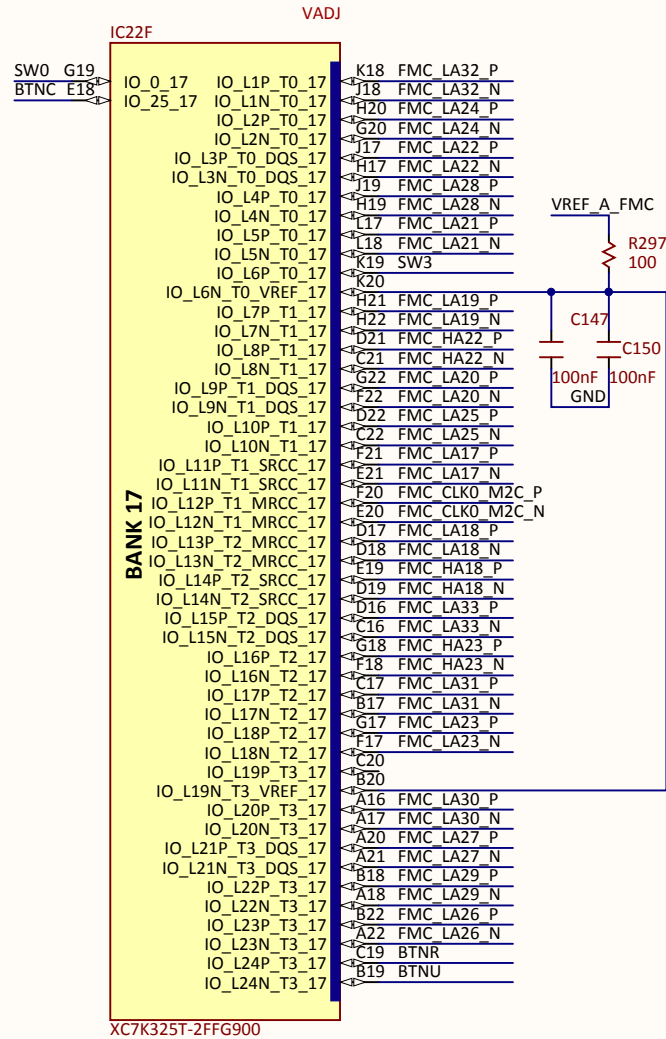
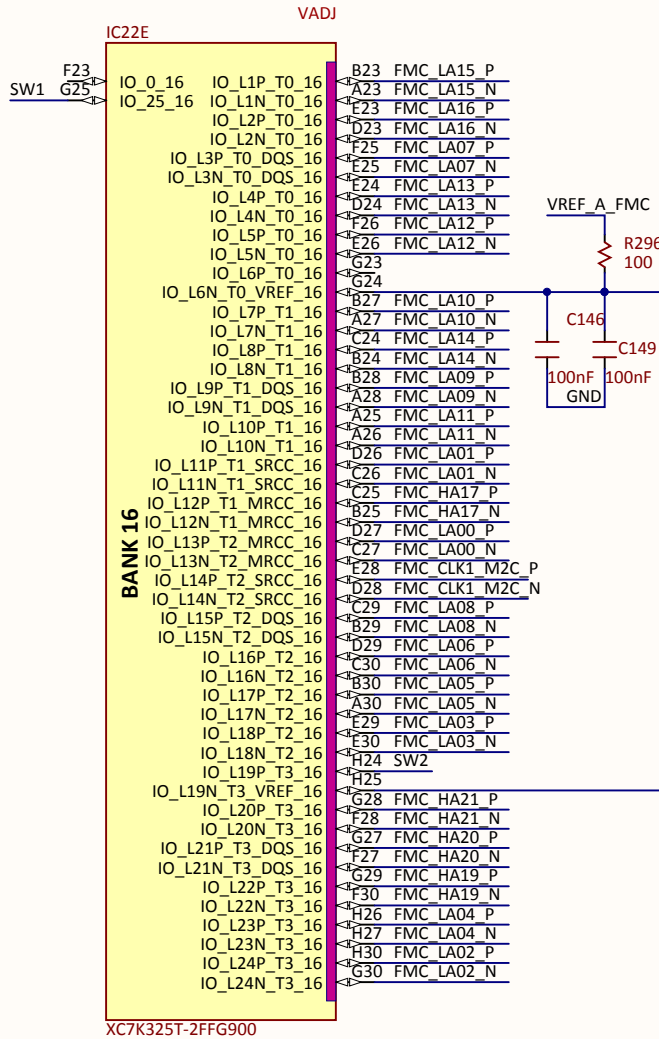
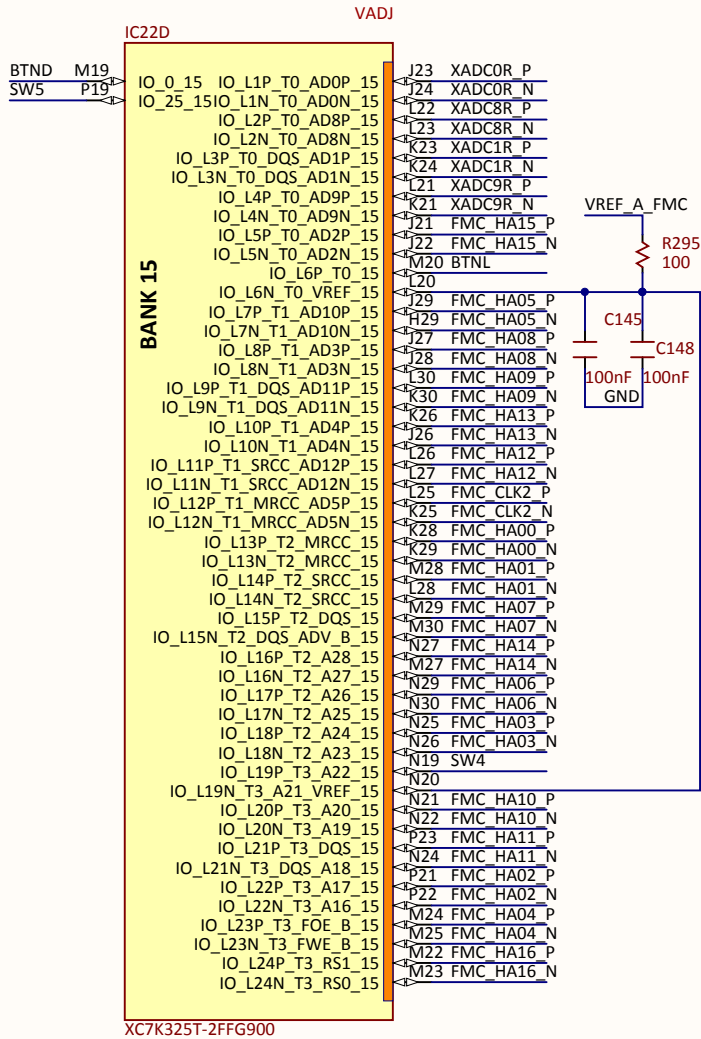


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|---------------------------|-----------------------|---|
| Title Genesis 2 | | Rev H.1 Copyright 2015 |
| Circuit ETHERNET | Doc# 500-300 |  |
| Engineer EG | Author DL | |
| Date 7/17/2015 | Sheet# 8 out of 22 | |




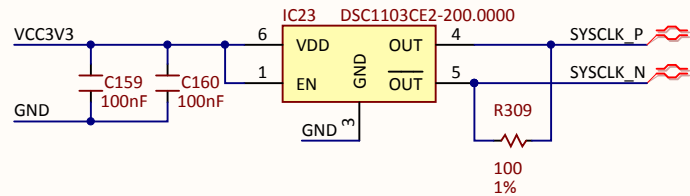
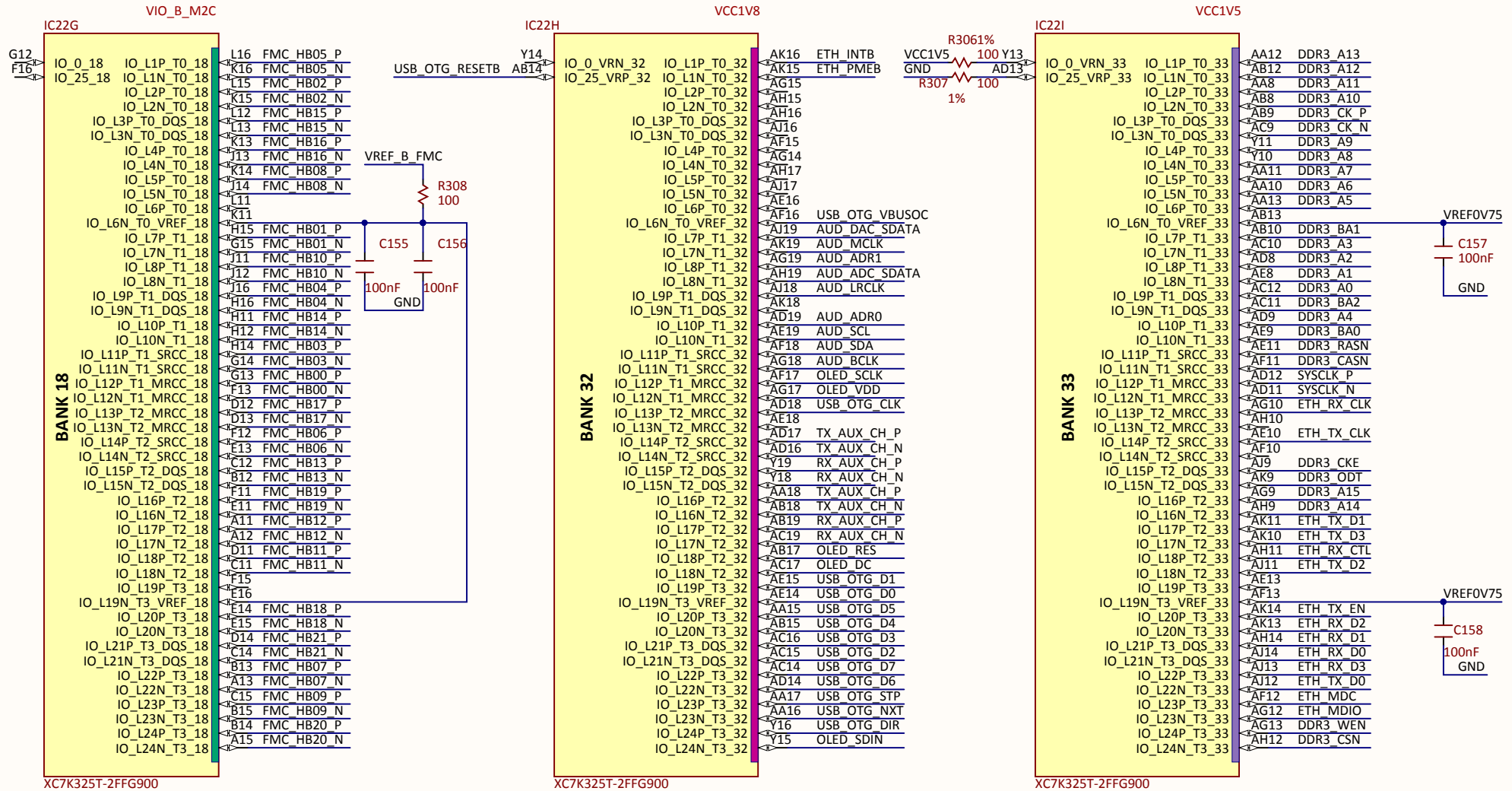
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|------------------|-------------|----------------|--|
| Title | | Rev | |
| Genesis 2 | | H.1 | |
| Circuit | | Copyright 2015 | |
| USB HID, UART | | | |
| Doc# | 500-300 | | |
| Engineer | EG | | |
| Author | DL | | |
| Date | 7/17/2015 | | |
| Sheet# | 9 out of 22 | | |

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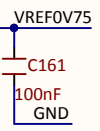
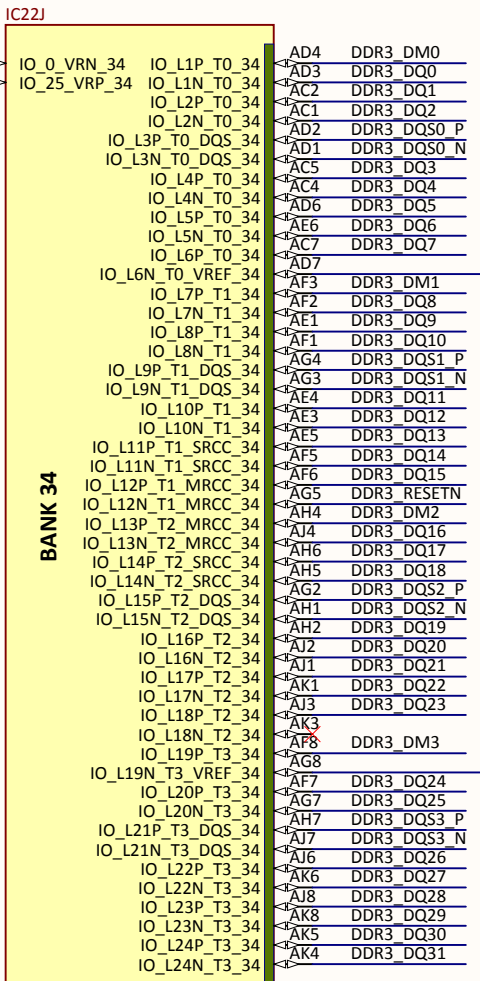
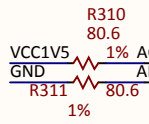


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|--------------------|--------------|----------------|
| Title | | Rev |
| <h1>Genesis 2</h1> | | H.1 |
| | | Copyright 2015 |
| Circuit | FPGA BANKS | |
| Doc# | 500-300 | |
| Engineer | EG | |
| Author | DL | |
| Date | 7/17/2015 | |
| Sheet# | 12 out of 22 | |



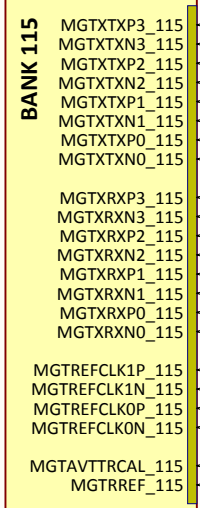


| | | |
|------------------|--------------|----------------|
| Title | | Rev |
| Genesys 2 | | H.1 |
| Circuit | | Copyright 2015 |
| FPGA BANKS | | |
| Doc# | 500-300 | |
| Engineer | EG | |
| Author | DL | |
| Date | 7/17/2015 | |
| Sheet# | 13 out of 22 | |



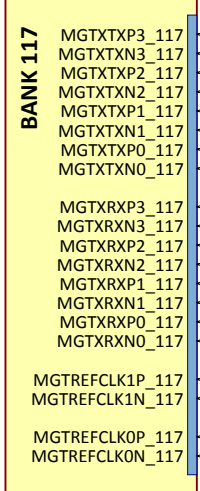
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IC22K



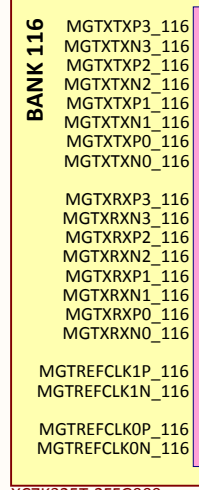
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IC22M



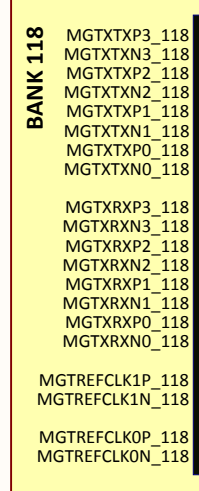
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IC22L

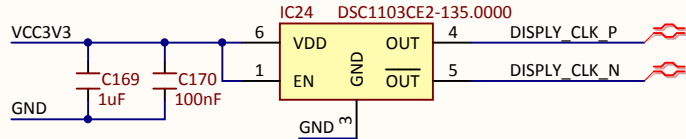


XC7K325T-2FFG900

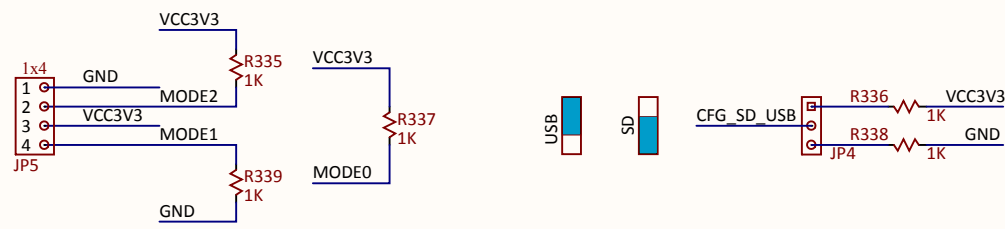
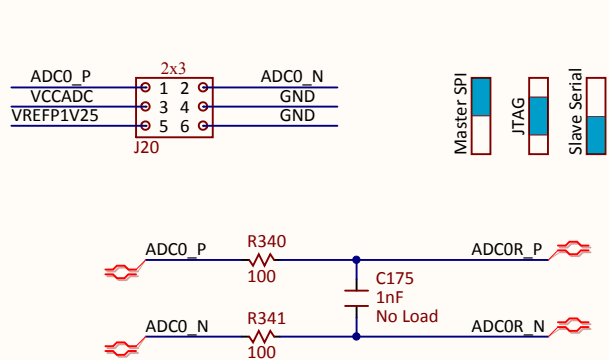
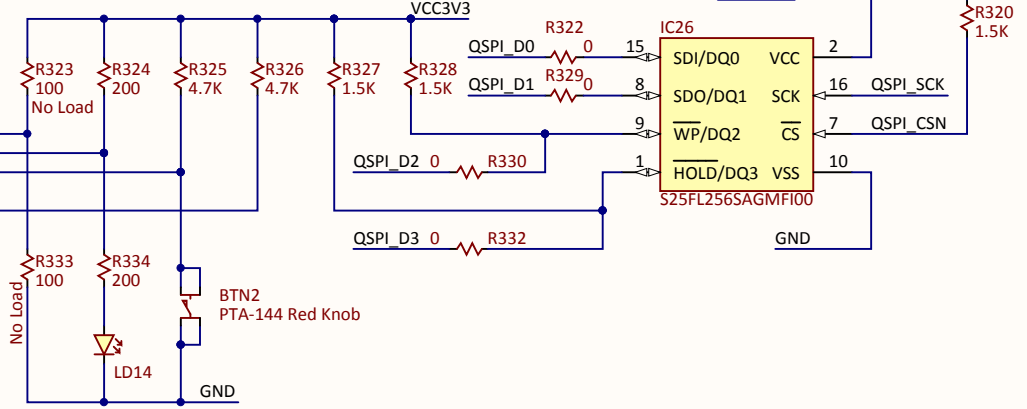
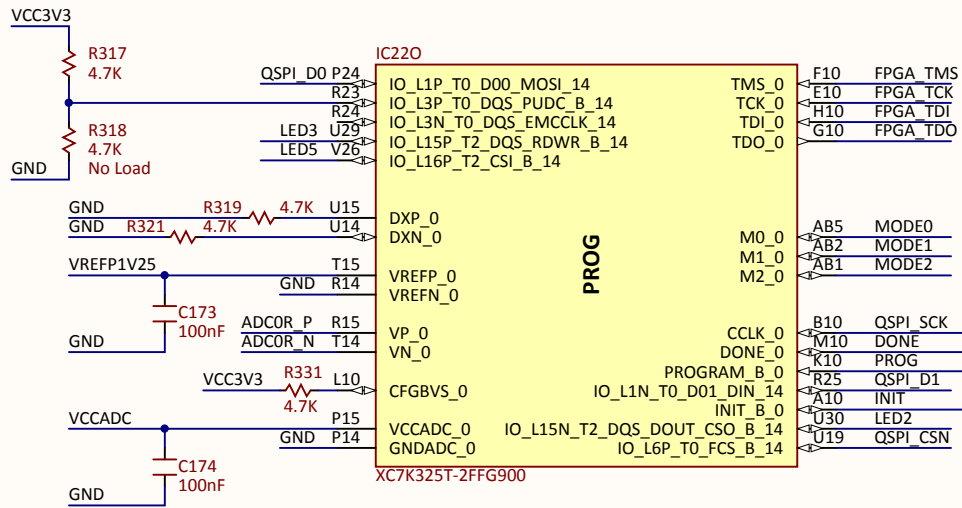
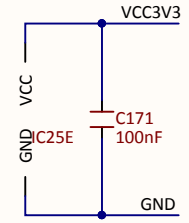
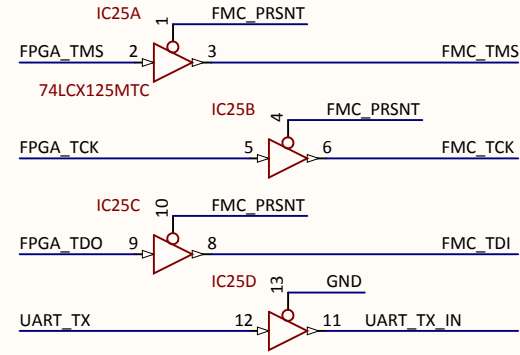
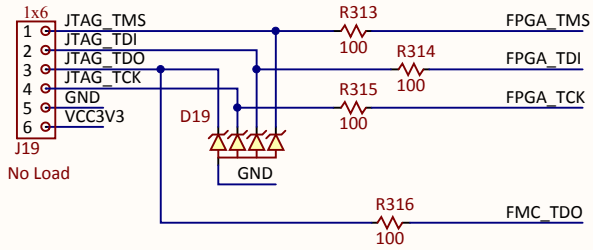
IC22N



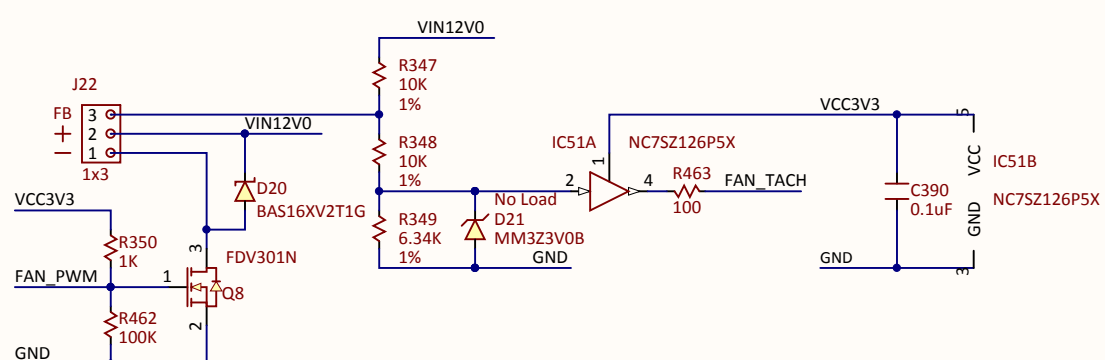
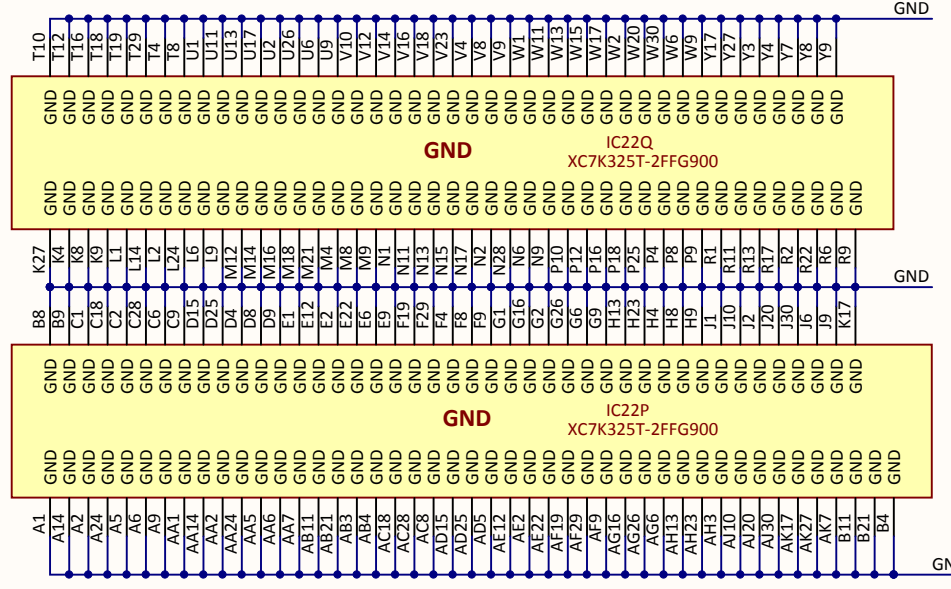
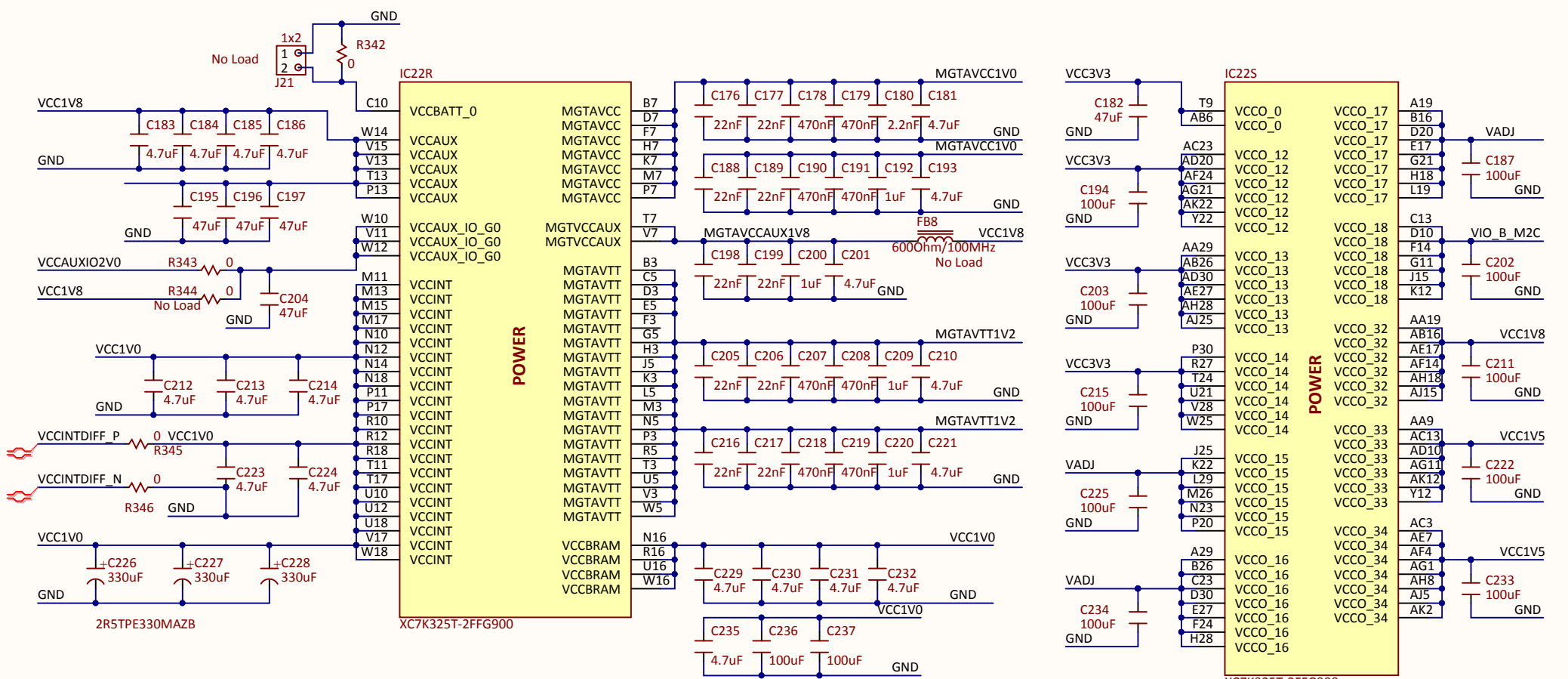
XC7K325T-2FFG900



| | | |
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| Title Genesys 2 | | Rev H.1 Copyright 2015 |
| Circuit FPGA BANKS | | |
| Doc# 500-300 | | |
| Engineer EG | | |
| Author DL | | |
| Date 7/17/2015 | | |
| Sheet# 14 out of 22 | | |



| | | |
|------------------------------|--|-------------------------------------|
| Title Genesis 2 | | Rev H.1 Copyright 2015 |
| Circuit CONFIG, SPI FLASH | | |
| Doc# 500-300 | | |
| Engineer EG | | |
| Author DL | | |
| Date 7/17/2015 | | |
| Sheet# 15 out of 22 | | |



| | | |
|---------------------------|--|-------------------|
| Title Genesis 2 | | Rev H.1 |
| Circuit FPGA POWER | | Copyright 2015 |
| Doc# 500-300 | | |
| Engineer EG | | |
| Author DL | | |
| Date 7/17/2015 | | |
| Sheet# 16 out of 22 | | |

A

A

B

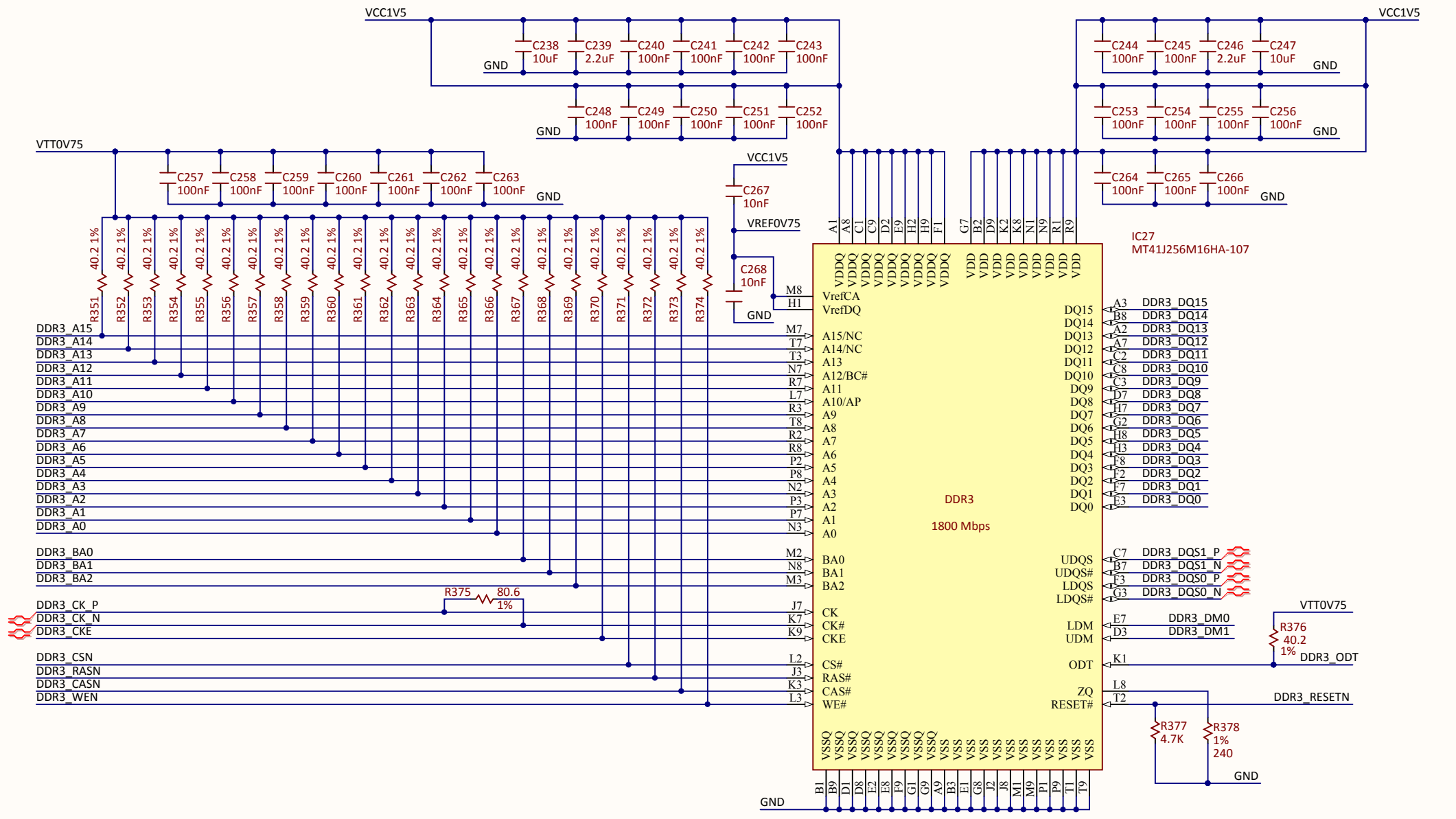
B

C

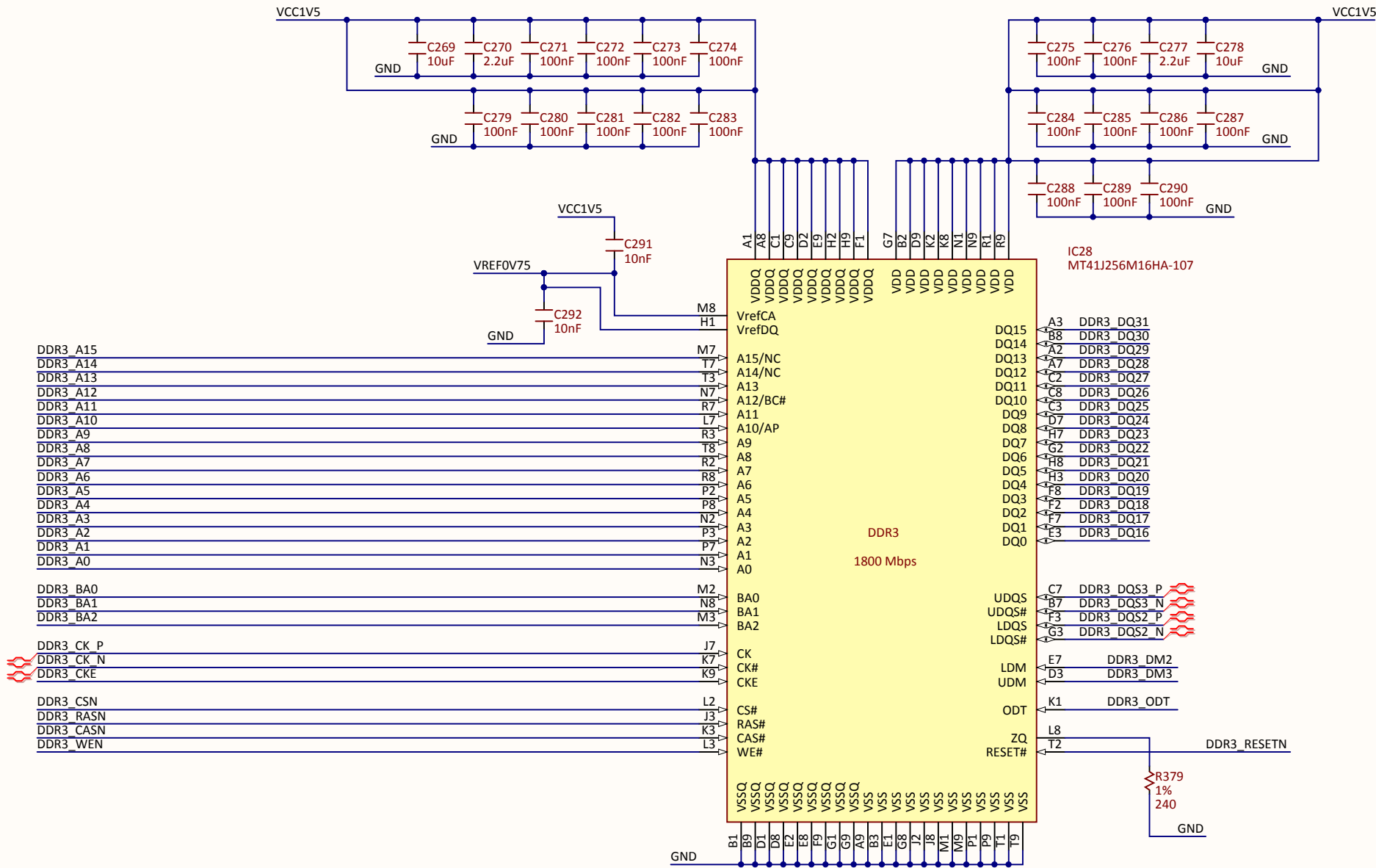
C

D

D



| | | | |
|--------------------|--------------|----------------|--|
| Title | | Rev | |
| <h1>Genesis 2</h1> | | <h1>H.1</h1> | |
| | | Copyright 2015 | |
| Circuit | DDR3 | | |
| Doc# | 500-300 | | |
| Engineer | EG | | |
| Author | DL | | |
| Date | 7/17/2015 | | |
| Sheet# | 17 out of 22 | | |



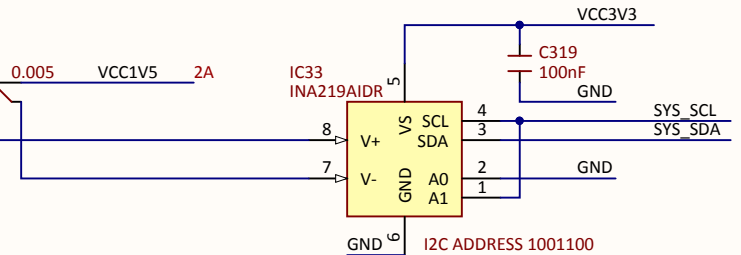
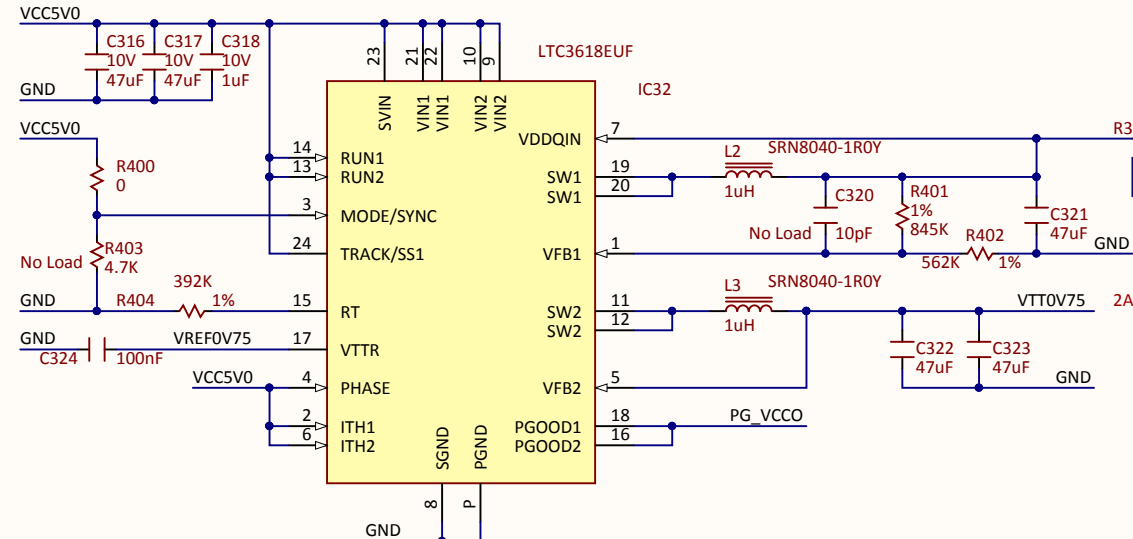
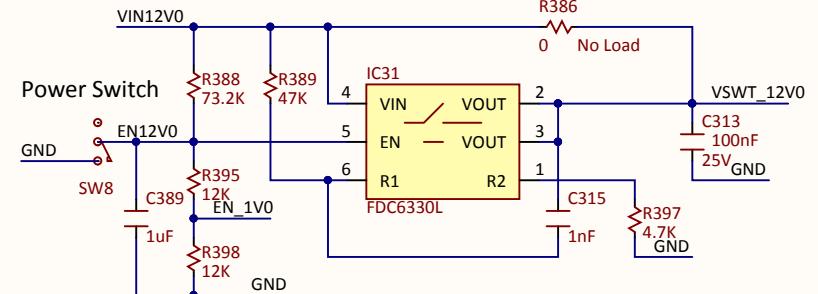
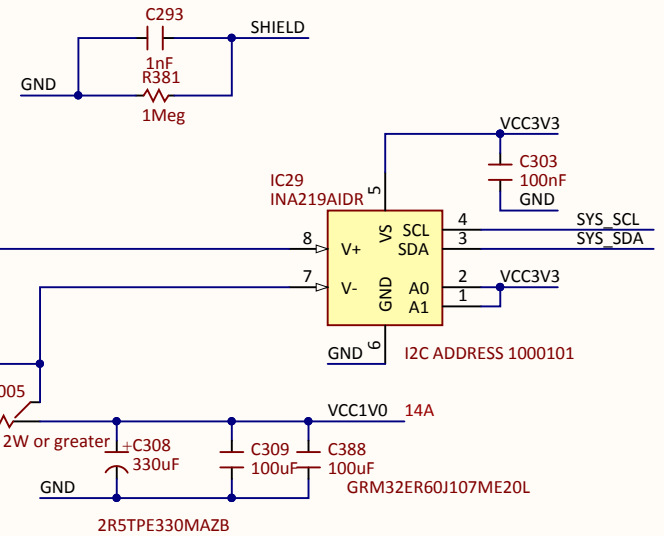
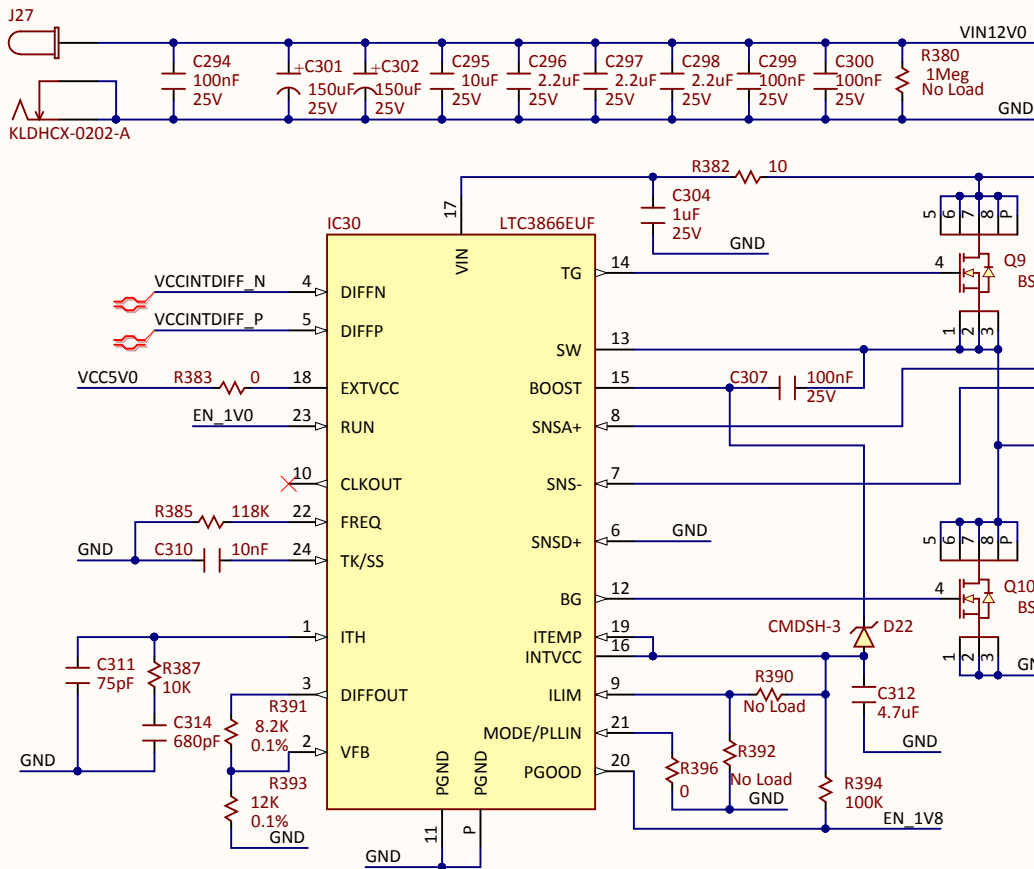
- DDR3_A15
- DDR3_A14
- DDR3_A13
- DDR3_A12
- DDR3_A11
- DDR3_A10
- DDR3_A9
- DDR3_A8
- DDR3_A7
- DDR3_A6
- DDR3_A5
- DDR3_A4
- DDR3_A3
- DDR3_A2
- DDR3_A1
- DDR3_A0

- DDR3_BA0
- DDR3_BA1
- DDR3_BA2

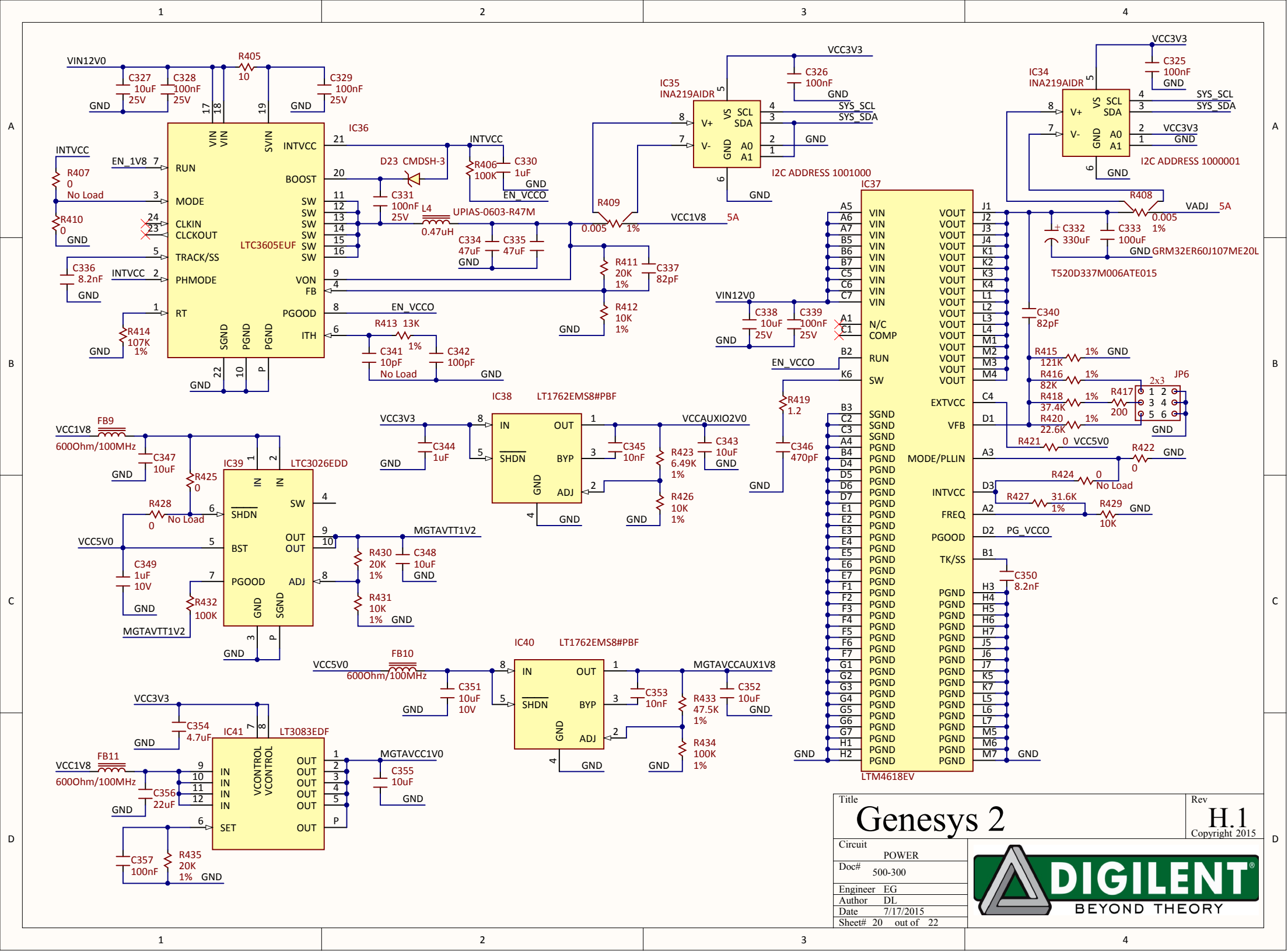
- DDR3_CK_P
- DDR3_CK_N
- DDR3_CKE

- DDR3_CSN
- DDR3_RASN
- DDR3_CASN
- DDR3_WEN

| | | |
|---------------------------|------------------------|-------------------------------------|
| Title Genesys 2 | | Rev H.1 Copyright 2015 |
| Circuit DDR3 | Doc# 500-300 | |
| Engineer EG | Author DL | |
| Date 7/17/2015 | Sheet# 18 out of 22 | |

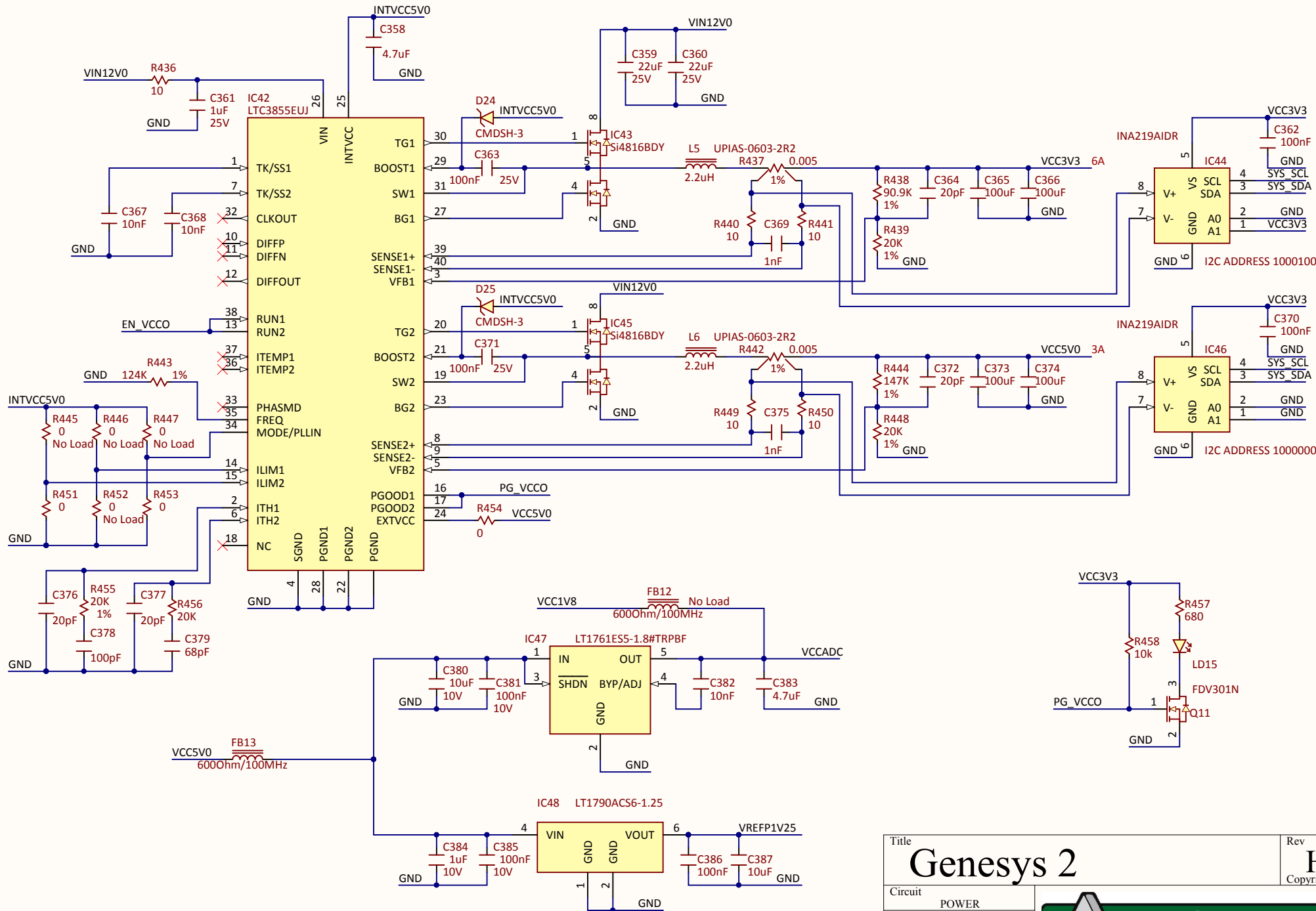


| | | | |
|--------------------|--------------|----------------|--|
| Title | | Rev | |
| <h1>Genesis 2</h1> | | H.1 | |
| | | Copyright 2015 | |
| Circuit | POWER | | |
| Doc# | 500-300 | | |
| Engineer | EG | | |
| Author | DL | | |
| Date | 7/17/2015 | | |
| Sheet# | 19 out of 22 | | |

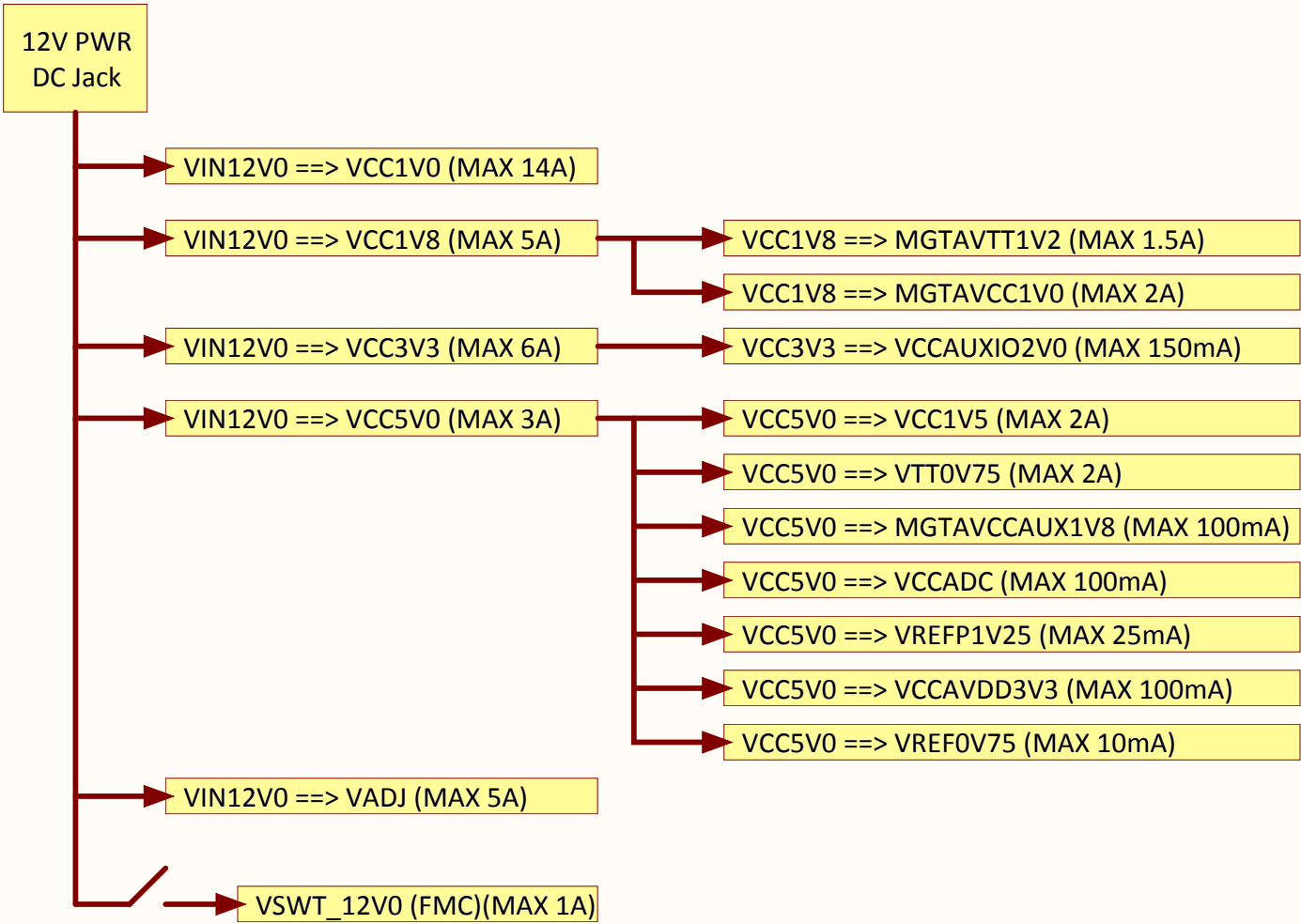


| | | |
|------------------|--------------|----------------|
| Title | | Rev |
| Genesis 2 | | H.1 |
| Circuit | | POWER |
| Doc# | 500-300 | Copyright 2015 |
| Engineer | EG | |
| Author | DL | |
| Date | 7/17/2015 | |
| Sheet# | 20 out of 22 | |





| | | |
|---------------------------|------------------------|-------------------------------------|
| Title Genesis 2 | | Rev H.1 Copyright 2015 |
| Circuit POWER | Doc# 500-300 | |
| Engineer EG | Author DL | |
| Date 7/17/2015 | Sheet# 21 out of 22 | |



| | | |
|---------------------------|--|-------------------------------------|
| Title Genesys 2 | | Rev H.1 Copyright 2015 |
| Circuit POWER TREE | | |
| Doc# 500-300 | | |
| Engineer EG | | |
| Author DL | | |
| Date 7/17/2015 | | |
| Sheet# 22 out of 22 | | |