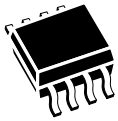
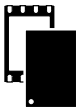
M24LR64E-R

Dynamic NFC/RFID tag IC with 64-Kbit EEPROM, energy harvesting, I²C bus and ISO 15693 RF interface

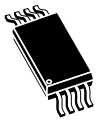
Datasheet - production data



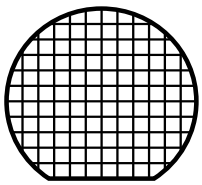
SO8 (MN)
150 mils width



UFDFPN8 (MC) 2 x 3 mm



TSSOP8 (DW)



Wafer (SB12I)

Features

I²C interface

- Two-wire I²C serial interface supports 400 kHz protocol
- Single supply voltage:
  - 1.8 V to 5.5 V
- Byte and Page Write (up to 4 bytes)
- Random and Sequential read modes
- Self-timed programming cycle
- Automatic address incrementing
- Enhanced ESD/latch-up protection
- I²C timeout

Contactless interface

- ISO 15693 and ISO 18000-3 mode 1 compatible
- 13.56 MHz ± 7 kHz carrier frequency
- To tag: 10% or 100% ASK modulation using 1/4 (26 Kbit/s) or 1/256 (1.6 Kbit/s) pulse position coding
- From tag: load modulation using Manchester coding with 423 kHz and 484 kHz subcarriers in low (6.6 kbit/s) or high (26 kbit/s) data rate mode. Supports the 53 kbit/s data rate with Fast commands
- Internal tuning capacitance: 27.5 pF
- 64-bit unique identifier (UID)
- Read Block & Write (32-bit blocks)

Digital output pin

- User configurable pin: RF write in progress or RF busy mode

Energy harvesting

- Analog pin for energy harvesting
- 4 sink current configurable ranges

Memory

- 64-Kbit EEPROM organized into:
  - 8192 bytes in I²C mode
  - 2048 blocks of 32 bits in RF mode
- Write time
  - I²C: 5 ms (max.)
  - RF: 5.75 ms including the internal Verify time
- More than 1 million write cycles
- More than 40-year data retention
- Multiple password protection in RF mode
- Single password protection in I²C mode
- Package
  - ECOPACK2® (RoHS compliant and Halogen-free)

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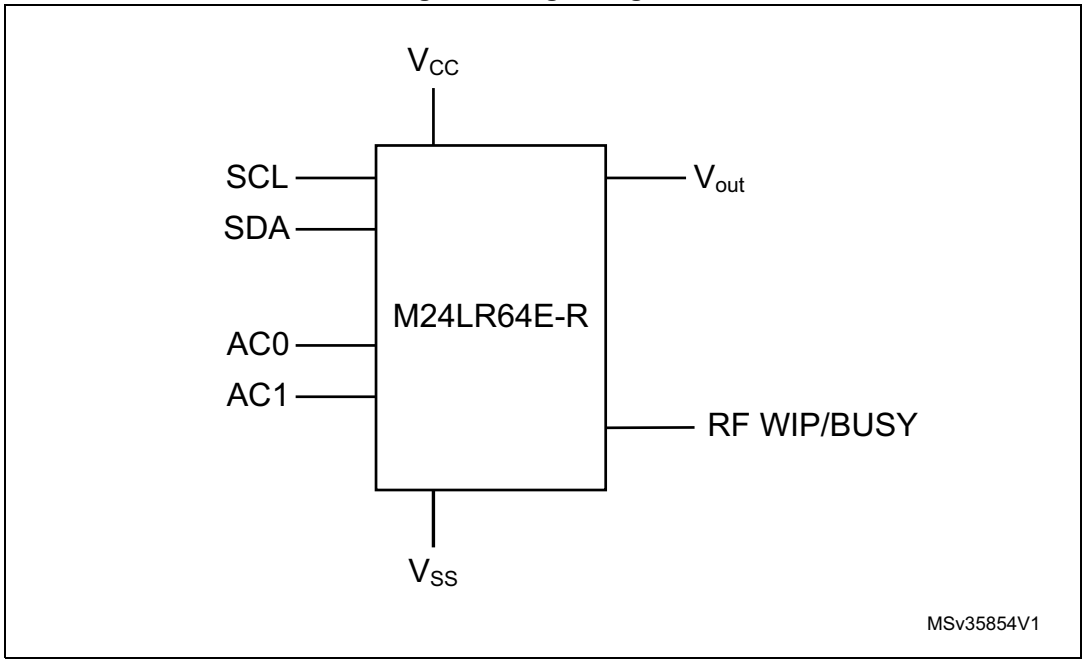
1 Description

The M24LR64E-R device is a Dynamic NFC/RFID tag IC with a dual-interface, electrically erasable programmable memory (EEPROM). It features an I^2C interface and can be operated from a V_{CC} power supply. It is also a contactless memory powered by the received carrier electromagnetic wave. The M24LR64E-R is organized as 8192 × 8 bits in the I^2C mode and as 2048 × 32 bits in the ISO 15693 and ISO 18000-3 mode 1 RF mode.

The M24LR64E-R also features an energy harvesting analog output, as well as a user-configurable digital output pin toggling during either RF write in progress or RF busy mode.

Figure 1. Logic diagram



I^2C uses a two-wire serial interface, comprising a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/Write bit ($\overline{RW}$) (as described in *Table 2*), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9^{th} bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

In the ISO15693/ISO18000-3 mode 1 RF mode, the M24LR64E-R is accessed via the 13.56 MHz carrier electromagnetic wave on which incoming data is demodulated from the received signal amplitude modulation (ASK: amplitude shift keying). When connected to an antenna, the operating power is derived from the RF energy and no external power supply is required. The received ASK wave is 10% or 100% modulated with a data rate of 1.6 Kbit/s

using the 1/256 pulse coding mode or a data rate of 26 Kbit/s using the 1/4 pulse coding mode.

Outgoing data is generated by the M24LR64E-R load variation using Manchester coding with one or two subcarrier frequencies at 423 kHz and 484 kHz. Data is transferred from the M24LR64E-R at 6.6 Kbit/s in low data rate mode and 26 Kbit/s in high data rate mode. The M24LR64E-R supports the 53 Kbit/s fast mode in high data rate mode using one subcarrier frequency at 423 kHz.

The M24LR64E-R follows the ISO 15693 and ISO 18000-3 mode 1 recommendation for radio-frequency power and signal interface.

The M24LR64E-R provides an Energy harvesting mode on the analog output pin Vout. When the Energy harvesting mode is activated, the M24LR64E-R can output the excess energy coming from the RF field on the Vout analog pin. In case the RF field strength is insufficient or when Energy harvesting mode is disabled, the analog output pin Vout goes into high-Z state and Energy harvesting mode is automatically stopped.

The M24LR64E-R features a user configurable digital out pin RF WIP/BUSY that can be used to drive a microcontroller interrupt input pin (available only when the M24LR64E-R is correctly powered on the Vcc pin).

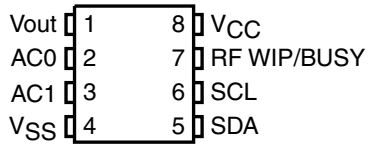
When configured in the RF write in progress mode (RF WIP mode), the RF WIP/BUSY pin is driven low for the entire duration of the RF internal write operation. When configured in the RF busy mode (RF BUSY mode), the RF WIP/BUSY pin is driven low for the entire duration of the RF command progress.

The RF WIP/BUSY pin is an open drain output and must be connected to a pull-up resistor.

Table 1. Signal names

Signal name	Function	Direction
Vout	Energy harvesting Output	Analog output
SDA	Serial Data	I/O
SCL	Serial Clock	Input
AC0, AC1	Antenna coils	I/O
V_{CC}	Supply voltage	-
RF WIP/BUSY	Digital signal	Digital output
V_{SS}	Ground	-

Figure 2. 8-pin package connections



MS19742V1

1. See *Section 30* for package dimensions, and how to identify pin 1.

2 Signal descriptions

2.1 Serial clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (*Figure 3* indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

2.2 Serial data (SDA)

This bidirectional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to V_{CC}. (*Figure 3* indicates how the value of the pull-up resistor can be calculated).

2.3 RF Write in progress / RF Busy (RF WIP/BUSY)

This configurable output signal is used either to indicate that the M24LR64E-R is executing an internal write cycle from the RF channel or that an RF command is in progress. RF WIP and signals are available only when the M24LR64E-R is powered by the Vcc pin. It is an open drain output and a pull-up resistor must be connected from RF WIP/BUSY to V_{CC}.

2.4 Energy harvesting analog output (Vout)

This analog output pin is used to deliver the analog voltage Vout available when the Energy harvesting mode is enabled and the RF field strength is sufficient. When the Energy harvesting mode is disabled or the RF field strength is not sufficient, the energy harvesting analog voltage output Vout is in High-Z state.

2.5 Antenna coil (AC0, AC1)

These inputs are used to connect the device to an external coil exclusively. It is advised not to connect any other DC or AC path to AC0 or AC1.

When correctly tuned, the coil is used to power and access the device using the ISO 15693 and ISO 18000-3 mode 1 protocols.

2.5.1 Device reset in RF mode

To ensure a proper reset of the RF circuitry, the RF field must be turned off (100% modulation) for a minimum t_{RF_OFF} period of time.

2.6 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage and Vout analog output voltage.

2.7 Supply voltage (V_{CC})

This pin can be connected to an external DC supply voltage.

Note: An internal voltage regulator allows the external voltage applied on V_{CC} to supply the M24LR64E-R, while preventing the internal power supply (rectified RF waveforms) to output a DC voltage on the V_{CC} pin.

2.7.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 119*). To maintain a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually around 10 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal I²C write cycle (t_W).

2.7.2 Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}. The V_{CC} rise time must not vary faster than 1V/µs.

2.7.3 Device reset in I²C mode

In order to prevent inadvertent write operations during power-up, a power-on reset (POR) circuit is included. At power-up (continuous rise of V_{CC}), the device does not respond to any I²C instruction until V_{CC} has reached the power-on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 119*). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby power mode. However, the device must not be accessed until V_{CC} has reached a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range.

In a similar way, during power-down (continuous decrease in V_{CC}), as soon as V_{CC} drops below the power-on reset threshold voltage, the device stops responding to any instruction sent to it.

2.7.4 Power-down conditions

During power-down (continuous decay of V_{CC}), the device must be in Standby power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

Figure 3. I^2C Fast mode (f_C = 400 kHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})

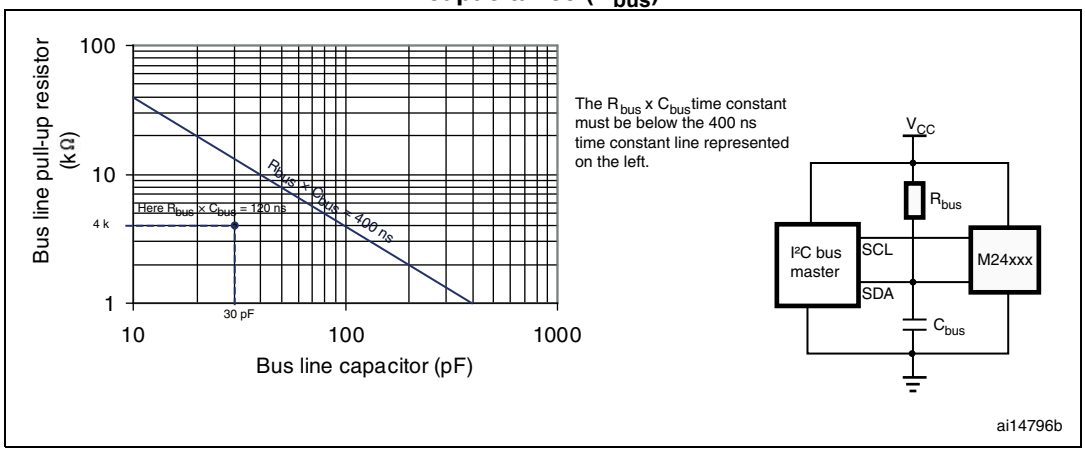


Figure 4. I^2C bus protocol

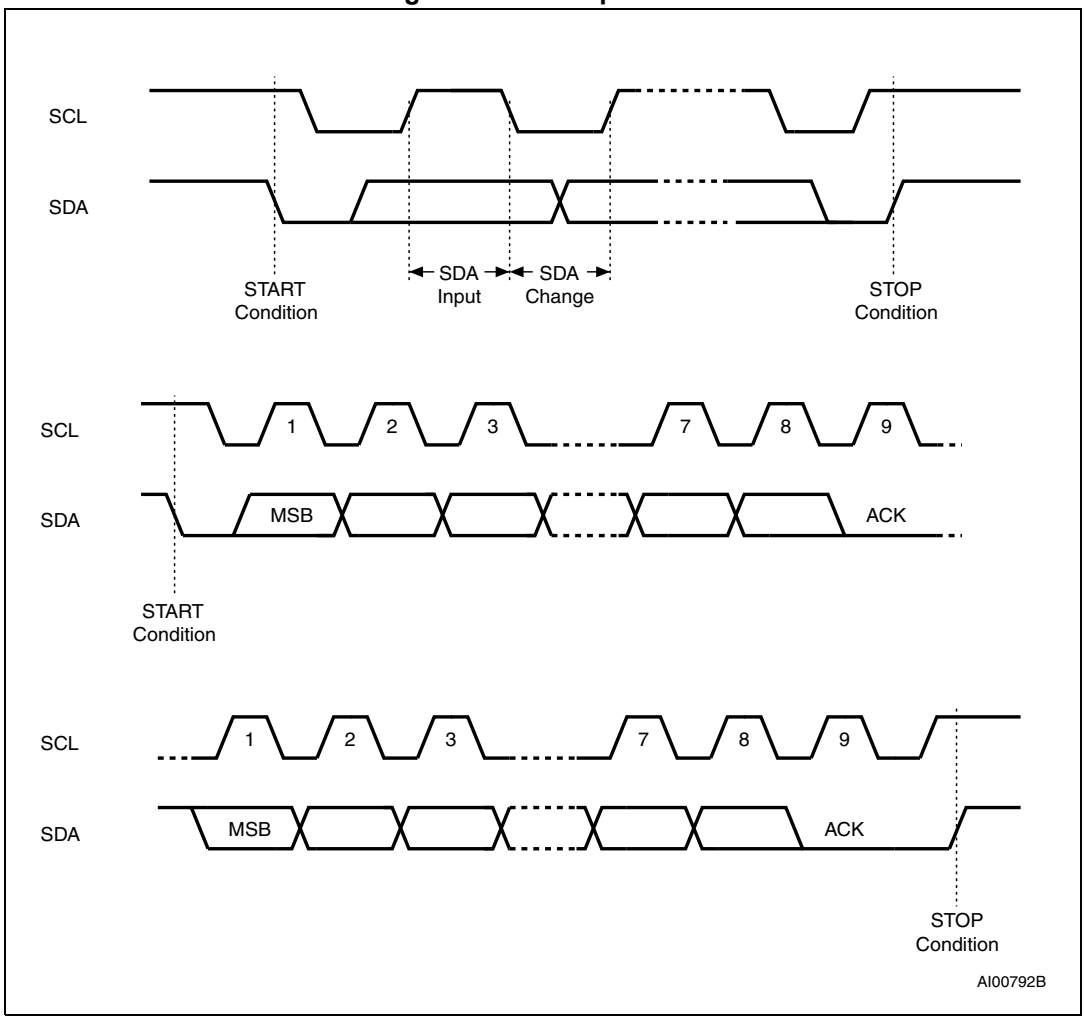


Table 2. Device select code

	Device type identifier(1)				Chip Enable address			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code	1	0	1	0	E2(2)	1	1	RW

1. The most significant bit, b7, is sent first.
2. E2 is not connected to any external pin. It is however used to address the M24LR64E-R as described in *Section 3* and *Section 4*.

Table 3. Address most significant byte

b15	b14	b13	b12	b11	b10	b9	b8

Table 4. Address least significant byte

b7	b6	b5	b4	b3	b2	b1	b0

3 User memory organization

The M24LR64E-R is divided into 64 sectors of 32 blocks of 32 bits, as shown in *Table 5*. *Figure 6* shows the memory sector organization. Each sector can be individually read- and/or write-protected using a specific password command. Read and write operations are possible if the addressed data is not in a protected sector.

The M24LR64E-R also has a 64-bit block that is used to store the 64-bit unique identifier (UID). The UID is compliant with the ISO 15963 description, and its value is used during the anticollision sequence (Inventory). This block is not accessible by the user in RF device operation and its value is written by ST on the production line.

The M24LR64E-R includes an AFI register that stores the application family identifier, and a DSFID register that stores the data storage family identifier used in the anticollision algorithm.

The M24LR64E-R has four 32-bit blocks that store an I^2C password plus three RF password codes.

Figure 5. Circuit diagram

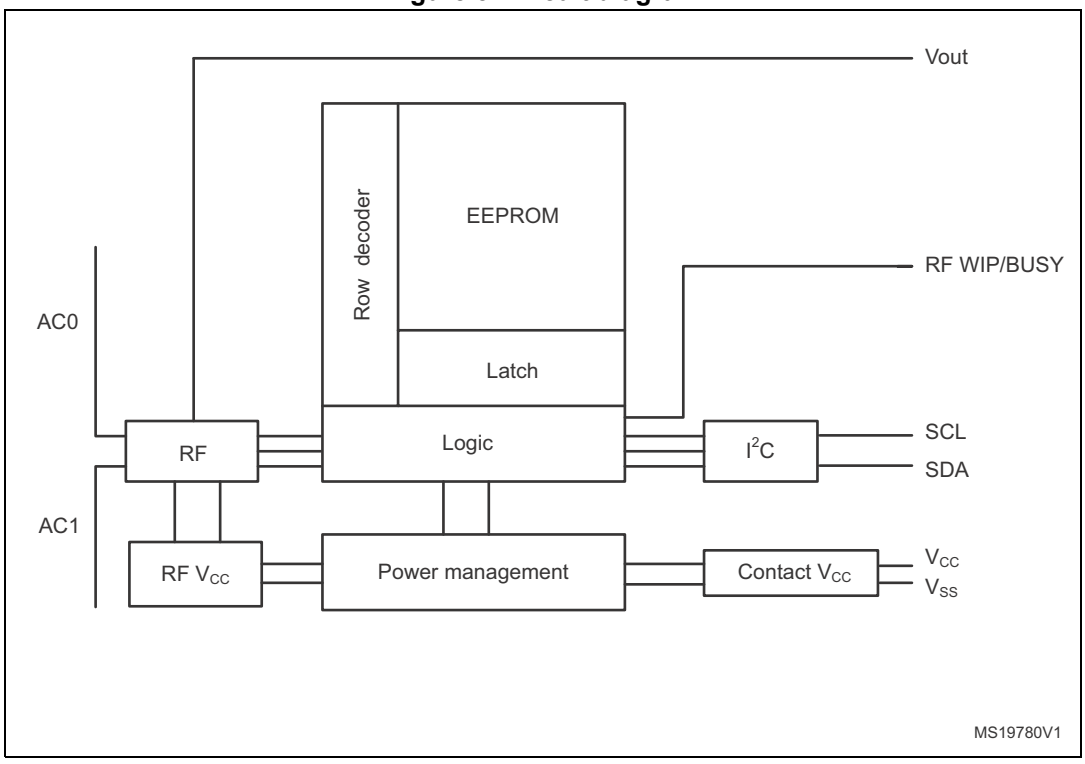
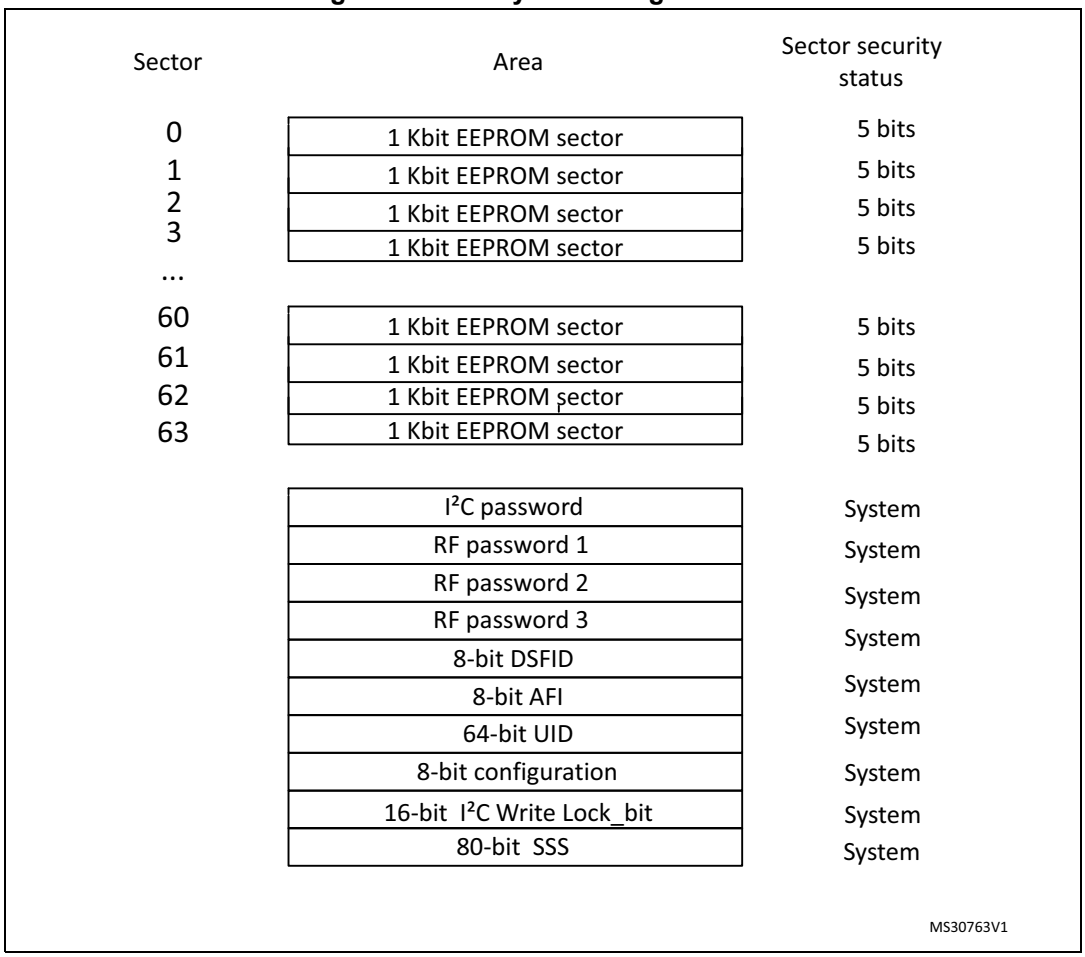


Figure 6. Memory sector organization



Sector details

The M24LR64E-R user memory is divided into 64 sectors. Each sector contains 1024 bits. The protection scheme is described in *Section 4: System memory area*.

In RF mode, a sector provides 32 blocks of 32 bits. Each read and write access is done by block. Read and write block accesses are controlled by a Sector Security Status byte that defines the access rights to the 32 blocks contained in the sector. If the sector is not protected, a Write command updates the complete 32 bits of the selected block.

In I^2C mode, a sector provides 128 bytes that can be individually accessed in Read and Write modes. When protected by the corresponding I2C_Write_Lock bit, the entire sector is write-protected. To access the user memory, the device select code used for any I^2C command must have the E2 Chip Enable address at 0.

Table 5. Sector details

Sector number	RF block address	I^2C byte address	Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
0	0	0	user	user	user	user
	1	4	user	user	user	user
	2	8	user	user	user	user
	3	12	user	user	user	user
	4	16	user	user	user	user
	5	20	user	user	user	user
	6	24	user	user	user	user
	7	28	user	user	user	user
	8	32	user	user	user	user
	9	36	user	user	user	user
	10	40	user	user	user	user
	11	44	user	user	user	user
	12	48	user	user	user	user
	13	52	user	user	user	user
	14	56	user	user	user	user
	15	60	user	user	user	user
	16	64	user	user	user	user
	17	68	user	user	user	user
	18	72	user	user	user	user
	19	76	user	user	user	user
	20	80	user	user	user	user
	21	84	user	user	user	user
	22	88	user	user	user	user
	23	92	user	user	user	user
	24	96	user	user	user	user
	25	100	user	user	user	user
	26	104	user	user	user	user
	27	108	user	user	user	user
	28	112	user	user	user	user
	29	116	user	user	user	user
	30	120	user	user	user	user
	31	124	user	user	user	user

Table 5. Sector details (continued)

Sector number	RF block address	I^2C byte address	Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
1	32	128	user	user	user	user
	33	132	user	user	user	user
	34	136	user	user	user	user
	35	140	user	user	user	user
	36	144	user	user	user	user
	37	148	user	user	user	user
	38	152	user	user	user	user
	39	156	user	user	user	user
	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮

Table 5. Sector details (continued)

Sector number	RF block address	I^2C byte address	Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
63	2016	8064	user	user	user	user
	2017	8068	user	user	user	user
	2018	8072	user	user	user	user
	2019	8076	user	user	user	user
	2020	8080	user	user	user	user
	2021	8084	user	user	user	user
	2022	8088	user	user	user	user
	2023	8092	user	user	user	user
	2024	8096	user	user	user	user
	2025	8100	user	user	user	user
	2026	8104	user	user	user	user
	2027	8108	user	user	user	user
	2028	8112	user	user	user	user
	2029	8116	user	user	user	user
	2030	8120	user	user	user	user
	2031	8124	user	user	user	user
	2032	8128	user	user	user	user
	2033	8132	user	user	user	user
	2034	8136	user	user	user	user
	2035	8140	user	user	user	user
	2036	8144	user	user	user	user
	2037	8148	user	user	user	user
	2038	8152	user	user	user	user
	2039	8156	user	user	user	user
	2040	8160	user	user	user	user
	2041	8164	user	user	user	user
	2042	8168	user	user	user	user
	2043	8172	user	user	user	user
	2044	8176	user	user	user	user
	2045	8180	user	user	user	user
	2046	8184	user	user	user	user
	2047	8188	user	user	user	user

4 System memory area

4.1 M24LR64E-R block security in RF mode

The M24LR64E-R provides a special protection mechanism based on passwords. In RF mode, each memory sector of the M24LR64E-R can be individually protected by one out of three available passwords, and each sector can also have Read/Write access conditions set.

Each memory sector of the M24LR64E-R is assigned with a Sector security status byte including a Sector Lock bit, two Password Control bits and two Read/Write protection bits, as shown in *Table 7*.

Table 6 describes the organization of the Sector security status byte, which can be read using the Read Single Block and Read Multiple Block commands with the Option_flag set to 1.

On delivery, the default value of the SSS bytes is set to 00h.

Table 6. Sector security status byte area

I^2C byte address		Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
E2 = 1	0	SSS 3	SSS 2	SSS 1	SSS 0
E2 = 1	4	SSS 7	SSS 6	SSS 5	SSS 4
E2 = 1	8	SSS 11	SSS 10	SSS 9	SSS 8
E2 = 1	12	SSS 15	SSS 14	SSS 13	SSS 12
E2 = 1	16	SSS 19	SSS 18	SSS 17	SSS 16
E2 = 1	20	SSS 23	SSS 22	SSS 21	SSS 20
E2 = 1	24	SSS 27	SSS 26	SSS 25	SSS 24
E2 = 1	28	SSS 31	SSS 30	SSS 29	SSS 28
E2 = 1	32	SSS 35	SSS 34	SSS 33	SSS 32
E2 = 1	36	SSS 39	SSS 38	SSS 37	SSS 36
E2 = 1	40	SSS 43	SSS 42	SSS 41	SSS 40
E2 = 1	44	SSS 47	SSS 46	SSS 45	SSS 44
E2 = 1	48	SSS 51	SSS 50	SSS 49	SSS 48
E2 = 1	52	SSS 55	SSS 54	SSS 53	SSS 52
E2 = 1	56	SSS 59	SSS 58	SSS 57	SSS 56
E2 = 1	60	SSS 63	SSS 62	SSS 61	SSS 60

Table 7. Sector security status byte organization

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	0	0	Password control bits		Read / Write protection bits		Sector Lock

When the Sector Lock bit is set to 1, for instance by issuing a Lock-sector command, the two Read/Write protection bits (b_1, b_2) are used to set the Read/Write access of the sector as described in *Table 8*.

Table 8. Read/Write protection bit setting

Sector Lock	b_2, b_1	Sector access when password presented		Sector access when password not presented	
0	xx	Read	Write	Read	Write
1	00	Read	Write	Read	No Write
1	01	Read	Write	Read	Write
1	10	Read	Write	No Read	No Write
1	11	Read	No Write	No Read	No Write

The next two bits of the Sector security status byte (b_3, b_4) are the password control bits. The value of these two bits is used to link a password to the sector, as defined in *Table 9*.

Table 9. Password control bits

b_4, b_3	Password
00	The sector is not protected by a password.
01	The sector is protected by password 1.
10	The sector is protected by password 2.
11	The sector is protected by password 3.

The M24LR64E-R password protection is organized around a dedicated set of commands, plus a system area of three password blocks where the password values are stored. This system area is described in *Table 10*.

Table 10. Password system area

Add	Password
1	Password 1
2	Password 2
3	Password 3

The dedicated commands for protection in RF mode are:

- Write-sector password:

  The Write-sector password command is used to write a 32-bit block into the password system area. This command must be used to update password values. After the write cycle, the new password value is automatically activated. It is possible to modify a password value after issuing a valid Present-sector password command. On delivery, the three default password values are set to 0000 0000h and are activated.

- Lock-sector:

  The Lock-sector command is used to set the sector security status byte of the selected sector. Bits b_4 to b_1 of the sector security status byte are affected by the Lock-sector

command. The sector lock bit, b_0, is set to 1 automatically. After issuing a Lock-sector command, the protection settings of the selected sector are activated. The protection of a locked block cannot be changed in RF mode. A Lock-sector command sent to a locked sector returns an error code.

- Present-sector password:

  The Present-sector password command is used to present one of the three passwords to the M24LR64E-R in order to modify the access rights of all the memory sectors linked to that password (*Table 8*) including the password itself. If the presented password is correct, the access rights remain activated until the tag is powered off or until a new Present-sector password command is issued. If the presented password value is not correct, all the access rights of all the memory sectors are deactivated.

- Sector security status byte area access conditions in I^2C mode:

  In I^2C mode, read access to the sector security status byte area is always allowed. Write access depends on the correct presentation of the I^2C password (see *Section 5.16.1: I2C present password command description*).

  To access the Sector security status byte area, the device select code used for any I^2C command must have the E2 Chip Enable address at 1.

  An I^2C write access to a sector security status byte re-initializes the RF access condition to the given memory sector.

4.1.1 Example of the M24LR64E-R security protection in RF mode

Table 11 and *Table 12* show the sector security protections before and after a valid Present-sector password command. *Table 11* shows the sector access rights of an M24LR64E-R after power-up. After a valid Present-sector password command with password 1, the memory sector access is changed as shown in *Table 12*.

Table 11. M24LR64E-R sector security protection after power-up

Sector address	Sector features			Sector security status byte					
				$b_7b_6b_5$	b_4	b_3	b_2	b_1	b_0
0	Protection: standard	Read	No Write	xxx	0	0	0	0	1
1	Protection: pswd 1	Read	No Write	xxx	0	1	0	0	1
2	Protection: pswd 1	Read	Write	xxx	0	1	0	1	1
3	Protection: pswd 1	No Read	No Write	xxx	0	1	1	0	1
4	Protection: pswd 1	No Read	No Write	xxx	0	1	1	1	1

Table 12. M24LR64E-R sector security protection after a valid presentation of password 1

Sector address	Sector features			Sector security status byte					
				$b_7b_6b_5$	b_4	b_3	b_2	b_1	b_0
0	Protection: standard	Read	No Write	xxx	0	0	0	0	1
1	Protection: pswd 1	Read	Write	xxx	0	1	0	0	1
2	Protection: pswd 1	Read	Write	xxx	0	1	0	1	1

Table 12. M24LR64E-R sector security protection after a valid presentation of password 1 (continued)

Sector address	Sector features			Sector security status byte					
				$b_7b_6b_5$	b_4	b_3	b_2	b_1	b_0
3	Protection: pswd 1	Read	Write	xxx	0	1	1	0	1
4	Protection: pswd 1	Read	No Write	xxx	0	1	1	1	1

4.2 M24LR64E-R block security in I²C mode (I2C_Write_Lock bit area)

In the I²C mode only, it is possible to protect individual sectors against Write operations. This feature is controlled by the I2C_Write_Lock bits stored in the 8 bytes of the I2C_Write_Lock bit area. I2C_Write_Lock bit area starts from location 8192 (see *Table 13*). To access the I2C_Write_Lock bit area, the device select code used for any I²C command must have the E2 Chip Enable address at 1.

Using these 16 bits, it is possible to write-protect all the 64 sectors of the M24LR64E-R memory. Each bit controls the I²C write access to a specific sector as shown in *Table 13*. It is always possible to unprotect a sector in the I²C mode. When an I2C_Write_Lock bit is reset to 0, the corresponding sector is unprotected. When the bit is set to 1, the corresponding sector is write-protected.

In I²C mode, read access to the I2C_Write_Lock bit area is always allowed. Write access depends on the correct presentation of the I²C password.

On delivery, the default value of the eight bytes of the I2C_Write_Lock bit area is reset to 00h.

Table 13. I2C_Write_Lock bit

I²C byte address		Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
E2 = 1	2048	sectors 31-24	sectors 23-16	sectors 15-8	sectors 7-0
E2 = 1	2052	sectors 63-56	sectors 55-48	sectors 47-40	sectors 39-32

4.3 Configuration byte and Control register

The M24LR64E-R offers an 8-bit non-volatile Configuration byte located at I²C location 2320 of the system area used to store the RF WIP/BUSY pin and the energy harvesting configuration (see *Table 14*).

The M24LR64E-R also offers an 8-bit volatile Control register located at I²C location 2336 of the system area used to store the energy harvesting enable bit as well as a FIELD_ON bit indicator (see *Table 15*).

4.3.1 RF WIP/BUSY pin configuration

The M24LR64E-R features a configurable open drain output RF WIP/BUSY pin used to provide RF activity information to an external device.

The RF WIP/BUSY pin functionality depends on the value of bit 3 of the Configuration byte.

- **RF busy mode**

When bit 3 of the Configuration byte is set to 0, the RF WIP/BUSY pin is configured in RF busy mode.

The purpose of this mode is to indicate to the I²C bus master whether the M24LR64E-R is busy in RF mode or not.

In this mode, the RF WIP/BUSY pin is tied to 0 from the RF command Start Of Frame (SOF) until the end of the command execution.

If a bad RF command is received, the RF WIP/BUSY pin is tied to 0 from the RF command SOF until the reception of the RF command CRC. Otherwise, the RF WIP/BUSY pin is in high-Z state.

When tied to 0, the RF WIP/BUSY signal returns to High-Z state if the RF field is cut-off.

During the execution of I²C commands, the RF WIP/BUSY pin remains in high-Z state.

- **RF Write in progress**

When bit 3 of the Configuration byte is set to 1, the RF WIP/BUSY pin is configured in RF Write in progress mode.

The purpose of this mode is to indicate to the I²C bus master that some data has been changed in RF mode.

In this mode, the RF WIP/BUSY pin is tied to 0 for the duration of an internal write operation (i.e. between the end of a valid RF write command and the beginning of the RF answer).

During the execution of I²C write operations, the RF WIP/BUSY pin remains in high-Z state.

4.3.2 Energy harvesting configuration

The M24LR64E-R features an Energy harvesting mode on the Vout analog output.

The general purpose of the Energy harvesting mode is to deliver a part of the non-necessary RF power received by the M24LR64E-R on the AC0-AC1 RF input in order to supply an external device. The current consumption on the analog voltage output Vout is limited to ensure that the M24LR64E-R is correctly supplied during the powering of the external device.

When the Energy harvesting mode is enabled and the power delivered on the AC0-AC1 RF input exceeds the minimum required $P_{AC0\text{-}AC1\_min}$, the M24LR64E-R is able to deliver a limited and unregulated voltage on the Vout pin, assuming the current consumption on the Vout does not exceed the I_{sink_max} maximum value.

If one of the conditions above is not met, the analog voltage output pin Vout is set in High-Z state.

For robust applications using the Energy harvesting mode, four current fan-out levels can be chosen.

- **Vout sink current configuration**

The sink current level is chosen by programming EH_cfg1 and EH_cfg0 into the Configuration byte (see *Table 14*).

The minimum power level required on AC0-AC1 RF input $P_{AC0\text{-}AC1\_min}$, the delivered voltage Vout, as well as the maximum current consumption I_{sink_max} on the Vout pin corresponding to the <EH_cfg1,EH_cfg0> bit values are described in *Table 126*.

Table 14. Configuration byte

I²C byte address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	BIT 1	BIT 0
E2=1	2320	X(1)	X(1)	X(1)	X(1)	RF WIP/BUSY	EH_mode	EH_cfg1	EH_cfg0

1. Bit 7 to bit 4 are don't care bits.

- **Energy harvesting enable control**

Delivery of Energy harvesting analog output voltage on the Vout pin depends on the value of the EH_enable bit of the volatile Control register (see *Table 15*).

Table 15. Control register

I²C byte address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	BIT 1	BIT 0
E2=1	2336	T-Prog(1)	0(1)	0(1)	0(1)	0(1)	0(1)	FIELD_ON(1)	EH_enable

1. Bit 7 to bit 1 are read-only bits.

  - When set to 1, the EH_enable bit enables the Energy harvesting mode, meaning that the Vout analog output signal is delivered when the $P_{AC0\text{-}AC1\_min}$ and I_{sink_max} conditions corresponding to the chosen sink current configuration bit are met (see *Table 126*).
  - When set to 0, the EH_enable bit disables the Energy harvesting mode and the analog output Vout remains in High-Z state.
  - The T_Prog flag indicates a correct duration of the I²C write time (tw). This bit is reset to 0 after POR and at the beginning of each writing cycle; it is set to 1 only after a correct completion of the writing cycle.

- **Energy harvesting default mode control**

At power-up, in I²C or RF mode, the EH_enable bit is updated according to the value of the EH_mode bit stored in the non-volatile Configuration byte (see *Table 16*). In other words, the EH_mode bit is used to configure whether the Energy harvesting mode is enabled or not by default.

Table 16. EH_enable bit value after power-up

EH_mode value	EH_enable after power-up	Energy harvesting after power-up
0	1	enabled
1	0	disabled

4.3.3 FIELD_ON indicator bit

The FIELD_ON indicator bit located as bit 1 of the Control register is a read-only bit used to indicate when the RF power level delivered to the M24LR64E-R is sufficient to execute RF commands.

- When FIELD_ON = 0, the M24LR64E-R is not able to execute any RF commands.
- When FIELD_ON =1, the M24LR64E-R is able to execute any RF commands.

Note: During read access to the Control register in RF mode, the FIELD_ON bit is always read at 1.

4.3.4 Configuration byte access in I²C and RF modes

In I²C mode, read and write accesses to the non-volatile Configuration byte are always allowed. To access the Configuration byte, the device select code used for any I²C command must have the E2 Chip enable address at 1.

The dedicated commands to access the Configuration byte in RF mode are:

- Read configuration byte command (ReadCfg):
  - The ReadCfg command is used to read the eight bits of the Configuration byte.
- Write energy harvesting configuration command (WriteEHCfg):
  - The WriteEHCfg command is used to write the EH_mode, EH_cfg1 and EH_cfg0 bits into the Configuration byte.
- Write RF WIP/BUSY pin configuration command (WriteDOCfg):
  - The WriteDOCfg command is used to write the RF WIP/BUSY bit into the Configuration byte.

After any write access to the Configuration byte, the new configuration is automatically applied.

4.3.5 Control register access in I²C or RF mode

In I²C mode, read and write accesses to the volatile Control register are always allowed. To access the Control register, the device select code used for any I²C command must have the E2 Chip enable address at 1.

The dedicated commands to access the Control register in RF mode are:

- Check energy harvesting enable bit command (CheckEHEn):
  - The CheckEHEn command is used to read the eight bits of the Control register. When it is run, the FIELD_ON bit is always read at 1.
- Set/reset energy harvesting enable bit command (SetRstEHEn):
  - The SetRstEHEn command is used to set or reset the value of the EH_enable bit into the Control register.

4.4 ISO 15693 system parameters

The M24LR64E-R provides the system area required by the ISO 15693 RF protocol, as shown in *Table 17*.

The first 32-bit block starting from I^2C address 2304 stores the I^2C password. This password is used to activate/deactivate the write protection of the protected sector in I^2C

mode. At power-on, all user memory sectors protected by the I2C_Write_Lock bits can be read but cannot be modified. To remove the write protection, it is necessary to use the I^2C present password described in *Figure 12*. When the password is correctly presented — that is, when all the presented bits correspond to the stored ones — it is also possible to modify the I^2C password using the I^2C write password command described in *Figure 13*.

The next three 32-bit blocks store the three RF passwords. These passwords are neither read- nor write- accessible in the I^2C mode.

The next byte stores the Configuration byte, at I²C location 2320. This Control register is used to store the three energy harvesting configuration bits and the RF WIP/BUSY configuration bit.

The next two bytes are used to store the AFI, at I^2C location 2322, and the DSFID, at I^2C location 2323. These two values are used during the RF inventory sequence. They are read-only in the I^2C mode.

The next eight bytes, starting from location 2324, store the 64-bit UID programmed by ST on the production line. Bytes at I^2C locations 2332 to 2335 store the IC Ref and the Mem_Size data used by the RF Get_System_Info command. The UID, Mem_Size and IC ref values are read-only data.

Table 17. System parameter sector

I^2C byte address		Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
E2 = 1	2304	I^2C password(1)			
E2 = 1	2308	RF password 1(1)			
E2 = 1	2312	RF password 2(1)			
E2 = 1	2316	RF password 3(1)			
E2 = 1	2320	DSFID (FFh)	AFI (00h)	ST reserved (Exh)(2)	Configuration byte (F4h)
E2 = 1	2324	UID	UID	UID	UID
E2 = 1	2328	UID (E0h)	UID (02h)	UID	UID
E2 = 1	2332	Mem_Size (03 07FFh)			IC Ref (5Eh)
E2 = 1	2336	-	-	-	Prog. completion and Energy harvesting status(3)

1. Delivery state: I^2C password = 0000 0000h, RF password = 0000 0000h, Configuration byte = F4h
2. The product revision is the Most significant nibble of the byte located at address 0x911 (2321 d) in the system area (Device select code E2 =1). From DS rev4, the product revision value is 0xE. The Least significant nibble is ST reserved.
3. Address system 2336 (920h, E2=1) is the control register.
   Bit 7 is T_Prog (refer to *Table 15: Control register*). When accessed in RF, this bit is not significant and set to 0.
   Bits 2-6 are RFU and set to 0.
   Bit 1 is FIELD_ON (refer to *Table 15: Control register*).
   Bit 0 is EH_enable (refer to *Table 15: Control register*).

5 I²C device operation

The device supports the I²C protocol. This is summarized in *Figure 4*. Any device that sends data to the bus is defined as a transmitter, and any device that reads data is defined as a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which also provides the serial clock for synchronization. The M24LR64E-R device is a slave in all communications.

5.1 Start condition

Start is identified by a falling edge of serial data (SDA) while the serial clock (SCL) is stable in the high state. A Start condition must precede any data transfer command. The device continuously monitors (except during a write cycle) the SDA and the SCL for a Start condition, and does not respond unless one is given.

5.2 Stop condition

Stop is identified by a rising edge of serial data (SDA) while the serial clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode. A Stop condition at the end of a Write command triggers the internal write cycle.

5.3 Acknowledge bit (Ack)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether a bus master or a slave device, releases the serial data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls the SDA low to acknowledge the receipt of the eight data bits.

5.4 Data input

During data input, the device samples serial data (SDA) on the rising edge of the serial clock (SCL). For correct device operation, the SDA must be stable during the rising edge of the SCL, and the SDA signal must change *only* when the SCL is driven low.

5.5 I²C timeout

During the execution of an I²C operation, RF communications are not possible.

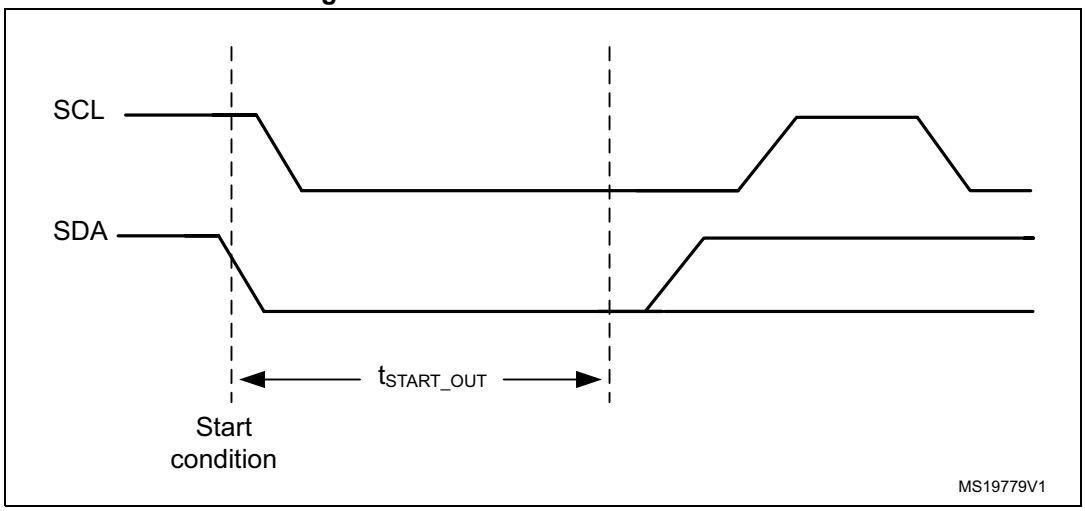
To prevent RF communication freezing due to inadvertent unterminated instructions sent to the I²C bus, the M24LR64E-R features a timeout mechanism that automatically resets the I²C logic block.

5.5.1 I²C timeout on Start condition

I²C communication with the M24LR64E-R starts with a valid Start condition, followed by a device select code.

If the delay between the Start condition and the following rising edge of the Serial Clock (SCL) that samples the most significant of the Device Select exceeds the t_{START_OUT} time (see *Table 123*), the I²C logic block is reset and further incoming data transfer is ignored until the next valid Start condition.

Figure 7. I²C timeout on Start condition



5.5.2 I²C timeout on clock period

During data transfer on the I²C bus, if the serial clock pulse width high (t_{CHCL}) or serial clock pulse width low (t_{CLCH}) exceeds the maximum value specified in *Table 123*, the I²C logic block is reset and any further incoming data transfer is ignored until the next valid Start condition.

5.6 Memory addressing

To start a communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 2* (on Serial Data (SDA), the most significant bit first).

The device select code consists of a 4-bit device type identifier and a 3-bit Chip Enable “Address” (E2,1,1). To address the memory array, the 4-bit device type identifier is 1010b. Refer to *Table 2*.

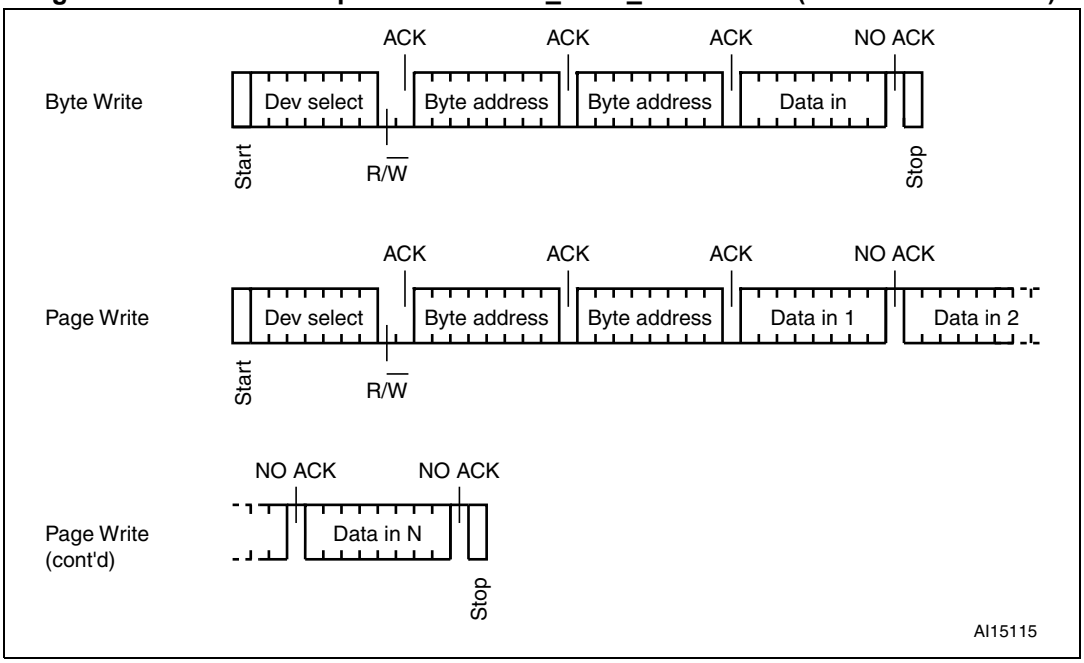
The eighth bit is the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$). It is set to 1 for Read and to 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on serial data (SDA) during the ninth bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

Table 18. Operating modes

Mode	RW bit	Bytes	Initial sequence
Current address read	1	1	Start, device select, RW = 1
Random address read	0	1	Start, device select, RW = 0, address
	1		reStart, device select, RW = 1
Sequential read	1	≥ 1	Similar to current or random address read
Byte write	0	1	Start, device select, RW = 0
Page write	0	≤ 4 bytes	Start, device select, RW = 0

Figure 8. Write mode sequences with I2C_Write_Lock bit = 1 (data write inhibited)



5.7 Write operations

Following a Start condition, the bus master sends a device select code with the Read/Write bit (RW) reset to 0. The device acknowledges this, as shown in *Figure 8*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Writing to the memory may be inhibited if the I2C_Write_Lock bit = 1. A Write instruction issued with the I2C_Write_Lock bit = 1 and with no I2C_Password presented does not modify the memory contents, and the accompanying data bytes are *not* acknowledged, as shown in *Figure 8*.

Each data byte in the memory has a 16-bit (two-byte wide) address. The most significant byte (*Table 3*) is sent first, followed by the least significant byte (*Table 4*). Bits b15 to b0 form the address of the byte in memory.

When the bus master generates a Stop condition immediately after the Ack bit (in the tenth-bit time slot), either at the end of a byte write or a page write, the internal write cycle is triggered. A Stop condition at any other time slot does not trigger the internal write cycle.

After the Stop condition, the delay t_W, and the successful completion of a Write operation, the device's internal address counter is incremented automatically, to point to the next byte address after the last one that was modified.

During the internal write cycle, the serial data (SDA) signal is disabled internally, and the device does not respond to any requests.

5.8 Byte write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is write-protected by the I2C_Write_Lock bit (= 1), the device replies with NoAck, and the location is not modified. If the addressed location is not write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 9*.

5.9 Page write

The Page write mode allows up to four bytes to be written in a single write cycle, provided that they are all located in the same "row" in the memory: that is, the most significant memory address bits (b12-b2) are the same. If more bytes are sent than fit up to the end of the row, a condition known as "roll-over" occurs. This should be avoided, as data starts to become overwritten in an implementation-dependent way.

The bus master sends from one to four bytes of data, each of which is acknowledged by the device if the I2C_Write_Lock bit = 0 or the I2C_Password was correctly presented. If the I2C_Write_Lock_bit = 1 and the I2C_password are not presented, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (inside the page) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 9. Write mode sequences with I2C_Write_Lock bit = 0 (data write enabled)

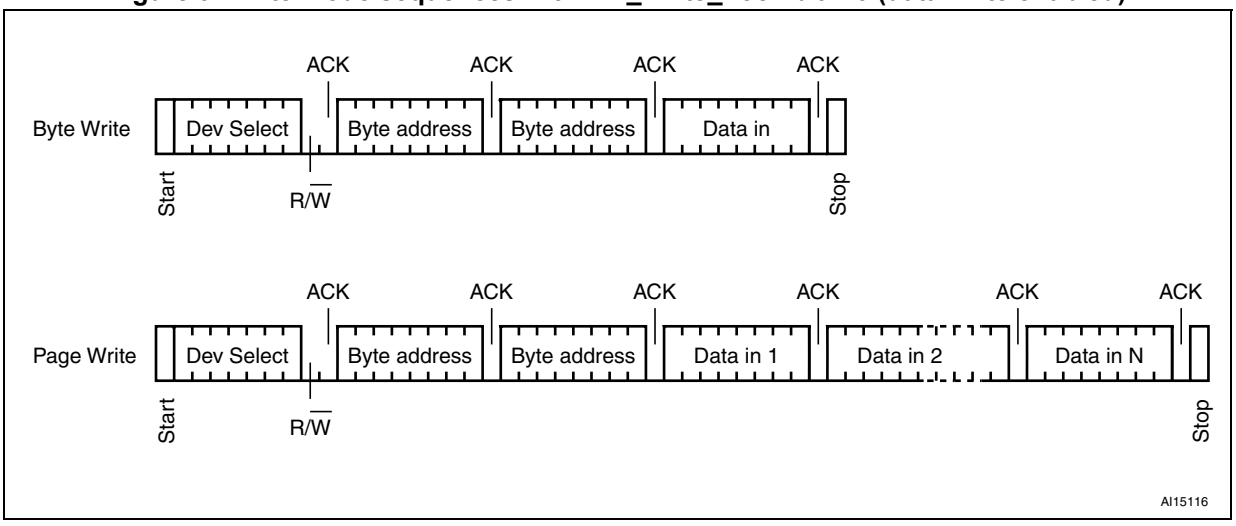
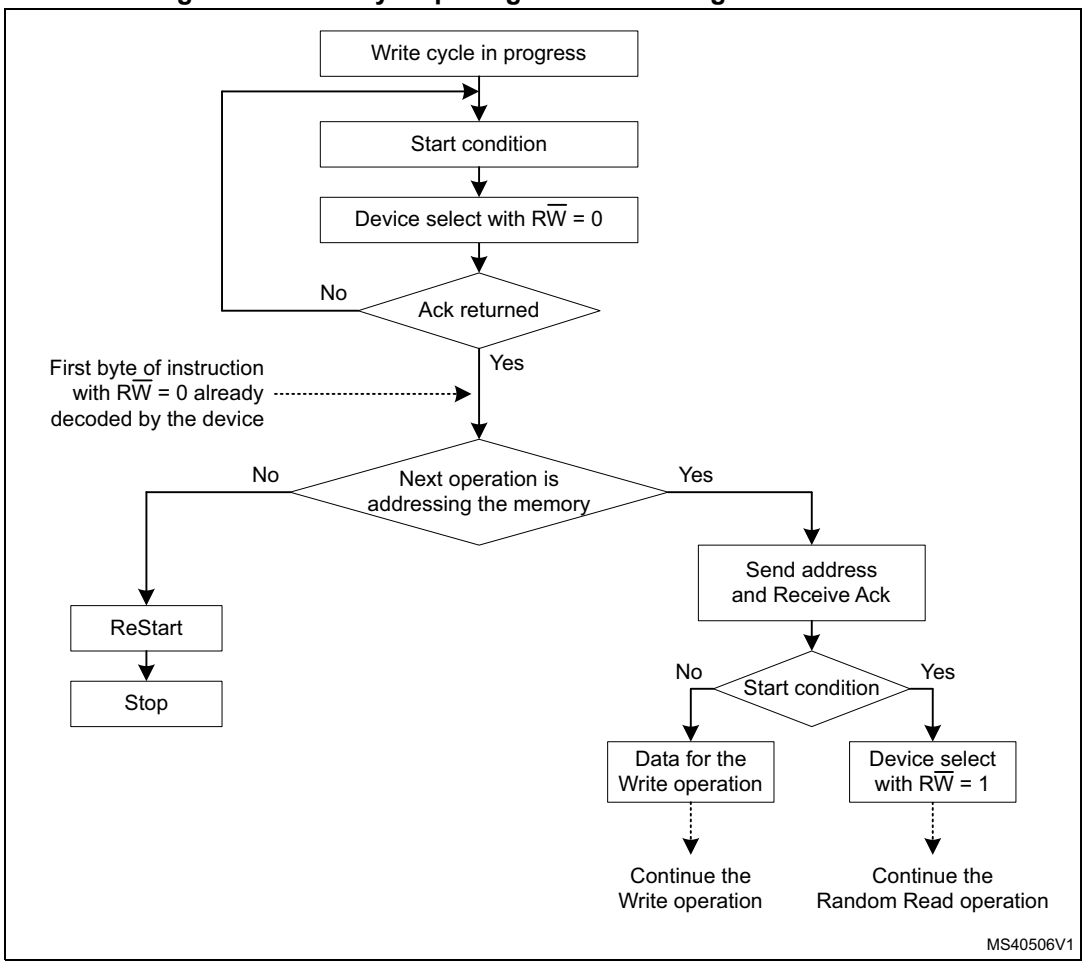


Figure 10. Write cycle polling flowchart using Ack



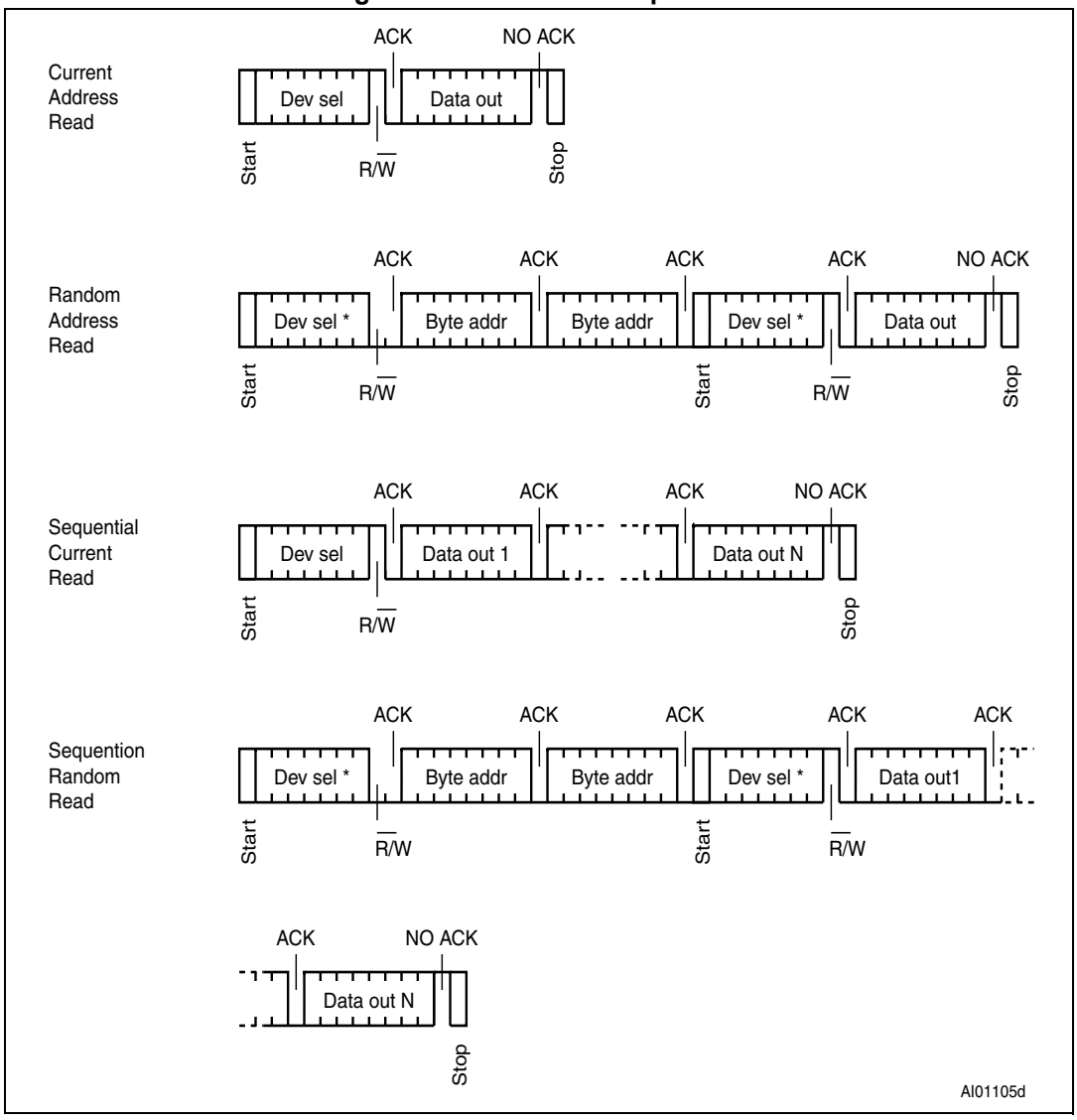
5.10 Minimizing system delays by polling on Ack

During the internal write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum I²C write time (t_w) is shown in *Table 123*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 10*, is:

1. Initial condition: a write cycle is in progress.
2. Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
3. Step 2: if the device is busy with the internal write cycle, no Ack is returned and the bus master goes back to Step 1. If the device has terminated the internal write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 11. Read mode sequences



1. The seven most significant bits of the device select code of a random read (in the first and fourth bytes) must be identical.

5.11 Read operations

Read operations are performed independently of the state of the I2C_Write_Lock bit.

After the successful completion of a read operation, the device's internal address counter is incremented by one, to point to the next byte address.

5.12 Random Address Read

A dummy write is first performed to load the address into this address counter (as shown in *Figure 11*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the Read/Write bit (RW) set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

5.13 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the Read/Write bit (RW) set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 11*, *without* acknowledging the byte.

5.14 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 11*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter "rolls over", and the device continues to output data from memory address 00h.

5.15 Acknowledge in Read mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the ninth bit time. If the bus master does not drive Serial Data (SDA) low during this time, the device terminates the data transfer and switches to its Standby mode.

5.16 M24LR64E-R I²C password security

The M24LR64E-R controls I²C sector write access using the 32-bit-long I²C password and the 64-bit I2C_Write_Lock bit area. The I²C password value is managed using two I²C commands: I²C present password and I²C write password.

5.16.1 I²C present password command description

The I²C present password command is used in I²C mode to present the password to the M24LR64E-R in order to modify the write access rights of all the memory sectors protected by the I2C_Write_Lock bits, including the password itself. If the presented password is correct, the access rights remain activated until the M24LR64E-R is powered off or until a new I²C present password command is issued.

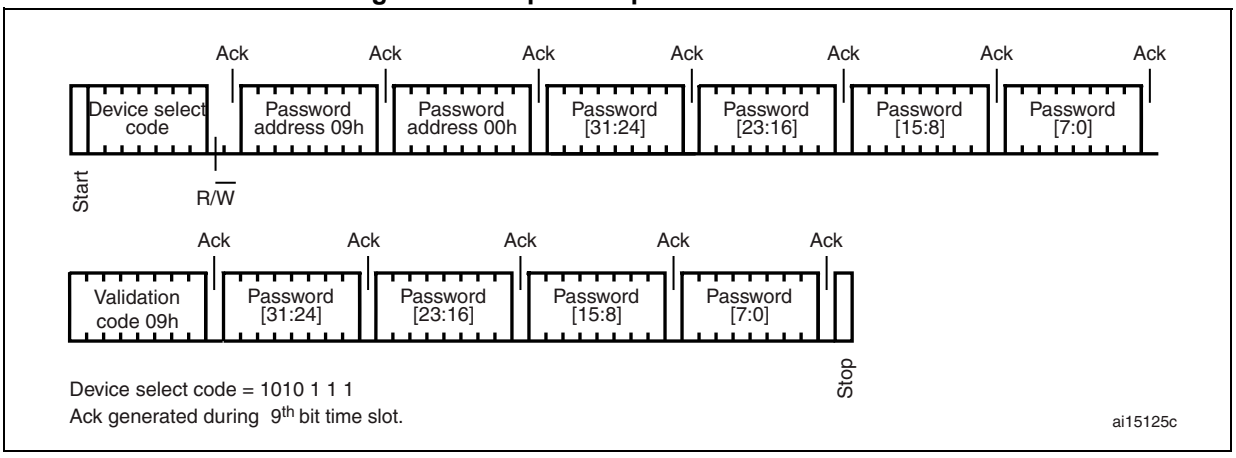
Following a Start condition, the bus master sends a device select code with the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$) reset to 0 and the Chip Enable bit E2 at 1. The device acknowledges this, as shown in *Figure 12*, and waits for two I²C password address bytes, 09h and 00h. The device responds to each address byte with an acknowledge bit, and then waits for the four password data bytes, the validation code, 09h, and a resend of the four password data bytes. The most significant byte of the password is sent first, followed by the least significant bytes.

It is necessary to send the 32-bit password twice to prevent any data corruption during the sequence. If the two 32-bit passwords sent are not exactly the same, the M24LR64E-R does not start the internal comparison.

When the bus master generates a Stop condition immediately after the Ack bit (during the tenth bit time slot), an internal delay equivalent to the write cycle time is triggered. A Stop condition at any other time does not trigger the internal delay. During that delay, the M24LR64E-R compares the 32 received data bits with the 32 bits of the stored I²C password. If the values match, the write access rights to all protected sectors are modified after the internal delay. If the values do not match, the protected sectors remain protected.

During the internal delay, the serial data (SDA) signal is disabled internally, and the device does not respond to any requests.

Figure 12. I²C present password command



5.16.2 I²C write password command description

The I²C write password command is used to write a 32-bit block into the M24LR64E-R I²C password system area. This command is used in I²C mode to update the I²C password value. It cannot be used to update any of the RF passwords. After the write cycle, the new I²C password value is automatically activated. The I²C password value can only be modified after issuing a valid I²C present password command.

On delivery, the I²C default password value is set to 0000 0000h and is activated.

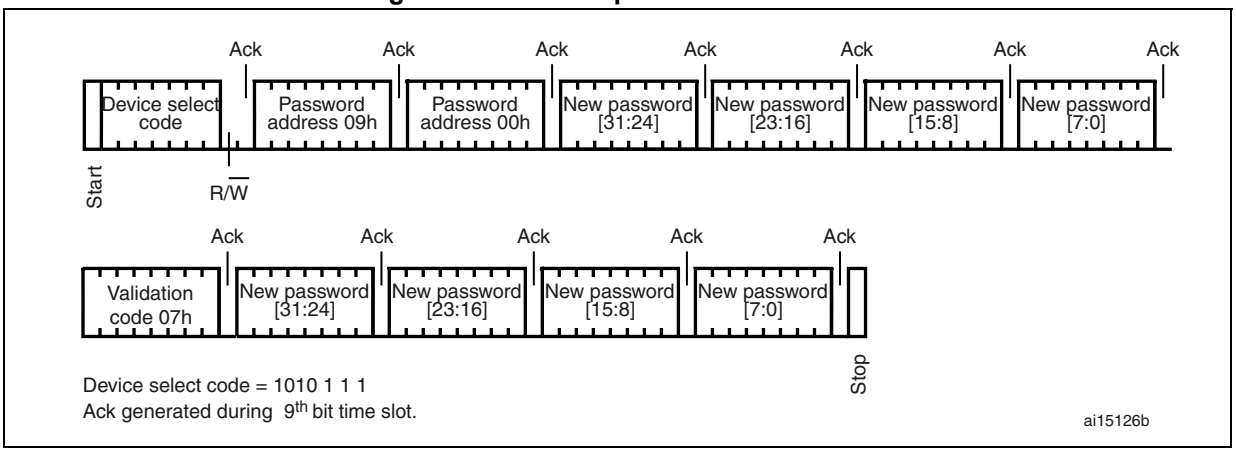
Following a Start condition, the bus master sends a device select code with the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$) reset to 0 and the Chip Enable bit E2 at 1. The device acknowledges this, as shown in *Figure 13*, and waits for the two I²C password address bytes, 09h and 00h. The device responds to each address byte with an acknowledge bit, and then waits for the four password data bytes, the validation code, 07h, and a resend of the four password data bytes. The most significant byte of the password is sent first, followed by the least significant bytes.

It is necessary to send twice the 32-bit password to prevent any data corruption during the write sequence. If the two 32-bit passwords sent are not exactly the same, the M24LR64E-R does not modify the I²C password value.

When the bus master generates a Stop condition immediately after the Ack bit (during the tenth bit time slot), the internal write cycle is triggered. A Stop condition at any other time does not trigger the internal write cycle.

During the internal write cycle, the serial data (SDA) signal is disabled internally, and the device does not respond to any requests.

Figure 13. I²C write password command



6 M24LR64E-R memory initial state

The device is delivered with all bits in the user memory array set to 1 (each byte contains FFh).

The DSFID is programmed to FFh and the AFI is programmed to 00h.

Configuration byte set to F4h:

- Bit 7 to bit 4: all set to 1
- Bit 3: set to 0 (RF BUSY mode on RF WIP/BUSY pin)
- Bit 2: set to 1 (Energy harvesting not activated by default)
- Bit 1 and bit 0: set to 0

7 RF device operation

The M24LR64E-R is divided into 64 sectors of 32 blocks of 32 bits, as shown in *Table 5*. Each sector can be individually read- and/or write-protected using a specific lock or password command.

Read and Write operations are possible if the addressed block is not protected. During a Write, the 32 bits of the block are replaced by the new 32-bit value.

The M24LR64E-R also has a 64-bit block that is used to store the 64-bit unique identifier (UID). The UID is compliant with the ISO 15963 description, and its value is used during the anticollision sequence (Inventory). This block is not accessible by the user in RF device operation and its value is written by ST on the production line.

The M24LR64E-R also includes an AFI register in which the application family identifier is stored, and a DSFID register in which the data storage family identifier used in the anticollision algorithm is stored.

The M24LR64E-R has three 32-bit blocks in which the password codes are stored and an 8-bit Configuration byte in which the Energy harvesting mode and RF WIP/BUSY pin configuration is stored.

7.1 RF communication and energy harvesting

As the current consumption can affect the AC signal delivered by the antenna, RF communications with M24LR64E-R are not guaranteed during voltage delivery on the energy harvesting analog output Vout.

RF communication can disturb and possibly stop Energy Harvesting mode.

7.2 Commands

The M24LR64E-R supports the following commands:

- ***Inventory***, used to perform the anticollision sequence.
- ***Stay quiet***, used to put the M24LR64E-R in quiet mode, where it does not respond to any inventory command.
- ***Select***, used to select the M24LR64E-R. After this command, the M24LR64E-R processes all Read/Write commands with Select_flag set.
- ***Reset to ready***, used to put the M24LR64E-R in the ready state.
- ***Read block***, used to output the 32 bits of the selected block and its locking status.
- ***Write block***, used to write the 32-bit value in the selected block, provided that it is not locked.
- ***Read multiple blocks***, used to read the selected blocks and send back their value.
- ***Write AFI***, used to write the 8-bit value in the AFI register.
- ***Lock AFI***, used to lock the AFI register.
- ***Write DSFID***, used to write the 8-bit value in the DSFID register.
- ***Lock DSFID***, used to lock the DSFID register.
- ***Get system info***, used to provide the system information value.
- ***Get multiple block security status***, used to send the security status of the selected block.
- ***Initiate***, used to trigger the tag response to the Inventory initiated sequence.
- ***Inventory initiated***, used to perform the anticollision sequence triggered by the Initiate command.
- ***Write-sector password***, used to write the 32 bits of the selected password.
- **Lock-sector**, used to write the sector security status bits of the selected sector.
- ***Present-sector password***, enables the user to present a password to unprotect the user blocks linked to this password.
- ***Fast initiate***, used to trigger the tag response to the Inventory initiated sequence.
- ***Fast inventory initiated***, used to perform the anticollision sequence triggered by the Initiate command.
- ***Fast read single block***, used to output the 32 bits of the selected block and its locking status.
- ***Fast read multiple blocks***, used to read the selected blocks and send back their value.
- ***ReadCfg,*** used to read the 8-bit Configuration byte and send back its value.
- ***WriteEHCfg***, used to write the energy harvesting configuration bits into the Configuration byte.
- ***WriteDOCfg***, used to write the RF WIP/BUSY pin configuration bit into the Configuration byte.
- ***SetRstEHEn***, used to set or reset the EH_enable bit into the volatile Control register.
- ***CheckEHEn***, used to send back the value of the volatile Control register.

7.3 Initial dialog for vicinity cards

The dialog between the vicinity coupling device or VCD (commonly the “RF reader”) and the vicinity integrated circuit card or VICC (M24LR64E-R) takes place as follows:

- activation of the M24LR64E-R by the RF operating field of the VCD,
- transmission of a command by the VCD,
- transmission of a response by the M24LR64E-R.

These operations use the RF power transfer and communication signal interface described below (see *Power transfer*, *Frequency* and *Operating field*). This technique is called RTF (Reader talk first).

7.3.1 Power transfer

Power is transferred to the M24LR64E-R by radio frequency at 13.56 MHz via coupling antennas in the M24LR64E-R and the VCD. The RF operating field of the VCD is transformed on the M24LR64E-R antenna to an AC voltage which is rectified, filtered and internally regulated.

During communications, the amplitude modulation (ASK) on this received signal is demodulated by the ASK demodulator.

7.3.2 Frequency

The ISO 15693 standard defines the carrier frequency (f_C) of the operating field as 13.56 MHz ±7 kHz.

7.3.3 Operating field

The M24LR64E-R operates continuously between the minimum and maximum values of the electromagnetic field H defined in *Table 124*. The VCD has to generate a field within these limits.

8 Communication signal from VCD to M24LR64E-R

Communications between the VCD and the M24LR64E-R take place using the modulation principle of ASK (Amplitude shift keying). Two modulation indexes are used, 10% and 100%. The M24LR64E-R decodes both. The VCD determines which index is used.

The modulation index is defined as [a – b]/[a + b], where a is the peak signal amplitude, and b the minimum signal amplitude of the carrier frequency.

Depending on the choice made by the VCD, a “pause” is created as described in *Figure 14* and *Figure 15*.

The M24LR64E-R is operational for the 100% modulation index or for any degree of modulation index between 10% and 30% (see *Table 124*).

Figure 14. 100% modulation waveform

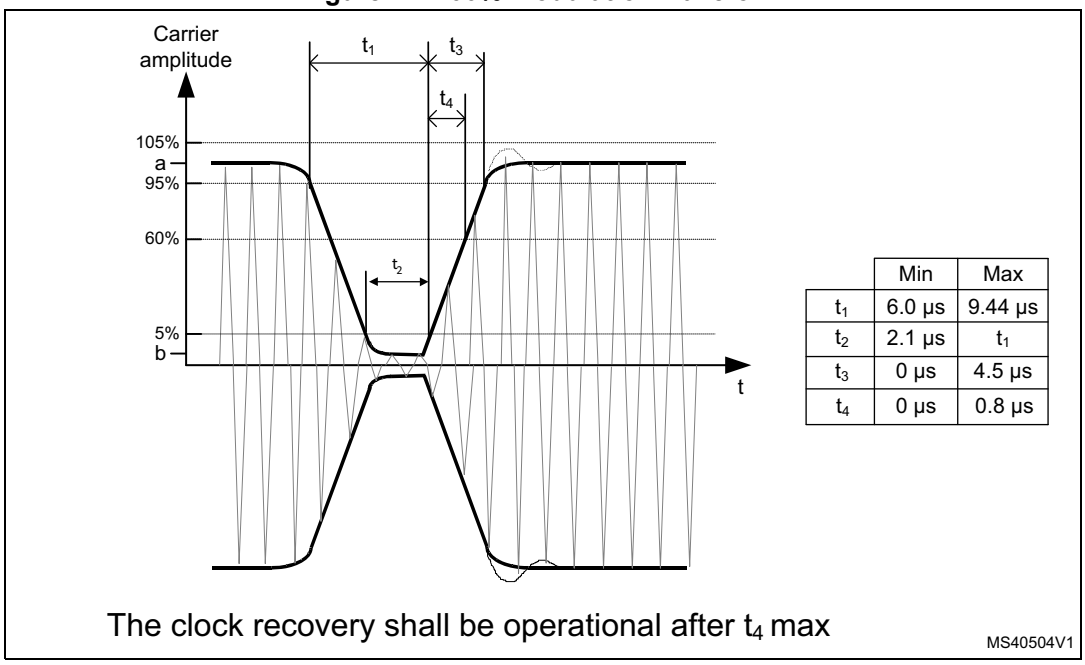
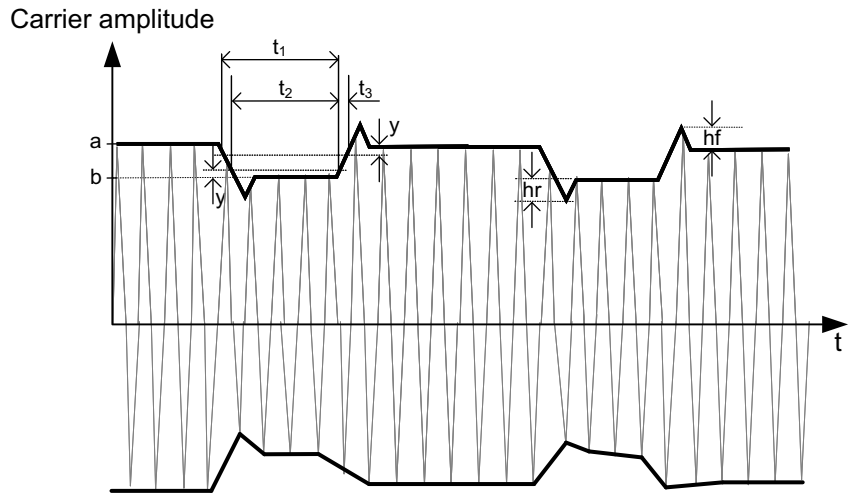


Table 19. 10% modulation parameters

Symbol	Parameter definition	Value
hr	0.1 x (a – b)	max
hf	0.1 x (a – b)	max

Figure 15. 10% modulation waveform



	Min	Max
t_1	6.0 µs	9.44 µs
t_2	3.0 µs	t_1
t_3	0	4.5 µs
Modulation index	10%	30%

y	0.05 (a-b)
hf, hr	0.1 (a-b) max

The VICC shall be operational for any value of modulation index between 10 and 30%.

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9 Data rate and data coding

The data coding implemented in the M24LR64E-R uses pulse position modulation. Both data coding modes that are described in the ISO15693 are supported by the M24LR64E-R. The selection is made by the VCD and indicated to the M24LR64E-R within the start of frame (SOF).

9.1 Data coding mode: 1 out of 256

The value of one single byte is represented by the position of one pause. The position of the pause on 1 of 256 successive time periods of 18.88 µs (256/f_C) determines the value of the byte. In this case, the transmission of one byte takes 4.833 ms and the resulting data rate is 1.65 Kbits/s (f_C/8192).

Figure 16 illustrates this pulse position modulation technique. In this figure, data E1h (225 decimal) is sent by the VCD to the M24LR64E-R.

The pause occurs during the second half of the position of the time period that determines the value, as shown in *Figure 17*.

A pause during the first period transmits the data value 00h. A pause during the last period transmits the data value FFh (255 decimal).

Figure 16. 1 out of 256 coding mode

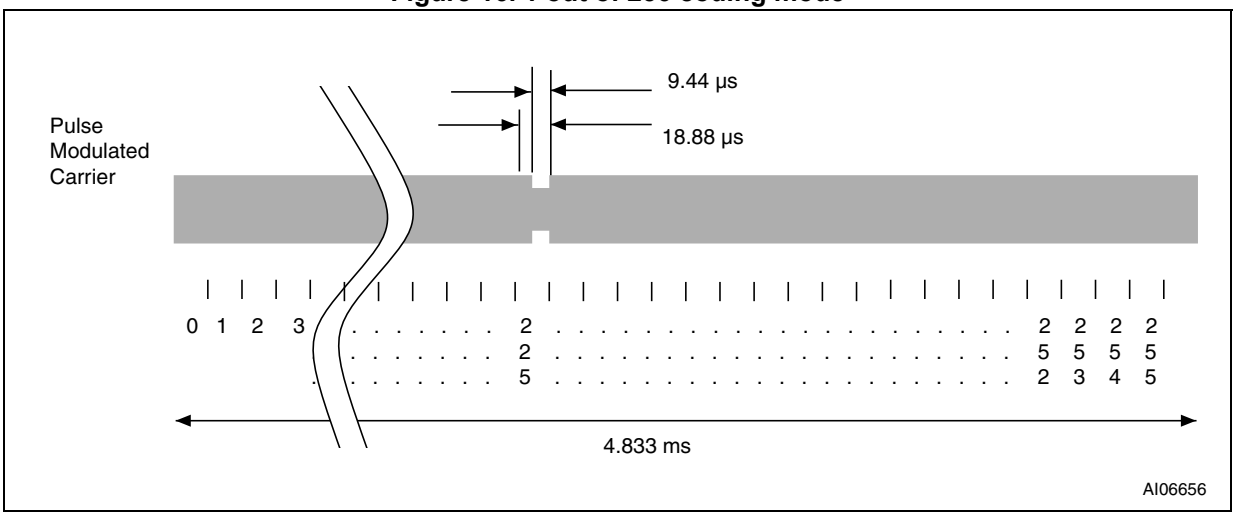
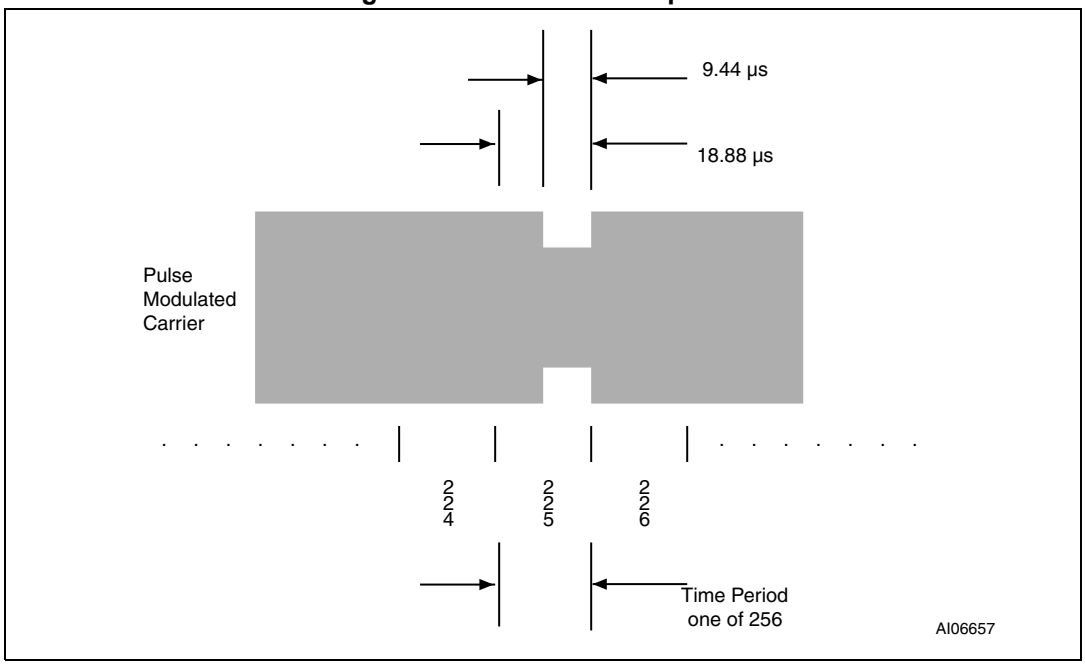


Figure 17. Detail of a time period



9.2 Data coding mode: 1 out of 4

The value of two bits is represented by the position of one pause. The position of the pause on 1 of 4 successive time periods of 18.88 µs ($256/f_C$) determines the value of the two bits. Four successive pairs of bits form a byte, where the least significant pair of bits is transmitted first.

In this case, the transmission of one byte takes 302.08 µs and the resulting data rate is 26.48 Kbits/s ($f_C/512$). *Figure 18* illustrates the 1 out of 4 pulse position technique and coding. *Figure 19* shows the transmission of E1h (225d - 1110 0001b) by the VCD.

Figure 18. 1 out of 4 coding mode

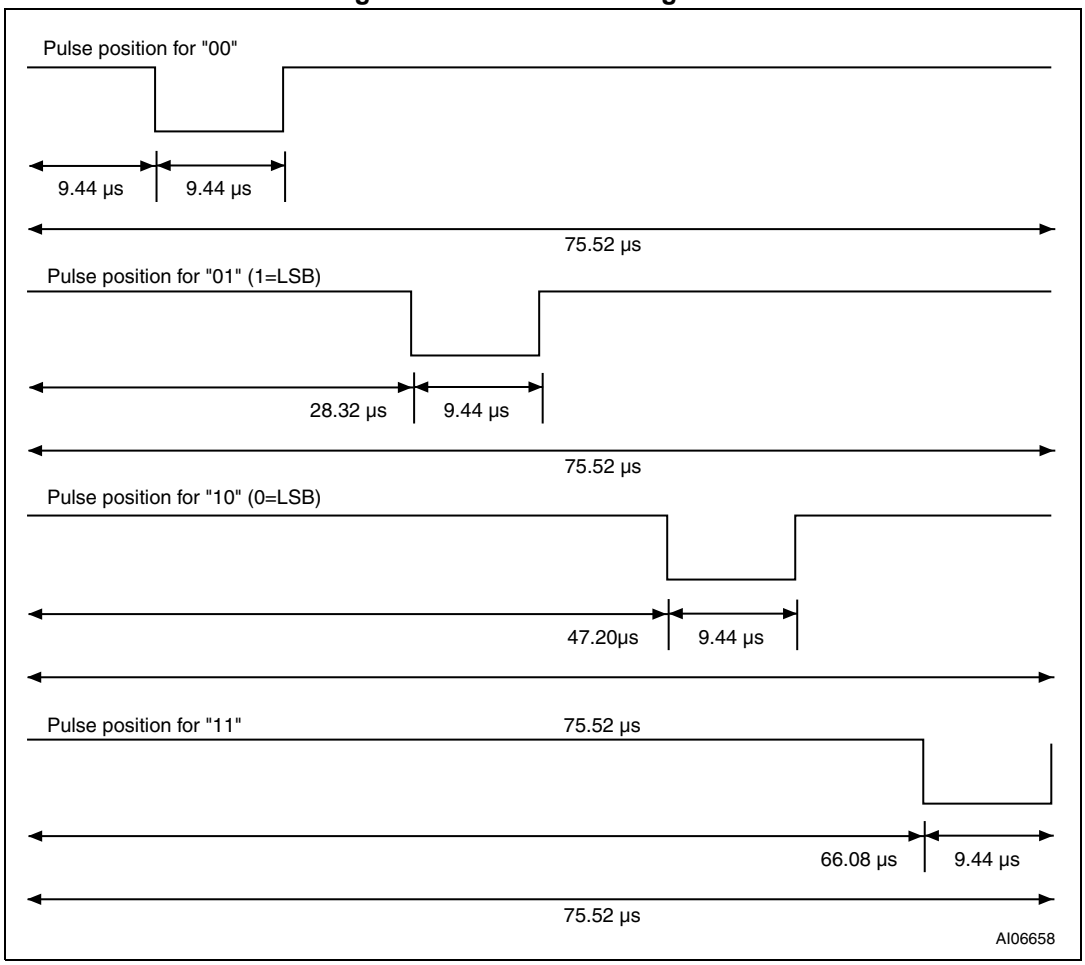
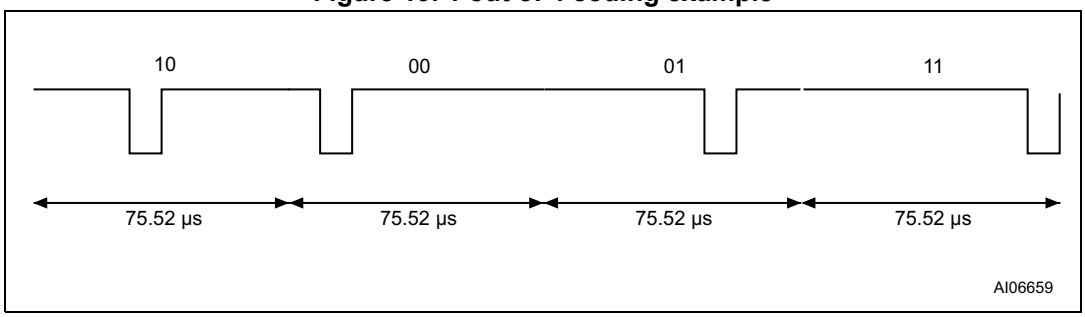


Figure 19. 1 out of 4 coding example



9.3 VCD to M24LR64E-R frames

Frames are delimited by a start of frame (SOF) and an end of frame (EOF). They are implemented using code violation. Unused options are reserved for future use.

The M24LR64E-R is ready to receive a new command frame from the VCD 311.5 µs after sending a response frame to the VCD.

The M24LR64E-R takes a power-up time of 0.1 ms after being activated by the powering field. After this delay, the M24LR64E-R is ready to receive a command frame from the VCD.

9.4 Start of frame (SOF)

The SOF defines the data coding mode the VCD is to use for the following command frame. The SOF sequence described in *Figure 20* selects the 1 out of 256 data coding mode. The SOF sequence described in *Figure 21* selects the 1 out of 4 data coding mode. The EOF sequence for either coding mode is described in *Figure 22*.

Figure 20. SOF to select 1 out of 256 data coding mode

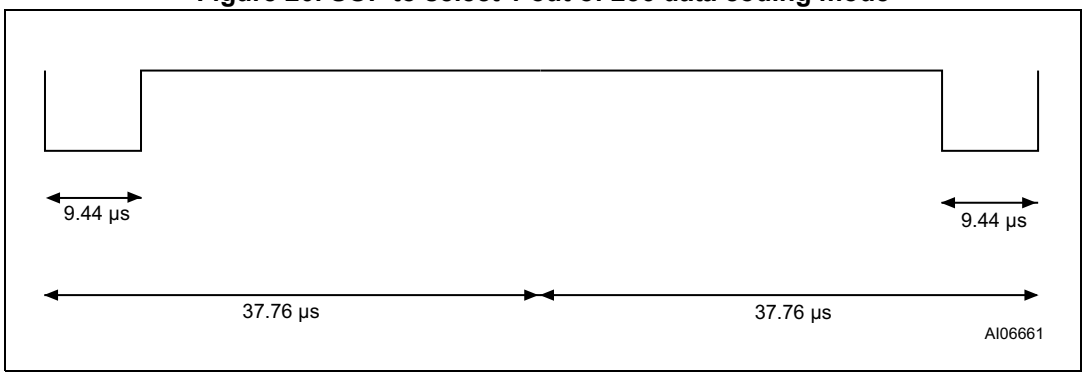


Figure 21. SOF to select 1 out of 4 data coding mode

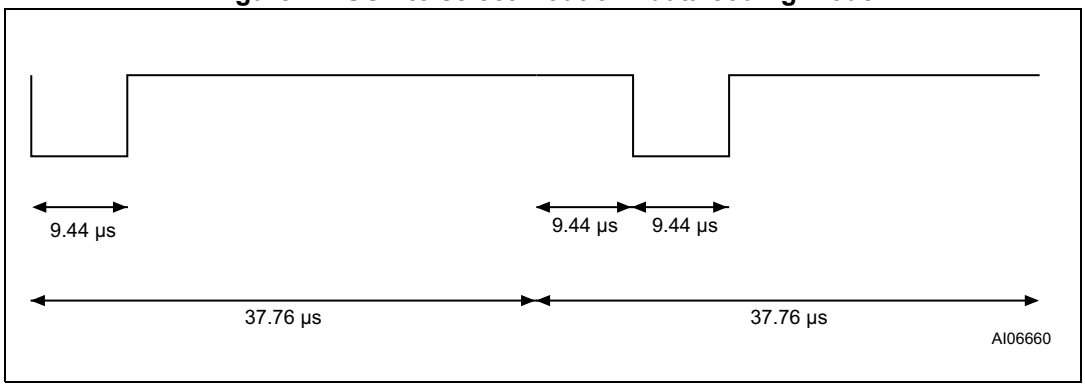
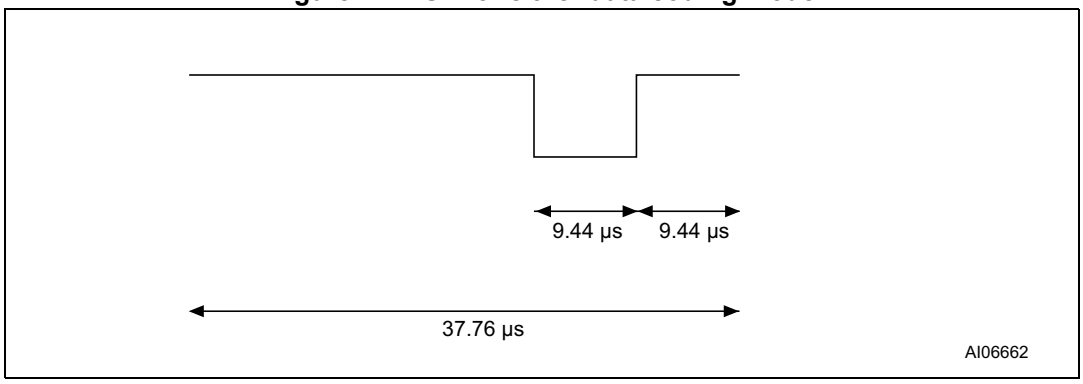


Figure 22. EOF for either data coding mode



10 Communication signal from M24LR64E-R to VCD

The M24LR64E-R has several modes defined for some parameters, so that it can operate in various noise environments and meet various application requirements.

10.1 Load modulation

The M24LR64E-R is capable of communicating to the VCD via an inductive coupling area whereby the carrier is loaded to generate a subcarrier with frequency f_S. The subcarrier is generated by switching a load in the M24LR64E-R.

The load-modulated amplitude received on the VCD antenna must be of at least 10 mV when measured, as described in the test methods defined in International Standard ISO10373-7.

10.2 Subcarrier

The M24LR64E-R supports the one-subcarrier and two-subcarrier response formats. These formats are selected by the VCD using the first bit in the protocol header. When one subcarrier is used, the frequency f_{S1} of the subcarrier load modulation is 423.75 kHz (f_C/32). When two subcarriers are used, the frequency f_{S1} is 423.75 kHz (f_C/32), and frequency f_{S2} is 484.28 kHz (f_C/28). When using the two-subcarrier mode, the M24LR64E-R generates a continuous phase relationship between f_{S1} and f_{S2}.

10.3 Data rates

The M24LR64E-R can respond using the low or the high data rate format. The selection of the data rate is made by the VCD using the second bit in the protocol header. For fast commands, the selected data rate is multiplied by two. *Table 20* shows the different data rates produced by the M24LR64E-R using the different response format combinations.

Table 20. Response data rates

Data rate		One subcarrier	Two subcarriers
Low	Standard commands	6.62 Kbit/s (f_c/2048)	6.67 Kbit/s (f_c/2032)
	Fast commands	13.24 Kbit/s (f_c/1024)	Not applicable
High	Standard commands	26.48 Kbit/s (f_c/512)	26.69 Kbit/s (f_c/508)
	Fast commands	52.97 Kbit/s (f_c/256)	Not applicable

11 Bit representation and coding

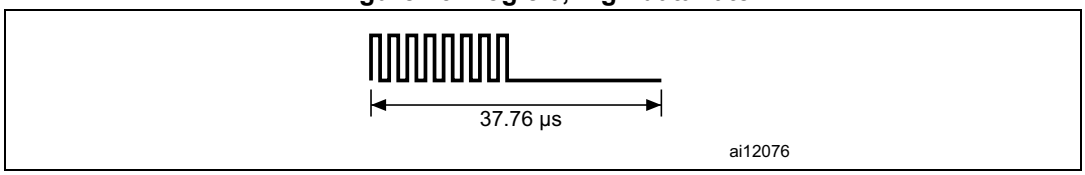
Data bits are encoded using Manchester coding, according to the following schemes. For the low data rate, same subcarrier frequency or frequencies is/are used. In this case, the number of pulses is multiplied by 4 and all times increase by this factor. For the Fast commands using one subcarrier, all pulse numbers and times are divided by 2.

11.1 Bit coding using one subcarrier

11.1.1 High data rate

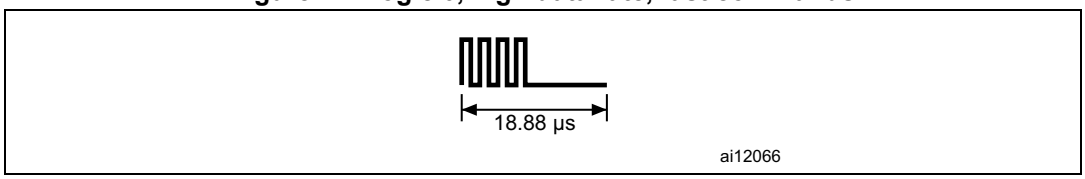
A logic 0 starts with eight pulses at 423.75 kHz (f_C/32) followed by an unmodulated time of 18.88 µs, as shown in *Figure 23*.

Figure 23. Logic 0, high data rate



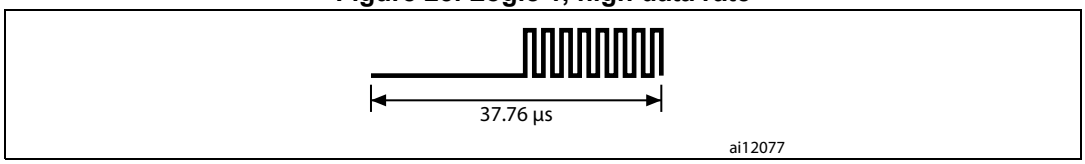
For the fast commands, a logic 0 starts with four pulses at 423.75 kHz (f_C/32) followed by an unmodulated time of 9.44 µs, as shown in *Figure 24*.

Figure 24. Logic 0, high data rate, fast commands



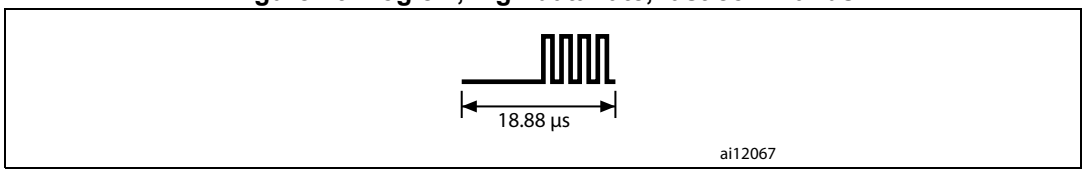
A logic 1 starts with an unmodulated time of 18.88 µs followed by eight pulses at 423.75 kHz (f_C/32), as shown in *Figure 25*.

Figure 25. Logic 1, high data rate



For the Fast commands, a logic 1 starts with an unmodulated time of 9.44 µs followed by four pulses of 423.75 kHz (f_C/32), as shown in *Figure 26*.

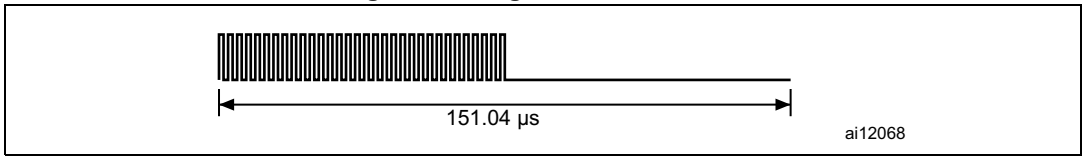
Figure 26. Logic 1, high data rate, fast commands



11.1.2 Low data rate

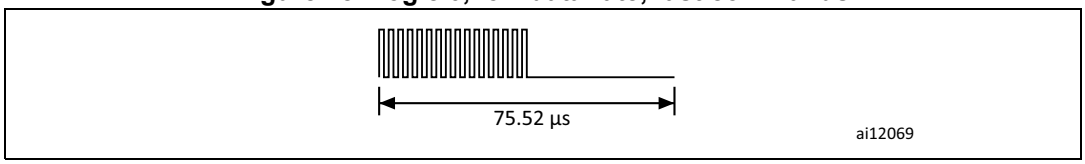
A logic 0 starts with 32 pulses at 423.75 kHz (f_C/32) followed by an unmodulated time of 75.52 µs, as shown in *Figure 27*.

Figure 27. Logic 0, low data rate



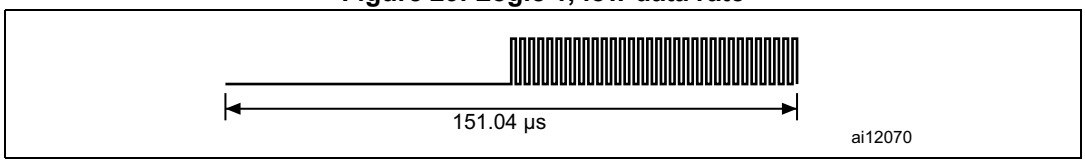
For the Fast commands, a logic 0 starts with 16 pulses at 423.75 kHz (f_C/32) followed by an unmodulated time of 37.76 µs, as shown in *Figure 28*.

Figure 28. Logic 0, low data rate, fast commands



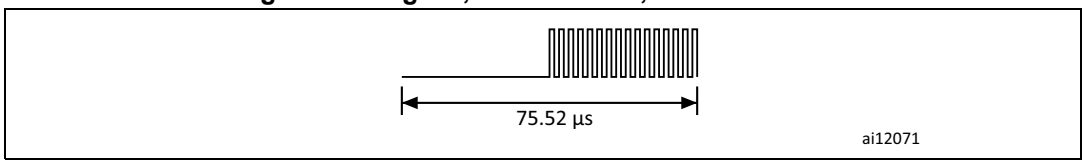
A logic 1 starts with an unmodulated time of 75.52 µs followed by 32 pulses at 423.75 kHz (f_C/32), as shown in *Figure 29*.

Figure 29. Logic 1, low data rate



For the Fast commands, a logic 1 starts with an unmodulated time of 37.76 µs followed by 16 pulses at 423.75 kHz (f_C/32), as shown in *Figure 30*.

Figure 30. Logic 1, low data rate, fast commands

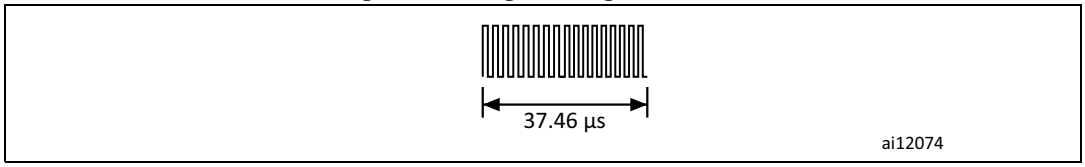


11.2 Bit coding using two subcarriers

11.2.1 High data rate

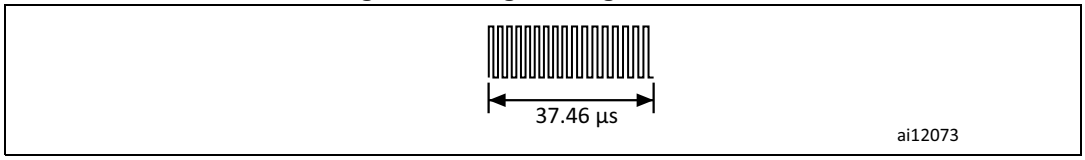
A logic 0 starts with eight pulses at 423.75 kHz ($f_C/32$) followed by nine pulses at 484.28 kHz ($f_C/28$), as shown in *Figure 31*. Bit coding using two subcarriers is not supported for the Fast commands.

Figure 31. Logic 0, high data rate



A logic 1 starts with nine pulses at 484.28 kHz ($f_C/28$) followed by eight pulses at 423.75 kHz ($f_C/32$), as shown in *Figure 32*. Bit coding using two subcarriers is not supported for the Fast commands.

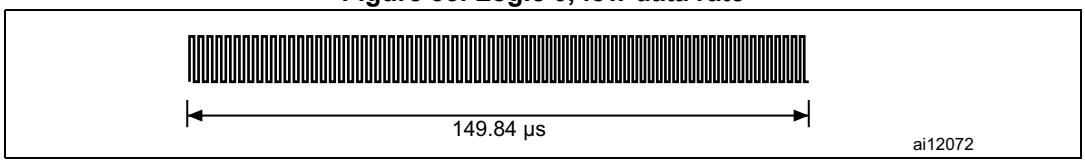
Figure 32. Logic 1, high data rate



11.2.2 Low data rate

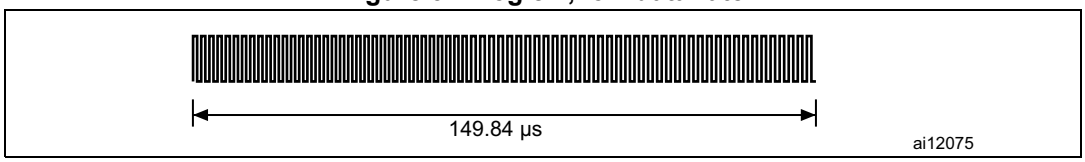
A logic 0 starts with 32 pulses at 423.75 kHz ($f_C/32$) followed by 36 pulses at 484.28 kHz ($f_C/28$), as shown in *Figure 33*. Bit coding using two subcarriers is not supported for the Fast commands.

Figure 33. Logic 0, low data rate



A logic 1 starts with 36 pulses at 484.28 kHz ($f_C/28$) followed by 32 pulses at 423.75 kHz ($f_C/32$) as shown in *Figure 34*. Bit coding using two subcarriers is not supported for the Fast commands.

Figure 34. Logic 1, low data rate



12 M24LR64E-R to VCD frames

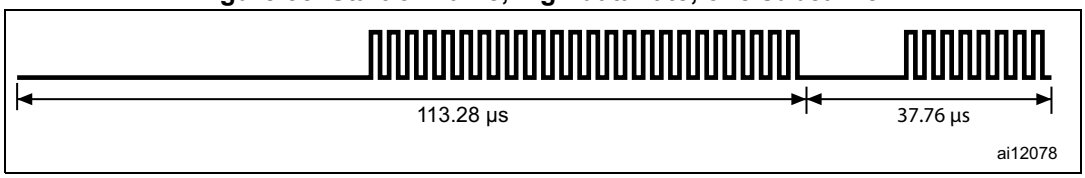
Frames are delimited by an SOF and an EOF. They are implemented using code violation. Unused options are reserved for future use. For the low data rate, the same subcarrier frequency or frequencies is/are used. In this case, the number of pulses is multiplied by 4. For the Fast commands using one subcarrier, all pulse numbers and times are divided by 2.

12.1 SOF when using one subcarrier

12.1.1 High data rate

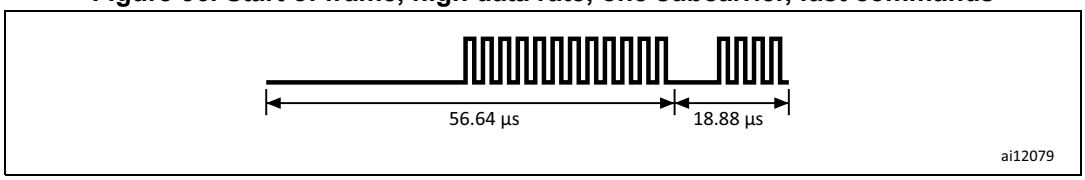
The SOF includes an unmodulated time of 56.64 µs, followed by 24 pulses at 423.75 kHz ($f_C/32$), and a logic 1 that consists of an unmodulated time of 18.88 µs followed by eight pulses at 423.75 kHz, as shown in *Figure 35*.

Figure 35. Start of frame, high data rate, one subcarrier



For the Fast commands, the SOF comprises an unmodulated time of 28.32 µs, followed by 12 pulses at 423.75 kHz ($f_C/32$), and a logic 1 that consists of an unmodulated time of 9.44 µs followed by four pulses at 423.75 kHz, as shown in *Figure 36*.

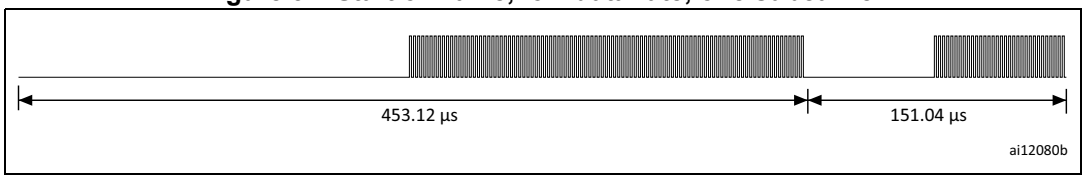
Figure 36. Start of frame, high data rate, one subcarrier, fast commands



12.1.2 Low data rate

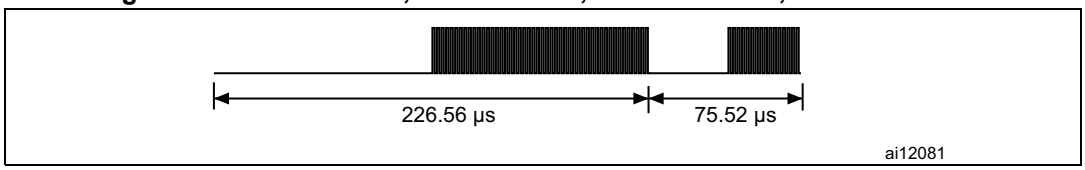
The SOF comprises an unmodulated time of 226.56 µs, followed by 96 pulses at 423.75 kHz ($f_C/32$), and a logic 1 that consists of an unmodulated time of 75.52 µs followed by 32 pulses at 423.75 kHz, as shown in *Figure 37*.

Figure 37. Start of frame, low data rate, one subcarrier



For the Fast commands, the SOF comprises an unmodulated time of 113.28 µs, followed by 48 pulses at 423.75 kHz (f_C/32), and a logic 1 that includes an unmodulated time of 37.76 µs followed by 16 pulses at 423.75 kHz, as shown in *Figure 38*.

Figure 38. Start of frame, low data rate, one subcarrier, fast commands



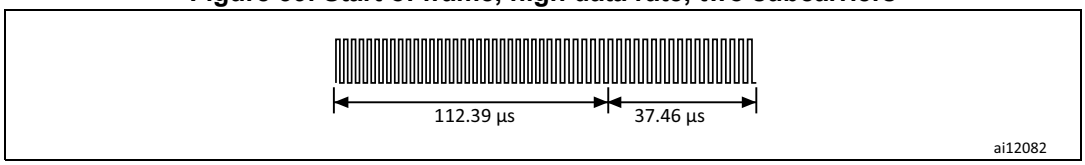
12.2 SOF when using two subcarriers

12.2.1 High data rate

The SOF comprises 27 pulses at 484.28 kHz (f_C/28), followed by 24 pulses at 423.75 kHz (f_C/32), and a logic 1 that includes nine pulses at 484.28 kHz followed by eight pulses at 423.75 kHz, as shown in *Figure 39*.

Bit coding using two subcarriers is not supported for the Fast commands.

Figure 39. Start of frame, high data rate, two subcarriers

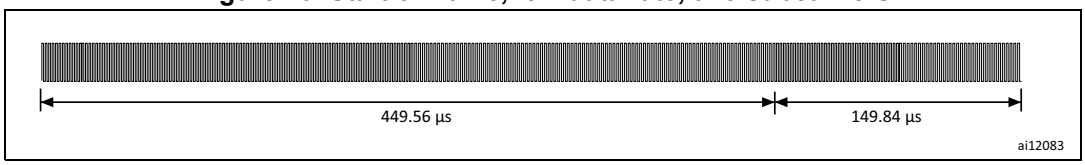


12.2.2 Low data rate

The SOF comprises 108 pulses at 484.28 kHz (f_C/28), followed by 96 pulses at 423.75 kHz (f_C/32), and a logic 1 that includes 36 pulses at 484.28 kHz followed by 32 pulses at 423.75 kHz, as shown in *Figure 40*.

Bit coding using two subcarriers is not supported for the Fast commands.

Figure 40. Start of frame, low data rate, two subcarriers

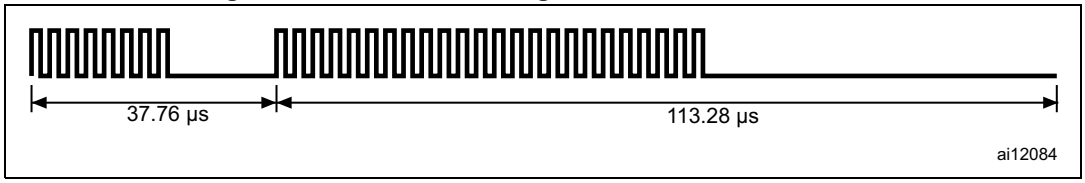


12.3 EOF when using one subcarrier

12.3.1 High data rate

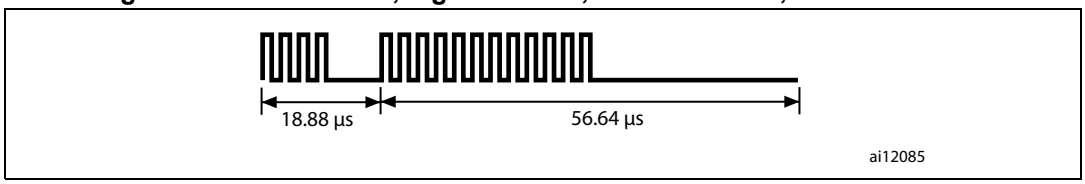
The EOF comprises a logic 0 that includes eight pulses at 423.75 kHz and an unmodulated time of 18.88 µs, followed by 24 pulses at 423.75 kHz (f_C/32), and by an unmodulated time of 56.64 µs, as shown in *Figure 41*.

Figure 41. End of frame, high data rate, one subcarrier



For the Fast commands, the EOF comprises a logic 0 that includes four pulses at 423.75 kHz and an unmodulated time of 9.44 µs, followed by 12 pulses at 423.75 kHz (f_C/32) and an unmodulated time of 37.76 µs, as shown in *Figure 42*.

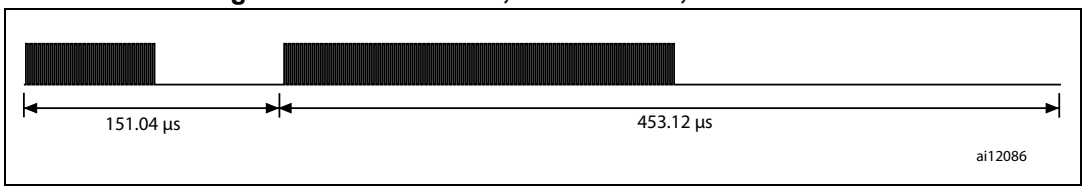
Figure 42. End of frame, high data rate, one subcarrier, fast commands



12.3.2 Low data rate

The EOF comprises a logic 0 that includes 32 pulses at 423.75 kHz and an unmodulated time of 75.52 µs, followed by 96 pulses at 423.75 kHz (f_C/32) and an unmodulated time of 226.56 µs, as shown in *Figure 43*.

Figure 43. End of frame, low data rate, one subcarrier



For the Fast commands, the EOF comprises a logic 0 that includes 16 pulses at 423.75 kHz and an unmodulated time of 37.76 µs, followed by 48 pulses at 423.75 kHz (f_C/32) and an unmodulated time of 113.28 µs, as shown in *Figure 44*.

Figure 44. End of frame, low data rate, one subcarrier, Fast commands

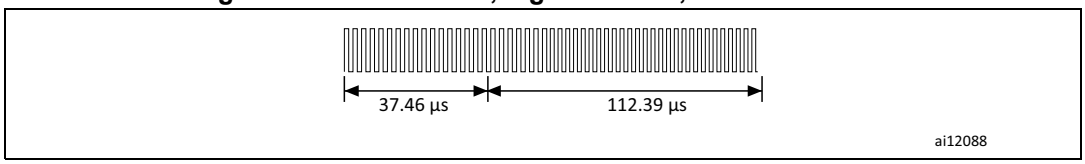
12.4 EOF when using two subcarriers

12.4.1 High data rate

The EOF comprises a logic 0 that includes eight pulses at 423.75 kHz and nine pulses at 484.28 kHz, followed by 24 pulses at 423.75 kHz (f_C/32) and 27 pulses at 484.28 kHz (f_C/28), as shown in *Figure 45*.

Bit coding using two subcarriers is not supported for the Fast commands.

Figure 45. End of frame, high data rate, two subcarriers

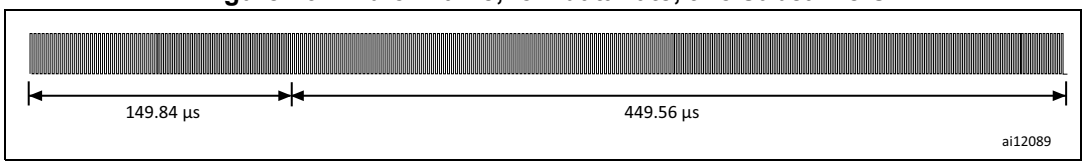


12.4.2 Low data rate

The EOF comprises a logic 0 that includes 32 pulses at 423.75 kHz and 36 pulses at 484.28 kHz, followed by 96 pulses at 423.75 kHz (f_C/32) and 108 pulses at 484.28 kHz (f_C/28), as shown in *Figure 46*.

Bit coding using two subcarriers is not supported for the Fast commands.

Figure 46. End of frame, low data rate, two subcarriers



13 Unique identifier (UID)

The M24LR64E-R is uniquely identified by a 64-bit unique identifier (UID). This UID complies with ISO/IEC 15963 and ISO/IEC 7816-6. The UID is a read-only code and comprises:

- eight MSBs with a value of E0h,
- the IC manufacturer code “ST 02h” on 8 bits (ISO/IEC 7816-6/AM1),
- a unique serial number on 48 bits.

Table 21. UID format

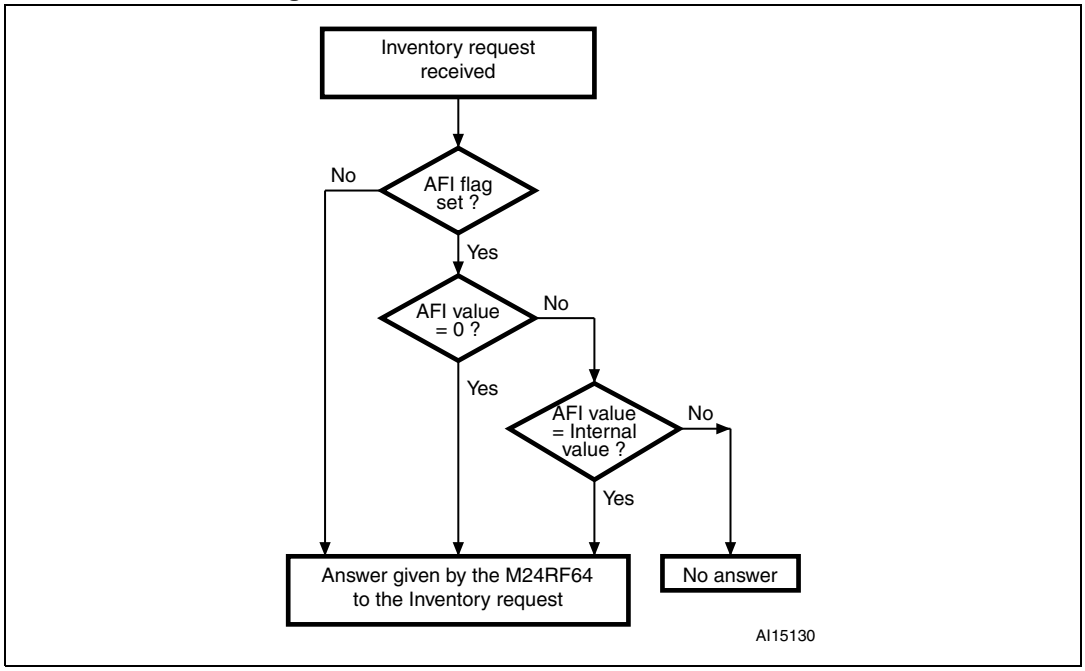
MSB		LSB	
63 **56**	**55** **48**	**47** **0**	
0xE0	0x02	Unique serial number	

With the UID, each M24LR64E-R can be addressed uniquely and individually during the anticollision loop and for one-to-one exchanges between a VCD and an M24LR64E-R.

14 Application family identifier (AFI)

The AFI (application family identifier) represents the type of application targeted by the VCD and is used to identify, among all the M24LR64E-Rs present, only those that meet the required application criteria.

Figure 47. M24LR64E-R decision tree for AFI



The AFI is programmed by the M24LR64E-R issuer (or purchaser) in the AFI register. Once programmed and locked, it can no longer be modified.

The most significant nibble of the AFI is used to code one specific or all application families.

The least significant nibble of the AFI is used to code one specific or all application subfamilies. Subfamily codes different from 0 are proprietary.

(See ISO 15693-3 documentation.)

15 Data storage format identifier (DSFID)

The data storage format identifier indicates how the data is structured in the M24LR64E-R memory. The logical organization of data can be known instantly using the DSFID. It can be programmed and locked using the Write DSFID and Lock DSFID commands.

15.1 CRC

The CRC used in the M24LR64E-R is calculated as per the definition in ISO/IEC 13239. The initial register contents are all ones: “FFFF”.

The two-byte CRC is appended to each request and response, within each frame, before the EOF. The CRC is calculated on all the bytes after the SOF up to the CRC field.

Upon reception of a request from the VCD, the M24LR64E-R verifies that the CRC value is valid. If it is invalid, the M24LR64E-R discards the frame and does not answer the VCD.

Upon reception of a response from the M24LR64E-R, it is recommended that the VCD verifies whether the CRC value is valid. If it is invalid, actions to be performed are left to the discretion of the VCD designer.

The CRC is transmitted least significant byte first. Each byte is transmitted least significant bit first.

Table 22. CRC transmission rules

LSByte		LSByte	
LSBit	**MSBit**	**LSBit**	**MSBit**
CRC 16 (8 bits)		CRC 16 (8 bits)	

16 M24LR64E-R protocol description

The transmission protocol (or simply “the protocol”) defines the mechanism used to exchange instructions and data between the VCD and the M24LR64E-R in both directions. It is based on the concept of “VCD talks first”.

This means that an M24LR64E-R does not start transmitting unless it has received and properly decoded an instruction sent by the VCD. The protocol is based on an exchange of:

- a request from the VCD to the M24LR64E-R,
- a response from the M24LR64E-R to the VCD.

Each request and each response are contained in a frame. The frame delimiters (SOF, EOF) are described in *Section 12*.

Each request consists of:

- a request SOF (see *Figure 20* and *Figure 21*),
- flags,
- a command code,
- parameters depending on the command,
- application data,
- a 2-byte CRC,
- a request EOF (see *Figure 22*).

Each response consists of:

- an answer SOF (see *Figure 35* to *Figure 40*),
- flags,
- parameters depending on the command,
- application data,
- a 2-byte CRC,
- an answer EOF (see *Figure 41* to *Figure 46*).

The protocol is bit-oriented. The number of bits transmitted in a frame is a multiple of eight (8), that is an integer number of bytes.

A single-byte field is transmitted least significant bit (LSBit) first. A multiple-byte field is transmitted least significant byte (LSByte) first and each byte is transmitted least significant bit (LSBit) first.

The setting of the flags indicates the presence of the optional fields. When the flag is set (to one), the field is present. When the flag is reset (to zero), the field is absent.

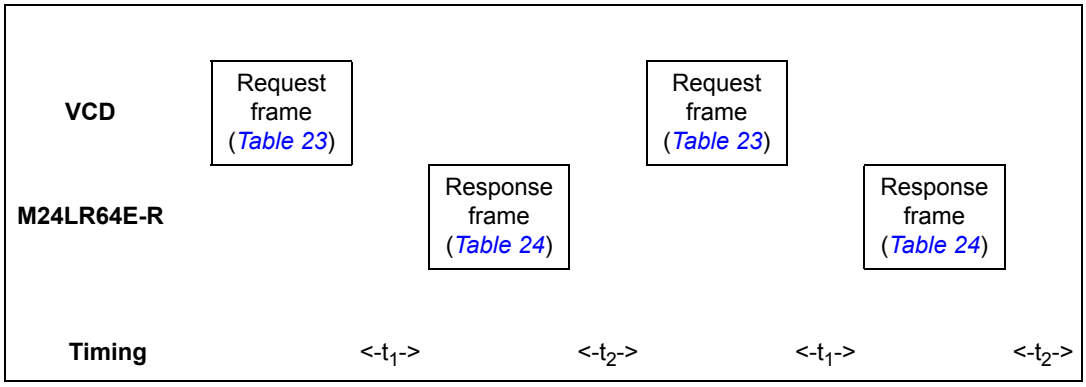
Table 23. VCD request frame format

Request SOF	Request_flags	Command code	Parameters	Data	2-byte CRC	Request EOF

Table 24. M24LR64E-R Response frame format

Response SOF	Response_flags	Parameters	Data	2-byte CRC	Response EOF

Figure 48. M24LR64E-R protocol timing



17 M24LR64E-R states

An M24LR64E-R can be in one of four states:

- Power-off
- Ready
- Quiet
- Selected

Transitions between these states are specified in *Figure 49* and *Table 25*.

17.1 Power-off state

The M24LR64E-R is in the Power-off state when it does not receive enough energy from the VCD.

17.2 Ready state

The M24LR64E-R is in the Ready state when it receives enough energy from the VCD. When in the Ready state, the M24LR64E-R answers any request where the Select_flag is not set.

17.3 Quiet state

When in the Quiet state, the M24LR64E-R answers any request except for Inventory requests with the Address_flag set.

17.4 Selected state

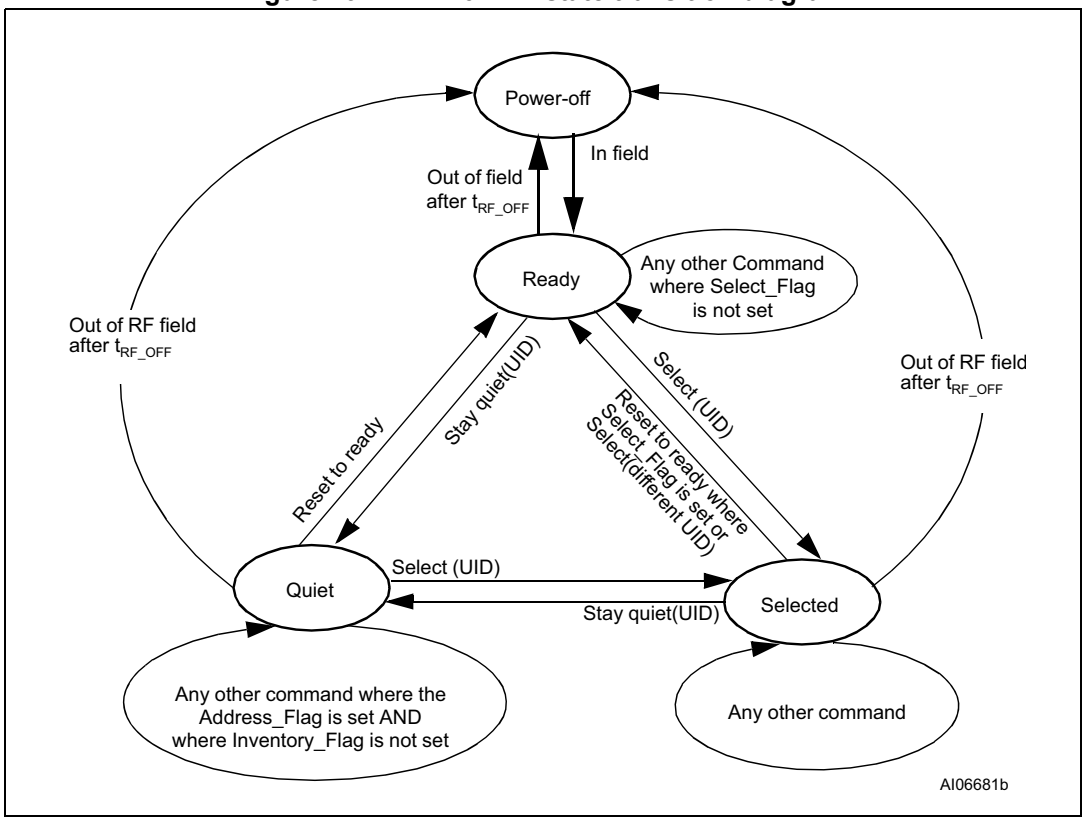
In the Selected state, the M24LR64E-R answers any request in all modes (see *Section 18*):

- Request in Select mode with the Select_flag set
- Request in Addressed mode if the UID matches
- Request in Non-Addressed mode as it is the mode for general requests

Table 25. M24LR64E-R response depending on Request_flags

Flags	Address_flag		Select_flag	
	1 Addressed	0 Non addressed	1 Selected	0 Non selected
M24LR64E-R in Ready or Selected state (Devices in Quiet state do not answer)	-	X	-	X
M24LR64E-R in Selected state	-	X	X	-
M24LR64E-R in Ready, Quiet or Selected state (the device which matches the UID)	X	-	-	X
Error (03h)	X	-	X	-

Figure 49. M24LR64E-R state transition diagram



1. The M24LR64E-R returns to the Power Off state if the tag is out of the RF field for at least t_{RF_OFF}. Please refer to application note AN4125 for more information.
2. The intention of the state transition method is that only one M24LR64E-R should be in the Selected state at a time.

18 Modes

The term “mode” refers to the mechanism used in a request to specify the set of M24LR64E-Rs that answers the request.

18.1 Addressed mode

When the Address_flag is set to 1 (Addressed mode), the request contains the Unique ID (UID) of the addressed M24LR64E-R.

Any M24LR64E-R that receives a request with the Address_flag set to 1 compares the received Unique ID to its own. If it matches, then the M24LR64E-R executes the request (if possible) and returns a response to the VCD as specified in the command description.

If the UID does not match, then it remains silent.

18.2 Non-addressed mode (general request)

When the Address_flag is cleared to 0 (Non-Addressed mode), the request does not contain a Unique ID. Any M24LR64E-R receiving a request with the Address_flag cleared to 0 executes it and returns a response to the VCD as specified in the command description.

18.3 Select mode

When the Select_flag is set to 1 (Select mode), the request does not contain an M24LR64E-R Unique ID. The M24LR64E-R in the Selected state that receives a request with the Select_flag set to 1 executes it and returns a response to the VCD as specified in the command description.

Only M24LR64E-Rs in the Selected state answer a request where the Select_flag is set to 1.

The system design ensures in theory that only one M24LR64E-R can be in the Select state at a time.

19 Request format

The request consists of:

- an SOF,
- flags,
- a command code,
- parameters and data,
- a CRC,
- an EOF.

Table 26. General request format

SOF	Request_flags	Command code	Parameters	Data	CRC	EOF

19.1 Request flags

In a request, the “flags” field specifies the actions to be performed by the M24LR64E-R and whether corresponding fields are present or not.

The flags field consists of eight bits. Bit 3 (Inventory_flag) of the request flag defines the contents of the four MSBs (bits 5 to 8). When bit 3 is reset (0), bits 5 to 8 define the M24LR64E-R selection criteria. When bit 3 is set (1), bits 5 to 8 define the M24LR64E-R Inventory parameters.

Table 27. Definition of request flags 1 to 4

Bit No.	Flag	Level	Description
Bit 1	Subcarrier_flag(1)	0	A single subcarrier frequency is used by the M24LR64E-R
		1	Two subcarriers are used by the M24LR64E-R
Bit 2	Data_rate_flag(2)	0	Low data rate is used
		1	High data rate is used
Bit 3	Inventory_flag	0	The meaning of flags 5 to 8 is described in *Table 28*
		1	The meaning of flags 5 to 8 is described in *Table 29*
Bit 4	Protocol_extension_flag(3)	0	No Protocol format extension
		1	Protocol format extension

1. Subcarrier_flag refers to the M24LR64E-R-to-VCD communication.
2. Data_rate_flag refers to the M24LR64E-R-to-VCD communication.
3. Protocol_extension_flag must be set to 1 for Read Single Block, Read Multiple Block, Fast Read Multiple Block, Write Single Block, and Get Multiple Block Security Status commands. Get System Info command supports two options: a standard response format when Protocol_extension_flag is set to 0, and a rich response when protocol extension is set to 1.

Table 28. Request flags 5 to 8 when Bit 3 = 0

Bit No.	Flag	Level	Description
Bit 5	Select flag(1)	0	The request is executed by any M24LR64E-R according to the setting of Address_flag
		1	The request is executed only by the M24LR64E-R in Selected state
Bit 6	Address flag(1)	0	The request is not addressed. UID field is not present. The request is executed by all M24LR64E-Rs.
		1	The request is addressed. UID field is present. The request is executed only by the M24LR64E-R whose UID matches the UID specified in the request.
Bit 7	Option flag	0	Option not activated.
		1	Option activated.
Bit 8	RFU	0	-

1. If the Select_flag is set to 1, the Address_flag is set to 0 and the UID field is not present in the request.

Table 29. Request flags 5 to 8 when Bit 3 = 1

Bit No.	Flag	Level	Description
Bit 5	AFI flag	0	AFI field is not present
		1	AFI field is present
Bit 6	Nb_slots flag	0	16 slots
		1	1 slot
Bit 7	Option flag	0	-
Bit 8	RFU	0	-

20 Response format

The response consists of:

- an SOF,
- flags,
- parameters and data,
- a CRC,
- an EOF.

Table 30. General response format

SOF	Response_flags	Parameters	Data	CRC	EOF

20.1 Response flags

In a response, the flags indicate how actions have been performed by the M24LR64E-R and whether corresponding fields are present or not. The response flags consist of eight bits.

Table 31. Definitions of response flags 1 to 8

Bit No.	Flag	Level	Description
Bit 1	Error_flag	0	No error
		1	Error detected. Error code is in the “Error” field.
Bit 2	RFU	0	-
Bit 3	RFU	0	-
Bit 4	Extension flag	0	No extension
Bit 5	RFU	0	-
Bit 6	RFU	0	-
Bit 7	RFU	0	-
Bit 8	RFU	0	-

20.2 Response error code

If the Error_flag is set by the M24LR64E-R in the response, the Error code field is present and provides information about the error that occurred.

Error codes not specified in *Table 32* are reserved for future use.

Table 32. Response error code definition

Error code	Meaning
03h	The option is not supported.
0Fh	Error with no information given.
10h	The specified block is not available.
11h	The specified block is already locked and thus cannot be locked again.
12h	The specified block is locked and its contents cannot be changed.
13h	The specified block was not successfully programmed.
14h	The specified block was not successfully locked.
15h	The specified block is read-protected.

21 Anticollision

The purpose of the anticollision sequence is to inventory the M24LR64E-Rs present in the VCD field using their unique ID (UID).

The VCD is the master of communications with one or several M24LR64E-Rs. It initiates an M24LR64E-R communication by issuing the Inventory request.

The M24LR64E-R sends its response in the determined slot or does not respond.

21.1 Request parameters

When issuing the Inventory Command:

- The VCD sets the Nb_slots_flag as desired.
- The VCD adds the mask length and the mask value after the command field:
  - The mask length is the number of significant bits of the mask value.
  - The mask value is contained in an integer number of bytes. The mask length indicates the number of significant bits. LSB is transmitted first.
- If the mask length is not a multiple of 8 (bits), as many 0-bits as required are added to the mask value MSB, so that the mask value is contained in an integer number of bytes.
- The next field starts at the next byte boundary.

Table 33. Inventory request format

MSB LSB

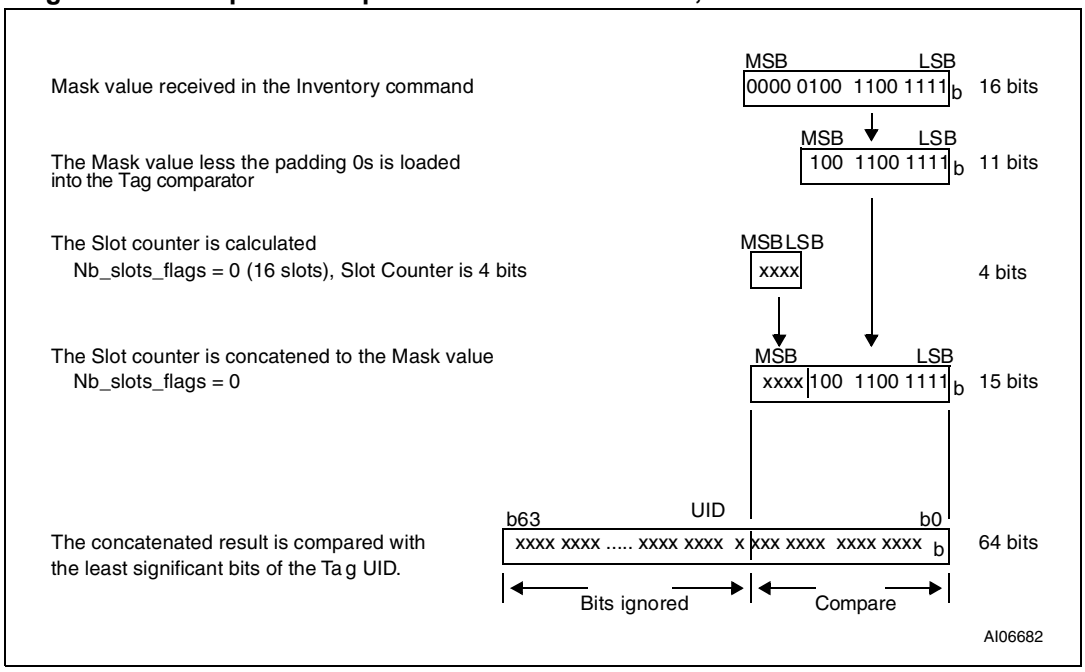
SOF	Request_flags	Command	Optional AFI	Mask length	Mask value	CRC	EOF
-	8 bits	8 bits	8 bits	8 bits	0 to 8 bytes	16 bits	-

In the example provided in *Table 34* and *Figure 50*, the mask length is 11 bits. Five 0-bits are added to the mask value MSB. The 11-bit mask and the current slot number are compared to the UID.

Table 34. Example of the addition of 0-bits to an 11-bit mask value

MSB (b_{15})	LSB (b_0)
0000 0	100 1100 1111
0-bits added	11-bit mask value

Figure 50. Principle of comparison between the mask, the slot number and the UID



The AFI field is present if the AFI_flag is set.

The pulse is generated according to the definition of the EOF in ISO/IEC 15693-2.

The first slot starts immediately after the request EOF is received. To switch to the next slot, the VCD sends an EOF.

The following rules and restrictions apply:

- If no M24LR64E-R answer is detected, the VCD may switch to the next slot by sending an EOF.
- If one or more M24LR64E-R answers are detected, the VCD waits until the complete frame has been received before sending an EOF for switching to the next slot.

22 Request processing by the M24LR64E-R

Upon reception of a valid request, the M24LR64E-R performs the following algorithm:

- NbS is the total number of slots (1 or 16)
- SN is the current slot number (0 to 15)
- LSB (value, n) function returns the n Less Significant Bits of value
- MSB (value, n) function returns the n Most Significant Bits of value
- “&” is the concatenation operator
- Slot_Frame is either an SOF or an EOF

```
SN = 0
if (Nb_slots_flag)
   then NbS = 1
        SN_length = 0
        endif
   else NbS = 16
        SN_length = 4
        endif

label1:
if LSB(UID, SN_length + Mask_length) =
  LSB(SN,SN_length)&LSB(Mask,Mask_length)
   then answer to inventory request
        endif

wait (Slot_Frame)

if Slot_Frame = SOF
   then Stop Anticollision
        decode/process request
        exit
        endif

if Slot_Frame = EOF
   if SN < NbS-1
      then SN = SN + 1
           goto label1
           exit
           endif
   endif
```

23 Explanation of the possible cases

Figure 51 summarizes the main possible cases that can occur during an anticollision sequence when the number of slots is 16.

The sequence of steps is as follows:

- The VCD sends an Inventory request, in a frame terminated by an EOF. The number of slots is 16.
- M24LR64E-R_1 transmits its response in Slot 0. It is the only one to do so, therefore no collision occurs and its UID is received and registered by the VCD.
- The VCD sends an EOF in order to switch to the next slot.
- In Slot 1, two M24LR64E-Rs (M24LR64E-R_2 and M24LR64E-R_3) transmit a response, thus generating a collision. The VCD records the event and registers that a collision was detected in Slot 1.
- The VCD sends an EOF in order to switch to the next slot.
- In Slot 2, no M24LR64E-R transmits a response. Therefore the VCD does not detect any M24LR64E-R SOF and switches to the next slot by sending an EOF.
- In Slot 3, another collision occurs due to responses from M24LR64E-R_4 and M24LR64E-R_5.
- The VCD sends a request (for instance a Read Block) to M24LR64E-R_1 whose UID has already been correctly received.
- All M24LR64E-Rs detect an SOF and exit the anticollision sequence. They process this request and since the request is addressed to M24LR64E-R_1, only M24LR64E-R_1 transmits a response.
- All M24LR64E-Rs are ready to receive another request. If it is an Inventory command, the slot numbering sequence restarts from 0.

Note: The decision to interrupt the anticollision sequence is made by the VCD. EOFs could have been sent until Slot 16, and the request to M24LR64E-R_1 sent then.

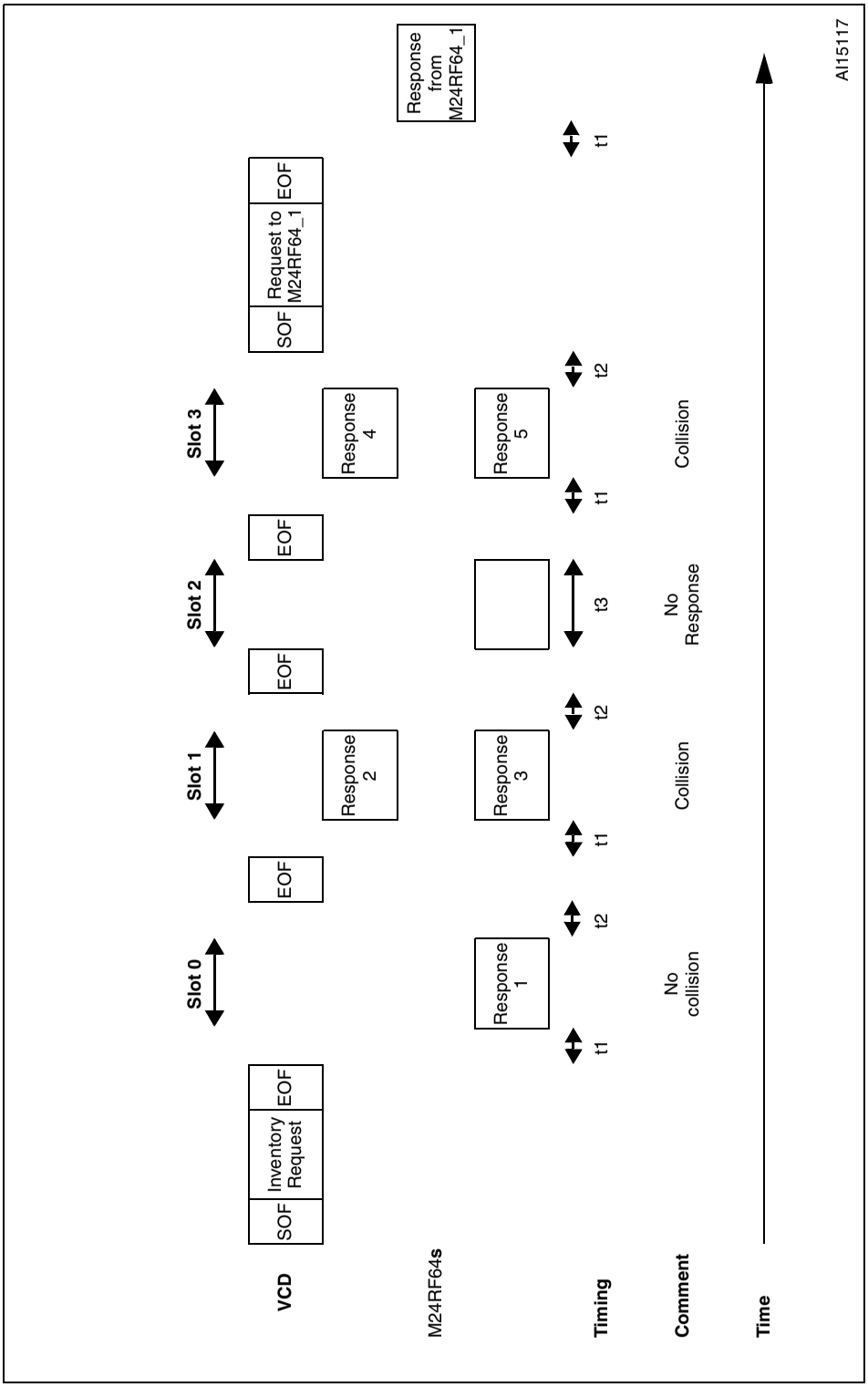


Figure 51. Description of a possible anticollision sequence

24 Inventory Initiated command

The M24LR64E-R provides a special feature to improve the inventory time response of moving tags using the Initiate_flag value. This flag, controlled by the Initiate command, allows tags to answer Inventory Initiated commands.

For applications in which multiple tags are moving in front of a reader, it is possible to miss tags using the standard inventory command. The reason is that the inventory sequence has to be performed on a global tree search. For example, a tag with a particular UID value may have to wait the run of a long tree search before being inventoried. If the delay is too long, the tag may be out of the field before it has been detected.

Using the Initiate command, the inventory sequence is optimized. When multiple tags are moving in front of a reader, the ones which are within the reader field are initiated by the Initiate command. In this case, a small batch of tags answers to the Inventory Initiated command, which optimizes the time necessary to identify all the tags. When finished, the reader has to issue a new Initiate command in order to initiate a new small batch of tags which are new inside the reader field.

It is also possible to reduce the inventory sequence time using the Fast Initiate and Fast Inventory Initiated commands. These commands allow the M24LR64E-Rs to increase their response data rate by a factor of 2, up to 53 Kbit/s.

25 Timing definition

25.1 t_1: M24LR64E-R response delay

Upon detection of the rising edge of the EOF received from the VCD, the M24LR64E-R waits for a t_{1nom} time before transmitting its response to a VCD request or switching to the next slot during an inventory process. Values of t_1 are given in *Table 35*. The EOF is defined in *Figure 22*.

25.2 t_2: VCD new request delay

t_2 is the time after which the VCD may send an EOF to switch to the next slot when one or more M24LR64E-R responses have been received during an Inventory command. It starts from the reception of the EOF from the M24LR64E-Rs.

The EOF sent by the VCD may be either 10% or 100% modulated regardless of the modulation index used for transmitting the VCD request to the M24LR64E-R.

t_2 is also the time after which the VCD may send a new request to the M24LR64E-R, as described in *Figure 48*.

Values of t_2 are given in *Table 35*.

25.3 t_3: VCD new request delay when no response is received from the M24LR64E-R

t_3 is the time after which the VCD may send an EOF to switch to the next slot when no M24LR64E-R response has been received.

The EOF sent by the VCD may be either 10% or 100% modulated regardless of the modulation index used for transmitting the VCD request to the M24LR64E-R.

From the time the VCD has generated the rising edge of an EOF:

- If this EOF is 100% modulated, the VCD waits for a time at least equal to t_{3min} before sending a new EOF.
- If this EOF is 10% modulated, the VCD waits for a time at least equal to the sum of t_{3min} + the M24LR64E-R nominal response time (which depends on the M24LR64E-R data rate and subcarrier modulation mode) before sending a new EOF.

Table 35. Timing values(1)

	Minimum (min) values	Nominal (nom) values	Maximum (max) values
t_1	318.6 µs	320.9 µs	323.3 µs
t_2	309.2 µs	No t_{nom}	No t_{max}
t_3	t_{1max}(2) + t_{SOF}(3)	No t_{nom}	No t_{max}

1. The tolerance of specific timings is ± 32/fC.
2. t_{1max} does not apply for write-alike requests. Timing conditions for write-alike requests are defined in the command description.
3. t_{SOF} is the time taken by the M24LR64E-R to transmit an SOF to the VCD. t_{SOF} depends on the current data rate: High data rate or Low data rate.

26 Command codes

The M24LR64E-R supports the commands described in this section. Their codes are given in *Table 36*.

Table 36. Command codes

Command code standard	Function	Command code custom	Function
01h	Inventory	2Ch	Get Multiple Block Security Status
02h	Stay Quiet	B1h	Write-sector Password
20h	Read Single Block	B2h	Lock-sector
21h	Write Single Block	B3h	Present-sector Password
23h	Read Multiple Block	C0h	Fast Read Single Block
25h	Select	C1h	Fast Inventory Initiated
26h	Reset to Ready	C2h	Fast Initiate
27h	Write AFI	C3h	Fast Read Multiple Block
28h	Lock AFI	D1h	Inventory Initiated
29h	Write DSFID	D2h	Initiate
2Ah	Lock DSFID	A0h	ReadCfg
2Bh	Get System Info	A1h	WriteEHCfg
-	-	A2h	SetRstEHEn
-	-	A3h	CheckEHEn
-	-	A4h	WriteDOCfg

26.1 Inventory

When receiving the Inventory request, the M24LR64E-R runs the anticollision sequence. The Inventory_flag is set to 1. The meaning of flags 5 to 8 is shown in *Table 29*.

The request contains:

- the flags,
- the Inventory command code (see *Table 36*),
- the AFI if the AFI flag is set,
- the mask length,
- the mask value,
- the CRC.

The M24LR64E-R does not generate any answer in case of error.

Table 37. Inventory request format

Request SOF	Request_flags	Inventory	Optional AFI	Mask length	Mask value	CRC16	Request EOF
-	8 bits	01h	8 bits	8 bits	0 - 64 bits	16 bits	-

The response contains:

- the flags,
- the Unique ID.

Table 38. Inventory response format

Response SOF	Response_flags	DSFID	UID	CRC16	Response EOF
-	8 bits	8 bits	64 bits	16 bits	-

During an Inventory process, if the VCD does not receive an RF M24LR64E-R response, it waits for a time t_3 before sending an EOF to switch to the next slot. t_3 starts from the rising edge of the request EOF sent by the VCD.

- If the VCD sends a 100% modulated EOF, the minimum value of t_3 is:
  $t_3 min = 4384/f_C$ (323.3µs) + t_{SOF}
- If the VCD sends a 10% modulated EOF, the minimum value of t_3 is:
  $t_3 min = 4384/f_C$ (323.3µs) + t_{NRT}

where:

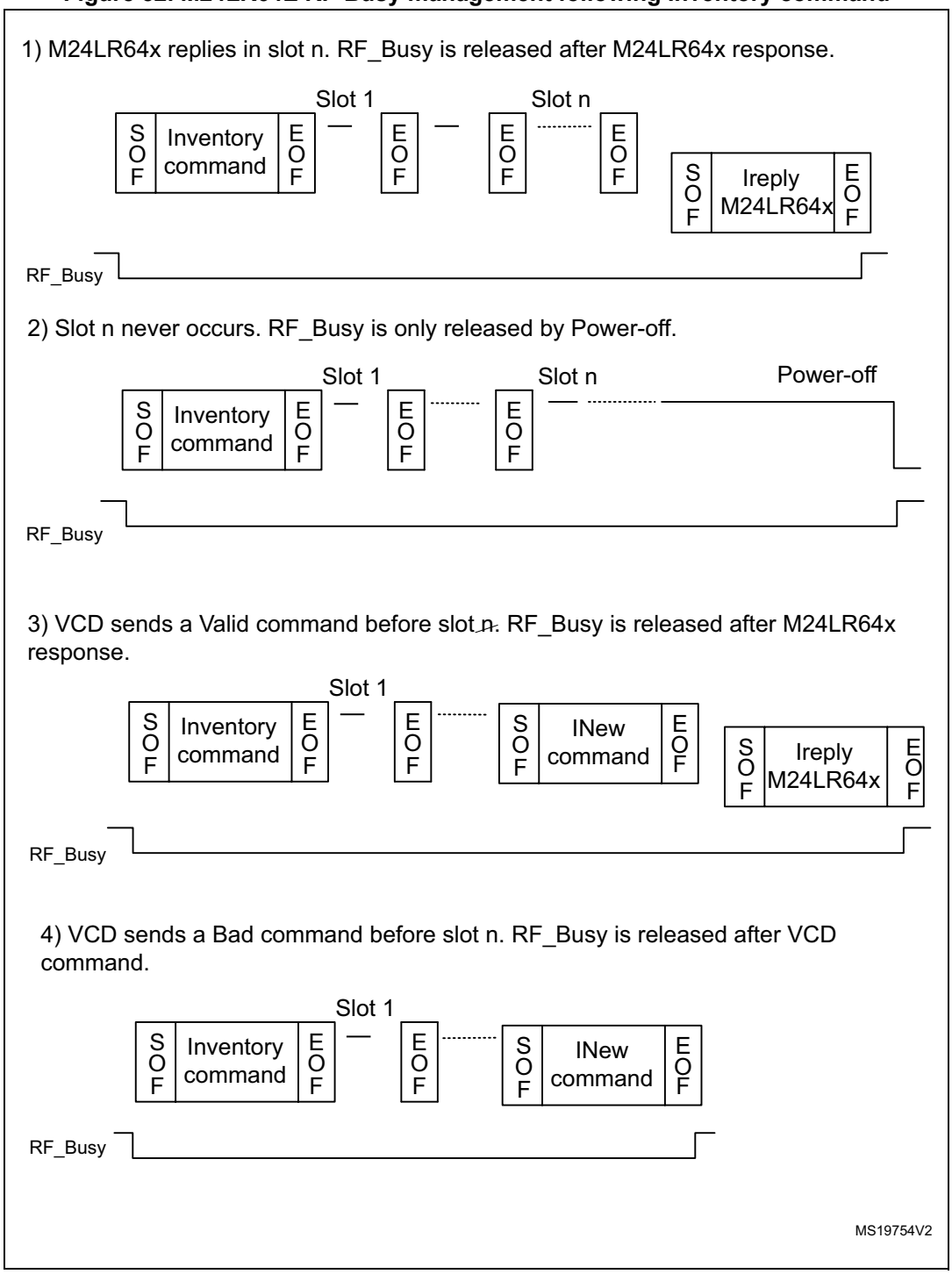
- t_{SOF} is the time required by the M24LR64E-R to transmit an SOF to the VCD,
- t_{NRT} is the nominal response time of the M24LR64E-R.

t_{NRT} and t_{SOF} are dependent on the M24LR64E-R-to-VCD data rate and subcarrier modulation mode.

When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF starting the inventory command to the end of the M24LR64E-R response. If the M24LR64E-R does not receive the corresponding slot marker, the RF WIP/BUSY pin remains at 0 until the next RF power-off.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

Figure 52. M24LR64E RF-Busy management following Inventory command



26.2 Stay Quiet

Command code = 0x02

On receiving the Stay Quiet command, the M24LR64E-R enters the Quiet state if no error occurs, and does NOT send back a response. There is NO response to the Stay Quiet command even if an error occurs.

When in the Quiet state:

- the M24LR64E-R does not process any request if the Inventory_flag is set,
- the M24LR64E-R processes any Addressed request.

The M24LR64E-R exits the Quiet state when:

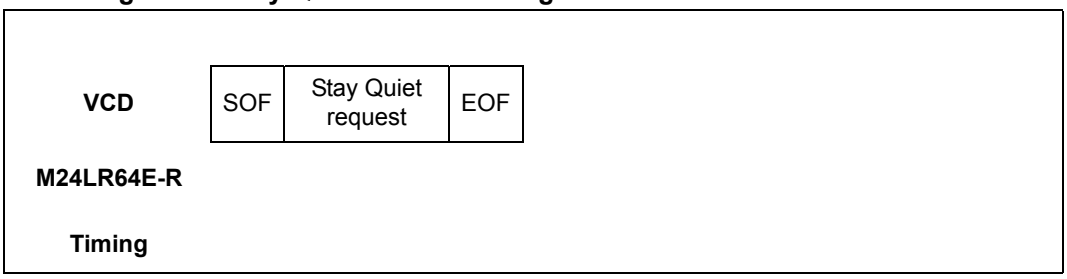
- it is reset (power off),
- receiving a Select request. It then goes to the Selected state,
- receiving a Reset to Ready request. It then goes to the Ready state.

Table 39. Stay Quiet request format

Request SOF	Request flags	Stay Quiet	UID	CRC16	Request EOF
-	8 bits	02h	64 bits	16 bits	-

The Stay Quiet command must always be executed in Addressed mode (Select_flag is reset to 0 and Address_flag is set to 1).

Figure 53. Stay Quiet frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 during the Stay Quiet command.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

26.3 Read Single Block

On receiving the Read Single Block command, the M24LR64E-R reads the requested block and sends back its 32-bit value in the response. The Protocol_extension_flag should be set to 1 for the M24LR64E-R to operate correctly. If the Protocol_extension_flag is at 0, the M24LR64E-R answers with an error code. The Option_flag is supported.

Table 40. Read Single Block request format

Request SOF	Request_flags	Read Single Block	UID(1)	Block number	CRC16	Request EOF
-	8 bits	20h	64 bits	16 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameters:

- Request flags
- UID (optional)
- Block number

Table 41. Read Single Block response format when Error_flag is NOT set

Response SOF	Response_flags	Sector security status(1)	Data	CRC16	Response EOF
-	8 bits	8 bits	32 bits	16 bits	-

1. Gray color means that the field is optional.

Response parameters:

- Sector security status if Option_flag is set (see *Table 42*)
- Four bytes of block data

Table 42. Sector security status

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Reserved for future use. All at 0.			Password control bits		Read / Write protection bits		0: Current sector not locked 1: Current sector locked

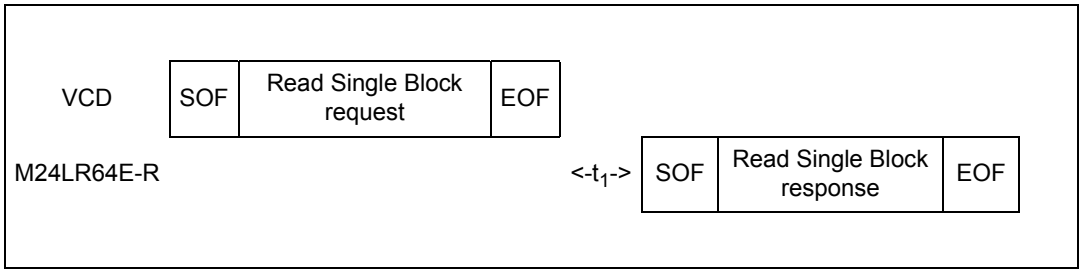
Table 43. Read Single Block response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set
  - 10h: the specified block is not available
  - 15h: the specified block is read-protected

Figure 54. Read Single Block frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Read Single Block command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

26.4 Write Single Block

On receiving the Write Single Block command, the M24LR64E-R writes the data contained in the request to the requested block and reports whether the write operation was successful in the response. The Protocol_extension_flag should be set to 1 for the M24LR64E-R to operate correctly. If the Protocol_extension_flag is at 0, the M24LR64E-R answers with an error code. The Option_flag is supported.

During the RF write cycle W_t, there should be no modulation (neither 100% nor 10%), otherwise the M24LR64E-R may not program correctly the data into the memory. The W_t time is equal to t_{1nom} + 18 × 302 µs.

Table 44. Write Single Block request format

Request SOF	Request_flags	Write Single Block	UID(1)	Block number	Data	CRC16	Request EOF
-	8 bits	21h	64 bits	16 bits	32 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameters:

- Request flags
- UID (optional)
- Block number
- Data

Table 45. Write Single Block response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter. The response is sent back after the writing cycle.

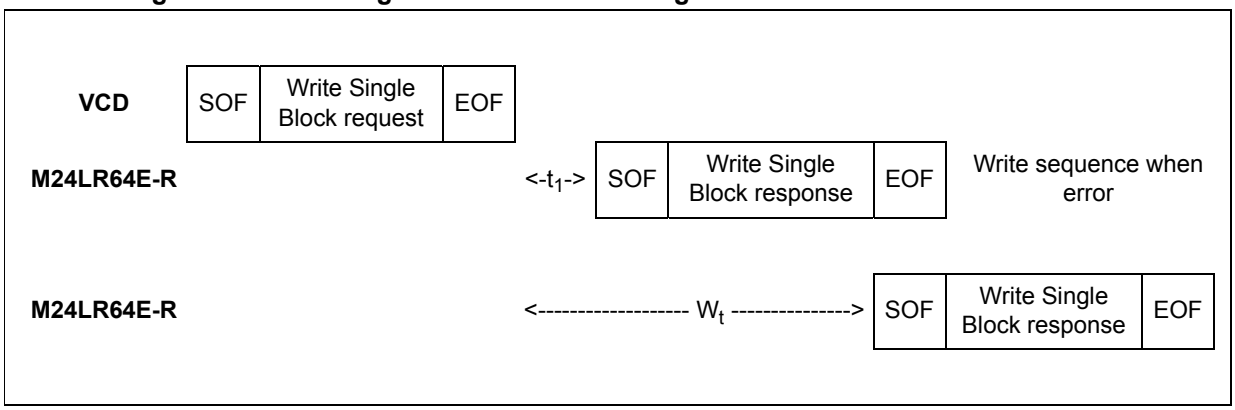
Table 46. Write Single Block response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 0Fh: error with no information given
  - 10h: the specified block is not available
  - 12h: the specified block is locked and its contents cannot be changed
  - 13h: the specified block was not successfully programmed

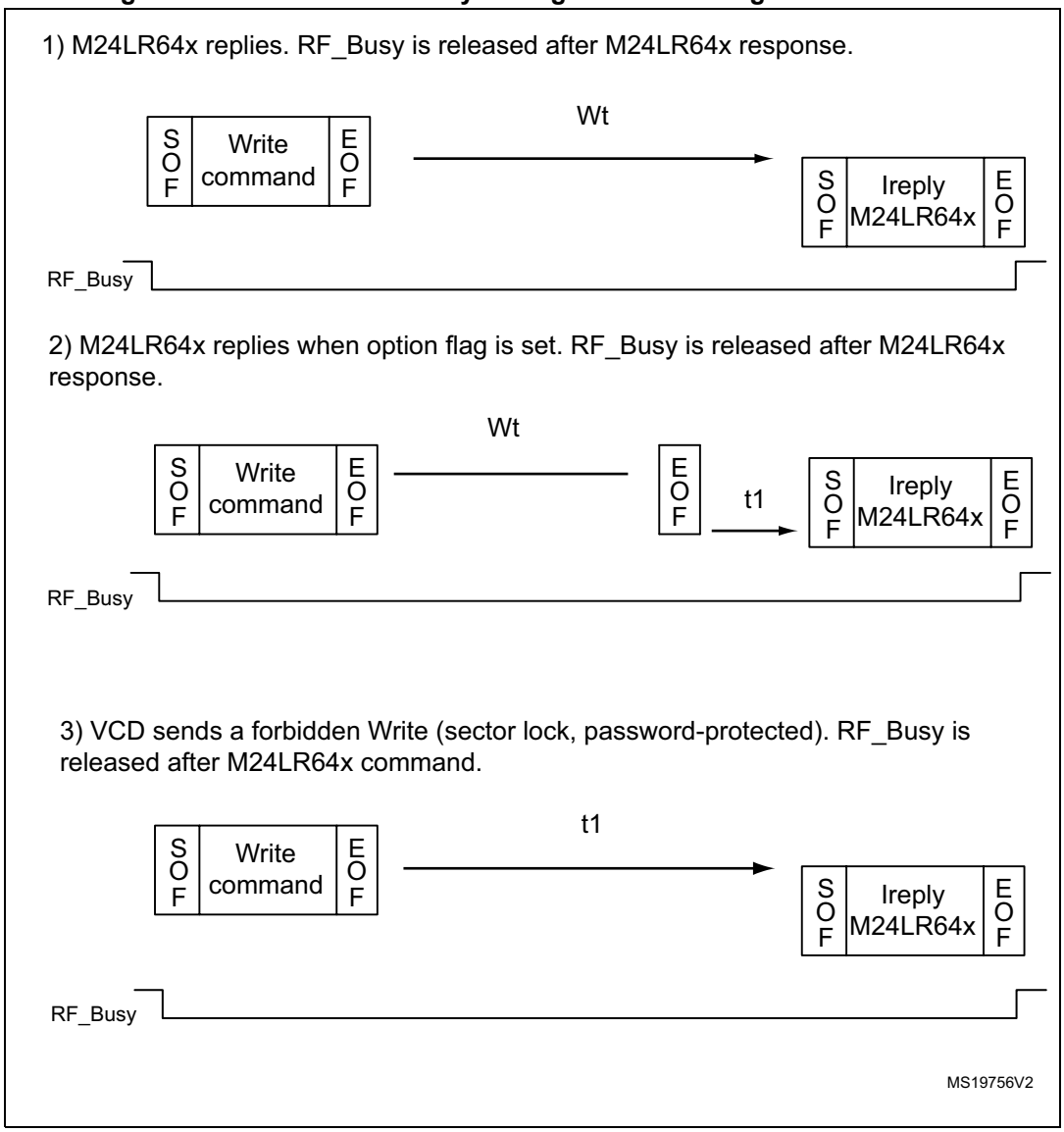
Figure 55. Write Single Block frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Write Single Block command to the end of the M24LR64E-R response.

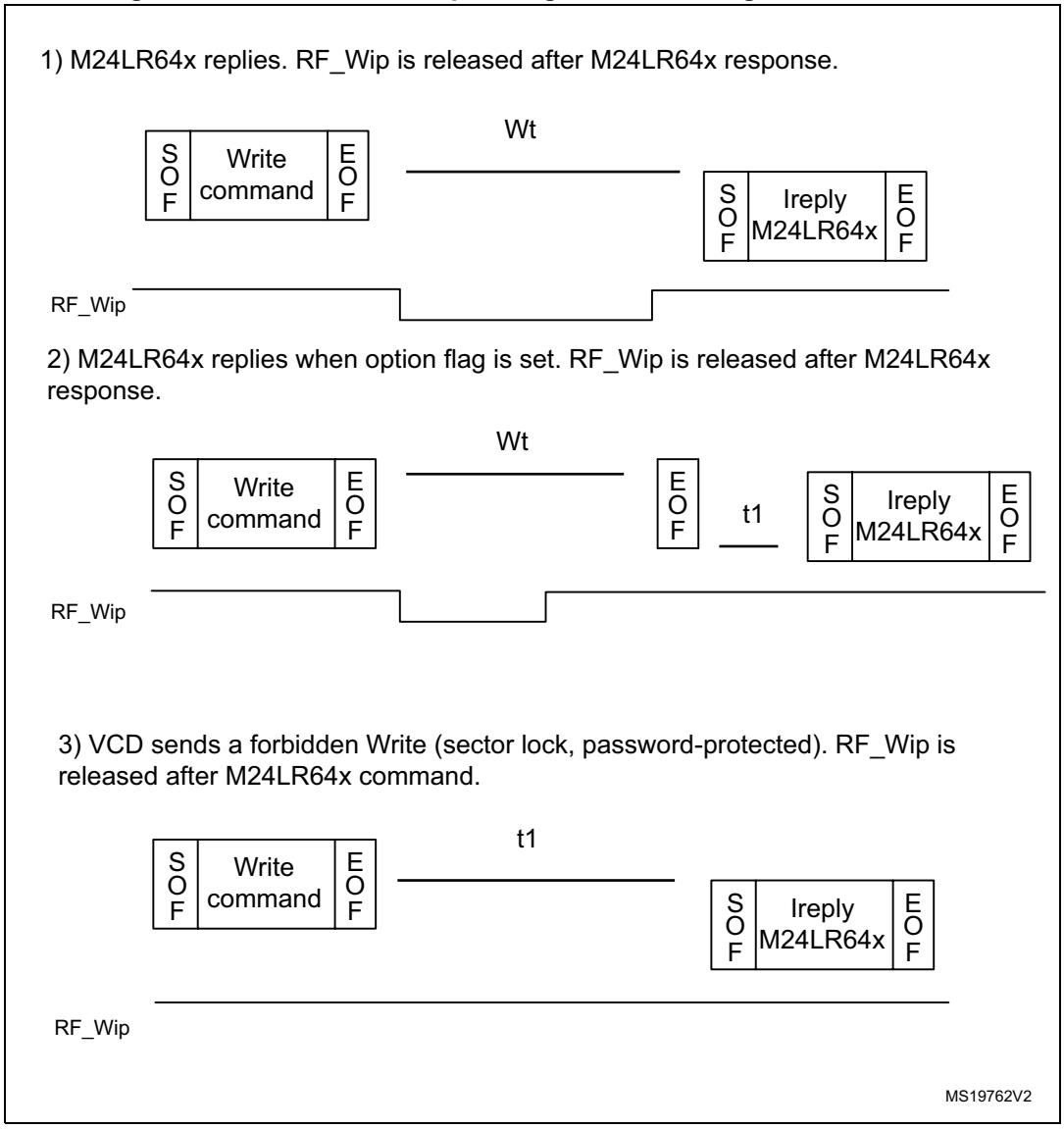
When configured in the RF write in progress mode, the RF WIP/BUSY pin is tied to 0 for the duration of the internal write cycle (from the end of a valid write single block command to the beginning of the M24LR64E-R response).

Figure 56. M24LR64E RF-Busy management following Write command



When configuring in the RF Write in progress mode, the RF WIP/BUSY pin is tied to 0 during the Write & verify sequence, as shown in *Figure 57*.

Figure 57. M24LR64E RF-Wip management following Write command



26.5 Read Multiple Block

When receiving the Read Multiple Block command, the M24LR64E-R reads the selected blocks and sends back their value in multiples of 32 bits in the response. The blocks are numbered from 00h to 1FFh in the request and the value is minus one (–1) in the field. For example, if the “Number of blocks” field contains the value 06h, seven blocks are read. The maximum number of blocks is fixed at 32 assuming that they are all located in the same sector. If the number of blocks overlaps sectors, the M24LR64E-R returns an error code.

The Protocol_extension_flag should be set to 1 for the M24LR64E-R to operate correctly. If the Protocol_extension_flag is at 0, the M24LR64E-R answers with an error code. The Option_flag is supported.

Table 47. Read Multiple Block request format

Request SOF	Request_ flags	Read Multiple Block	UID(1)	First block number	Number of blocks	CRC16	Request EOF
-	8 bits	23h	64 bits	16 bits	8 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameters:

- Request flags
- UID (optional)
- First block number
- Number of blocks

Table 48. Read Multiple Block response format when Error_flag is NOT set

Response SOF	Response_ flags	Sector security status(1)	Data	CRC16	Response EOF
-	8 bits	8 bits(2)	32 bits(2)	16 bits	-

1. Gray color means that the field is optional.
2. Repeated as needed.

Response parameters:

- Sector security status if Option_flag is set (see *Table 49*)
- N blocks of data

Table 49. Sector security status

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Reserved for future use. All at 0.			Password control bits		Read / Write protection bits		0: Current sector not locked 1: Current sector locked

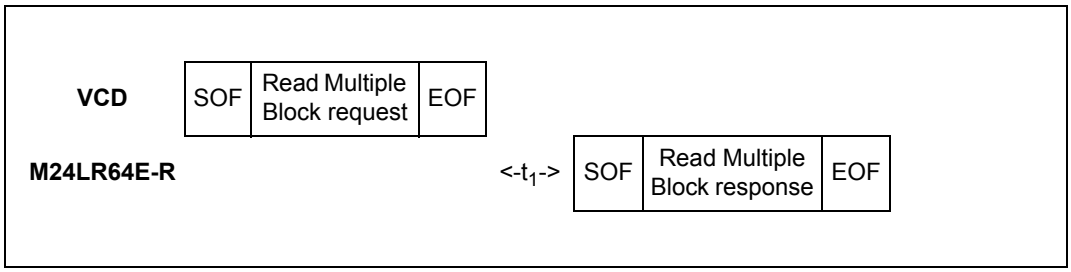
Table 50. Read Multiple Block response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 0Fh: error with no information given
  - 10h: the specified block is not available
  - 15h: the specified block is read-protected

Figure 58. Read Multiple Block frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Read Multiple Block command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

26.6 Select

When receiving the Select command:

- If the UID is equal to its own UID, the M24LR64E-R enters or stays in the Selected state and sends a response.
- If the UID does not match its own UID, the selected M24LR64E-R returns to the Ready state and does not send a response.

The M24LR64E-R answers an error code only if the UID is equal to its own UID. If not, no response is generated. If an error occurs, the M24LR64E-R remains in its current state.

Table 51. Select request format

Request SOF	Request_flags	Select	UID	CRC16	Request EOF
-	8 bits	25h	64 bits	16 bits	-

Request parameter:

- UID

Table 52. Select Block response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter

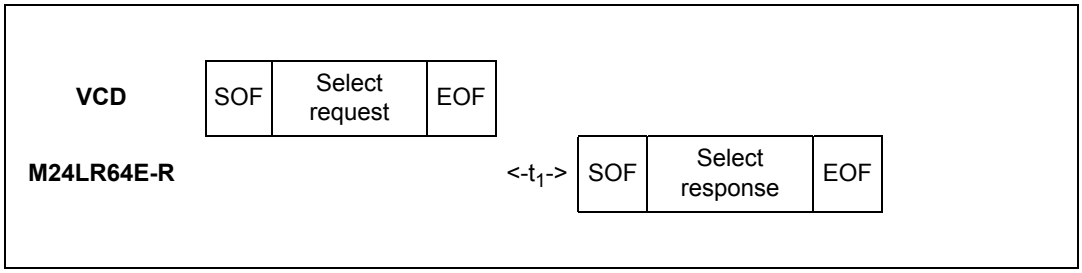
Table 53. Select response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 03h: the option is not supported

Figure 59. Select frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Select command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

26.7 Reset to Ready

On receiving a Reset to Ready command, the M24LR64E-R returns to the Ready state if no error occurs. In the Addressed mode, the M24LR64E-R answers an error code only if the UID is equal to its own UID. If not, no response is generated.

Table 54. Reset to Ready request format

Request SOF	Request_flags	Reset to Ready	UID(1)	CRC16	Request EOF
-	8 bits	26h	64 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameter:

- UID (optional)

Table 55. Reset to Ready response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter

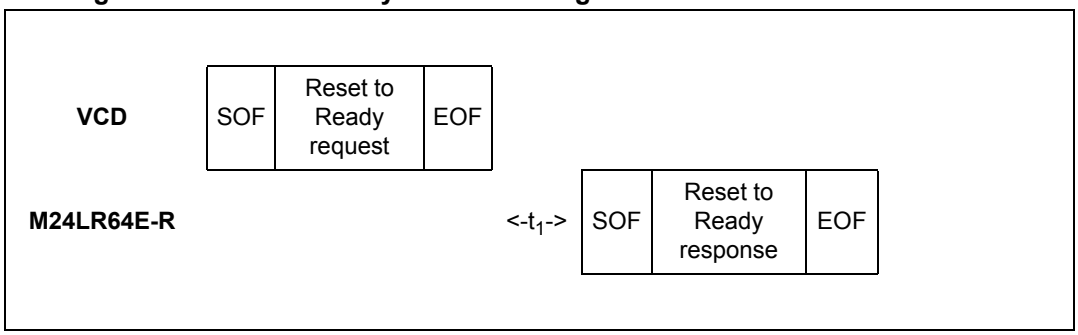
Table 56. Reset to ready response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 03h: the option is not supported

Figure 60. Reset to Ready frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Reset to ready command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

26.8 Write AFI

On receiving the Write AFI request, the M24LR64E-R programs the 8-bit AFI value to its memory. The Option_flag is supported.

During the RF write cycle W_t, there should be no modulation (neither 100% nor 10%), otherwise the M24LR64E-R may not write correctly the AFI value into the memory. The W_t time is equal to t_{1nom} + 18 × 302 µs.

Table 57. Write AFI request format

Request SOF	Request_flags	Write AFI	UID(1)	AFI	CRC16	Request EOF
-	8 bits	27h	64 bits	8 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameter:

- Request flags
- UID (optional)
- AFI

Table 58. Write AFI response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter

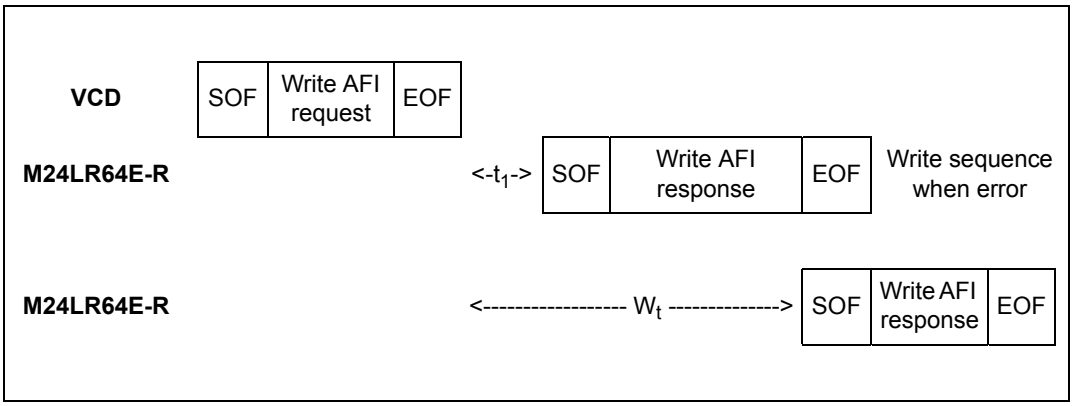
Table 59. Write AFI response format when Error_flag is set

Response SOF	Response_ flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set
  - 12h: the specified block is locked and its contents cannot be changed
  - 13h: the specified block was not successfully programmed

Figure 61. Write AFI frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Write AFI command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin is tied to 0 for the duration of the internal write cycle (from the end of a valid Write AFI command to the beginning of the M24LR64E-R response).

26.9 Lock AFI

On receiving the Lock AFI request, the M24LR64E-R locks the AFI value permanently. The Option_flag is supported.

During the RF write cycle W_t, there should be no modulation (neither 100% nor 10%), otherwise the M24LR64E-R may not lock correctly the AFI value in memory. The W_t time is equal to t_{1nom} + 18 × 302 µs.

Table 60. Lock AFI request format

Request SOF	Request_flags	Lock AFI	UID(1)	CRC16	Request EOF
-	8 bits	28h	64 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameter:

- Request Flags
- UID (optional)

Table 61. Lock AFI response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter

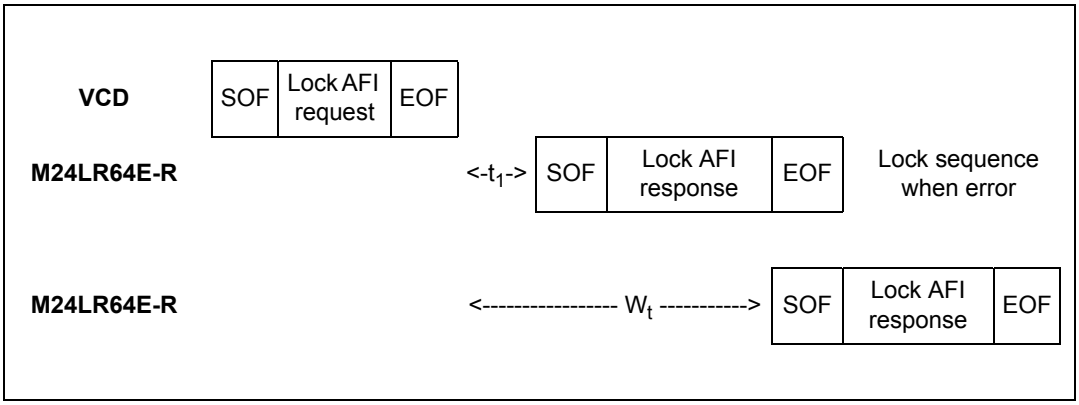
Table 62. Lock AFI response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set
  - 11h: the specified block is already locked and thus cannot be locked again
  - 14h: the specified block was not successfully locked

Figure 62. Lock AFI frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Lock AFI command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin is tied to 0 for the entire duration of the internal write cycle (from the end of valid Lock AFI command to the beginning of the M24LR64E-R response).

26.10 Write DSFID

On receiving the Write DSFID request, the M24LR64E-R programs the 8-bit DSFID value to its memory. The Option_flag is supported.

During the RF write cycle W_t, there should be no modulation (neither 100% nor 10%), otherwise the M24LR64E-R may not write correctly the DSFID value in memory. The W_t time is equal to t_{1nom} + 18 × 302 µs.

Table 63. Write DSFID request format

Request SOF	Request_flags	Write DSFID	UID(1)	DSFID	CRC16	Request EOF
-	8 bits	29h	64 bits	8 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameter:

- Request flags
- UID (optional)
- DSFID

Table 64. Write DSFID response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter

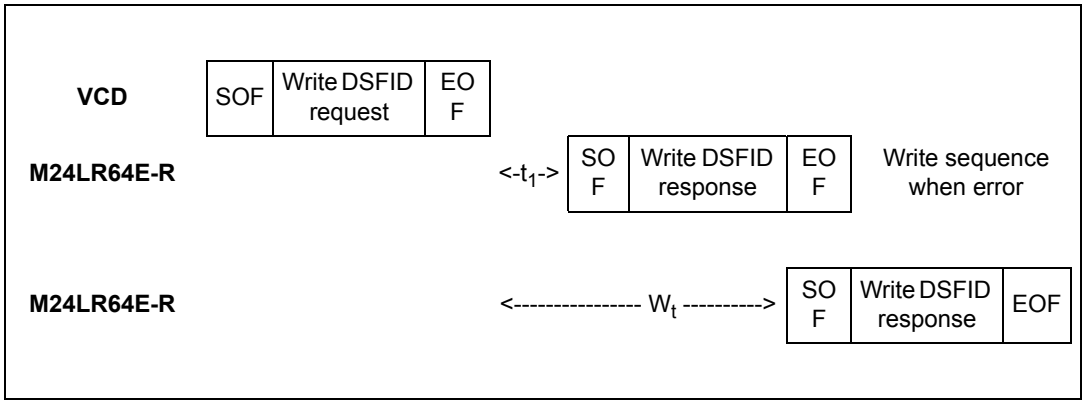
Table 65. Write DSFID response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set
  - 12h: the specified block is locked and its contents cannot be changed
  - 13h: the specified block was not successfully programmed

Figure 63. Write DSFID frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Write DSFID command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin is tied to 0 for the duration of the internal write cycle (from the end of a valid Write DSFID command to the beginning of the M24LR64E-R response).

26.11 Lock DSFID

On receiving the Lock DSFID request, the M24LR64E-R locks the DSFID value permanently. The Option_flag is supported.

During the RF write cycle W_t, there should be no modulation (neither 100% nor 10%), otherwise the M24LR64E-R may not lock correctly the DSFID value in memory. The W_t time is equal to t_{1nom} + 18 × 302 µs.

Table 66. Lock DSFID request format

Request SOF	Request_flags	Lock DSFID	UID(1)	CRC16	Request EOF
-	8 bits	2Ah	64 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameter:

- Request flags
- UID (optional)

Table 67. Lock DSFID response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter.

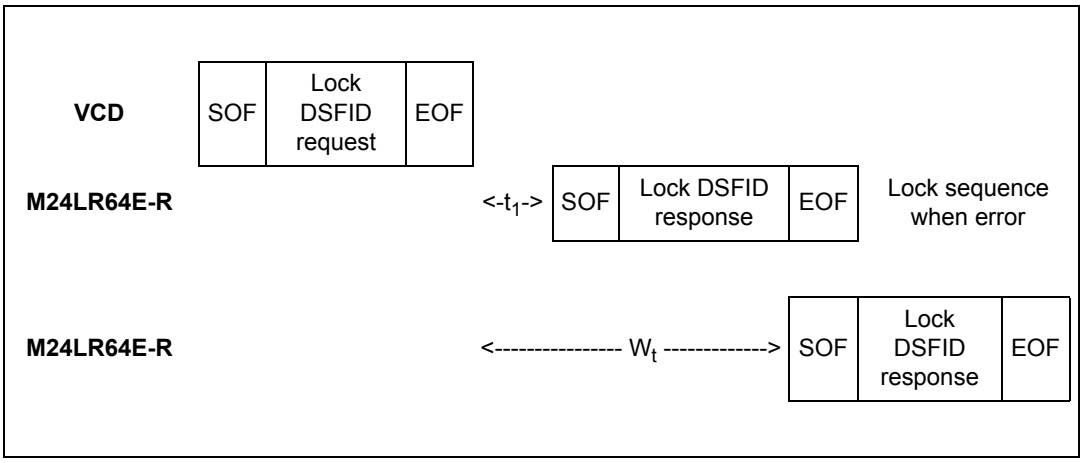
Table 68. Lock DSFID response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 11h: the specified block is already locked and thus cannot be locked again
  - 14h: the specified block was not successfully locked

Figure 64. Lock DSFID frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Lock DSFID command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin is tied to 0 for the duration of the internal write cycle (from the end of a valid Lock DSFID command to the beginning of the M24LR64E-R response).

26.12 Get System Info

When receiving the Get System Info command, the M24LR64E-R sends back its information data in the response. The Option_flag is not supported. The Get System Info can be issued in both Addressed and Non Addressed modes.

The Protocol_extension_flag can be set to 0 or 1. *Table 70* and *Table 72* show M24LR64E-R response to the Get System Info command depending on the value of the Protocol_extension_flag.

Table 69. Get System Info request format

Request SOF	Request_flags	Get System Info	UID(1)	CRC16	Request EOF
-	8 bits	2Bh	64 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameter:

- Request flags
- UID (optional)

Table 70. Get System Info response format when Protocol_extension_flag = 0 and Error_flag is NOT set

Response SOF	Response_ flags	Information flags	UID	DSFID	AFI	IC ref.	CRC16	Response EOF
-	00h	0Bh	64 bits	8 bits	8 bits	5Eh	16 bits	-

Response parameters:

- Information flags set to 0Ch. DSFID, AFI and IC reference fields are present.
- UID code on 64 bits
- DSFID value
- AFI value
- M24LR64E-R IC reference: the 8 bits are significant.

Table 71. Get System Info response format when Protocol_extension_flag = 1 and Error_flag is NOT set

Response SOF	Response _flags	Information flags	UID	DSFID	AFI	Memory size	IC ref	CRC16	Response EOF
-	00h	0Fh	64 bits	8 bits	8 bits	03 07FFh	5Eh	16 bits	-

Response parameters:

- Information flags set to 0Fh. DSFID, AFI, Memory Size and IC reference fields are present.
- UID code on 64 bits
- DSFID value
- AFI value
- Memory size. The M24LR64E-R provides 2048 blocks (07FFh) of 4 bytes (03h)
- IC reference: the 8 bits are significant.

Table 72. Get System Info response format when Error_flag is set

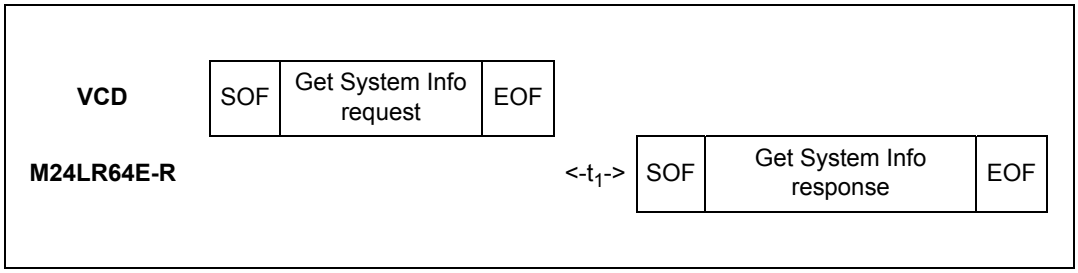
Response SOF	Response_flags	Error code	CRC16	Response EOF
-	01h	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 03h: Option not supported

.

Figure 65. Get System Info frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Get System Info command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

26.13 Get Multiple Block Security Status

When receiving the Get Multiple Block Security Status command, the M24LR64E-R sends back the sector security status. The blocks are numbered from 00h to 01FFh in the request and the value is minus one (–1) in the field. For example, a value of '06' in the “Number of blocks” field requests to return the security status of seven blocks.

The Protocol_extension_flag should be set to 1 for the M24LR64E-R to operate correctly. If the Protocol_extension_flag is at 0, the M24LR64E-R answers with an error code.

During the M24LR64E-R response, if the internal block address counter reaches 01FFh, it rolls over to 0000h and the Sector Security Status bytes for that location are sent back to the reader.

Table 73. Get Multiple Block Security Status request format

Request SOF	Request _flags	Get Multiple Block Security Status	UID(1)	First block number	Number of blocks	CRC16	Request EOF
-	8 bits	2Ch	64 bits	16 bits	16 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameter:

- Request flags
- UID (optional)
- First block number
- Number of blocks

Table 74. Get Multiple Block Security Status response format when Error_flag is NOT set

Response SOF	Response_flags	Sector security status	CRC16	Response EOF
-	8 bits	8 bits(1)	16 bits	-

1. Repeated as needed.

Response parameters:

- Sector security status (see *Table 75*)

Table 75. Sector security status

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Reserved for future use All at 0			Password control bits		Read / Write protection bits		0: Current sector not locked 1: Current sector locked

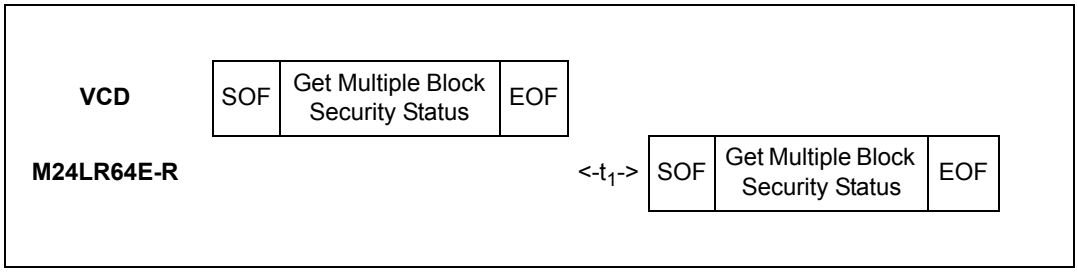
Table 76. Get Multiple Block Security Status response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 03h: the option is not supported
  - 10h: the specified block is not available

Figure 66. Get Multiple Block Security Status frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Get Multiple Block Security Status command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

26.14 Write-sector Password

On receiving the Write-sector Password command, the M24LR64E-R uses the data contained in the request to write the password and reports whether the operation was successful in the response. The Option_flag is supported.

During the RF write cycle time, W_t, there must be no modulation at all (neither 100% nor 10%), otherwise the M24LR64E-R may not correctly program the data into the memory.

The W_t time is equal to t_{1nom} + 18 × 302 µs. After a successful write, the new value of the selected password is automatically activated. It is not required to present the new password value until M24LR64E-R power-down.

Table 77. Write-sector Password request format

Request SOF	Request _flags	Write-sector password	IC Mfg code	UID(1)	Password number	Data	CRC16	Request EOF
-	8 bits	B1h	02h	64 bits	8 bits	32 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameter:

- Request flags
- UID (optional)
- Password number (01h = Pswd1, 02h = Pswd2, 03h = Pswd3, other = Error)
- Data

Table 78. Write-sector Password response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- no parameter.

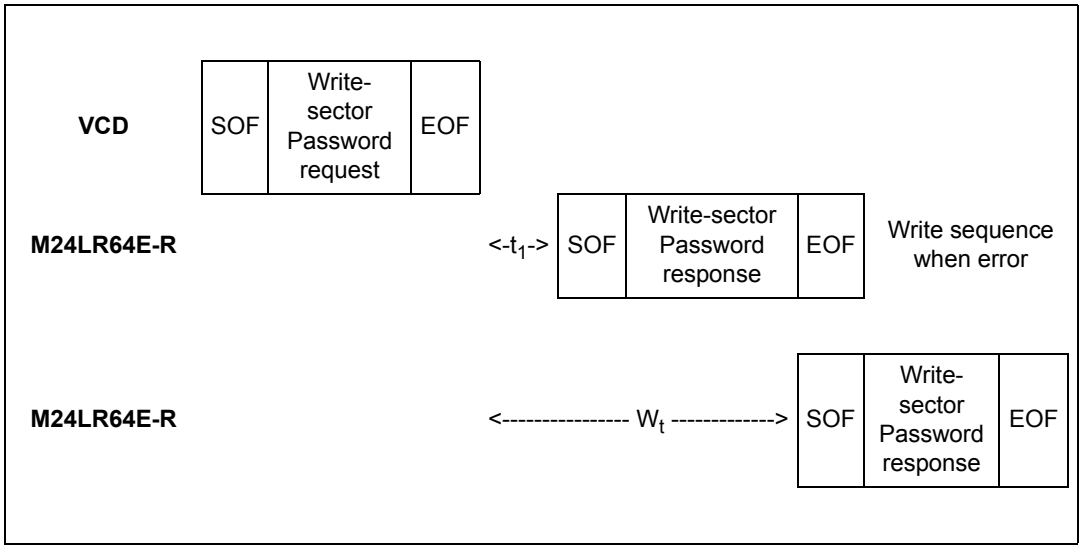
Table 79. Write-sector Password response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 10h: the password number is incorrect
  - 12h: the session was not opened before the password update
  - 13h: the specified block was not successfully programmed
  - 0Fh: the presented password is incorrect

Figure 67. Write-sector Password frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Write-sector Password command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin is tied to 0 for the duration of the internal write cycle (from the end of a valid Write sector password command to the beginning of the M24LR64E-R response).

26.15 Lock-sector

On receiving the Lock-sector command, the M24LR64E-R sets the access rights and permanently locks the selected sector. The Option_flag is supported.

A sector is selected by giving the address of one of its blocks in the Lock-sector request (Sector number field). For example, addresses 0 to 31 are used to select sector 0 and addresses 32 to 63 are used to select sector 1. Care must be taken when issuing the Lock-sector command as all the blocks belonging to the same sector are automatically locked by a single command.

The Protocol_extension_flag should be set to 1 for the M24LR64E-R to operate correctly. If the Protocol_extension_flag is at 0, the M24LR64E-R answers with an error code.

During the RF write cycle W_t, there should be no modulation (neither 100% nor 10%), otherwise the M24LR64E-R may not correctly lock the memory block. The W_t time is equal to t_{1nom} + 18 × 302 µs.

Table 80. Lock-sector request format

Request SOF	Request _flags	Lock-sector	IC Mfg code	UID(1)	Sector number	Sector security status	CRC16	Request EOF
-	8 bits	B2h	02h	64 bits	16 bits	8 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameters:

- Request flags
- (optional) UID
- Sector number
- Sector security status (refer to *Table 81*)

Table 81. Sector security status

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	0	0	Password control bits		Read / Write protection bits		1

Table 82. Lock-sector response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter

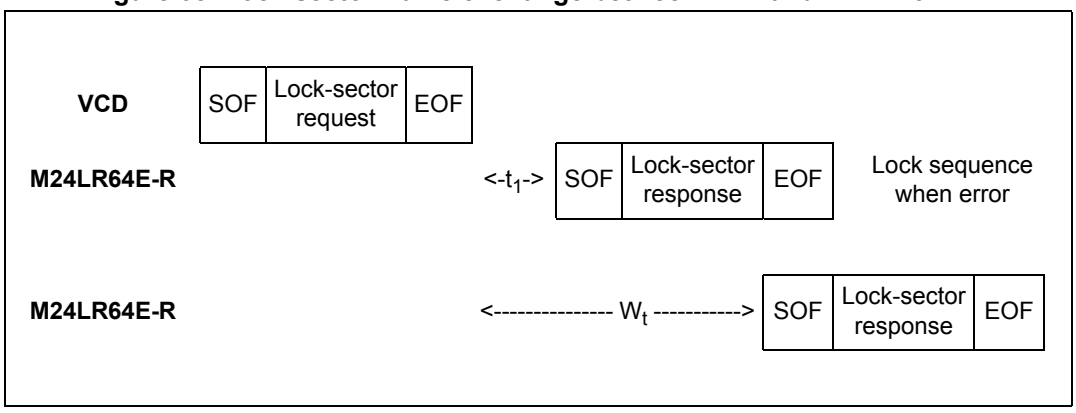
Table 83. Lock-sector response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 10h: the specified block is not available
  - 11h: the specified block is already locked and thus cannot be locked again
  - 14h: the specified block was not successfully locked

Figure 68. Lock-sector frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Lock-sector command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin is tied to 0 for the duration of the internal write cycle (from the end of a valid Lock sector command to the beginning of the M24LR64E-R response).

26.16 Present-sector Password

On receiving the Present-sector Password command, the M24LR64E-R compares the requested password with the data contained in the request and reports whether the operation has been successful in the response. The Option_flag is supported.

During the comparison cycle equal to W_t, there should be no modulation (neither 100% nor 10%), otherwise the M24LR64E-R Password value may not be correctly compared. The W_t time is equal to t_{1nom} + 18 × 302 µs.

After a successful command, the access to all the memory blocks linked to the password is changed as described in *Section 4.1: M24LR64E-R block security in RF mode*.

Table 84. Present-sector Password request format

Request SOF	Request _flags	Present-sector Password	IC Mfg code	UID(1)	Password number	Password	CRC16	Request EOF
-	8 bits	B3h	02h	64 bits	8 bits	32 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameter:

- Request flags
- UID (optional)
- Password Number (0x01 = Pswd1, 0x02 = Pswd2, 0x03 = Pswd3, other = Error)
- Password

Table 85. Present-sector Password response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter. The response is sent back after the write cycle.

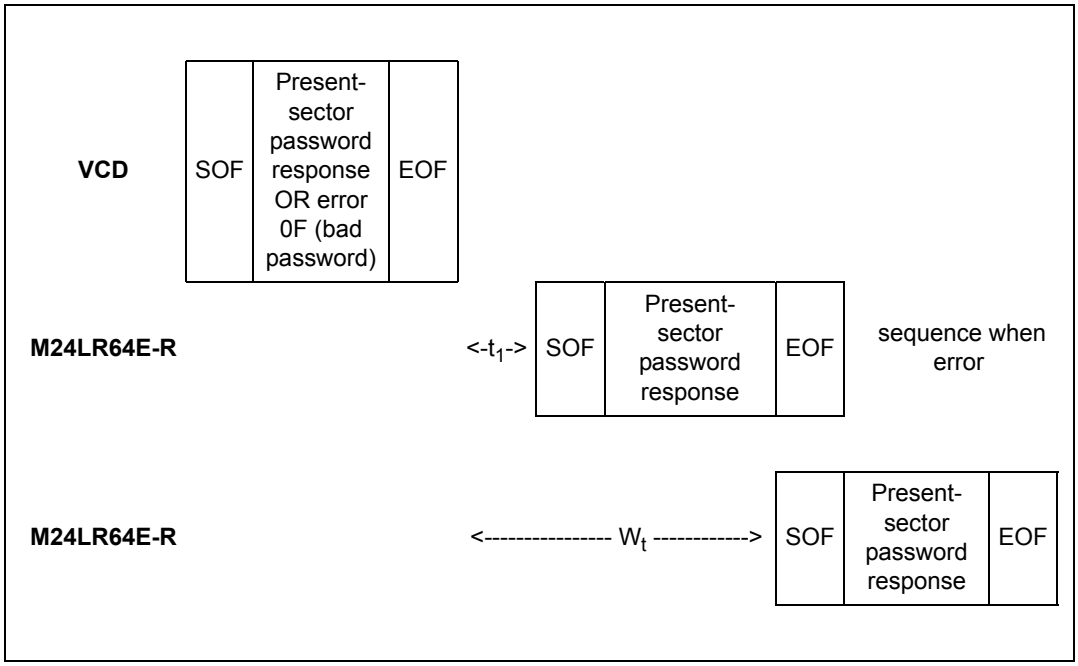
Table 86. Present-sector Password response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 10h: the password number is incorrect
  - 0Fh: the present password is incorrect

Figure 69. Present-sector Password frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Present Sector Password command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY remains in high-Z state.

26.17 Fast Read Single Block

On receiving the Fast Read Single Block command, the M24LR64E-R reads the requested block and sends back its 32-bit value in the response. The Option_flag is supported. The data rate of the response is multiplied by 2.

The Protocol_extension_flag should be set to 1 for the M24LR64E-R to operate correctly. If the Protocol_extension_flag is at 0, the M24LR64E-R answers with an error code.

The subcarrier_flag should be set to 0, otherwise the M24LR64E-R answers with an error code.

Table 87. Fast Read Single Block request format

Request SOF	Request_flags	Fast Read Single Block	IC Mfg code	UID(1)	Block number	CRC16	Request EOF
-	8 bits	C0h	02h	64 bits	16 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameters:

- Request flags
- UID (optional)
- Block number

Table 88. Fast Read Single Block response format when Error_flag is NOT set

Response SOF	Response_flags	Sector security status(1)	Data	CRC16	Response EOF
-	8 bits	8 bits	32 bits	16 bits	-

1. Gray color means that the field is optional.

Response parameters:

- Sector security status if Option_flag is set (see *Table 89*)
- Four bytes of block data

Table 89. Sector security status

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Reserved for future use All at 0			Password control bits		Read / Write protection bits		0: Current sector not locked 1: Current sector locked

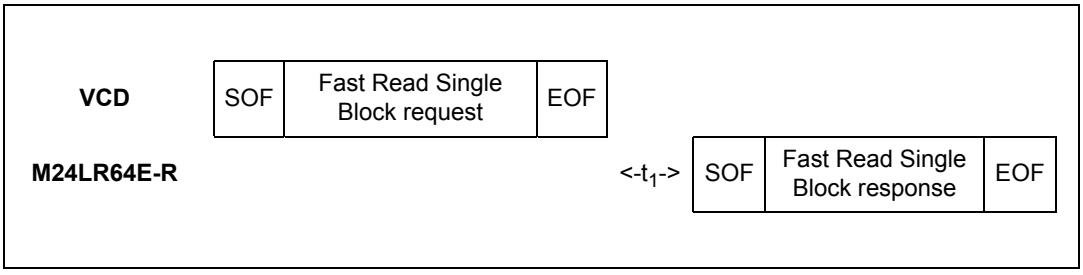
Table 90. Fast Read Single Block response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 10h: the specified block is not available
  - 15h: the specified block is read-protected

Figure 70. Fast Read Single Block frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Fast Read Single block command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

26.18 Fast Inventory Initiated

Before receiving the Fast Inventory Initiated command, the M24LR64E-R must have received an Initiate or a Fast Initiate command in order to set the Initiate_ flag. If not, the M24LR64E-R does not answer the Fast Inventory Initiated command.

The subcarrier_flag should be set to 0, otherwise the M24LR64E-R answers with an error code.

On receiving the Fast Inventory Initiated request, the M24LR64E-R runs the anticollision sequence. The Inventory_flag must be set to 1. The meaning of flags 5 to 8 is shown in *Table 29*. The data rate of the response is multiplied by 2.

The request contains:

- the flags,
- the Inventory command code,
- the AFI if the AFI flag is set,
- the mask length,
- the mask value,
- the CRC.

The M24LR64E-R does not generate any answer in case of error.

Table 91. Fast Inventory Initiated request format

Request SOF	Request _flags	Fast Inventory Initiated	IC Mfg code	Optional AFI	Mask length	Mask value	CRC16	Request EOF
-	8 bits	C1h	02h	8 bits	8 bits	0 - 64 bits	16 bits	-

The Response contains:

- the flags,
- the Unique ID.

Table 92. Fast Inventory Initiated response format

Response SOF	Response_flags	DSFID	UID	CRC16	Response EOF
-	8 bits	8 bits	64 bits	16 bits	-

During an Inventory process, if the VCD does not receive an RF M24LR64E-R response, it waits for a time t_3 before sending an EOF to switch to the next slot. t_3 starts from the rising edge of the request EOF sent by the VCD.

- If the VCD sends a 100% modulated EOF, the minimum value of t_3 is:
  $t_3 min = 4384/f_C$ (323.3µs) + t_{SOF}
- If the VCD sends a 10% modulated EOF, the minimum value of t_3 is:
  $t_3 min = 4384/f_C$ (323.3µs) + t_{NRT}

where:

- t_{SOF} is the time required by the M24LR64E-R to transmit an SOF to the VCD
- t_{NRT} is the nominal response time of the M24LR64E-R

t_{NRT} and t_{SOF} are dependent on the M24LR64E-R-to-VCD data rate and subcarrier modulation mode.

When configured in the RF busy mode, the RF WIP/BUSY pin is driven to 0 from the SOF starting the inventory command to the end of the M24LR64E-R response. If the M24LR64E-R does not receive the corresponding slot marker, the RF WIP/BUSY pin remains at 0 until the next RF power-off.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

26.19 Fast Initiate

On receiving the Fast Initiate command, the M24LR64E-R sets the internal Initiate_flag and sends back a response only if it is in the Ready state. The command has to be issued in the Non Addressed mode only (Select_flag is reset to 0 and Address_flag is reset to 0). If an error occurs, the M24LR64E-R does not generate any answer. The Initiate_flag is reset after a power-off of the M24LR64E-R. The data rate of the response is multiplied by 2.

The subcarrier_flag should be set to 0, otherwise the M24LR64E-R answers with an error code.

The request contains:

- No data

Table 93. Fast Initiate request format

Request SOF	Request_flags	Fast Initiate	IC Mfg Code	CRC16	Request EOF
-	8 bits	C2h	02h	16 bits	-

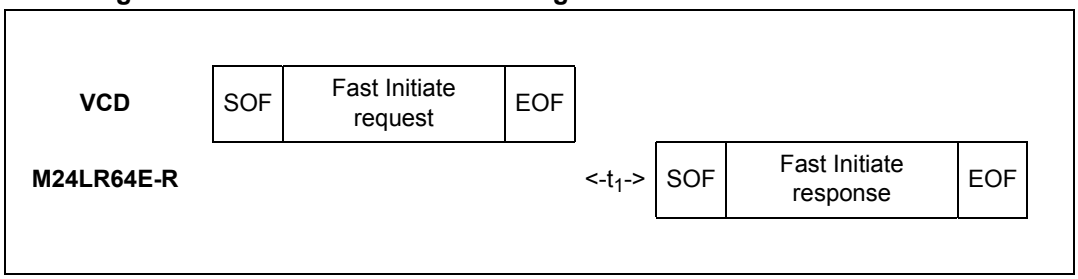
The response contains:

- the flags,
- the Unique ID.

Table 94. Fast Initiate response format

Response SOF	Response_flags	DSFID	UID	CRC16	Response EOF
-	8 bits	8 bits	64 bits	16 bits	-

Figure 71. Fast Initiate frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Fast Initiate command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

26.20 Fast Read Multiple Block

On receiving the Fast Read Multiple Block command, the M24LR64E-R reads the selected blocks and sends back their value in multiples of 32 bits in the response. The blocks are numbered from 00h to 1FFh in the request and the value is minus one (–1) in the field. For example, if the “Number of blocks” field contains the value 06h, seven blocks are read. The maximum number of blocks is fixed to 32 assuming that they are all located in the same sector. If the number of blocks overlaps sectors, the M24LR64E-R returns an error code.

The Protocol_extension_flag should be set to 1 for the M24LR64E-R to operate correctly. If the Protocol_extension_flag is at 0, the M24LR64E-R answers with an error code.

The Option_flag is supported. The data rate of the response is multiplied by 2.

The subcarrier_flag should be set to 0, otherwise the M24LR64E-R answers with an error code.

Table 95. Fast Read Multiple Block request format

Request SOF	Request_ flags	Fast Read Multiple Block	IC Mfg code	UID(1)	First block number	Number of blocks	CRC16	Request EOF
-	8 bits	C3h	02h	64 bits	16 bits	8 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameters:

- Request flag
- UID (Optional)
- First block number
- Number of blocks

Table 96. Fast Read Multiple Block response format when Error_flag is NOT set

Response SOF	Response_flags	Sector security status(1)	Data	CRC16	Response EOF
-	8 bits	8 bits(2)	32 bits(2)	16 bits	-

1. Gray color means that the field is optional.
2. Repeated as needed.

Response parameters:

- Sector security status if Option_flag is set (see *Table 97*)
- N block of data

Table 97. Sector security status if Option_flag is set

b_7 b_6 b_5	b_4 b_3	b_2 b_1	b_0
Reserved for future use All at 0	Password control bits	Read / Write protection bits	0: Current sector not locked 1: Current sector locked

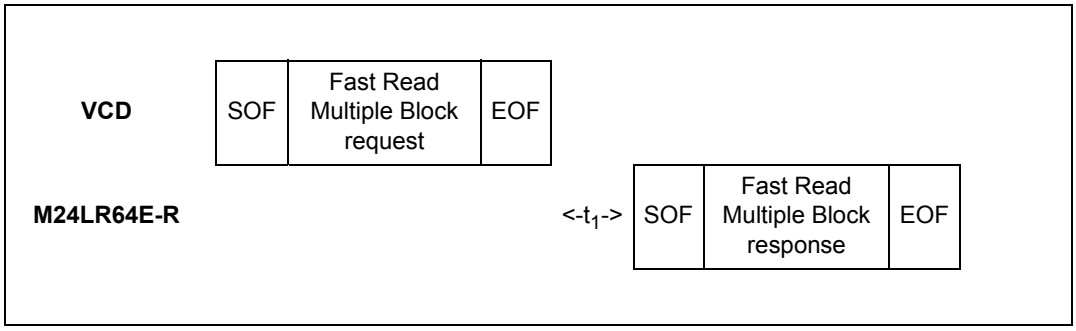
Table 98. Fast Read Multiple Block response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 03h: the option is not supported
  - 10h: block address not available
  - 15h: block read-protected

Figure 72. Fast Read Multiple Block frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Fast Read Multiple Block command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

26.21 Inventory Initiated

Before receiving the Inventory Initiated command, the M24LR64E-R must have received an Initiate or a Fast Initiate command in order to set the Initiate_ flag. If not, the M24LR64E-R does not answer the Inventory Initiated command.

On receiving the Inventory Initiated request, the M24LR64E-R runs the anticollision sequence. The Inventory_flag must be set to 1. The meaning of flags 5 to 8 is given in *Table 29*.

The request contains:

- the flags,
- the Inventory Command code,
- the AFI if the AFI flag is set,
- the mask length,
- the mask value,
- the CRC.

The M24LR64E-R does not generate any answer in case of error.

Table 99. Inventory Initiated request format

Request SOF	Request _flags	Inventory Initiated	IC Mfg code	Optional AFI	Mask length	Mask value	CRC16	Request EOF
-	8 bits	D1h	02h	8 bits	8 bits	0 - 64 bits	16 bits	-

The response contains:

- the flags,
- the Unique ID.

Table 100. Inventory Initiated response format

Response SOF	Response_flags	DSFID	UID	CRC16	Response EOF
-	8 bits	8 bits	64 bits	16 bits	-

During an Inventory process, if the VCD does not receive an RF M24LR64E-R response, it waits for a time t_3 before sending an EOF to switch to the next slot. t_3 starts from the rising edge of the request EOF sent by the VCD.

- If the VCD sends a 100% modulated EOF, the minimum value of t_3 is:
  $t_3min = 4384/f_C$ (323.3µs) + t_{SOF}
- If the VCD sends a 10% modulated EOF, the minimum value of t_3 is:
  $t_3min = 4384/f_C$ (323.3µs) + t_{NRT}

where:

- t_{SOF} is the time required by the M24LR64E-R to transmit an SOF to the VCD
- t_{NRT} is the nominal response time of the M24LR64E-R

t_{NRT} and t_{SOF} are dependent on the M24LR64E-R-to-VCD data rate and subcarrier modulation mode.

When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF starting the inventory command to the end of the M24LR64E-R response. If the M24LR64E-R does not receive the corresponding slot marker, the RF WIP/BUSY pin remains at 0 until the next RF power-off.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

26.22 Initiate

On receiving the Initiate command, the M24LR64E-R sets the internal Initiate_flag and sends back a response only if it is in the ready state. The command has to be issued in the Non Addressed mode only (Select_flag is reset to 0 and Address_flag is reset to 0). If an error occurs, the M24LR64E-R does not generate any answer. The Initiate_flag is reset after a power-off of the M24LR64E-R.

The request contains:

- No data

Table 101. Initiate request format

Request SOF	Request_flags	Initiate	IC Mfg code	CRC16	Request EOF
-	8 bits	D2h	02h	16 bits	-

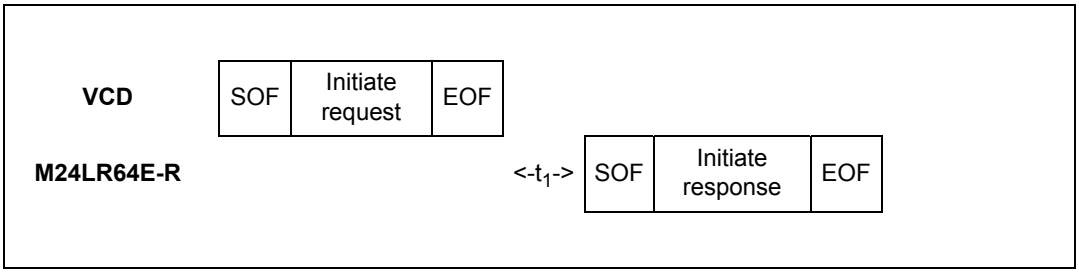
The response contains:

- the flags,
- the Unique ID.

Table 102. Initiate response format

Response SOF	Response_flags	DSFID	UID	CRC16	Response EOF
-	8 bits	8 bits	64 bits	16 bits	-

Figure 73. Initiate frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the Initiate command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

26.23 ReadCfg

On receiving the ReadCfg command, the M24LR64E-R reads the Configuration byte and sends back its 8-bit value in the response.

The Protocol_extension_flag should be set to 0 for the M24LR64E-R to operate correctly. If the Protocol_extension_flag is at 1, the M24LR64E-R answers with an error code. The Option_flag is not supported. The Inventory_flag must be set to 0.

Table 103. ReadCfg request format

Request SOF	Request_flags	ReadCfg	IC Mfg code	UID(1)	CRC16	Request EOF
-	8 bits	A0h	02h	64 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameters:

- UID (optional)

Table 104. ReadCfg response format when Error_flag is NOT set

Response SOF	Response_flags	Data	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameters:

- One byte of data: Configuration byte

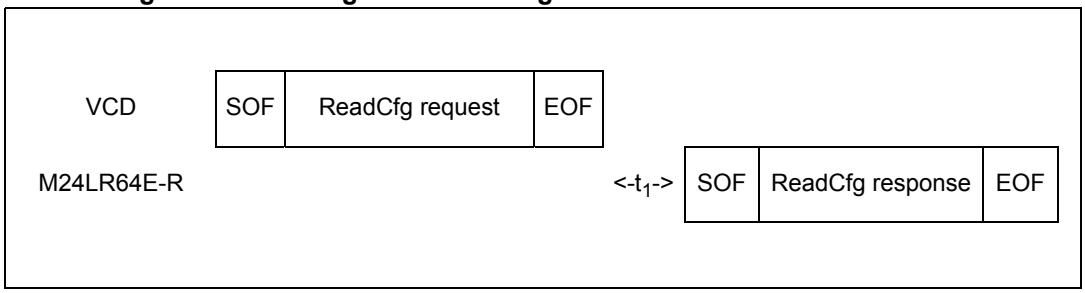
Table 105. ReadCfg response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set
  - 03h: the option is not supported
  - 0Fh: error with no information given

Figure 74. ReadCfg frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the ReadCfg command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

26.24 WriteEHCfg

On receiving the WriteEHCfg command, the M24LR64E-R writes the data contained in the request to the Configuration byte and reports whether the write operation was successful in the response. The Protocol_extension_flag should be set to 0 for the M24LR64E-R to operate correctly. If the Protocol_extension_flag is at 1, the M24LR64E-R answers with an error code.

The Option_flag is supported, the Inventory_flag is not supported.

During the RF write cycle W_t, there should be no modulation (neither 100% nor 10%), otherwise the M24LR64E-R may not program correctly the data into the Configuration byte. The W_t time is equal to t_{1nom} + 18 × 302 µs.

Table 106. WriteEHCfg request format

Request SOF	Request_flags	WriteEHCfg	IC Mfg code	UID(1)	Data	CRC16	Request EOF
-	8 bits	A1h	02h	64 bits	8 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameters:

- Request flags
- UID (optional)
- Data: during WriteEHCfg command, bit 3 of the data is ignored (see *Table 14*).

Table 107. WriteEHCfg response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter. The response is sent back after the writing cycle.

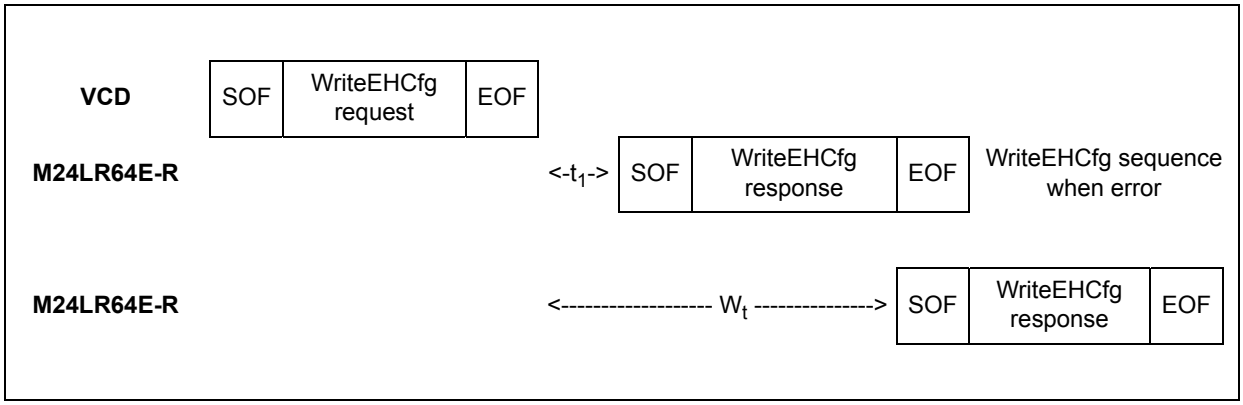
Table 108. WriteEHCfg response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 13h: the specified block was not successfully programmed

Figure 75. WriteEHCfg frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the WriteEHCfg command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin is tied to 0 for the entire duration of the internal write cycle (from the end of a valid WriteEHCfg command to the beginning of the M24LR64E-R response).

26.25 WriteDOCfg

On receiving the WriteDOCfg command, the M24LR64E-R writes the data contained in the request to the Configuration byte and reports whether the write operation was successful in the response. The Protocol_extension_flag should be set to 0 for the M24LR64E-R to operate correctly. If the Protocol_extension_flag is at 1, the M24LR64E-R answers with an error code.

The Option_flag is supported, the Inventory_flag is not supported.

During the RF write cycle W_t, there should be no modulation (neither 100% nor 10%), otherwise the M24LR64E-R may not program correctly the data into the Configuration byte. The W_t time is equal to t_{1nom} + 18 × 302 µs.

Table 109. WriteDOCfg request format

Request SOF	Request_ flags	WriteDOCfg	IC Mfg code	UID(1)	Data	CRC16	Request EOF
-	8 bits	A4h	02h	64 bits	8 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameters:

- Request flag
- UID (optional)
- Data: during a WriteDOCfg command, bits 2 to 0 of the data are ignored (see *Table 14*).

Table 110. WriteDOCfg response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter. The response is sent back after the writing cycle.

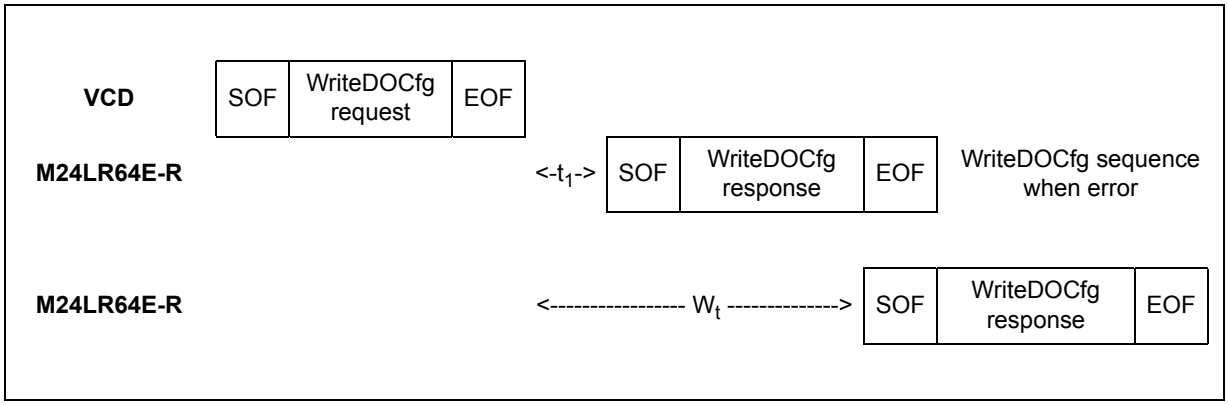
Table 111. WriteDOCfg response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 13h: the specified block was not successfully programmed

Figure 76. WriteDOCfg frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the WriteEHCfg command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin is tied to 0 for the entire duration of the internal write cycle (from the end of a valid WriteDOCfg command to the beginning of the M24LR64E-R response).

26.26 SetRstEHEn

On receiving the SetRstEHEn command, the M24LR64E-R sets or resets the EH_enable bit in the volatile Control register. The Protocol_extension_flag should be set to 0 for the M24LR64E-R to operate correctly. If the Protocol_extension_flag is at 1, the M24LR64E-R answers with an error code. The Option_flag and the Inventory_flag are not supported.

Table 112. SetRstEHEn request format

Request SOF	Request_flags	SetRstEHEn	IC Mfg code	UID(1)	Data	CRC16	Request EOF
-	8 bits	A2h	02h	64 bits	8 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameters:

- Request flags
- UID (optional)
- Data: during a SetRstEHEn command, bits 7 to 1 are ignored. Bit 0 is the EH_enable bit.

Table 113. SetRstEHEn response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter. The response is sent back after t_1.

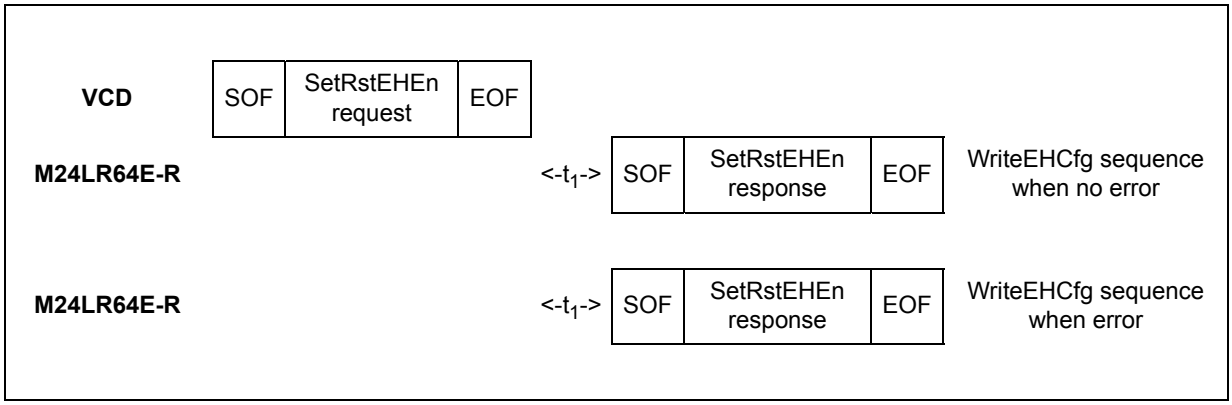
Table 114. SetRstEHEn response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 03h: the option is not supported

Figure 77. SetRstEHEn frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the SetRstEHEn command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

26.27 CheckEHEn

On receiving the CheckEHEn command, the M24LR64E-R reads the Control register and sends back its 8-bit value in the response.

The Protocol_extension_flag should be set to 0 for the M24LR64E-R to operate correctly. If the Protocol_extension_flag is at 1, the M24LR64E-R answers with an error code. The Option_flag is not supported. The Inventory_flag must be set to 0.

Table 115. CheckEHEn request format

Request SOF	Request_flags	CheckEHEn	IC Mfg code	UID(1)	CRC16	Request EOF
-	8 bits	A3h	02h	64 bits	16 bits	-

1. Gray color means that the field is optional.

Request parameters:

- UID (optional)

Table 116. CheckEHEn response format when Error_flag is NOT set

Response SOF	Response_flags	Data	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameters:

- One byte of data: volatile Control register (see *Table 15*)

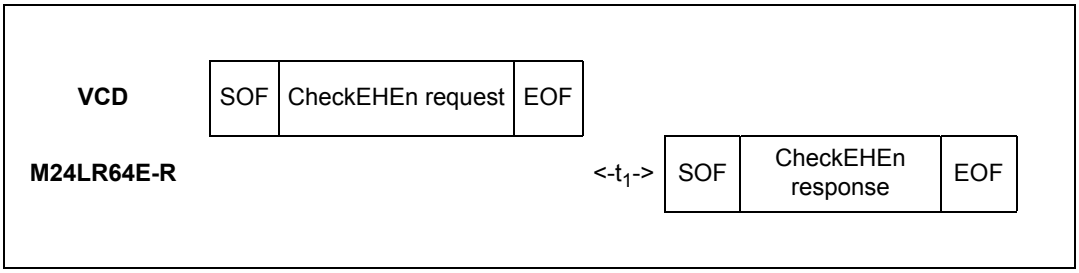
Table 117. CheckEHEn response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set
  - 03h: the option is not supported

Figure 78. CheckEHEn frame exchange between VCD and M24LR64E-R



When configured in the RF busy mode, the RF WIP/BUSY pin is tied to 0 from the SOF that starts the CheckEHEn command to the end of the M24LR64E-R response.

When configured in the RF write in progress mode, the RF WIP/BUSY pin remains in high-Z state.

27 Maximum ratings

Stressing the device above the rating listed in *Table 118* may cause permanent damage to the device. These are stress ratings only and operation of the device, at these or any other conditions above those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 118. Absolute maximum ratings

Symbol	Parameter		Min.	Max.	Unit
T_A	Ambient operating temperature		-40	85	°C
T_{STG}, h_{STG}, t_{STG}	Storage conditions	Sawn wafer on UV tape	15	25	°C
			-	6(1)	months
			kept in its original packing form		
T_{STG}	Storage temperature	UFDFPN8 (MLP8), SO8, TSSOP8	-65	150	°C
T_{LEAD}	Lead temperature during soldering	UFDFPN8 (MLP8), SO8, TSSOP8	see note (2)		°C
V_{IO}	I^2C input or output range		-0.50	6.5	V
V_{CC}	I^2C supply voltage		-0.50	6.5	V
I_{OL_MAX}	DC output current on pin SDA or RF WIP/BUSY (when equal to 0)		-	5	mA
I_{CC}(3)	RF supply current AC0 - AC1		-	50	mA
V_{MAX_1}(3)	RF input voltage amplitude peak to peak between AC0 and AC1, GND pad left floating	VAC0-VAC1	-	27	V
V_{MAX_2}(3)	AC voltage between AC0 and GND, or AC1 and GND	VAC0-GND, or VAC1-GND	-1	11	V
V_{ESD}	Electrostatic discharge voltage (human body model)(4)	AC0, AC1	-	1000	V
		Other pads	-	3500	
	Electrostatic discharge voltage on antenna (5)	AC0, AC1	-	4000	

1. Counted from ST shipment date.
2. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
3. Based on characterization, not tested in production.
4. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω)
5. Compliant with IEC 61000-4-3 method. (M24LRxxE packaged in S08N is mounted on ST's reference antenna ANT1- M24LRxxE)

28 I²C DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device in I²C mode. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 119. I²C operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	-40	85	°C

Table 120. AC test measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	100		pF
t_r, t_f	Input rise and fall times	-	50	ns
$V_{hi\text{-}lo}$	Input levels	0.2 V_{CC} to 0.8 V_{CC}		V
$V_{ref(t)}$	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 79. AC test measurement I/O waveform

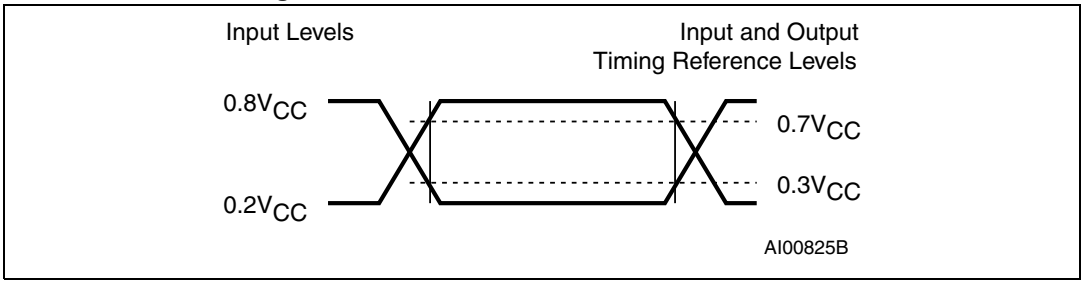


Table 121. Input parameters

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)	-	8	pF
C_{IN}	Input capacitance (other pins)	-	6	pF
t_{NS}(1)	Pulse width ignored (Input filter on SCL and SDA)	-	80	ns

1. Characterized only.

Table 122. I²C DC characteristics

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA)	V_{IN} = V_{SS} or V_{CC} device in Standby mode	-	± 2	µA
I_{LO_Vout}	Vout output leakage current	External voltage applied on Vout: V_{SS} or V_{CC}	-	± 5	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)(1)	V_{CC} = 1.8 V, f_c = 100 kHz (rise/fall time < 50 ns)	-	50	µA
		V_{CC} = 1.8 V, f_c = 400 kHz (rise/fall time < 50 ns)	-	100	
		V_{CC} = 2.5 V, f_c = 400 kHz (rise/fall time < 50 ns)	-	200	
		V_{CC} = 5.5 V, f_c = 400 kHz (rise/fall time < 50 ns)	-	400	
I_{CC0}	Supply current (Write)(1)	V_{CC} = 1.8 - 5.5 V	-	220	µA
I_{CC1}	Standby supply current	V_{IN} = V_{SS} or V_{CC} V_{CC} = 1.8 V	-	30	µA
		V_{IN} = V_{SS} or V_{CC} V_{CC} = 2.5 V	-	30	
		V_{IN} = V_{SS} or V_{CC} V_{CC} = 5.5 V	-	100	
V_{IL}	Input low voltage (SDA, SCL)	V_{CC} = 1.8 V	-0.45	$0.25V_{CC}$	V
		V_{CC} = 2.5 V	-0.45	$0.25V_{CC}$	
		V_{CC} = 5.5 V	-0.45	$0.3V_{CC}$	
V_{IH}	Input high voltage (SDA, SCL)	V_{CC} = 1.8 V	$0.75V_{CC}$	V_{CC}+1	V
		V_{CC} = 2.5 V	$0.75V_{CC}$	V_{CC}+1	
		V_{CC} = 5.5 V	$0.7V_{CC}$	V_{CC}+1	
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 1.8 V or I_{OL} = 3 mA, V_{CC} = 5.5 V	-	0.4	V

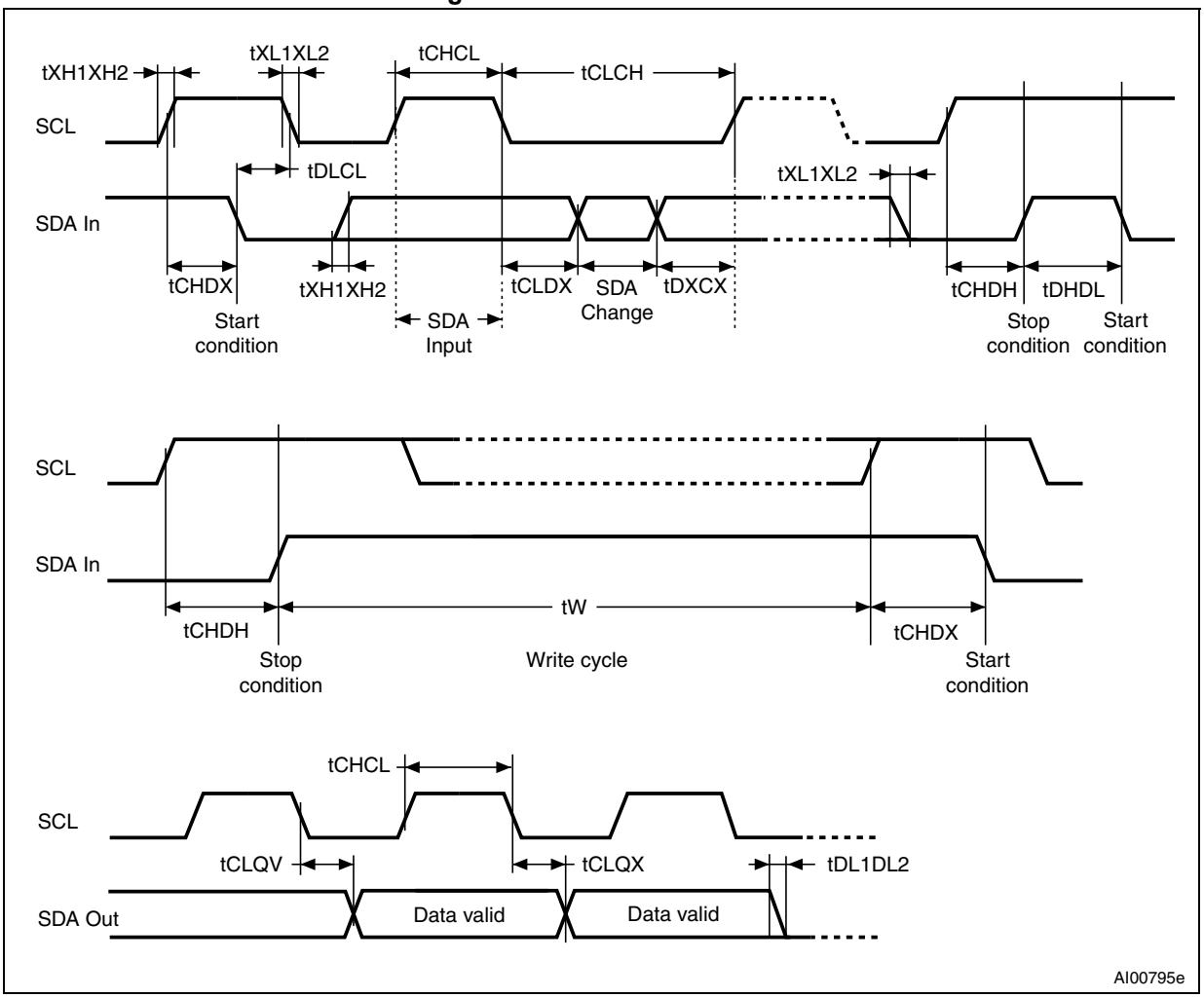
1. SCL, SDA connected to Ground or V_{CC}. SDA connected to V_{CC} through a pull-up resistor.

Table 123. I²C AC characteristics

Test conditions specified in *Table 119*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCL}	Clock frequency	25	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	0.6	20000(1)	µs
t_{CLCH}	t_{LOW}	Clock pulse width low	1.3	20000(2)	µs
t_{START_OUT}	-	I²C timeout on Start condition	40	-	ms
t_{XH1XH2}(3)	t_R	Input signal rise time	20	300	ns
t_{XL1XL2}(3)	t_F	Input signal fall time	20	300	ns
t_{DL1DL2}	t_F	SDA (out) fall time	20	100	ns
t_{DXCX}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}(4)	t_{DH}	Data out hold time	100	-	ns
t_{CLQV}(5)	t_{AA}	Clock low to next data valid (access time)	100	900	ns
t_{CHDX}(6)	$t_{SU:STA}$	Start condition set up time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	0.6	35000(7)	µs
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
t_W	-	I²C write time	-	5	ms

1. t_{CHCL} timeout.
2. t_{CLCH} timeout.
3. Values recommended by the I²C-bus Fast-Mode specification.
4. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
5. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach $0.8V_{CC}$ in a compatible way with the I²C specification (which specifies $t_{SU:DAT}$ (min) = 100 ns), assuming that the $R_{bus} \times C_{bus}$ time constant is less than 500 ns (as specified in *Figure 3*).
6. For a reStart condition, or following a write cycle.
7. t_{DLCL} timeout.

Figure 80. I²C AC waveforms



29 RF electrical parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device in RF mode.

The parameters in the DC and AC characteristics tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 124. RF characteristics(1) (2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{CC}	External RF signal frequency	-	13.553	13.56	13.567	MHz
H_ISO	Operating field according to ISO	T_A = -40 °C to 85 °C	150	-	5000	mA/m
$MI_{CARRIER}$	10% carrier modulation index(3) MI=(A-B)/(A+B)	150 mA/m > H_ISO > 1000 mA/m	15	-	30	%
		H_ISO > 1000 mA/m	10	-	30	
t_{RFR}, t_{RFF}	10% rise and fall time	-	0.5	-	3.0	µs
t_{RFSBL}	10% minimum pulse width for bit	-	7.1	-	9.44	µs
$MI_{CARRIER}$	100% carrier modulation index	MI=(A-B)/(A+B)(4)	95	-	100	%
t_{RFR}, t_{RFF}	100% rise and fall time	-	0.5	-	3.5	µs
t_{RFSBL}	100% minimum pulse width for bit	-	7	-	9.44	µs
$t_{MIN\ CD}$	Minimum time from carrier generation to first data	From H-field min	-	-	1	ms
f_{SH}	Subcarrier frequency high	F_{CC}/32	-	423.75	-	kHz
f_{SL}	Subcarrier frequency low	F_{CC}/28	-	484.28	-	kHz
t_1	Time for M24LR64E-R response	4224/F_S	318.6	320.9	323.3	µs
t_2	Time between commands	4224/F_S	309	311.5	314	µs
W_t	RF write time (including internal Verify)	-	-	5.75	-	ms
I_{CC_RF}	Operating current (Read)(5)	VAC0-VAC1 (4 V peak to peak)	-	20	-	µA
C_{TUN}	Internal tuning capacitor in SO8(6)	f = 13.56 MHz	24.8	27.5	30.2	pF
V_{BACK}	Backscattered level as defined by ISO test	ISO10373-7	10	-	-	mV
V_{MAX_1}(3)	RF input voltage amplitude between AC0 and AC1, GND pad left floating, VAC0-VAC1 peak to peak(7)	-	-	-	20	V
V_{MAX_2}(3)	AC voltage between AC0 and GND or between AC1 and GND	-	-1	-	8.5	V

Table 124. RF characteristics(1) (2) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{MIN_1}(3)	RF input voltage amplitude between AC0 and AC1, GND pad left floating, VAC0-VAC1 peak to peak(7)	Inventory and Read operations	-	4	4.5	V
		Write operations	-	4.5	5	V
V_{MIN_2}(3)	AC voltage between AC0 and GND or between AC1 and GND	Inventory and Read operations	-	1.8	2	V
		Write operations	-	2	2.2	V
t_{RF_OFF}	RF OFF time	Chip reset	2	-	-	ms

1. T_A = –40 to 85 °C. Characterized only.
2. All timing characterizations were performed on a reference antenna with the following characteristics:
   External size: 75 mm x 48 mm
   Number of turns: 5
   Width of conductor: 0.5 mm
   Space between two conductors: 0.3 mm
   Value of the tuning capacitor in SO8: 27.5 pF (M24LR64E-R)
   Value of the coil: 5 µH
   Tuning frequency: 13.56 MHz.
3. 15% (or more) carrier modulation index offers a better signal/noise ratio and therefore a wider operating range with a better noise immunity.
4. Temperature range 0 °C to 90 °C.
5. Characterized on bench.
6. Characterized only, at room temperature only, measured at VAC0-VAC1 = 1 V peak to peak.
7. Characterized only, at room temperature only.

Table 125. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient operating temperature	-40	85	°C

Figure 81 shows an ASK modulated signal from the VCD to the M24LR64E-R. The test conditions for the AC/DC parameters are:

- Close coupling condition with tester antenna (1 mm)
- M24LR64E-R performance measured at the tag antenna
- M24LR64E-R synchronous timing, transmit and receive

Figure 81. ASK modulated signal

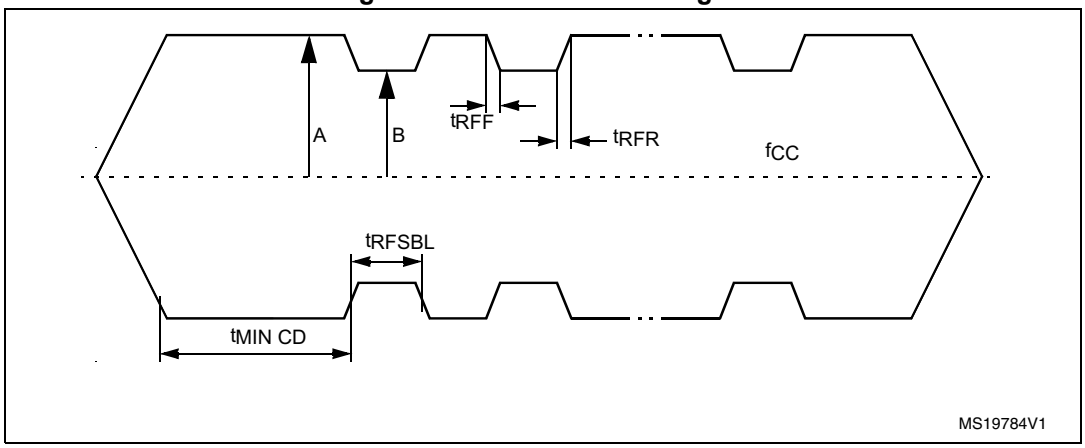


Table 126 below summarizes respectively the minimum AC0-AC1 input power level $P_{AC0\text{-}AC1\_min}$ required for the Energy harvesting mode, the corresponding maximum current consumption I_{sink_max} and variation of the analog voltage Vout for the various Energy harvesting fan-out configurations defined by bits b0 and b1 of the Configuration byte.

Table 126. Energy harvesting(1) (2)

Range	H_{min}(3)	P_{min}(4)	Vout@I=0	Vout@I_{sink_max}	I_{sink_max}@P_{min}
00	3.5 A/m	100 mW	2.7 V min 4.5 V max	1.7 V	6 mA
01	2.4 A/m	60 mW	2.7 V min 4.5 V max	1.9 V	3 mA
10	1.6 A/m	30 mW	2.7 V min 4.5 V max	2.1 V	1 mA
11	1.0 A/m	16 mW	2.7 V min 4.5 V max	2.3 V	300 µA

1. Characterized only.
2. Valid from -40 °C to +85 °C.
3. H_{min} characterized according to ISO10373-7 test method.
4. P_{min} calculated from DC measurements.

We recommend to choose the Energy Harvesting Range according to the maximum current requested by the application to avoid any disabling of Energy Harvesting mode (for example, choose Range 01 for a max consumption of 2 mA).

Figure 82. Energy harvesting: V_{out} min vs. I_{sink}

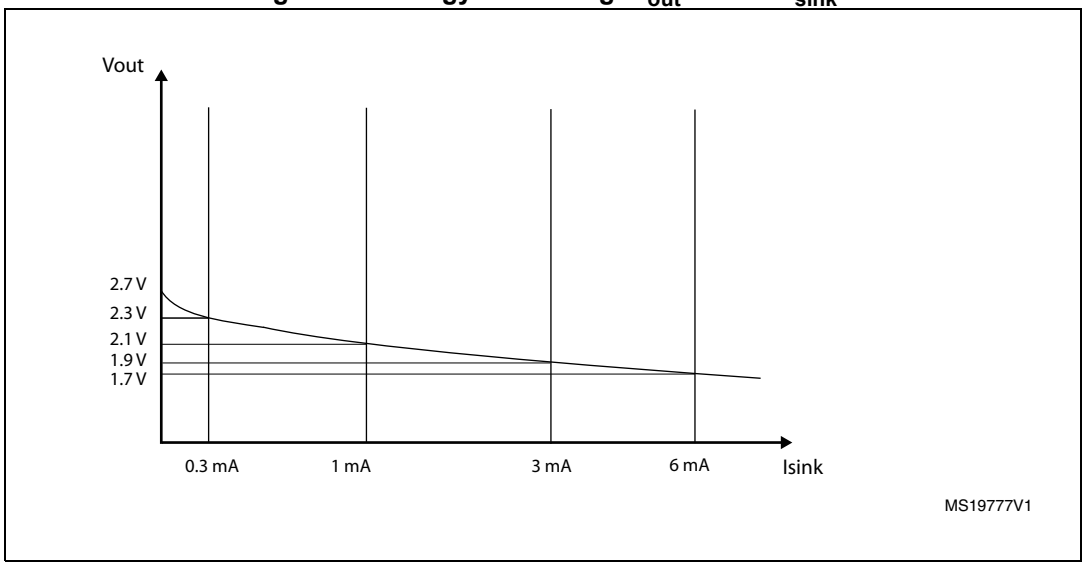


Figure 83. Energy harvesting: working domain range 11

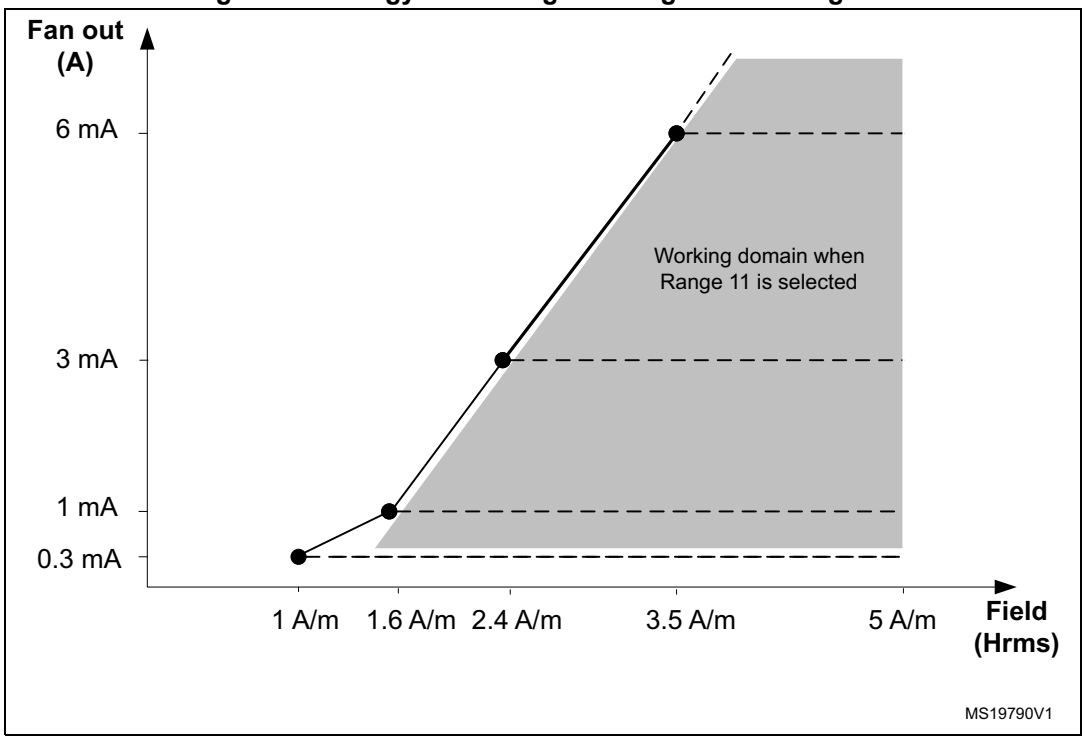


Figure 84. Energy harvesting: working domain range 10

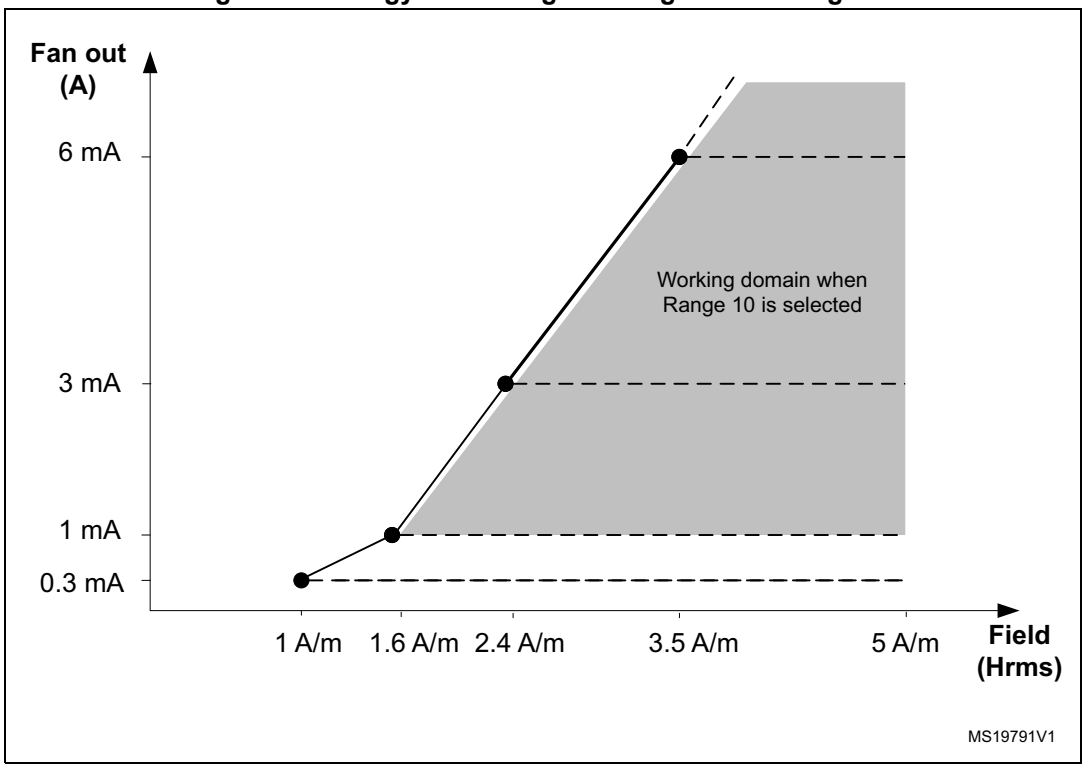


Figure 85. Energy harvesting: working domain range 01

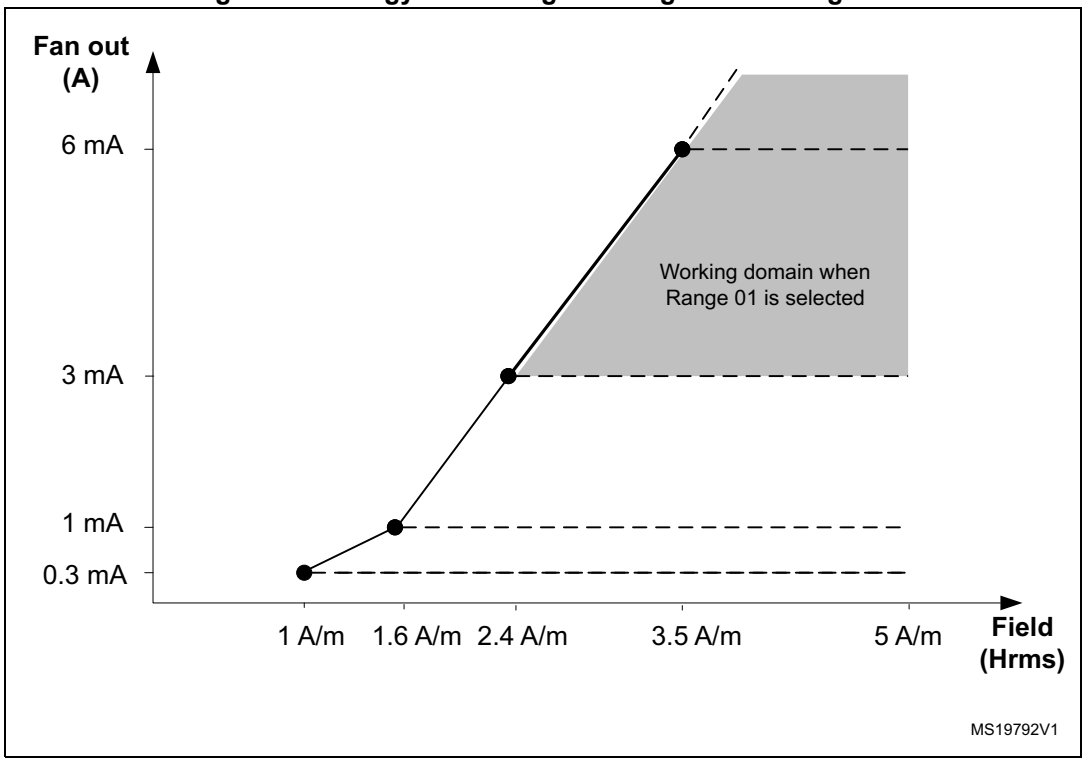
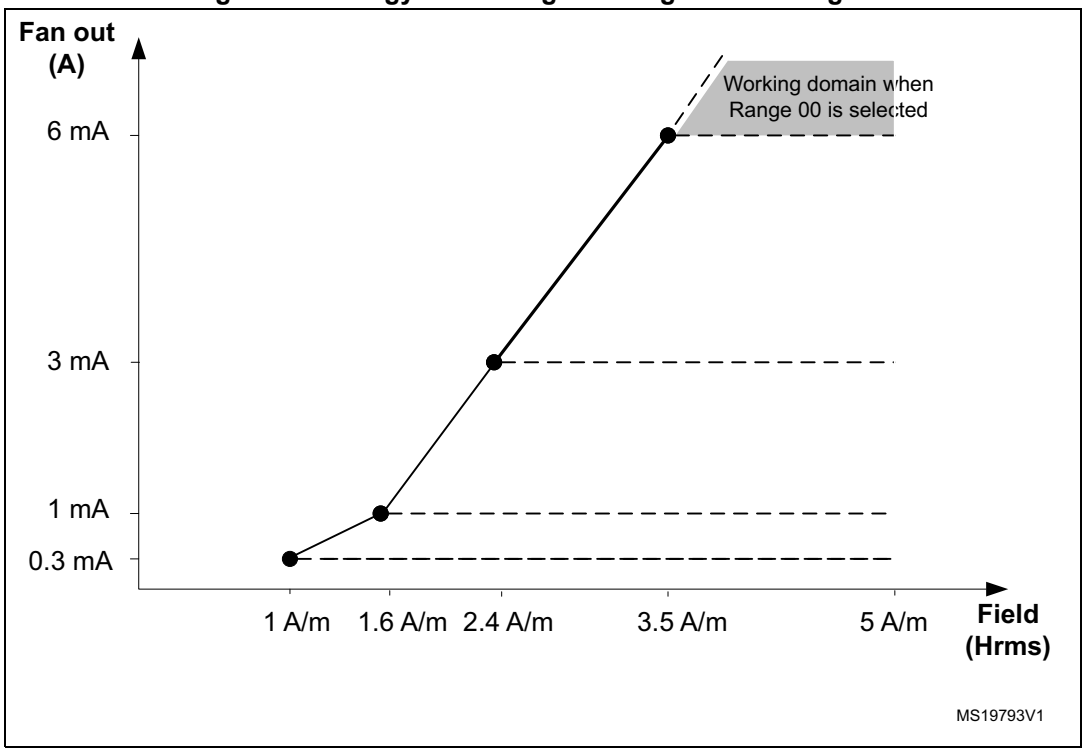


Figure 86. Energy harvesting: working domain range 00

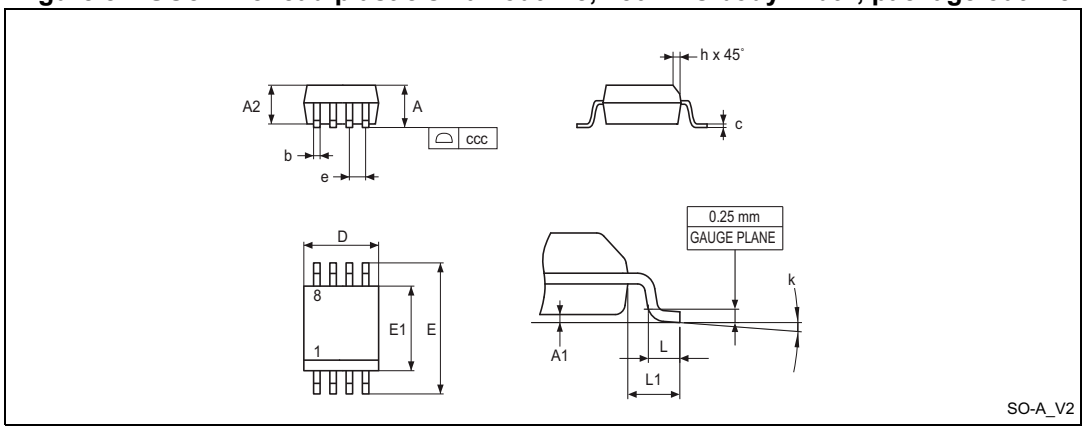


30 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

30.1 SO8N package information

Figure 87. SO8N – 8-lead plastic small outline, 150 mils body width, package outline



1. Drawing is not to scale.

Table 127. SO8N – 8-lead plastic small outline, 150 mils body width, package mechanical data

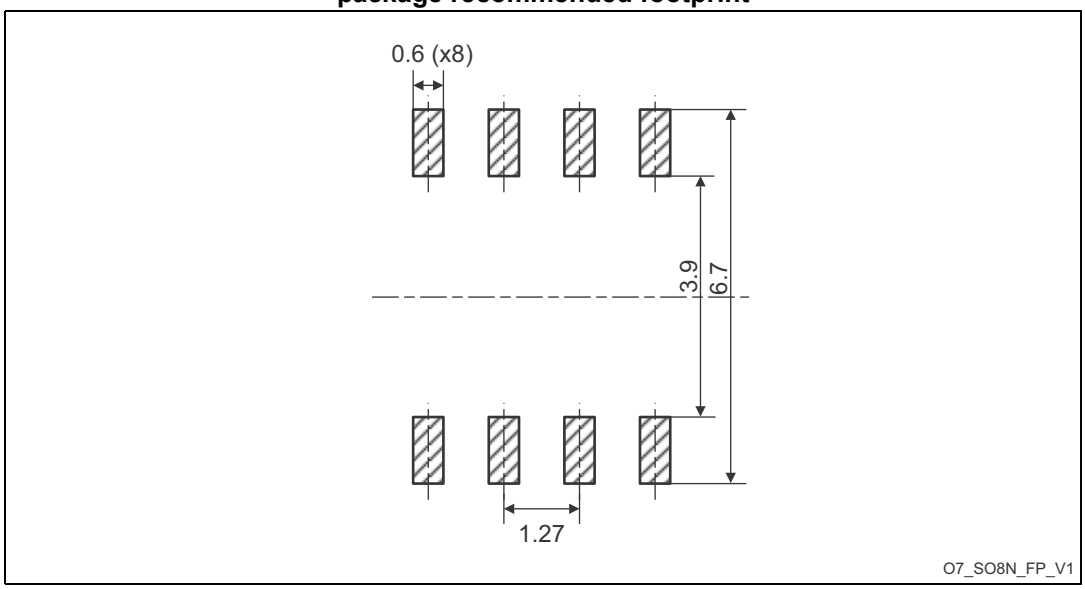
Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.170	-	0.230	0.0067	-	0.0091
D	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500

Table 127. SO8N – 8-lead plastic small outline, 150 mils body width, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.

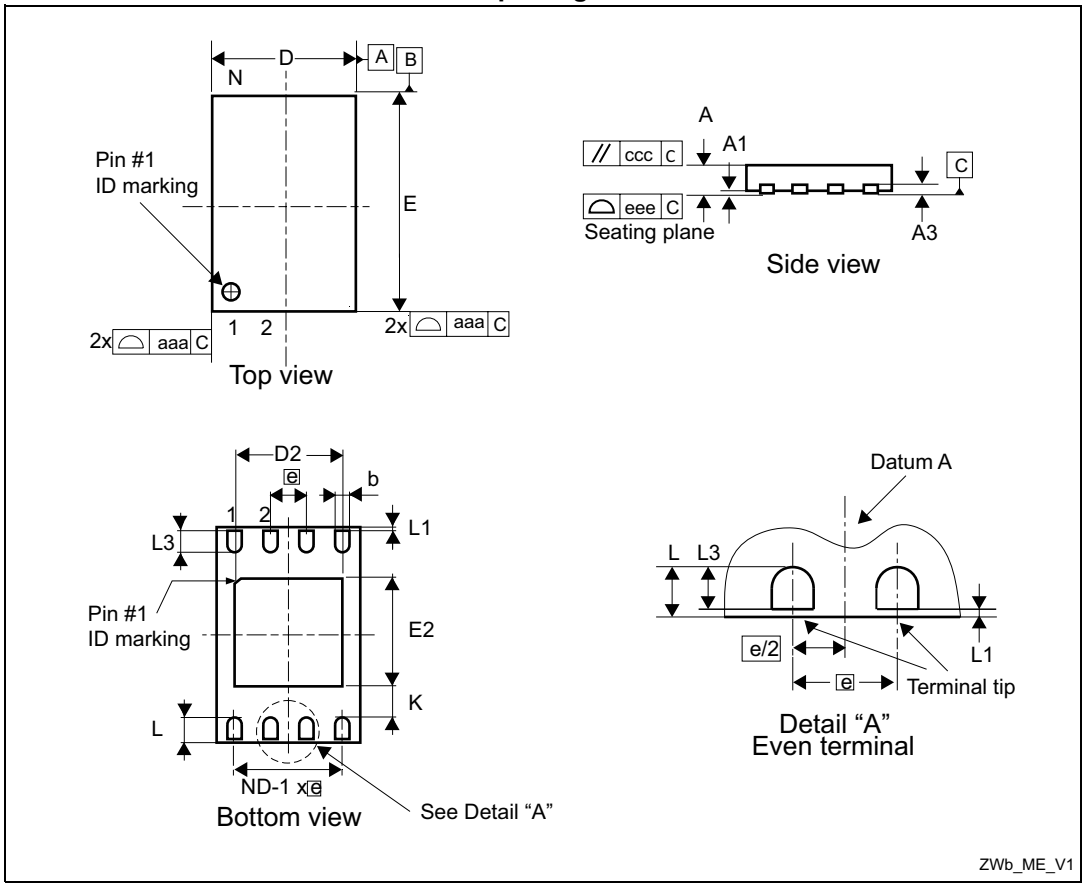
Figure 88. SO8N – 8-lead plastic small outline, 150 mils body width, package recommended footprint



1. Dimensions are expressed in millimeters.

30.2 UFDFN8 package information

Figure 89. UFDFN8 - 8-lead, 2 × 3 mm, 0.5 mm pitch ultra thin profile fine pitch dual flat package outline



1. Max. package warpage is 0.05 mm.
2. Exposed copper is not systematic and can appear partially or totally according to the cross section.
3. Drawing is not to scale.

Table 128. UFDFN8 - 8-lead, 2 × 3 mm, 0.5 mm pitch ultra thin profile fine pitch dual flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.450	0.550	0.600	0.0177	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
b[2]	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	1.900	2.000	2.100	0.0748	0.0787	0.0827
D2	1.200	-	1.600	0.0472	-	0.0630
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
E2	1.200	-	1.600	0.0472	-	0.0630

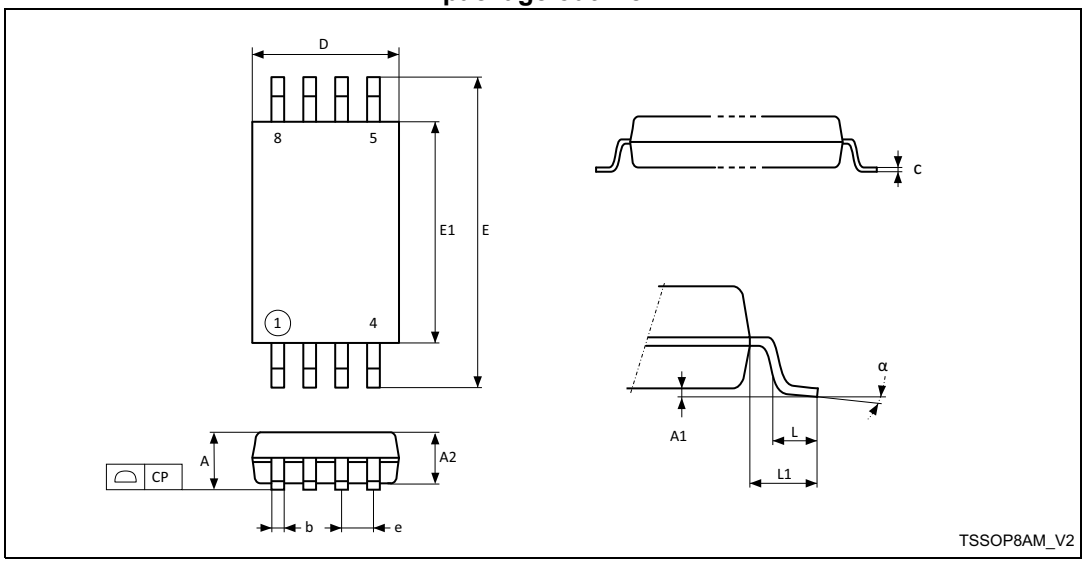
Table 128. UFDFN8 - 8-lead, 2 × 3 mm, 0.5 mm pitch ultra thin profile fine pitch dual flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	0.0197		
K	0.300	-	-	0.0118	-	-
L	0.300	-	0.500	0.0118	-	0.0197
L1	-	-	0.150	-	-	0.0059
L3	0.300	-	-	0.0118	-	-
aaa	-	-	0.150	-	-	0.0059
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee[3]	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension b applies to plated terminal and is measured between 0.15 and 0.30 mm from the terminal tip.
3. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

30.3 TSSOP8 package information

Figure 90.TSSOP8 – 8-lead thin shrink small outline, 3 x 4.4 mm, 0.5 mm pitch, package outline



1. Drawing is not to scale.

Table 129. TSSOP8 – 8-lead thin shrink small outline, 3 x 4.4 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
CP	-	-	0.100	-	-	0.0039
D	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.650	-	-	0.0256	-
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1	4.300	4.400	4.500	0.1693	0.1732	0.1772
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
α	0°	-	8°	0°	-	8°

1. Values in inches are converted from mm and rounded to four decimal digits.

31 Part numbering

Table 130. Ordering information scheme for packaged devices

Example: M24LR64E-R MN 6 T /2

Device type

M24LR = dynamic NFC/RFID tag IC

64 = memory size in Kbit

E = support for energy harvesting

Operating voltage(1)

R = V_{CC} = 1.8 to 5.5 V

Package

MN = SO8N (150 mils width)

MC = UFDFPN8 (MLP8)

DW = TSSOP8

SB12I = 120 µm ± 15 µm bumped and sawn inkless wafer on 8-inch frame(2)

Device grade(1)

6 = industrial: device tested with standard test flow over –40 to 85 °C

Option(1)

T = Tape and reel packing

Capacitance(1)

/2 = 27.5 pF

1. For packaged devices only.
2. Delivery type: wafer tested. Bad chip identification by STIF wafer maps available on STMicroelectronics inkless central transfer server.

Note: Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 131. Ordering and marking information

Reference	Package	Ordering code	First line marking	
			Initial revision 0xF	Actual revision 0xE and below
M24LR64E-R	TSSOP08	M24LR64E-RDW6T/2	464EU	4FEUB
	MLP	M24LR64E-RMC6T/2	464E	4FEB
	SO8N	M24LR64E-RMN6T/2	24L64ER	24LFERB

Appendix A Anticollision algorithm (informative)

The following pseudocode describes how anticollision could be implemented on the VCD, using recursivity.

A.1 Algorithm for pulsed slots

```
function push (mask, address); pushes on private stack
function pop (mask, address); pops from private stack
function pulse_next_pause; generates a power pulse
function store(M24LR64E-R_UID); stores M24LR64E-R_UID

function poll_loop (sub_address_size as integer)
   pop (mask, address)
   mask = address & mask; generates new mask
              ; send the request
   mode = anticollision
   send_Request (Request_cmd, mode, mask length, mask value)
   for sub_address = 0 to (2^sub_address_size - 1)
      pulse_next_pause
      if no_collision_is_detected ; M24LR64E-R is inventoried
         then
            store (M24LR64E-R_UID)
         else ; remember a collision was detected
            push(mask,address)
         endif
      next sub_address

   if stack_not_empty ; if some collisions have been detected and
      then    ; not yet processed, the function calls itself
        poll_loop (sub_address_size); recursively to process the last
stored collision
     endif
end poll_loop

main_cycle:
   mask = null
   address = null
   push (mask, address)
   poll_loop(sub_address_size)
end_main_cycle
```

Appendix B CRC (informative)

B.1 CRC error detection method

The cyclic redundancy check (CRC) is calculated on all data contained in a message, from the start of the flags through to the end of Data. The CRC is used from VCD to M24LR64E-R and from M24LR64E-R to VCD.

Table 132. CRC definition

CRC type	Length	Polynomial	Direction	Preset	Residue
ISO/IEC 13239	16 bits	$X^{16} + X^{12} + X^5 + 1 = 8408h$	Backward	FFFFh	F0B8h

To add extra protection against shifting errors, a further transformation on the calculated CRC is made. The one's complement of the calculated CRC is the value attached to the message for transmission.

To check received messages, the two CRC bytes are often also included in the re-calculation, for ease of use. In this case, the expected value for the generated CRC is the residue F0B8h.

B.2 CRC calculation example

This example in C language illustrates one method of calculating the CRC on a given set of bytes comprising a message.

C-example to calculate or check the CRC16 according to ISO/IEC 13239

```
#define  POLYNOMIAL0x8408//  x^16 + x^12 + x^5 + 1
#define  PRESET_VALUE0xFFFF
#define  CHECK_VALUE0xF0B8

#define  NUMBER_OF_BYTES4// Example: 4 data bytes
#define  CALC_CRC1
#define  CHECK_CRC0

void main()
{
  unsigned int  current_crc_value;
  unsigned char array_of_databytes[NUMBER_OF_BYTES + 2] = {1, 2, 3, 4, 0x91,
0x39};
  int           number_of_databytes = NUMBER_OF_BYTES;
  int           calculate_or_check_crc;
  int           i, j;
  calculate_or_check_crc = CALC_CRC;
// calculate_or_check_crc = CHECK_CRC;// This could be an other example
  if (calculate_or_check_crc == CALC_CRC)
  {
      number_of_databytes = NUMBER_OF_BYTES;
```

```
  }
  else    // check CRC
  {
      number_of_databytes = NUMBER_OF_BYTES + 2;
  }

  current_crc_value = PRESET_VALUE;

  for (i = 0; i < number_of_databytes; i++)
  {
      current_crc_value = current_crc_value ^ ((unsigned
int)array_of_databytes[i]);

      for (j = 0; j < 8; j++)
      {
          if (current_crc_value & 0x0001)
          {
              current_crc_value = (current_crc_value >> 1) ^ POLYNOMIAL;
          }
          else
          {
              current_crc_value = (current_crc_value >> 1);
          }
      }
  }

  if (calculate_or_check_crc == CALC_CRC)
  {
      current_crc_value = ~current_crc_value;

      printf ("Generated CRC is 0x%04X\n", current_crc_value);

      // current_crc_value is now ready to be appended to the data stream
      // (first LSByte, then MSByte)
  }
  else   // check CRC
  {
      if (current_crc_value == CHECK_VALUE)
      {
          printf ("Checked CRC is ok (0x%04X)\n", current_crc_value);
      }
      else
      {
          printf ("Checked CRC is NOT ok (0x%04X)\n", current_crc_value);
      }
  }
}
```

Appendix C Application family identifier (AFI) (informative)

The AFI (application family identifier) represents the type of application targeted by the VCD and is used to extract from all the M24LR64E-Rs present only the one meeting the required application criteria.

It is programmed by the M24LR64E-R issuer (the purchaser of the M24LR64E-R). Once locked, it cannot be modified.

The most significant nibble of the AFI is used to code one specific or all application families, as defined in *Table 133*.

The least significant nibble of the AFI is used to code one specific or all application subfamilies. Subfamily codes different from 0 are proprietary.

Table 133. AFI coding(1)

AFI most significant nibble	AFI least significant nibble	Meaning VICCs respond from	Examples / Note
‘0’	‘0’	All families and subfamilies	No applicative preselection
‘X’	'0	All subfamilies of family X	Wide applicative preselection
'X	"Y’	Only the Y^{th} subfamily of family X	-
‘0’	‘Y’	Proprietary subfamily Y only	-
‘1	"0’, ‘Y’	Transport	Mass transit, bus, airline,...
'2	"0’, ‘Y’	Financial	IEP, banking, retail,...
'3	"0’, ‘Y’	Identification	Access control,...
'4	"0’, ‘Y’	Telecommunication	Public telephony, GSM,...
‘5’	‘0’, ‘Y’	Medical	-
'6	"0’, ‘Y’	Multimedia	Internet services....
'7	"0’, ‘Y’	Gaming	-
8	"0’, ‘Y’	Data Storage	Portable files,...
'9	"0’, ‘Y’	Item management	-
'A	"0’, ‘Y’	Express parcels	-
'B	"0’, ‘Y’	Postal services	-
'C	"0’, ‘Y’	Airline bags	-
'D	"0’, ‘Y’	RFU	-
'E	"0’, ‘Y’	RFU	-
‘F’	‘0’, ‘Y’	RFU	-

1. X = '1' to 'F', Y = '1' to 'F'

Revision history

Table 134. Document revision history

Date	Revision	Changes
12-Apr-2012	1	Initial release.
08-Jun-2012	2	Updated *Section 7.1: RF communication and energy harvesting on page 42* and *Figure 49: M24LR64E-R state transition diagram on page 65*. Updated clock pulse width values in *Table 123: I2C AC characteristics on page 122*.
19-Jun-2012	3	Updated notes for *Figure 49: M24LR64E-R state transition diagram on page 65*.
21-Feb-2013	4	– Number of sectors updated in *Section 3*. – Updated *Section 4.2*. – Updated *Figure 6: Memory sector organization*. – M24LR64E changed into M24LR64x in *Figure 52: M24LR64E RF-Busy management following Inventory command*, *Figure 56: M24LR64E RF-Busy management following Write command* and *Figure 57: M24LR64E RF-Wip management following Write command*. – Updated *Table 15: Control register*, *Table 17: System parameter sector*, *Table 118: Absolute maximum ratings*, *Table 122: I2C DC characteristics* and *Table 124: RF characteristics*.
07-Mar-2013	5	Added *Table 131: Ordering and marking information*.
12-Jun-2013	6	Added “Dynamic NFC/RFID tag IC” to the title, *Section 1: Description*, and the M24LR definition in *Table 130: Ordering information scheme for packaged devices*. Updated V_{ESD} and Note 5 in *Table 118: Absolute maximum ratings*. Removed MB package from *Figure 88: UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat package no lead 2 × 3mm, package outline*.
21-Nov-2014	7	Updated *Figure 1: Logic diagram*, *Figure 14: 100% modulation waveform* and *Figure 15: 10% modulation waveform*. Updated footnote *4* in *Table 123: I2C AC characteristics*. Added note on Engineering samples marking in *Section 31: Part numbering*.
06-Nov-2015	8	Updated figure on Cover page with new wafer code SB12I. Updated *Figure 10: Write cycle polling flowchart using Ack*, *Figure 14: 100% modulation waveform* and *Figure 15: 10% modulation waveform*. Updated *Table 118: Absolute maximum ratings* and its footnote *4*. Updated *Section 30: Package information* and its subsections. Updated *Table 130: Ordering information scheme for packaged devices* and added footnotes *1* and *2*.