

# Spartan-3A DSP Starter Platform User Guide

UG454 (v1.0) October 3, 2007





© 2007 Xilinx, Inc. All Rights Reserved. XILINX, the Xilinx logo, and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

NOTICE OF DISCLAIMER: Xilinx is providing this design, code, or information "as is." By providing the design, code, or information as one possible implementation of this feature, application, or standard, Xilinx makes no representation that this implementation is free from any claims of infringement. You are responsible for obtaining any rights you may require for your implementation. Xilinx expressly disclaims any warranty whatsoever with respect to the adequacy of the implementation, including but not limited to any warranties or representations that this implementation is free from claims of infringement and any implied warranties of merchantability or fitness for a particular purpose.

---

---

## Revision History

The following table shows the revision history for this document.

| Date    | Version | Revision               |
|---------|---------|------------------------|
| 10/3/07 | 1.0     | Initial Xilinx release |

---

# Table of Contents

---

|   |    |
|---|----|
| <b>Overview</b> .....   | 3  |
| <b>Design Description</b> .....                                   | 3  |
| Features .....  | 3  |
| Ordering Information .....  | 4  |
| <b>Functional Description</b> .....                               | 5  |
| Xilinx Spartan-3A DSP FPGA .....                                  | 6  |
| Memory .....  | 7  |
| Micron DDR2 SDRAM Interface .....                                 | 7  |
| Intel J3 Parallel Flash .....                                     | 10 |
| Intel S33 Serial Flash .....                                      | 11 |
| SystemACE Module (SAM) Connector .....                            | 11 |
| Interfaces .....  | 13 |
| National Semiconductor 10/100/1000 Ethernet PHY .....             | 13 |
| RS232 .....   | 16 |
| SPI Expansion .....   | 17 |
| Digilent Headers .....  | 17 |
| Eridon Debug Connector (This is not a Serial ATA Connector) ..... | 18 |
| VGA Output .....  | 18 |
| Miscellaneous I/O .....   | 19 |
| Expansion Connectors .....  | 20 |
| EXP Interfaces .....  | 20 |
| <b>Configuration</b> .....  | 26 |
| Configuration Modes .....   | 26 |
| <b>Board Power</b> .....  | 27 |
| <b>Board Clocks</b> .....   | 29 |
| <b>PCB Stackup</b> .....  | 30 |



# Spartan-3A DSP 1800A Board Features

---

## Overview

The purpose of this manual is to describe the functionality and contents of the Spartan™-3A DSP Starter Platform from Xilinx. This document includes instructions for operating the board and descriptions of the hardware features.

## Design Description

The Spartan-3A Starter Platform provides a platform for engineers designing with the Xilinx Spartan-3A DSP FPGA. The board provides the necessary hardware to not only evaluate the advanced features of the Spartan-3A DSP but also to implement complete user applications using peripherals on the Spartan-3A DSP Starter Platform and/or EXP modules plugged into EXP expansion connectors on the Spartan-3A DSP Starter Platform.

## Features

The Spartan-3A DSP Starter Platform provides the following features:

- Xilinx 3SD1800A-FG676 FPGA
- Clocks
  - ◆ 125 MHz LVTTTL SMT Oscillator
  - ◆ LVTTTL Oscillator Socket
  - ◆ 25.175 MHz LVTTTL SMT Oscillator (Video clock)
- Memory
  - ◆ 128M x 32-bit DDR2 SDRAM
  - ◆ 16Mx8 Parallel / BPI Configuration Flash
  - ◆ 64Mb SPI Configuration / Storage Flash (with 4 extra SPI selects)
- Interfaces
  - ◆ 10/100/1000 PHY
  - ◆ JTAG Programming/Configuration Port
  - ◆ RS232 Port
  - ◆ Low-cost VGA
- Buttons and switches
  - ◆ 8 User LEDs
  - ◆ 8-position User DIP Switch
  - ◆ 4 User Push Button Switches

- ◆ Reset Push Button Switch
- User I/O and expansion
  - ◆ Digilent 6-pin header (2)
  - ◆ EXP Expansion Connector (2)
- Configuration and Debug
  - ◆ JTAG
  - ◆ SystemACE™ Module Connector
  - ◆ Eridon debug connector (SATA)

## Ordering Information

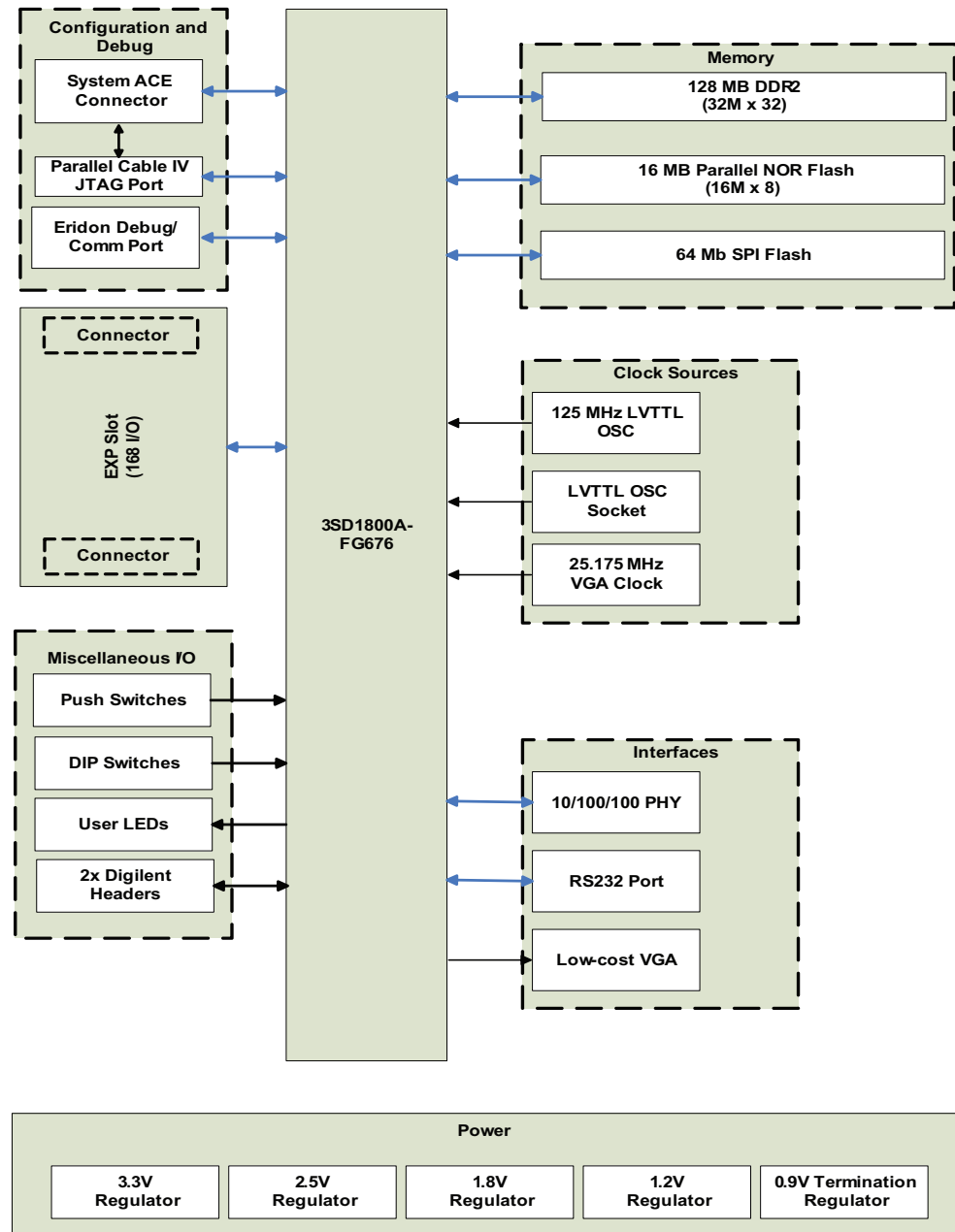
[Table 1](#) lists the evaluation kit part numbers.

*Table 1: Evaluation Kit and Hardware Ordering Information*

| Part Number             | Hardware   |
|-------------------------|--|
| HW-SD1800A-DSP-SB-UNI-G | XtremeDSP Starter Platform - Spartan-3A<br>DSP 1800A Edition |

# Functional Description

A high-level block diagram of the Spartan-3A DSP Starter Platform is shown in Figure 1. Subsequent sections provide details of the board design.



UGxxx\_01\_090407

Figure 1: Spartan-3A DSP Starter Platform Block Diagram

## Xilinx Spartan-3A DSP FPGA

The Xilinx XC3SD1800A-4FG676C device designed into the Spartan-3A DSP Starter Platform provides four I/O banks, two of which are fixed voltage and two of which are I/O voltage-selectable. The four I/O banks are described in Table 2 and detailed I/O pin usage is provided throughout this document. Note that in some cases, voltage translation of I/O signals may be necessary in order to meet requirements of peripheral devices that are connected to a particular I/O bank, or EXP modules plugged into the EXP expansion connectors. Table 2 indicates where voltage translation will occur or, if a source is fixed at a particular voltage, even though the bank to which it is connected may be at different I/O voltage.

Table 2: XC3SD1800A Input and Output Allocation

| I/O Bank Number | I/O Function            | Number of I/O Pins | Number of Input-only Pins | Voltage Translation | Bank I/O Voltage |
|-----------------|-------------------------|--------------------|---------------------------|---------------------|------------------|
| 0               | EXP Connector JX1       | 84                 | 0                         |                     | 2.5 or 3.3 V     |
| 0               | User Pushbuttons        | 0                  | 4                         |                     |                  |
| 0               | 8-pos DIP Switch        | 0                  | 8                         |                     |                  |
| 0               | 125 MHz Clock           | 1                  | 0                         |                     |                  |
| 0               | SMA Connector           | 1                  | 0                         |                     |                  |
| 0               | Configuration (PUDC_B)  | 1                  | 0                         |                     |                  |
| 1               | SystemACE Module        | 28                 | 1                         |                     | 3.3 V            |
| 1               | J3 Flash Memory         | 28                 | 0                         |                     |                  |
| 1               | SPI Selects (4)         | 4                  | 0                         |                     |                  |
| 1               | DAC                     | 14                 | 0                         |                     |                  |
| 1               | User LEDs               | 8                  | 0                         |                     |                  |
| 1               | Digilent Connectors     | 8 <sup>(1)</sup>   | 0                         |                     |                  |
| 1               | RS-232                  | 2                  | 0                         |                     |                  |
| 1               | Eridon Debug Connector  | 4                  | 0                         |                     |                  |
| 1               | Configuration (Suspend) | 1                  | 0                         |                     |                  |
| 1               | 25.175 MHz Clock        | 1                  | 0                         |                     |                  |
| 1               | EXP Connector JX2       | 8                  | 0                         | 2.5 or 3.3 V        |                  |



Table 2: XC3SD1800A Input and Output Allocation (Contd)

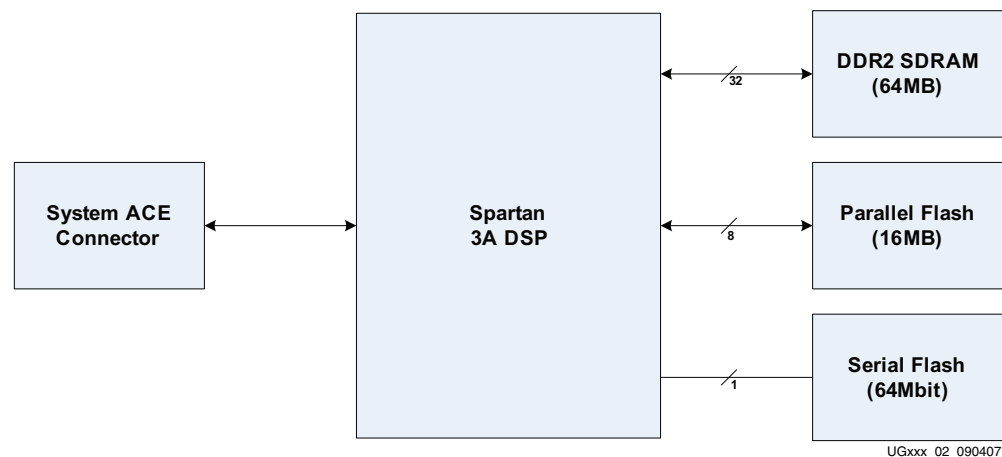
| I/O Bank Number | I/O Function      | Number of I/O Pins   | Number of Input-only Pins | Voltage Translation | Bank I/O Voltage |
|-----------------|-------------------|----------------------|---------------------------|---------------------|------------------|
| 2               | EXP Connector JX2 | 76                   | 0                         |                     | 2.5 or 3.3 V     |
| 2               | J3 Flash Memory   | 8 <sup>[Ref 1]</sup> | 0                         | 2.5 or 3.3 V        |                  |
| 2               | SPI               | 4 <sup>[Ref 1]</sup> | 0                         |                     |                  |
| 2               | Configuration     | 5                    | 0                         |                     |                  |
| 2               | Plug-in Reset     | 1                    | 0                         |                     |                  |
| 2               | LED               | 1                    | 0                         |                     |                  |
| 2               | Power-on Reset    | 0                    | 1                         |                     |                  |
| 3               | DDR2 Memory       | 73                   | 0                         |                     | 1.8 V            |
| 3               | Ethernet          | 17                   | 13                        | 2.5 V               |                  |

**Note:**

1. FLASH\_DO and SPI\_MISO are a common pin.

## Memory

The Spartan-3A DSP Starter Platform is populated with both high-speed RAM (128Mbytes DDR2) and non-volatile ROM (16Mbytes parallel, and 64Mbit serial) to support various types of applications. Additionally, a 50-pin connector is provided for SystemACE interface (not included) that can be used to configure the Spartan-3A DSP FPGA, and provide storage for A/V media files from removable Compact Flash cards. Figure 2 shows a high-level block diagram of the memory interfaces on this board



UGxxx\_02\_090407

Figure 2: Spartan-3A DSP Memory Interface

### Micron DDR2 SDRAM Interface

Two Micron MT47H32M16BM DDR2 devices provide 128Mbytes of 32-bit wide memory to the FPGA. The FPGA DDR2 interface supports SSTL18 signaling and all DDR2 signals

are controlled impedance. The DDR2 data, mask, and strobe signals are matched length across all signals. Using I/O Bank 3 the DDR2 pinout on the FPGA is MIG-compliant. Pinout of the FPGA DDR2 interface is provided in [Table 3](#) below.

SSTL18 Class I termination (series termination at the driving node and stub termination at the receiving node) is used between the FPGA and DDR on all unidirectional signals, such as Address, Control, and Clock. SSTL18 Class II termination (series and stub termination at both nodes) is used on the FPGA side of the interface for all bidirectional signals such as Data and Strobe. No board terminations are implemented for Data and Strobe on the memory side. ODT is strapped as enabled, although an FPGA I/O is still connected to allow the FPGA to drive this off. Note that stub terminations for address and control signals are not populated in production based on HyperLynx simulation and exhaustive, error-free testing of the FPGA-DDR2 interface at 133MHz. [Figure 4](#) provides details of terminator locations relative to the FPGA and the DDR2 memory devices.

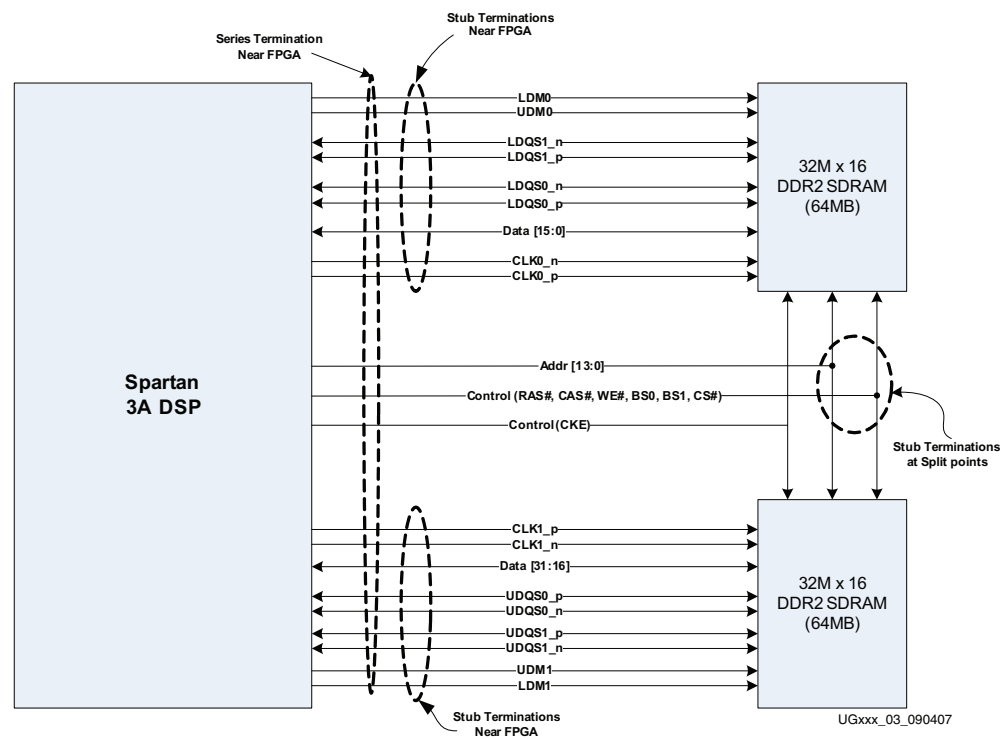


Figure 3: DDR2 SDRAM Interface

The following guidelines were used in the design of the DDR2 interface to the Spartan-3A DSP FPGA. These guidelines are based on Micron recommendations and board level simulation.

- Memory clocks routed differentially
- 50-ohm<sup>(1)</sup> controlled trace impedance
- 24-ohm<sup>(1)</sup> series termination on bidirectional signals at the FPGA
- Parallel termination following the memory device connection on all signals
- 60-ohm<sup>(1)</sup> pull-up resistor to the termination supply (0.9V) on data and srrobe signals at the FPGA
- 60-ohm<sup>(1)</sup> pull-up resistor to the termination supply at the split-point of shared signals (control, address)
- Termination supply that can both source and sink current
- Feedback clock routed with twice the length to simulate the total flight time

All DDR2 routing is length-matched within certain tolerances; these are:

- Members of a differential pair matched to +/-10mil
- DQ, DQS, DM and CK matched to +/- 45mil
- Control matched to +/- 100mil of data interface
- RST\_DQS\_DIV and MB\_FB\_CLK matched to +/- 45mil of sum of average DQS and average CK

The DDR2 signals are connected to I/O Bank 3 of the Spartan-3 SA DSP FPGA; the output supply pins (VCCO) for Bank 3 is connected to 1.8 Volts. A Texas Instruments TPS51116 Buck Controller and ancillary circuitry provides the 1.8V DDR2 power, the 0.9V termination voltage (FPGA\_0.9V\_TT) and the DDR2 reference voltage (FPGA\_DDR2\_VREF). Note that this power source also supplies the 1.8V core voltage to the Ethernet PHY.

**Table 3: FPGA DDR2 Interface Pinout**

| DDR2 Signal | FPGA Pin Number | DDR2 Signal      | FPGA Pin Number |
|-------------|-----------------|------------------|-----------------|
| FPGA_DDR_A0 | J5              | FPGA_DDR_LDM_0   | V2              |
| FPGA_DDR_A1 | M8              | FPGA_DDR_LDM_0   | V1              |
| FPGA_DDR_A2 | M10             | FPGA_DDR_LDM_1   | R2              |
| FPGA_DDR_A3 | K4              | FPGA_DDR_UDM_1   | M6              |
| FPGA_DDR_A4 | K5              | DDR2_ODT_Control | G3              |
| FPGA_DDR_A5 | K2              | FPGA_DDR_D0      | U9              |
| FPGA_DDR_A6 | K3              | FPGA_DDR_D1      | V8              |
| FPGA_DDR_A7 | L3              | FPGA_DDR_D2      | AB1             |
| FPGA_DDR_A8 | L4              | FPGA_DDR_D3      | AC1             |

1. Ideal impedance values are listed. Actual values may vary.

Table 3: FPGA DDR2 Interface Pinout (Contd)

| DDR2 Signal       | FPGA Pin Number | DDR2 Signal  | FPGA Pin Number |
|-------------------|-----------------|--------------|-----------------|
| FPGA_DDR_A9       | M7              | FPGA_DDR_D4  | Y5              |
| FPGA_DDR_A10      | M8              | FPGA_DDR_D5  | Y6              |
| FPGA_DDR_A11      | M3              | FPGA_DDR_D6  | U7              |
| FPGA_DDR_A12      | M4              | FPGA_DDR_D7  | U8              |
| FPGA_DDR_BS0      | K6              | FPGA_DDR_D8  | AA2             |
| FPGA_DDR_BS1      | J4              | FPGA_DDR_D9  | AA3             |
| FPGA_DDR_RAS#     | H1              | FPGA_DDR_D10 | Y1              |
| FPGA_DDR_CAS#     | L10             | FPGA_DDR_D11 | Y2              |
| FPGA_DDR_WE#      | L9              | FPGA_DDR_D12 | T7              |
| FPGA_DDR_CS#      | H2              | FPGA_DDR_D13 | U6              |
| FPGA_DDR_CKE      | L7              | FPGA_DDR_D14 | U5              |
| FPGA_DDR_CLK_0    | N1              | FPGA_DDR_D15 | V5              |
| FPGA_DDR_CLK_0#   | N2              | FPGA_DDR_D16 | R8              |
| FPGA_DDR_CLK_1    | N5              | FPGA_DDR_D17 | R7              |
| FPGA_DDR_CLK_1#   | N4              | FPGA_DDR_D18 | U1              |
| MB_FB_CLK (out)   | M2              | FPGA_DDR_D19 | U2              |
| MB_FB_CLK (in)    | N7              | FPGA_DDR_D20 | P8              |
| RST_DQS_DIV (out) | T10             | FPGA_DDR_D21 | P9              |
| RST_DQS_DIV (in)  | T9              | FPGA_DDR_D22 | R5              |
| FPGA_DDR_LDQS_0   | V7              | FPGA_DDR_D23 | R6              |
| FPGA_DDR_LDQS_#0  | V6              | FPGA_DDR_D24 | P7              |
| FPGA_DDR_LDQS_1   | W3              | FPGA_DDR_D25 | P6              |
| FPGA_DDR_LDQS_#_1 | W4              | FPGA_DDR_D26 | T3              |
| FPGA_DDR_UDQS_0   | T5              | FPGA_DDR_D27 | T4              |
| FPGA_DDR_UDQS_#0  | U4              | FPGA_DDR_D28 | N9              |
| FPGA_DDR_UDQS_1   | R2              | FPGA_DDR_D29 | P10             |
| FPGA_DDR_UDQS_#_1 | R4              | FPGA_DDR_D30 | P4              |
|                   |                 | FPGA_DDR_D31 | P3              |

## Intel J3 Parallel Flash

The Flash memory consists of a single J3 Flash device in a TSOP-56 package and connected to the dedicated BPI configuration port of the FPGA. The Intel JS28F128J3D is a 128-Mbit device organized as 16-Mbit x 8. The installed J3 device supports asynchronous memory accesses at a 75 nanosecond access time. The Flash interface is split across two banks, with all but the 8 data bits connected to Bank 1 (3.3V), and the 8 data bits connected to Bank 2. Because Bank 2 may be set to either 2.5V or 3.3V, the 8 Flash data bits are interfaced to Bank 2 via a Texas Instruments SN74AVC8T245 dual-supply bus transceiver with the Flash Write Enable (FLASH\_WE#) signal controlling transceiver direction and the Flash chip select signal (FLASH\_CS) enabling the transceiver. The maximum propagation delay of 2.9 nanoseconds through this transceiver is not significant with the 75 nanosecond Flash access time. Jumper JP1 may be used to write-protect the Flash memory by placing a shunt across pins 2 and 3. Default setting is JP1 1:2. [Table 4](#) details the Parallel Flash FPGA interface pinout.

**Table 4: Parallel Flash Interface Pinout**

| J3 Flash Signal | FPGA Pin No. | J3 Flash Signal | FPGA Pin No. |
|-----------------|--------------|-----------------|--------------|
| FLASH_A0        | AC23         | FLASH_A18       | J26          |
| FLASH_A1        | AC24         | FLASH_A19       | J25          |
| FLASH_A2        | R21          | FLASH_A20       | J21          |
| FLASH_A3        | R22          | FLASH_A21       | H21          |
| FLASH_A4        | T23          | FLASH_A22       | C26          |
| FLASH_A5        | T24          | FLASH_A23       | C25          |
| FLASH_A6        | R18          | FLASH_WE#       | Y20          |
| FLASH_A7        | R17          | FLASH_OE#       | AE26         |
| FLASH_A8        | R25          | FLASH_CE#       | AE25         |
| FLASH_A9        | R26          | FLASH_Reset#    | N24          |
| FLASH_A10       | M26          | FLASH_D0        | AF24         |
| FLASH_A11       | M25          | FLASH_D1        | AE18         |
| FLASH_A12       | L24          | FLASH_D2        | AF18         |
| FLASH_A13       | M23          | FLASH_D3        | Y15          |
| FLASH_A14       | N18          | FLASH_D4        | AE12         |
| FLASH_A15       | N17          | FLASH_D5        | AF12         |
| FLASH_A16       | N20          | FLASH_D6        | AF10         |
| FLASH_A17       | M20          | FLASH_D7        | AE10         |

## Intel S33 Serial Flash

Table 5: Serial (SPI) Flash Interface Pinout

| J3 Flash Signal | FPGA Pin | J3 Flash Signal | FPGA Pin |
|-----------------|----------|-----------------|----------|
| SPISEL_1        | W20      | * SPI_SEL#      | AA7      |
| SPISEL_1        | W21      | * SPI_CLK       | AE24     |
| SPISEL_1        | AD26     | * SPI_MOSI      | AB15     |
| SPISEL_1        | AC25     | * SPI_MISO      | AF24     |

## SystemACE Module (SAM) Connector

The Spartan-3A DSP Starter Platform provides a SAM 50-pin connector (J8) for SystemACE interface that can be used to configure the Spartan-3A DSP FPGA, and provide storage for A/V media files from removable Compact Flash cards. The Avnet SystemACE Module (DS-KIT-SYSTEMACE) can be used to perform both of these functions.

Further information on the Avnet SystemACE Module may be found at: [www.em.avnet.com/systemace](http://www.em.avnet.com/systemace). This SystemACE module is not provided as part of this product.

Figure 4 shows the SystemACE Module connected to the header on the Spartan-3A DSP board; Table 6 provides the pinout of SAM connector J8. The clock from the SAM connector (Pin 6) is routed to GCLK1 on Bank 2 of the FPGA.

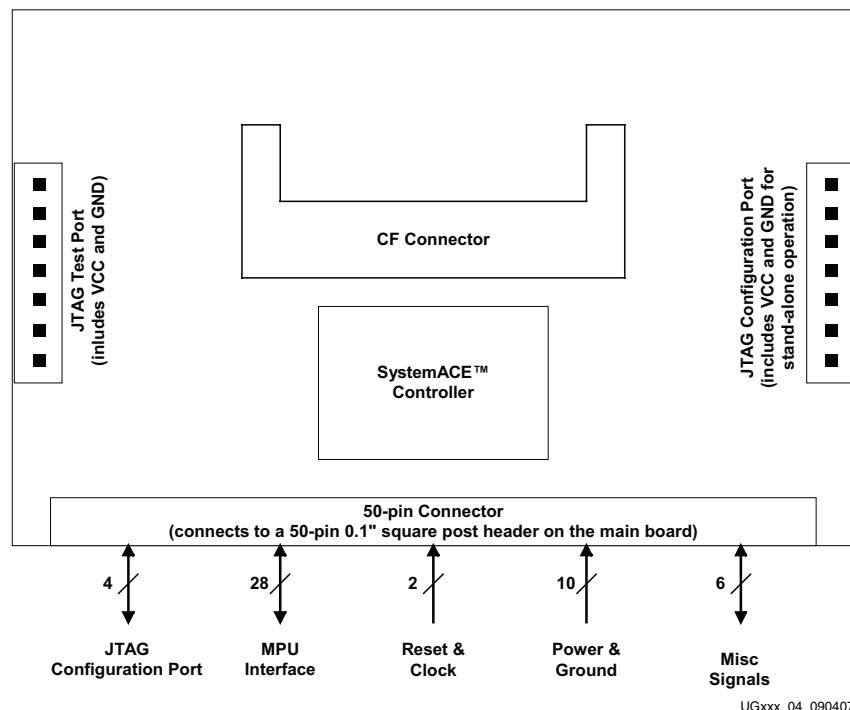


Figure 4: SystemACE Module Interconnections

**Table 6: SAM Interface Signals**

| FPGA Pin Number | SystemACE Signal Name  | SAM Connector Pin Number |    | SystemACE Signal Name  | FPGA Pin Number |
|-----------------|------------------------|--------------------------|----|------------------------|-----------------|
| —               | 3.3 V                  | 1                        | 2  | 3.3 V                  | —               |
| E23             | JTAG_TDO               | 3                        | 4  | GND                    | —               |
| D4              | JTAG_TMS               | 5                        | 6  | SAM_CLK                | AA14            |
| G7              | JTAG_TDI               | 7                        | 8  | GND                    | —               |
| A2              | FPGA_PROG <sub>n</sub> | 9                        | 10 | JTAG_TCK               | A25             |
| —               | GND                    | 11                       | 12 | GND                    | —               |
| V22             | SAM_OE <sub>n</sub>    | 13                       | 14 | FPGA_INIT <sub>n</sub> | AA15            |
| AC26            | SAM_A0                 | 14                       | 16 | SAM_WE <sub>n</sub>    | V24             |
| AB23            | SAM_A2                 | 17                       | 18 | SAM_A1                 | AB26            |
| —               | 2.5 V                  | 19                       | 20 | SAM_A3                 | AB24            |
| AA23            | SAM_D0                 | 21                       | 22 | 2.5 V                  | —               |
| U20             | SAM_D2                 | 23                       | 24 | SAM_D1                 | V21             |
| AA25            | SAM_D4                 | 25                       | 26 | SAM_D3                 | AA24            |
| U18             | SAM_D6                 | 27                       | 28 | SAM_D5                 | U19             |
| Y23             | SAM_D8                 | 29                       | 30 | SAM_D7                 | Y22             |
| T20             | SAM_D10                | 31                       | 32 | SAM_D9                 | U21             |
| Y25             | SAM_D12                | 33                       | 34 | SAM_D11                | Y24             |
| T17             | SAM_D14                | 35                       | 36 | SAM_D13                | T18             |
| V18             | SAM_A4                 | 37                       | 38 | SAM_D15                | W23             |
| AA22            | SAM_A6                 | 39                       | 40 | SAM_A5                 | V19             |
| L23             | SAM_IRQ                | 41                       | 42 | GND                    | —               |
| V23             | Sam_RESET <sub>n</sub> | 43                       | 44 | SAM_CE <sub>n</sub>    | V25             |
| AB21            | FPGA_DONE              | 45                       | 46 | SAM_BRDY               | P21             |
| AB24            | FPGA_CCLK              | 47                       | 48 | BITSTREAM*             | AF24            |
| —               | GND                    | 49                       | 50 | NC (Key)               | —               |

## Interfaces

The Spartan-3A DSP FPGA has access to Ethernet and RS232 physical layer transceivers for communication purposes. Network access is provided by a 10/100/1000 Mb/s Ethernet PHY, which is connected to the Spartan-3A via a standard GMII interface. The PHY connects to the outside world with a standard RJ45 connector. Serial port communication to the FPGA fabric is provided through an RS232 transceiver using a DB9 DCE female connector.

Other interfaces consist of two 0.1" 6-pin headers to accept Digilent plug-in modules, a 7-pin Serial ATA connector (this is not a serial ATA interface) to connect to an Eridon debug module, and a 0.1" 2 x 6 header for SPI interface expansion.

### National Semiconductor 10/100/1000 Ethernet PHY

The PHY is a National DP83865DVH Gig PHYTER™ V. The DP83865 is a low power version of National's Gig PHYTER V with a 1.8V core voltage and 2.5V I/O voltage. The PHY also supports 3.3V I/O, but the 2.5V option is used on the board. The PHY is connected to a Tyco-AMP RJ-45 jack with integrated magnetics (part number: 1-6605833-1). The jack also integrates two LEDs and their corresponding resistors as well as several other passive components. External logic is used to logically OR the three link indicators for 10, 100 and 1000 Mb/s to drive a Link LED on the RJ-45 jack. The external logic is for the default strap options and may not work if the strap options are changed. Four more LEDs are provided on the board for status indication. These LEDs indicate Link at 10 Mb/s, Link at 100 Mb/s, Link at 1000 Mb/s and Full Duplex operation. The PHY clock is generated from its own 25 MHz crystal (FOX FX325BS). [Figure 5](#) shows a high-level block diagram of the interface to the DP83865 Tri-mode Ethernet PHY. [Table 7](#) lists the PHY signal connections at the FPGA. Note that these signals are connected to FPGA Bank 3 which is fixed at +1.8V I/O voltage, necessitating voltage translation between +1.8V and +2.5V to match the PHY I/O voltage requirements.

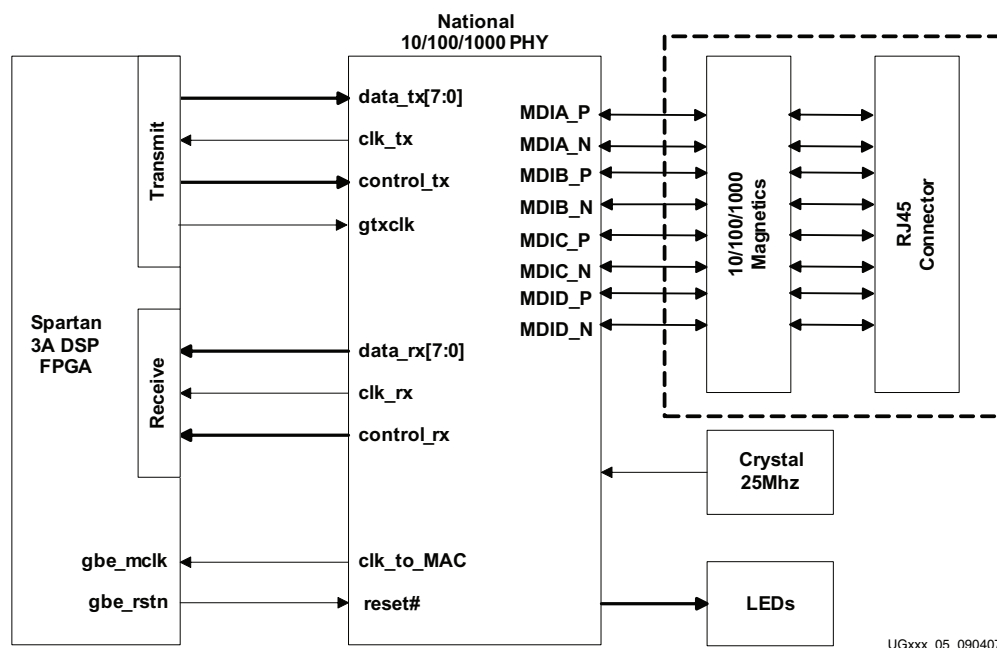


Figure 5: 10/100/1000 Mb/s Ethernet Interface



**Table 7: Ethernet PHY Interface Signals**

| Ethernet PHY Signal | FPGA Pin | Ethernet PHY Signal | FPGA Pin |
|---------------------|----------|---------------------|----------|
| ETH_Tx_D            | J8       | ETH_COL             | Y3       |
| ETH_Tx_D            | J9       | ETH_INT#            | J1       |
| ETH_Tx_D            | B2       | ETH_Rx_DV           | D1       |
| ETH_Tx_D            | B1       | ETH_Rx_ER           | J3       |
| ETH_Tx_D            | G6       | ETH_MCLK            | N6       |
| ETH_Tx_D            | H7       | ETH_Rx_CLK          | P1       |
| ETH_Tx_D            | K9       | ETH_Tx_CLK          | P2       |
| ETH_Tx_D            | K8       | ETH_Rx_D0           | C2       |
| ETH_Tx_EN           | D3       | ETH_Rx_D1           | G2       |
| ETH_Tx_ER           | E4       | ETH_Rx_D2           | G5       |
| ETH_GTX_CLK         | E3       | ETH_Rx_D3           | D2       |
| ETH_MDC             | F4       | ETH_Rx_D4           | Ab3      |
| ETH_MDIO            | F5       | ETH_Rx_D5           | Aa4      |
| ETH_RST#            | G4       | ETH_Rx_D6           | Ab4      |
| ETH_CR_S            | G1       | ETH_Rx_D7           | Y4       |

The PHY address is set to 0b00001 by default. PHY address 0b00000 is reserved for a test mode and should not be used. Three-pad resistor jumpers are used to set the strapping options. These jumper pads provide the user with the ability to change the settings by moving the resistors. The dual-function pins that are used for both a strapping option and to drive an LED have a set of two jumpers per pin. The dual-function pins are indicated by an asterisk in the table.

The default options as indicated in [Table 8](#) below are Auto-Negotiation enabled, Full Duplex mode, Speed advertised as 10/100/1000 Mb/s, PHY address 0b00001, IEEE Compliant and Non-compliant support, straight cable in non-MDIX mode, auto-MDIX mode enabled, Single node (NIC) and CLK\_TO\_MAC enabled. These and other settings are enabled by three-pad jumpers with a resistor connecting either pads 1 and 2 or pads 2 and 3.

**Table 8: Ethernet PHY Hardware Strapping Options**

| Function         | Jumper Installation | Resistor | Mode Enabled                       |
|------------------|---------------------|----------|------------------------------------|
| Auto Negotiation | JT8: Pins 1-2       | 0 Ohm    | Auto-negotiation enabled (default) |
|                  | JT9: Pins 1-2       |          |                                    |
|                  | JT8: Pins 2-3       | 0 Ohm    | Auto-negotiation disabled          |
|                  | JT9: Pins 2-3       |          |                                    |

Table 8: Ethernet PHY Hardware Strapping Options

| Function                | Jumper Installation                                  | Resistor | Mode Enabled  |
|-------------------------|--|----------|---|
| Full/Half Duplex*       | JT10: Pins 1-2                                       | 0 Ohm    | Full Duplex (default)   |
|                         | JT10: Pins 1-2                                       |          |   |
|                         | JT10: Pins 2-3                                       | 0 Ohm    | Half Duplex   |
|                         | JT11: Pins 2-3                                       |          |   |
| Speed 1*                | JT12: Pins 1-2<br>JT13: Pins 1-1<br><br>(Speed1 – 0) | 0 ohm    | Speed Selection: (Auto-Neg enabled)<br>Speed1 Speed0 Speed Advertised<br>1 1 1000BASE-T, 10BASE-T<br>1 0 1000BASE-T |
| Speed 0*                | JT6: Pins 1-2<br>JT7: Pins 1-1<br><br>(Speed0 – 0)   | 0 Ohm    | 0 1 1000BASE-T, 100BASE-Tx<br>0 0 10BASE-T<br><br>Default: 1000BASE-T, 100BASE-TX, 10BASE-T                         |
| PHY address 0*          | JT14: Pins 1-2                                       | 0 Ohm    | PHY Address 0b00001 (default)   |
|                         | JT15: Pins 1-2                                       |          |   |
|                         | JT24: Pins 2-3                                       |          | PHY Address 0b00000   |
|                         | JT25: Pins 2-3                                       |          |   |
| Non-IEEE Compliant Mode | JT1: Pins 1-2  | 1 K      | Compliant and non-compliant operation (default)   |
|                         | JT1: Pins 2-3  |          | Inhibits non-compliant operation  |
| Manual MDIX Setting     | JT39: Pins 1-2                                       | 1 K      | Straight Mode (default)   |
|                         | JT2: Pins 2-3  |          | Cross-over Mode   |
| Auto MDIX Setting       | JT4: Pins 1-2  | 1 K      | Automatic Pair Swap – MDIX (default)  |
|                         | JT4: Pins 2-3  |          | Set to manual preset – Manual MDIX Setting (JT12)   |
| Multiple Node Enable    | JT3: Pins 1-2  | 1 K      | Single node – NIC (default)   |
|                         | JT3: Pins 2-3  |          | Multiple node priority – switch/hub   |
| Clock to MAC Enable     | JT5: Pins 1-2  | 1 K      | CLK_TO_MAC output enabled (default)   |
|                         | JT5: Pins 2-3  |          | CLK_TO_MAC output disabled  |

The auto-MDIX mode provides automatic swapping of the differential pairs. This allows the PHY to work with either a straight-through cable or crossover cable. Use a CAT-5e or CAT-6 Ethernet cable when operating at 1000 Mb/s (Gigabit Ethernet). The boundary-scan Test Access Port (TAP) controller of the DP83865 must be in reset for normal operation. This active low reset pin of the TAP (TRST) is pulled low through a 1K resistor on the board.

## RS232

The RS232 transceiver is a Texas Instruments MAX3221 device. This transceiver operates at 3.3V with an internal charge pump to create the RS232 compatible output levels. The RS232 interface is brought out on DB9 connector P2. This RS232 interface supports only null-modem serial cables. A male-to-female serial cable should be used to plug J11 into a standard PC serial port (male DB9). [Table 9](#) shows the FPGA pin-out for the RS232 interface.

**Table 9: RS232 Signals**

| Net Name      | Description       | FPGA Pin Number |
|---------------|-------------------|-----------------|
| FPGA_RS232_Rx | Receive data, RD  | N21             |
| FPGA_RS232_Tx | Transmit data, TD | P22             |

## SPI Expansion

A 0.1" 2 x 6 header (J10) provides an expansion of the FPGA SPI interface. In addition to the SPI signals SPI\_SEL#, SPI\_CLK, SPI\_MOSI and SPI\_MISO, four additional SPI select signals are provided (SPISEL\_1, SPISEL\_2, SPISEL\_3, and SPISEL\_4). All SPI select signals have 4.7K pull-ups, SPI\_CLK has a 4.7K pull-down. 3.3V power and Ground are also provided on J10. [Table 10](#) lists and describes the J10 connections.

**Table 10: SPI Connector (J10)**

| FPGA Pin Number | Signal   | J10 Pin Number | J10 Pin Number | Signal   | FPGA Pin Number |
|-----------------|----------|----------------|----------------|----------|-----------------|
| W20             | SPISEL_1 | 2              | 1              | SPI_SEL# | AA7             |
| W21             | SPISEL_2 | 4              | 3              | SPI_MOSI | Ab15            |
| AD26            | SPISEL_3 | 6              | 5              | SPI_MISO | AF24            |
| AC25            | SPISEL_4 | 8              | 7              | SPI_CLK  | AE24            |
| —               | GND      | 10             | 9              | GND      | —               |
| —               | 3.3 V    | 12             | 11             | 3.3 V    | —               |

## Digilent Headers

Two right-angle, 6 pin (1 x 6 female) Digilent headers (J6, J7) are provided on the Spartan-3A DSP Starter Platform. Each header provides 3.3V power, Ground, and four I/O's. It "looks" like an SPI port, or can be used as 4 general purpose I/O's. [Figure 6](#) shows the pinout of the Digilent headers; [Table 11](#) provides the FPGA pinout.

For Digilent modules, see:

<http://www.digilentinc.com/Products/Catalog.cfm?Nav1=Products&Nav2=Peripheral&Cat=Peripheral>

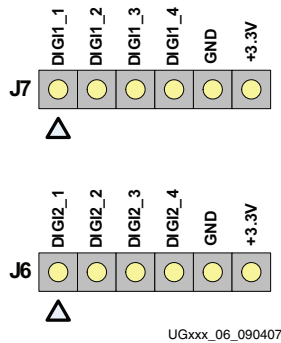


Figure 6: Digilent Header Pinout

Table 11: Digilent Header Connections

| J6 Signal | FPGA Pin | J7 Signal | FPGA Pin |
|-----------|----------|-----------|----------|
| DIGI2_1   | K19      | DIGI1_1   | L18      |
| DIGI2_2   | K18      | DIGI1_2   | L17      |
| DIGI2_3   | F22      | DIGI1_3   | E24      |
| DIGI2_4   | G22      | DIGI1_4   | F23      |

### Eridon Debug Connector (This is not a Serial ATA Connector)

A Serial ATA connector (J3) provides a high-speed interface for use with an Eridon debug module, but may be used as a general-purpose communication interface. Two 3.3V LVDS differential pairs, nominally one transmit pair (DBG\_Tx\_p/DBG\_Tx\_n) and one receive pair (DBG\_Rx\_p/DBG\_Rx\_n), provide this high-speed communication channel. Common-mode of the transmit pair is set to 1.25V by resistor R11 to 3.3V and resistor R8 to Ground. 100-ohm differential termination of the receive pair is provided by resistor R10. Nominal trace impedance is 50-ohms, with 49.9-ohm series resistors placed close to the FPGA. Table 12 identifies the connection of the J3 signals to the FPGA. See [www.eridon.com](http://www.eridon.com) for further information.

Table 12: Eridon Debug Connector (J3)

| J3 Pin Number | Signal Name | FPGA Pin |
|---------------|-------------|----------|
| 1             | GND         | —        |
| 2             | DBG_Tx_n    | D26      |
| 3             | DBG_Tx_p    | E26      |
| 4             | GND         | —        |
| 5             | DBG_Rx_n    | J20      |
| 6             | DBG_Rx_p    | J10      |
| 7             | GND         | —        |

## VGA Output

The Spartan-3A DSP Starter Platform includes a VGA video output using a resistor-divider network and 4-bits per RGB color as shown in Figure 7. This resistor-divider network is 510, 1K, 2K, & 4K ohms for each color. The outputs of the three resistor-divider networks are presented to DB15 connector P1. Horizontal and Vertical synchronization signals are also generated by the FPGA and provided to P1. Additionally, a 25.175 MHz clock (VGA-resolution) is added to the board, feeding directly to the FPGA at RHCLK2 (P26) on Bank 1. This clock should be used in the FPGA controller for timing the output and generating the image and syncs. The VGA pin assignments are listed in Table 13.

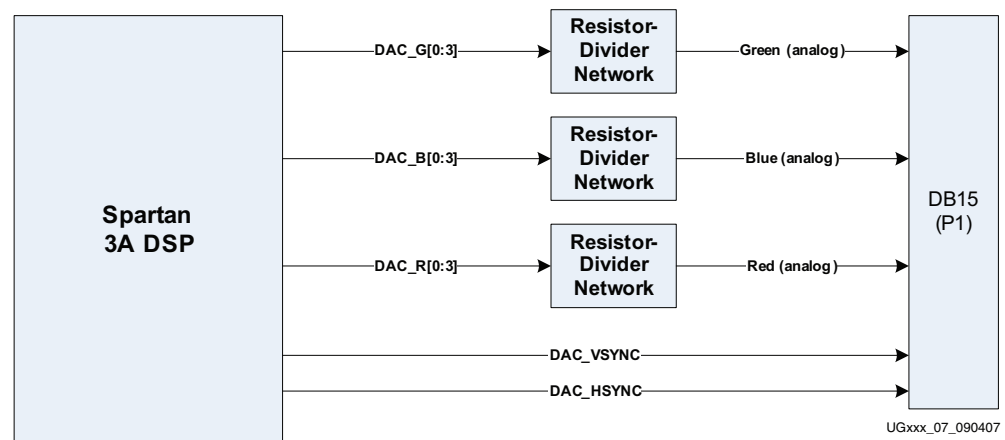


Figure 7: VGA Output

Table 13: VGA Pin Assignments

| VGA Signal | FPGA Pin | VGA Signal    | FPGA Pin |
|------------|----------|---------------|----------|
| DAC_G0     | M19      | DAC_R0        | L20      |
| DAC_G1     | M18      | DAC_R1        | K20      |
| DAC_G2     | J23      | DAC_R2        | F25      |
| DAC_G3     | J22      | DAC_R3        | F24      |
| DAC_B0     | L22      | DAC_VSYNC     | K25      |
| DAC_B1     | K21      | DAC_HSYNC     | K26      |
| DAC_B2     | G23      | CLK_25.175MHz | P26      |
| DAC_B3     | G24      |               |          |

## Miscellaneous I/O

An 8-position DIP switch, 4 user Pushbuttons, and 8 user LEDs are provided on the Spartan-3A DSP Starter Platform. The connection of these devices to the FPGA is detailed in [Table 14](#). The DIP switch is connected to FPGA Bank 0 and each switch is pulled low in the “OFF” position. Turning the switch “ON” causes the corresponding FPGA pin to be pulled to 2.5V or 3.3V, depending on the setting of the Bank 0 I/O voltage (VCCO\_0). Like the DIP switch, the four user pushbuttons are also pulled low and depressing any button will cause the corresponding FPGA pin to be driven to the value of VCCO\_0. Driving a “high” to the LEDs will cause them to light.

**Table 14: Devices and Pin Assignments**

| Device       | Name             | FPGA Pin |
|--------------|------------------|----------|
| DIP Switch   | SW3.1            | A7       |
|              | SW3.2            | G16      |
|              | SW3.3            | E9       |
|              | SW3.4            | D16      |
|              | SW3.5            | D19      |
|              | SW3.6            | B24      |
|              | SW3.7            | A5       |
|              | SW3.8            | A23      |
| Push Buttons | SW5 (SWITCH_PB1) | J17      |
|              | SW6 (SWITCH_PB2) | J15      |
|              | SW7 (SWITCH_PB3) | J13      |
|              | SW8 (SWITCH_PB4) | J10      |
| LEDs         | LED1 (D14)       | P18      |
|              | LED2 (D13)       | P25      |
|              | LED3 (D12)       | N19      |
|              | LED4 (D11)       | K22      |
|              | LED5 (D10)       | H20      |
|              | LED6 (D9)        | G21      |
|              | LED7 (D8)        | D24      |
|              | LED8 (D7)        | D25      |

## Expansion Connectors

The Spartan-3A DSP Starter Platform provides expansion capabilities for customized user application daughter cards and interfaces over two EXP expansion connectors. The EXP expansion connectors on the board can support two half-card EXP modules, or a single dual slot EXP module. Both off-the-shelf EXP modules and user-developed modules can easily be plugged onto the Spartan-3A DSP Starter Platform to add features and functions to the backend application of the main board.

## EXP Interfaces

The EXP specification defines a 132-pin connector, with 24 power I/Os, 24 grounds I/Os, and 84 user I/Os. The standard EXP configuration implemented on the Spartan-3A DSP Starter Platform uses two connectors (Samtec part number QTE-060-09-F-D-A) in a dual slot EXP configuration, for a total of 168 user I/Os. Using a jumper, you can set the voltage levels for the EXP user I/O to either 2.5V or 3.3V. As shown in Figure 8, JP2 and JP3 set the I/O voltage for the EXP connectors labeled JX1 and JX2 respectively, by setting the VCCO voltage for the banks of the FPGA that connect to the EXP I/O. Table 15 provides an overview of the EXP signals; Tables 17 and 18 provide the FPGA pinouts for EXP connectors JX1 and JX2, respectively. Note that Table 16 and Table 17 do not show the connector ground blades (numbered 122 through 131 on the schematic and PCB) that are positioned in the center of the connector. Technically, these are not *pins* and are not identified as such in this document.

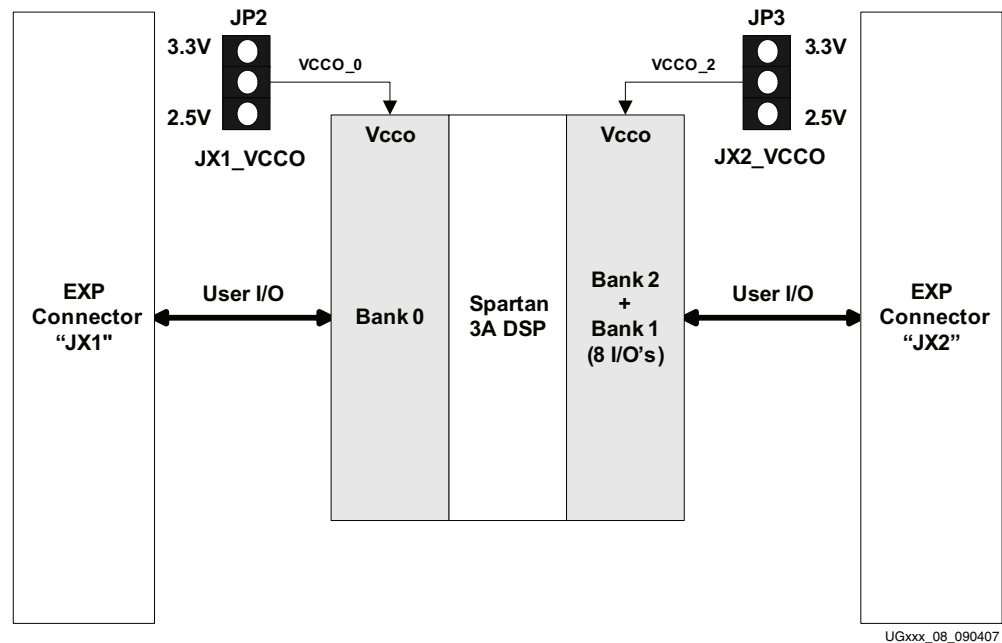


Figure 8: EXP I/O Voltage Settings

The EXP specification defines four user signal types:

Single Ended I/O, Differential I/O, Differential, Single Ended Clock Inputs, and Differential and Single Ended Clock Outputs. Because the FPGA I/Os can be configured for either single-ended or differential use, the differential I/Os defined in the EXP specification can serve a dual role. All the differential I/O signals can be configured as either differential pairs or single-ended signals, as required by the end application. In providing differential signaling, higher performance LVDS interfaces can be implemented between the baseboard and EXP module. Connection to high speed A/Ds, D/As, and flat panel displays are possible with this signaling configuration. Applications that require

single-ended signals only can use each differential pair as two single-ended signals, for a total of 84 single-ended I/O per connector (168 total in the dual slot configuration).

**Table 15: EXP Connector Signals**

| Net Names                          | Signal Description                    | Quantity | Quantity per Dual Slot |
|------------------------------------|---------------------------------------|----------|------------------------|
| EXP <sub>x</sub> _SE_IO            | Single-ended I/O                      | 34       | 68                     |
| EXP <sub>x</sub> _SE_CLK_IN        | Single-ended clock inputs             | 2        | 4                      |
| EXP <sub>x</sub> _DIFF_p/n         | Differential I/O pairs                | 22       | 44                     |
| EXP <sub>x</sub> _DIFF_CLK_IN_p/n  | Differential clock input pair, global | 1        | 2                      |
| EXP <sub>x</sub> _DIFF_CLK_OUT_p/n | Differential clock output pairs       | 1        | 2                      |
| Total                              |                                       | 64       | 168                    |

The Spartan-3A DSP FPGA user I/O pins that connect to the two EXP connectors are shown in the following tables. The Samtec QTE connector plugs on the Spartan-3A DSP Starter Platform (part number: QTE-060-09-F-D-A) mate with the Samtec QSE high-performance receptacles (part number: QSE-060-01-F-D-A), located on the daughter card. Samtec also provides several high-performance ribbon cables that will mate to the JX1 and JX2 connectors.

**Table 16: EXP Connector JX1 Pinout**

| FPGA Pin No. | Net Name      | EXP Connector Pin No. (JX1) |    | Net Name      | FPGA Pin No. |
|--------------|---------------|-----------------------------|----|---------------|--------------|
| C22          | EXP1_SE_IO_0  | 2                           | 1  | EXP1_SE_IO_1  | G20          |
| A22          | EXP1_SE_IO_2  | 4                           | 3  | EXP1_SE_IO_3  | G19          |
| -            | 2.5V          | 6                           | 5  | 2.5V          | -            |
| C21          | EXP1_SE_IO_4  | 8                           | 7  | EXP1_SE_IO_5  | E21          |
| B21          | EXP1_SE_IO_6  | 10                          | 9  | EXP1_SE_IO_7  | D23          |
| -            | 2.5V          | 12                          | 11 | 2.5V          | -            |
| C20          | EXP1_SE_IO_8  | 14                          | 13 | EXP1_SE_IO_9  | B23          |
| B20          | EXP1_SE_IO_10 | 16                          | 15 | EXP1_SE_IO_11 | C23          |
| -            | 2.5V          | 18                          | 17 | 2.5V          | -            |
| A20          | EXP1_SE_IO_12 | 20                          | 19 | EXP1_SE_IO_13 | D22          |
| D20          | EXP1_SE_IO_14 | 22                          | 21 | EXP1_SE_IO_15 | D21          |
| -            | 2.5V          | 24                          | 23 | 2.5V          | -            |
| -            | 2.5V          | 24                          | 23 | 2.5V          | -            |
| B19          | EXP1_SE_IO_16 | 26                          | 25 | EXP1_SE_IO_17 | F20          |
| A19          | EXP1_SE_IO_18 | 28                          | 27 | EXP1_SE_IO_19 | H17          |
| -            | 2.5V          | 30                          | 29 | 2.5V          | -            |



**Table 16: EXP Connector JX1 Pinout (Contd)**

| FPGA Pin No. | Net Name            | EXP Connector Pin No. (JX1) |    | Net Name        | FPGA Pin No. |
|--------------|---------------------|-----------------------------|----|-----------------|--------------|
| C18          | EXP1_SE_IO_20       | 32                          | 31 | EXP1_SE_IO_21   | F19          |
| B18          | EXP1_SE_IO_22       | 34                          | 33 | EXP1_SE_IO_23   | G17          |
| -            | 2.5V                | 36                          | 35 | 2.5V            | -            |
| A18          | EXP1_SE_IO_24       | 38                          | 37 | EXP1_SE_IO_25   | K16          |
| C17          | EXP1_SE_IO_26       | 40                          | 39 | EXP1_SE_IO_27   | F17          |
| B14          | EXP1_DIFF_CLK_IN_p  | 42                          | 41 | EXP1_SE_IO_28   | D18          |
| A14          | EXP1_DIFF_CLK_IN_n  | 44                          | 43 | EXP1_SE_CLK_IN  | J14          |
| -            | GND                 | 46                          | 45 | GND             | -            |
| D17          | EXP1_SE_IO_30       | 48                          | 47 | EXP1_SE_IO_29   | E17          |
| B17          | EXP1_SE_IO_31       | 50                          | 49 | EXP1_SE_CLK_OUT | G10          |
|              | GND                 | 52                          | 51 | GND             | -            |
| D16          | EXP1_DIFF_p20       | 54                          | 53 | EXP1_DIFF_p21   | B15          |
| C15          | EXP1_DIFF_n20       | 56                          | 55 | EXP1_DIFF_n21   | A15          |
| -            | GND                 | 58                          | 57 | GND             | -            |
| D13          | EXP1_DIFF_p18       | 60                          | 59 | EXP1_SE_IO_32   | C16          |
| C12          | EXP1_DIFF_n18       | 62                          | 61 | EXP1_SE_IO_33   | J16          |
| -            | GND                 | 64                          | 63 | GND             | -            |
| A12          | EXP1_DIFF_p16       | 66                          | 65 | EXP1_DIFF_p19   | F15          |
| B12          | EXP1_DIFF_n16       | 68                          | 67 | EXP1_DIFF_n19   | E15          |
| -            | GND                 | 70                          | 69 | GND             | -            |
| A4           | EXP1_DIFF_CLK_OUT_p | 72                          | 71 | EXP1_DIFF_p17   | E14          |
| B4           | EXP1_DIFF_CLK_OUT_n | 74                          | 73 | EXP1_DIFF_n17   | F14          |
| -            | GND                 | 76                          | 75 | GND             | -            |
| C11          | EXP1_DIFF_p14       | 78                          | 77 | EXP1_DIFF_p15   | G15          |
| D11          | EXP1_DIFF_n14       | 80                          | 79 | EXP1_DIFF_n15   | H15          |
| C10          | EXP1_DIFF_p12       | 82                          | 81 | EXP1_DIFF_p13   | G12          |
| D10          | EXP1_DIFF_n12       | 84                          | 83 | EXP1_DIFF_n13   | H12          |
| -            | 3.3V                | 86                          | 85 | 3.3V            | -            |
| -            | 3.3V                | 86                          | 85 | 3.3V            | -            |

Table 16: EXP Connector JX1 Pinout (Contd)

| FPGA Pin No. | Net Name           | EXP Connector Pin No. (JX1) |     | Net Name      | FPGA Pin No. |
|--------------|--------------------|-----------------------------|-----|---------------|--------------|
| B13          | EXP1_RCLK_DIFF_p10 | 88                          | 87  | EXP1_DIFF_p11 | E12          |
| C13          | EXP1_RCLK_DIFF_n10 | 90                          | 89  | EXP1_DIFF_n11 | F12          |
| A9           | EXP1_DIFF_p8       | 94                          | 93  | EXP1_DIFF_p9  | J12          |
| B9           | EXP1_DIFF_n8       | 96                          | 95  | EXP1_DIFF_n9  | K12          |
| -            | 3.3V               | 98                          | 97  | 3.3V          | -            |
| A8           | EXP1_DIFF_p6       | 100                         | 99  | EXP1_DIFF_p7  | A10          |
| B8           | EXP1_DIFF_n6       | 102                         | 101 | EXP1_DIFF_n7  | B10          |
| -            | 3.3V               | 104                         | 103 | 3.3V          | -            |
| B7           | EXP1_DIFF_p4       | 106                         | 105 | EXP1_DIFF_p5  | E10          |
| C7           | EXP1_DIFF_n4       | 108                         | 107 | EXP1_DIFF_n5  | D9           |
| -            | 3.3V               | 110                         | 109 | 3.3V          | -            |
| B6           | EXP1_DIFF_p2       | 112                         | 111 | EXP1_DIFF_p3  | C8           |
| C6           | EXP1_DIFF_n2       | 114                         | 113 | EXP1_DIFF_n3  | D8           |

Table 17: EXP Connector JX2 Pinout

| FPGA Pin No. | Net Name      | EXP Connector Pin No. (JX1) |    | Net Name      | FPGA Pin No. |
|--------------|---------------|-----------------------------|----|---------------|--------------|
| V16          | EXP2_SE_IO_0  | 2                           | 1  | EXP2_SE_IO_1  | AE25         |
| Y17          | EXP2_SE_IO_2  | 4                           | 3  | EXP2_SE_IO_3  | AF25         |
| -            | 2.5V          | 6                           | 5  | 2.5V          | -            |
| AA18         | EXP2_SE_IO_4  | 8                           | 7  | EXP2_SE_IO_5  | AE23         |
| AC20         | EXP2_SE_IO_6  | 10                          | 9  | EXP2_SE_IO_7  | AF23         |
| -            | 2.5V          | 12                          | 11 | 2.5V          | -            |
| AA17         | EXP2_SE_IO_8  | 14                          | 13 | EXP2_SE_IO_9  | AD22         |
| AC19         | EXP2_SE_IO_10 | 16                          | 15 | EXP2_SE_IO_11 | AE21         |
| -            | 2.5V          | 18                          | 17 | 2.5V          | -            |
| AB18         | EXP2_SE_IO_12 | 20                          | 19 | EXP2_SE_IO_13 | AD21         |
| V15          | EXP2_SE_IO_14 | 22                          | 21 | EXP2_SE_IO_15 | AC21         |
| -            | 2.5V          | 24                          | 23 | 2.5V          | -            |
| W15          | EXP2_SE_IO_16 | 26                          | 25 | EXP2_SE_IO_17 | U23          |
| AB16         | EXP2_SE_IO_18 | 28                          | 27 | EXP2_SE_IO_19 | U24          |

**Table 17: EXP Connector JX2 Pinout (Contd)**

| FPGA Pin No. | Net Name            | EXP Connector Pin No. (JX1) |    | Net Name        | FPGA Pin No. |
|--------------|---------------------|-----------------------------|----|-----------------|--------------|
| -            | 2.5V                | 30                          | 29 | 2.5V            | -            |
| M21          | EXP2_SE_IO_20       | 32                          | 31 | EXP2_SE_IO_21   | AD20         |
| AC16         | EXP2_SE_IO_22       | 34                          | 33 | EXP2_SE_IO_23   | AF19         |
| -            | 2.5V                | 36                          | 35 | 2.5V            | -            |
| U22          | EXP2_SE_IO_24       | 38                          | 37 | EXP2_SE_IO_25   | AE19         |
| AC15         | EXP2_SE_IO_26       | 40                          | 39 | EXP2_SE_IO_27   | AD19         |
| AA13         | EXP2_DIFF_CLK_IN_p  | 42                          | 41 | EXP2_SE_IO_28   | R20          |
| Y13          | EXP2_DIFF_CLK_IN_n  | 44                          | 43 | EXP2_SE_CLK_IN  | AF13         |
| -            | GND                 | 46                          | 45 | GND             | -            |
| V14          | EXP2_SE_IO_30       | 48                          | 47 | EXP2_SE_IO_29   | R19          |
| U15          | EXP2_SE_IO_31       | 50                          | 49 | EXP2_SE_CLK_OUT | Y14          |
| -            | GND                 | 52                          | 51 | GND             | -            |
| V10          | EXP2_DIFF_p20       | 54                          | 53 | EXP2_DIFF_p21   | AD14         |
| W10          | EXP2_DIFF_n20       | 56                          | 55 | EXP2_DIFF_n21   | AC14         |
| -            | GND                 | 58                          | 57 | GND             | -            |
| V13          | EXP2_DIFF_p18       | 60                          | 59 | EXP2_SE_IO_32   | K23          |
| W13          | EXP2_DIFF_n18       | 62                          | 61 | EXP2_SE_IO_33   | M22          |
| -            | GND                 | 64                          | 63 | GND             | -            |
| Y12          | EXP2_DIFF_p16       | 66                          | 65 | EXP2_DIFF_p19   | AB12         |
| AA12         | EXP2_DIFF_n16       | 68                          | 67 | EXP2_DIFF_n19   | AC12         |
| -            | GND                 | 70                          | 69 | GND             | -            |
| W17          | EXP2_DIFF_CLK_OUT_p | 72                          | 71 | EXP2_DIFF_p17   | AE17         |
| V17          | EXP2_DIFF_CLK_OUT_n | 74                          | 73 | EXP2_DIFF_n17   | AD17         |
| -            | GND                 | 76                          | 75 | GND             | -            |
| V12          | EXP2_DIFF_p14       | 78                          | 77 | EXP2_DIFF_p15   | AF20         |
| W12          | EXP2_DIFF_n14       | 80                          | 79 | EXP2_DIFF_n15   | AE20         |
| AD11         | EXP2_DIFF_p12       | 82                          | 81 | EXP2_DIFF_p13   | AE9          |
| AC11         | EXP2_DIFF_n12       | 84                          | 83 | EXP2_DIFF_n13   | AF9          |
| -            | 3.3V                | 86                          | 85 | 3.3V            | -            |

Table 17: EXP Connector JX2 Pinout (Contd)

| FPGA Pin No. | Net Name           | EXP Connector Pin No. (JX1) |     | Net Name      | FPGA Pin No. |
|--------------|--------------------|-----------------------------|-----|---------------|--------------|
| AF14         | EXP2_RCLK_DIFF_p10 | 88                          | 87  | EXP2_DIFF_p11 | AE8          |
| AE14         | EXP2_RCLK_DIFF_n10 | 90                          | 89  | EXP2_DIFF_n11 | AF8          |
| -            | 3.3V               | 92                          | 91  | 3.3V          | -            |
| AB9          | EXP2_DIFF_p8       | 94                          | 93  | EXP2_DIFF_p9  | AD7          |
| AC9          | EXP2_DIFF_n8       | 96                          | 95  | EXP2_DIFF_n9  | AE7          |
| -            | 3.3V               | 98                          | 97  | 3.3V          | -            |
| Y10          | EXP2_DIFF_p6       | 100                         | 99  | EXP2_DIFF_p7  | AC6          |
| AA10         | EXP2_DIFF_n6       | 102                         | 101 | EXP2_DIFF_n7  | AD6          |
| -            | 3.3V               | 104                         | 103 | 3.3V          | -            |
| V11          | EXP2_DIFF_p2       | 112                         | 111 | EXP2_DIFF_p3  | AE4          |
| U11          | EXP2_DIFF_n2       | 114                         | 113 | EXP2_DIFF_n3  | AF4          |
| -            | 3.3V               | 116                         | 115 | 3.3V          | -            |
| AF5          | EXP2_DIFF_p0       | 118                         | 117 | EXP2_DIFF_p1  | AE3          |
| AE6          | EXP2_DIFF_n0       | 120                         | 119 | EXP2_DIFF_n1  | AF3          |

## Configuration

The Spartan-3A DSP Starter Platform provides four mechanisms to program and configure the FPGA; these are JTAG, parallel flash, serial flash, and the SystemACE Module (SAM). The SAM configures the FPGA in Boundary Scan mode. The serial and parallel Flash devices may also be programmed via the JTAG connector. The FPGA is the only device in the JTAG chain on the Spartan-3A DSP Starter Platform. The serial Flash, Parallel Flash, and SystemACE are described earlier in this document. Depending on the setting of configuration jumpers M[2:0], any of these configuration options can be the source.

Programming the Spartan-3A DSP via Boundary Scan requires that a JTAG download cable be attached to one of two interfaces that are wired in parallel on the board as shown in Figure 9. A download cable can be attached to either the 14-pin 2mm spaced header (J2) with a ribbon cable or to the 0.1" header (J4) with flying leads. If the Xilinx Parallel Cable IV is used, the ribbon cable connector mates with the keyed J2 connector. The Xilinx Platform USB cable will also mate directly with J2.

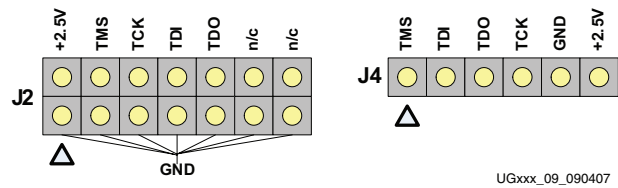


Figure 9: Configuration Connectors

## Configuration Modes

The following table shows the Spartan-3A DSP configuration modes set by Jumper JP9. All mode jumpers (including the PUDC\_B pin) are pulled up; jumper installation grounds the connection. Figure 10 depicts configuration jumper JP9; Table 19 provides the various configuration settings at JP9. Note that Table 18 shows all possible modes for a Spartan-3A DSP FPGE; however, only BPI, SPI and JTAG modes are supported on the Spartan-3A DSP Starter Platform.

A push button labeled **PROG** is connected to the FPGA PROG pin and pulled up. Pushing the button connects PROG to ground. Upon releasing the button, a re-configuration is initiated based upon the setting of JP9. A blue LED (D1) should light when FPGA **DONE** is asserted. A jumper (JP7) connects PROG to ground; this will be used during Direct SPI programming of the SPI flash.

Table 18: FPGA Configuration Mode Jumper (JP9) Settings

| Mode           | PC Pullup | Configuration Mode Jumpers |          |          |              |
|----------------|-----------|----------------------------|----------|----------|--------------|
|                |           | 1-2 (M2)                   | 3-4 (M2) | 5-6 (M2) | 7-8 (PUDC_B) |
| Master Serial  | Yes       | Closed                     | Closed   | Closed   | Closed       |
| Master Serial  | No        | Closed                     | Closed   | Closed   | Open         |
| Slave Serial   | Yes       | Open                       | Open     | Open     | Closed       |
| Slave Serial   | No        | Open                       | Open     | Open     | Open         |
| Master SPI     | Yes       | Closed                     | Closed   | Open     | Closed       |
| Master SPI     | No        | Closed                     | Closed   | Open     | Open         |
| BPI Up         | Yes       | Closed                     | Open     | Closed   | Closed       |
| BPI Up         | No        | Closed                     | Open     | Closed   | Open         |
| Slave Parallel | Yes       | Open                       | Open     | Closed   | Closed       |
| Slave Parallel | No        | Open                       | Open     | Closed   | Open         |
| JTAG           | Yes       | Open                       | Closed   | Open     | Closed       |
| JTAG           | No        | Open                       | Closed   | Open     | Open         |

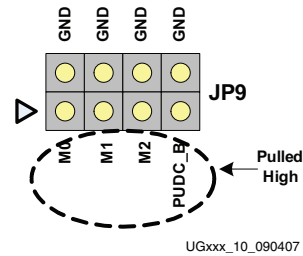


Figure 10: Configuration Jumpers (JP9)

## Board Power

A 5V, 6A, RoHS compliant wall transformer is sufficient to power the board for the majority of applications. Power is supplied via barrel jack J5. A Texas Instruments TPS3828 supervisor monitors the incoming +5V power and holds all power conversion off until incoming power is stable. Figure 11 shows the action of the TPS3828 where the PTH\_INH# signal goes high after stable +5V is applied (CH1). Channels 2, 3 and 4 (3.3V, 2.5V and 1.2V) are allowed to function by the TPS3828 200ms after PTH\_INH# goes high. Slide switch SW1 inhibits conversion until set to "ON". Texas Instruments PTH05050WAZ 6A power modules are utilized to create the +2.5V and +3.3V power rails. The +1.2V power rail (VCC\_INT) is produced by a Texas Instruments PTH04000WAZ 3A power module. These switching converters can exhibit switching spikes in the 650 kHz – 750 kHz region; consequently, PI filters on the output of each of the PTH05050WAZ and PTH04000WAZ are utilized to minimize these transients.

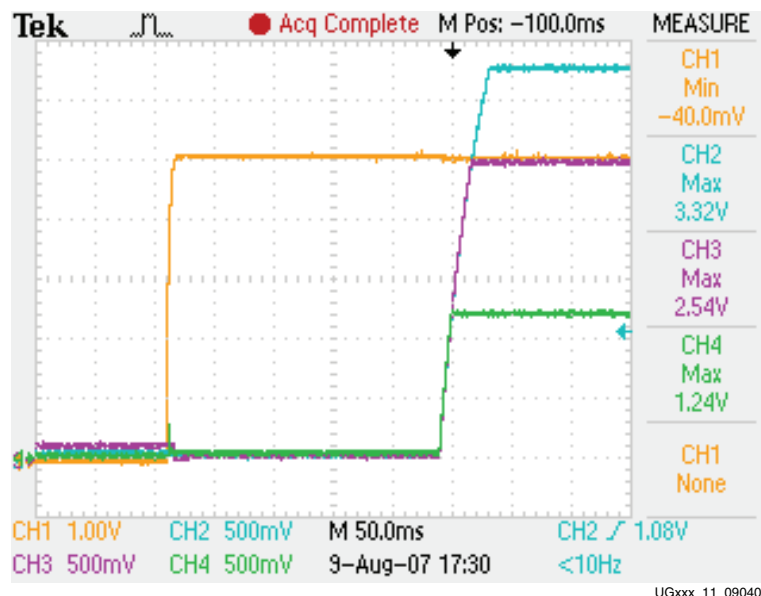


Figure 11: Application of Power

Based on measurements during prototyping, the PTH04000 circuit for 1.2V was tuned to slightly increase the output voltage. The voltage measured at the FPGA was observed to be about 20mV low. Therefore, the set resistor for the PTH04000 was modified based on

the calculations provided in the TI datasheet to raise the voltage by 20mV. Nominally, resistor R42 should be 26.1K, but on this board it is 24.3K.

The DDR2 0.9V reference and termination voltages (FPGA\_DDR2\_VREF, FPGA\_0.9V\_TT) and the 1.8V power rail for the DDR2 memory and the DP83865 Ethernet PHY core voltage are provided by a switching power supply designed around the Texas Instruments TPS51116 Synchronous Buck Controller. The +1.2V, +2.5V and +3.3V power rails are monitored to provide an active-low reset condition (PO\_RESET#) until these rails are above their threshold settings. A pushbutton switch (SW4) may be used to manually create the PO\_RESET# condition. LED D6 is lit when PO\_RESET# is driven active. LEDs D16, D17 and D18 are lit to show the presence of +1.2V, +2.5V and P3.3V, respectively.

Current measurements of the various power rails may be taken by removing the shunts on jumpers JP10 (+3.3V), JP14 (+2.5V), JP6 (+1.8V), and JP5 (+1.2V), and placing an ammeter across the pins. Note that these jumpers are 2x2 requiring two shunts each in order to provide enough current-carrying capacity so the user should ensure that both shunts are in place for normal operation.

The user may experiment with the Spartan-3A DSP low-power SUSPEND mode by jumpering JP11 pins 2:3 (default 1:2). The AWAKE LED (D15) indicates the SUSPEND mode status.

Proper decoupling of the various FPGA power rails is extremely important; this design adheres to Xilinx application note XAPP623 <http://direct.xilinx.com/bvdocs/appnotes/xapp623.pdf>. The Table 19 details the decoupling strategy on the Spartan-3A DSP Starter Platform.

**Table 19: FPGA Decoupling Capacitors**

|                                 | 3.3 V | 2.5 V | Bank 0 | Bank2 | 1.8 V | 1.2 V | 0.9 V |                                      |     |              |       |
|---------------------------------|-------|-------|--------|-------|-------|-------|-------|--------------------------------------|-----|--------------|-------|
| Total Number of Power/Gnd Pairs | 9     | 14    | 9      | 9     | 9     | 23    | 9     |                                      |     |              | Total |
| 470 uF                          | 1     | 1     | 1      | 1     | 1     | 1     | 0     | Tantalum Capacitor<br>4.7 uF         | AVX | TAJD477K004R | 6     |
| 4.7 uF (0603)                   | 2     | 2     | 2      | 2     | 2     | 4     | 0     | Ceramic Capacitor<br>4.7 uF<br>0603  | PIC | ECJ1VB0J475M | 14    |
| 1.0 uF (0402)                   | 3     | 4     | 3      | 3     | 3     | 7     | 5     | Ceramic Capacitor<br>41.0 uF<br>0402 | PIC | EJC-EB0J105M | 28    |
| .01 uF (0201)                   | 5     | 8     | 5      | 5     | 5     | 13    | 5     | Ceramic Capacitor<br>0.01 uF<br>0201 | PIC | ECJZEB0J103K | 46    |
| Actual Number of Capacitors     | 11    | 15    | 11     | 11    | 11    | 25    | 10    |                                      |     |              |       |

## Board Clocks

There are four clock sources provided on the Spartan-3A DSP Starter Platform:

- A 125MHz oscillator connected to GCLK7 (Bank 0).
- A 25.175MHz oscillator (primarily for VGA timing) connected to RHCLK2 (Bank 1).
- A socket for a half-can oscillator connected to GCLK14 (Bank 2). The user must install this oscillator.
- An SMA connector footprint (J1) connected to GCLK4 (Bank 0). The user must install this connector.

The clock sources are listed and described in [Table 20](#).

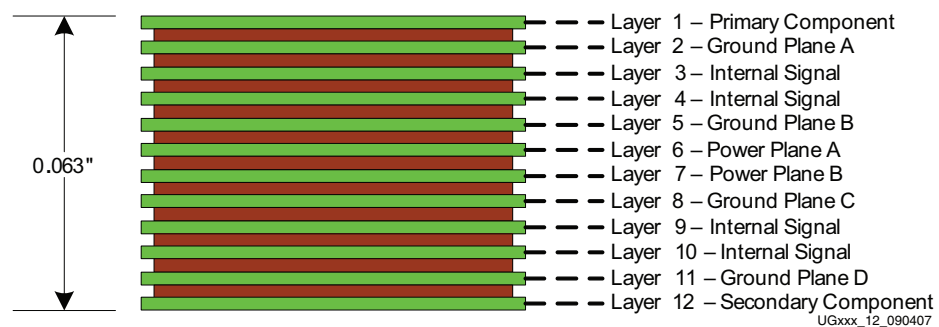
**Table 20: Clock Sources**

| Clock Source              | FPGA Pin No. | Part Number                             |
|---------------------------|--------------|---|
| 125MHz oscillator (U7)    | F13          | Fox FXO-HC535-125.000                   |
| 25.175MHz oscillator (U4) | P26          | Fox FXO-HC530-25.175                    |
| Socket                    | AE13         | Populate with Fox 350LF-type oscillator |
| SMA connector J1          | K14          | Tyco-AMP part #221789-3                 |

The SMA connector is AC-terminated through a 0.1uF 0402 capacitor. Between J1 and the capacitor is a 0-ohm 0402 resistor. Between the capacitor and FPGA pin K14 are two 49.9-ohm 0402 resistors, one pulling high to the Bank 0 I/O voltage (VCCO\_0) and the other pulling low to GND. The user may alter this configuration to suit his requirements.

## PCB Stackup

[Figure 12](#) shows the 12-layer stackup of the Spartan-3A DSP Starter Platform Printed Circuit Board (PCB). The PCB substrate is FR4-class epoxy glass with 1/2oz copper used for all layers.



**Figure 12: PCB Stackup**



## Related Resources

Xilinx would like to acknowledge the following key partners for their key contributions to this project.

### Avnet Electronics Marketing

[www.em.avnet.com/xilinx](http://www.em.avnet.com/xilinx)

[www.em.avnet.com/drc](http://www.em.avnet.com/drc)

[www.em.avnet.com/exp](http://www.em.avnet.com/exp)

[www.em.avnet.com/systemace](http://www.em.avnet.com/systemace)

[www.em.avnet.com/aes](http://www.em.avnet.com/aes)

### Texas Instruments

[www.ti.com](http://www.ti.com)

[www.ti.com/power](http://www.ti.com/power)

[www.ti.com/xilinx](http://www.ti.com/xilinx)

#### Regulators

[focus.ti.com/docs/prod/folders/print/pth04000w.html](http://focus.ti.com/docs/prod/folders/print/pth04000w.html)

[focus.ti.com/docs/prod/folders/print/pth05050w.html](http://focus.ti.com/docs/prod/folders/print/pth05050w.html)

[focus.ti.com/docs/prod/folders/print/tps51116.html](http://focus.ti.com/docs/prod/folders/print/tps51116.html)

#### Supervisors

[focus.ti.com/docs/prod/folders/print/tps3828-50.html](http://focus.ti.com/docs/prod/folders/print/tps3828-50.html)

[focus.ti.com/docs/prod/folders/print/tps3808g01.html](http://focus.ti.com/docs/prod/folders/print/tps3808g01.html)

[focus.ti.com/docs/prod/folders/print/tps3307-25.html](http://focus.ti.com/docs/prod/folders/print/tps3307-25.html)

#### RS232

[focus.ti.com/docs/prod/folders/print/max3221e.html](http://focus.ti.com/docs/prod/folders/print/max3221e.html)

### Intel

[www.intel.com](http://www.intel.com)

[www.intel.com/design/flcomp/prodbref/s33.htm?iid=ipp\\_embed+flash\\_s33&](http://www.intel.com/design/flcomp/prodbref/s33.htm?iid=ipp_embed+flash_s33&)

[www.intel.com/design/flcomp/prodbref/308275.htm?iid=ipp\\_embed+flash\\_j3d&](http://www.intel.com/design/flcomp/prodbref/308275.htm?iid=ipp_embed+flash_j3d&)

### Fox

[www.foxonline.com/](http://www.foxonline.com/)

[www.foxonline.com/xpresso\\_xo.htm](http://www.foxonline.com/xpresso_xo.htm)

[www.foxonline.com/smd\\_xtals.htm](http://www.foxonline.com/smd_xtals.htm)

[www.foxonline.com/thruhole\\_osc.htm](http://www.foxonline.com/thruhole_osc.htm)

## National Semiconductor

[www.national.com](http://www.national.com)

[www.national.com/pf/DP/DP83865.html](http://www.national.com/pf/DP/DP83865.html)

## Samtec

[www.samtec.com/](http://www.samtec.com/)

[www.samtec.com/technical\\_specifications/overview.aspx?series=QTE](http://www.samtec.com/technical_specifications/overview.aspx?series=QTE)

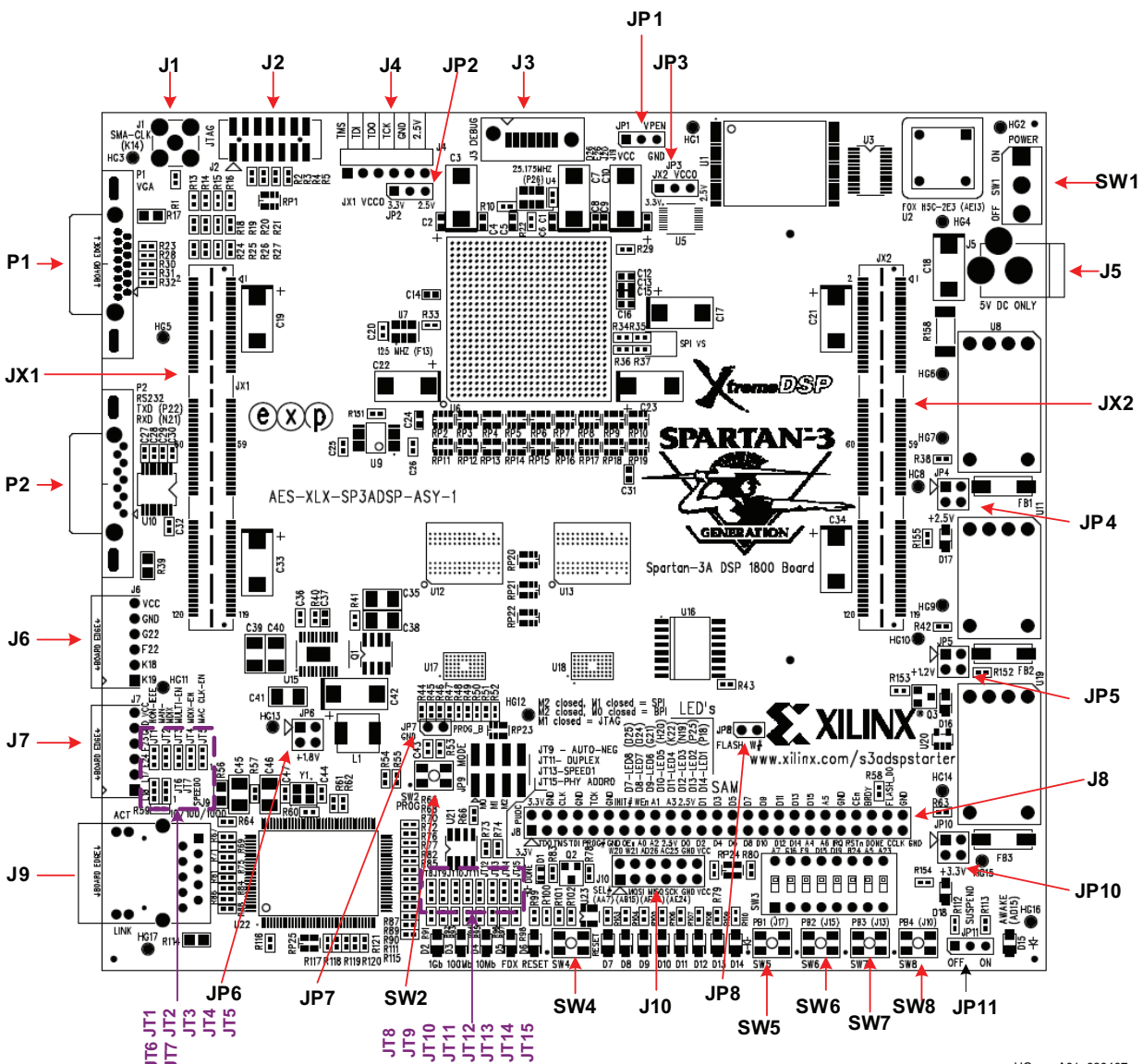
## Tyco/Amp

[www.tycoelectronics.com/](http://www.tycoelectronics.com/)

<http://catalog.tycoelectronics.com/TE/bin/TE.Connect?C=1&M=BYPN&PID=407634&PN=1-6605833-1&I=13>

## Connector, Header, and Jumper Locations

This appendix contains the board outline with the connector, header, and jumper locations:



UGxxx\_A01\_090407

Figure 2-1: Connector, Header, and Jumper Locations

