Spartan-3A DSP Starter Board

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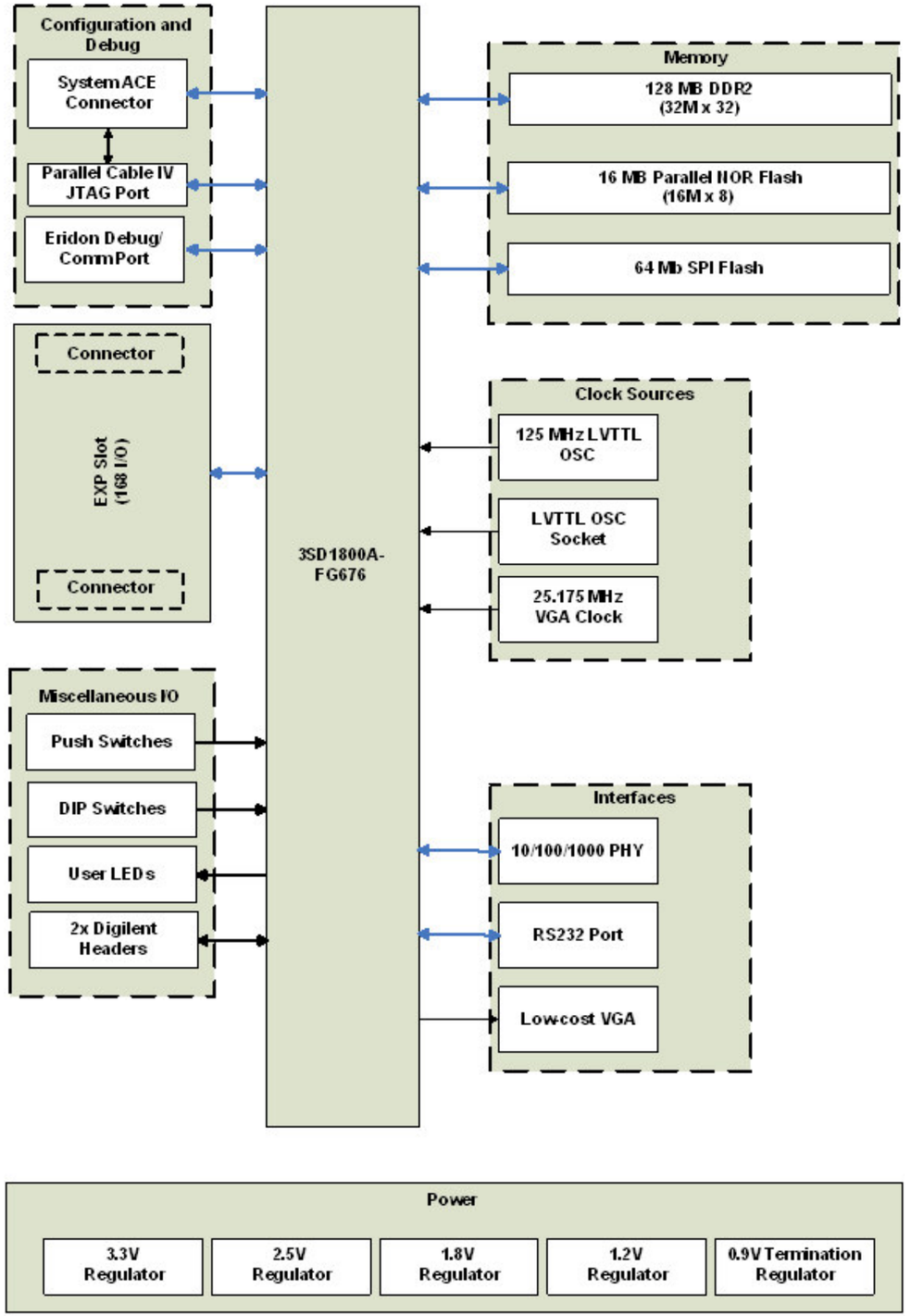
Title: Spartan-3A DSP Starter Board		Sheet 1 - Lead Sheet	
Size: B	Document Number: 0381257		Rev: 1
Date: Friday, September 21, 2007	Sheet 1 of 17		



Title	Spartan-3A DSP Starter Board	Sheet 2 - Block Diagram
Size B	Document Number 0381257	Rev 1
Date: Friday, September 21, 2007	Sheet 2 of 17	

4,5,15 EXP2_SE_IO_[0:33] — EXP2_SE_IO_33

14 EXP1_SE_IO_[0:33]
EXP1_SE_IO_0
EXP1_SE_IO_1
EXP1_SE_IO_2
EXP1_SE_IO_3
EXP1_SE_IO_4
EXP1_SE_IO_5
EXP1_SE_IO_6
EXP1_SE_IO_7
EXP1_SE_IO_8
EXP1_SE_IO_9
EXP1_SE_IO_10
EXP1_SE_IO_11
EXP1_SE_IO_12
EXP1_SE_IO_13
EXP1_SE_IO_14
EXP1_SE_IO_15
EXP1_SE_IO_16
EXP1_SE_IO_17
EXP1_SE_IO_18
EXP1_SE_IO_19
EXP1_SE_IO_20
EXP1_SE_IO_21
EXP1_SE_IO_22
EXP1_SE_IO_23
EXP1_SE_IO_24
EXP1_SE_IO_25
EXP1_SE_IO_26
EXP1_SE_IO_27
EXP1_SE_IO_28
EXP1_SE_IO_29
EXP1_SE_IO_30
EXP1_SE_IO_31
EXP1_SE_IO_32
EXP1_SE_IO_33

14 EXP1_DIFF_p[0:21]
EXP1_DIFF_p0
EXP1_DIFF_p1
EXP1_DIFF_p2
EXP1_DIFF_p3
EXP1_DIFF_p4
EXP1_DIFF_p5
EXP1_DIFF_p6
EXP1_DIFF_p7
EXP1_DIFF_p8
EXP1_DIFF_p9
EXP1_DIFF_p11
EXP1_DIFF_p12
EXP1_DIFF_p13
EXP1_DIFF_p14
EXP1_DIFF_p15
EXP1_DIFF_p16
EXP1_DIFF_p17
EXP1_DIFF_p18
EXP1_DIFF_p19
EXP1_DIFF_p20
EXP1_DIFF_p21

14 EXP1_DIFF_n[0:21]
EXP1_DIFF_n0
EXP1_DIFF_n1
EXP1_DIFF_n2
EXP1_DIFF_n3
EXP1_DIFF_n4
EXP1_DIFF_n5
EXP1_DIFF_n6
EXP1_DIFF_n7
EXP1_DIFF_n8
EXP1_DIFF_n9
EXP1_DIFF_n11
EXP1_DIFF_n12
EXP1_DIFF_n13
EXP1_DIFF_n14
EXP1_DIFF_n15
EXP1_DIFF_n16
EXP1_DIFF_n17
EXP1_DIFF_n18
EXP1_DIFF_n19
EXP1_DIFF_n20
EXP1_DIFF_n21

+3.3V
U7
VDD n/c
E/D OUT
GND n/c
C20 0.1uF
R33 33R0
CLK_125MHz
OSC_HC53x_125mhZ

U6A
BANK 0

IP_0	A13	
IP_0	A17	
IP_0_VREF_0	D7	
IP_0	D12	
IP_0_VREF_0	D14	
IP_0	E11	
IP_0	E18	
IP_0_VREF_0	G11	
IP_0	G14	
IP_0	H13	
IP_0	H18	
IP_0	J10	
IP_0	J13	
IP_0	J15	
IP_0	J17	
IP_0_VREF_0		
IO_L01p_0	G20	EXP1_SE_IO_1
IO_L01n_0	F20	EXP1_SE_IO_17
IO_L02p_0_VREF_0	G19	EXP1_SE_IO_3
IO_L02n_0	F19	EXP1_SE_IO_21
IO_L05p_0	D22	EXP1_SE_IO_13
IO_L05n_0	C22	EXP1_SE_IO_0
IO_L06p_0	D23	EXP1_SE_IO_7
IO_L06n_0	C23	EXP1_SE_IO_11
IO_L07p_0	B23	EXP1_SE_IO_9
IO_L07n_0	A22	EXP1_SE_IO_2
IO_L08p_0	H17	EXP1_SE_IO_19
IO_L08n_0	G17	EXP1_SE_IO_23
IO_L09p_0	C21	EXP1_SE_IO_4
IO_L09n_0	B21	EXP1_SE_IO_6
IO_L10p_0	F21	EXP1_SE_IO_5
IO_L10n_0	D21	EXP1_SE_IO_15
IO_L11p_0	D20	EXP1_SE_IO_14
IO_L11n_0	C20	EXP1_SE_IO_8
IO_L12p_0	J16	EXP1_SE_IO_33
IO_L12n_0	K16	EXP1_SE_IO_25
IO_L13p_0	F17	EXP1_SE_IO_27
IO_L13n_0	E17	EXP1_SE_IO_29
IO_L14p_0_VREF_0	B20	EXP1_SE_IO_10
IO_L14n_0	A20	EXP1_SE_IO_12
IO_L15p_0	B19	EXP1_SE_IO_16
IO_L15n_0	A19	EXP1_SE_IO_18
IO_L16p_0	G15	EXP1_DIFF_p15
IO_L16n_0	H15	EXP1_DIFF_n15
IO_L17p_0	D18	EXP1_SE_IO_28
IO_L17n_0	C18	EXP1_SE_IO_20
IO_L18p_0	B18	EXP1_SE_IO_22
IO_L18n_0	A18	EXP1_SE_IO_24
IO_L19p_0	C17	EXP1_SE_IO_26
IO_L19n_0	B17	EXP1_SE_IO_31
IO_L20p_0	E15	EXP1_DIFF_p19
IO_L20n_0_VREF_0	E15	EXP1_DIFF_n19
IO_L21p_0	D17	EXP1_SE_IO_30
IO_L21n_O	C16	EXP1_SE_IO_32
IO_L22p_0	D16	EXP1_DIFF_p20
IO_L22n_0	C15	EXP1_DIFF_n20
IO_L23p_0	B15	EXP1_DIFF_p21
IO_L23n_0	A15	EXP1_DIFF_n21
IO_L24p_0	F14	EXP1_DIFF_p17
IO_L24n_0	F14	EXP1_DIFF_n17
IO_L25p_0_GCLK4	K14	
IO_L25n_0_GCLK5	B14	EXP1_SE_CLK_IN 14
IO_L26p_0_GCLK6	A14	EXP1_DIFF_CLK_IN_p 14
IO_L26n_0_GCLK7	F13	CLK_125MHz — EXP1_DIFF_CLK_IN_n 14
IO_L27p_0_GCLK8	G13	
IO_L27n_0_GCLK9	R13	
IO_L28p_0_GCLK10	C13	EXP1_DIFF_p10 14
IO_L28n_0_GCLK11	A12	EXP1_DIFF_n10 14
IO_L29p_0	B12	EXP1_DIFF_p16
IO_L29n_0	D13	EXP1_DIFF_n16
IO_L30p_0	C12	EXP1_DIFF_p18
IO_L30n_0	F12	EXP1_DIFF_n18
IO_L31p_0	F12	EXP1_DIFF_p11
IO_L31n_0	C11	EXP1_DIFF_n11
IO_L32p_0	D11	EXP1_DIFF_p14
IO_L32n_0_VREF_0	A10	EXP1_DIFF_n14
IO_L33p_0	B10	EXP1_DIFF_p7
IO_L33n_0	C10	EXP1_DIFF_n7
IO_L34p_0	D10	EXP1_DIFF_p12
IO_L34n_0	G12	EXP1_DIFF_n12
IO_L35p_0	H12	EXP1_DIFF_p13
IO_L35n_0	A9	EXP1_DIFF_n13
IO_L36p_0	B9	EXP1_DIFF_p8
IO_L36n_0	E10	EXP1_DIFF_n8
IO_L37p_0	D9	EXP1_DIFF_p5
IO_L37n_0	A8	EXP1_DIFF_n5
IO_L38p_0	B8	EXP1_DIFF_p6
IO_L38n_0	H11	EXP1_DIFF_n6
IO_L39p_0	K12	EXP1_DIFF_p9
IO_L39n_0	C8	EXP1_DIFF_n9
IO_L40p_0	D8	EXP1_DIFF_p3
IO_L40n_0	B6	EXP1_DIFF_n3
IO_L41p_0	C6	EXP1_DIFF_p2
IO_L41n_0	B7	EXP1_DIFF_n2
IO_L42p_0	C7	EXP1_DIFF_p4
IO_L42n_0	J11	EXP1_DIFF_n4
IO_L43p_0	K11	EXP1_DIFF_p1
IO_L43n_0	C5	EXP1_DIFF_n1
IO_L44p_0	D6	EXP1_DIFF_p0
IO_L44n_0		EXP1_DIFF_n0
IO_L45p_0	A4	EXP1_DIFF_CLK_OUT_p 14
IO_L45n_0	B4	EXP1_DIFF_CLK_OUT_n 14
IO_L46p_0	G10	EXP1_SE_CLK_OUT 14
IO_L46n_0	H10	
IO_L47p_0	G9	
IO_L47n_0	H9	
IO_L48p_0	F7	
IO_L48n_0	E7	
IO_L51p_0	A3	
IO_L51n_0	B3	
IO_L52p_0_VREF_0	F8	
IO_L52n_0_PUDC_B	G8	FPGA_PUDC 5
IP_0	A7	
IP_0	G16	
IP_0	E9	
IP_0	D15	
IP_0	D19	
IP_0	B24	
IP_0	A5	
IP_0	A23	
IP_0	F9	
IP_0	F20	
IP_0	A24	
IP_0	G18	
IP_0	F10	
IP_0	F18	
IP_0	E6	
IP_0	D5	
IP_0	C4	
IP_0		

XC3SD1800AFG676_1

Vcco_0
SWITCH_PB4 — SW8 SPST
SWITCH_PB3 — SW7 SPST
SWITCH_PB2 — SW6 SPST
SWITCH_PB1 — SW5 SPST
R150 1K
R149 1K
R148 1K
R147 1K

Vcco_0
R156 49.9
R157 49.9
C240 0.1uF
R1 0R0
J1 SMA Connector
DNP

Vcco_0
SW3 SW DIP-8
RP40 1K
RP39 1K

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Title: Spartan-3A DSP Starter Board		Sheet 3 - FPGA Bank 0	
Size: C	Document Number: 0381257		Rev: 1
Date: Friday, September 21, 2007	Sheet 3	of 17	

U6B

BANK 1

IP_L65p_1_VREF_1	B26		
IP_L52n_1_VREF_1	G25		
IP_L48n_1	H24		
IP_L44p_1_VREF_1	H26		
IP_L24n_1_VREF_1	U26		
IP_L20n_1_VREF_1	V26		
IP_L28p_1_VREF_1	R23		
IP_L28n_1	R24		
IP_L32p_1	N26		
IP_L32n_1	N25		
IP_L36p_1_VREF_1	M24		
IP_L36n_1	N23		
IP_L40p_1	K24		
IP_L40n_1	L23	SAM_IRQ	10
IO_L01p_1_HDC	Y20	FLASH_WE#	10
IO_L01n_1_LDC2	Y21		
IO_L02p_1_LDC1	AE26	FLASH_OE#	10
IO_L02n_1_LDC0	AD25	FLASH_CE#	10
IO_L03p_1_A0	AC23	FLASH_A0	
IO_L03n_1_A1	AC24	FLASH_A1	
IO_L04p_1	W20	SPISEL_1	5
IO_L04n_1	W21	SPISEL_2	5
IO_L05p_1	AD26	SPISEL_3	5
IO_L05n_1	AC25	SPISEL_4	5
IO_L06p_1	AC26	SAM_A0	10
IO_L06n_1	AB26	SAM_A1	10
IO_L07p_1	AB23	SAM_A2	10
IO_L07n_1_VREF_1	AB24	SAM_A3	10
IO_L08p_1	V18	SAM_A4	10
IO_L08n_1	V19	SAM_A5	10
IO_L09p_1	AA22	SAM_A6	10
IO_L09n_1	AA23	SAM_D0	10
IO_L10p_1	V21	SAM_D1	10
IO_L10n_1	U20	SAM_D2	10
IO_L11p_1	AA24	SAM_D3	10
IO_L11n_1	AA25	SAM_D4	10
IO_L12p_1	U19	SAM_D5	10
IO_L12n_1	U18	SAM_D6	10
IO_L13p_1	Y22	SAM_D7	10
IO_L13n_1	Y23	SAM_D8	10
IO_L14p_1	U21	SAM_D9	10
IO_L14n_1	T20	SAM_D10	10
IO_L15p_1	Y24	SAM_D11	10
IO_L15n_1	Y25	SAM_D12	10
IO_L17p_1	T18	SAM_D13	10
IO_L17n_1	T17	SAM_D14	10
IO_L18p_1	W23	SAM_D15	10
IO_L18n_1	V22	SAM_OEn	10
IO_L19p_1	V24	SAM_WEn	10
IO_L19n_1	V25	SAM_CEn	10
IO_L21p_1	V23	SAM_RESETn	10
IO_L21n_1	U22	EXP2_SE24	
IO_L22p_1	R19	EXP2_SE29	
IO_L22n_1	R20	EXP2_SE28	
IP_L23p_1	U23	EXP2_SE17	
IO_L23n_1_VREF_1	U24	EXP2_SE19	
IO_L25p_1_A2	R21	FLASH_A2	
IO_L25n_1_A3	R22	FLASH_A3	
IO_L26p_1_A4	T23	FLASH_A4	
IO_L26n_1_A5	T24	FLASH_A5	
IO_L27p_1_A6	R18	FLASH_A6	
IO_L27n_1_A7	R17	FLASH_A7	
IO_L29p_1_A8	R25	FLASH_A8	
IO_L29n_1_A9	R26	FLASH_A9	
IO_L30p_1_RHCLK0	P21	SAM_BRDY	10
IO_L30n_1_RHCLK1	P20	SUSPEND	7
IO_L31p_1_RHCLK2	P26	CLK_25.175MHz	
IO_L31n_1_TRDY1_RHCLK3	P25	LED2	
IO_L33p_1_RHCLK4	P23		
IO_L33n_1_RHCLK5	N24	FLASH_Reset#	10
IO_L34p_1_RDY1_RHCLK6	P18	LED1	
IO_L34n_1_RHCLK7	N19	LED3	
IO_L35p_1_A10	M26	FLASH_A10	
IO_L35n_1_A11	M25	FLASH_A11	
IO_L37p_1	P22	FPGA_RS232_Tx	
IO_L37n_1	N21	FPGA_RS232_Rx	
IO_L38p_1_A12	L24	FLASH_A12	
IO_L38n_1_A13	M23	FLASH_A13	
IO_L39p_1_A14	N18	FLASH_A14	
IO_L39n_1_A15	N17	FLASH_A15	
IO_L41p_1	K25	DAC_VSYNC	13
IO_L41n_1	K26	DAC_HSYNC	13
IO_L42p_1_A16	N20	FLASH_A16	
IO_L42n_1_A17	M20	FLASH_A17	
IO_L43p_1_A18	J26	FLASH_A18	
IO_L43n_1_A19	J25	FLASH_A19	
IO_L45p_1	M21	EXP2_SE20	
IO_L45n_1	M22	EXP2_SE33	
IO_L46p_1	K23	EXP2_SE32	
IO_L46n_1	K22	LED4	
IO_L47p_1	M19	DAC_G0	
IO_L47n_1	M18	DAC_G1	
IO_L49p_1	J23	DAC_G2	
IO_L49n_1	J22	DAC_G3	
IO_L50p_1	L22	DAC_B0	
IO_L50n_1	K21	DAC_B1	
IO_L51p_1	G23	DAC_B2	
IO_L51n_1	G24	DAC_B3	
IO_L53p_1	L20	DAC_R0	
IO_L53n_1	K20	DAC_R1	
IO_L54p_1	F25	DAC_R2	
IO_L54n_1	F24	DAC_R3	
IO_L55p_1	L18	DIGI1_1	
IO_L55n_1	L17	DIGI1_2	
IO_L56p_1	E24	DIGI1_3	
IO_L56n_1	F23	DIGI1_4	
IO_L57p_1	K19	DIGI2_1	
IO_L57n_1	K18	DIGI2_2	
IO_L58p_1_VREF_1	F22	DIGI2_3	
IO_L58n_1	G22	DIGI2_4	
IO_L59p_1	J19	DBG_Rx_p	
IO_L59n_1	J20	DBG_Rx_n	
IO_L60p_1	E26	DBG_Tx_p	
IO_L60n_1	D26	DBG_Tx_n	
IO_L61p_1	D25	LED8	
IO_L61n_1	D24	LED7	
IO_L62p_1_A20	J21	FLASH_A20	
IO_L62n_1_A21	H21	FLASH_A21	
IO_L63p_1_A22	C26	FLASH_A22	
IO_L63n_1_A23	C25	FLASH_A23	
IO_L64p_1_A24	H20	LED5	
IO_L64n_1_A25	G21	LED6	
IP_L16n_1	Y26		
IP_L44n_1	H25		
IP_L16p_1	W25		
IP_L24p_1	U25		
IP_L65n_1	B25		
IP_L20p_1	W26		
IP_L48p_1	H23		
IP_L52p_1	G26		

XC3SD1800AFG676_1

DAC_G[0:3] 13

DAC_B[0:3] 13

DAC_R[0:3] 13

+3.3V

R11 8.25K

R12 49R9 R10 100 R9 49R9 R7 49R9 R6 49R9

R8 4.99K

J3 SATA Connector

Place resistors as close as possible to the FPGA

LED4 R107 681 D11 LED_GREEN

LED1 R110 681 D14 LED_GREEN

LED5 R106 681 D10 LED_GREEN

LED6 R105 681 D9 LED_GREEN

LED2 R109 681 D13 LED_GREEN

LED3 R108 681 D12 LED_GREEN

LED8 R103 681 D7 LED_GREEN

LED7 R104 681 D8 LED_GREEN

FLASH_A0 … FLASH_A23 → FLASH_A[0:23] 10

C56 0.1uF Vcco_2

U5 SN74CB3T3245DGVR

EXP2_SE29	2	A1	B1	18	EXP2_SE_IO_29 15
EXP2_SE28	3	A2	B2	17	EXP2_SE_IO_28 15
EXP2_SE17	4	A3	B3	16	EXP2_SE_IO_17 15
EXP2_SE19	5	A4	B4	15	EXP2_SE_IO_19 15
EXP2_SE24	6	A5	B5	14	EXP2_SE_IO_24 15
EXP2_SE20	7	A6	B6	13	EXP2_SE_IO_20 15
EXP2_SE33	8	A7	B7	12	EXP2_SE_IO_33 15
EXP2_SE32	9	A8	B8	11	EXP2_SE_IO_32 15
	10	GND	n/c	1	

(19 OE, 20 VCC)

+3.3V

DIGI1_1 … DIGI1_4 → J7

+3.3V

DIGI2_1 … DIGI2_4 → J6

+3.3V C30 0.1uF C28 0.1uF C29 0.1uF

U10 MAX3221

EN	1	F_OFF	16
C1+	2	VCC	15
V+	3	GND	14
C1-	4	DOUT	13
C2+	5	F_ON	12
C2-	6	DIN	11
V-	7	INVALID	10
RIN	8	ROUT	9

+3.3V C32 0.1uF

C27 0.1uF

P2 CONNECTOR DB9

R39 10R0

FPGA_RS232_Tx

FPGA_RS232_Rx

U4 OSC_HC53x_25.175mhZ

CLK_25.175MHz R22 33R0

n/c	5	VDD	6
OUT	4	E/D	1
n/c	2	GND	3

+3.3V C1 0.1uF

Avnet, Inc. *Engineering Services*		
Title: Spartan-3A DSP Starter Board	Sheet 4 - FPGA Bank 1	
Size: C	Document Number: 0381257	Rev: 1
Date: Friday, September 21, 2007	Sheet 4 of 17	

4,15 EXP2_SE_IO_[0:33]

EXP2_SE_IO_0
EXP2_SE_IO_1
EXP2_SE_IO_2
EXP2_SE_IO_3
EXP2_SE_IO_4
EXP2_SE_IO_5
EXP2_SE_IO_6
EXP2_SE_IO_7
EXP2_SE_IO_8
EXP2_SE_IO_9
EXP2_SE_IO_10
EXP2_SE_IO_11
EXP2_SE_IO_12
EXP2_SE_IO_13
EXP2_SE_IO_14
EXP2_SE_IO_15
EXP2_SE_IO_16
EXP2_SE_IO_18
EXP2_SE_IO_20
EXP2_SE_IO_21
EXP2_SE_IO_22
EXP2_SE_IO_23
EXP2_SE_IO_24
EXP2_SE_IO_25
EXP2_SE_IO_26
EXP2_SE_IO_27
EXP2_SE_IO_30
EXP2_SE_IO_31
EXP2_SE_IO_32
EXP2_SE_IO_33

15 EXP2_DIFF_p[0:21]

EXP2_DIFF_p0
EXP2_DIFF_p1
EXP2_DIFF_p2
EXP2_DIFF_p3
EXP2_DIFF_p4
EXP2_DIFF_p5
EXP2_DIFF_p6
EXP2_DIFF_p7
EXP2_DIFF_p8
EXP2_DIFF_p9
EXP2_DIFF_p11
EXP2_DIFF_p12
EXP2_DIFF_p13
EXP2_DIFF_p14
EXP2_DIFF_p15
EXP2_DIFF_p16
EXP2_DIFF_p17
EXP2_DIFF_p18
EXP2_DIFF_p19
EXP2_DIFF_p20
EXP2_DIFF_p21

15 EXP2_DIFF_n[0:21]

EXP2_DIFF_n0
EXP2_DIFF_n1
EXP2_DIFF_n2
EXP2_DIFF_n3
EXP2_DIFF_n4
EXP2_DIFF_n5
EXP2_DIFF_n6
EXP2_DIFF_n7
EXP2_DIFF_n8
EXP2_DIFF_n9
EXP2_DIFF_n11
EXP2_DIFF_n12
EXP2_DIFF_n13
EXP2_DIFF_n14
EXP2_DIFF_n15
EXP2_DIFF_n16
EXP2_DIFF_n17
EXP2_DIFF_n18
EXP2_DIFF_n19
EXP2_DIFF_n20
EXP2_DIFF_n21

U6C

BANK 2

IP_2_VREF_2	AA9	
IP_2_VREF_2	AA20	
IP_2_VREF_2	AB6	
IP_2	AB13	
IP_2_VREF_2	AC10	
IP_2	AC13	
IP_2	AC17	
IP_2	AA8	
IP_2	AD9	
IP_2	AD10	
IP_2_VREF_2	AD12	
IP_2	AD16	
IP_2_VREF_2	AE15	
IP_2_VREF_2	AE17	
IP_2_VREF_2	AF22	
IP_2_VREF_2	Y16	PO_RESET# 16
IO_L01p_2_M1	AC4	FPGA_M2
IO_L01n_2_M0	AD4	FPGA_M1
IO_L02p_2_M2	Y7	FPGA_M0
IO_L02n_2_CSO_B	AA7	SPI_SEL# 10
IO_L05p_2	W9	EXP2_DIFF_p4
IO_L05n_2	Y9	EXP2_DIFF_n4
IO_L06p_2	AE3	EXP2_DIFF_p1
IO_L06n_2	AF3	EXP2_DIFF_n1
IO_L07p_2	AE4	EXP2_DIFF_p3
IO_L07n_2	AF4	EXP2_DIFF_n3
IO_L08p_2	AC6	EXP2_DIFF_p7
IO_L08n_2	AD6	EXP2_DIFF_n7
IO_L09p_2	V10	EXP2_DIFF_p20
IO_L09n_2	W10	EXP2_DIFF_n20
IO_L10p_2	AF5	EXP2_DIFF_p0
IO_L10n_2	AE6	EXP2_DIFF_n0
IO_L11p_2	AD7	EXP2_DIFF_p9
IO_L11n_2	AE7	EXP2_DIFF_n9
IO_L12p_2	Y10	EXP2_DIFF_p6
IO_L12n_2	AA10	EXP2_DIFF_n6
IO_L13p_2	V11	EXP2_DIFF_p2
IO_L13n_1	U11	EXP2_DIFF_n2
IO_L14p_2	AC8	EXP2_DIFF_p5
IO_L14n_2	AB7	EXP2_DIFF_n5
IO_L15p_2	AB9	EXP2_DIFF_p8
IO_L15n_2	AC9	EXP2_DIFF_n8
IO_L16p_2	V12	EXP2_DIFF_p14
IO_L16n_2	W12	EXP2_DIFF_n14
IO_L17p_2_RDWR_B	Y12	EXP2_DIFF_p16
IO_L17n_2_VS2	AA12	EXP2_DIFF_n16
IO_L18p_2	AE8	EXP2_DIFF_p11
IO_L18n_2	AF8	EXP2_DIFF_n11
IO_L19p_2_VS1	AE9	EXP2_DIFF_p13
IO_L19n_2_VS0	AF9	EXP2_DIFF_n13
IO_L20p_2	V13	EXP2_DIFF_p18
IO_L20n_2	W13	EXP2_DIFF_n18
IO_L21p_2	AB12	EXP2_DIFF_p19
IO_L21n_2	AC12	EXP2_DIFF_n19
IO_L22p_2_D7	AE10	FLASH_D7
IO_L22n_2_D6	AF10	FLASH_D6
IO_L23p_2	AD11	EXP2_DIFF_p12
IO_L23n_2	AC11	EXP2_DIFF_n12
IO_L24p_2_D5	AF12	FLASH_D5
IO_L24n_1_D4	AE12	FLASH_D4
IO_L25p_2_GCLK12	AA13	EXP2_DIFF_CLK_IN_p 15
IO_L25n_2_GCLK13	Y13	EXP2_DIFF_CLK_IN_n 15
IO_L26p_2_GCLK14	AF13	EXP2_SE_CLK_IN 15
IO_L26n_2_GCLK15	AE13	CLK_Socket
IO_L27p_2_GCLK0	Y14	EXP2_SE_CLK_OUT 15
IO_L27n_2_GCLK1	AA14	SAM_CLK 10
IO_L28p_2_GCLK2	AE14	EXP2_DIFF_p10 15
IO_L28n_2_GCLK3	AF14	EXP2_DIFF_n10 15
IO_L29p_2	AD14	EXP2_DIFF_p21
IO_L29n_2	AC14	EXP2_DIFF_n21
IO_L30p_2	AC15	EXP2_SE_IO_26
IO_L30n_2_MOSI_CSI_B	AB15	SPI_MOSI SPI_MOSI 10
IO_L31p_2	V14	EXP2_SE_IO_30
IO_L31n_2	W15	EXP2_SE_IO_16
IO_L32p_2_AWAKE	AD15	
IO_L32n_2_DOUT	AE15	
IO_L33p_2	AE17	EXP2_DIFF_p17
IO_L33n_2	AD17	EXP2_DIFF_n17
IO_L34p_2_INIT_B	AA15	FPGA_INIT# 10
IO_L34n_2_D3	Y15	FLASH_D3
IO_L35p_2	V15	EXP2_SE_IO_14
IO_L35n_2	U15	EXP2_SE_IO_31
IO_L36p_2_D2	AF18	FLASH_D2
IO_L36n_2_D1	AE18	FLASH_D1
IO_L37p_2	AF19	EXP2_SE_IO_23
IO_L37n_2	AE19	EXP2_SE_IO_25
IO_L38p_2	AC16	EXP2_SE_IO_22
IO_L38n_2	AB16	EXP2_SE_IO_18
IO_L39p_2	AF20	EXP2_DIFF_p15
IO_L39n_2	AE20	EXP2_DIFF_n15
IO_L40p_2	AD19	EXP2_SE_IO_27
IO_L40n_2	AC19	EXP2_SE_IO_10
IO_L41p_2	AD20	EXP2_SE_IO_21
IO_L41n_2	AC20	EXP2_SE_IO_6
IO_L42p_2	V16	EXP2_SE_IO_0
IO_L42n_2	U16	
IO_L43p_2	AA17	EXP2_SE_IO_8
IO_L43n_2	Y17	EXP2_SE_IO_2
IO_L44p_2	AE21	EXP2_SE_IO_11
IO_L44n_2	AD21	EXP2_SE_IO_13
IO_L45p_2	AD22	EXP2_SE_IO_9
IO_L45n_2	AC21	EXP2_SE_IO_15
IO_L46p_2	W17	
IO_L46n_2	V17	
IO_L47p_2	AB18	EXP2_SE_IO_12
IO_L47n_2	AA18	EXP2_SE_IO_4
IO_L48p_2	AF23	EXP2_SE_IO_7
IO_L48n_2	AE23	EXP2_SE_IO_5
IOIO_L51p_2	AF25	EXP2_SE_IO_3
IO_L51n_2	AE25	EXP2_SE_IO_1
IO_L52p_2_D0_DIN_MISO	AF24	FLASH_D0 FLASH_D0 10
IO_L52n_2_CCLK	AE24	SPI_MISO SPI_MISO 10
IO_2	AC22	SPI_CLK SPI_CLK 10
IP_2	AE7	FPGA_CCLK FPGA_CCLK 10
IP_2	AD5	
IP_2	AD23	
IP_2	AC5	
IP_2	AC7	
IP_2	AC18	
IP_2	AB10	
IP_2_VREF_2	AB20	
IP_2	AA19	
IP_2	AF2	
IP_2	AB17	
IP_2	Y8	
IP_2	Y11	
IP_2	Y18	
IP_2	Y19	
IP_2_VREF	W18	
IP_2		

XC3SD1800AFG676_1

Vcco_2

RP23 1K

FPGA_PUDC 3

JP9

JP9 Default: JP9 3:4, 5:6 (Master SPI)

Configuration Mode	PC Pull-up	M2 JP9 5:6	M1 JP9 3:4	M0 JP9 1:2	PUDC_B JP9 7:8
Master Serial	Yes	Closed	Closed	Closed	Closed
Master Serial	No	Closed	Closed	Closed	Open
Slave Serial	Yes	Open	Open	Open	Closed
Slave Serial	No	Open	Open	Open	Open
Master SPI	Yes	Closed	Closed	Open	Closed
Master SPI	No	Closed	Closed	Open	Open
BPI Up	Yes	Closed	Open	Closed	Closed
BPI Up	No	Closed	Open	Closed	Open
Slave Parallel	Yes	Open	Open	Closed	Closed
Slave Parallel	No	Open	Open	Closed	Open
JTAG	Yes	Open	Closed	Open	Closed
JTAG	No	Open	Closed	Open	Open

Resistors R34 - R37 and R133-R134 are for variant select (VS) to support SPI configuration of the FPGA.

VS[2:0] = b111 results in a SPI read command of Fast Read (0x0B) which is compatible with Intel S33 Flash.

Vcco_2

R35 1K
R37 1K
R133 1K

EXP2_DIFF_n16
EXP2_DIFF_p13
EXP2_DIFF_n13

DNP
R34 1K
R36 1K
R134 1K

FLASH_D0
FLASH_D1
FLASH_D2
FLASH_D3
FLASH_D4
FLASH_D5
FLASH_D6
FLASH_D7

FLASH_D[0:7] 10

+3.3V

RP24 4.7K

J10

4 SPISEL_1
4 SPISEL_2
4 SPISEL_3
4 SPISEL_4

SPI_SEL#
SPI_MOSI
SPI_MISO
SPI_CLK

R79 4.75K
R80 4.75K

CLK_Socket 5
33R0 R132

U2
OUT
VCC 8
OSC
ENABLE 1
GND 4

C55 0.1uF

Fox H5C-2E3 compatible

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Title	Spartan-3A DSP Starter Board	Sheet 5 - FPGA Bank 2
Size C	Document Number 0381257	Rev 1
Date: Friday, September 21, 2007	Sheet 5 of 17	

1.8V

BANK 3

U6D

FPGA_DDR2_VREF

IP_L16n_3	G1	ETH_CRS
IP_L54p_3	Y3	ETH_COL
IP_L58n_3_VREF_3	AA5	
IP_L04n_3_VREF_3	C1	
IP_L08n_3	D1	ETH_Rx_DV
IP_L12n_3_VREF_3	H4	
IP_L20p_3	J3	ETH_Rx_ER
IP_L20n_3_VREF_3	J2	
IP_L24p_3	J1	ETH_INT#
IP_L24n_3	K1	
IP_L46p_3	U3	
IP_L46n_3	V4	
IP_L50p_3	W1	
IP_L50n_3_VREF_3	W2	
IP_L66p_3	AE1	
IP_L66n_3_VREF_3	AE2	
IO_L01p_3	J8	ETH_Tx_D0
IO_L01n_3	J9	ETH_Tx_D1
IO_L02p_3	B2	ETH_Tx_D2
IO_L02n_3	B1	ETH_Tx_D3
IO_L03p_3	G6	ETH_Tx_D4
IO_L03n_3	H7	ETH_Tx_D5
IO_L05p_3	K9	ETH_Tx_D6
IO_L05n_3	K8	ETH_Tx_D7
IO_L06p_3	D3	ETH_Tx_EN
IO_L06n_3	E4	ETH_Tx_ER
IO_L07p_3	E3	ETH_GTX_CLK
IO_L07n_3	F4	ETH_MDC
IO_L09p_3	F5	ETH_MDIO
IO_L09n_3	G4	ETH_RST#
IO_L10p_3	J7	
IO_L10n_3	H6	
IO_L11p_3	E1	
IO_L11n_3	F2	
IO_L13p_3	K7	
IO_L13n_3	J6	
IO_L14p_3	G3	DDR2_ODT
IO_L14n_3	F3	
IO_L15p_3	L10	DDR2_CAS#
IO_L15n_3	L9	DDR2_WE#
IO_L17p_3	H2	DDR2_CS#
IO_L17n_3	H1	DDR2_RAS#
IO_L18p_3	K6	DDR2_BS0
IO_L18n_3	L7	DDR2_CKE
IO_L19p_3	J5	DDR2_A0
IO_L19n_3	J4	DDR2_BS1
IO_L21p_3	M10	DDR2_A2
IO_L21n_3	M9	DDR2_A1
IO_L22p_3	K5	DDR2_A4
IO_L22n_3	K4	DDR2_A3
IO_L23p_3	K3	DDR2_A6
IO_L23n_3	K2	DDR2_A5
IO_L25p_3	L4	DDR2_A8
IO_L25n_3	L3	
IO_L26p_3	M8	DDR2_A10
IO_L26n_3	M7	DDR2_A9
IO_L27p_3	M4	DDR2_A12
IO_L27n_3	M3	DDR2_A11
IO_L28p_3	M5	
IO_L28n_3	M6	CLK_FB_MB
IO_L29p_3	M1	
IO_L29n_3_VREF_3	N5	FPGA_DDR_CLK1_p
IO_L30p_3	N4	FPGA_DDR_CLK1_n
IO_L30n_3	N1	FPGA_DDR_CLK0_p
IO_L31p_3	N2	FPGA_DDR_CLK0_n
IO_L31n_3	N6	ETH_MCLK
IO_L32p_3_LHCLK0	N7	MB_FB_CLK
IO_L32n_3_LHCLK1	P1	ETH_Rx_CLK
IO_L33p_3_LHCLK2	P2	ETH_Tx_CLK
IO_L33n_3_IRDY2_LHCLK3	P4	FPGA_DDR_D30
IO_L34p_3_LHCLK4	P3	FPGA_DDR_D31
IO_L34n_3_LHCLK5	N9	FPGA_DDR_D28
IO_L35p_3_TRDY2_LHCLK6	P10	FPGA_DDR_D29
IO_L35n_3_LHCLK7	R1	
IO_L36p_3_VREF_3	R2	DDR2_LDM_1
IO_L36n_3	R3	DDR2_UDQS_1
IO_L37p_3	R4	DDR2_UDQS#_1
IO_L37n_3	T3	FPGA_DDR_D26
IO_L38p_3	T4	FPGA_DDR_D27
IO_L38n_3	P7	FPGA_DDR_D24
IO_L39p_3	P6	FPGA_DDR_D25
IO_L39n_3	R5	FPGA_DDR_D22
IO_L40p_3	R6	FPGA_DDR_D23
IO_L40n_3	P8	FPGA_DDR_D20
IO_L41p_3	P9	FPGA_DDR_D21
IO_L41n_3	T5	DDR2_UDQS_0
IO_L42p_3	U4	DDR2_UDQS#_0
IO_L42n_3	R10	
IO_L43p_3_VREF_3	R9	
IO_L43n_3	U1	FPGA_DDR_D18
IO_L44p_3	U2	FPGA_DDR_D19
IO_L44n_3	R8	FPGA_DDR_D16
IO_L45p_3	R7	FPGA_DDR_D17
IO_L45n_3	V1	DDR2_UDM_0
IO_L47p_3	V2	DDR2_LDM_0
IO_L47n_3	T10	
IO_L48p_3	T9	RST_DQS_DIV
IO_L48n_3	U5	FPGA_DDR_D14
IO_L49p_3	V5	FPGA_DDR_D15
IO_L49n_3	T7	FPGA_DDR_D12
IO_L51p_3	U6	FPGA_DDR_D13
IO_L51n_3	W3	DDR2_LDQS_1
IO_L52p_3	W4	DDR2_LDQS#_1
IO_L52n_3	Y1	FPGA_DDR_D10
IO_L53p_2	Y2	FPGA_DDR_D11
IO_L53n_3	AA2	FPGA_DDR_D8
IO_L55p_3	AA3	FPGA_DDR_D9
IO_L55n_3	U7	FPGA_DDR_D6
IO_L56p_3	U8	FPGA_DDR_D7
IO_L56n_3	Y5	FPGA_DDR_D4
IO_L57p_3	Y6	FPGA_DDR_D5
IO_L57n_3	V7	DDR2_LDQS_0
IO_L59p_3	V6	DDR2_LDQS#_0
IO_L59n_3	AB1	FPGA_DDR_D2
IO_L60p_3	AC1	FPGA_DDR_D3
IO_L60n_3	U9	FPGA_DDR_D0
IO_L61p_3	V8	FPGA_DDR_D1
IO_L61n_3	W7	
IO_L63p_3	W6	
IO_L63n_3	AC2	
IO_L64p_3	AC3	
IO_L64n_3	AD1	
IO_L65p_3	AD2	
IO_L65n_3		
IP_L04p_3	C2	ETH_Rx_D0
IP_L16p_3	G2	ETH_Rx_D1
IP_L12p_3	G5	ETH_Rx_D2
IP_L08p_3	D2	ETH_Rx_D3
IP_L62p_3	AB3	ETH_Rx_D4
IP_L58p_3	AA4	ETH_Rx_D5
IP_L62n_3	AB4	ETH_Rx_D6
IP_L54n_3	Y4	ETH_Rx_D7

XC3SD1800AFG676_1

R141 22R0 — DDR2_BS0 → FPGA_DDR_BS0 8,9

R140 24R3 — DDR2_A7 → FPGA_DDR_A7

R138 22R0 — CLK_FB_MB → FPGA_DDR_UDM_1 8,9

Place R136 close to pin N7

R136 60R4 — ETH_MCLK → FPGA_0.9V_TT

MB_FB_CLK - This trace should have length equal to DDR_CLK trace length + DQStrace length

RST_DQS_DIV - The trace from T10 to T9 should have length equal to DDR_CLK trace length + DQStrace length

R137 22R0 — RST_DQS_DIV → R135 60R4 → FPGA_0.9V_TT

Place R135 close to pin T9

FPGA_DDR2_VREF

C127 0.01uF, C117 0.01uF, C112 0.01uF, C129 0.01uF, C133 0.01uF, C135 1.0uF, C138 1.0uF, C137 1.0uF, C131 1.0uF

RP3 33R0

DDR2_A0	8	1	FPGA_DDR_A0
DDR2_CAS#	7	2	FPGA_DDR_CAS# 8,9
DDR2_WE#	6	3	FPGA_DDR_WE# 8,9
DDR2_A2	5	4	FPGA_DDR_A2

RP4 33R0

R139 10K

DDR2_CKE	8	1	FPGA_DDR_CKE 8
DDR2_A4	7	2	FPGA_DDR_A4
DDR2_A1	6	3	FPGA_DDR_A1
DDR2_A10	5	4	FPGA_DDR_A10

RP11 33R0

DDR2_ODT	8	1	
DDR2_BS1	7	2	
DDR2_A3	6	3	DDR2_ODT_Control 8
	5	4	FPGA_DDR_BS1 8,9

RP2 33R0

	8	1	
	7	2	
DDR2_RAS#	6	3	FPGA_DDR_RAS# 8,9
DDR2_CS#	5	4	FPGA_DDR_CS# 8,9

RP13 33R0

DDR2_A8	8	1	FPGA_DDR_A8
	7	2	
DDR2_A11	6	3	FPGA_DDR_A11
DDR2_A12	5	4	FPGA_DDR_A12

RP12 33R0

DDR2_A5	8	1	FPGA_DDR_A5
DDR2_A6	7	2	FPGA_DDR_A6
DDR2_A9	6	3	FPGA_DDR_A9
	5	4	

RP6 33R0

FPGA_DDR_CLK1_n	8	1	FPGA_DDR_CLK_1# 8
FPGA_DDR_CLK1_p	7	2	FPGA_DDR_CLK_1 8
FPGA_DDR_CLK0_n	6	3	FPGA_DDR_CLK_0# 8
FPGA_DDR_CLK0_p	5	4	FPGA_DDR_CLK_0 8

RP15 33R0

CLK_FB_MB	8	1	MB_FB_CLK
DDR2_LDM_1	7	2	FPGA_DDR_LDM_1 8,9
DDR2_UDQS_1	6	3	FPGA_DDR_UDQS_1 8,9
DDR2_UDQS#_1	5	4	FPGA_DDR_UDQS#_1 8,9

RP16 24R0

DDR2_UDQS_0	8	1	FPGA_DDR_UDQS_0 8,9
DDR2_UDQS#_0	7	2	FPGA_DDR_UDQS#_0 8,9
DDR2_LDM_0	6	3	FPGA_DDR_LDM_0 8,9
DDR2_UDM_0	5	4	FPGA_DDR_UDM_0 8,9

RP33 24R0

DDR2_LDQS#_1	8	1	FPGA_DDR_LDQS#_1 8,9
DDR2_LDQS_1	7	2	FPGA_DDR_LDQS_1 8,9
DDR2_LDQS#_0	6	3	FPGA_DDR_LDQS#_0 8,9
DDR2_LDQS_0	5	4	FPGA_DDR_LDQS_0 8,9

FPGA_DDR_A[0:12] 8,9

FPGA_DDR_A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12

FPGA_DDR_D[0:31] 8,9

FPGA_DDR_D0 … FPGA_DDR_D31

+1.8V, +2.5V

C26 0.1uF, C25 0.1uF

U9

ADG3304

	1	VCCA	VCCY 14
ETH_MDIO	2	A1	Y1 13 → GMII_MDIO 11
ETH_MDC	3	A2	Y2 12 → GMII_MDC 11
	4	A3	Y3 11
	5	A4	Y4 10
	8	EN	GND 7

R151 1K

U18

SN74AVC20T245ZQL

	C4, H4	VCCA	VCCB C3, H3
ETH_CRS	A6	1A1	1B1 A1 → GMII_CRS 11
ETH_COL	A5	1A2	1B2 A2 → GMII_COL 11
ETH_Rx_DV	B6	1A3	1B3 B1 → GMII_RX_DV 11
ETH_Rx_ER	B5	1A4	1B4 B2 → GMII_RX_ER 11
ETH_INT#	C6	1A5	1B5 C1 → GBEINT# 11
ETH_MCLK	C5	1A6	1B6 G2 → GBE_MCLK 11
ETH_Rx_CLK	D6	1A7	1B7 D1 → GMII_RX_CLK 11
ETH_Tx_CLK	D5	1A8	1B8 D2 → GMII_TX_CLK 11
	E6	1A9	1B9 E1
	E5	1A10	1B10 E2
ETH_Rx_D0	F6	2A1	2B1 F1 → GMII_RXD0 11
ETH_Rx_D1	F5	2A2	2B2 F2 → GMII_RXD1 11
ETH_Rx_D2	G6	2A3	2B3 G1 → GMII_RXD2 11
ETH_Rx_D3	G5	2A4	2B4 G2 → GMII_RXD3 11
ETH_Rx_D4	H6	2A5	2B5 H1 → GMII_RXD4 11
ETH_Rx_D5	H5	2A6	2B6 H2 → GMII_RXD5 11
ETH_Rx_D6	J6	2A7	2B7 J1 → GMII_RXD6 11
ETH_Rx_D7	J5	2A8	2B8 J2 → GMII_RXD7 11
	K6	2A9	2B9 K1
	K5	2A10	2B10 K2
	A3	1DIR	2DIR K3
	A4	1OE	2OE K4
	B3, B4, D3, D4	GND	GND G3, G4, J3, J4

+1.8V: C203 0.1uF, C201 0.1uF, C202 0.1uF, C200 0.1uF

+2.5V: C208 0.1uF, C205 0.1uF, C207 0.1uF, C206 0.1uF

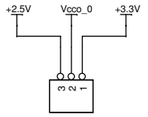
U17

SN74AVC20T245ZQL

	C4, H4	VCCA	VCCB C3, H3
ETH_Tx_D0	A6	1A1	1B1 A1 → GMII_TXD0 11
ETH_Tx_D1	A5	1A2	1B2 A2 → GMII_TXD1 11
ETH_Tx_D2	B6	1A3	1B3 B1 → GMII_TXD2 11
ETH_Tx_D3	B5	1A4	1B4 B2 → GMII_TXD3 11
ETH_Tx_D4	C6	1A5	1B5 C1 → GMII_TXD4 11
ETH_Tx_D5	C5	1A6	1B6 C2 → GMII_TXD5 11
ETH_Tx_D6	D6	1A7	1B7 D1 → GMII_TXD6 11
ETH_Tx_D7	D5	1A8	1B8 D2 → GMII_TXD7 11
ETH_Tx_EN	F6	1A9	1B9 E1 → GMII_TX_EN 11
ETH_Tx_ER	E5	1A10	1B10 E2 → GMII_TX_ER 11
ETH_GTX_CLK	F6	2A1	2B1 F1 → GMII_GTX_CLK 11
	F5	2A2	2B2 F2
ETH_RST#	G6	2A3	2B3 G1 → GBE_RST# 11
	G5	2A4	2B4 G2
	H6	2A5	2B5 H1
	H5	2A6	2B6 H2
	J6	2A7	2B7 J1
	J5	2A8	2B8 J2
	K6	2A9	2B9 K1
	K5	2A10	2B10 K2
	A3	1DIR	2DIR K3
	A4	1OE	2OE K4
	B3, B4, D3, D4	GND	GND G3, G4, J3, J4

Title	Spartan-3A DSP Starter Board	Sheet 6 - FPGA Bank 3
Size C	Document Number 0381257	Rev 1
Date: Friday, September 21, 2007	Sheet 6 of 17	

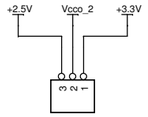
EXP1 VOLTAGE SELECT

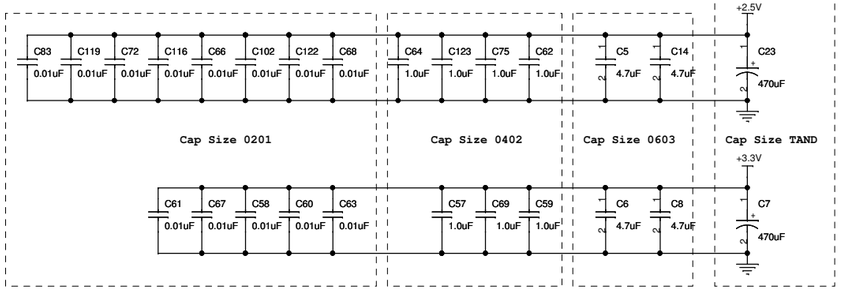


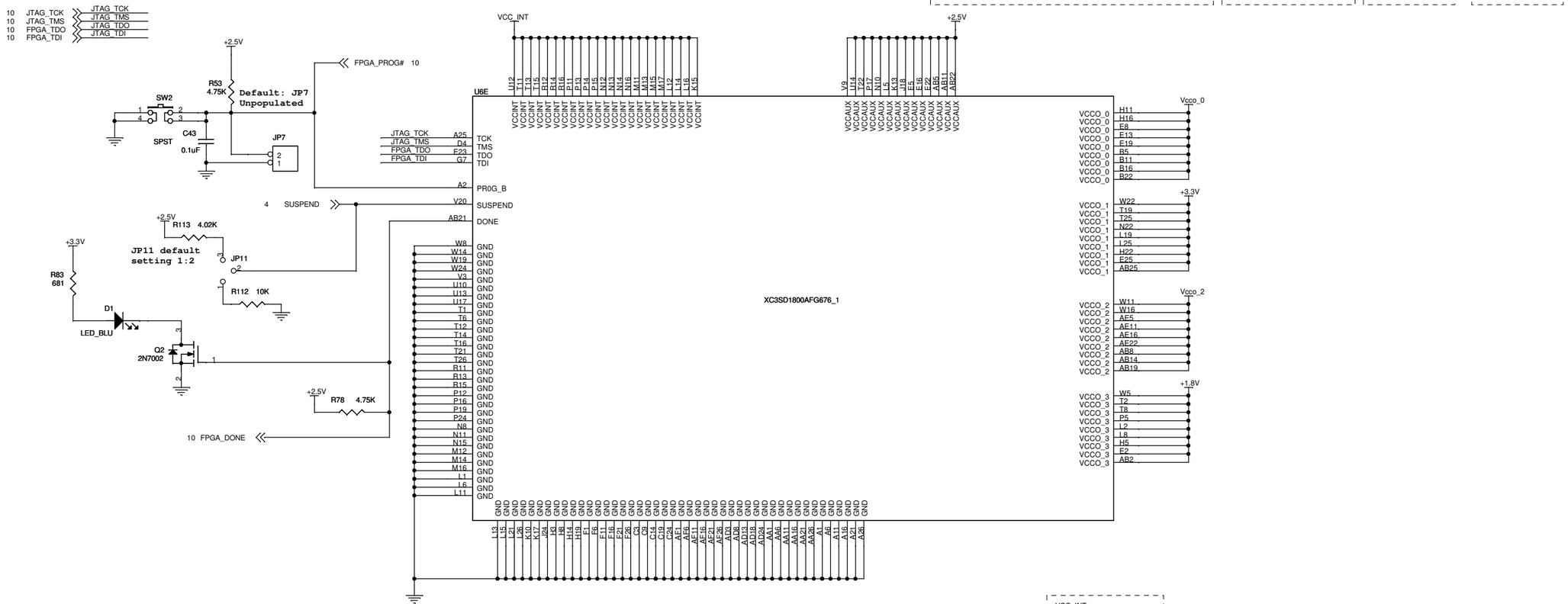
Default: JP2 1:2 (VCCO_0 = +3.3V)

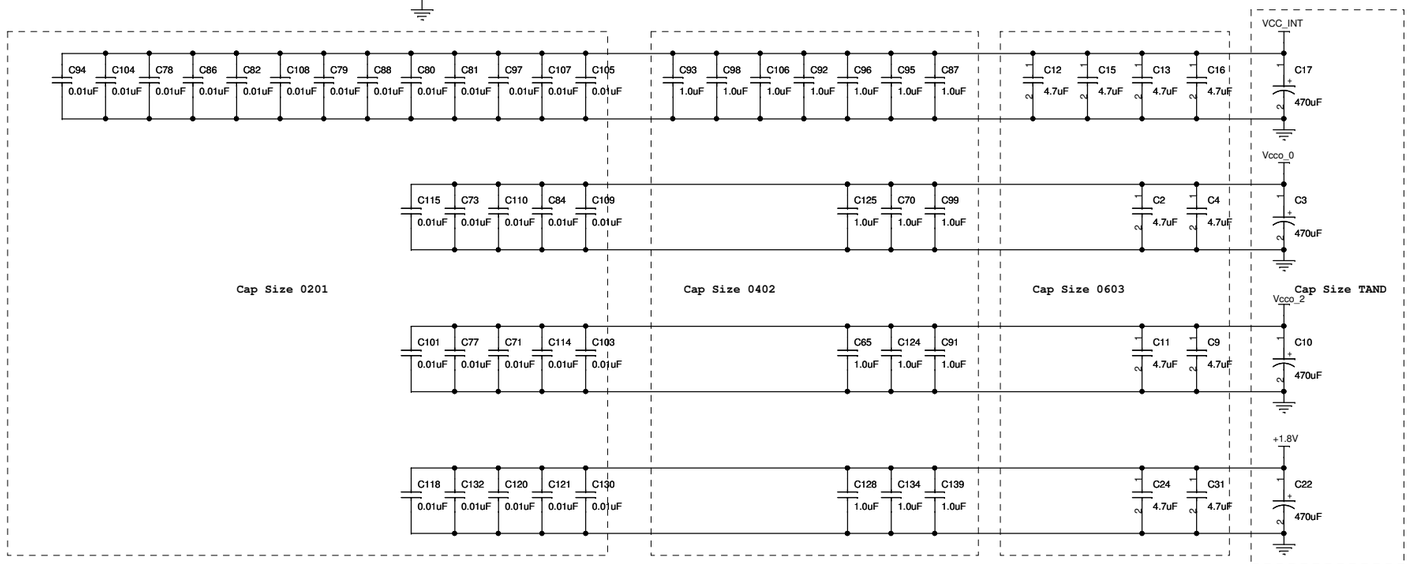
Default: JP3 1:2 (VCCO_2 = +3.3V)

EXP2 VOLTAGE SELECT









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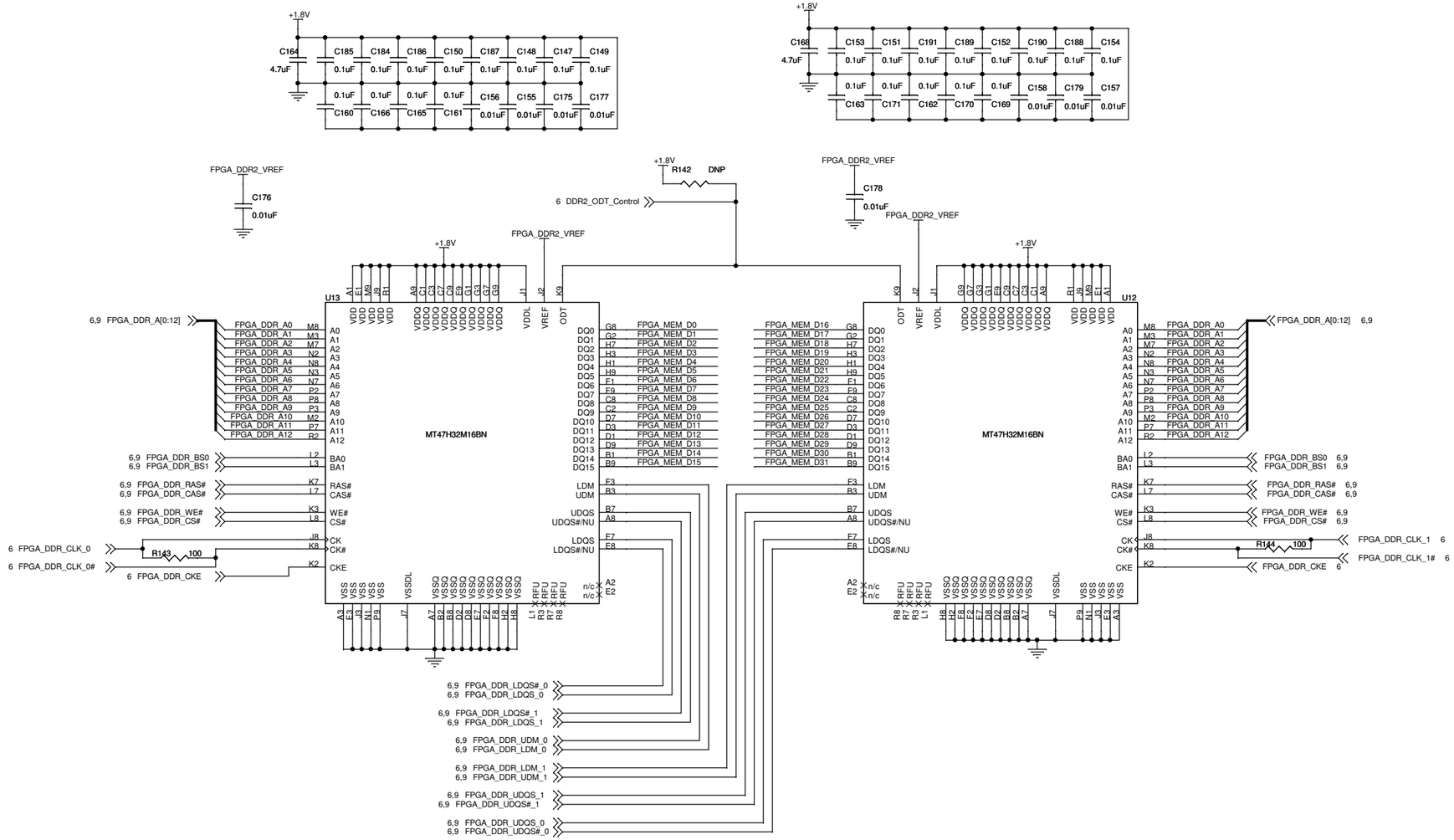
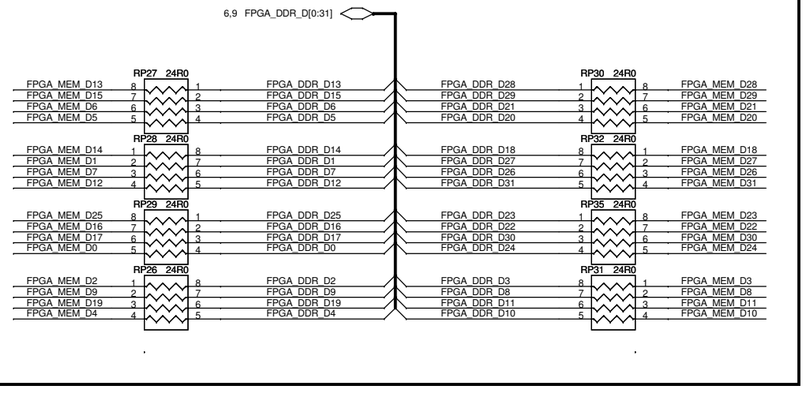
Title: Spartan-3A DSP Starter Board		Sheet 7 - FPGA Power	
Size: C	Document Number: 0381257		Rev: 1
Date: Friday, September 21, 2007	Sheet 7 of 17		



Place series terminations close to FPGA



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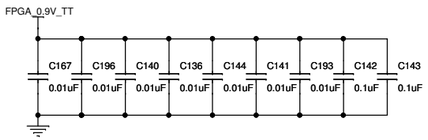
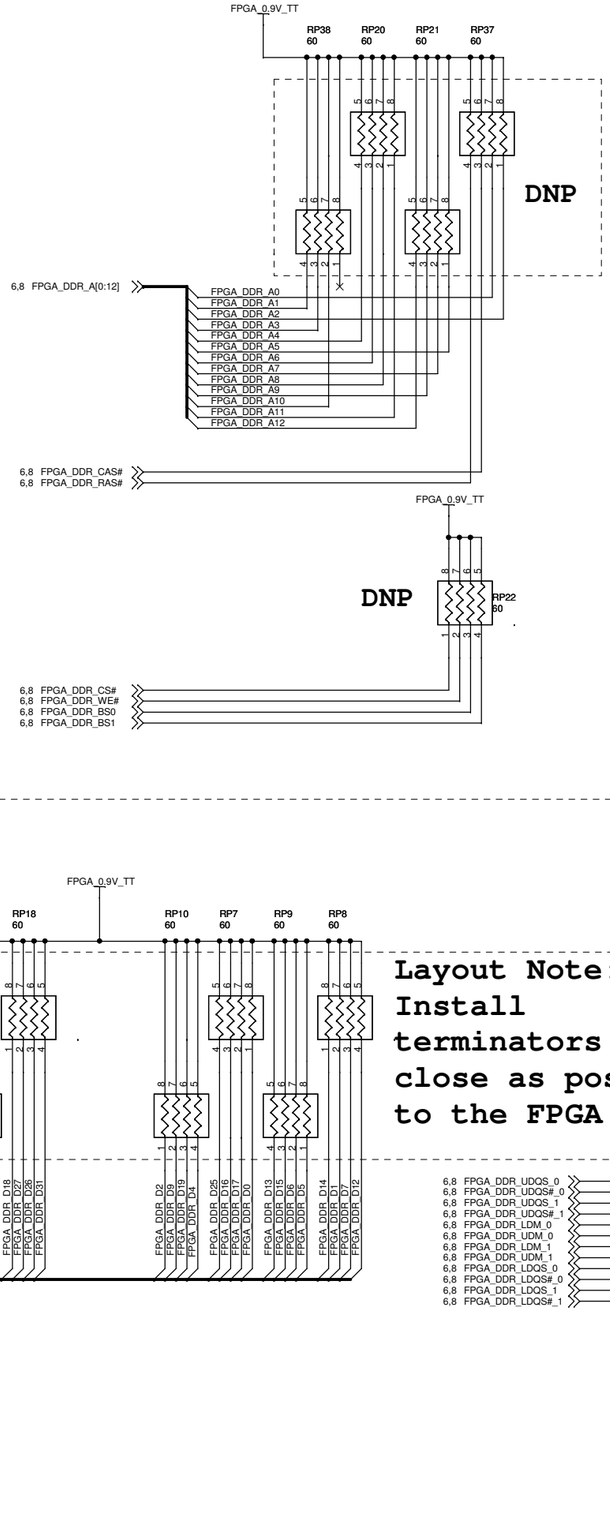
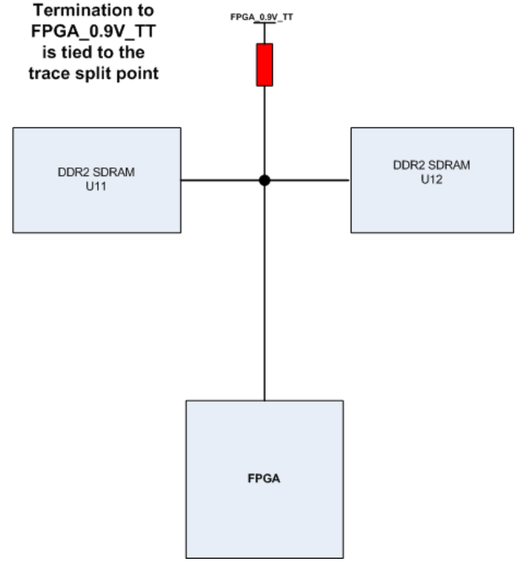
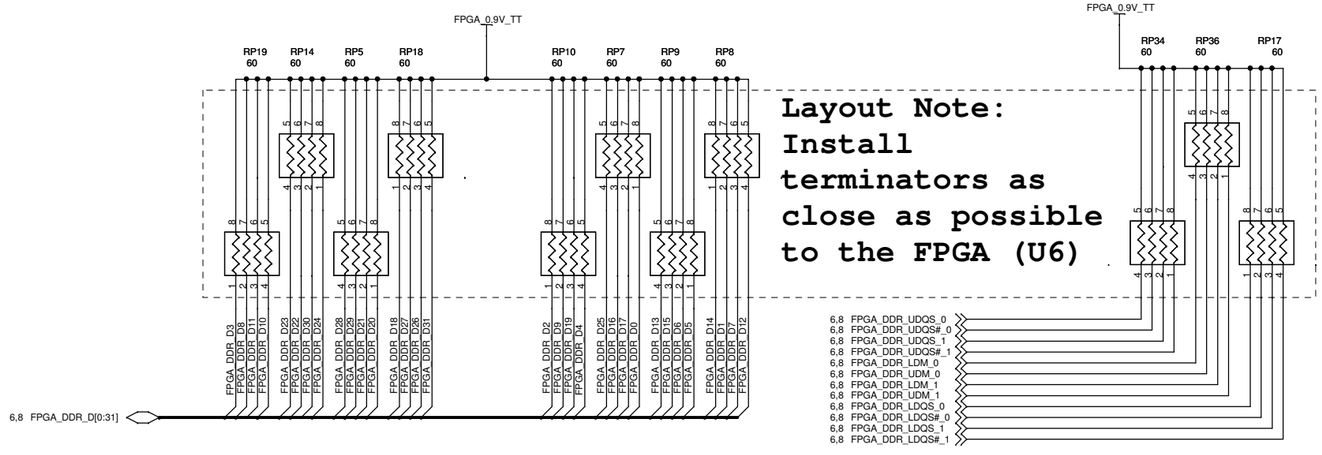
Title: Spartan-3A DSP Starter Board		Sheet 8 - DDR2 Memory	
Size: C	Document Number: 0381257		Rev: 1
Date: Friday, September 21, 2007	Sheet 8 of 17		









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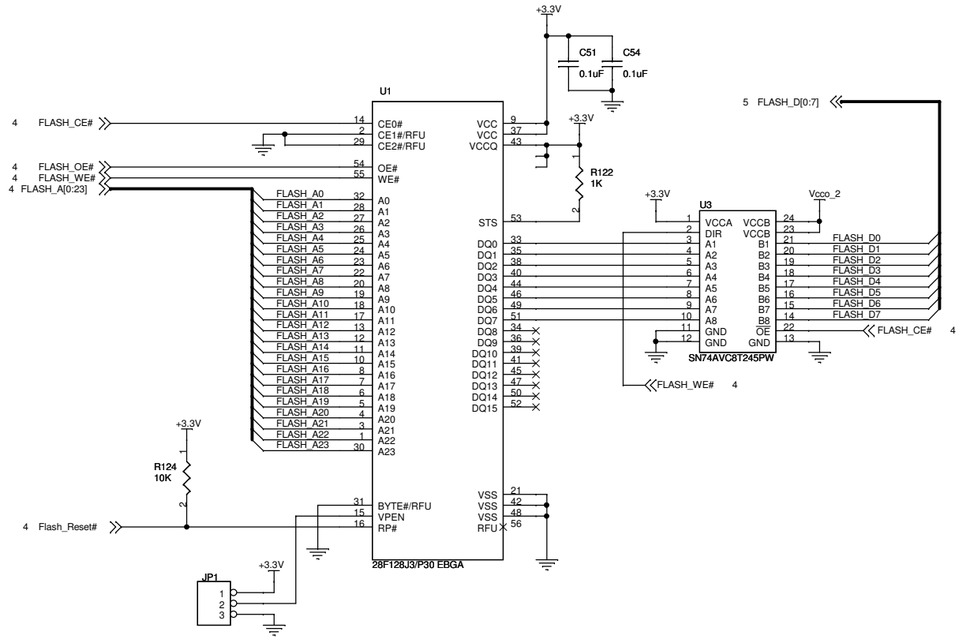
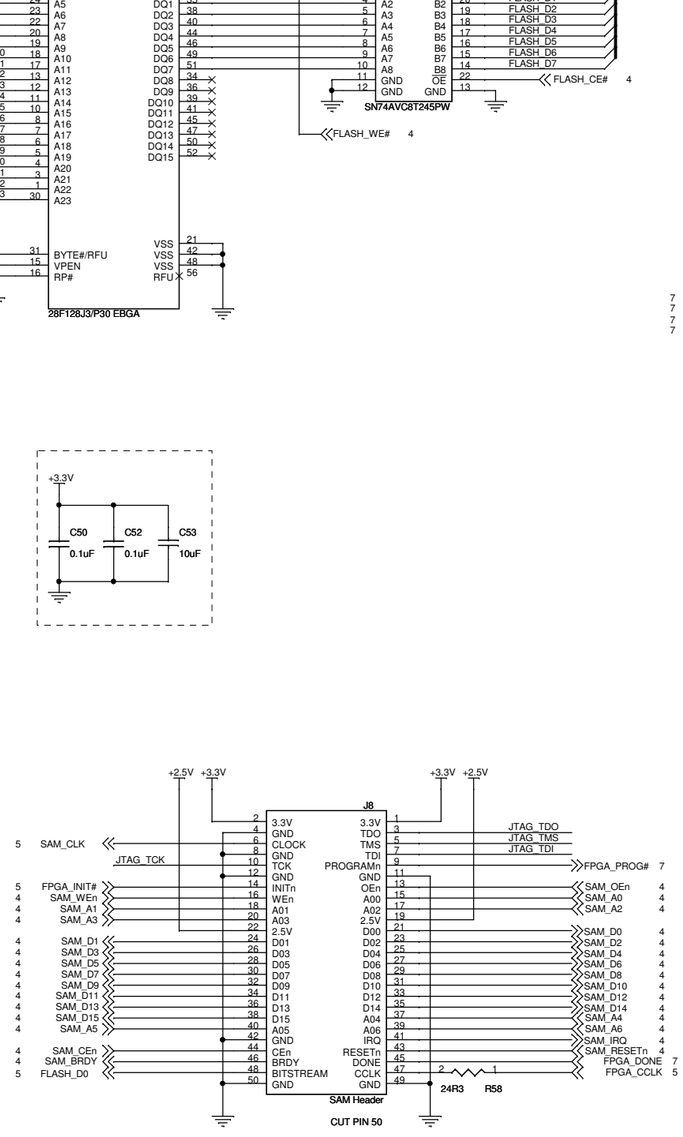
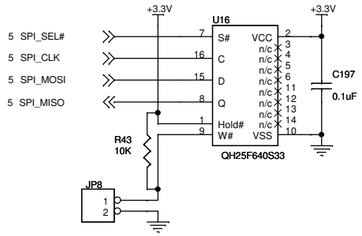
Title: Spartan-3A DSP Starter Board	Sheet 9 - DDR2 Termination	
Size: C	Document Number: 0381257	Rev: 1
Date: Friday, September 21, 2007	Sheet 9 of 17	



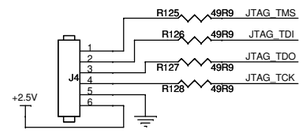
Default: JP1 1:2





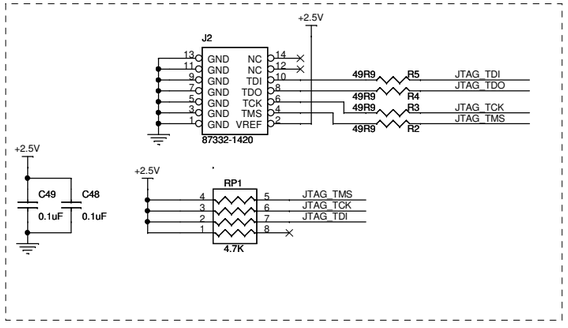
Default: JP8 No Jumper

7 JTAG_TCK
7 JTAG_TMS
7 FPGA_TDO
7 FPGA_TDI



Layout Note: Place J4 and J2 close together

JTAG Parallel IV Connector



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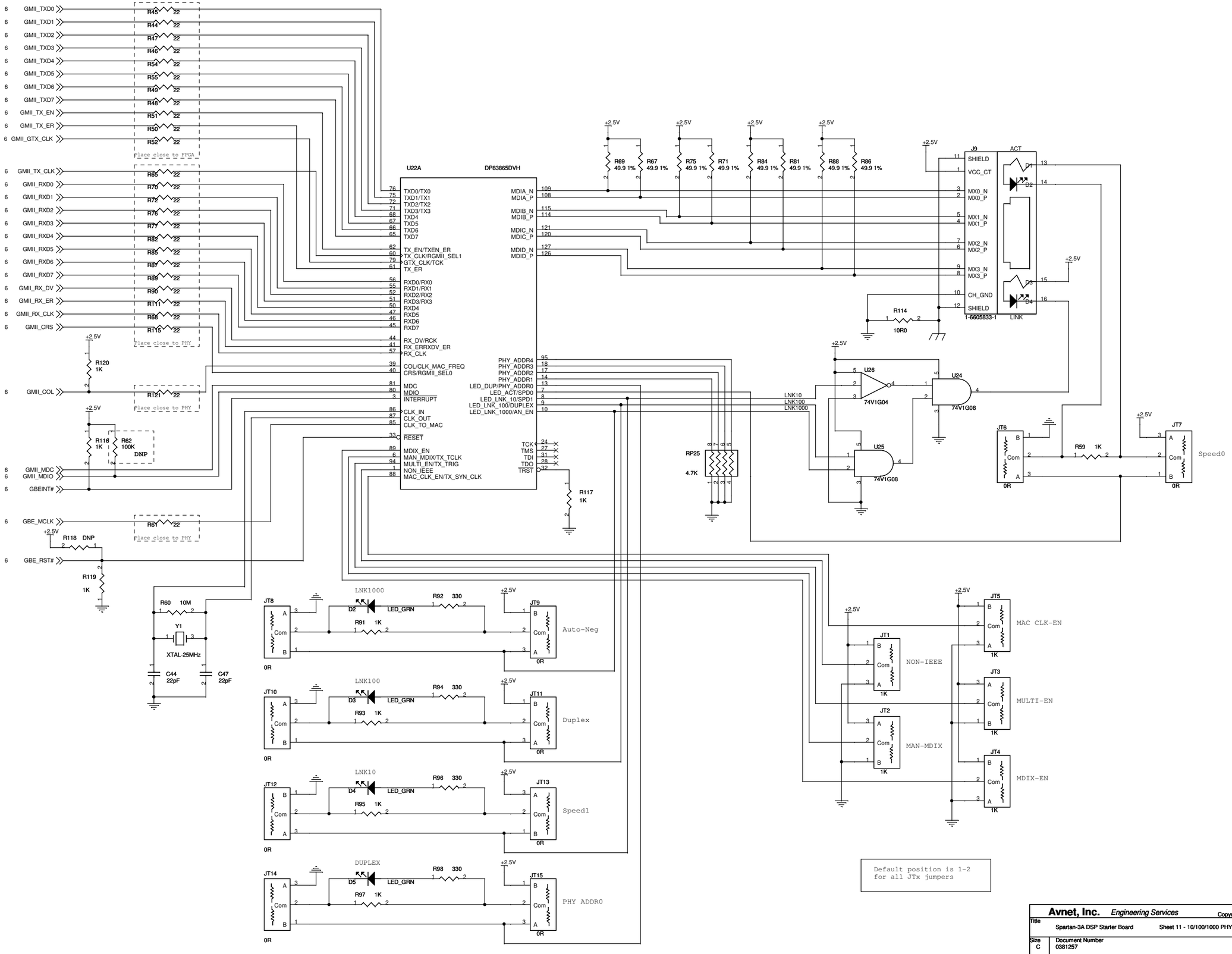
Title: Spartan-3A DSP Starter Board	Sheet 10 - Configuration/Flash Memory	
Size: C	Document Number: 0381257	Rev: 1
Date: Friday, September 21, 2007	Sheet 10 of 17	



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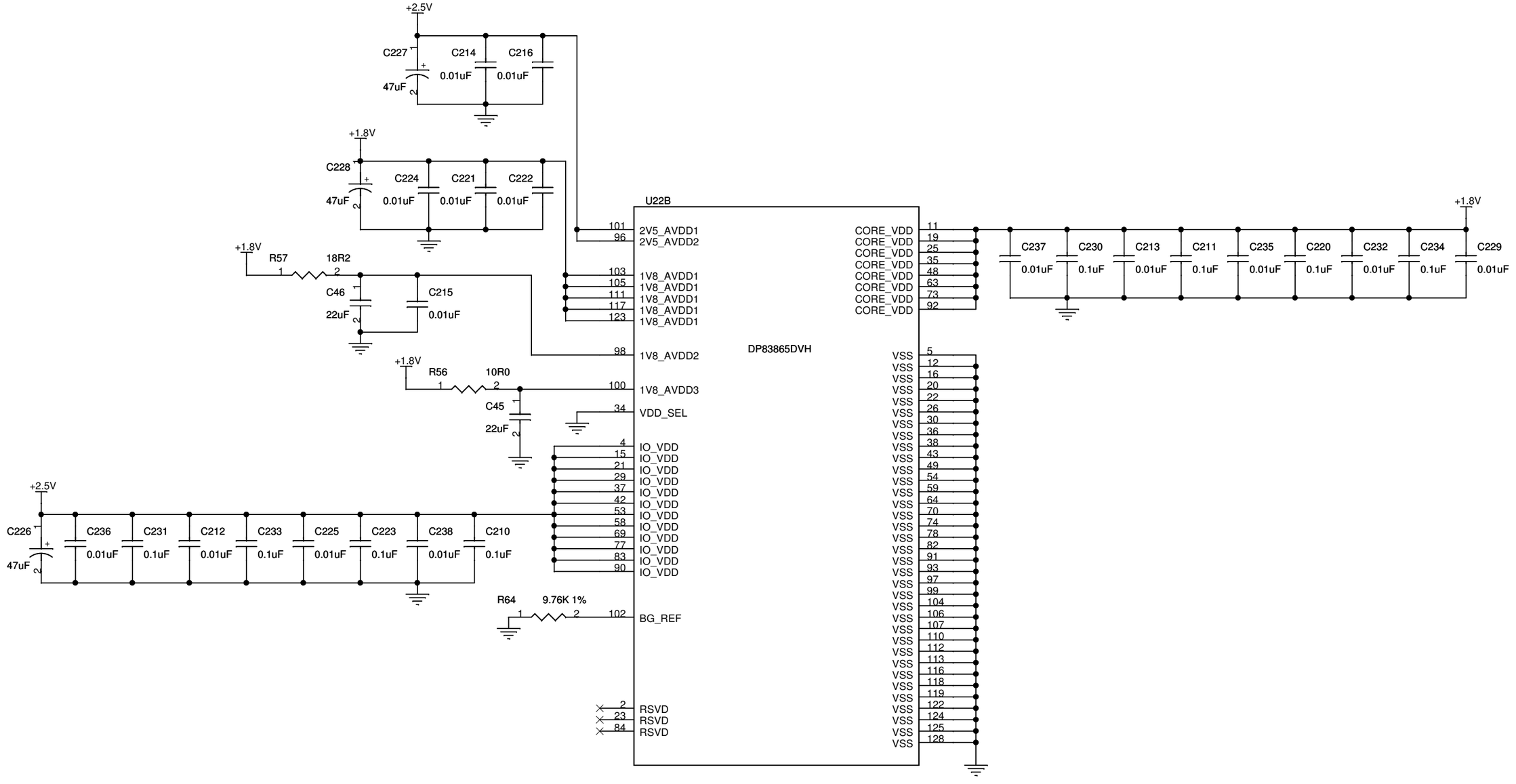
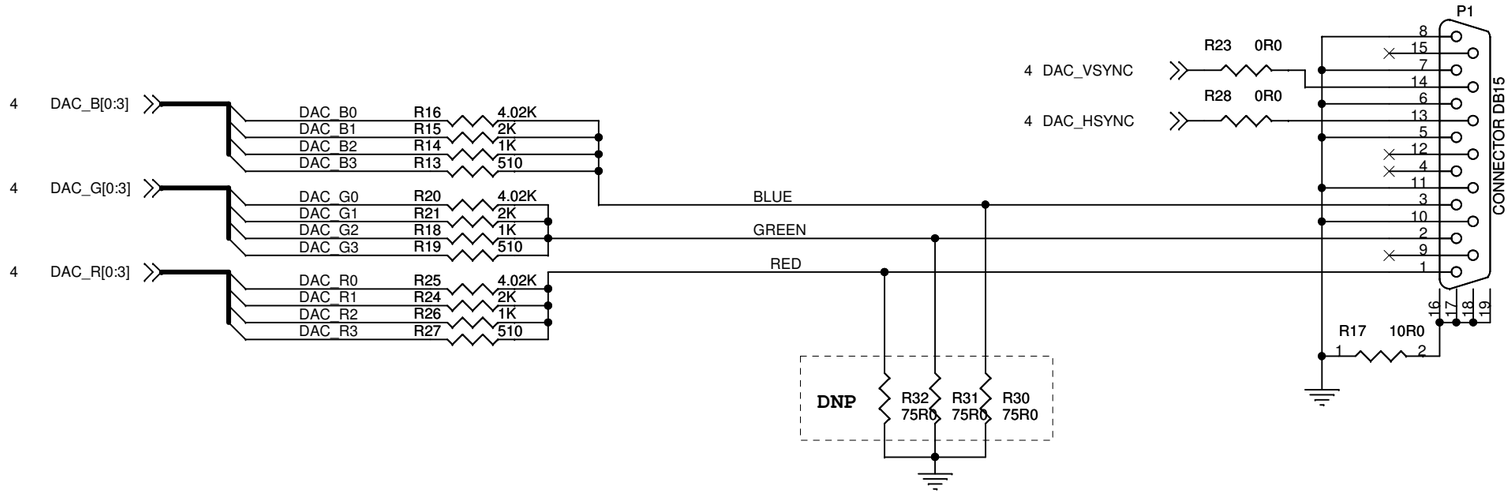
Title: Spartan-3A DSP Starter Board	Sheet 11 - 10/100/1000 PHY	
Size: C	Document Number: 0381257	Rev: 1
Date: Friday, September 21, 2007	Sheet 11 of 17	



Title	Spartan-3A DSP Starter Board	Sheet 12 - PHY Power
Size B	Document Number 0381257	Rev 1
Date: Friday, September 21, 2007	Sheet 12 of 17	



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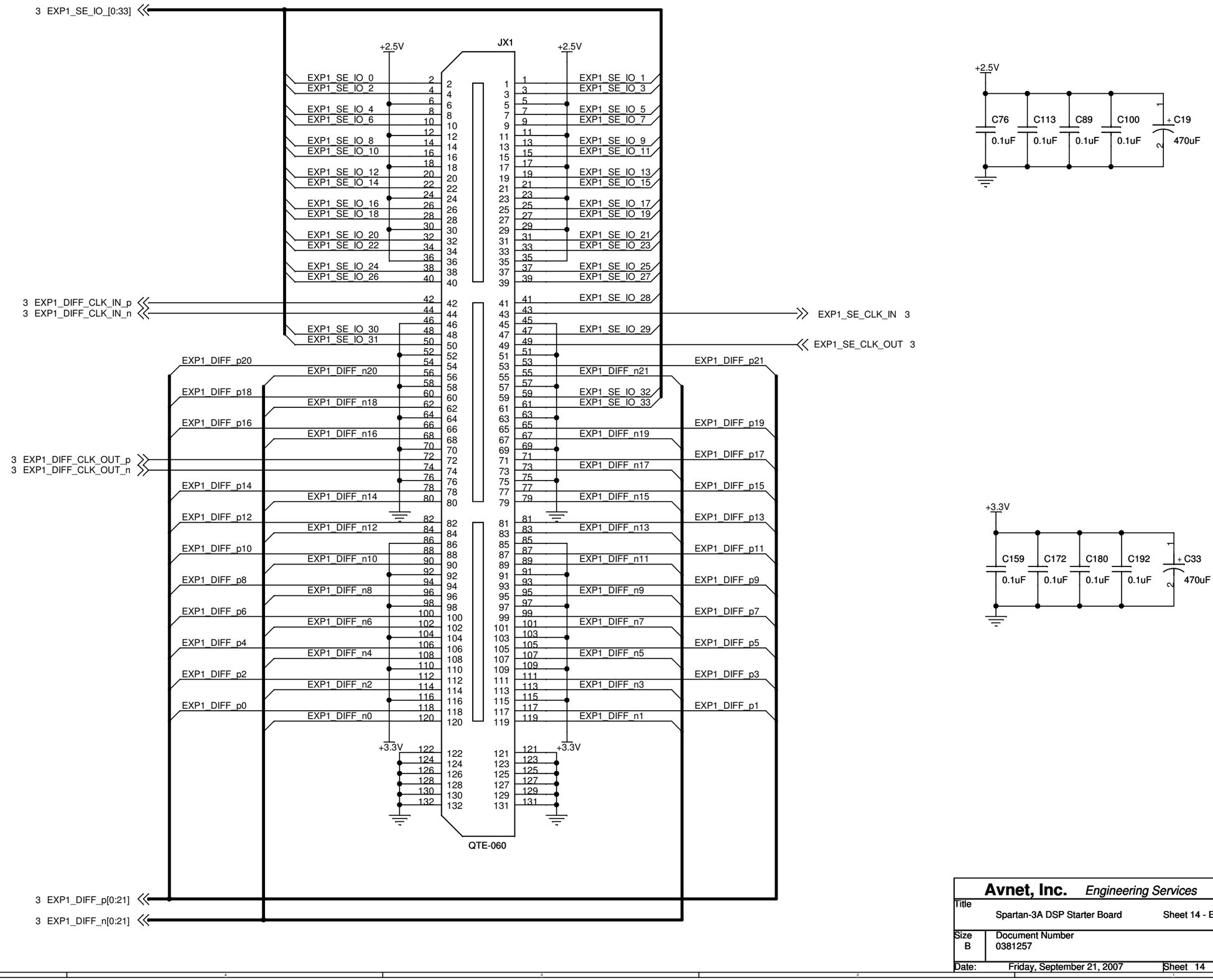
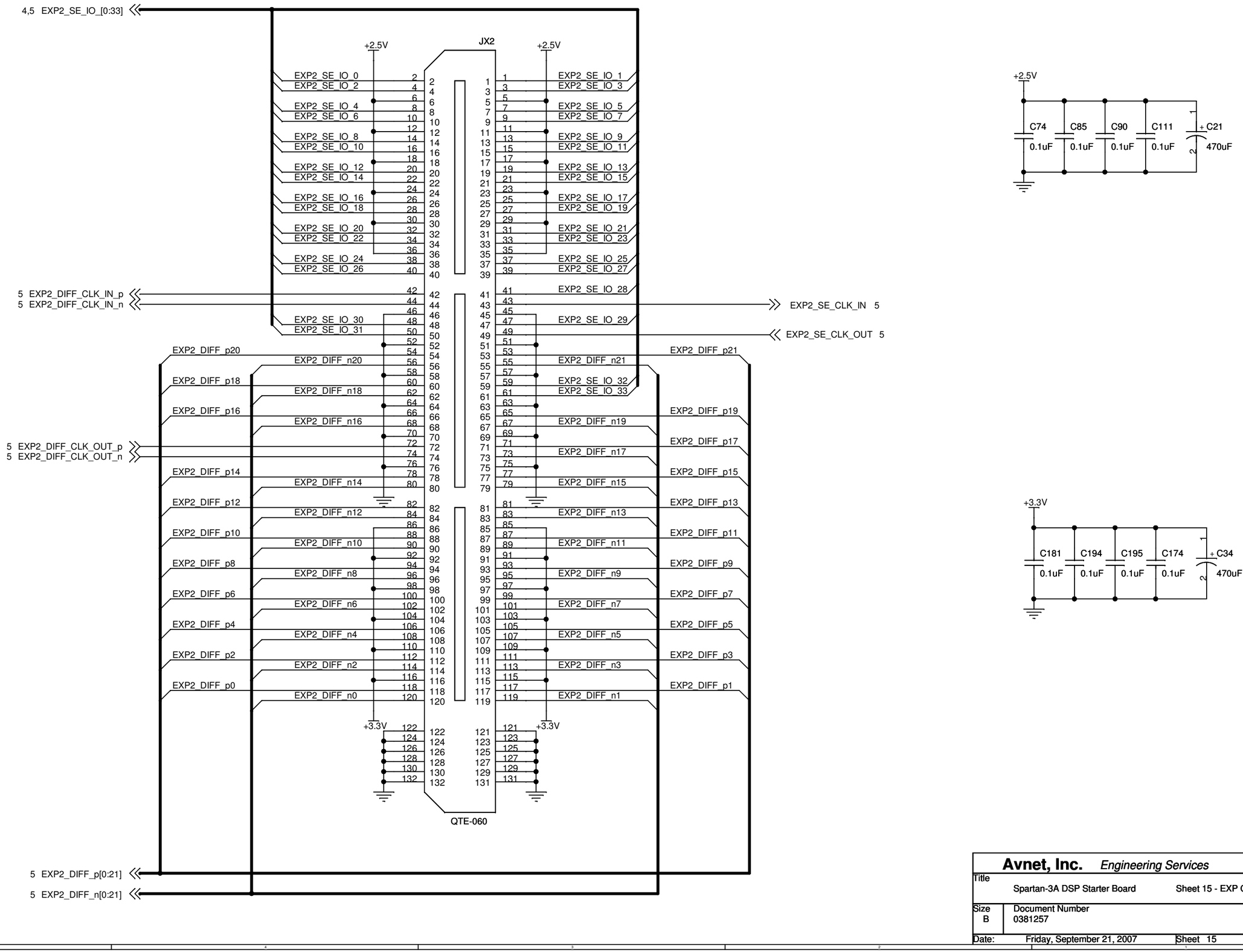
Title: Spartan-3A DSP Starter Board	Sheet 13 - DAC Out	
Size: B	Document Number: 0381257	Rev: 1
Date: Friday, September 21, 2007	Sheet 13 of 17	



Title	Spartan-3A DSP Starter Board	Sheet 14 - EXP Connector (JX1)
Size B	Document Number 0381257	Rev 1
Date: Friday, September 21, 2007	Sheet 14 of 17	



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Title: Spartan-3A DSP Starter Board		Sheet 15 - EXP Connextor (JX2)
Size: B	Document Number: 0381257	Rev: 1
Date: Friday, September 21, 2007	Sheet 15 of 17	

POWER (+5V) INPUT

J5 Barrel Socket

R158 DNP (SMT-2512)

C18 470uF

C209 100uF

HG4 +5V

U19 PTH05050WAZ — Vin, Vout, Track, ADJ, INH, GND; PTH_Track, PTH_INH#

R63 698

FB3 Fair-Rite 2773021447

C217 22uF (muRata GRM32ER61C226KE20)

C218 47uF (AVX TPSD476K016R0100)

HG15 +3.3V

JP10 — JP10 Default jumper 1:3, 2:4

R154 681

D18 +3.3V

U20 TPS3828 — VDD, RESET, WDI, MR, GND; PTH_Track, PTH_INH#

Main Power Switch

DNP: R123 1K, R129 0R0

PWR_ON, PWR_OFF

SW1 SPDT Slide 6A

PTH_INH#

HG2 DGND HG6 DGND HG3 DGND HG1 DGND

HG14 DGND HG16 DGND HG7 DGND HG9 DGND

HG5 DGND HG12 DGND HG17 DGND HG11 DGND

U11 PTH04000WAZ — Vin, Vout, Track, ADJ, INH, GND; PTH_Track, PTH_INH#

C173 100uF

R42 24.3K

FB2 Fair-Rite 2773021447

C198 22uF (muRata GRM32ER61C226KE20)

C199 47uF (AVX TPSD476K016R0100)

HG10 +1.2V

JP5 — JP5 Default jumper 1:3, 2:4

VCC_INT

R152 1K

D16 +1.2V

Q3 MMBT2222LT1

R153 49R9

U8 PTH05050WAZ — Vin, Vout, Track, ADJ, INH, GND; PTH_Track, PTH_INH#

C126 100uF

R38 2.21K

FB1 Fair-Rite 2773021447

C145 22uF (muRata GRM32ER61C226KE20)

C146 100uF (AVX TPSE107K016R0100)

HG8 +2.5V

JP4 — JP4 Default jumper 1:3, 2:4

R155 510

D17 +2.5V

Vsense = (1 + 18.2K/10K)0.405
Vsense = 1.142V

VCC_INT

R100 18.2K

R101 10K

SW4 GLOBAL RESET

C239 0.1uF

U23 TPS3808 — SENSE, VDD, MR, RESET, GND, CT

R102 10K

Power-On Reset

U21 TPS3307-25 — Sns1, Sns2, Sns3, GND, VDD, MR, RST, RST

R73 750K

R74 274K

C219 0.1uF

R98 6R1

R66 10K

D6 RESET

PO_RESET# 5

C41 10uF

U15 TPS51116PWP — VLDOIN, VTT, VTTGND, VTTSNS, GND, MODE, VTTREF, COMP, VDDQSNS, VDDQSET, VBST, DRVH, LL, DRVL, PGND, CS, VSIN, PGOOD, S5, S3

FPGA_0.9V_TT

FPGA_DDR2_VREF

C36 0.1uF

R40 5.11K

C39 10uF

C40 10uF

C204 0.033uF

C37 4.7uF

C38 10uF

C35 10uF

Q1A STS2DNF30L

Q1B STS2DNF30L

L1 2.2uH

C42 150uF

HG13 +1.8V

JP6 — JP6 Default jumper 1:3, 2:4

R41 100K

PGOOD

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Title: Spartan-3A DSP Starter Board	Sheet 16 - Board Power	
Size: C	Document Number: 0381257	Rev: 1
Date: Friday, September 21, 2007	Sheet 16 of 17	

REV A	REV 1

ADDED POWER LEDS TO VCC_INT, +2.5V AND +3.3V RAILS
CONNECTED U20.3 TO PTH_INH# NET
ADDED A 2512 PKG LOAD RESISTOR TO +5V RAIL AT PWR JACK
ADDED PARALLEL TERMINATION TO SMA CLOCK INPUT
REMOVED LEVEL SHIFTER U14 & DIRECTLY CONNECTED SPI NETS TO U16
GROUNDED UNUSED I/O PINS ON TRANSCEIVERS U9, U17 & U18
CHANGED NAME OF PIN "V24" ON FPGA SYMBOL FROM "IP" TO "IO"

09/21/07: Updated Bank 2 of FPGA package by adding pin AA8 (IP_2) and changing pin AC22 from IP_2 (input only) to IO_2 (bidirectional)

Title: Spartan-3A DSP Starter Board — Sheet 17 - Revision History

Size: B | Document Number: 0381257 | Rev: 1

Date: Friday, September 21, 2007 | Sheet 17 of 17