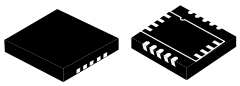
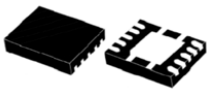
L6984

36 V 400 mA synchronous step-down switching regulator

Datasheet - production data



VFDFPN10 4 x 4 x 1.0 mm



VDFPN10 3 x 3 x 1.0 mm

Features

- 400 mA DC output current
- 4.5 V to 36 V operating input voltage
- Synchronous rectification
- Low consumption mode or low noise mode
- 100 µA I_Q at light load (LCM V_{OUT} = 3.3 V)
- 13 µA $I_{Q\text{-}SHTDWN}$
- Adjustable f_{SW} (250 kHz - 600 kHz)
- Output voltage adjustable from 0.9 V
- No resistor divider required for 3.3 V V_{OUT}
- V_{BIAS} maximizes efficiency at light load
- 350 mA valley current limit
- Constant on-time control scheme
- PGOOD open collector
- Thermal shutdown

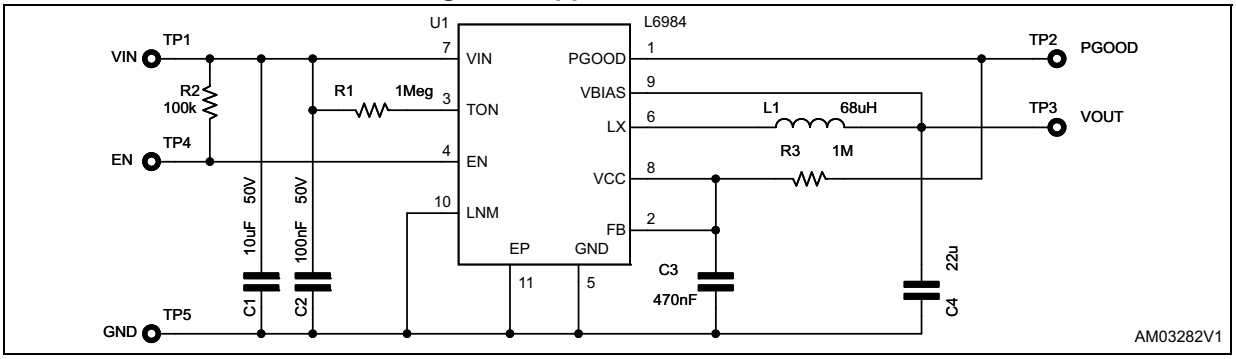
Application

- Automotive systems (LCM)
- Battery powered applications (LCM)
- Car audio and low noise applications (LNM)
- Sensors (LNM)
- E- metering

Description

The L6984 is a step-down monolithic switching regulator able to deliver up to 400 mA DC. The output voltage adjustability ranges from 0.9 V. The fixed 3.3 V V_{OUT} requires no external resistor divider. The “Low Consumption Mode” (LCM) is designed for applications active during car parking, so it maximizes the efficiency at light load with controlled output voltage ripple. The “Low Noise Mode” (LNM) makes the switching frequency almost constant over the load current range, serving low noise application specification like car audio/sensors. The PGOOD open collector output can implement output voltage sequencing during the power-up phase. The synchronous rectification, designed for high efficiency at medium - heavy load, and the high switching frequency capability make the size of the application compact. Pulse-by-pulse current sensing on low-side power element implements an effective constant current protection.

Figure 1. Application schematic

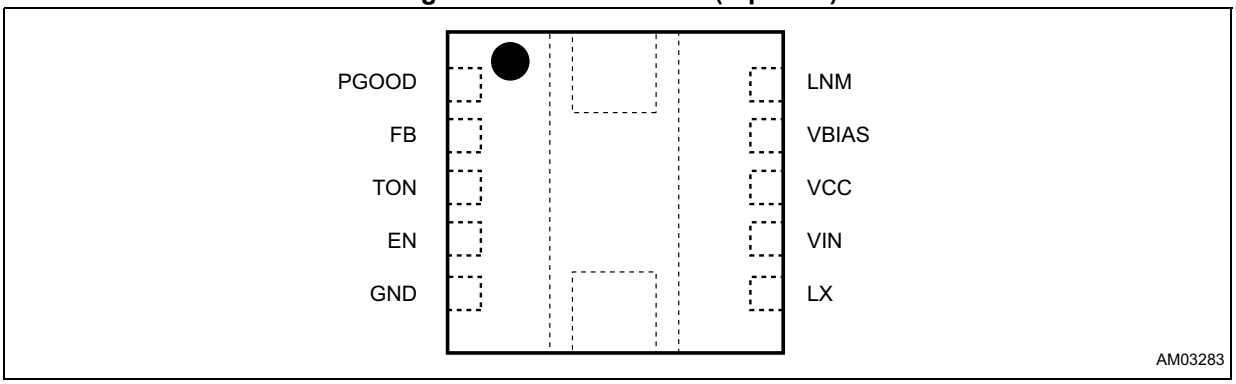


Contents

1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

No.	Pin	Description
1	PGOOD	The open collector output is driven low when the FB voltage is below the $V_{PGD\ L}$ threshold (see *Table 5*).
2	FB	Inverting input of the error amplifier
3	TON	A resistor connected between this pin and V_{IN} sets the switching frequency.
4	EN	Enable pin. A logical active high signal enables the device. Connect this pin to V_{IN} if not used.
5	GND	Power GND
6	LX	Switching node
7	VIN	DC input voltage
8	VCC	Embedded regulator output that supplies the main switching controller. Connect an external 1 µF capacitor for proper operation. An integrated LDO regulates VCC = 3.3 V if VBIAS voltage is < 2.4 V. VCC is connected to VBIAS through a MOSFET switch if VBIAS > 3.2 V and the embedded LDO is disabled to increase the light load efficiency.
9	VBIAS	Typically connected to the regulated output voltage. An external voltage reference can be used to supply the analog circuitry to increase the efficiency at light load. Connect to GND if not used.
10	LNM	Connect to V_{CC} for low noise mode (LNM) / to GND for low consumption mode (LCM) operation.

1.3 Maximum ratings

Stressing the device above the rating listed in *Table 2: Absolute maximum ratings* may cause permanent damage to the device.

These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 5* of this specification is not implied.

Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
V_{IN}	see *Table 1*	-0.3	40	V
EN		-0.3	V_{IN} + 0.3	
LX				
TON				
V_{CC}		-0.3	6	
V_{BIAS}				
PGOOD		-0.3	V_{CC} + 0.3	
FB				
LNM				
T_J	Operating temperature range	-40	150	°C
T_{STG}	Storage temperature range		-55 to 150	
T_{LEAD}	Lead temperature (soldering 10 sec.)		260	
I_{HS}, I_{LS}	High-side RMS switch current		420	mA
	Low-side RMS switch current		500	

1.4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ JA}$	Thermal resistance junction ambient (device soldered on the STMicroelectronics® evaluation board)	50	°C/W

1.5 ESD protection

Table 4. ESD protection

Symbol	Test condition	Value	Unit
ESD	HBM	2	KV
	MM	200	V
	CDM	500	V

2 Electrical characteristics

T_J = 25 °C, V_{IN} = V_{EN} = 12 V, V_{BIAS} = 3.3 V unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range			4.5		36	V
V_{IN_UVLO}	UVLO thresholds	rising edge V_{CC} regulator V_{BIAS} = GND		3.1	3.8	4.5	
		falling edge V_{CC} regulator V_{BIAS} = GND		2.9	3.6	4.3	
V_{OUT}	Fixed output voltage valley regulation	FB = V_{CC}, no load		3.23	3.3	3.37	
V_{FB}	Adjustable output voltage valley regulation	No load, V_{BIAS} = 3.3 V		0.88	0.9	0.92	
$R_{DSON\ HS}$	High-side RDSON	I_{SW} = 0.1 A		0.9	1.3	1.7	Ω
$R_{DSON\ LS}$	Low-side RDSON	I_{SW} = 0.1 A		0.6	1.0	1.4	
Current limit and zero crossing comparator							
I_{VY}	Valley current limit			350	400	470	mA
I_{ZCD}	Zero crossing current threshold		(1)	12	27	46	
VCC regulator							
V_{CC}	VCC voltage	V_{FB} = 1 V, V_{BIAS} = GND		3	3.8	4.6	V
V_{BIAS}	V_{BIAS} falling threshold			2.4	2.6	2.8	
	V_{BIAS} rising threshold			2.6	2.9	3.2	
Power consumption							
I_{SHTDWN}	Shutdown current from V_{IN}	EN = GND		3	13	22	µA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
$I_{Q\ OPVIN}$	Quiescent current from V_{IN}	**LCM - SWO** $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = 3.3 V	(2)	11	26	41	µA
		LCM - NO SWO $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = GND	(2)	90	160	230	
		LNM - SWO $V_{REF} < V_{FB} < V_{OVP}$ V_{BIAS} = 3.3 V		11	26	42	
		LNM - NO SWO $V_{REF} < V_{FB} < V_{OVP}$ V_{BIAS} = GND		200	320	440	
$I_{Q\ OPVBIAS}$	Quiescent current from V_{BIAS}	**LCM - SWO** $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = 3.3 V	(2)	80	150	200	
		LNM - SWO $V_{REF} < V_{FB} < V_{OVP}$ V_{BIAS} = 3.3 V		180	300	390	
Enable							
EN	EN thresholds	Device inhibited		1.1			V
		Device enabled				2.6	
	EN hysteresis		(3)		650		mV
Overvoltage protection							
V_{OVP}	Overvoltage trip (V_{OVP}/V_{REF})	Rising edge		18	23	28	%
PGOOD							
$V_{PGD\ L}$	Power good LOW threshold	V_{FB} rising edge (PGOOD high impedance)	(3)		90		%
		V_{FB} falling edge (PGOOD low impedance)		84	88	92	
$V_{PGD\ H}$	Power good HIGH threshold	Internal FB rising edge (PGOOD low impedance) $V_{FB} = V_{CC}$		118	123	128	
		Internal FB falling edge (PGOOD high impedance) $V_{FB} = V_{CC}$	(3)		100		
V_{PGOOD}	PGOOD open collector output	$V_{IN} > V_{IN\_UVLO\_H}$, V_{FB}=GND 4 mA sinking load				0.6	V
		$2.9 < V_{IN} < V_{IN\_UVLO\_H}$ 100 µA sinking load				0.6	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
Thermal shutdown							
T_{SHDWN}	Thermal shutdown temperature		(3)		150		°C
T_{HYS}	Thermal shutdown hysteresis		(3)		20		°C

1. Parameter tested in static condition during testing phase. Parameter value may change over dynamic application condition.
2. LCM enables SLEEP mode (part of the internal circuitry is disabled) at light load.
3. Not tested in production.

3 Device description

The L6984 device is based on a “Constant On-Time” (COT) control scheme with frequency feed-forward correction over the V_{IN} range. As a consequence the device features fast load transient response, almost constant switching frequency operation over the input voltage range and simple stability control.

The switching frequency can be adjusted in the 250 kHz - 600 kHz range.

The LNM (low noise mode) implements constant PWM control to minimize the voltage ripple over the load range, the LCM (low consumption mode) pulse skipping technique to increase the efficiency at the light load.

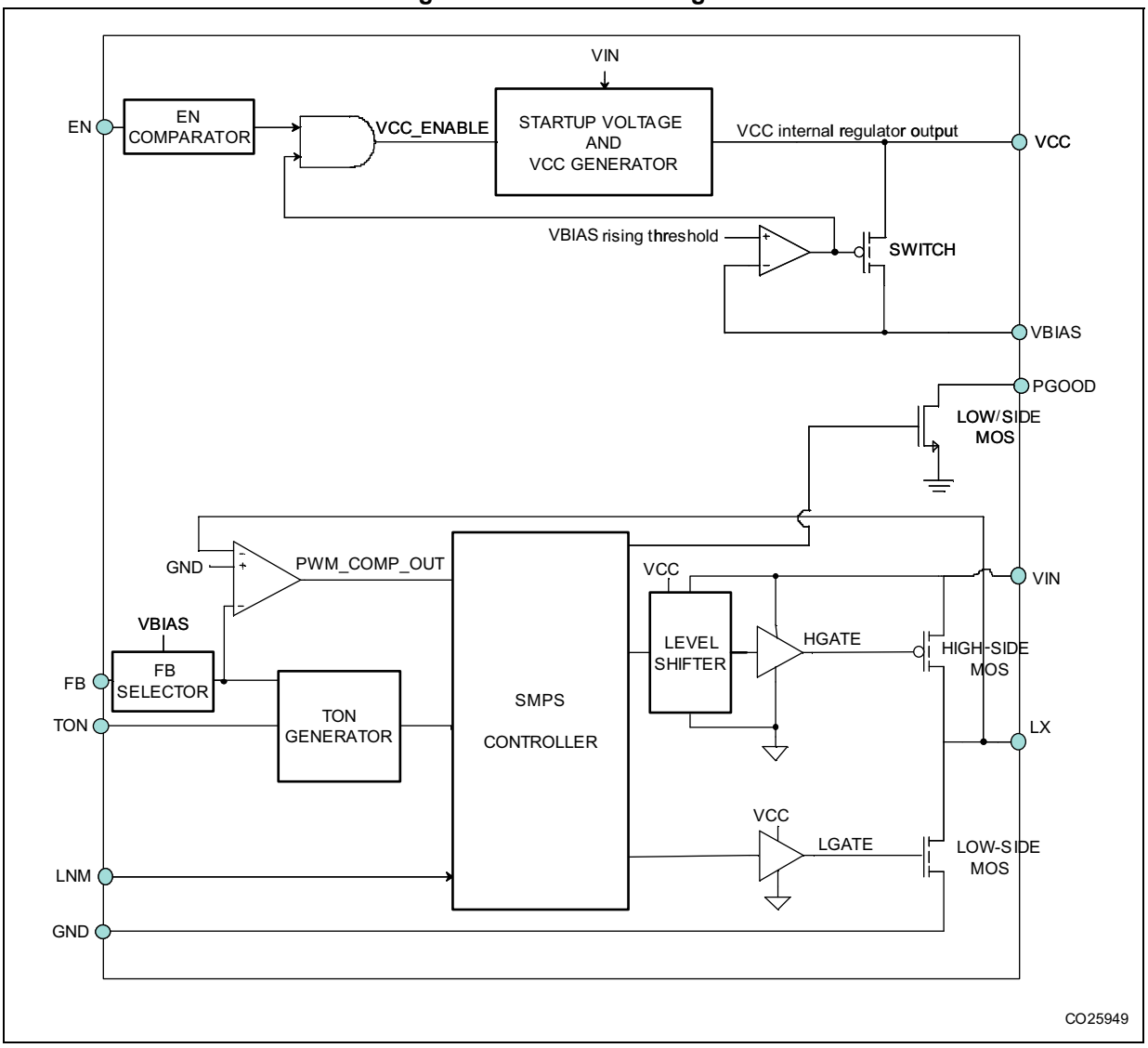
No external resistor divider is required to regulate fixed 3.3 V output voltage, connecting FB to the V_{CC} pin and V_{BIAS} to the regulated output voltage (see *Figure 1 on page 1*). An external voltage divider implements the output voltage adjustability.

The switchover capability of the internal regulator derives a portion of the quiescent current from an external voltage source (V_{BIAS} pin is typically connected to the regulated output voltage) to maximize the efficiency at the light load.

The device main internal blocks are shown in the block diagram in *Figure 5*:

- The bandgap reference voltage
- The on-time controller
- A “Pulse Width Modulator” (PWM) comparator and the driving circuitry of the embedded power elements
- The SMPS controller block
- The soft-start block to ramp the current limitation
- The switchover capability of the internal regulator to supply a portion of the quiescent current when the VBIAS pin is connected to an external output voltage
- The current limitation circuit to implement the constant current protection, sensing pulse-by-pulse low-side switch current.
- A circuit to implement the thermal protection function
- LNM pin strapping sets the LNM/LCM mode
- The PG (“Power Good”) open collector output
- The thermal protection circuitry.

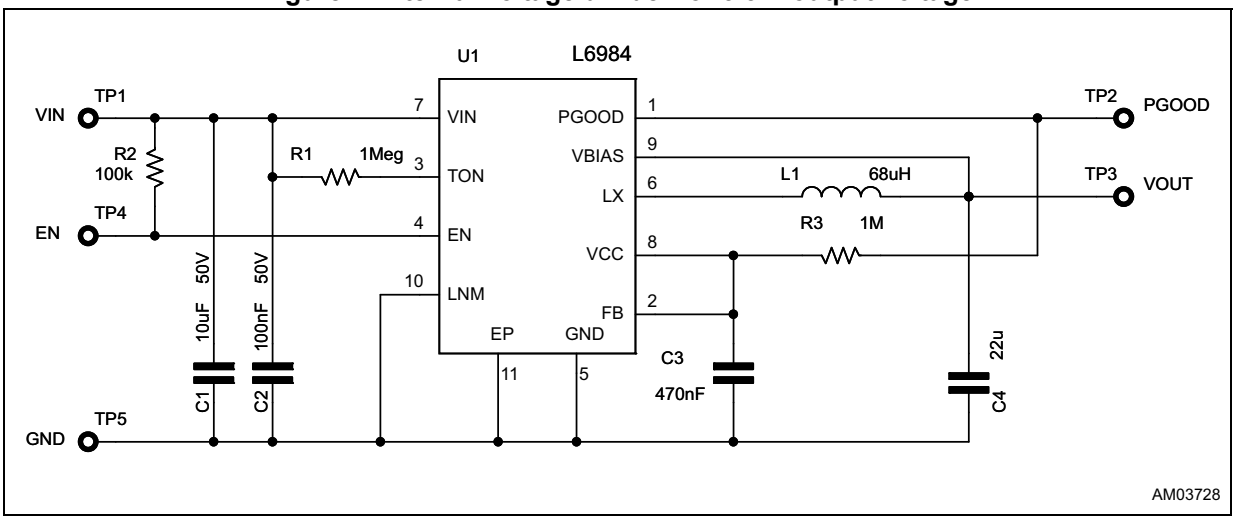
Figure 3. L6984 block diagram



3.1 Output voltage adjustment

No external resistor divider is required to regulate fixed 3.3 V output voltage, connecting FB to the V_{CC} pin and V_{BIAS} to the regulated output voltage (see *Figure 1 on page 1*). An external voltage divider otherwise implements the output voltage adjustability.

Figure 4. Internal voltage divider for 3.3 V output voltage



The error amplifier reference voltage is 0.9 V typical.

The output voltage is adjusted accordingly with the following formula (see *Figure 5*):

Equation 1

$$V_{OUT} = 0.9 \cdot \left(1 + \frac{R_3}{R_2}\right)$$

Leading network

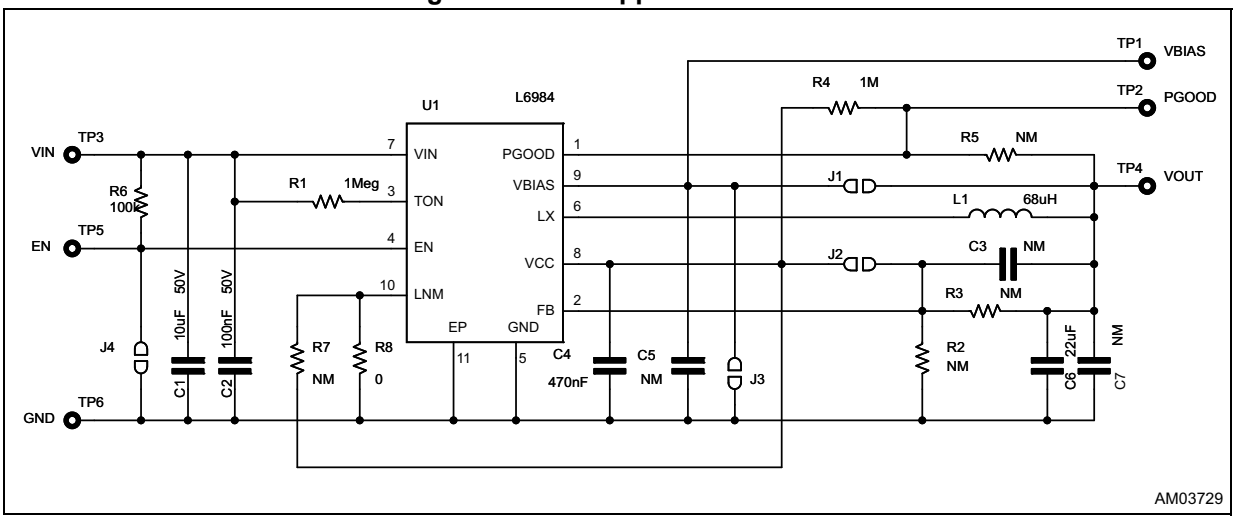
The small signal contribution of a simple voltage divider is:

Equation 2

$$G_{DIV}(s) = \frac{R_2}{R_2 + R_3}$$

A small signal capacitor in parallel to the upper resistor (see C3 in *Figure 5*) of the voltage divider implements a leading network ($f_{zero} < f_{pole}$) that can improve the dynamic regulation for boundary application conditions (high f_{SW} / high duty cycle conversion) or a not optimized board layout.

Figure 5. L6984 application circuit



Laplace transformer of the leading network:

Equation 3

$$G_{DIV}(s) = \frac{R_2}{R_2 + R_3} \cdot \frac{(1 + s \cdot R_3 \cdot C_{R3})}{\left(1 + s \cdot \frac{R_2 \cdot R_3}{R_2 + R_3} \cdot C_{R3}\right)}$$

where:

Equation 4

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_3 \cdot C_{R3}}$$

$$f_P = \frac{1}{2 \cdot \pi \cdot \frac{R_2 \cdot R_3}{R_2 + R_3} \cdot C_{R3}}$$

$$f_Z < f_P$$

The R2, R3 compose the voltage divider. C_{R3} is calculated as (see *Section 4.3.2: COUT specification and loop stability on page 26* for C_{OUT} selection):

Equation 5

$$C_{R3} = 28 \cdot 10^{-3} \cdot \frac{V_{OUT} \cdot C_{OUT}}{R_3}$$

3.2 Control loop

The L6984 device is based on a constant on-time control loop with frequency feed-forward correction over the input range. As a consequence the on-time generator compensates the input voltage variations in order to keep the switching frequency almost constant over the input voltage range.

A standard COT loop requires a high ESR output capacitor to generate a proper PWM signal. The L6984 device supports output ceramic capacitors with negligible ESR.

The controller generates a T_{ON} duration switching pulse as soon as the voltage ripple drops below the valley voltage threshold. The L6984 on-time is calculated as:

Equation 6

$$T_{ON} = \frac{0.9 \cdot R_{TON} \cdot C_{TON}}{V_{IN}} = \frac{0.9 \cdot R_{TON} \cdot 7.5pF}{V_{IN}}$$

where R_{TON} represents the external resistor connected between V_{IN}, T_{ON} pins and C_{TON} the overall contribution given by the integrated capacitor and the parasitic capacitor of the board trace at the pin 3.

C_{TON} value for the L6984 soldered on the STM evaluation board is 7.5 pF typical, anyway it depends on the parasitic capacitance connected at the pin 3 (TON) that changes over the different board layouts. If the final application requires precise TON adjustment, a further fine tune for R_{TON} value may be required accordingly with the designed board layout. This is simply done adjusting the R_{TON} value to get the desired TON value with direct scope measurement.

The L6984 internal circuitry compensates the TOFF time variation over the input voltage range to keep the switching frequency almost constant.

The almost constant switching frequency depends on the output current and it can be calculated as:

Equation 7

$$f_{SW}(I_{OUT}) = \frac{D_{REAL}(I_{OUT})}{T_{ON}}$$

where D_{REAL} is the real duty cycle accounting conduction losses:

Equation 8

$$D_{REAL}(I_{OUT}) = \frac{V_{OUT} + (R_{ON\_LS} + DCR) \cdot I_{OUT}}{V_{IN} + (R_{ON\_LS} - R_{ON\_HS}) \cdot I_{OUT}}$$

R_{ON_HS} and R_{ON_LS} represent the RDSON value of the embedded power elements (see *Table 5 on page 7*) and DCR the equivalent series resistor of the selected inductor.

The L6984 small signal loop compensates the internal losses, that depends on the output current value, adjusting the TOFF time so the switching frequency.

Finally from *Equation 6* and *Equation 7*:

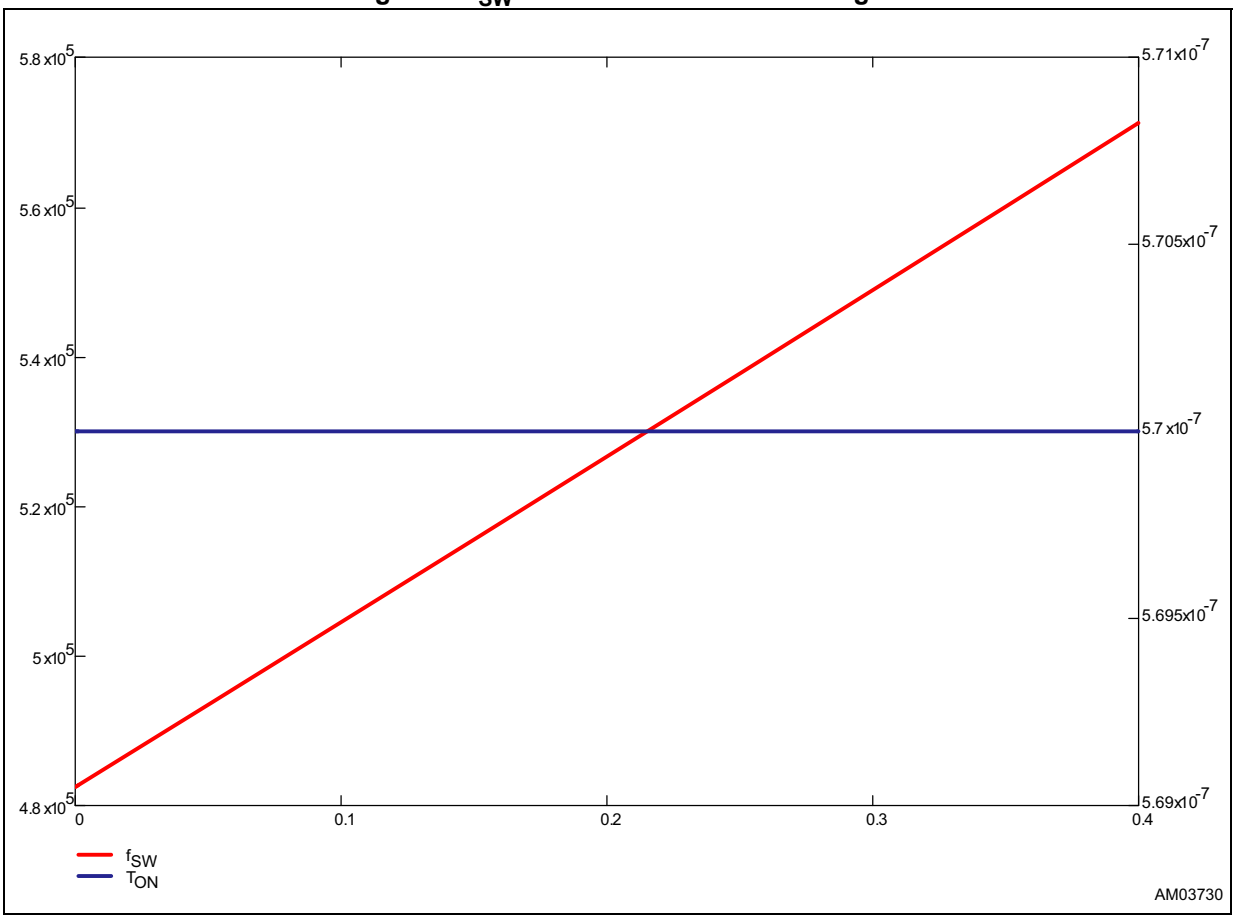
Equation 9

$$R_{TON} = \frac{1}{0.9} \cdot \frac{V_{IN} \cdot D_{REAL}(I^{*}_{OUT})}{f_{SW} \cdot C_{TON}}$$

where f_{SW} is the desired switching frequency at a certain load current level.

Figure 6 shows the estimated f_{SW} variation over the load range assuming the typical RDSON of the power elements, DCR = 420 mΩ (see *Section 5 on page 27* for details of the selected inductor for the reference application board.) and R_{TON} = 1 Meg.

Figure 6. f_{SW} variation over the load range



3.3 Soft-start

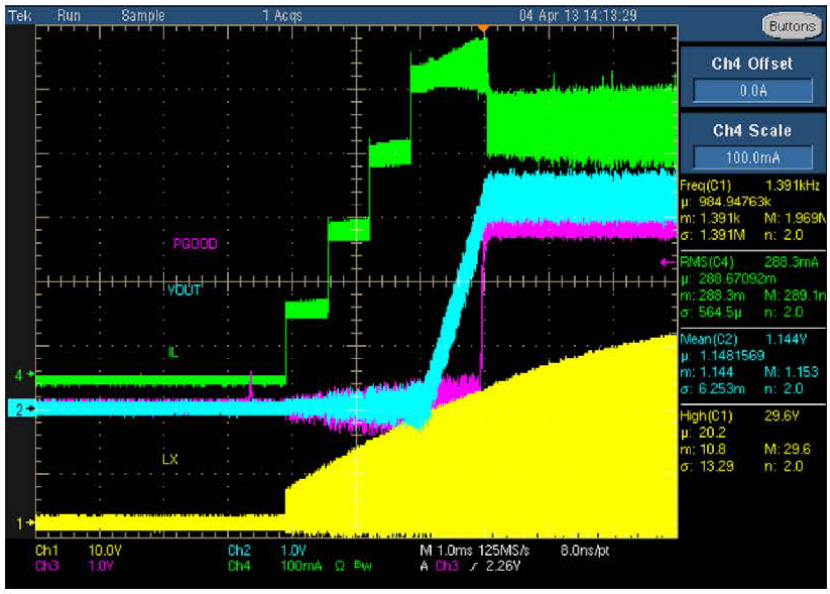
The soft-start feature minimizes the inrush current and decreases the stress of the power components during the power-up phase. The L6984 implements the soft-start clamping the device current limitation in four different steps.

During normal operation a new soft-start cycle takes place in case of:

- Thermal shutdown event
- UVLO event
- EN pin rising

Figure 7 shows the soft-start feature. The green trace represents the inductor current which shows different current protection thresholds.

Figure 7. Soft-start feature



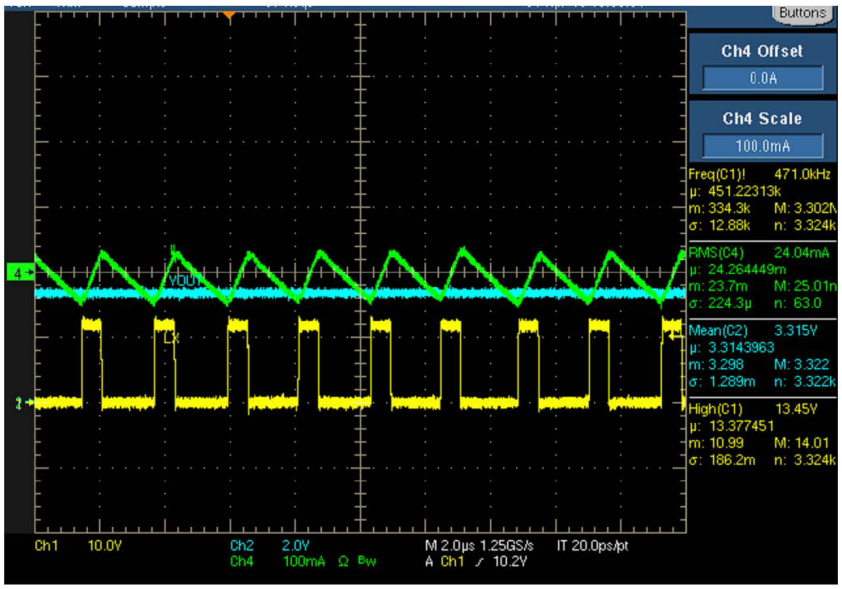
3.4 Light load operation

The LNM pinstrapping during the power-up phase determines the light load operation.

3.4.1 Low noise mode (LNM)

Low noise mode implements a forced PWM operation over the different loading conditions. The LNM features a constant switching frequency to minimize the noise in the final application and a constant voltage ripple at fixed V_{IN}. The regulator in steady loading condition never skips pulses and it operates in continuous conduction mode (CCM) over the different loading conditions.

Figure 8. Low noise mode operation



Typical applications for the LNM operation are car audio, sensors.

3.4.2 Low consumption mode (LCM)

The low consumption mode maximizes the efficiency at the light load. As soon as the output voltage drops, the regulator generates a pulse to have the FB back in regulation. In order to minimize the current consumption in the LCM part of the internal circuitry is disabled in the time between bursts.

Figure 9. LCM operation at zero load

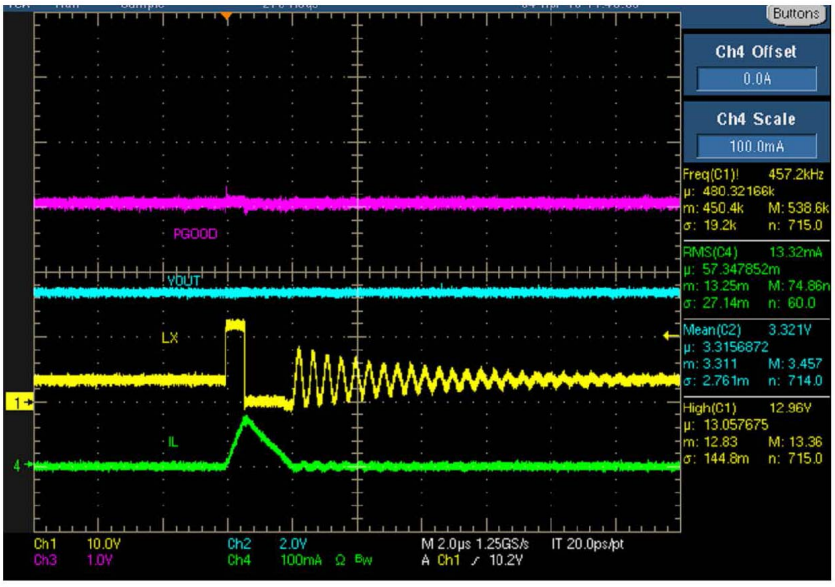
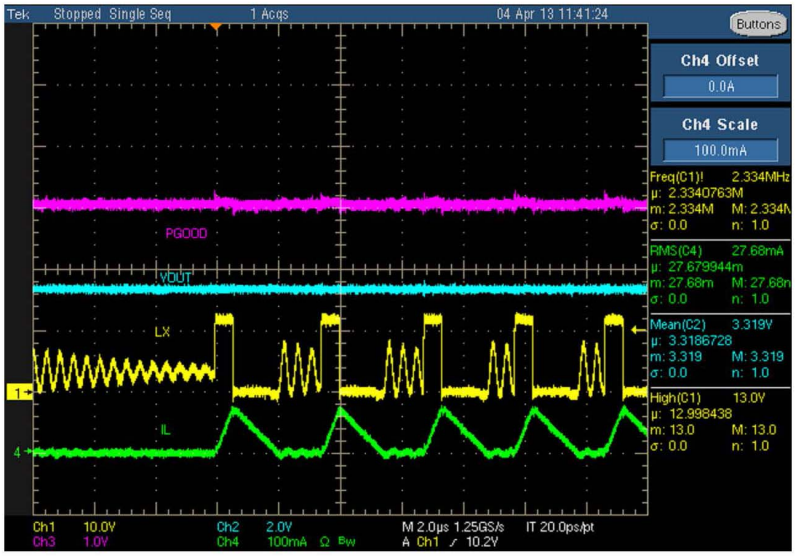


Figure 10. LCM operation over loading condition (1)

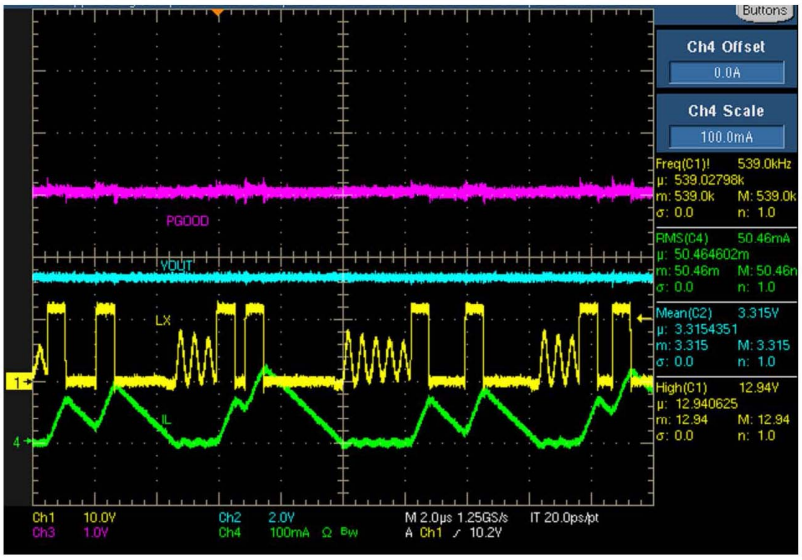


Given the energy stored in the inductor during a burst, the voltage ripple depends on the capacitor value:

Equation 10

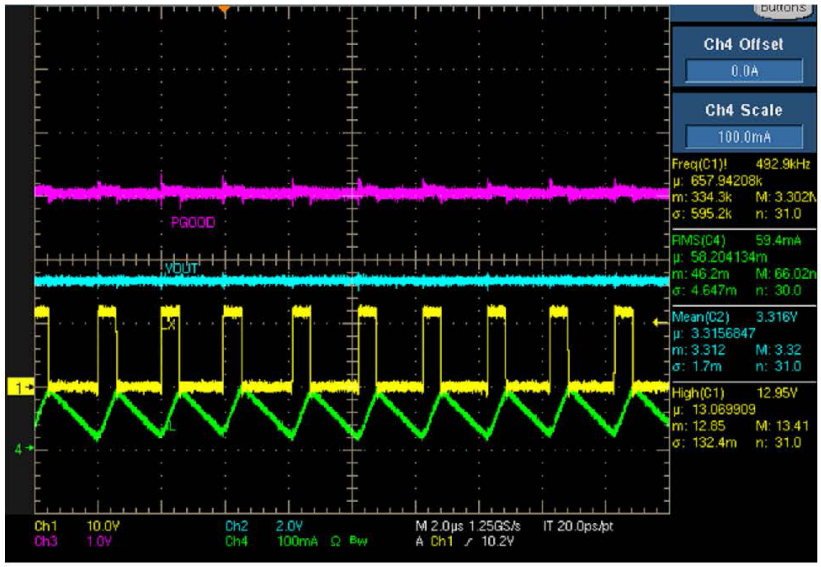
$$V_{OUT\ RIPPLE} = \frac{\Delta Q_{IL}}{C_{OUT}} = \frac{\int_0^{T_{BURST}} (i_L(t) \cdot dt)}{C_{OUT}}$$

Figure 11. LCM operation over loading condition (2)



When the load current is higher, the $I_{RIPPLE}/2$ the regulator works in CCM.

Figure 12. The regulator works in CCM



3.5 Switchover feature

The switch over maximizes the efficiency at the light load that is crucial for LCM applications.

The main switching controller is supplied by the VCC pin regulator

An integrated LDO regulates VCC = 3.3 V if VBIAS voltage is < 2.4 V.

VCC is connected to VBIAS through a MOSFET switch if VBIAS > 3.2 V and the embedded LDO is disabled to increase the light load efficiency.

3.5.1 LCM

The LCM operation satisfies the requirements of battery powered applications where it is crucial to increase the efficiency at the light load.

In order to minimize the regulator quiescent current request from the input voltage, the VBIAS pin can be connected to an external voltage source in the range 3 V < V_{BIAS} < 5.5 V.

In case the VBIAS pin is connected to the regulated output voltage (V_{OUT}), the total current drawn from the input voltage can be calculated as:

Equation 11

$$I_{Q\ VIN} = I_{Q\ OP\ VIN} + \frac{1}{\eta_{L6984}} \cdot \frac{V_{BIAS}}{V_{IN}} \cdot I_{Q\ OP\ VBIAS}$$

where $I_{Q\ OP\ VIN}$, $I_{Q\ OP\ VBIAS}$ are defined in *Table 5: Electrical characteristics on page 7* and η_{L6984} is the efficiency of the conversion in the working point.

3.5.2 LNM

Equation 11 is also valid when the device works in LNM and it can boost the efficiency at the medium load since the regulator always operates in continuous conduction mode.

3.6 Overcurrent protection

The current protection circuitry features a constant current protection, so the device limits the maximum current (see *Table 5: Electrical characteristics on page 7*) in overcurrent condition.

The low-side switch pulse-by-pulse current sensing, called “valley”, implements the constant current protection. In overcurrent condition the internal logic keeps the low-side switch conducting as long as the switch current is higher than the valley current threshold.

As a consequence the maximum DC output current is:

Equation 12

$$I_{MAX} = I_{VALLEY\_TH} + \frac{I_{RIPPLE}}{2} = I_{VALLEY\_TH} + \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON}$$

Figure 13. Constant current operation in dynamic short-circuit

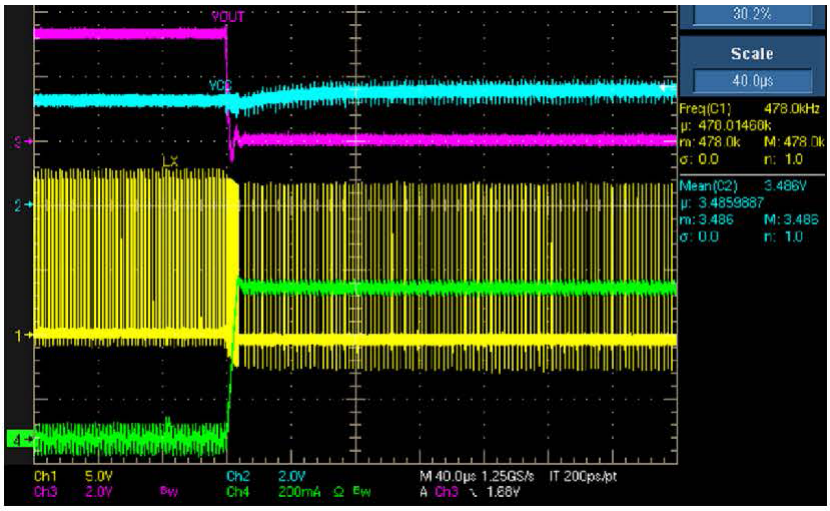
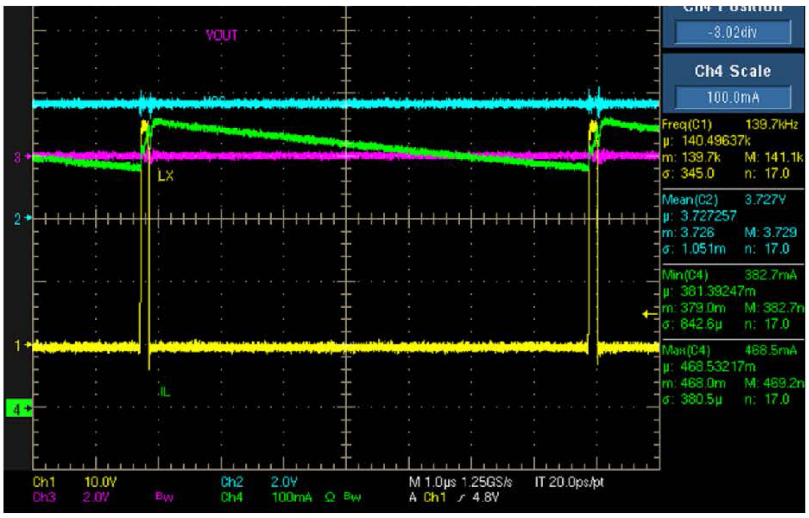


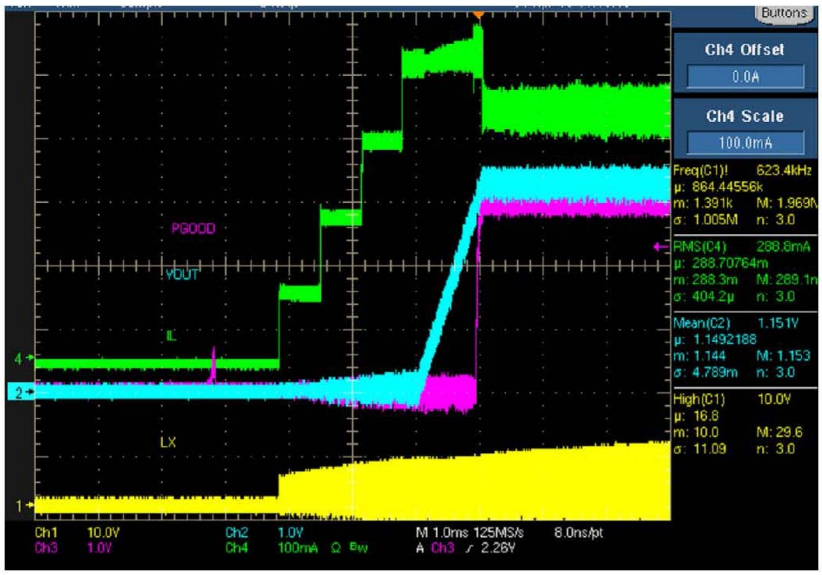
Figure 14. Valley current sense implements constant current protection



3.7 PGOOD

The internal circuitry monitors the regulated output voltage and keeps the PGOOD open collector output in low impedance as long as the feedback voltage is below the $V_{PGD\ L}$ threshold (see *Table 5*).

Figure 15. PGOOD behavior during soft-start time



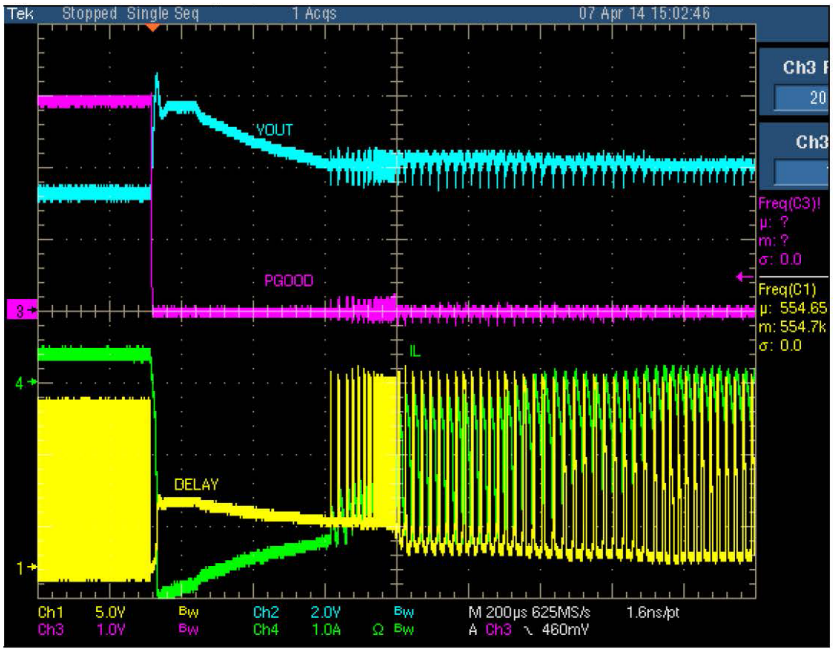
The PGOOD is driven low impedance if $V_{FB} = V_{CC}$ (internal voltage divider, see *Section 3.1 on page 12*) and $V_{BIAS} > V_{PGD\ H}$ threshold (see *Table 5 on page 7*).

The $V_{PGD\ H}$ threshold has no effect on PGOOD behavior in case the external voltage divider is being used.

3.8 Overvoltage protection

The overvoltage protection monitors the FB pin and enables the low-side MOSFET to discharge the output capacitor if the output voltage is 20% over the nominal value. A new soft-start takes place after the OVP event ends.

Figure 16. Overvoltage operation



The OVP feature is a second level protection and should never be triggered in normal operating conditions if the system is properly dimensioned. In other words, the selection of the external power components and the dynamic performance should guarantee an output voltage regulation within the overvoltage threshold even during the worst case scenario in term of load transitions.

The protection is reliable and also able to operate even during normal load transitions for a system whose dynamic performance is not in line with the load dynamic request. As a consequence the output voltage regulation would be affected.

In *Figure 16* the PGOOD output is driven in low impedance (refer to *Section 3.7*) as long as the OVP event is present ($V_{FB} = V_{CC}$, that is an internal resistor divider for $V_{OUT} = 3.3$ V).

3.9 Thermal shutdown

The shutdown block disables the switching activity if the junction temperature is higher than a fixed internal threshold (150 °C typical). The thermal sensing element is close to the power elements, ensuring fast and accurate temperature detection. A hysteresis of approximately 20 °C prevents the device from turning ON and OFF continuously. When the thermal protection runs away a new soft-start cycle will take place.

4 Design of the power components

4.1 Input capacitor selection

The input capacitor voltage rating must be higher than the maximum input operating voltage of the application. During the switching activity a pulsed current flows into the input capacitor and so its RMS current capability must be selected accordingly with the application conditions. Internal losses of the input filter depend on the ESR value, so usually low ESR capacitors (like multilayer ceramic capacitors) have a higher RMS current capability. On the other hand, given the RMS current value, lower ESR input filter has lower losses and so contributes to higher conversion efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

Equation 13

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

Where I_O is the maximum DC output current, D is the duty cycles, η is the efficiency. This function has a maximum at D = 0.5 and, considering η = 1, it is equal to $I_O/2$.

In a specific application the range of possible duty cycles has to be considered in order to find out the maximum RMS input current. The maximum and minimum duty cycles can be calculated as:

Equation 14

$$D_{MAX} = \frac{V_{OUT} + \Delta V_{LOW\_SIDE}}{V_{INMIN} + \Delta V_{LOW\_SIDE} - \Delta V_{HIGH\_SIDE}}$$

and

Equation 15

$$D_{MIN} = \frac{V_{OUT} + \Delta V_{LOW\_SIDE}}{V_{INMAX} + \Delta V_{LOW\_SIDE} - \Delta V_{HIGH\_SIDE}}$$

Where ΔV_{HIGH_SIDE} and ΔV_{LOW_SIDE} are the voltage drops across the embedded switches.

The peak-to-peak voltage across the input filter can be calculated as:

Equation 16

$$V_{PP} = \frac{I_O}{C_{IN} \cdot f_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right] + ESR \cdot I_O$$

In case of negligible ESR (MLCC capacitor) the equation of C_{IN} as a function of the target V_{PP} can be written as follows:

Equation 17

$$C_{IN} = \frac{I_O}{V_{PP} \cdot f_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right]$$

Considering $\eta = 1$ this function has its maximum in D = 0.5:

Equation 18

$$C_{IN\_MIN} = \frac{I_O}{2 \cdot V_{PP\_MAX} \cdot f_{SW}}$$

Typically C_{IN} is dimensioned to keep the maximum peak-to-peak voltage across the input filter in the order of 5% V_{IN_MAX}.

Table 6. Input capacitors

Manufacture	Series	Size	Cap value (µF)	Rated voltage (V)
TDK	C3225X7S1H106M	1210	10	50
	C3216X5R1H106M	1206		
Taiyo Yuden	UMK325BJ106MM-T	1210		

4.2 Inductor selection

The inductor current ripple flowing into the output capacitor determines the output voltage ripple (please refer to *Section 4.3: Output capacitor selection*). Usually the inductor value is selected in order to keep the current ripple lower than 20% - 40% of the output current over the input voltage range. The inductance value can be calculated by the following equation:

Equation 19

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT}}{L} \cdot T_{OFF}$$

Where T_{ON} and T_{OFF} are the on and off time of the internal power switch. The maximum current ripple, at fixed $V_{OUT,}$ is obtained at maximum T_{OFF} that is at minimum duty cycle (see *Section 4.1* to calculate minimum duty). So fixing ΔI_L = 20 % to 40 % of the maximum output current, the minimum inductance value can be calculated:

Equation 20

$$L_{MIN} = \frac{V_{OUT}}{\Delta I_{MAX}} \cdot \frac{1 - D_{MIN}}{F_{SW}}$$

where F_{SW} is the switching frequency $1/(T_{ON} + T_{OFF})$.

For example for V_{OUT} = 3.3 V, V_{IN} = 12 V, I_O = 0.4 A and F_{SW} = 600 kHz the minimum inductance value to have ΔI_L = 30 % of I_O is about 33 µH.

The peak current through the inductor is given by:

Equation 21

$$I_{L,PK} = I_O + \frac{\Delta I_L}{2}$$

So if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. The higher is the inductor value, the higher is the average output current that can be delivered, without reaching the current limit.

In the table below some inductor part numbers are listed.

Table 7. Inductors

Manufacturer	Series	Inductor value (μH)	Saturation current (A)
Coilcraft	LPS6225	47 to 150	0.98 to 0.39
	LPS5030	10 to 47	1.4 to 0.5

4.3 Output capacitor selection

4.3.1 Output voltage ripple

The triangular shape current ripple (with zero average value) flowing into the output capacitor gives the output voltage ripple, that depends on the capacitor value and the equivalent resistive component (ESR). As a consequence the output capacitor has to be selected in order to have a voltage ripple compliant with the application requirements.

The voltage ripple equation can be calculated as:

Equation 22

$$\Delta V_{OUT} = ESR \cdot \Delta I_{MAX} + \frac{\Delta I_{MAX}}{8 \cdot C_{OUT} \cdot f_{SW}}$$

Usually the resistive component of the ripple can be neglected if the selected output capacitor is a multilayer ceramic capacitor (MLCC).

For example with V_{OUT} = 3.3 V, V_{IN} = 12 V, ΔI_L = 0.12 A, f_{SW} = 600 kHz (resulting by the inductor value) and C_{OUT} = 4.7 μF MLCC:

Equation 23

$$\frac{\Delta V_{OUT}}{V_{OUT}} \cong \frac{1}{V_{OUT}} \cdot \frac{\Delta I_{MAX}}{8 \cdot C_{OUT} \cdot f_{SW}} = \left(\frac{1}{3.3} \cdot \frac{0.12}{8 \cdot 4.7\mu F \cdot 600kHz}\right) = \frac{5mV}{3.3} = 0.15\%$$

The output capacitor value has a key role to sustain the output voltage during a steep load transient. When the load transient slew rate exceeds the system bandwidth, the output capacitor provides the current to the load. In case the final application specifies a high slew rate load transient, the system bandwidth must be maximized and the output capacitor has to sustain the output voltage for time response shorter than the loop response time.

In the table below some capacitor series are listed.

Table 8. Output capacitors

Manufacturer	Series	Cap value (μF)	Rated voltage (V)	ESR (mΩ)
MURATA	GRM32	22 to 100	6.3 to 25	< 5
	GRM31	10 to 47	6.3 to 25	< 5
PANASONIC	ECJ	10 to 22	6.3	< 5
	EEFCD	10 to 68	6.3	15 to 55
SANYO	TPA/B/C	100 to 470	4 to 16	40 to 80
TDK	C3225	22 to 100	6.3	< 5

4.3.2 C_{OUT} specification and loop stability

Output capacitor value

A minimum output capacitor value is required for the COT loop stability:

Equation 24

$$C_{OUT} \geq \frac{35}{V_{OUT} \cdot f_{SW}}$$

Equivalent series resistor (ESR)

The maximum ESR of the output capacitor is:

Equation 25

$$ESR_{MAX} \leq 2.8 \cdot 10^{-3} \cdot V_{OUT}$$

5 Application board

The reference evaluation board schematic is shown in *Figure 17*.

Figure 17. Evaluation board schematic

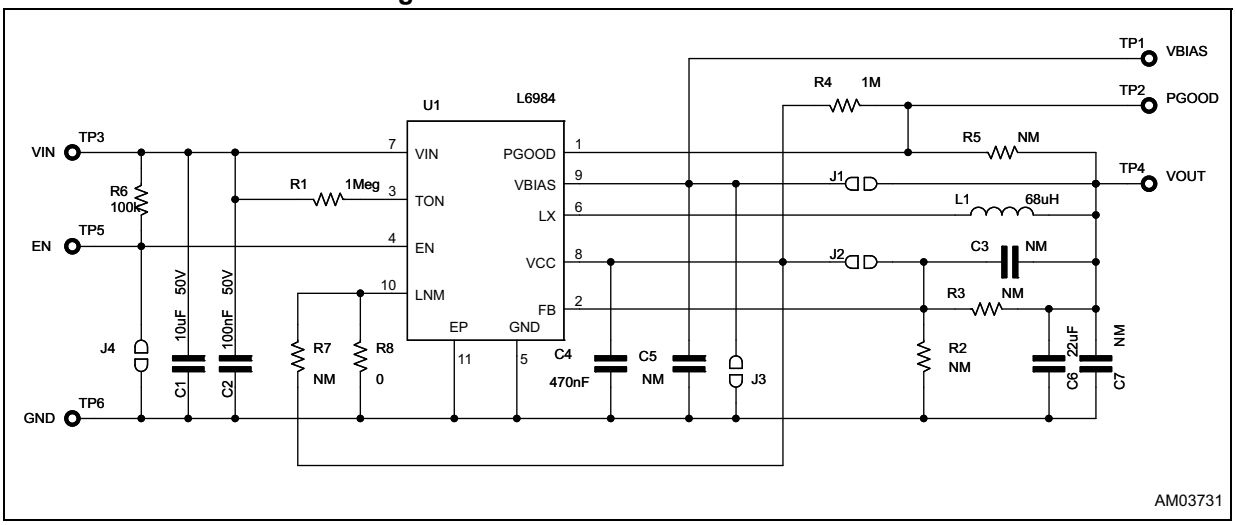


Table 9. Bill of material

Reference	Part number	Description	Manufacturer
C1	C3216X5R1H106M	10 µF - 50 V - 1206	TDK
C2		100 nF - 50 V - 0805	
C4		470 nF - 10 V - 0603	
C6	C3216X5R1E226M	22 µF - 25 V - 1206	TDK
L1	LPS6225-683MLC	68 µH	Coilcraft
R1		1 MΩ - 1% - 0603	
R4		1 MΩ - 5% - 0603	
R6		100 kΩ - 5% - 0603 V	
R8		0 Ω - 0603	
U1	L6984		STM
J1		JUMPER - CLOSED	
J2		JUMPER - CLOSED	
J3		JUMPER - OPEN	
J4		JUMPER - OPEN	
R2, R3, C3, R5, C5, R7, C7		NOT MOUNTED	
TP1, TP2, TP3, TP4, TP5, TP6, TP7		VBIAS, PGOOD, VIN, VOUT, EN, GND, GND	

Figure 18. Top layer 3 x 3 DFN demonstration board

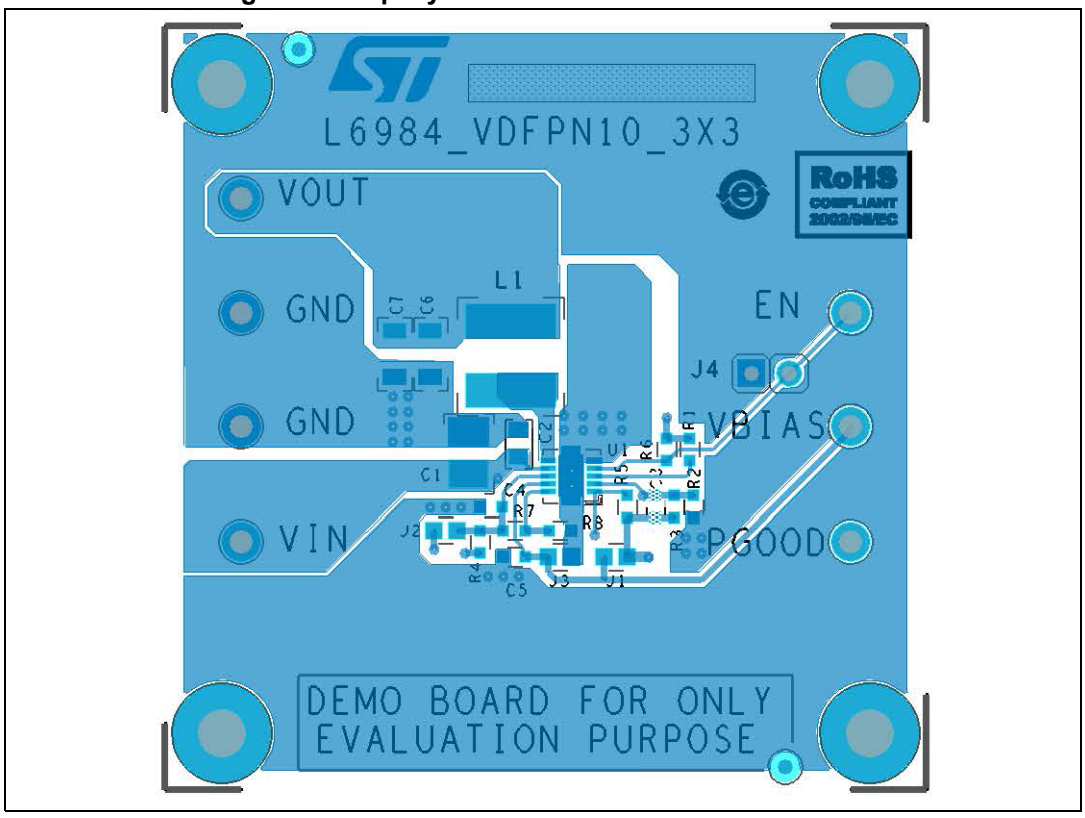


Figure 19. Bottom layer 3 x 3 DFN demonstration board

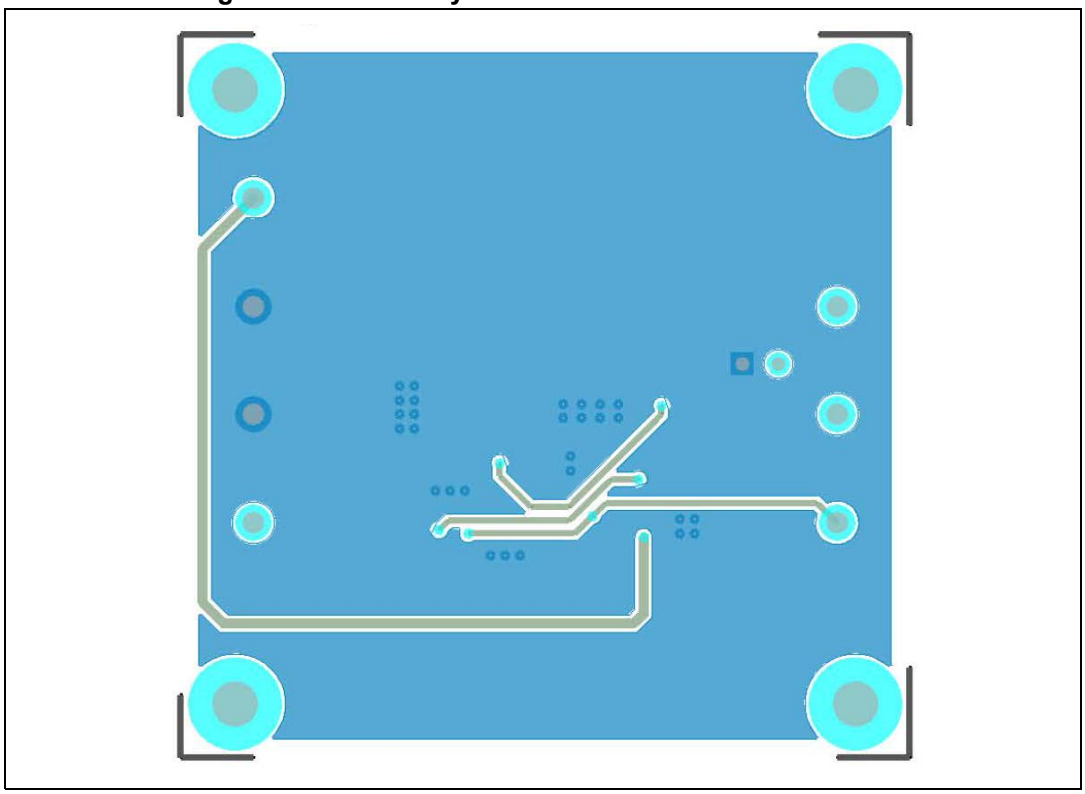


Figure 20. Top layer 4 x 4 DFN demonstration board

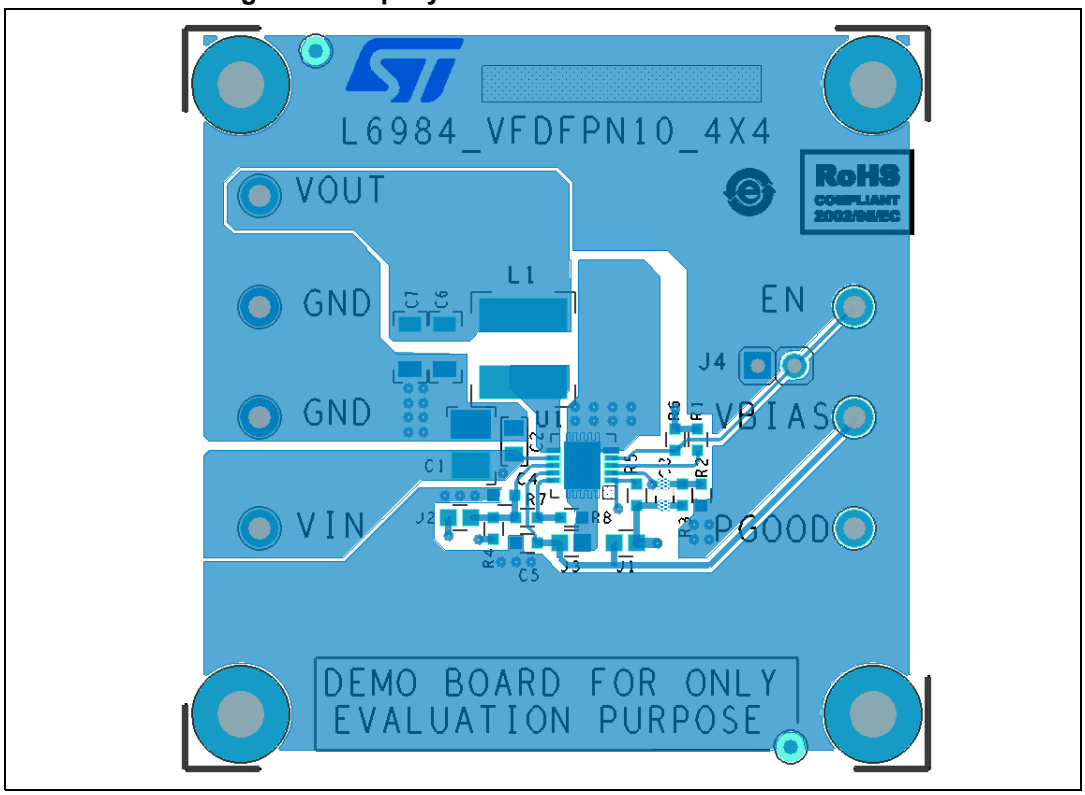
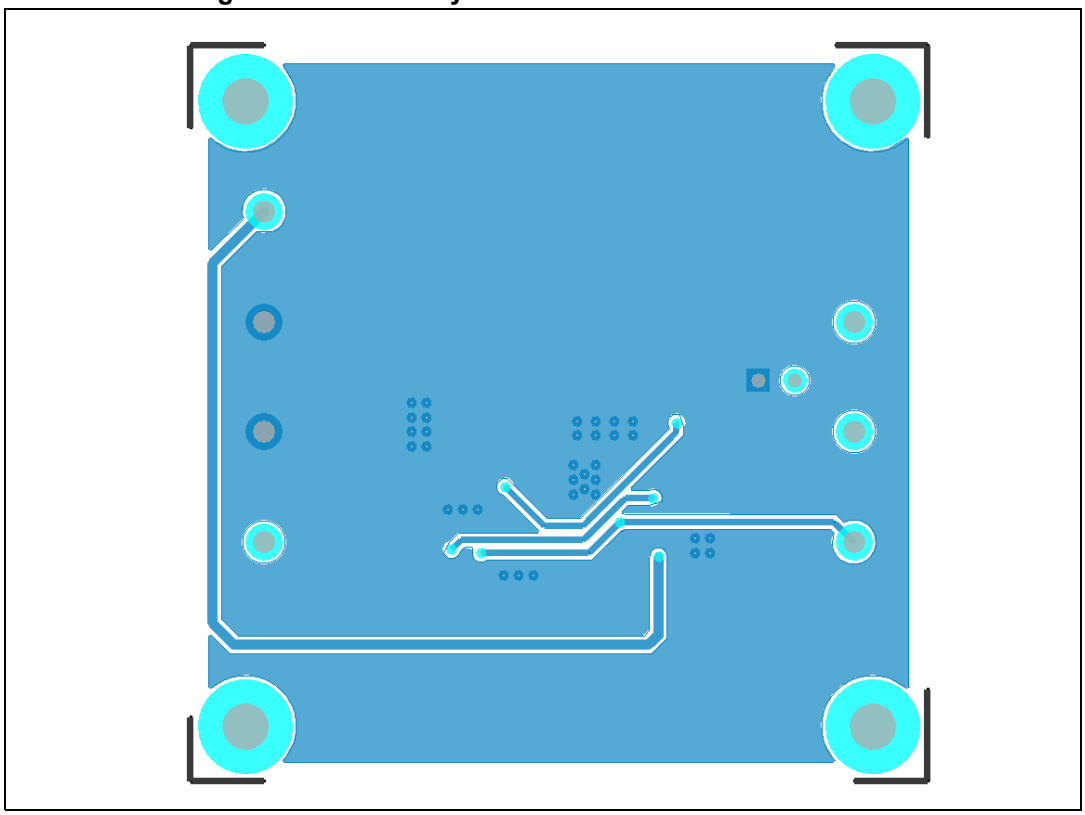


Figure 21. Bottom layer 4 x 4 DFN demonstration board



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 22. VFDFPN10 4 x 4 x 1.0 mm package outline

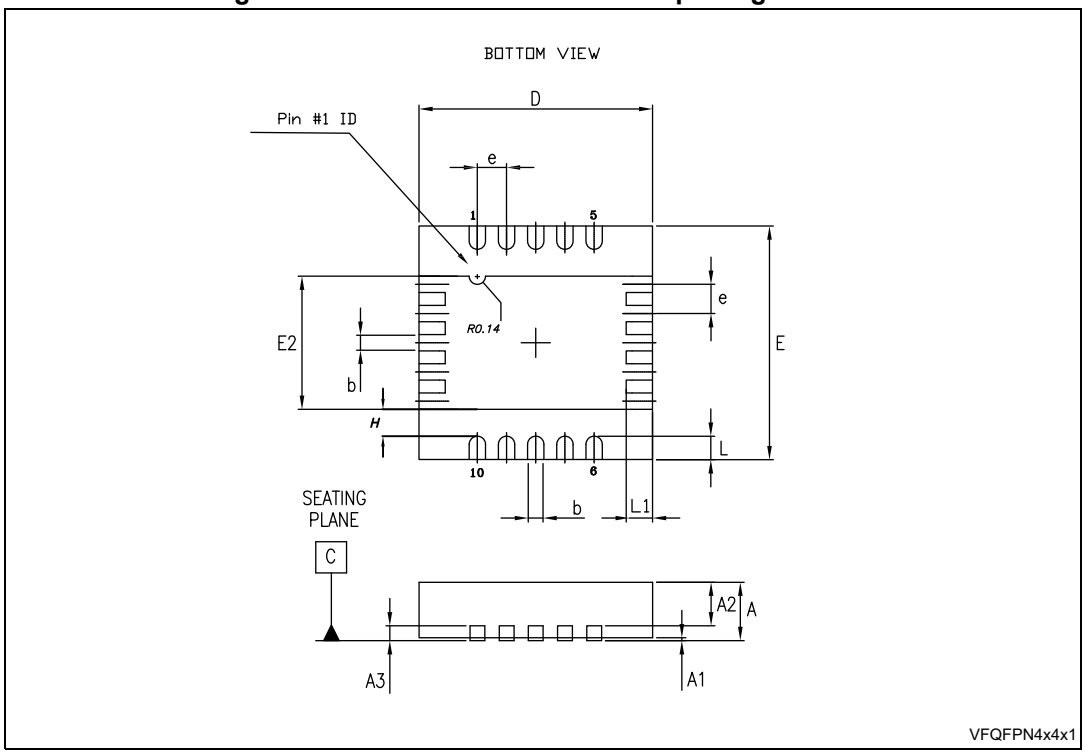
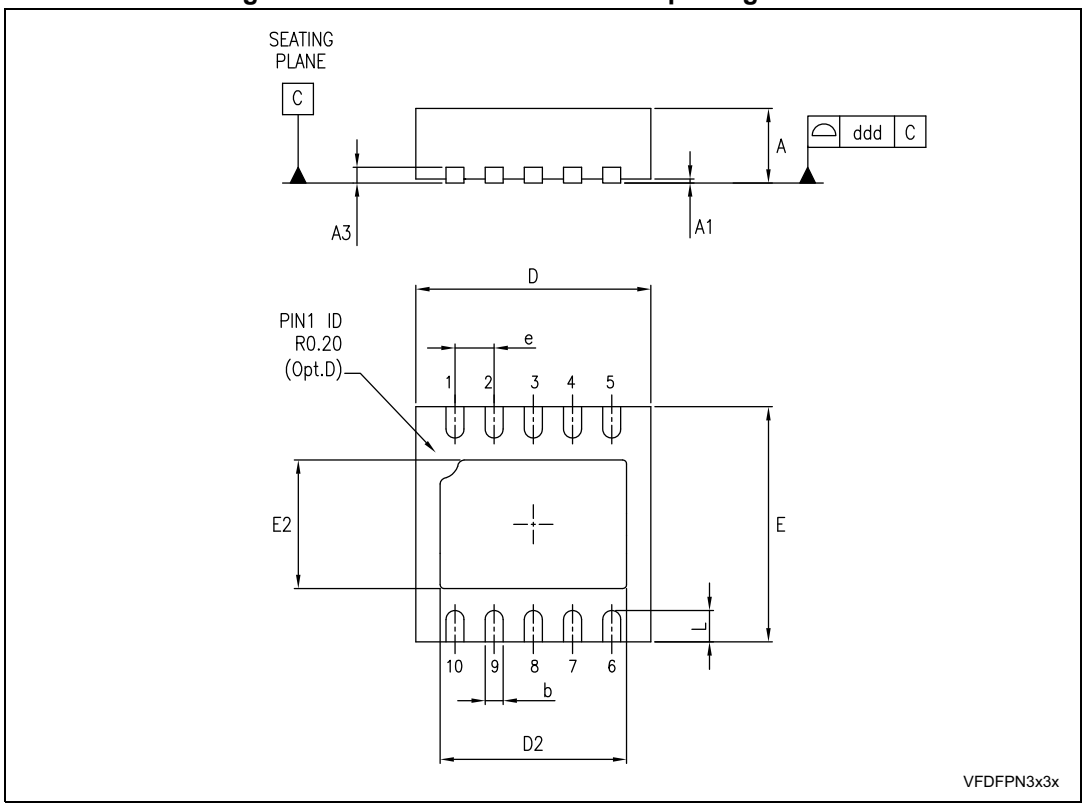


Table 10. VFDFPN10 4 x 4 x 1.0 mm package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1		0.02	
A2		0.65	
A3		0.20	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
E2	2.15	2.25	2.35
e	0.45	0.50	0.55
H		0.46	
L	0.30	0.40	0.50
L1	0.35	0.45	0.55

Figure 23. VDFPN10 3 x 3 x 1.0 mm package outline



1. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body. Exact shape and size of this feature is optional.

Table 11. VDFPN10 3 x 3 x 1.0 mm mechanical data

Symbol	Dimensions (mm)			Note
	Min.	Typ.	Max.	
A	0.80	0.90	1.00	(1)
A1		0.02	0.05	
A2	0.55	0.65	0.80	
A3		0.20		
b	0.18	0.25	0.30	
D	2.85	3.00	3.15	
D2	2.20		2.70	
E	2.85	3.00	3.15	
E2	1.40		1.75	
e		0.50		
L	0.30	0.40	0.50	
ddd			0.08	

1. VFDFPN stands for “Thermally Enhanced Very thin Fine pitch Dual Flat Packages No lead”. Very thin: 0.80 mm < A . 1.00 mm / fine pitch: e < 1.00 mm.

7 Order codes

Table 12. Order codes

Part number	Package	Packaging
L6984	VFDFPN10 4 x 4	Tube
L6984TR	VFDFPN10 4 x 4	Tape and reel
L6984A	VDFPN10 3 x 3	Tube
L6984ATR	VDFPN10 3 x 3	Tape and reel

8 Revision history

Table 13. Document revision history

Date	Revision	Changes
11-Oct-2013	1	Initial release.
30-May-2014	2	Updated main title*: 36 V 400 mA synchronous step-down switching regulator on page 1* (replaced “350 mA” by “400 mA”). Updated *Section : Features on page 1* (replaced “350 mA” by “400 mA ”in “DC output current”). Updated *Section : Description on page 1* (replaced “350 mA” by “400 mA” in “DC”). Updated *Figure 1: Application schematic on page 1* (replaced by new figure, moved from page 2 to page 1). Added *Contents on page 2*. Updated *Table 1.: Pin description on page 4* (minor modifications throughout table). Updated *Section 1.3: Maximum ratings on page 5* (added text above *Table 2*, added I_{HS} and I_{LS} max. values in *Table 2*). Updated *Table 3.: Thermal data on page 5* (added value for “$R_{th\ JA}$” symbol). Updated *Table 5.: Electrical characteristics on page 7* (updated notes *1.* to *3.*, minor modifications throughout table). Added *Section 3: Device description on page 10*, *Section 4: Design of the power components on page 23* and *Section 5: Application board on page 27*. Added and updated cross-references throughout document. Minor modifications throughout document.
04-Jul-2014	3	Updated *Table 1.: Pin description on page 4* (updated Description of VCC pin). Updated *Section 3.5: Switchover feature on page 19* (added text).

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