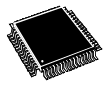
STM32F437xx

ARM Cortex-M4 32b MCU+FPU, 210DMIPS, up to 2MB Flash/256+4KB RAM, crypto, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 20 comm. interfaces & camera

Data brief

Features

- Core: ARM 32-bit Cortex™-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 168 MHz, memory protection unit, 210 DMIPS/ 1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
  - Up to 2 Mbyte of Flash memory
  - Up to 256+4 Kbytes of SRAM including 64-Kbyte of CCM (core coupled memory) data RAM
  - Flexible static memory controller supporting Compact Flash, SRAM, PSRAM, NOR and NAND memories
- LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 1.8 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC (1% accuracy)
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC, 20×32 bit backup registers + optional 4 KB backup SRAM
- 3×12-bit, 2.4 MSPS A/D converters: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 17 timers: up to twelve 16-bit and two 32-bit timers up to 168 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex-M4 Embedded Trace Macrocell™



LQFP100 (14 × 14 mm)
LQFP144 (20 × 20 mm)
LQFP176 (24 × 24 mm)

UFBGA176
(10 × 10 mm)

- Up to 140 I/O ports with interrupt capability
  - Up to 136 fast I/Os up to 84 MHz
  - Up to 138 5 V-tolerant I/Os
- Up to 20 communication interfaces
  - Up to 3 × I^2C interfaces (SMBus/PMBus)
  - Up to 4 USARTs/4 UARTs (10.5 Mbit/s, ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 6 SPIs (42 Mbits/s), 2 with muxed full-duplex I^2S to achieve audio class accuracy via internal audio PLL or external clock
  - 2 × CAN interfaces (2.0B Active)
  - SDIO interface
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
  - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- Cryptographic acceleration: hardware acceleration for AES 128, 192, 256, Triple DES, HASH (MD5, SHA-1, SHA-2), and HMAC
- True random number generator
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar

Table 1. Device summary

Reference	Part number
STM32F437xx	STM32F437VG, STM32F437ZG, STM32F437IG, STM32F437VI, STM32F437ZI, STM32F437II

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1 Introduction

This databrief provides the description of the STM32F437xx line of microcontrollers. For more details on the whole STMicroelectronics STM32™ family, please refer to *Section 2.1: Full compatibility throughout the family*.

The STM32F437xx datasheet should be read in conjunction with the STM32F4xx reference manual.

The reference manual is available from the STMicroelectronics website *www.st.com*. It includes all information concerning Flash memory programming.

For information on the Cortex™-M4 core, please refer to the Cortex™-M4 programming manual (PM0214) available from www.st.com.

2 Description

The STM32F437xx devices is based on the high-performance ARM® Cortex™-M4 32-bit RISC core operating at a frequency of up to 168 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security. The Cortex-M4 core with FPU will be referred to as Cortex-M4F throughout this document.

The STM32F437xx devices incorporates high-speed embedded memories (Flash memory up to 2 Mbytes, up to 256 Kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers. a true random number generator (RNG), and a cryptographic acceleration cell. They also feature standard and advanced communication interfaces.

- Up to three I^2Cs
- Six SPIs
- Two I^2Ss full duplex. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- Two USB OTG full-speed with internal PHY or one USB OTG high-speed (with ULPI interface) plus one USB OTG full-speed with internal PHY
- Two CANs
- An SDIO/MMC interface

The advanced peripherals include an enhanced flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more), a camera interface for CMOS sensors and a cryptographic acceleration cell. Refer to *Table 2: STM32F437xx features and peripheral counts* for the list of peripherals available on each part number.

The STM32F437xx devices operates in the –40 to +105 °C temperature range from a 1.8 to 3.6 V power supply. The supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range and an inverted reset signal is applied to PDR_ON. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F437xx devices offers devices in 3 packages ranging from 100 pins to 176 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F437xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Figure 4 shows the general block diagram of the device family.

Table 2. STM32F437xx features and peripheral counts

Peripherals		STM32F437Vx		STM32F437Zx		STM32F437Ix	
Flash memory in Kbytes		1024	2048	1024	2048	1024	2048
SRAM in Kbytes	System	256(112+16+64+64)					
	Backup	4					
FSMC memory controller		Yes(1)					
Ethernet		Yes					
Timers	General-purpose	10					
	Advanced-control	2					
	Basic	2					
Random number generator		Yes					
Communication interfaces	SPI / I^2S	6/2 (full duplex)(2)					
	I^2C	3					
	USART/UART	4/4					
	USB OTG FS	Yes					
	USB OTG HS	Yes					
	CAN	2					
	SDIO	Yes					
Camera interface		Yes					
Cryptography		Yes					
GPIOs		82		114		140	
12-bit ADC Number of channels		3					
		16		24		24	
12-bit DAC Number of channels		Yes 2					
Maximum CPU frequency		168 MHz					
Operating voltage		1.8 to 3.6 V(3)					

Table 2. STM32F437xx features and peripheral counts (continued)

Peripherals	STM32F437Vx	STM32F437Zx	STM32F437Ix
Operating temperatures	Ambient temperatures: –40 to +85 °C /–40 to +105 °C		
	Junction temperature: –40 to + 125 °C		
Package	LQFP100	LQFP144	UFBGA176 LQFP176

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in the 0 to 70 °C temperature range and an inverted reset signal is applied to PDR_ON.

2.1 Full compatibility throughout the family

The STM32F437xx are part of the STM32F4 family. They are fully pin-to-pin, software and feature compatible with the STM32F2xx devices, allowing the user to try different memory densities, peripherals, and performances (FPU, higher frequency) for a greater degree of freedom during the development cycle.

The STM32F437xx devices maintain a close compatibility with the whole STM32F10xx family. All functional pins are pin-to-pin compatible. The STM32F437xx, however, are not drop-in replacements for the STM32F10xx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xx to the STM32F43x family remains simple as only a few pins are impacted.

Figure 1, *Figure 2*, and *Figure 3*, give compatible board designs between the STM32F4xx, STM32F2xx, and STM32F10xx families.

Figure 1. Compatible board design STM32F10xx/STM32F2xx/STM32F4xx for LQFP100 package

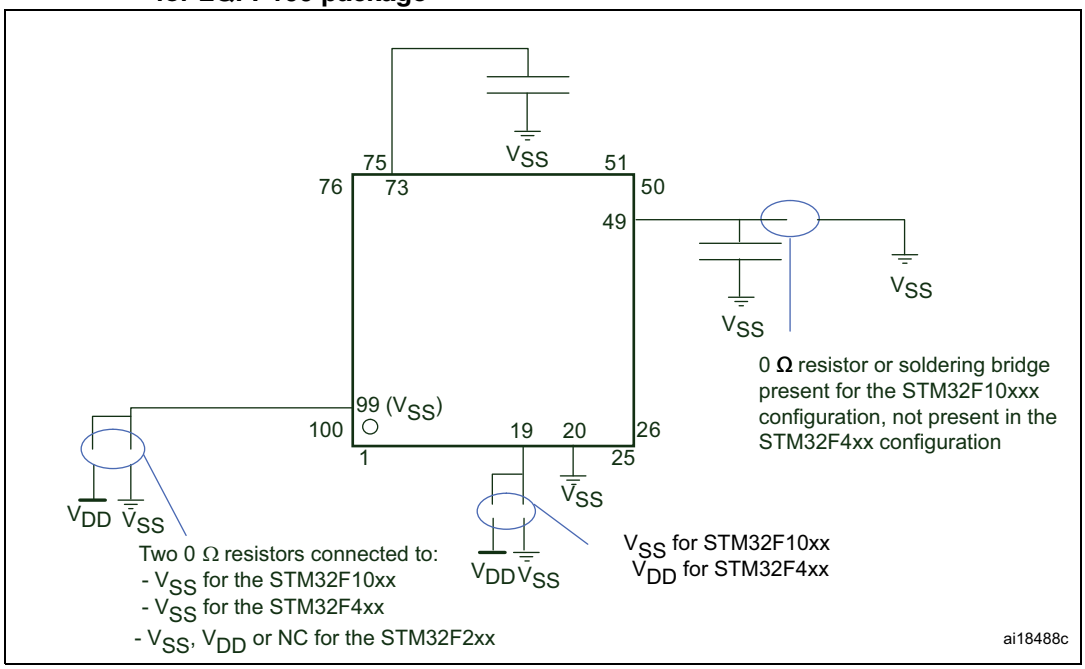


Figure 2. Compatible board design between STM32F10xx/STM32F2xx/STM32F4xx for LQFP144 package

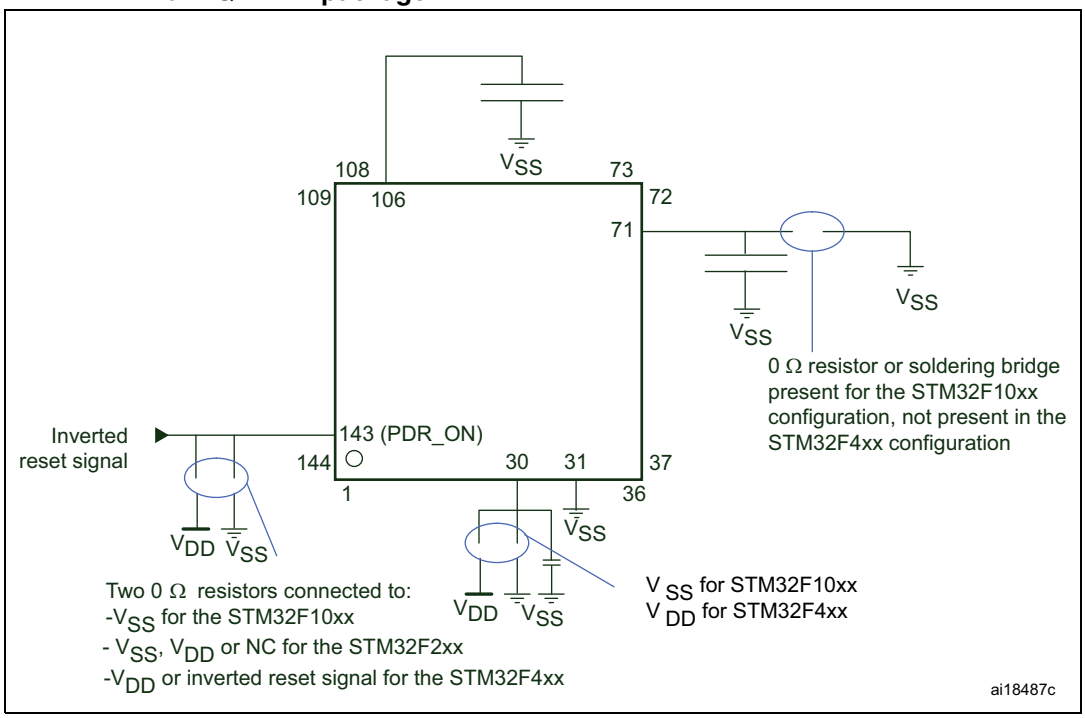


Figure 3. Compatible board design between STM32F2xx and STM32F4xx for LQFP176 package

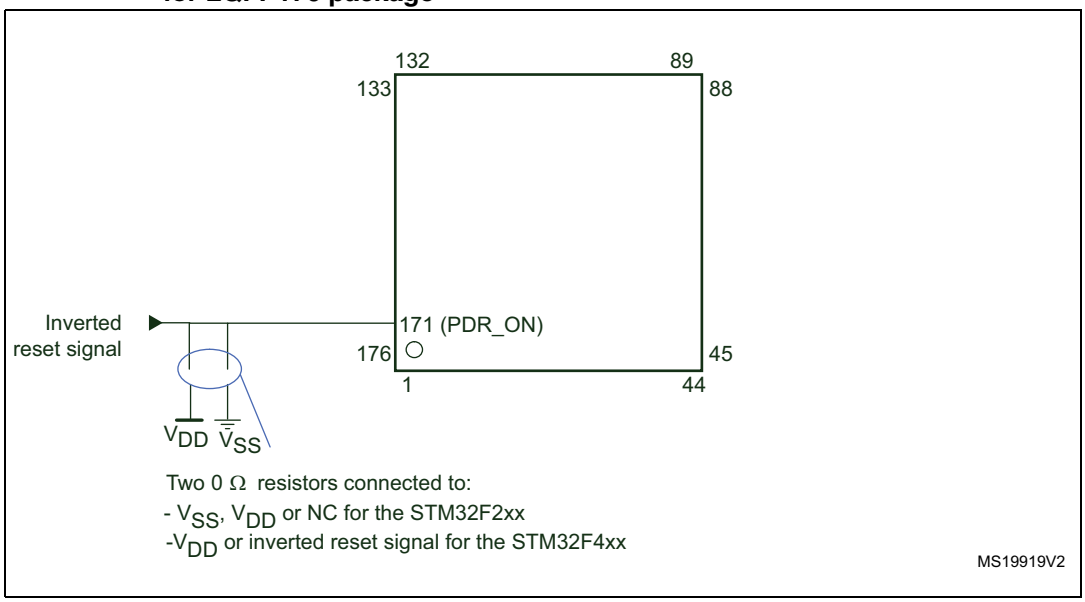
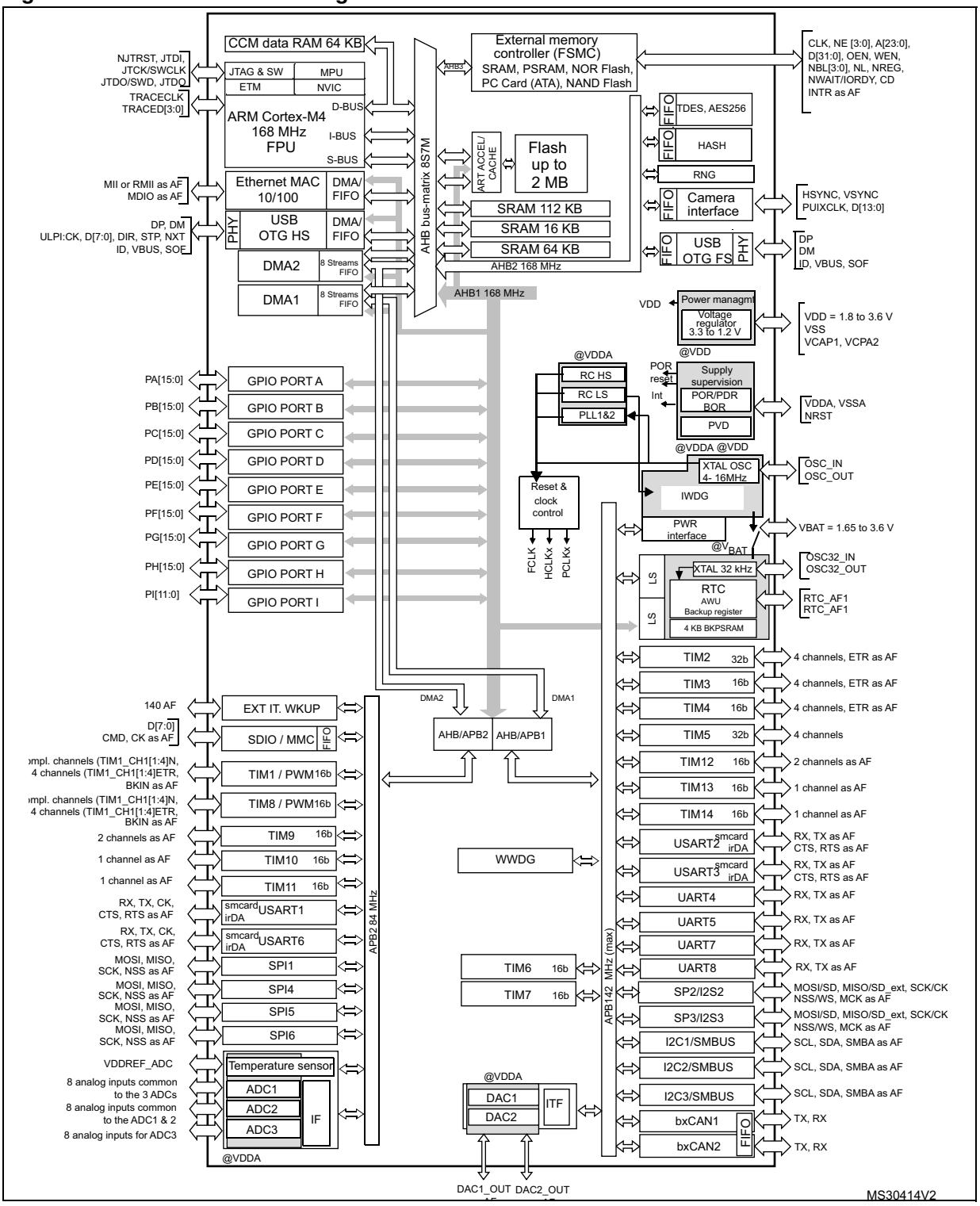


Figure 4. STM32F43x block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 168 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 84 MHz or 168 MHz.

3 Functional overview

3.1 ARM® Cortex™-M4F core with embedded Flash and SRAM

The ARM Cortex-M4F processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4F 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F43x family is compatible with all ARM tools and software.

Figure 4 shows the general block diagram of the STM32F43x family.

Note: Cortex-M4F is binary compatible with Cortex-M3.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex™-M4F processors. It balances the inherent performance advantage of the ARM Cortex-M4F over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 210 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 168 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

The devices embed a Flash memory of 1 Mbytes or 2 Mbytes available for storing programs and data.

3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6 Embedded SRAM

All devices embed:

- Up to 256 Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM

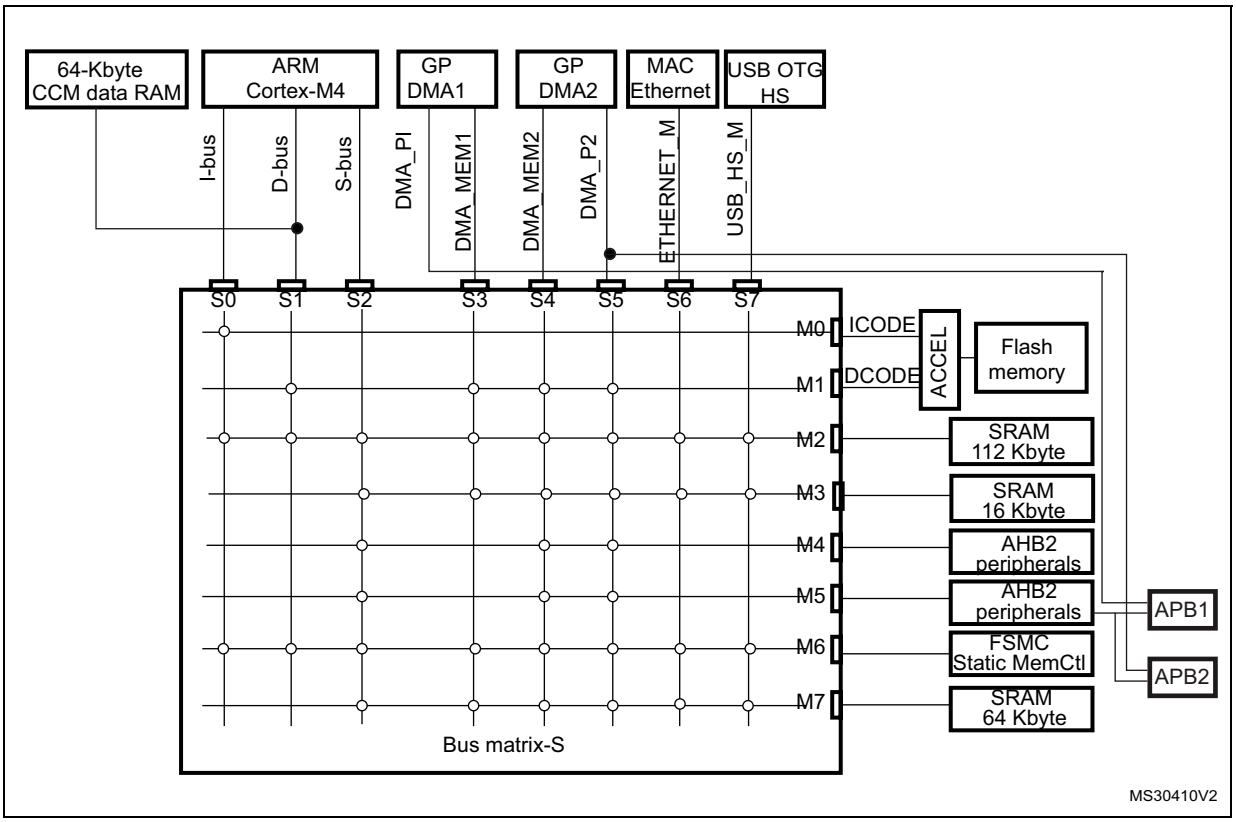
  RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM

  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

3.8 Multi-AHB matrix



3.9 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I^2S
- I^2C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Cryptographic acceleration
- Camera interface (DCMI)
- ADC.

3.10 Flexible static memory controller (FSMC)

All devices embed an FSMC. It has four Chip Select outputs supporting the following modes: PCCard/Compact Flash, SRAM, PSRAM, NOR Flash and NAND Flash.

Functionality overview:

- Write FIFO
- Maximum FSMC_CLK frequency for synchronous accesses is 60 MHz.

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.11 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 87 maskable interrupt channels plus the 16 interrupt lines of the Cortex™-M4F.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.12 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 140 GPIOs can be connected to the 16 external interrupt lines.

3.13 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 168 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 168 MHz while the maximum frequency of the high-speed APB domains is 84 MHz. The maximum allowed frequency of the low-speed APB domain is 42 MHz.

The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

3.14 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB13), USB OTG FS in Device mode (PA11/PA12) through DFU (device firmware upgrade).

3.15 Power supply schemes

- V_{DD} = 1.8 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.8 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in the 0 to 70 °C temperature range and an inverted reset signal is applied to PDR_ON.

3.16 Power supply supervisor

The power supply supervisor is enabled by holding PDR_ON high.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

All packages, except for the LQFP100, have an internal reset controlled through the PDR_ON signal.

3.17 Voltage regulator

The regulator has eight operating modes:

- Regulator ON/internal reset ON
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator ON/internal reset OFF
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator OFF/internal reset ON
- Regulator OFF/internal reset OFF

Regulator ON

- Regulator ON/internal reset ON

  On LQFP100 package, the regulator ON/internal reset ON mode is always enabled.

  On LQFP144 package, this mode is activated by setting PDR_ON to V_{DD}.

  On UFBGA176 and LQFP176 packages, the internal regulator must be activated by connecting BYPASS_REG to V_{SS} and by setting PDR_ON to V_{DD}.

  There are three low-power modes:

  – MR is used in the nominal regulation mode (Run)

  – LPR is used in the Stop modes

  – Power-down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

- Regulator ON/internal reset OFF

  On the LQFP100 package, this mode is not available.

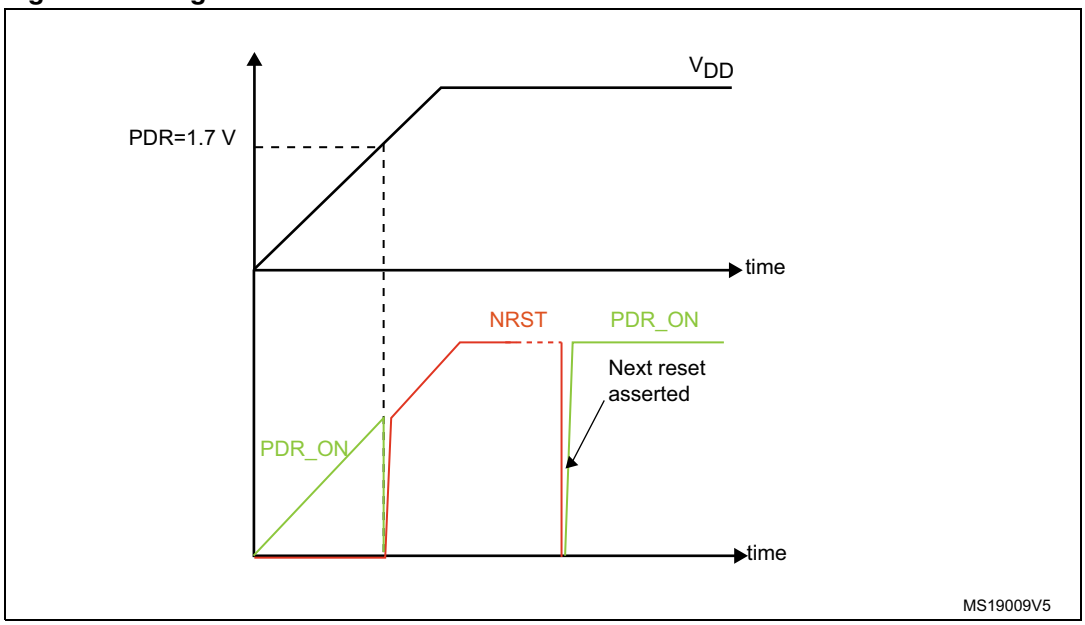
  On LQFP144 package, the internal reset is controlled by applying an inverted reset signal to PDR_ON pin.

  On UFBGA176 and LQFP176 packages, the internal regulator is activated by connecting BYPASS_REG to V_{SS}. The internal reset is controlled by applying an inverted reset signal to PDR_ON pin.

  V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in the 0 to 70 °C temperature range and an inverted reset signal is applied to PDR_ON.

  The NRST pin should be controlled by an external reset controller to keep the device under reset when V_{DD} is below 1.8 V (see *Figure 5*).

Figure 5. Regulator ON/internal reset OFF



Regulator OFF

This mode allows to power the device as soon as V_{DD} reaches 1.8 V.

- Regulator OFF/internal reset ON

  This mode is available only on UFBGA176 and LQFP176 packages. It is activated by setting BYPASS_REG and PDR_ON pins to V_{DD}.

  The regulator OFF/internal reset ON mode allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins, in addition to V_{DD}.

  The following conditions must be respected:

  – V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.

  – If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is faster than the time for V_{DD} to reach 1.8 V, then PA0 should be connected to the NRST pin (see *Figure 6*). Otherwise, PA0 should be asserted low externally during POR until V_{DD} reaches 1.8 V (see *Figure 7*).

  – If V_{CAP_1} and V_{CAP_2} go below 1.08 V and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

  In regulator OFF/internal reset ON mode, PA0 cannot be used as a GPIO pin since it allows to reset the part of the 1.2 V logic which is not reset by the NRST pin, when the internal voltage regulator in off.

- Regulator OFF/internal reset OFF

  This mode is available only on UFBGA176 and LQFP176 packages. It is activated by setting BYPASS_REG pin to V_{DD} and by applying an inverted reset signal to PDR_ON. It allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins, in addition to V_{DD}.

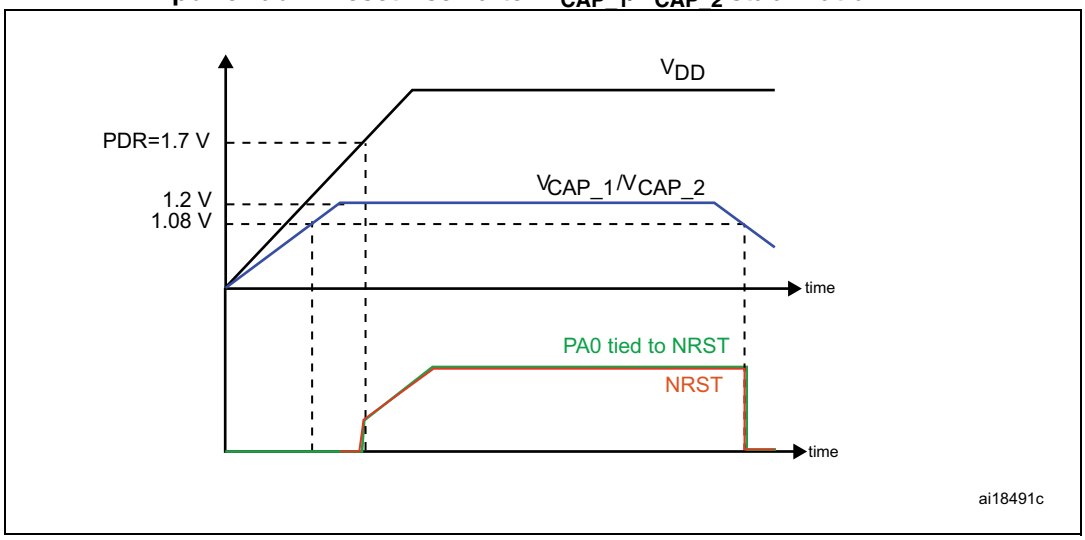
  The following conditions must be respected:

  – V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.

  – PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach 1.08 V and until V_{DD} reaches 1.8 V (see *Figure 6*).

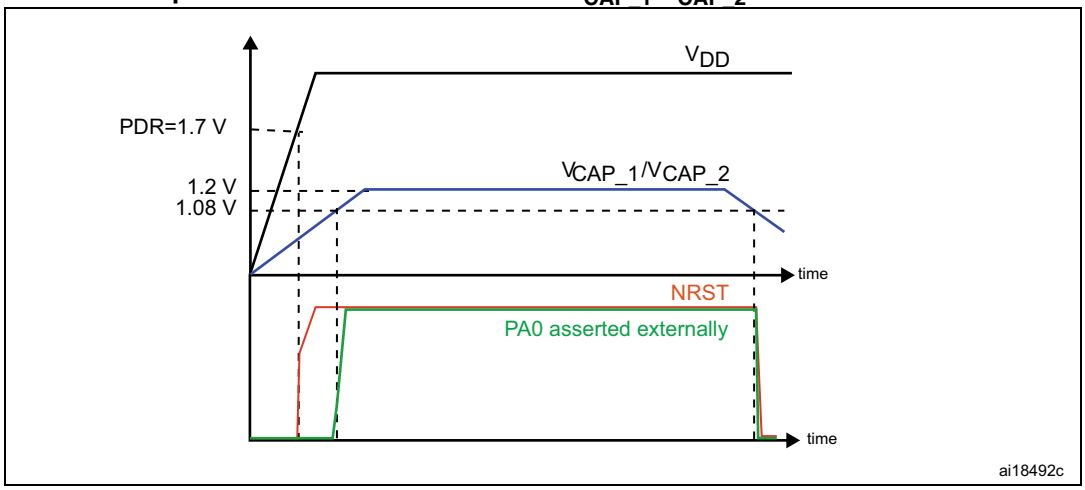
  – NRST should be controlled by an external reset controller to keep the device under reset when V_{DD} is below 1.8 V (see *Figure 7*).

Figure 6. Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid both whatever the internal reset mode (on or off).

Figure 7. Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid both whatever the internal reset mode (on or off).

3.18 Real-time clock (RTC), backup SRAM and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 4 Kbytes of backup SRAM
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC provides a programmable alarm and programmable

periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The 4-Kbyte backup SRAM is an EEPROM-like memory area. It can be used to store data which need to be retained in VBAT and standby mode. This memory area is disabled by default to minimize power consumption (see *Section 3.19: Low-power modes*). It can be enabled by software.

The backup registers are 32-bit registers used to store 80 bytes of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.19: Low-power modes*).

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

Like backup SRAM, the RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or from the V_{BAT} pin.

3.19 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm/ wakeup/ tamper/ time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup).

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering

Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm/ wakeup/ tamper/time stamp event occurs.

The standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

Note: When in Standby mode, only an RTC alarm/event or an external reset can wake up the device provided V_{DD} is supplied by an external battery.

3.20 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

3.21 Timers and watchdogs

The devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 3 compares the features of the advanced-control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz) (1)
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	84	168
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	42	84/168
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	42	84/168
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	84	168
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	84	168
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	42	84/168
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	42	84/168
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	42	84/168

1. The maximum timer clock is either 84 or 168 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

3.21.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

3.21.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F43x devices (see *Table 3* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F43x include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4.The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

3.21.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

3.21.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.21.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.21.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.22 Inter-integrated circuit interface (I²C)

Up to three I²C bus interfaces can operate in multimaster and slave modes. They can support the Standard- and Fast-modes. They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see *Table 4*).

Table 4. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Disabled when Wakeup from Stop mode is enabled

3.23 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and two universal asynchronous receiver transmitters (UART4, UART5, UART7, and UART8).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 10.5 Mbit/s. The other available interfaces communicate at up to 5.25 bit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 5. USART feature comparison

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	5.25	10.5	APB2 (max. 84 MHz)
USART2	X	X	X	X	X	X	2.62	5.25	APB1 (max. 42 MHz)
USART3	X	X	X	X	X	X	2.62	5.25	APB1 (max. 42 MHz)
UART4	X	-	X	-	X	-	2.62	5.25	APB1 (max. 42 MHz)
UART5	X	-	X	-	X	-	2.62	5.25	APB1 (max. 42 MHz)
USART6	X	X	X	X	X	X	5.25	10.5	APB2 (max. 84 MHz)
UART7	X	-	X	-	X	-	2.62	5.25	APB1 (max. 42 MHz)
UART8	X	-	X	-	X	-	2.62	5.25	APB1 (max. 42 MHz)

3.24 Serial peripheral interface (SPI)

The devices feature up to six SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, SPI5, and SPI6 can communicate at up to 42 Mbits/s, SPI2 and SPI3 can communicate at up to 21 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

3.25 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of

the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I^2Sx can be served by the DMA controller.

Note: For I2S2 full-duplex mode, I2S2_CK and I2S2_WS signals can be used only on GPIO Port B and GPIO Port D.

3.26 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S application. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I^2S sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I2S flow with an external PLL (or Codec output).

3.27 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 48 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

3.28 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F46x reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

3.29 Controller area network (bxCAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

3.30 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.31 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI)

for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1 Kbit × 35 with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.32 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbyte/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

3.33 Cryptographic acceleration

The devices embed a cryptographic accelerator. This cryptographic accelerator provides a set of hardware acceleration for the advanced cryptographic algorithms usually needed to

provide confidentiality, authentication, data integrity and non repudiation when exchanging messages with a peer.

- These algorithms consists of:

  Encryption/Decryption

  – DES/TDES (data encryption standard/triple data encryption standard): ECB (electronic codebook) and CBC (cipher block chaining) chaining algorithms, 64-, 128- or 192-bit key

  – AES (advanced encryption standard): ECB, CBC, GCM, CCM, and CTR (counter mode) chaining algorithms, 128, 192 or 256-bit key

  Universal hash

  – SHA-1 and SHA-2 (secure hash algorithms)

  – MD5

  – HMAC

The cryptographic accelerator supports DMA request generation.

3.34 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.35 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 84 MHz.

3.36 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

3.37 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.8 V and 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

3.38 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.39 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.40 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F43x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded

and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

4 Pinouts and pin description

Figure 8. STM32F43x LQFP100 pinout

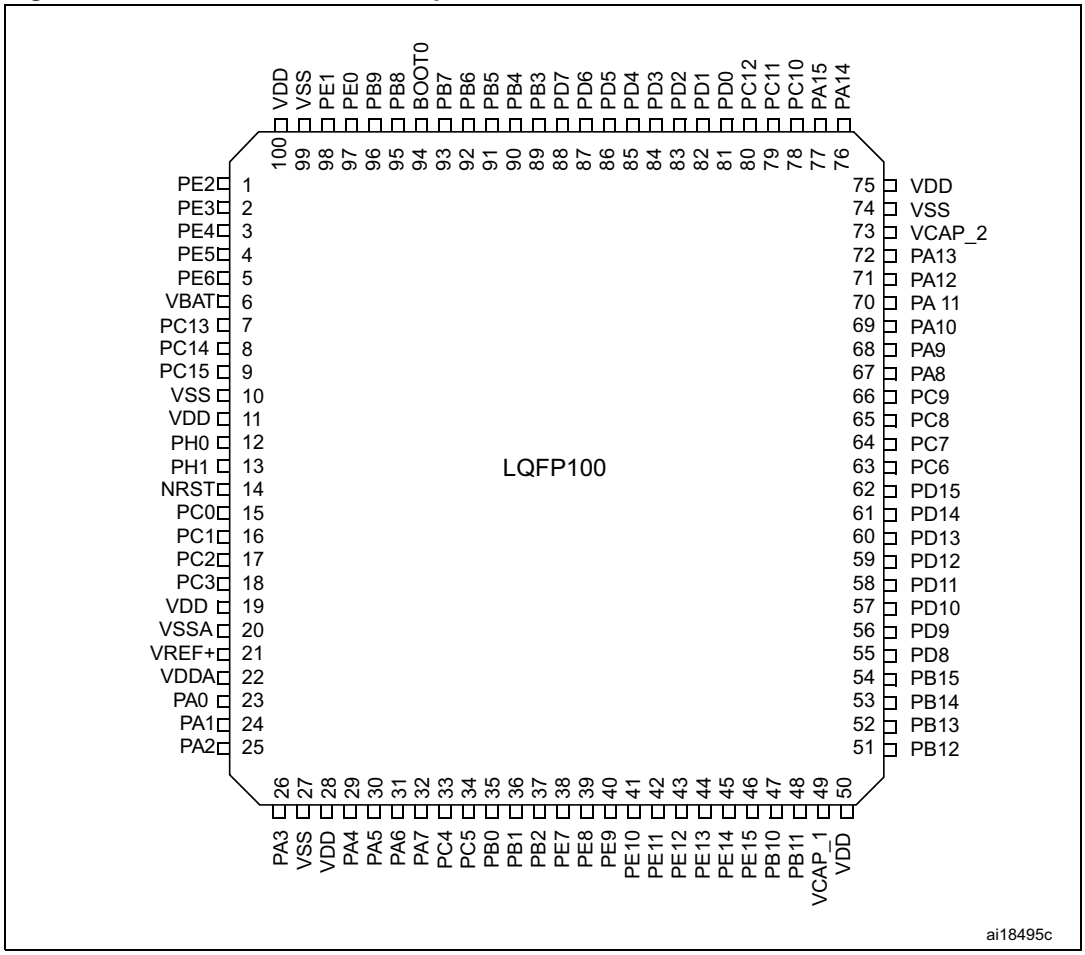


Figure 9. STM32F43x LQFP144 pinout

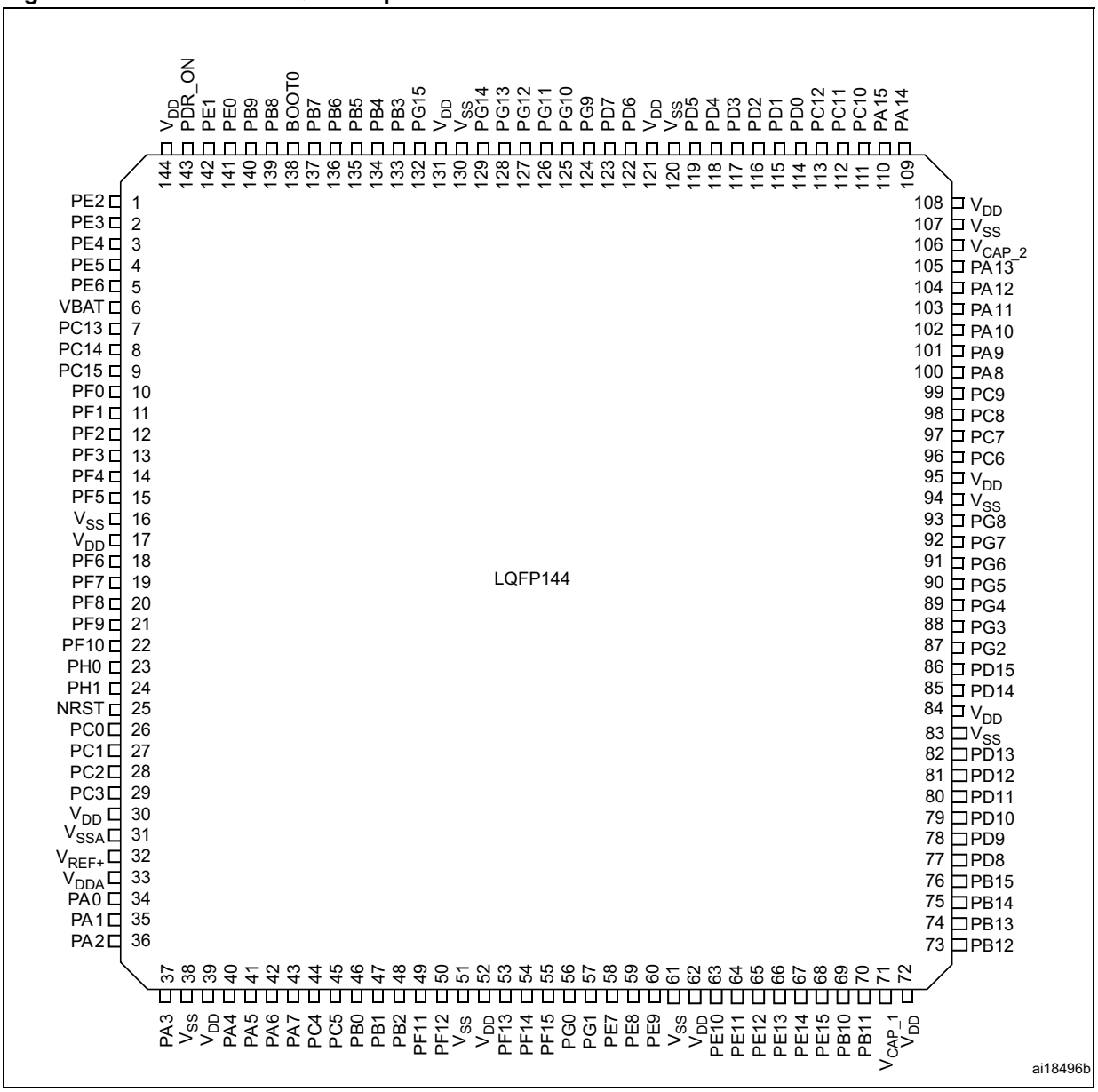


Figure 10. STM32F43x LQFP176 pinout

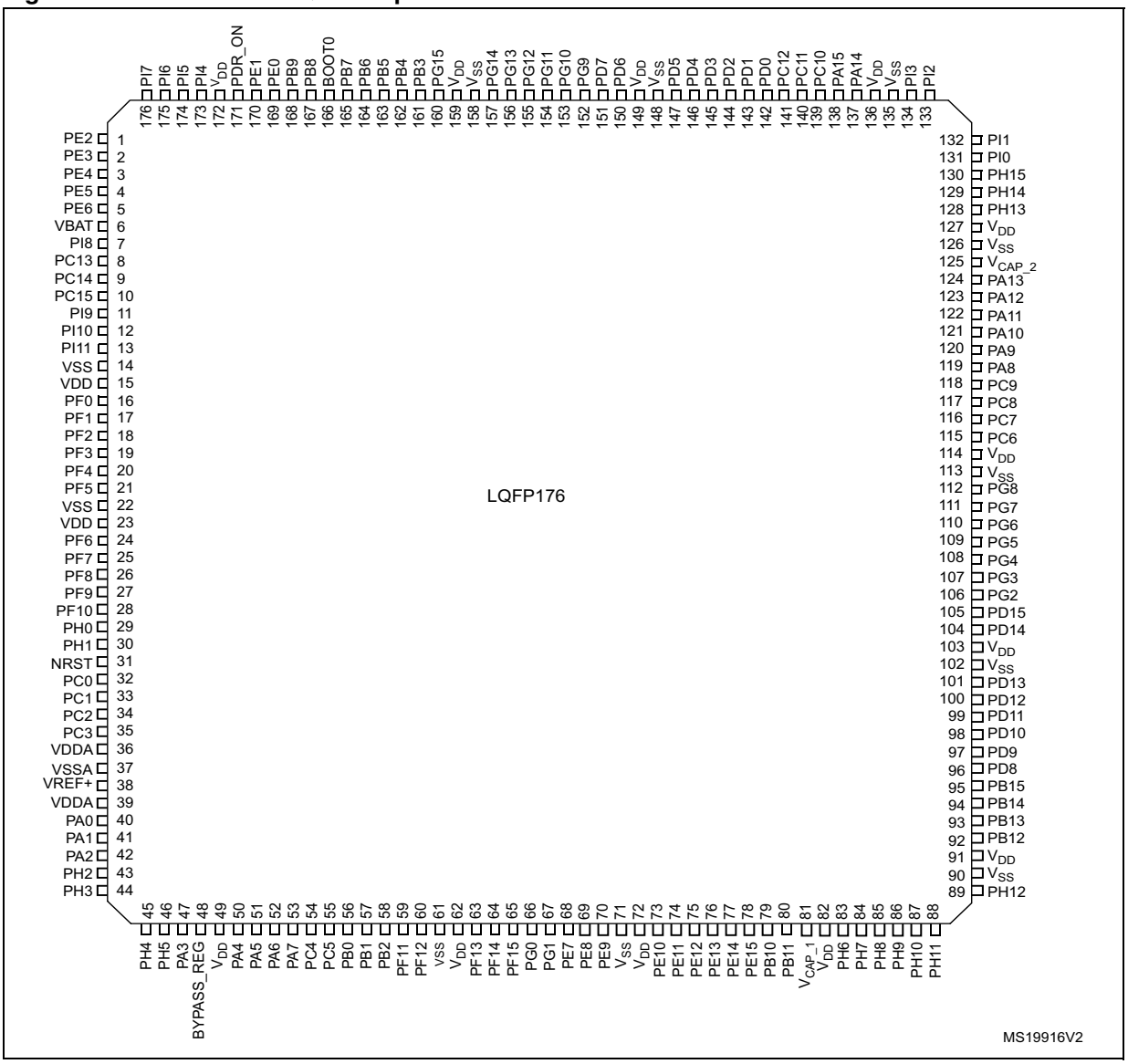
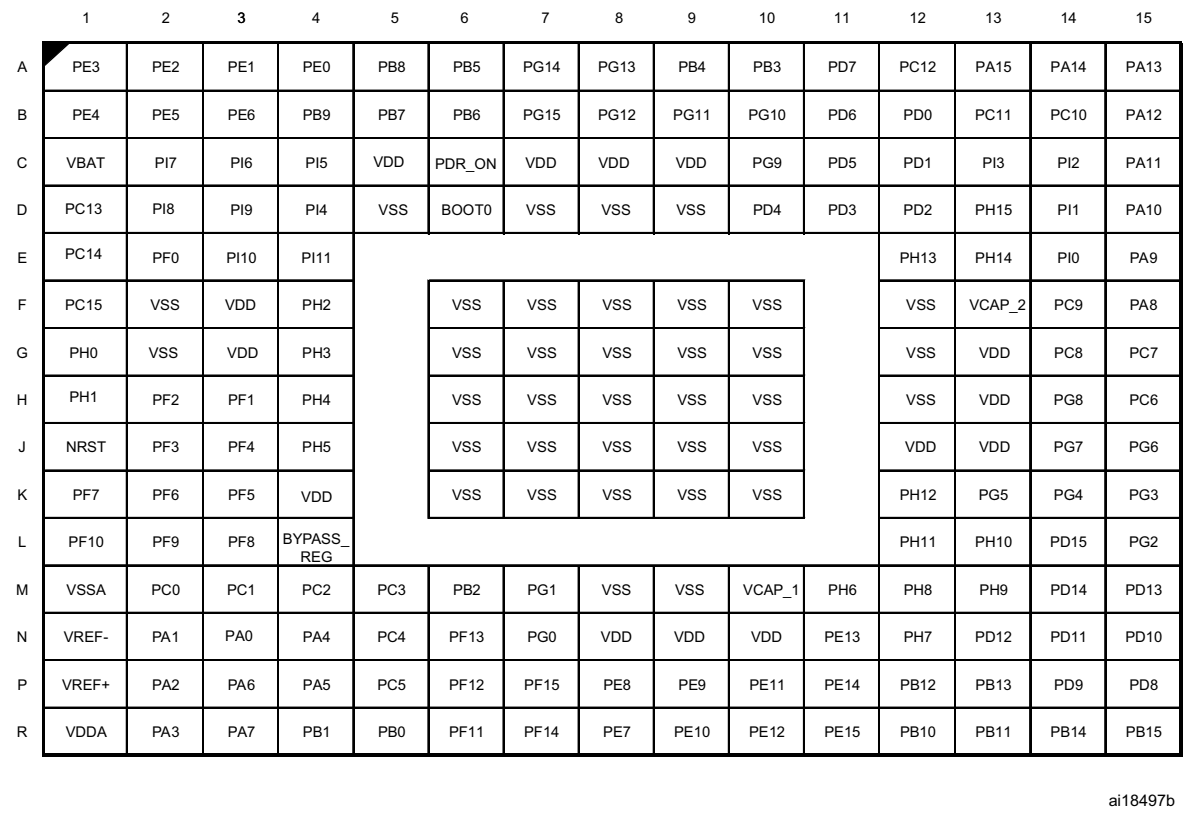


Figure 11. STM32F43x UFBGA176 ballout



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PE3	PE2	PE1	PE0	PB8	PB5	PG14	PG13	PB4	PB3	PD7	PC12	PA15	PA14	PA13
B	PE4	PE5	PE6	PB9	PB7	PB6	PG15	PG12	PG11	PG10	PD6	PD0	PC11	PC10	PA12
C	VBAT	PI7	PI6	PI5	VDD	PDR_ON	VDD	VDD	VDD	PG9	PD5	PD1	PI3	PI2	PA11
D	PC13	PI8	PI9	PI4	VSS	BOOT0	VSS	VSS	VSS	PD4	PD3	PD2	PH15	PI1	PA10
E	PC14	PF0	PI10	PI11								PH13	PH14	PI0	PA9
F	PC15	VSS	VDD	PH2		VSS	VSS	VSS	VSS	VSS		VSS	VCAP_2	PC9	PA8
G	PH0	VSS	VDD	PH3		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PC8	PC7
H	PH1	PF2	PF1	PH4		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PG8	PC6
J	NRST	PF3	PF4	PH5		VSS	VSS	VSS	VSS	VSS		VDD	VDD	PG7	PG6
K	PF7	PF6	PF5	VDD		VSS	VSS	VSS	VSS	VSS		PH12	PG5	PG4	PG3
L	PF10	PF9	PF8	BYPASS_REG								PH11	PH10	PD15	PG2
M	VSSA	PC0	PC1	PC2	PC3	PB2	PG1	VSS	VSS	VCAP_1	PH6	PH8	PH9	PD14	PD13
N	VREF-	PA1	PA0	PA4	PC4	PF13	PG0	VDD	VDD	VDD	PE13	PH7	PD12	PD11	PD10
P	VREF+	PA2	PA6	PA5	PC5	PF12	PF15	PE8	PE9	PE11	PE14	PB12	PB13	PD9	PD8
R	VDDA	PA3	PA7	PB1	PB0	PF11	PF14	PE7	PE10	PE12	PE15	PB10	PB11	PB14	PB15

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Table 6. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input/ output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 7. STM32F43x pin and ball definitions

Pin number				Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176	LQFP176						
1	1	A2	1	PE2	I/O	FT		TRACECLK, FSMC_A23, ETH_MII_TXD3, EVENTOUT, SPI4_SCK	
2	2	A1	2	PE3	I/O	FT		TRACED0, FSMC_A19, EVENTOUT, SPI4_NSS	
3	3	B1	3	PE4	I/O	FT		TRACED1, FSMC_A20, DCMI_D4, EVENTOUT, SPI4_NSS	
4	4	B2	4	PE5	I/O	FT		TRACED2, FSMC_A21, TIM9_CH1, DCMI_D6, EVENTOUT, SPI4_MISO	
5	5	B3	5	PE6	I/O	FT		TRACED3, FSMC_A22, TIM9_CH2, DCMI_D7, EVENTOUT, SPI4_MOSI	
6	6	C1	6	V_{BAT}	S				
-	-	D2	7	PI8	I/O	FT	(2)(3)	EVENTOUT	RTC_TAMP1, RTC_TAMP2, RTC_TS
7	7	D1	8	PC13	I/O	FT	(2)(3)	EVENTOUT	RTC_OUT, RTC_TAMP1, RTC_TS
8	8	E1	9	PC14/OSC32_IN (PC14)	I/O	FT	(2)(3)	EVENTOUT	OSC32_IN[4]
9	9	F1	10	PC15/OSC32_OUT (PC15)	I/O	FT	(2)(3)	EVENTOUT	OSC32_OUT[4]
-	-	D3	11	PI9	I/O	FT		CAN1_RX, EVENTOUT	
-	-	E3	12	PI10	I/O	FT		ETH_MII_RX_ER, EVENTOUT	
-	-	E4	13	PI11	I/O	FT		OTG_HS_ULPI_DIR, EVENTOUT	
-	-	F2	14	V_{SS}	S				
-	-	F3	15	V_{DD}	S				
-	10	E2	16	PF0	I/O	FT		FSMC_A0, I2C2_SDA, EVENTOUT	
-	11	H3	17	PF1	I/O	FT		FSMC_A1, I2C2_SCL, EVENTOUT	
-	12	H2	18	PF2	I/O	FT		FSMC_A2, I2C2_SMBA, EVENTOUT	
-	13	J2	19	PF3	I/O	FT	(4)	FSMC_A3, EVENTOUT	ADC3_IN9
-	14	J3	20	PF4	I/O	FT	(4)	FSMC_A4, EVENTOUT	ADC3_IN14

Table 7. STM32F43x pin and ball definitions (continued)

Pin number				Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176	LQFP176						
-	15	K3	21	PF5	I/O	FT	(4)	FSMC_A5, EVENTOUT	ADC3_IN15
10	16	G2	22	V_{SS}	S				
11	17	G3	23	V_{DD}	S				
-	18	K2	24	PF6	I/O	FT	(4)	TIM10_CH1, FSMC_NIORD, EVENTOUT, SPI5_NSS, UART7_Rx	ADC3_IN4
-	19	K1	25	PF7	I/O	FT	(4)	TIM11_CH1, FSMC_NREG, EVENTOUT, SPI5_SCK, UART7_Tx	ADC3_IN5
-	20	L3	26	PF8	I/O	FT	(4)	TIM13_CH1, FSMC_NIOWR, EVENTOUT, SPI5_MISO	ADC3_IN6
-	21	L2	27	PF9	I/O	FT	(4)	TIM14_CH1, FSMC_CD, EVENTOUT, SPI5_MOSI	ADC3_IN7
-	22	L1	28	PF10	I/O	FT	(4)	FSMC_INTR, EVENTOUT, DCMI_D11	ADC3_IN8
12	23	G1	29	PH0/OSC_IN (PH0)	I/O	FT		EVENTOUT	OSC_IN(4)
13	24	H1	30	PH1/OSC_OUT (PH1)	I/O	FT		EVENTOUT	OSC_OUT(4)
14	25	J1	31	NRST	I/O	RST			
15	26	M2	32	PC0	I/O	FT	(4)	OTG_HS_ULPI_STP, EVENTOUT	ADC123_IN10
16	27	M3	33	PC1	I/O	FT	(4)	ETH_MDC, EVENTOUT	ADC123_IN11
17	28	M4	34	PC2	I/O	FT	(4)	SPI2_MISO, OTG_HS_ULPI_DIR, TH_MII_TXD2, I2S2ext_SD, EVENTOUT	ADC123_IN12
18	29	M5	35	PC3	I/O	FT	(4)	SPI2_MOSI/I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, EVENTOUT	ADC123_IN13
19	30	G3	36	V_{DD}	S				
20	31	M1	37	V_{SSA}	S				
-	-	N1	-	V_{REF-}	S				
21	32	P1	38	V_{REF+}	S				
22	33	R1	39	V_{DDA}	S				

Table 7. STM32F43x pin and ball definitions (continued)

Pin number				Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176	LQFP176						
23	34	N3	40	PA0/WKUP (PA0)	I/O	FT	(5)	USART2_CTS, UART4_TX, ETH_MII_CRS, TIM2_CH1_ETR, TIM5_CH1, TIM8_ETR, EVENTOUT	ADC123_IN0, WKUP[4]
24	35	N2	41	PA1	I/O	FT	(4)	USART2_RTS, UART4_RX, ETH_RMII_REF_CLK, ETH_MII_RX_CLK, TIM5_CH2, TIMM2_CH2, EVENTOUT	ADC123_IN1
25	36	P2	42	PA2	I/O	FT	(4)	USART2_TX, TIM5_CH3, TIM9_CH1, TIM2_CH3, ETH_MDIO, EVENTOUT	ADC123_IN2
-	-	F4	43	PH2	I/O	FT		ETH_MII_CRS, EVENTOUT	
-	-	G4	44	PH3	I/O	FT		ETH_MII_COL, EVENTOUT	
-	-	H4	45	PH4	I/O	FT		I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT	
-	-	J4	46	PH5	I/O	FT		I2C2_SDA, EVENTOUT, SPI5_NSS	
26	37	R2	47	PA3	I/O	FT	(4)	USART2_RX, TIM5_CH4, TIM9_CH2, TIM2_CH4, OTG_HS_ULPI_D0, ETH_MII_COL, EVENTOUT	ADC123_IN3
27	38	-	-	V_{SS}	S				
		L4	48	BYPASS_REG	I	FT			
28	39	K4	49	V_{DD}	S				
29	40	N4	50	PA4	I/O	TTa	(4)	SPI1_NSS, SPI3_NSS, USART2_CK, DCMI_HSYNC, OTG_HS_SOF, I2S3_WS, EVENTOUT	ADC12_IN4, DAC1_OUT
30	41	P4	51	PA5	I/O	TTa	(4)	SPI1_SCK, OTG_HS_ULPI_CK, TIM2_CH1_ETR, TIM8_CHIN, EVENTOUT	ADC12_IN5, DAC2_OUT
31	42	P3	52	PA6	I/O	FT	(4)	SPI1_MISO, TIM8_BKIN, TIM13_CH1, DCMI_PIXCLK, TIM3_CH1, TIM1_BKIN, EVENTOUT	ADC12_IN6

Table 7. STM32F43x pin and ball definitions (continued)

Pin number				Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176	LQFP176						
32	43	R3	53	PA7	I/O	FT	(4)	SPI1_MOSI, TIM8_CH1N, TIM14_CH1, TIM3_CH2, ETH_MII_RX_DV, TIM1_CH1N, RMII_CRS_DV, EVENTOUT	ADC12_IN7
33	44	N5	54	PC4	I/O	FT	(4)	ETH_RMII_RX_D0, ETH_MII_RX_D0, EVENTOUT	ADC12_IN14
34	45	P5	55	PC5	I/O	FT	(4)	ETH_RMII_RX_D1, ETH_MII_RX_D1, EVENTOUT	ADC12_IN15
35	46	R5	56	PB0	I/O	FT	(4)	TIM3_CH3, TIM8_CH2N, OTG_HS_ULPI_D1, ETH_MII_RXD2, TIM1_CH2N, EVENTOUT	ADC12_IN8
36	47	R4	57	PB1	I/O	FT	(4)	TIM3_CH4, TIM8_CH3N, OTG_HS_ULPI_D2, ETH_MII_RXD3, TIM1_CH3N, EVENTOUT	ADC12_IN9
37	48	M6	58	PB2/BOOT1 (PB2)	I/O	FT		EVENTOUT	
-	49	R6	59	PF11	I/O	FT		DCMI_12, EVENTOUT, SPI5_MOSI	
-	50	P6	60	PF12	I/O	FT		FSMC_A6, EVENTOUT	
-	51	M8	61	V_{SS}	S				
-	52	N8	62	V_{DD}	S				
-	53	N6	63	PF13	I/O	FT		FSMC_A7, EVENTOUT	
-	54	R7	64	PF14	I/O	FT		FSMC_A8, EVENTOUT	
-	55	P7	65	PF15	I/O	FT		FSMC_A9, EVENTOUT	
-	56	N7	66	PG0	I/O	FT		FSMC_A10, EVENTOUT	
-	57	M7	67	PG1	I/O	FT		FSMC_A11, EVENTOUT	
38	58	R8	68	PE7	I/O	FT		FSMC_D4, TIM1_ETR, EVENTOUT, UART7_RX	
39	59	P8	69	PE8	I/O	FT		FSMC_D5, TIM1_CH1N, EVENTOUT, UART7_TX	
40	60	P9	70	PE9	I/O	FT		FSMC_D6, TIM1_CH1, EVENTOUT	
-	61	M9	71	V_{SS}	S				
-	62	N9	72	V_{DD}	S				

Table 7. STM32F43x pin and ball definitions (continued)

Pin number				Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176	LQFP176						
41	63	R9	73	PE10	I/O	FT		FSMC_D7, TIM1_CH2N, EVENTOUT	
42	64	P10	74	PE11	I/O	FT		FSMC_D8, TIM1_CH2, EVENTOUT, SPI4_NSS	
43	65	R10	75	PE12	I/O	FT		FSMC_D9, TIM1_CH3N, EVENTOUT, SPI4_SCK	
44	66	N11	76	PE13	I/O	FT		FSMC_D10, TIM1_CH3, EVENTOUT, SPI4_MISO	
45	67	P11	77	PE14	I/O	FT		FSMC_D11, TIM1_CH4, EVENTOUT, SPI4_MOSI	
46	68	R11	78	PE15	I/O	FT		FSMC_D12, TIM1_BKIN, EVENTOUT	
47	69	R12	79	PB10	I/O	FT		SPI2_SCK/I2S2_CK, I2C2_SCL, USART3_TX, OTG_HS_ULPI_D3, ETH_MII_RX_ER, TIM2_CH3, EVENTOUT	
48	70	R13	80	PB11	I/O	FT		I2C2_SDA, USART3_RX, OTG_HS_ULPI_D4, ETH_RMII_TX_EN, ETH_MII_TX_EN, TIM2_CH4, EVENTOUT	
49	71	M10	81	V_{CAP_1}	S				
50	72	N10	82	V_{DD}	S				
-	-	M11	83	PH6	I/O	FT		I2C2_SMBA, TIM12_CH1, ETH_MII_RXD2, EVENTOUT, SPI5_SCK, DCMI_D8	
-	-	N12	84	PH7	I/O	FT		I2C3_SCL, ETH_MII_RXD3, EVENTOUT, SPI5_MISO, DCMI_D9	
-	-	M12	85	PH8	I/O	FT		I2C3_SDA, DCMI_HSYNC, EVENTOUT	
-	-	M13	86	PH9	I/O	FT		I2C3_SMBA, TIM12_CH2, DCMI_D0, EVENTOUT	
-	-	L13	87	PH10	I/O	FT		TIM5_CH1, DCMI_D1, EVENTOUT	
-	-	L12	88	PH11	I/O	FT		TIM5_CH2, DCMI_D2, EVENTOUT	

Table 7. STM32F43x pin and ball definitions (continued)

Pin number				Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176	LQFP176						
-	-	K12	89	PH12	I/O	FT		TIM5_CH3, DCMI_D3, EVENTOUT	
-	-	H12	90	V_{SS}	S				
-	-	J12	91	V_{DD}	S				
51	73	P12	92	PB12	I/O	FT		SPI2_NSS/I2S2_WS, I2C2_SMBA, USART3_CK, TIM1_BKIN, CAN2_RX, OTG_HS_ULPI_D5, ETH_RMII_TXD0, ETH_MII_TXD0, OTG_HS_ID, EVENTOUT	
52	74	P13	93	PB13	I/O	FT		SPI2_SCK,/I2S2_CK, USART3_CTS, TIM1_CH1N, CAN2_TX, OTG_HS_ULPI_D6, ETH_RMII_TXD1, ETH_MII_TXD1, EVENTOUT	OTG_HS_VBUS
53	75	R14	94	PB14	I/O	FT		SPI2_MISO, TIM1_CH2N, TIM12_CH1, OTG_HS_DM, USART3_RTS, TIM8_CH2N, I2S2ext_SD, EVENTOUT	
54	76	R15	95	PB15	I/O	FT		SPI2_MOSI/I2S2_SD, TIM1_CH3N, TIM8_CH3N, TIM12_CH2, OTG_HS_DP, EVENTOUT, RTC_REFIN	
55	77	P15	96	PD8	I/O	FT		FSMC_D13, USART3_TX, EVENTOUT	
56	78	P14	97	PD9	I/O	FT		FSMC_D14, USART3_RX, EVENTOUT	
57	79	N15	98	PD10	I/O	FT		FSMC_D15, USART3_CK, EVENTOUT	
58	80	N14	99	PD11	I/O	FT		FSMC_CLE, FSMC_A16, USART3_CTS, EVENTOUT	
59	81	N13	100	PD12	I/O	FT		FSMC_ALE, FSMC_A17, TIM4_CH1, USART3_RTS, EVENTOUT	
60	82	M15	101	PD13	I/O	FT		FSMC_A18, TIM4_CH2, EVENTOUT	
-	83	-	102	V_{SS}	S				

Table 7. STM32F43x pin and ball definitions (continued)

Pin number				Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176	LQFP176						
-	84	J13	103	V_{DD}	S				
61	85	M14	104	PD14	I/O	FT		FSMC_D0, TIM4_CH3, EVENTOUT	
62	86	L14	105	PD15	I/O	FT		FSMC_D1, TIM4_CH4, EVENTOUT	
-	87	L15	106	PG2	I/O	FT		FSMC_A12, EVENTOUT	
-	88	K15	107	PG3	I/O	FT		FSMC_A13, EVENTOUT	
-	89	K14	108	PG4	I/O	FT		FSMC_A14, EVENTOUT	
-	90	K13	109	PG5	I/O	FT		FSMC_A15, EVENTOUT	
-	91	J15	110	PG6	I/O	FT		FSMC_INT2, EVENTOUT, DCMI_D12	
-	92	J14	111	PG7	I/O	FT		FSMC_INT3, USART6_CK, EVENTOUT, DCMI_D13	
-	93	H14	112	PG8	I/O	FT		USART6_RTS, ETH_PPS_OUT, EVENTOUT, SPI6_NSS	
-	94	G12	113	V_{SS}	S				
-	95	H13	114	V_{DD}	S				
63	96	H15	115	PC6	I/O	FT		I2S2_MCK, TIM8_CH1, SDIO_D6, USART6_TX, DCMI_D0, TIM3_CH1, EVENTOUT	
64	97	G15	116	PC7	I/O	FT		I2S3_MCK, TIM8_CH2, SDIO_D7, USART6_RX, DCMI_D1, TIM3_CH2, EVENTOUT	
65	98	G14	117	PC8	I/O	FT		TIM8_CH3, SDIO_D0, TIM3_CH3, USART6_CK, DCMI_D2, EVENTOUT	
66	99	F14	118	PC9	I/O	FT		I2S_CKIN, MCO2, TIM8_CH4, SDIO_D1, I2C3_SDA, DCMI_D3, TIM3_CH4, EVENTOUT	
67	100	F15	119	PA8	I/O	FT		MCO1, USART1_CK, TIM1_CH1, I2C3_SCL, OTG_FS_SOF, EVENTOUT	
68	101	E15	120	PA9	I/O	FT		USART1_TX, TIM1_CH2, I2C3_SMBA, DCMI_D0, EVENTOUT	OTG_FS_VBUS

Table 7. STM32F43x pin and ball definitions (continued)

Pin number				Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176	LQFP176						
69	102	D15	121	PA10	I/O	FT		USART1_RX, TIM1_CH3, OTG_FS_ID, DCMI_D1, EVENTOUT	
70	103	C15	122	PA11	I/O	FT		USART1_CTS, CAN1_RX, TIM1_CH4, OTG_FS_DM, EVENTOUT	
71	104	B15	123	PA12	I/O	FT		USART1_RTS, CAN1_TX, TIM1_ETR, OTG_FS_DP, EVENTOUT	
72	105	A15	124	PA13 (JTMS-SWDIO)	I/O	FT		JTMS-SWDIO, EVENTOUT	
73	106	F13	125	V_{CAP_2}	S				
74	107	F12	126	V_{SS}	S				
75	108	G13	127	V_{DD}	S				
-	-	E12	128	PH13	I/O	FT		TIM8_CH1N, CAN1_TX, EVENTOUT	
-	-	E13	129	PH14	I/O	FT		TIM8_CH2N, DCMI_D4, EVENTOUT	
-	-	D13	130	PH15	I/O	FT		TIM8_CH3N, DCMI_D11, EVENTOUT	
-	-	E14	131	PI0(6)	I/O	FT		TIM5_CH4, SPI2_NSS, I2S2_WS, DCMI_D13, EVENTOUT	
-	-	D14	132	PI1(6)	I/O	FT		SPI2_SCK, I2S2_CK, DCMI_D8, EVENTOUT	
-	-	C14	133	PI2	I/O	FT		TIM8_CH4, SPI2_MISO, DCMI_D9, I2S2ext_SD, EVENTOUT	
-	-	C13	134	PI3	I/O	FT		TIM8_ETR, SPI2_MOSI, I2S2_SD, DCMI_D10, EVENTOUT	
-	-	D9	135	V_{SS}	S				
-	-	C9	136	V_{DD}	S				
76	109	A14	137	PA14 (JTCK-SWCLK)	I/O	FT		JTCK-SWCLK, EVENTOUT	
77	110	A13	138	PA15 (JTDI)	I/O	FT		JTDI, SPI3_NSS, I2S3_WS, TIM2_CH1_ETR, SPI1_NSS, EVENTOUT	

Table 7. STM32F43x pin and ball definitions (continued)

Pin number				Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176	LQFP176						
78	111	B14	139	PC10	I/O	FT		SPI3_SCK/I2S3_CK, UART4_TX, SDIO_D2, DCMI_D8, USART3_TX, EVENTOUT	
79	112	B13	140	PC11	I/O	FT		UART4_RX, SPI3_MISO, SDIO_D3, DCMI_D4, USART3_RX, I2S3ext_SD, EVENTOUT	
80	113	A12	141	PC12	I/O	FT		UART5_TX, SDIO_CK, DCMI_D9, SPI3_MOSI, I2S3_SD, USART3_CK, EVENTOUT	
81	114	B12	142	PD0	I/O	FT		FSMC_D2, CAN1_RX, EVENTOUT	
82	115	C12	143	PD1	I/O	FT		FSMC_D3, CAN1_TX, EVENTOUT	
83	116	D12	144	PD2	I/O	FT		TIM3_ETR, UART5_RX, SDIO_CMD, DCMI_D11, EVENTOUT	
84	117	D11	145	PD3	I/O	FT		FSMC_CLK, USART2_CTS, EVENTOUT, SPI2_SCK, I2S2_CK, DCMI_D5	
85	118	D10	146	PD4	I/O	FT		FSMC_NOE, USART2_RTS, EVENTOUT	
86	119	C11	147	PD5	I/O	FT		FSMC_NWE, USART2_TX, EVENTOUT	
-	120	D8	148	V_{SS}	S				
-	121	C8	149	V_{DD}	S				
87	122	B11	150	PD6	I/O	FT		FSMC_NWAIT, USART2_RX, EVENTOUT, SPI3_MOSI, I2S3_MOSI, DCMI_D10	
88	123	A11	151	PD7	I/O	FT		USART2_CK, FSMC_NE1, FSMC_NCE2, EVENTOUT	
-	124	C10	152	PG9	I/O	FT		USART6_RX, FSMC_NE2, FSMC_NCE3, EVENTOUT	
-	125	B10	153	PG10	I/O	FT		FSMC_NCE4_1, FSMC_NE3, EVENTOUT, DCMI_D2	

Table 7. STM32F43x pin and ball definitions (continued)

Pin number				Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176	LQFP176						
-	126	B9	154	PG11	I/O	FT		FSMC_NCE4_2, ETH_MII_TX_EN, ETH _RMII_TX_EN, EVENTOUT, DCMI_D3	
-	127	B8	155	PG12	I/O	FT		FSMC_NE4, USART6_RTS, EVENTOUT, SPI6_MISO	
-	128	A8	156	PG13	I/O	FT		FSMC_A24, USART6_CTS , ETH_MII_TXD0, ETH_RMII_TXD0, EVENTOUT, SPI6_SCK	
-	129	A7	157	PG14	I/O	FT		FSMC_A25, USART6_TX, ETH_MII_TXD1, ETH_RMII_TXD1, EVENTOUT, SPI6_MOSI	
-	130	D7	158	V_{SS}	S				
-	131	C7	159	V_{DD}	S				
-	132	B7	160	PG15	I/O	FT		USART6_CTS, DCMI_D13, EVENTOUT	
89	133	A10	161	PB3 (JTDO/ TRACESWO)	I/O	FT		JTDO/TRACESWO, SPI3_SCK/I2S3_CK, TIM2_CH2, SPI1_SCK, EVENTOUT	
90	134	A9	162	PB4 (NJTRST)	I/O	FT		NJTRST, SPI3_MISO, TIM3_CH1, SPI1_MISO, I2S3ext_SD, EVENTOUT	
91	135	A6	163	PB5	I/O	FT		I2C1_SMBA, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, TIM3_CH2, SPI1_MOSI, SPI3_MOSI, DCMI_D10, I2S3_SD, EVENTOUT	
92	136	B6	164	PB6	I/O	FT		I2C1_SCL, TIM4_CH1, CAN2_TX, DCMI_D5, USART1_TX, EVENTOUT	
93	137	B5	165	PB7	I/O	FT		I2C1_SDA, FSMC_NL, DCMI_VSYNC, USART1_RX, TIM4_CH2, EVENTOUT	
94	138	D6	166	BOOT0	I	B			V_{PP}

Table 7. STM32F43x pin and ball definitions (continued)

Pin number				Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176	LQFP176						
95	139	A5	167	PB8	I/O	FT		TIM4_CH3, SDIO_D4, TIM10_CH1, DCMI_D6, ETH_MII_TXD3, I2C1_SCL, CAN1_RX, EVENTOUT	
96	140	B4	168	PB9	I/O	FT		SPI2_NSS/I2S2_WS, TIM4_CH4, TIM11_CH1, SDIO_D5, DCMI_D7, I2C1_SDA, CAN1_TX, EVENTOUT	
97	141	A4	169	PE0	I/O	FT		TIM4_ETR, FSMC_NBL0, DCMI_D2, EVENTOUT, UART8_Rx	
98	142	A3	170	PE1	I/O	FT		FSMC_NBL1, DCMI_D3, EVENTOUT, UART8_Tx	
99	-	D5	-	V_{SS}	S				
-	143	C6	171	PDR_ON	I	FT			
100	144	C5	172	V_{DD}	S				
-	-	D4	173	PI4	I/O	FT		TIM8_BKIN, DCMI_D5, EVENTOUT	
-	-	C4	174	PI5	I/O	FT		TIM8_CH1, DCMI_VSYNC, EVENTOUT	
-	-	C3	175	PI6	I/O	FT		TIM8_CH2, DCMI_D6, EVENTOUT	
-	-	C2	176	PI7	I/O	FT		TIM8_CH3, DCMI_D7, EVENTOUT	

1. Function availability depends on the chosen device.
2. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F4xx reference manual, available from the STMicroelectronics website: www.st.com.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
5. If the device is delivered in an UFBGA176 or LQFP176 package and the BYPASS_REG pin is set to VDD (Regulator off/internal reset ON mode), then PA0 is used as an internal Reset (active low).
6. PI0 and PI1 cannot be used in I2S2 full-duplex mode.

Table 8. FSMC pin definition

Pins(1)	FSMC				LQFP100(2)
	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE2		A23	A23		Yes
PE3		A19	A19		Yes
PE4		A20	A20		Yes
PE5		A21	A21		Yes
PE6		A22	A22		Yes
PF0	A0	A0			-
PF1	A1	A1			-
PF2	A2	A2			-
PF3	A3	A3			-
PF4	A4	A4			-
PF5	A5	A5			-
PF6	NIORD				-
PF7	NREG				-
PF8	NIOWR				-
PF9	CD				-
PF10	INTR				-
PF12	A6	A6			-
PF13	A7	A7			-
PF14	A8	A8			-
PF15	A9	A9			-
PG0	A10	A10			-
PG1		A11			-
PE7	D4	D4	DA4	D4	Yes
PE8	D5	D5	DA5	D5	Yes
PE9	D6	D6	DA6	D6	Yes
PE10	D7	D7	DA7	D7	Yes
PE11	D8	D8	DA8	D8	Yes
PE12	D9	D9	DA9	D9	Yes
PE13	D10	D10	DA10	D10	Yes
PE14	D11	D11	DA11	D11	Yes
PE15	D12	D12	DA12	D12	Yes
PD8	D13	D13	DA13	D13	Yes
PD9	D14	D14	DA14	D14	Yes

Table 8. FSMC pin definition (continued)

Pins[1]	FSMC				LQFP100[2]
	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PD10	D15	D15	DA15	D15	Yes
PD11		A16	A16	CLE	Yes
PD12		A17	A17	ALE	Yes
PD13		A18	A18		Yes
PD14	D0	D0	DA0	D0	Yes
PD15	D1	D1	DA1	D1	Yes
PG2		A12			-
PG3		A13			-
PG4		A14			-
PG5		A15			-
PG6				INT2	-
PG7				INT3	-
PD0	D2	D2	DA2	D2	Yes
PD1	D3	D3	DA3	D3	Yes
PD3		CLK	CLK		Yes
PD4	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7		NE1	NE1	NCE2	Yes
PG9		NE2	NE2	NCE3	-
PG10	NCE4_1	NE3	NE3		-
PG11	NCE4_2				-
PG12		NE4	NE4		-
PG13		A24	A24		-
PG14		A25	A25		-
PB7		NADV	NADV		Yes
PE0		NBL0	NBL0		Yes
PE1		NBL1	NBL1		Yes

1. Full FSMC features are available on LQFP144, LQFP176, and UFBGA176. The features available on smaller packages are given in the dedicated package column.
2. Ports F and G are not available in devices delivered in 100-pin packages.

Table 9. Alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/4/5/6 I2S2/I2S2ext	SPI3/I2Sext/ I2S3	USART1/2/3/ I2S3ext	UART4/5/7/8 USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI		
Port A	PA0		TIM2_CH1 TIM2_ETR	TIM 5_CH1	TIM8_ETR				USART2_CTS	UART4_TX			ETH_MII_CRS				EVENTOUT
	PA1		TIM2_CH2	TIM5_CH2					USART2_RTS	UART4_RX			ETH_MII _RX_CLK ETH_RMII _REF_CLK				EVENTOUT
	PA2		TIM2_CH3	TIM5_CH3	TIM9_CH1				USART2_TX				ETH_MDIO				EVENTOUT
	PA3		TIM2_CH4	TIM5_CH4	TIM9_CH2				USART2_RX			OTG_HS_ULPI_D0	ETH _MII_COL				EVENTOUT
	PA4						SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK					OTG_HS_SOF	DCMI_HSYNC		EVENTOUT
	PA5		TIM2_CH1 TIM2_ETR		TIM8_CH1N		SPI1_SCK					OTG_HS_ULPI_CK					EVENTOUT
	PA6		TIM1_BKIN	TIM3_CH1	TIM8_BKIN		SPI1_MISO				TIM13_CH1				DCMI_PIXCK		EVENTOUT
	PA7		TIM1_CH1N	TIM3_CH2	TIM8_CH1N		SPI1_MOSI				TIM14_CH1		ETH_MII _RX_DV ETH_RMII _CRS_DV				EVENTOUT
	PA8	MCO1	TIM1_CH1			I2C3_SCL			USART1_CK			OTG_FS_SOF					EVENTOUT
	PA9		TIM1_CH2			I2C3_SMBA			USART1_TX						DCMI_D0		EVENTOUT
	PA10		TIM1_CH3						USART1_RX			OTG_FS_ID			DCMI_D1		EVENTOUT
	PA11		TIM1_CH4						USART1_CTS		CAN1_RX	OTG_FS_DM					EVENTOUT
	PA12		TIM1_ETR						USART1_RTS		CAN1_TX	OTG_FS_DP					EVENTOUT
	PA13	JTMS-SWDIO															EVENTOUT
	PA14	JTCK-SWCLK															EVENTOUT
	PA15	JTDI	TIM 2_CH1 TIM 2_ETR				SPI1_NSS	SPI3_NSS/ I2SS3_WS									EVENTOUT

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/4/5/6 I2S2/I2S2ext	SPI3/I2Sext/ I2S3	USART1/2/3/ I2S3ext	UART4/5/7/8 USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI		
Port B	PB0		TIM1_CH2N	TIM3_CH3	TIM8_CH2N							OTG_HS_ULPI_D1	ETH _MII_RXD2				EVENTOUT
	PB1		TIM1_CH3N	TIM3_CH4	TIM8_CH3N							OTG_HS_ULPI_D2	ETH _MII_RXD3				EVENTOUT
	PB2																EVENTOUT
	PB3	JTDO/ TRACESWO	TIM2_CH2				SPI1_SCK	SPI3_SCK I2S3_CK									EVENTOUT
	PB4	NJTRST		TIM3_CH1			SPI1_MISO	SPI3_MISO	I2S3ext_SD								EVENTOUT
	PB5			TIM3_CH2		I2C1_SMBA	SPI1_MOSI	SPI3_MOSI I2S3_SD			CAN2_RX	OTG_HS_ULPI_D7	ETH _PPS_OUT		DCMI_D10		EVENTOUT
	PB6			TIM4_CH1		I2C1_SCL	I2S2_WS		USART1_TX		CAN2_TX				DCMI_D5		EVENTOUT
	PB7			TIM4_CH2		I2C1_SDA			USART1_RX					FSMC_NL	DCMI_VSYNC		EVENTOUT
	PB8			TIM4_CH3	TIM10_CH1	I2C1_SCL					CAN1_RX		ETH _MII_TXD3	SDIO_D4	DCMI_D6		EVENTOUT
	PB9			TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS I2S2_WS				CAN1_TX			SDIO_D5	DCMI_D7		EVENTOUT
	PB10		TIM2_CH3			I2C2_SCL	SPI2_SCK I2S2_CK		USART3_TX			OTG_HS_ULPI_D3	ETH_ MII_RX_ER				EVENTOUT
	PB11		TIM2_CH4			I2C2_SDA			USART3_RX			OTG_HS_ULPI_D4	ETH _MII_TX_EN ETH _RMII_TX_EN				EVENTOUT
	PB12		TIM1_BKIN			I2C2_SMBA	SPI2_NSS I2S2_WS		USART3_CK		CAN2_RX	OTG_HS_ULPI_D5	ETH _MII_TXD0 ETH _RMII_TXD0	OTG_HS_ID			EVENTOUT
	PB13		TIM1_CH1N				SPI2_SCK I2S2_CK		USART3_CTS		CAN2_TX	OTG_HS_ULPI_D6	ETH _MII_TXD1 ETH _RMII_TXD1				EVENTOUT
	PB14		TIM1_CH2N		TIM8_CH2N		SPI2_MISO	I2S2ext_SD	USART3_RTS		TIM12_CH1			OTG_HS_DM			EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N		TIM8_CH3N		SPI2_MOSI I2S2_SD				TIM12_CH2			OTG_HS_DP			EVENTOUT
Port C	PC0											OTG_HS_ULPI_STP					EVENTOUT
	PC1												ETH_MDC				EVENTOUT
	PC2						SPI2_MISO	I2S2ext_SD				OTG_HS_ULPI_DIR	ETH _MII_TXD2				EVENTOUT
	PC3						SPI2_MOSI I2S2_SD					OTG_HS_ULPI_NXT	ETH _MII_TX_CLK				EVENTOUT
	PC4												ETH_MII_RXD0 ETH_RMII_RXD0				EVENTOUT
	PC5												ETH _MII_RXD1 ETH _RMII_RXD1				EVENTOUT
	PC6			TIM3_CH1	TIM8_CH1		I2S2_MCK			USART6_TX				SDIO_D6	DCMI_D0		EVENTOUT
	PC7			TIM3_CH2	TIM8_CH2			I2S3_MCK		USART6_RX				SDIO_D7	DCMI_D1		EVENTOUT
	PC8			TIM3_CH3	TIM8_CH3					USART6_CK				SDIO_D0	DCMI_D2		EVENTOUT
	PC9	MCO2		TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN							SDIO_D1	DCMI_D3		EVENTOUT
	PC10							SPI3_SCK/ I2S3S_CK	USART3_TX/	UART4_TX				SDIO_D2	DCMI_D8		EVENTOUT
	PC11					/	I2S3ext_SD	SPI3_MISO	USART3_RX	UART4_RX				SDIO_D3	DCMI_D4		EVENTOUT
	PC12							SPI3_MOSI I2S3_SD	USART3_CK	UART5_TX				SDIO_CK	DCMI_D9		EVENTOUT
	PC13																
	PC14																
	PC15																

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/4/5/6 I2S2/I2S2ext	SPI3/I2Sext/ I2S3	USART1/2/3/ I2S3ext	UART4/5/7/8 USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI		
Port D	PD0										CAN1_RX			FSMC_D2			EVENTOUT
	PD1										CAN1_TX			FSMC_D3			EVENTOUT
	PD2			TIM3_ETR						UART5_RX				SDIO_CMD	DCMI_D11		EVENTOUT
	PD3						SPI2_SCK I2S2_CK		USART2_CTS					FSMC_CLK	DCMI_D5		EVENTOUT
	PD4								USART2_RTS					FSMC_NOE			EVENTOUT
	PD5								USART2_TX					FSMC_NWE			EVENTOUT
	PD6						SPI3_MOSI I2S3_MOSI		USART2_RX					FSMC_NWAIT	DCMI_D10		EVENTOUT
	PD7								USART2_CK					FSMC_NE1/ FSMC_NCE2			EVENTOUT
	PD8								USART3_TX					FSMC_D13			EVENTOUT
	PD9								USART3_RX					FSMC_D14			EVENTOUT
	PD10								USART3_CK					FSMC_D15			EVENTOUT
	PD11								USART3_CTS					FSMC_A16			EVENTOUT
	PD12			TIM4_CH1					USART3_RTS					FSMC_A17			EVENTOUT
	PD13			TIM4_CH2										FSMC_A18			EVENTOUT
	PD14			TIM4_CH3										FSMC_D0			EVENTOUT
	PD15			TIM4_CH4										FSMC_D1			EVENTOUT
Port E	PE0			TIM4_ETR						UART8_Rx				FSMC_NBL0	DCMI_D2		EVENTOUT
	PE1									UART8_Tx				FSMC_BLN1	DCMI_D3		EVENTOUT
	PE2	TRACECLK					SPI4_SCK						ETH _MII_TXD3	FSMC_A23			EVENTOUT
	PE3	TRACED0												FSMC_A19			EVENTOUT
	PE4	TRACED1					SPI4_NSS							FSMC_A20	DCMI_D4		EVENTOUT
	PE5	TRACED2			TIM9_CH1		SPI4_MISO							FSMC_A21	DCMI_D6		EVENTOUT
	PE6	TRACED3			TIM9_CH2		SPI4_MOSI							FSMC_A22	DCMI_D7		EVENTOUT
	PE7		TIM1_ETR							UART7_Rx				FSMC_D4			EVENTOUT
	PE8		TIM1_CH1N							UART7_Tx				FSMC_D5			EVENTOUT
	PE9		TIM1_CH1											FSMC_D6			EVENTOUT
	PE10		TIM1_CH2N											FSMC_D7			EVENTOUT
	PE11		TIM1_CH2				SPI4_NSS							FSMC_D8			EVENTOUT
	PE12		TIM1_CH3N				SPI4_SCK							FSMC_D9			EVENTOUT
	PE13		TIM1_CH3				SPI4_MISO							FSMC_D10			EVENTOUT
	PE14		TIM1_CH4				SPI4_MOSI							FSMC_D11			EVENTOUT
	PE15		TIM1_BKIN											FSMC_D12			EVENTOUT

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/4/5/6 I2S2/I2S2ext	SPI3/I2Sext/ I2S3	USART1/2/3/ I2S3ext	UART4/5/7/8 USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI		
Port F	PF0					I2C2_SDA								FSMC_A0			EVENTOUT
	PF1					I2C2_SCL								FSMC_A1			EVENTOUT
	PF2					I2C2_SMBA								FSMC_A2			EVENTOUT
	PF3													FSMC_A3			EVENTOUT
	PF4													FSMC_A4			EVENTOUT
	PF5													FSMC_A5			EVENTOUT
	PF6				TIM10_CH1		SPI5_NSS			UART7_Rx				FSMC_NIORD			EVENTOUT
	PF7				TIM11_CH1		SPI5_SCK			UART7_Tx				FSMC_NREG			EVENTOUT
	PF8						SPI5_MISO				TIM13_CH1			FSMC_NIOWR			EVENTOUT
	PF9						SPI5_MOSI				TIM14_CH1			FSMC_CD			EVENTOUT
	PF10													FSMC_INTR	DCMI_D11		EVENTOUT
	PF11						SPI5_MOSI								DCMI_D12		EVENTOUT
	PF12													FSMC_A6			EVENTOUT
	PF13													FSMC_A7			EVENTOUT
	PF14													FSMC_A8			EVENTOUT
	PF15													FSMC_A9			EVENTOUT
Port G	PG0													FSMC_A10			EVENTOUT
	PG1													FSMC_A11			EVENTOUT
	PG2													FSMC_A12			EVENTOUT
	PG3													FSMC_A13			EVENTOUT
	PG4													FSMC_A14			EVENTOUT
	PG5													FSMC_A15			EVENTOUT
	PG6													FSMC_INT2	DCMI_D12		EVENTOUT
	PG7									USART6_CK				FSMC_INT3	DCMI_D13		EVENTOUT
	PG8						SPI6_NSS			USART6_RTS			ETH _PPS_OUT				EVENTOUT
	PG9									USART6_RX				FSMC_NE2/ FSMC_NCE3			EVENTOUT
	PG10													FSMC_NCE4_1/ FSMC_NE3	DCMI_D2		EVENTOUT
	PG11												ETH _MII_TX_EN ETH _RMII_TX_EN	FSMC_NCE4_2	DCMI_D3		EVENTOUT
	PG12						SPI6_MISO			USART6_RTS				FSMC_NE4			EVENTOUT
	PG13						SPI6_SCK			UART6_CTS			ETH _MII_TXD0 ETH _RMII_TXD0	FSMC_A24			EVENTOUT
	PG14						SPI6_MOSI			USART6_TX			ETH _MII_TXD1 ETH _RMII_TXD1	FSMC_A25			EVENTOUT
	PG15									USART6_CTS					DCMI_D13		EVENTOUT

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/4/5/6 I2S2/I2S2ext	SPI3/I2Sext/ I2S3	USART1/2/3/ I2S3ext	UART4/5/7/8 USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI		
Port H	PH0																
	PH1																
	PH2												ETH _MII_CRS				EVENTOUT
	PH3												ETH _MII_COL				EVENTOUT
	PH4					I2C2_SCL						OTG_HS_ULPI_NXT					EVENTOUT
	PH5					I2C2_SDA	SPI5_NSS										EVENTOUT
	PH6					I2C2_SMBA	SPI5_SCK				TIM12_CH1		ETH _MII_RXD2		DCMI_D8		EVENTOUT
	PH7					I2C3_SCL	SPI5_MISO						ETH _MII_RXD3		DCMI_D9		EVENTOUT
	PH8					I2C3_SDA									DCMI_HSYNC		EVENTOUT
	PH9					I2C3_SMBA					TIM12_CH2				DCMI_D0		EVENTOUT
	PH10			TIM5_CH1											DCMI_D1		EVENTOUT
	PH11			TIM5_CH2											DCMI_D2		EVENTOUT
	PH12			TIM5_CH3											DCMI_D3		EVENTOUT
	PH13				TIM8_CH1N						CAN1_TX						EVENTOUT
	PH14				TIM8_CH2N										DCMI_D4		EVENTOUT
	PH15				TIM8_CH3N										DCMI_D11		EVENTOUT
Port I	PI0			TIM5_CH4			SPI2_NSS I2S2_WS								DCMI_D13		EVENTOUT
	PI1						SPI2_SCK I2S2_CK								DCMI_D8		EVENTOUT
	PI2				TIM8_CH4		SPI2_MISO	I2S2ext_SD							DCMI_D9		EVENTOUT
	PI3				TIM8_ETR		SPI2_MOSI I2S2_SD								DCMI_D10		EVENTOUT
	PI4				TIM8_BKIN										DCMI_D5		EVENTOUT
	PI5				TIM8_CH1										DCMI_VSYNC		EVENTOUT
	PI6				TIM8_CH2										DCMI_D6		EVENTOUT
	PI7				TIM8_CH3										DCMI_D7		EVENTOUT
	PI8																
	PI9										CAN1_RX						EVENTOUT
	PI10												ETH _MII_RX_ER				EVENTOUT
	PI11											OTG_HS_ULPI_DIR					EVENTOUT

5 Memory mapping

The memory map is shown in *Figure 12*.

Figure 12. Memory map

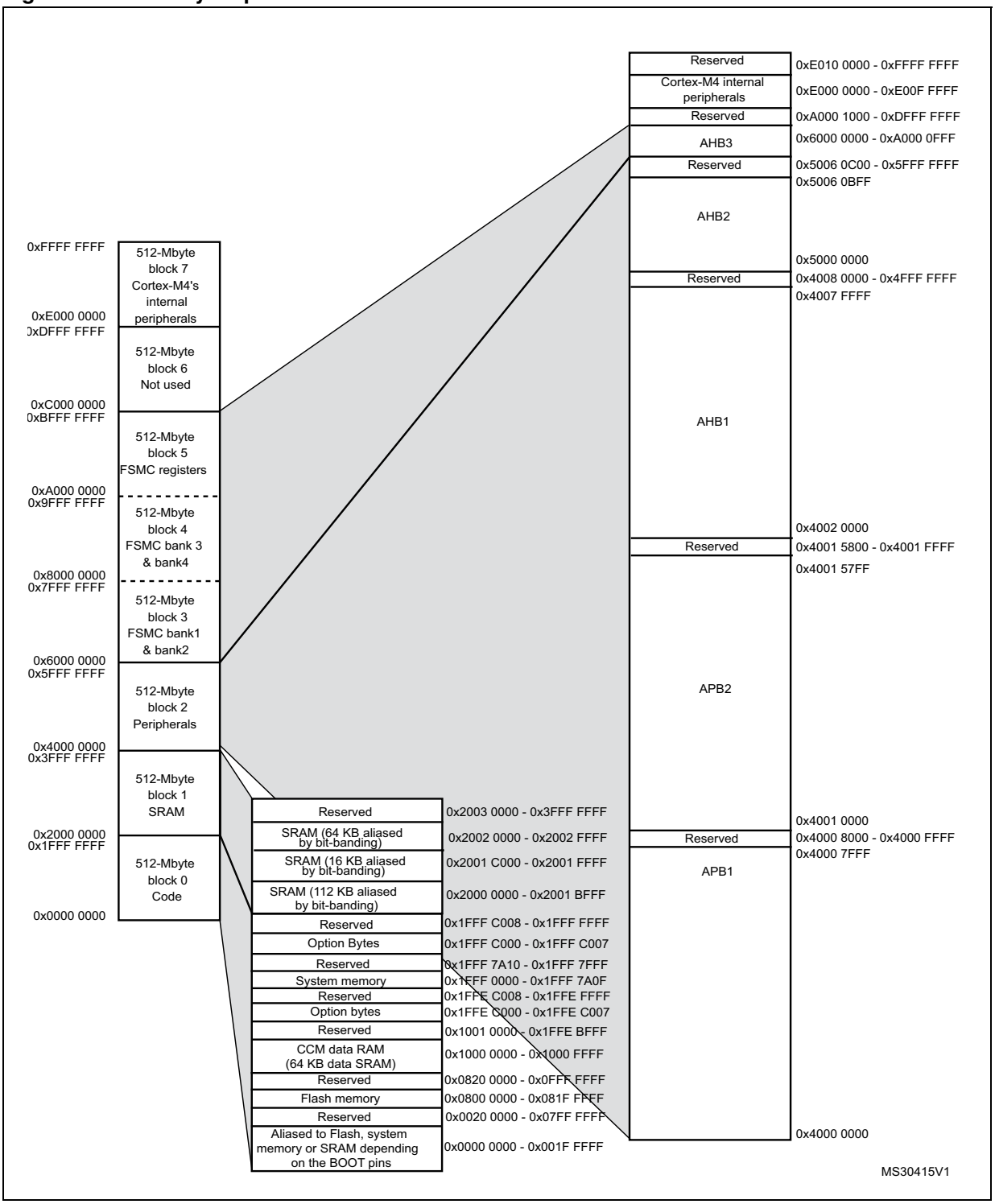


Table 10. STM32F43x register boundary addresses

Bus	Boundary address	Peripheral
	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex-M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
	0xA000 1000 - 0xDFFF FFFF	Reserved
AHB3	0xA000 0000 - 0xA000 0FFF	FSMC control register
	0x9000 0000 - 0x9FFF FFFF	FSMC bank 4
	0x8000 0000 - 0x8FFF FFFF	FSMC bank 3
	0x7000 0000 - 0x7FFF FFFF	FSMC bank 2
	0x6000 0000 - 0x6FFF FFFF	FSMC bank 1
	0x5006 0C00- 0x5FFF FFFF	Reserved
AHB2	0x5006 0800 - 0X5006 0BFF	RNG
	0x5006 0400 - 0X5006 07FF	HASH
	0x5006 0000 - 0X5006 03FF	CRYP
	0x5005 0400 - 0x5005 FFFF	Reserved
	0x5005 0000 - 0X5005 03FF	DCMI
	0x5004 0000- 0x5004 FFFF	Reserved
	0x5000 0000 - 0X5003 FFFF	USB OTG FS
	0x4008 0000- 0x4FFF FFFF	Reserved

Table 10. STM32F43x register boundary addresses (continued)

Bus	Boundary address	Peripheral
AHB1	0x4004 0000 - 0x4007 FFFF	USB OTG HS
	0X4002 9400 - 0x4003 FFFF	Reserved
	0x4002 9000 - 0x4002 93FF	ETHERNET MAC
	0x4002 8C00 - 0x4002 8FFF	
	0x4002 8800 - 0x4002 8BFF	
	0x4002 8400 - 0x4002 87FF	
	0x4002 8000 - 0x4002 83FF	
	0x4002 6800 - 0x4002 7FFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0X4002 5000 - 0X4002 5FFF	Reserved
	0x4002 4000 - 0x4002 4FFF	BKPSRAM
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0X4002 3400 - 0X4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2400 - 0x4002 2FFF	Reserved
	0x4002 2000 - 0x4002 23FF	GPIOI
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0X4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA
	0x4001 5800- 0x4001 FFFF	Reserved

Table 10. STM32F43x register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB2	0x4001 5400 - 0x4001 57FF	SPI6
	0x4001 5000 - 0x4001 53FF	SPI5
	0x4001 4C00 - 0x4001 4FFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4
	0x4001 3000 - 0x4001 33FF	SPI1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1
	0x4000 7800- 0x4000 FFFF	Reserved

Table 10. STM32F43x register boundary addresses (continued)

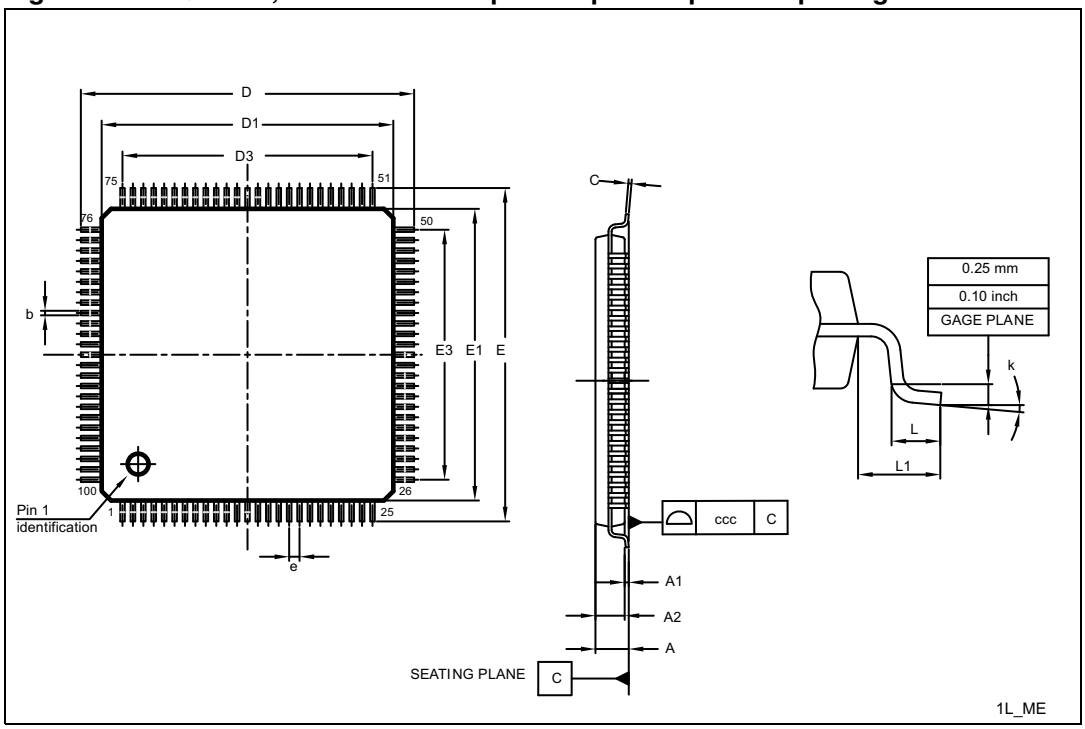
Bus	Boundary address	Peripheral
APB1	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	Reserved
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	Reserved
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	I2S2ext
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	Reserved
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

6 Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 13. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 11. LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data

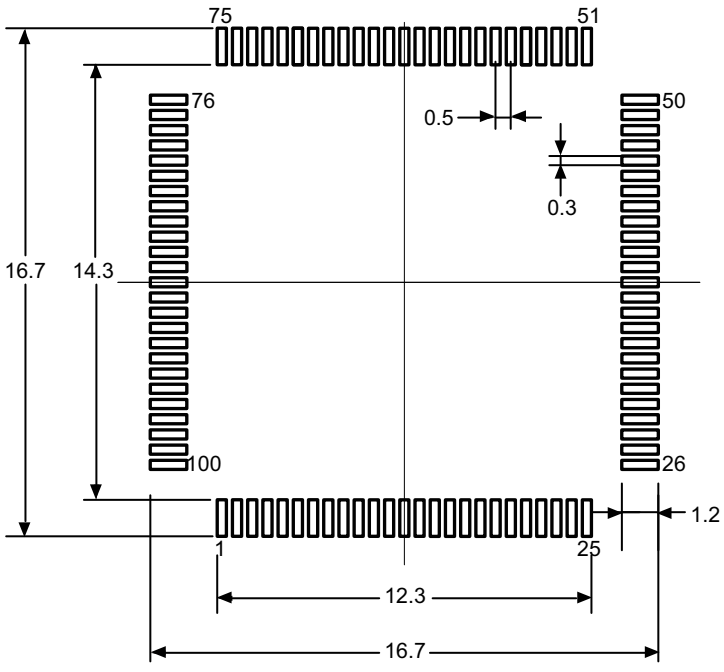
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3		12.000			0.4724	

Table 11. LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3		12.000			0.4724	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc			0.080			0.0031

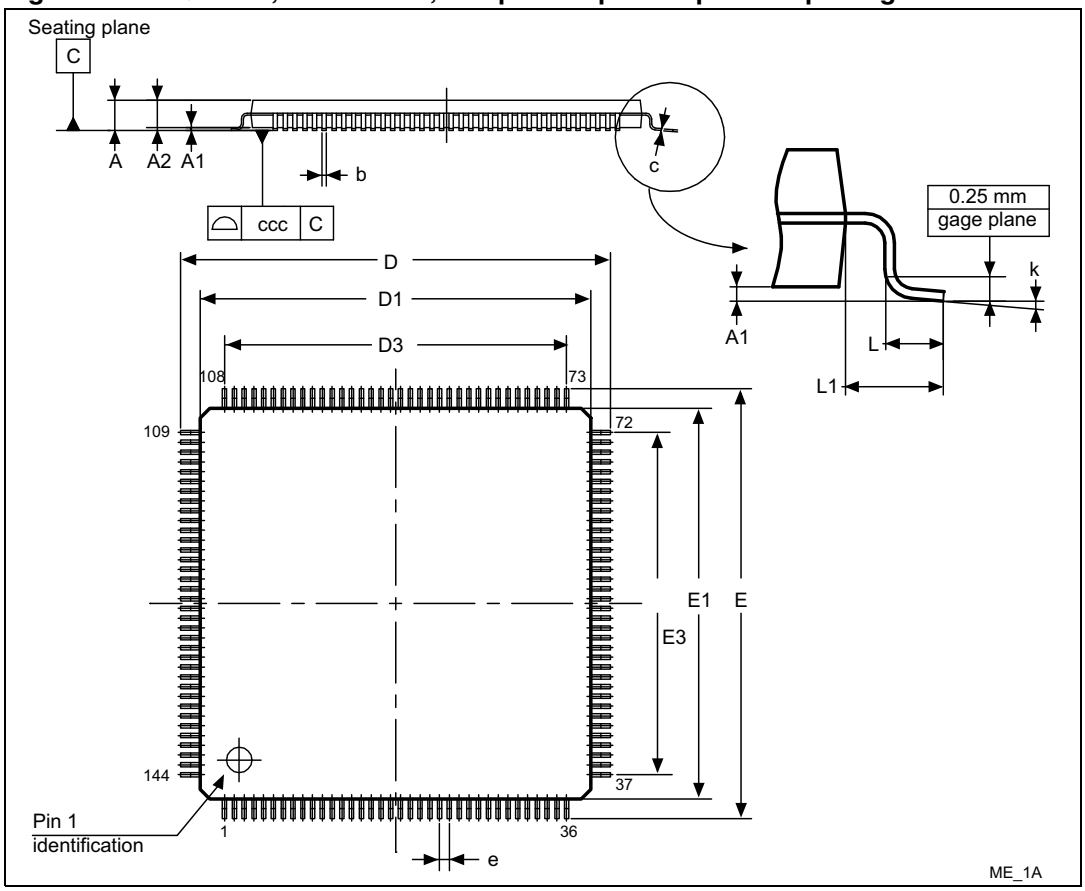
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 14. Recommended footprint



1. Dimensions are expressed in millimeters.

Figure 15. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 12. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

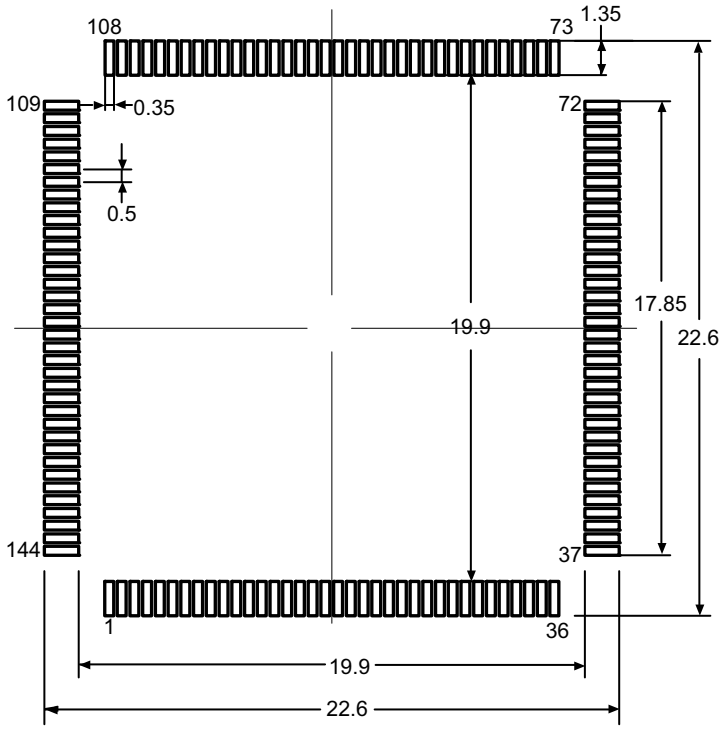
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.874
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3		17.500			0.689	
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3		17.500			0.6890	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295

Table 12. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
L1		1.000			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc	0.080			0.0031		

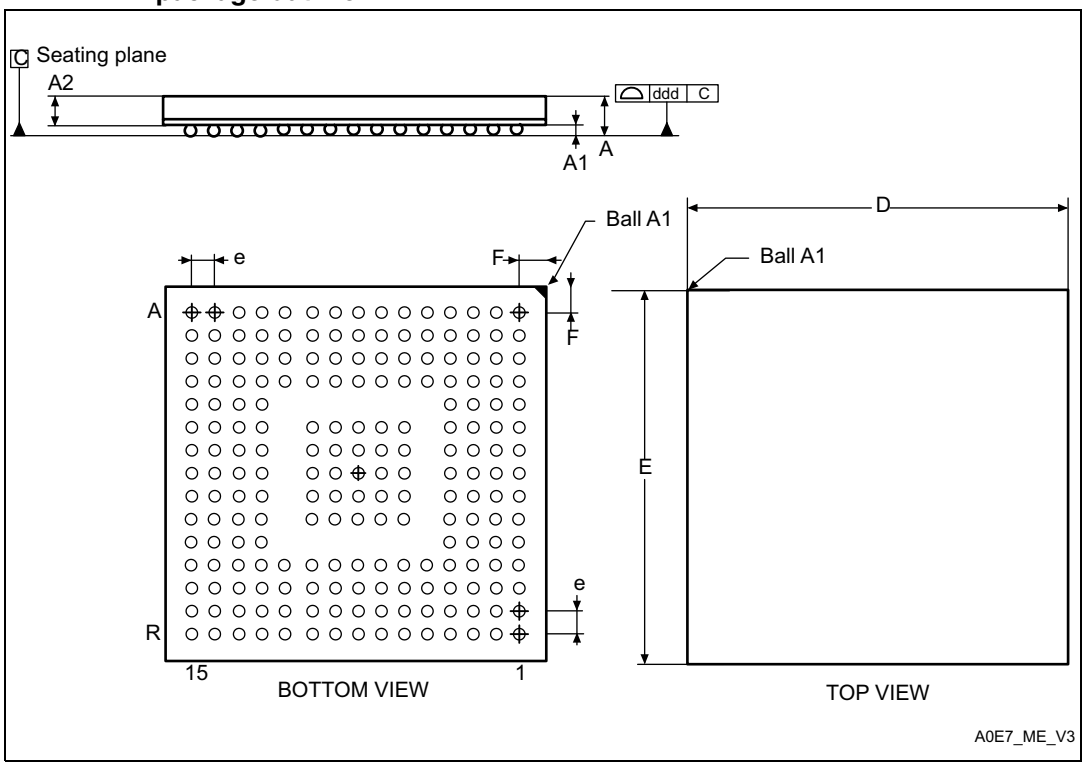
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 16. Recommended footprint



1. Dimensions are expressed in millimeters.

Figure 17. UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline



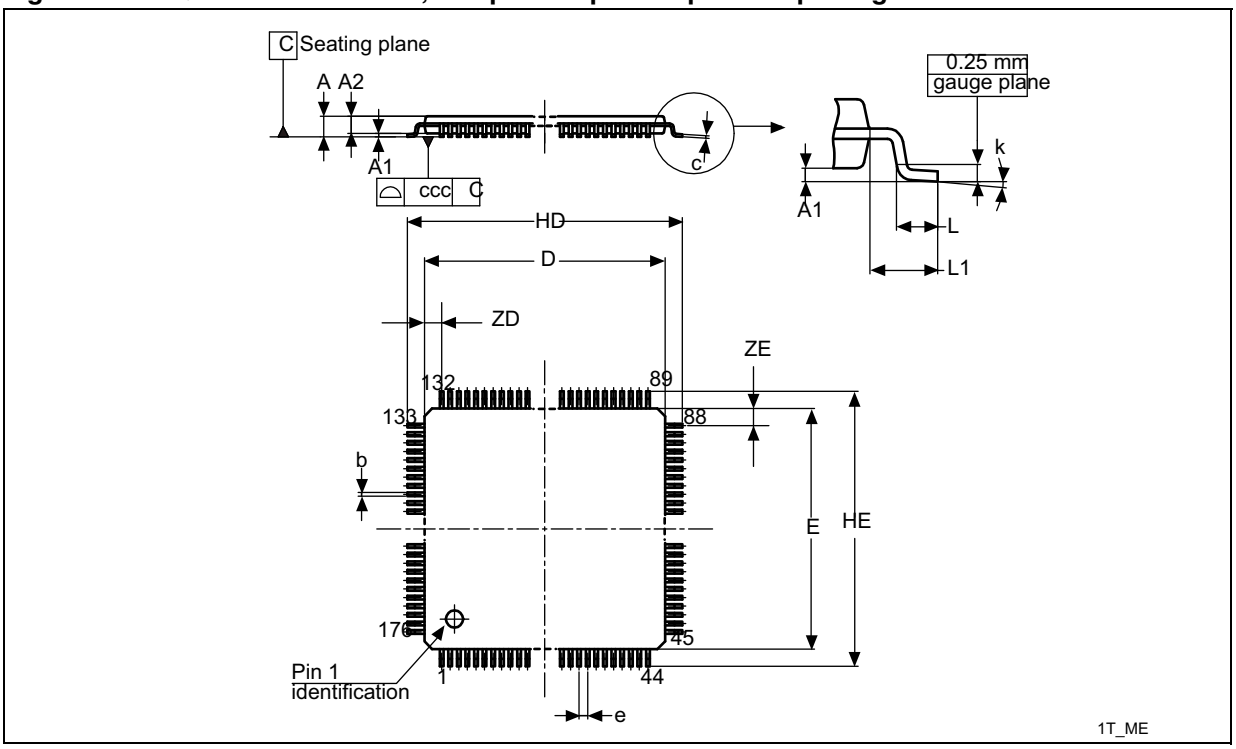
1. Drawing is not to scale.

Table 13. UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.002	0.0031	0.0043
A4	0.400	0.450	0.500	0.0157	0.0177	0.0197
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	9.900	10.000	10.100	0.3898	0.3937	0.3976
E	9.900	10.000	10.100	0.3898	0.3937	0.3976
e		0.650			0.0256	
F	0.425	0.450	0.475	0.0167	0.0177	0.0187
ddd			0.080			0.0031
eee			0.150			0.0059
fff			0.080			0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 18. LQFP176 24 x 24 mm, 176-pin low-profile quad flat package outline



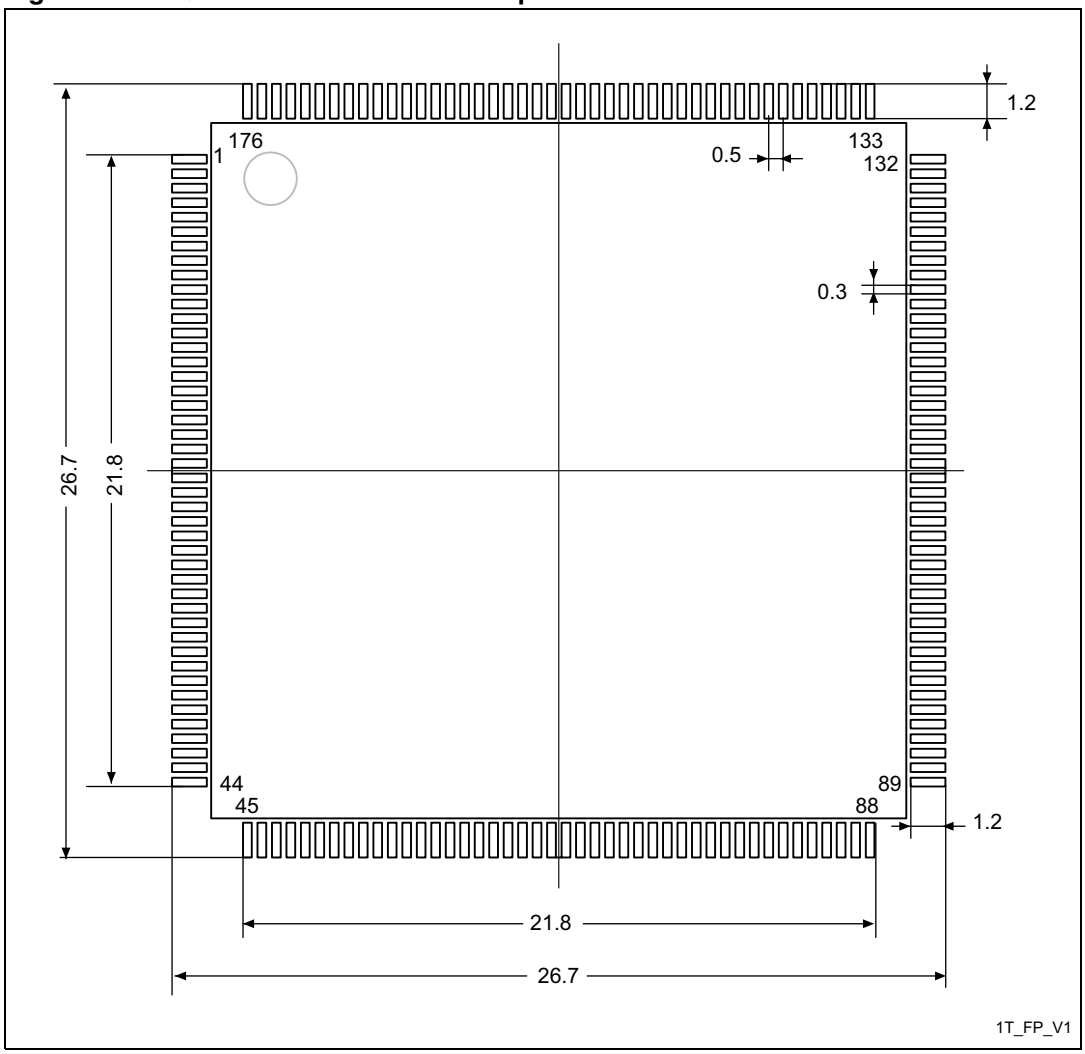
1. Drawing is not to scale.

Table 14. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		
A2	1.350		1.450	0.0531		0.0060
b	0.170		0.270	0.0067		0.0106
C	0.090		0.200	0.0035		0.0079
D	23.900		24.100	0.9409		0.9488
E	23.900		24.100	0.9409		0.9488
e		0.500			0.0197	
HD	25.900		26.100	1.0200		1.0276
HE	25.900		26.100	1.0200		1.0276
L	0.450		0.750	0.0177		0.0295
L1		1.000			0.0394	
ZD		1.250			0.0492	
ZE		1.250			0.0492	
ccc			0.080			0.0031
k	0 °		7 °	0 °		7 °

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 19. LQFP176 recommended footprint



1. Dimensions are expressed in millimeters.

6.2 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max x } \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL}/ I_{OL} and V_{OH}/ I_{OH} of the I/Os at low and high level in the application.

Table 15. Package thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP100 - 14 × 14 mm/ 0.5 mm pitch	43	°C/W
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm/ 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm/ 0.5 mm pitch	38	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm/ 0.65 mm pitch	39	

1. TBD stands for “to be defined”.

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

7 Part numbering

Table 16. Ordering information scheme

Example: STM32 F 437 V I T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

437= STM32F43x, connectivity, USB OTG FS/HS, camera interface, Ethernet, cryptographic acceleration

Pin count

V = 100 pins
Z = 144 pins
I = 176 pins

Flash memory size

G = 1024 Kbytes of Flash memory
I = 2048 Kbytes of Flash memory

Package

T = LQFP
H = UFBGA

Temperature range

6 = Industrial temperature range, –40 to 85 °C.
7 = Industrial temperature range, –40 to 105 °C.

Options

xxx = programmed parts
TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Appendix A Application block diagrams

A.1 Main applications versus package

Table 17 gives examples of configurations for each package.

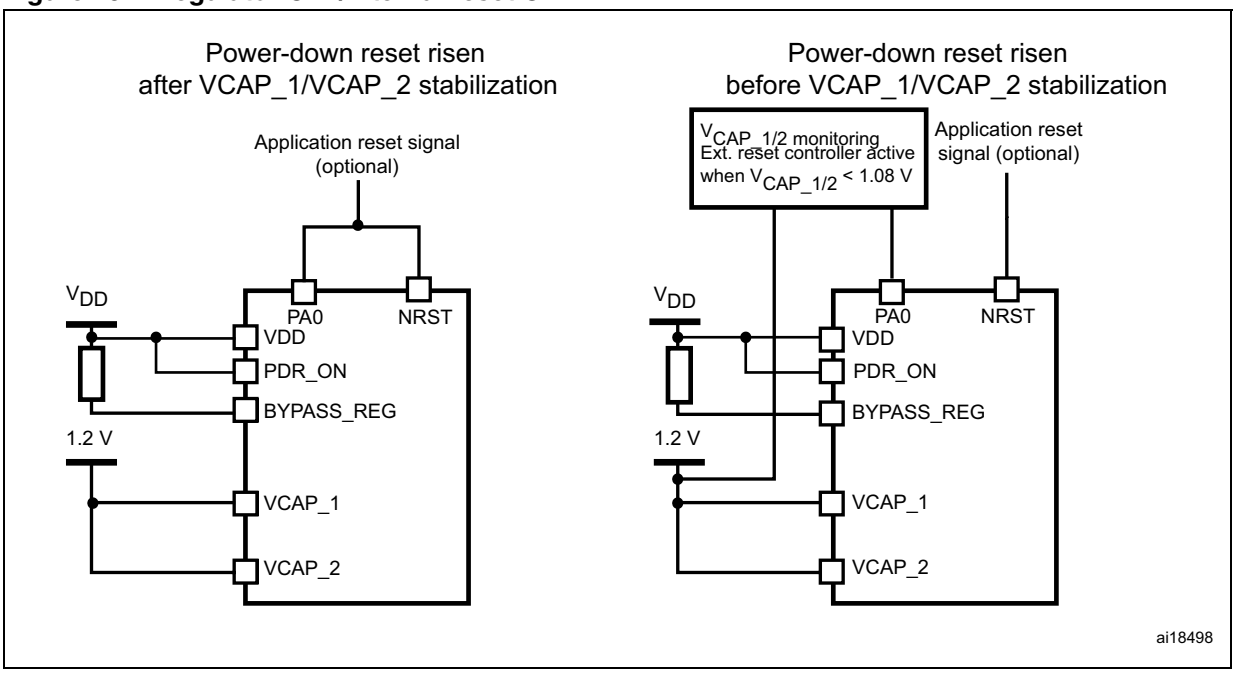
Table 17. Main applications versus package for STM32F437xx microcontrollers

		100 pins				144 pins				176 pins	
		Config 1	Config2	Config3	Config 4	Config1	Config 2	Config3	Config4	Config1	Config2
USB 1	OTG FS	X	X	X	-	X		X		X	
	FS	X	X	X	X	X	X	X	X	X	
USB 2	HS ULPI	X	-	-	-	X	X			X	X
	OTGFS	X				X	X			X	X
	FS	X	X	X	X	X	X	X	X	X	X
Ethernet	MII	-	-	X	X			X	X	X	X
	RMII	-	X	X	X	X	X	X	X	X	X
SPI/I2S2 SPI/I2S3		X(1)	X	X	X	X	X	X	X	X	X
SDIO	SDIO	SDIO or DCMI	SDIO or DCMI	SDIO or DCMI	X	SDIO or DCMI	X	SDIO or DCMI	X	X	X
DCMI	8bits Data				X		X		X	X	X
	10bits Data				X		X		X	X	X
	12bits Data				X		X		X	X	X
	14bits Data	-	-	-	-		X		X	X	X
FSMC	NOR/ RAM Muxed	X	X	X	X	X	X	X	X	X	X
	NOR/ RAM					X	X	X	X	X	X
	NAND	X	X	X	X	X	X	X	X	X	X
	CF	-	-	-	-	X	X	X	X	X	X
CAN		-	X	X	X	-	-	X	X	-	X

1. Only SPI/I2S3 is available.

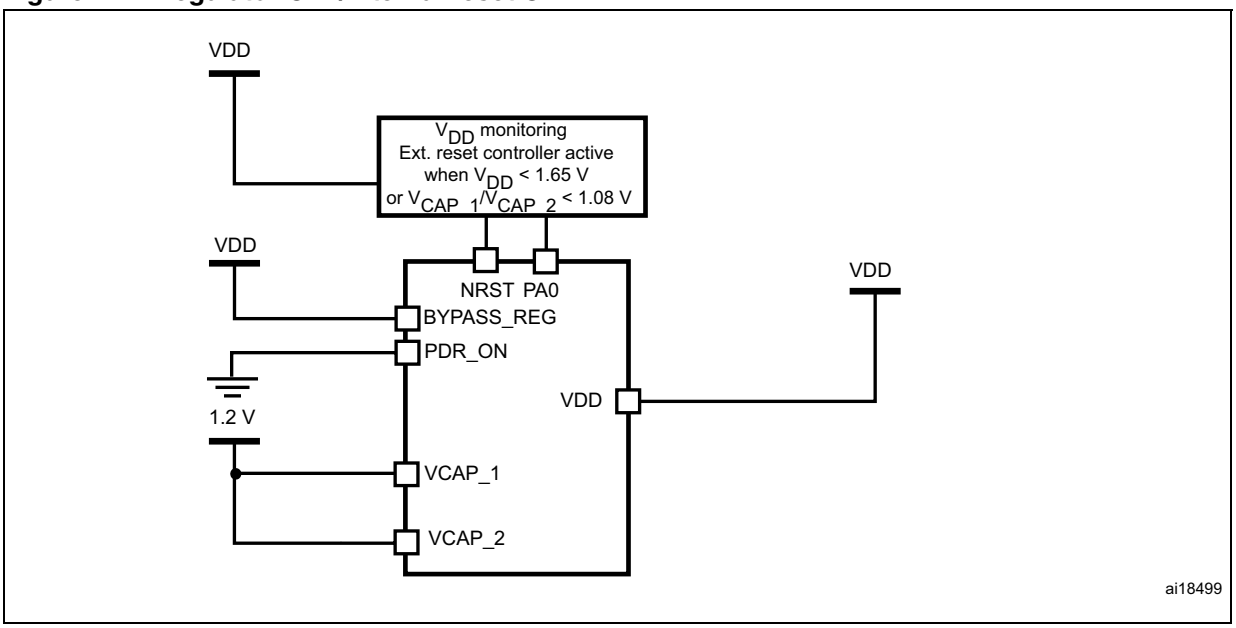
A.2 Application example with regulator OFF

Figure 20. Regulator OFF/internal reset ON



1. This mode is available only on UFBGA176 and LQFP176 packages.
2. In regulator bypass mode, PA0 is used as power-on reset. The connection between PA0 and NRST can consequently prevent debug connection. If the debug connection under reset or pre-reset is required, the user must manage the reset and the power-on reset separately.

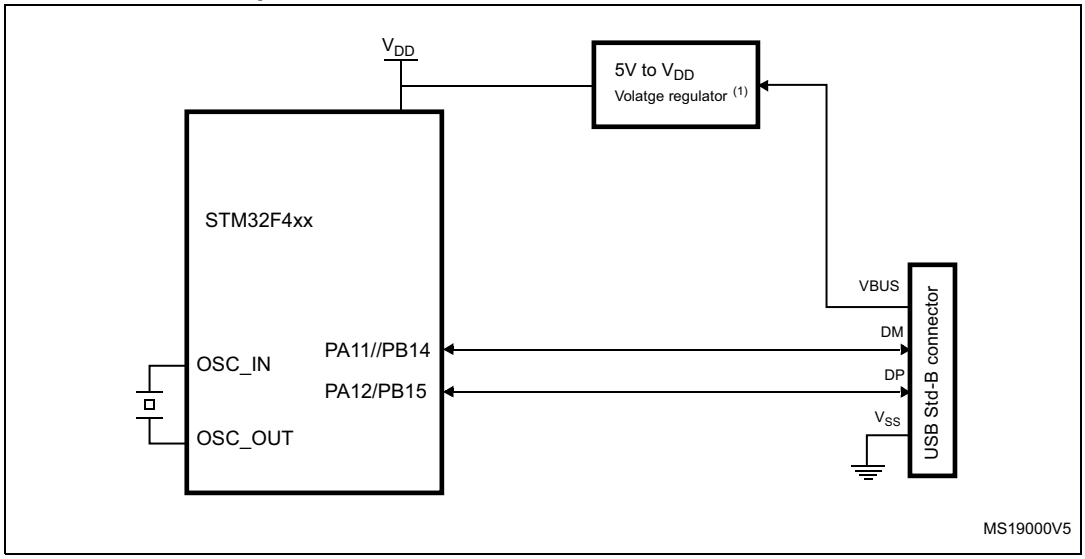
Figure 21. Regulator OFF/internal reset OFF



1. This mode is available only on UFBGA176 and LQFP176 packages.

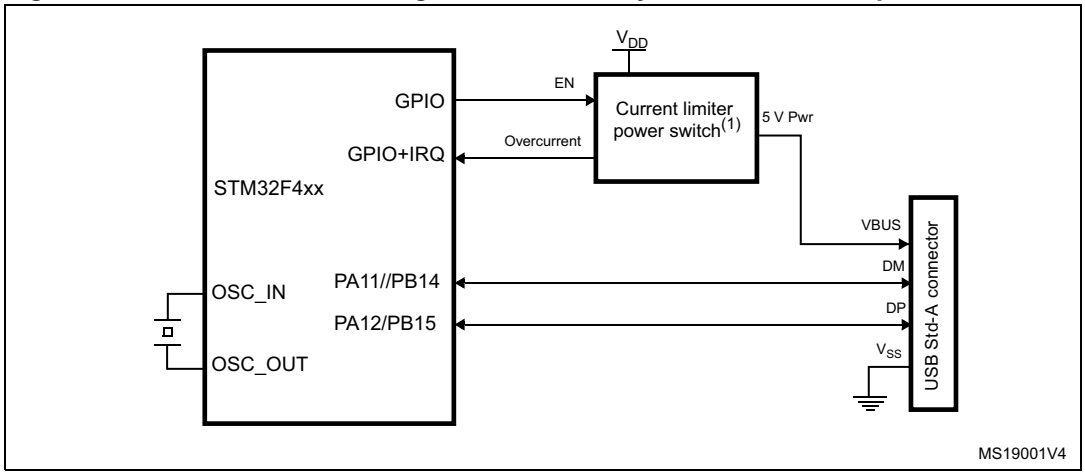
A.3 USB OTG full speed (FS) interface solutions

Figure 22. USB controller configured as peripheral-only and used in Full speed mode



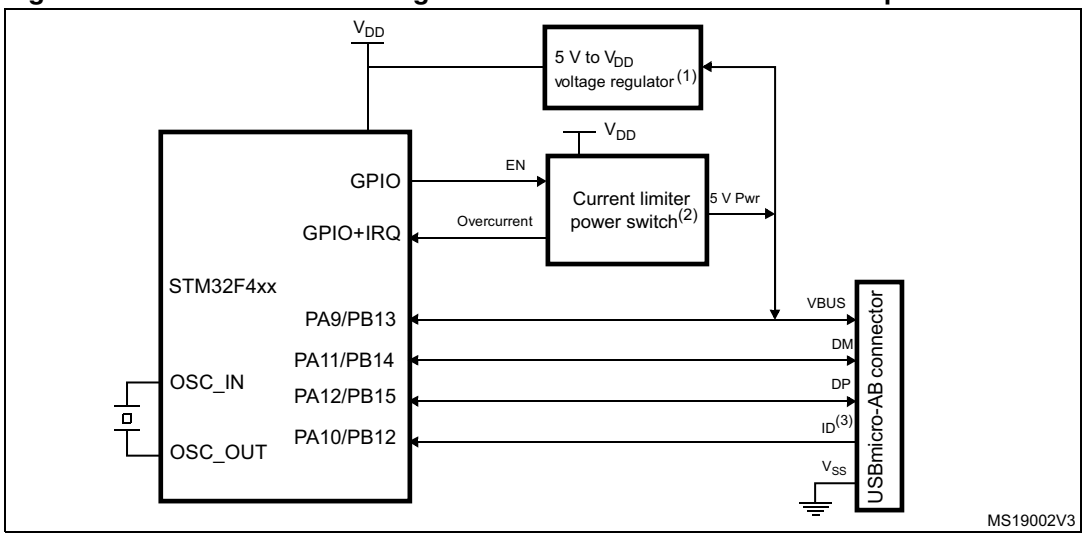
1. External voltage regulator only needed when building a V_{BUS} powered device.
2. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

Figure 23. USB controller configured as host-only and used in full speed mode



1. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
2. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

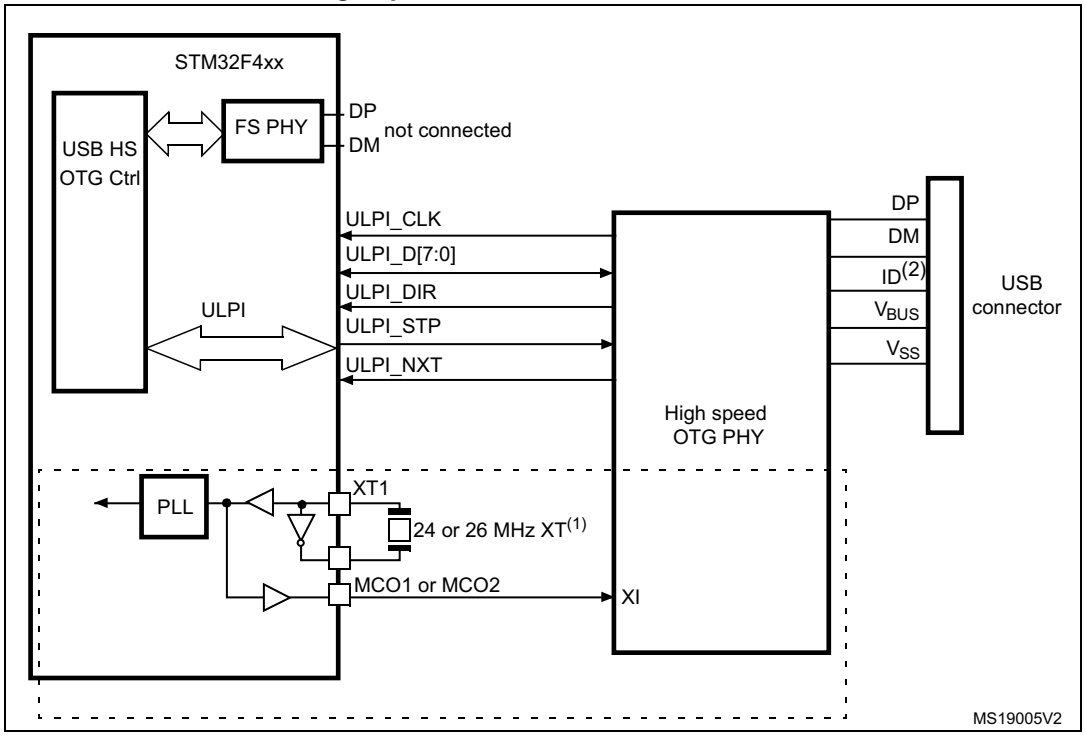
Figure 24. USB controller configured in dual mode and used in full speed mode



1. External voltage regulator only needed when building a V_{BUS} powered device.
2. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
3. The ID pin is required in dual role only.
4. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

A.4 USB OTG high speed (HS) interface solutions

Figure 25. USB controller configured as peripheral, host, or dual-mode and used in high speed mode



1. It is possible to use MCO1 or MCO2 to save a crystal. It is however not mandatory to clock the STM32F43x with a 24 or 26 MHz crystal when using USB HS. The above figure only shows an example of a possible connection.
2. The ID pin is required in dual role only.

A.5 Complete audio player solutions

Two solutions are offered, illustrated in *Figure 26* and *Figure 27*.

Figure 26 shows storage media to audio DAC/amplifier streaming using a software Codec. This solution implements an audio crystal to provide audio class I^2S accuracy on the master clock (0.5% error maximum, see the Serial peripheral interface section in the reference manual for details).

Figure 26. Complete audio player solution 1

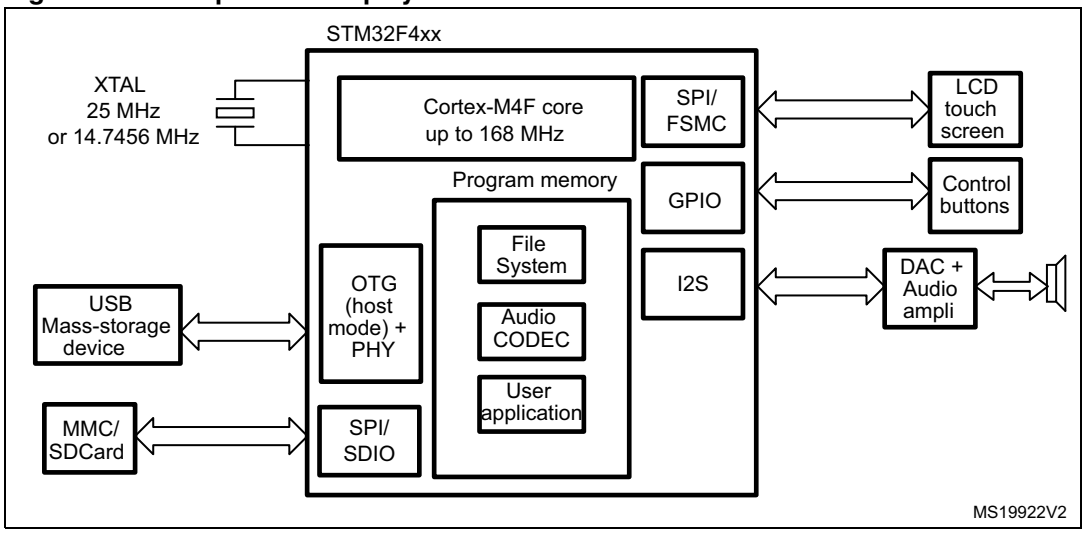


Figure 27 shows storage media to audio Codec/amplifier streaming with SOF synchronization of input/output audio streaming using a hardware Codec.

Figure 27. Complete audio player solution 2

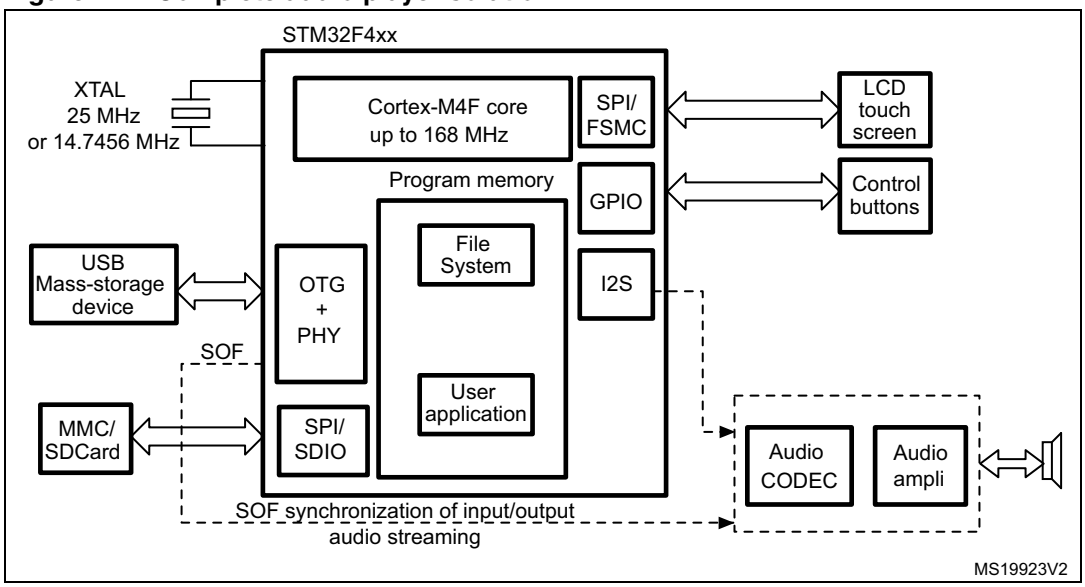


Figure 28. Audio player solution using PLL, PLLI2S, USB and 1 crystal

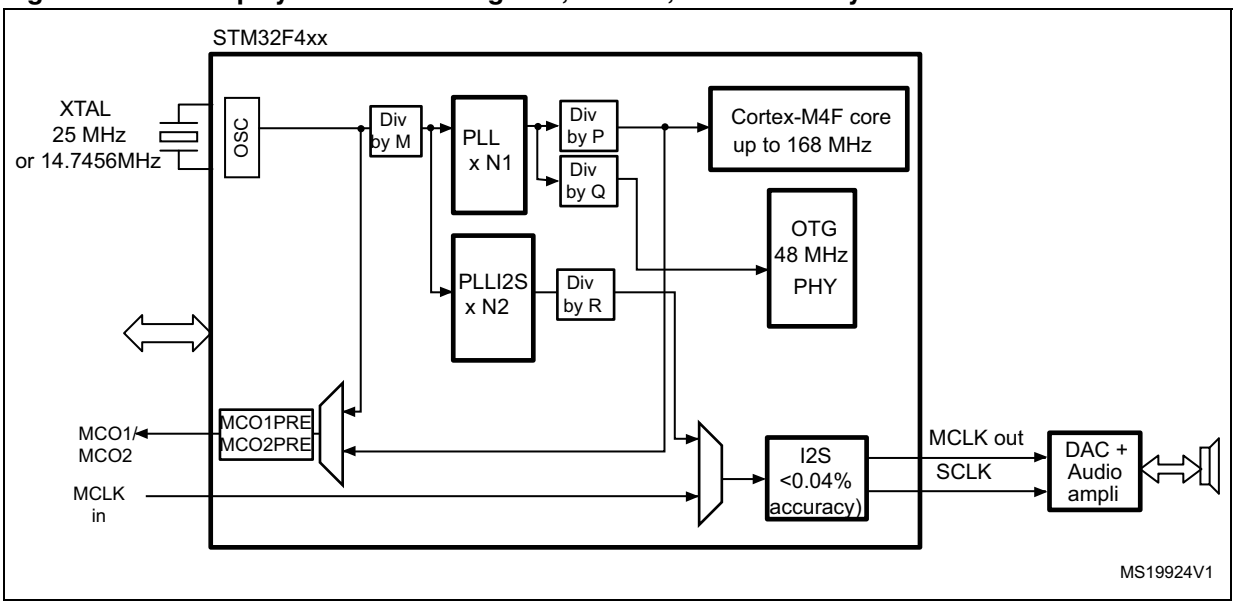


Figure 29. Audio PLL (PLLI2S) providing accurate I2S clock

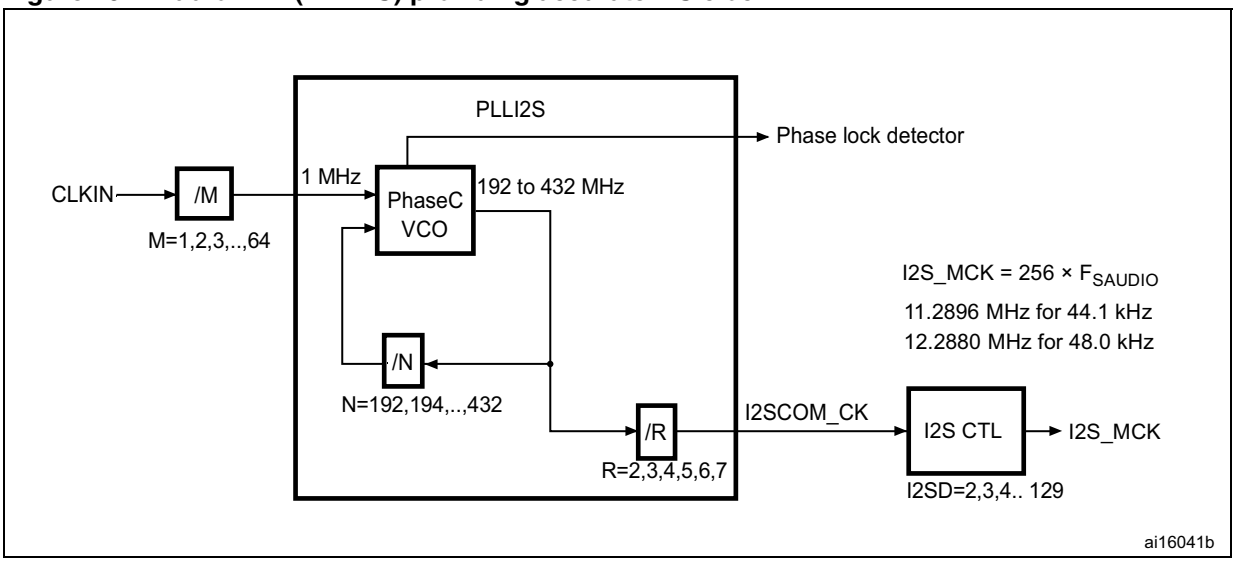
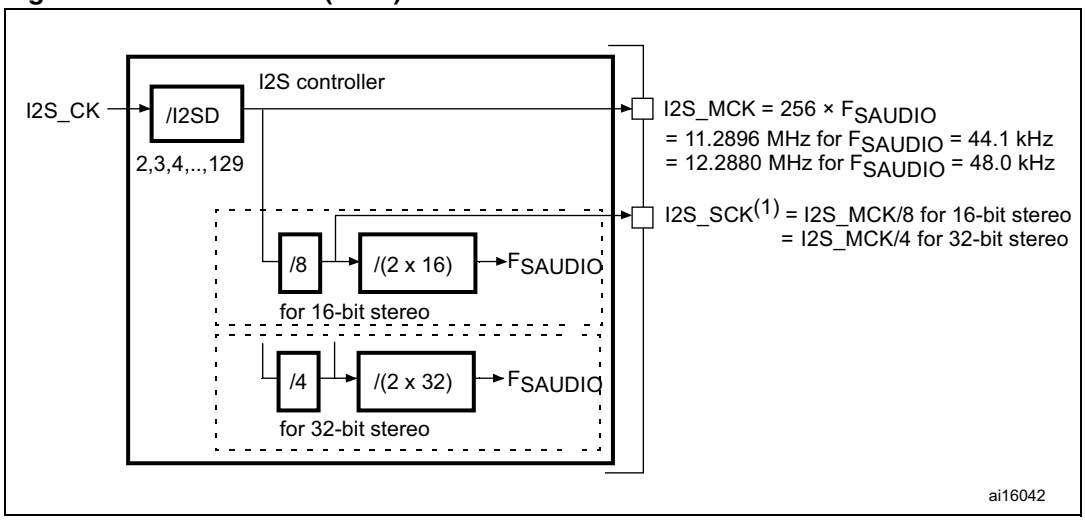
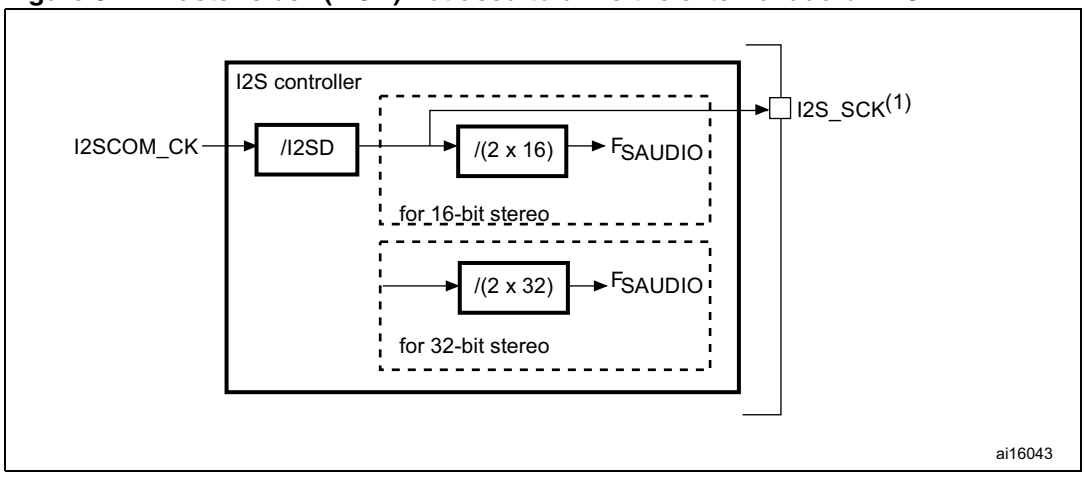


Figure 30. Master clock (MCK) used to drive the external audio DAC



1. I2S_SCK is the I2S serial clock to the external audio DAC (not to be confused with I2S_CK).

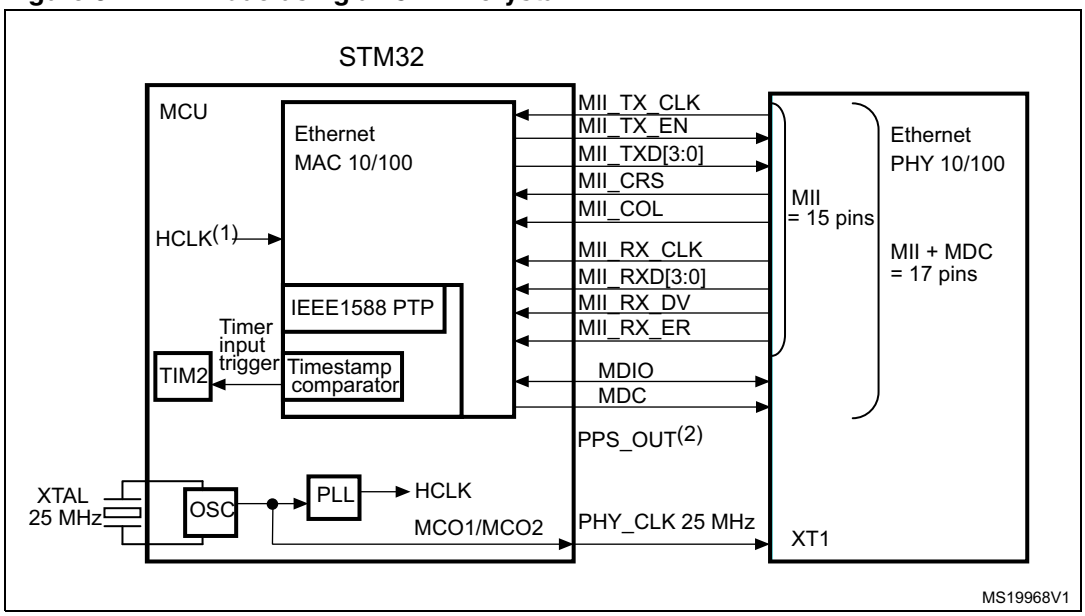
Figure 31. Master clock (MCK) not used to drive the external audio DAC



1. I2S_SCK is the I2S serial clock to the external audio DAC (not to be confused with I2S_CK).

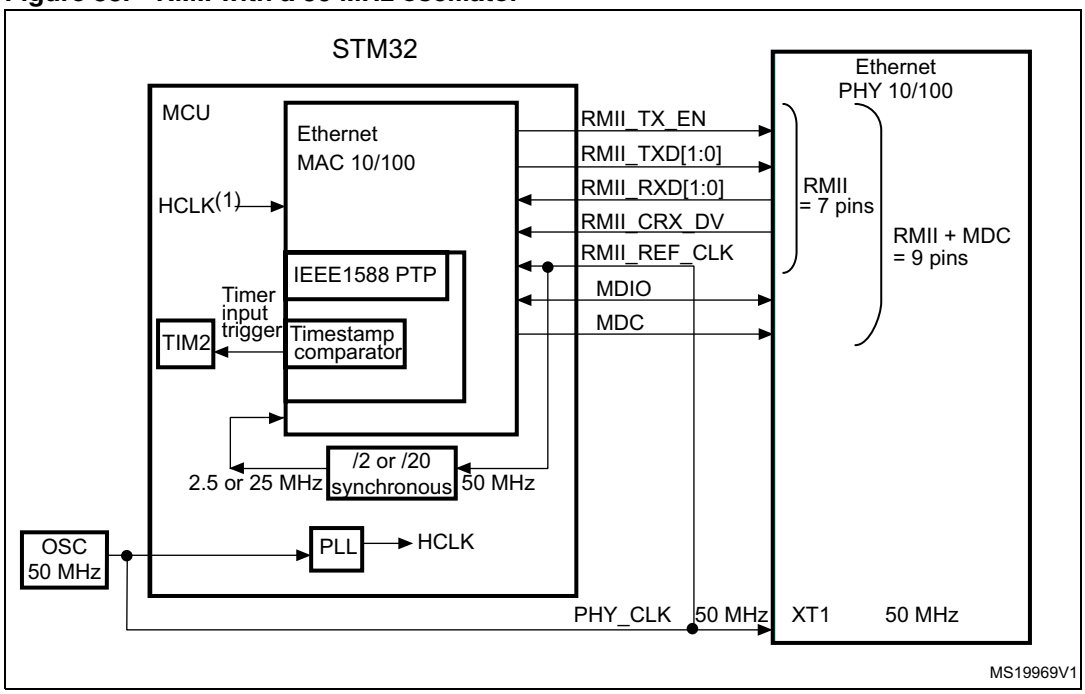
A.6 Ethernet interface solutions

Figure 32. MII mode using a 25 MHz crystal



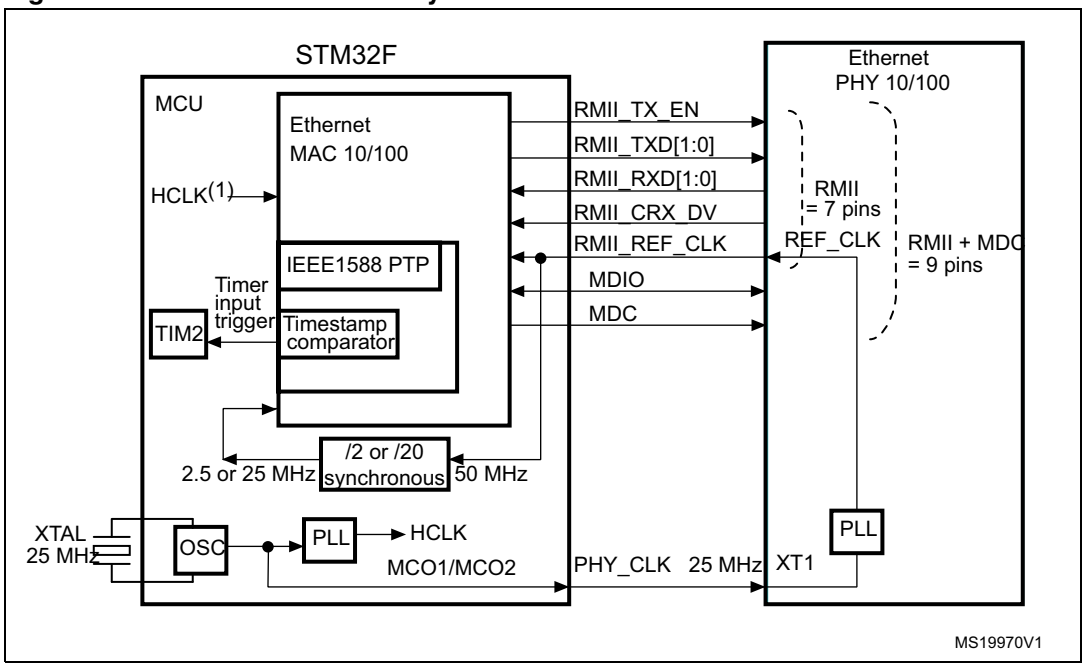
1. f_{HCLK} must be greater than 25 MHz.
2. Pulse per second when using IEEE1588 PTP optional signal.

Figure 33. RMII with a 50 MHz oscillator



1. f_{HCLK} must be greater than 25 MHz.

Figure 34. RMII with a 25 MHz crystal and PHY with PLL



1. f_{HCLK} must be greater than 25 MHz.
2. The 25 MHz (PHY_CLK) must be derived directly from the HSE oscillator, before the PLL block.

8 Revision history

Table 18. Full document revision history

Date	Revision	Changes
09-Nov-2012	1.0	Initial release.

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