TB-7V-2000T-LSI
Hardware User Manual

Rev.1.03

Revision History

Version	Date	Description	Publisher
Rev.1.00	2013/04/25	Release version	Amano
Rev.1.01	2013/06/21	Modify Table 8-28,Table 8-29,Figure 8-33	Amano
Rev.1.02	2013/08/02	Modify Table 8-7,Table 8-15,Table 8-23,Table 9-7,Table 9-17, Table 9-19	Amano
Rev.1.03	2013/08/12	Modify Table 9-19	Amano

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Introduction

Thank you for purchasing the **TB-7V-2000T-LSI** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, then always keep it handy.

SAFETY PRECAUTIONS

Be sure to observe these precautions

Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to assure correct use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to always keep it handy.**

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
Warning	Indicates the possibility of serious injury or death if the product is handled incorrectly.
Caution	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

Warning	
	**In the event of a failure, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.
	**If an unpleasant smell or smoking occurs, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.
	**Do not disassemble, repair or modify the product.** Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	**Do not touch a cooling fan.** As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.
	**Do not place the product on unstable locations.** Otherwise, it may drop or fall, resulting in injury to persons or failure.
	**If the product is dropped or damaged, do not use it as is.** Otherwise, a fire or electric shock may occur.
	**Do not touch the product with a metallic object.** Otherwise, a fire or electric shock may occur.
	**Do not place the product in dusty or humid locations or where water may splash.** Otherwise, a fire or electric shock may occur.
	**Do not get the product wet or touch it with a wet hand.** Otherwise, the product may break down or it may cause a fire, smoking or electric shock.
	**Do not touch a connector on the product (gold-plated portion).** Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Caution	
	Do not use or place the product in the following locations. • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Staticky locations • Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
	Do not place heavy things on the product. Otherwise, the product may be damaged.

■ Disclaimer

This product is a board intended for evaluation of Xilinx FPGA, Virtex-7 and Kintex-7 functions. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

(1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
(2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
(3) Use of this product against the instructions given in this manual.
(4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

(1) Erasure or corruption of data arising from use of this product.
(2) Any consequences or other abnormalities arising from use of this product, or
(3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.

1. Related Documents and Accessories

Related Documents:

All documents relating to this board can be downloaded from our website. Please see attached paper on the products.

Xilinx FPGA document: http://japan.xilinx.com/support/

DS180: 7 Series Overview

UG473: 7 Series FPGAs Memory Resources User Guide

UG474: 7 Series FPGAs Configurable Logic Block User Guide

UG471: 7 Series FPGAs SelectIO Resources User Guide

UG472: 7 Series FPGAs Clocking Resources User Guide

UG470: 7 Series FPGAs Configuration User Guide

UG476: 7 Series FPGAs GTX/GTH Transceivers User Guide

UG480: 7 Series FPGAs XADC User Guide

PG054: 7 Series FPGAs Integrated Block v1.7 for PCI Express Product Guide (AXI)

UG475: 7 Series FPGAs Packaging and Pinout Specifications

Board Fixtures:

74.25MHz Oscillator (Mita Denpa: MXO-50B 74.25MHz), X2 IC socket)

DVI Rx Serial EEPROM (Microchip: 24LC16B-I/P)

CYUSB3014 (USB3.0 Controller) Serial EEPROM (Microchip: 24LC256-E/P)

FAN/Heat Sink

Kintex-7 325T FAN/ Heat Sink (ALPHA: FS40-15M42: x1

Board Foot Set

Rubber foot: 27, M3 x6 screws: 54, M3 x10 spacers: 27

Short-circuit socket (SAMTEC: 2SN-BK-G): 66

Accessories:

FAN/Heat Sink

Virtex-7 2000T FAN/heat sink (ALPHA: S08BMJ05): 1, TIM: 1

SD card (2GB), Adaptor

QTH-FMC conversion board (2 sets of TB-OP-FMCL L/R2): 1

Conversion board and Option Board fixing spacer set

M2.6x8.5 spacer: 4, M2.6x19 spacer: 8, M2.6x27 spacer: 8, M2.6x10 screw with washer: 12

Switching power supply (Cosel: PLA600F-12 with a power supply cable: 1

2. Overview

The TB-7V-2000T-LSI board is an LSI development platform equipped with Xilinx FPGA Virtex-7 Series “2000T” and Kintex-7 Series “325T”.

The TB-7V-2000T-LSI board is also equipped with speed grade "-2" FPGA (XC7V2000T-2FLG1925) and speed grade "-2" FPGA (XC7K325T-2FFG900).

3. Feature

FPGA :	Virtex-7 FPGA “XC7V2000T-2FLG1925”
	Kintex-7 FPGA “XC7K325T-2FFG900”
	Spartan-3AN FPGA “XC3S700AN-4FGG484C” for configuration only.
Connectors :	Samtec QTH connectors (120pin) x5
	FMC HPC x1 (TED TB-FMCH-VBY1 only)(*1)
Memory :	1600Mbps DDR3 SDRAM 2Gbit x8
	Address shard connection 16 bit data width x2, 4set
Interfaces :	DVI TX/RX single mode, Max 165MHz pixel clock
	USB2.0/3.0 (device mode) Type B connector
	PCIexpress Gen2 x8, 1 connector
	UART RS-232C Dsub9pin
Clock(Virtex-7/Kintex-7):	
	74.25MHz OSC on the socket.
Clock(Virtex-7) :	200MHz for DDR3 memory controller
	250MHZ for PCIexpress interface
	50MHz for XC3S700AN configuration controller
	MMCX single-end/differential, input/output
	OSC socket x3 (used one socket for 74.25MHz OSC)
Clock(Kintex-7) :	250MHz for SERDES reference clock
Configuration Method	
Virtex7 :	Configuration from Spartan3AN, microSD card and NAND Flash Memory, JTAG
Kintex-7 :	QSPI Flash Memory, JTAG
Other peripherals	
	LED
	Dip Switch
	Push Switch
	Pin Header
Power Supply :	ATX 12V
Cooling :	FAN, Heat sink

(*1)

Because of available number of pins on FPGA, all pins defined for the FMC connector are not connected. For details, refer to the connector pin layout table contained in this manual.

4. Block Diagram

4.1. Block diagram of TB-7V-2000T-LSI

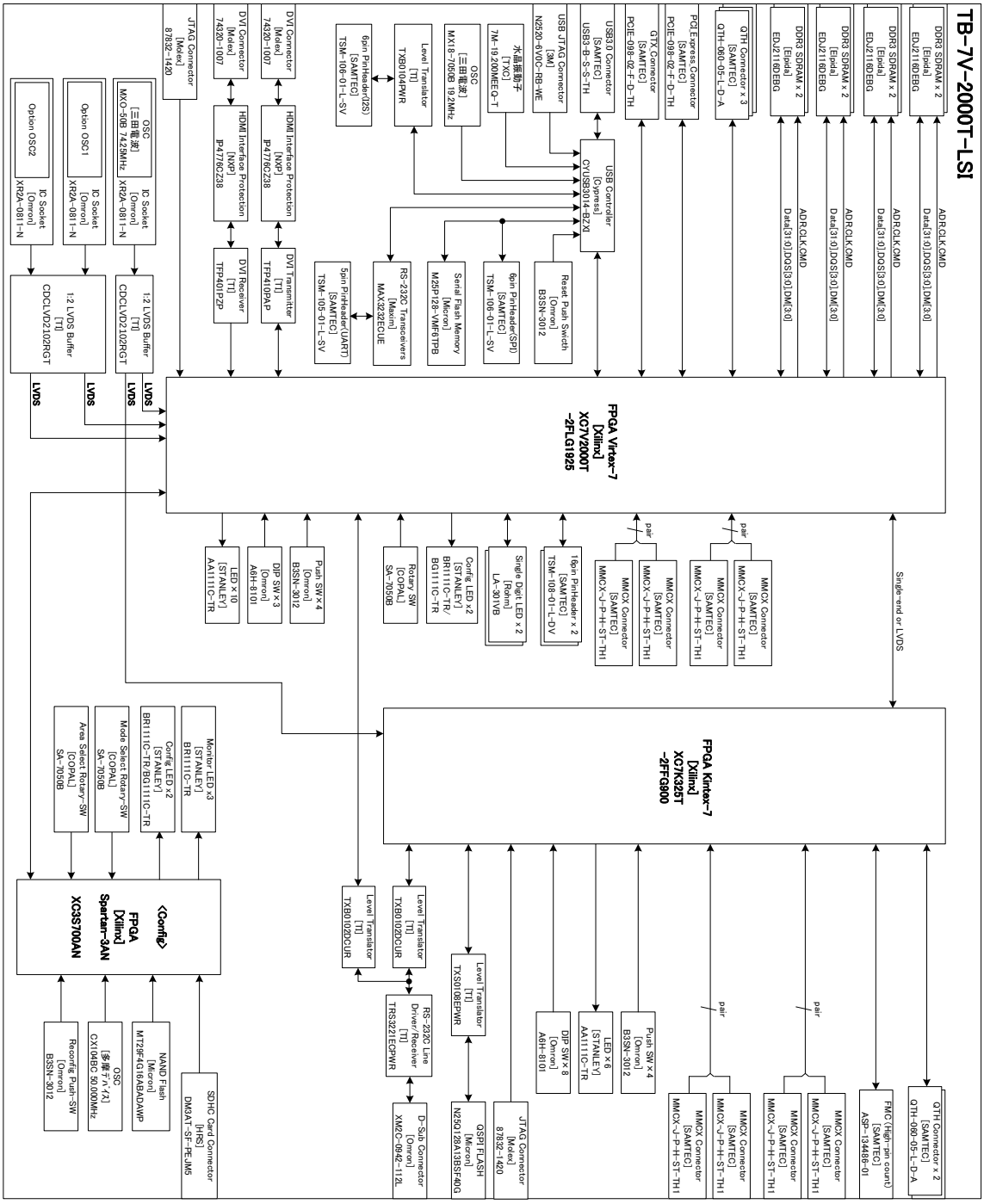


Figure 4-1 Block Diagram

4.2. FPGA Bank Assgin

The following subsections describes the FPGA bank assignments.

4.2.1. Bank assign of XC7V2000T

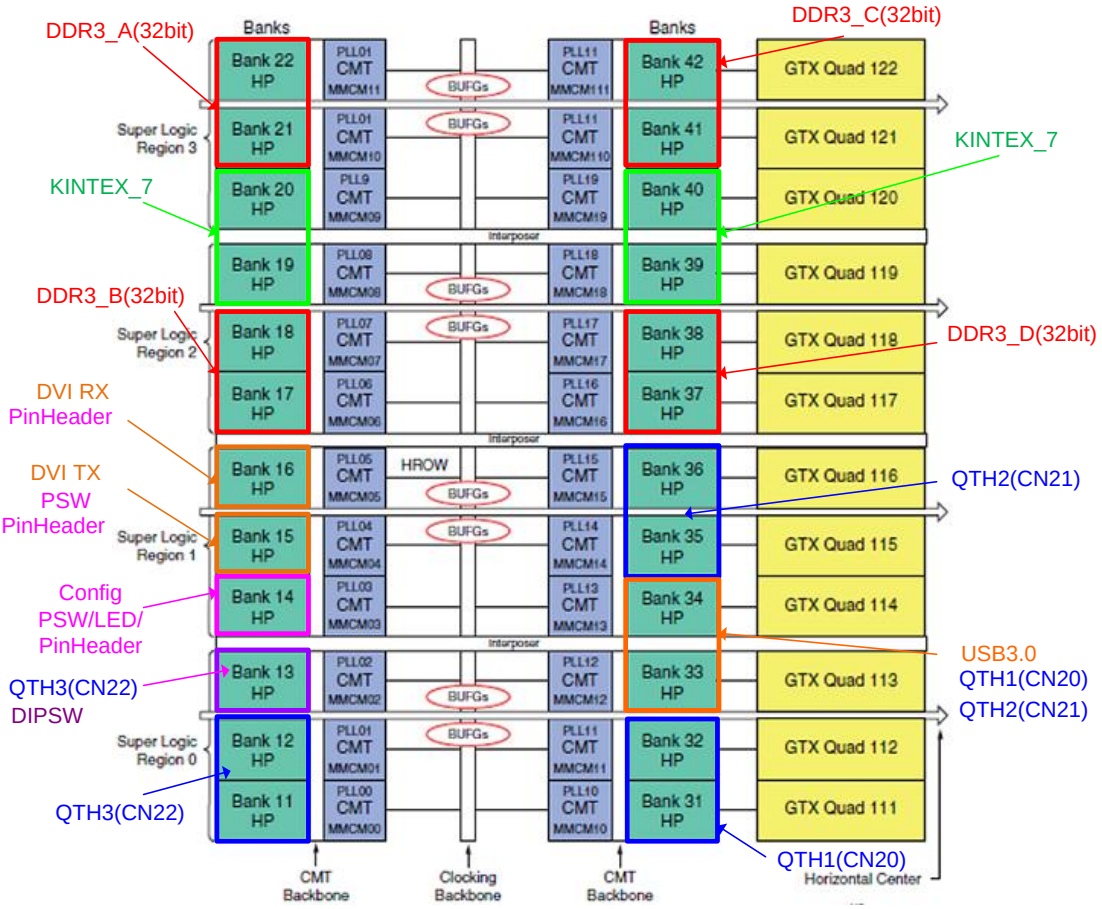


Figure 4-2 Bank Assignments of XC7V2000T

4.2.2. Bank assignments of XC7K325T

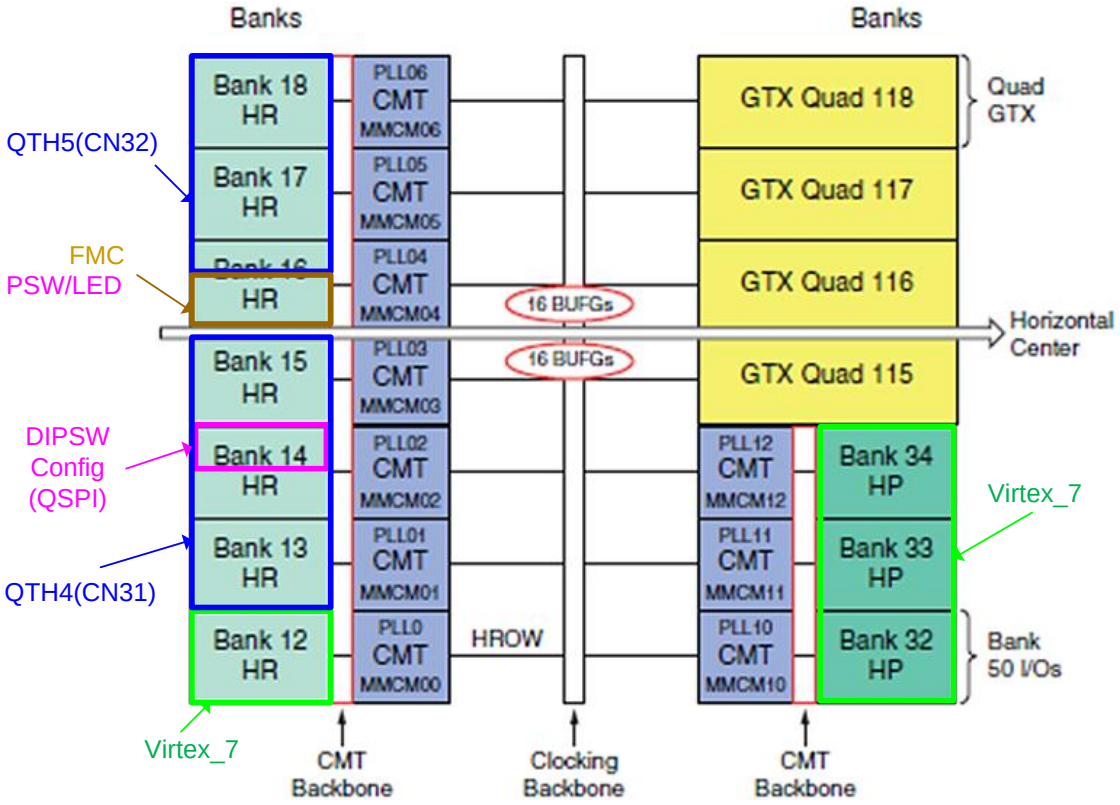


Figure 4-3 Bank Assignments of XC7K325T

5. External View of the Board

Figures 5-1 and 5-2 show the external view of the TB-7V-2000T-LSI board.

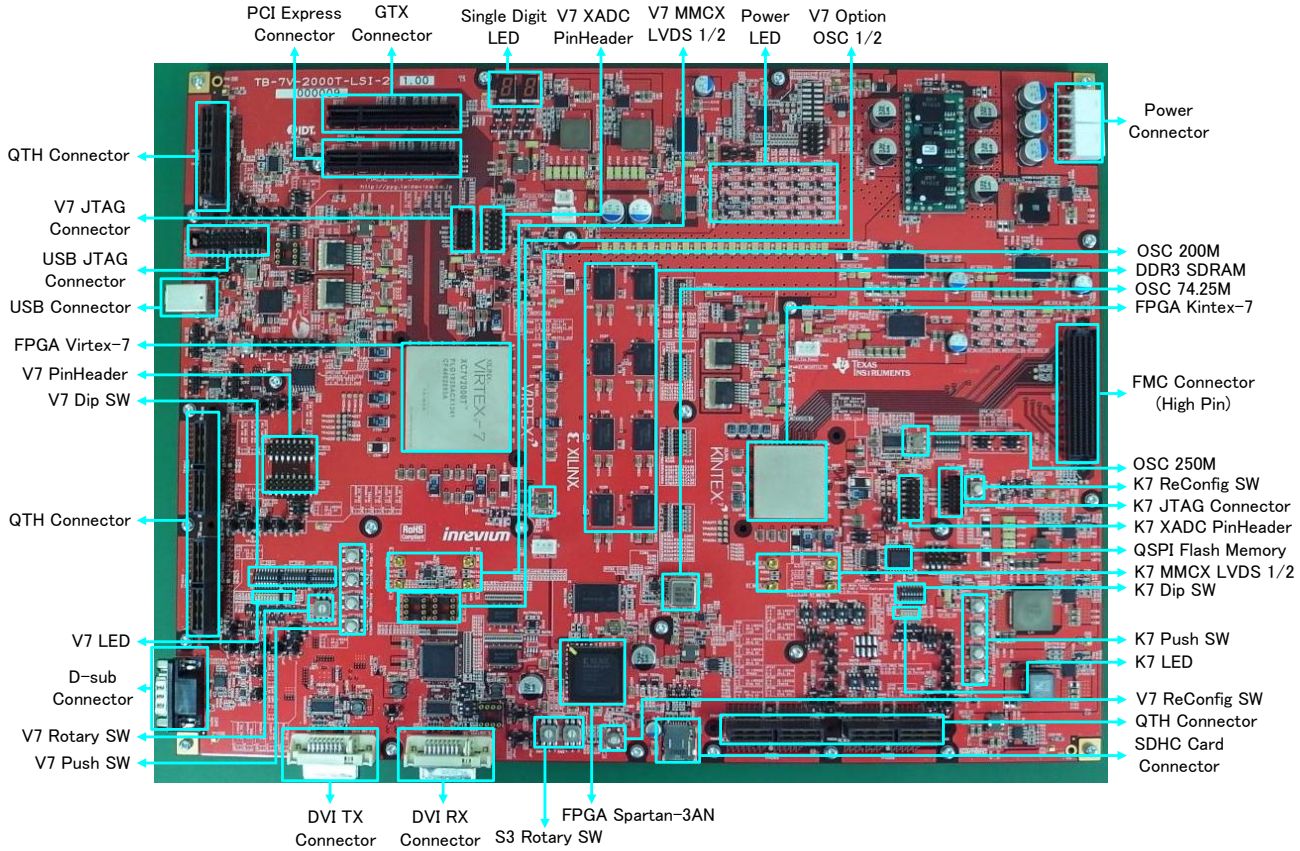


Figure 5-1 Component Side

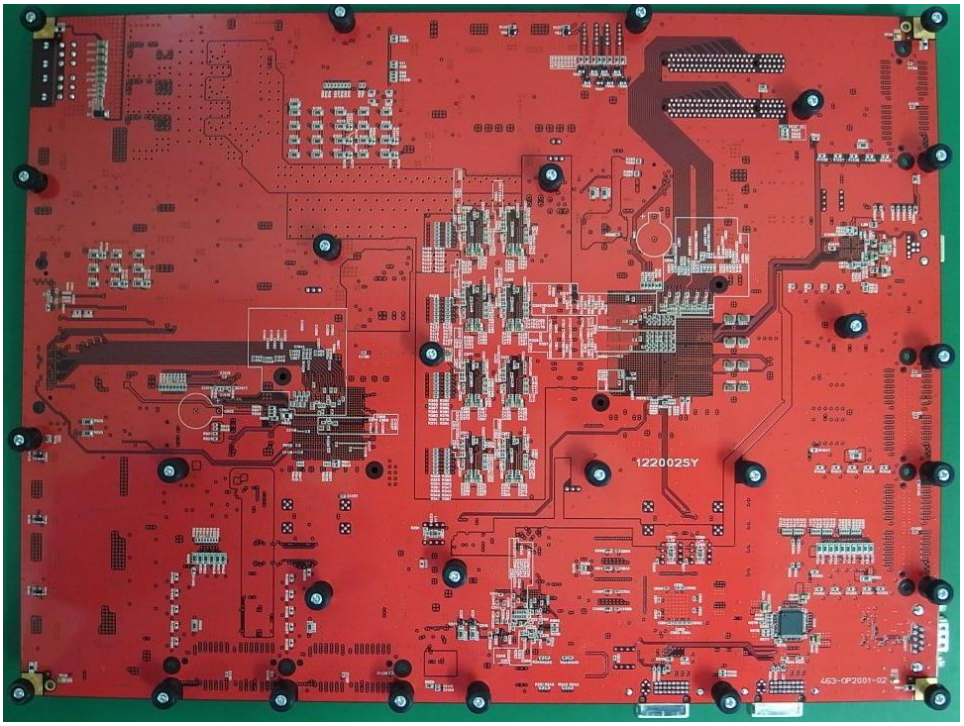


Figure 5-2 Solder Side

6. Board Specifications

The following shows the board specifications.

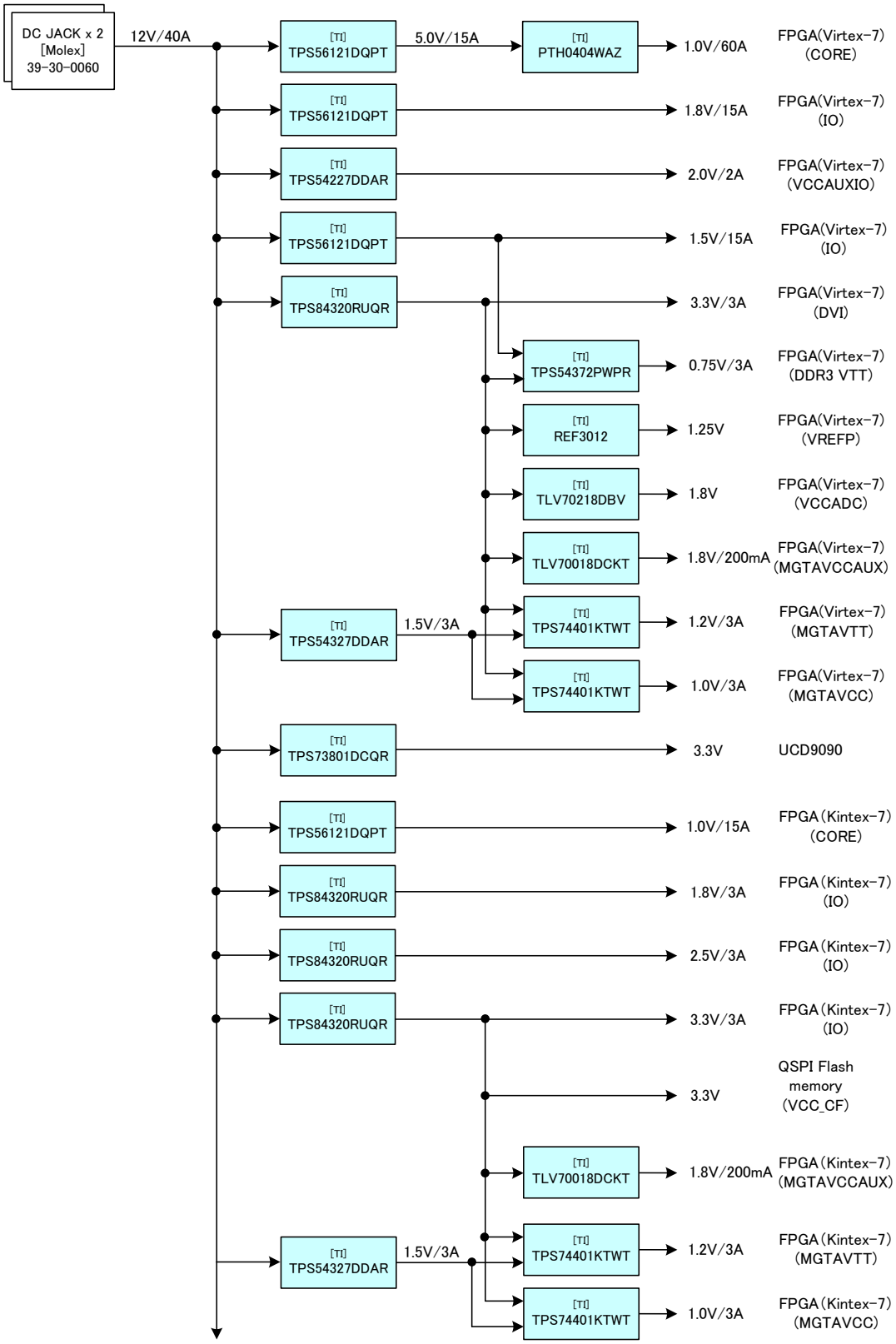
External dimensions: W:400.00mm x H:300.00mm
Number of layers: 20
Board Thickness: 2.4mm
Material: FR-5 or equivalent
Weight: About 1.2kg (excluding FAN/heat sink and power supply)

*For board dimensions, refer to Appendix " TB-7V-2000T-LSI Board Dimensions.pdf".

7. Power Supply/Clock (Virtex-7/Kintex-7)

7.1. Power Supply Structure

Figure 7-1 shows the internal power supply structure.



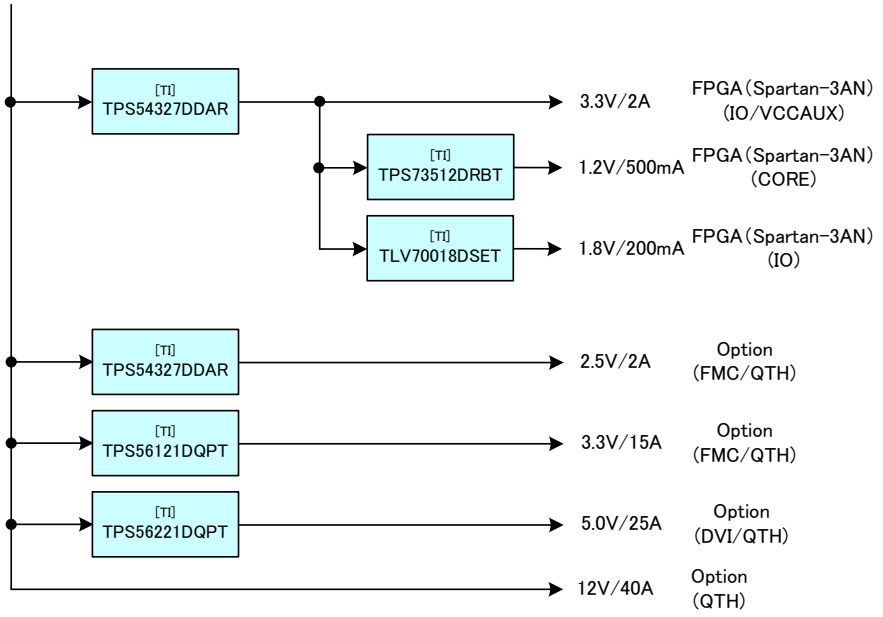


Figure 7-1 Power Supply Structure

7.1.1. Power Input

Power is supplied through the ATX connector.

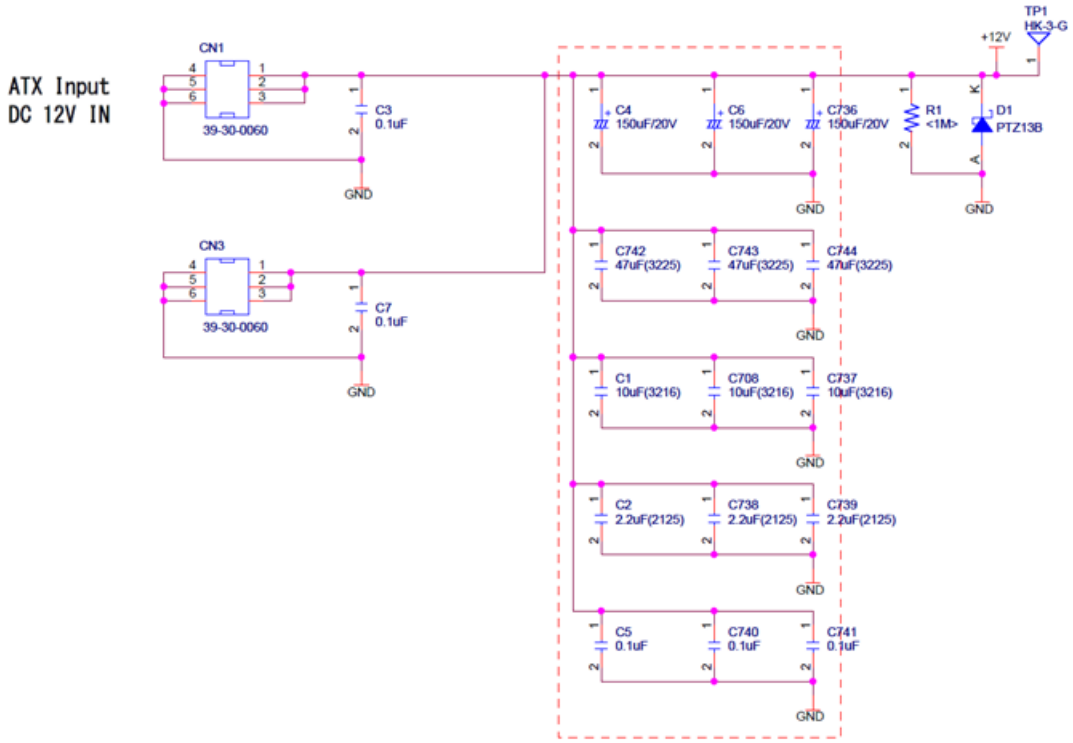


Figure 7-2 Power Supply Structure

7.1.2. Power Supply Status Checking

The current status of power supplies can be verified on the following power status LEDs (if the power status LED is blinking and continuously red, the power supply is functional).

In the following table, V7 refers to Virtex-7, K7 to Kintex-7 and S3 to Spartan-3AN.

Table 7-1 Power Status LEDs (Virtex-7/Spartan-3AN)

Power	LED	Status	Voltage	Color
V7_VCC+5.0V	LED17	Power source for V7_ VCCINT+1.0V	+5.0V	RED
V7_VCC+3.3V	LED18	Power source for V7_MGTVCCAUX+1.8V	+3.3V	RED
S3_VCC+3.3V	LED19	Power source for S3_VCC+1.8V Power source for S3_VCC+1.2V S3_VCCIO / S3_VCCAUX	+3.3V	RED
OP+2.5V	LED20	QTH/FMC 2.5V	+2.5V	RED
V7_ VCCINT+1.0V	LED21	V7 VCCINT / V7 VCCBRAM	+1.0V	RED
V7_MGT_PW+1.5V	LED22	Power source for V7_MGTAVTT+1.2V Power source for V7_MGTAVCC+1.0V	+1.5V	RED
S3_VCC+1.8V	LED23	S3 VCCIO	+1.8V	RED
OP+3.3V	LED24	QTH/FMC 3.3V	+3.3V	RED
V7_MGTVCCAUX+1.8V	LED25	V7 MGTVCCAUX	+1.2V	RED
S3_VCC+1.2V	LED26	S3 VCCINT	+1.2V	RED
OP+5.0V	LED27	QTH/DVI	+5.0V	RED
V7_VCC+1.5V	LED28	V7 VCCO	+1.5V	RED
V7_VTT+0.75V	LED29	V7 VREF(DDR3)	+0.75V	RED
V7_MGTAVTT+1.2V	LED30	V7 MGTAVTT	+1.2V	RED
UCD9090_+3.3V	LED31	UCD9090RGZT	+3.3V	RED
+12V	LED32	12V Power Input	+12V	RED
V7_VCC+1.8V	LED33	V7 VCCIO	+1.8V	RED
V7_MGTAVCC+1.0V	LED34	V7 MGTAVCC	+1.0V	RED
V7_VCCAUXIO+2.0V	LED48	V7 VCCAUX IO	+2.0V	RED
V7_VCCADC+1.8V	LED66	V7 VCCADC	+1.8V	RED
V7_ VREFP+1.25V	LED67	V7 VREFP	+1.25V	RED

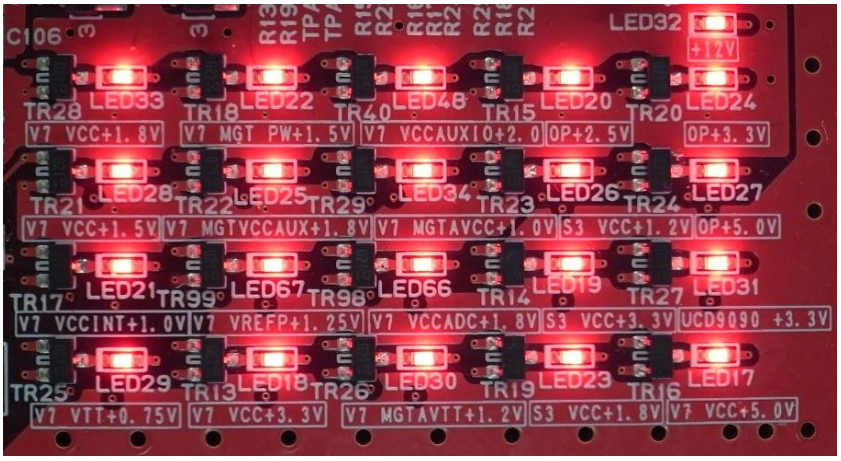


Figure 7-3 Power Status LEDs (Virtex-7/Spartan-3AN)

Table 7-2 Power Status LED (Kintex-7)

Power	LED	Status	Voltage	Color
K7_ VCCINT+1.0V	LED49	K7 VCCINT	+1.0V	RED
K7_ VCC+2.5V	LED50	K7 VCCIO	+2.5V	RED
K7_ MGTAVTT+1.2V	LED51	K7 MGTAVTT	+1.2V	RED
K7_ VCC_CF	LED52	QSPI Flash Memory		RED
K7_ VCC+3.3V	LED53	K7 VCCIO	+3.3V	RED
K7_ MGTAVCC+1.0V	LED54	K7 MGTAVCC	+1.0V	RED
K7_ VCC+1.8V	LED55	K7 VCCIO	+1.8V	RED
K7_MGT_PW+1.5V	LED56	Power source for K7_MGTAVTT+1.2V Power source for K7_MGTAVCC+1.0V	+1.5V	RED
K7_ MGTVCCAUX+1.8V	LED57	K7 MGTVCCAUX	+1.8V	RED

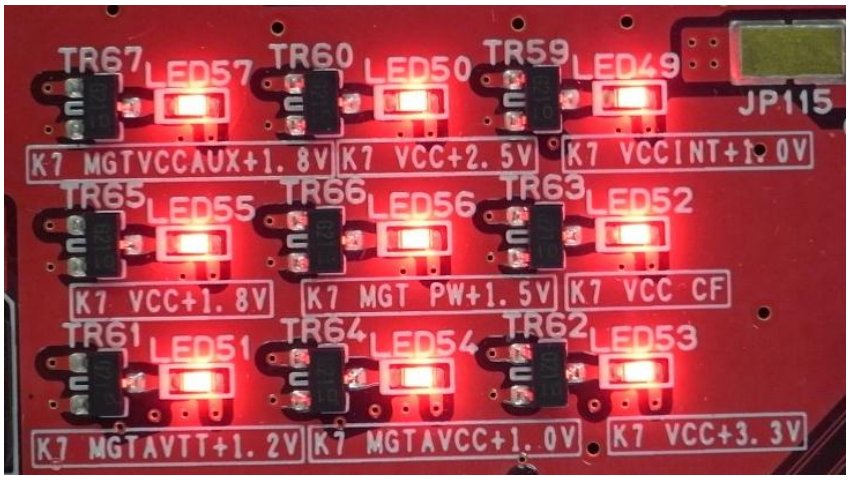


Figure 7-4 Power Sutatus LEDs (Kintex-7)

7.1.3. Kintex-7 FPGA Bank Voltage Selection

The following peripheral devices shown in Figure 7-5 are connected to the Kintex-7.

The QTH and FMC connectors allow the developers to select an appropriate KIntex-7 bank voltage (VCCIO) by setting onboard jumpers (JP94/95/102) to meet the voltage requirements (1.8V, 2.5V or 3.3V) of the connected interfaces. Note that the Virtex-7 has a fixed voltage of 1.8V (no bank voltage selection).

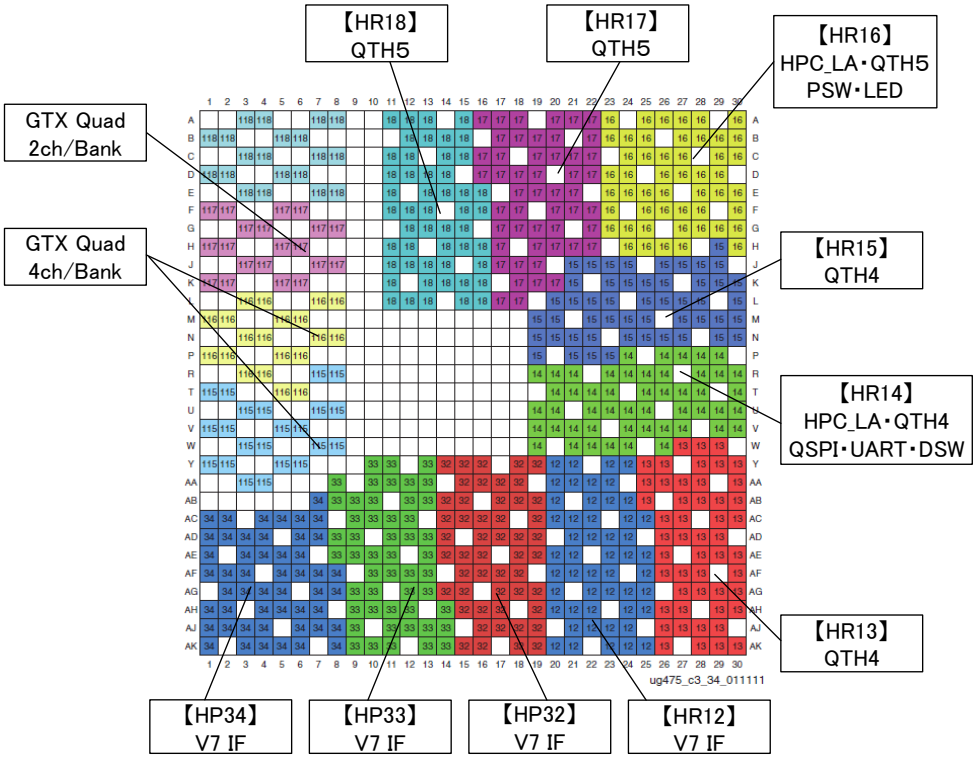


Figure 7-5 Kintex-7 Banks and Peripheral Devices

Table 7-3 Kintex-7 Bank – Peripheral Device Voltage Selection

Bank	Connected Device	Voltage	Voltage Selection			
			JP No.	1.8V	2.5V	3.3V
HR13/14/15	FMC_HPC(CN34) QTH4(CN31) QSPI,DSW, UART	Variable (1.8V/2.5V/3.3V)	JP94	1-2	3-4	5-6uit
			JP102	1-2	3-4	5-6
HR16/17/18	FMC_HPC(CN34) QTH5(CN32) LED,PSW	Variable (1.8V/2.5V/3.3V)	JP95	1-2	2-3	5-6

Be sure to set JP94 and JP102 to the same pin settings.

By default all the above voltage setting is set to 1.8V.

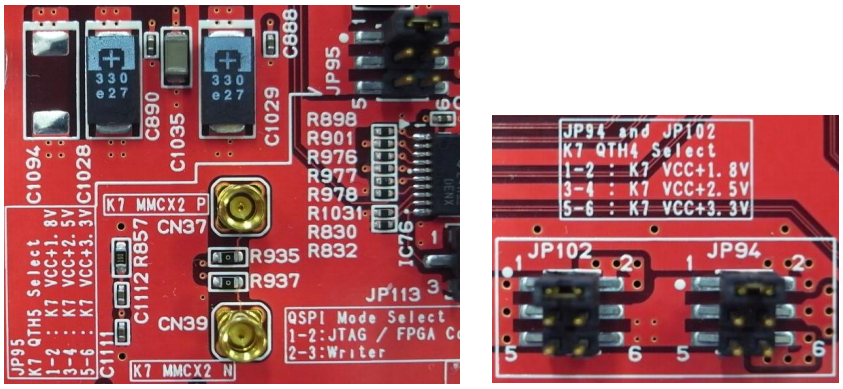


Figure 7-6 Bank Voltage Setting Location on FPGA (Kintex-7)

7.1.3.1. XADC Power Supply on Virtex-7

VCCADC (XADC analog circuit power supply) can be supplied either at V7_VCC+1.8V or V7_VCCADC+1.8V. This supply voltage selection is made using JP39.

VREFP (differencial reference voltage to the A/D conversion process) can be supplied either at V7_XADC_AGND or V7_VREFP+1.25V. This supply voltage selection is made using JP40.

Table 7-4 VCCADC/VREFP Voltage Selection on Virtex-7

Power Supply	JP Setting		Supply Voltage
VCCADC	JP39	1-2	V7_VCC+1.8V
		2-3	V7_VCCADC+1.8V
VREFP	JP40	1-2	V7_XADC_AGND
		2-3	V7_VREFP+1.25V

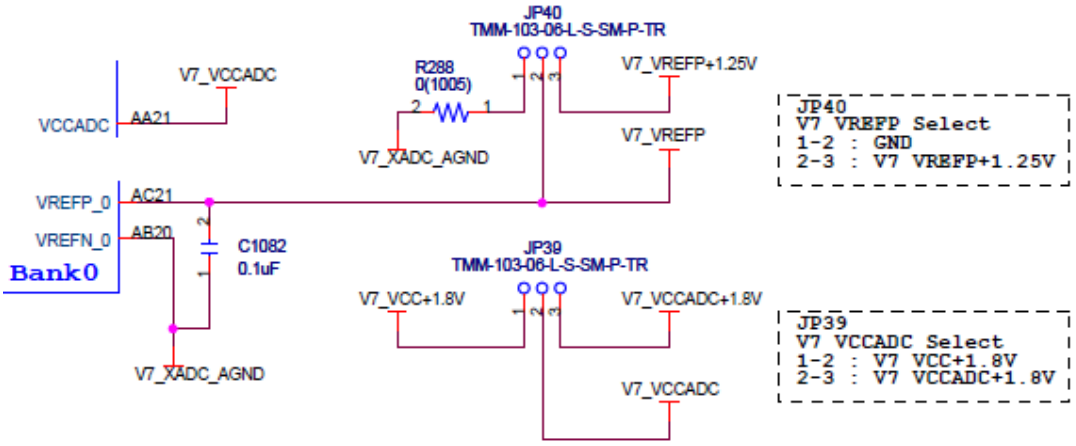


Figure 7-7 VCCADC/VREFP Voltage Selection on Virtex-7

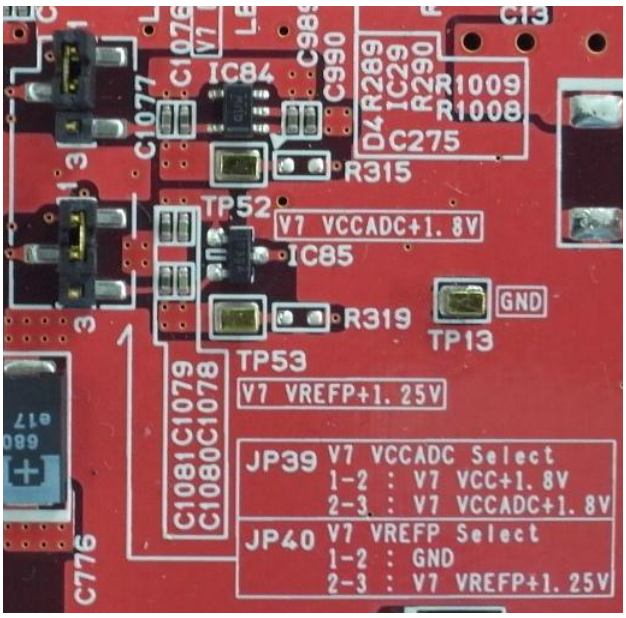


Figure 7-8 VCCADC/VREFP Selection Location on Virtex-7

7.1.3.2. XADC Power Supply on Kintex-7

VCCADC (XADC analog circuit power supply) can be supplied either from a K7_VCC+1.8V or CN28 9pin. This supply voltage selection is made using JP92.

VREFP (differential reference voltage to the A/D conversion process) can be supplied either from a V7_XADC_AGND or CN28 11pin. This supply voltage selection is made using JP93.

Table 7-5 VCCADC/VREFP Selection on Kintex-7

Power Supply	JP Setting		Supply Voltage
VCCADC	JP92	1-2	K7_VCC+1.8V
		2-3	CN28 9pin
VREFP	JP93	1-2	K7_XADC_AGND
		2-3	CN28 11pin

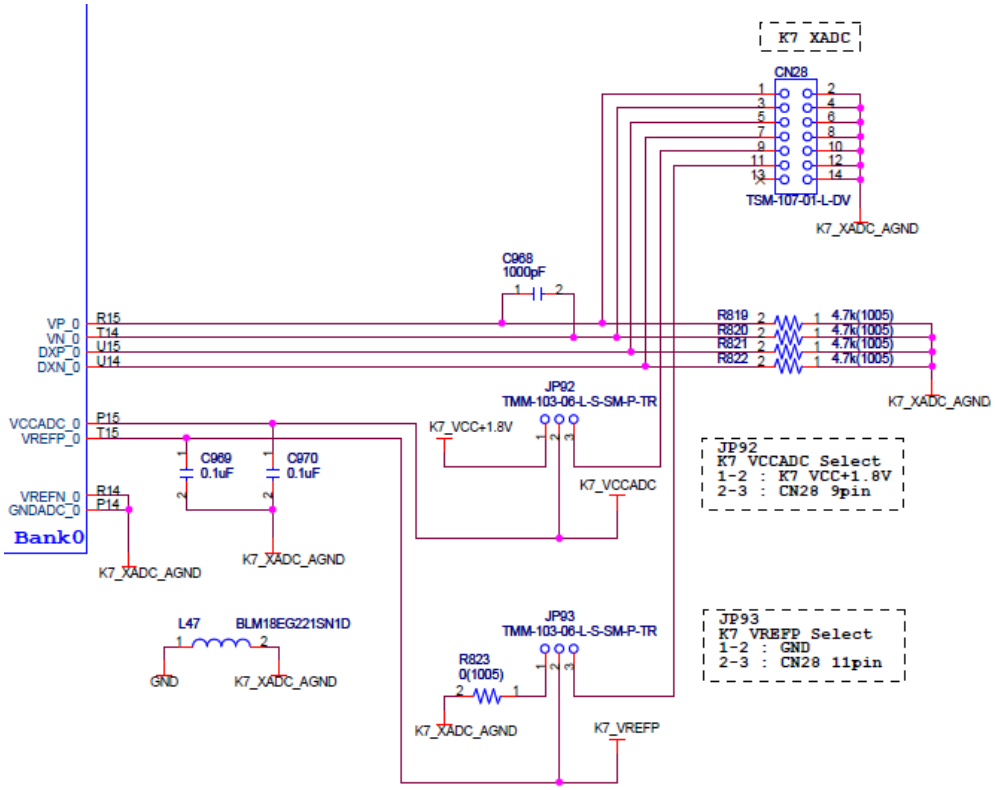


Figure 7-9 VCCADC/VREFP Selection on Kintex-7

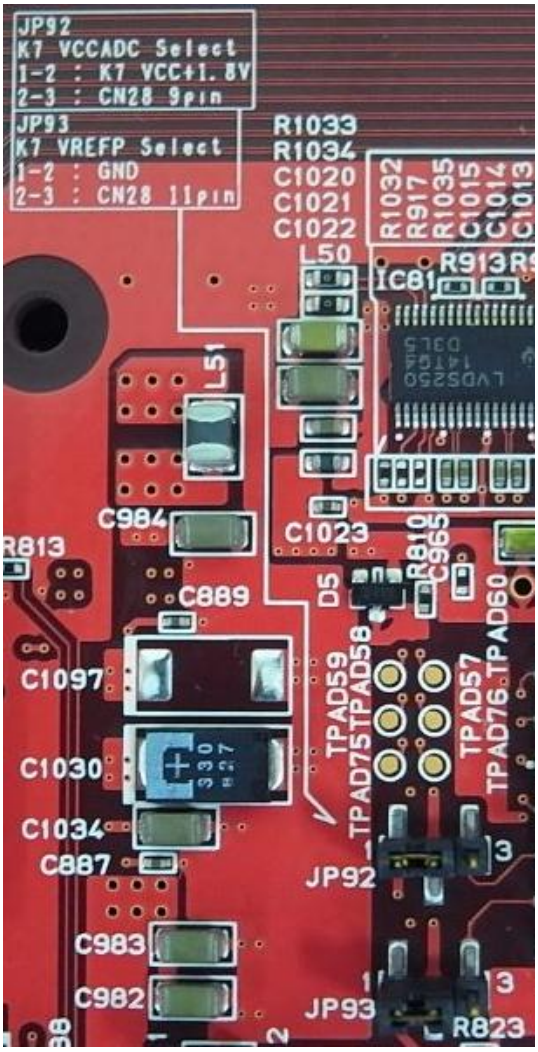


Figure 7-10 VCCADC/VREFP Selection Location on Kintex-7

7.1.4. PM Bus Interface (CN5)

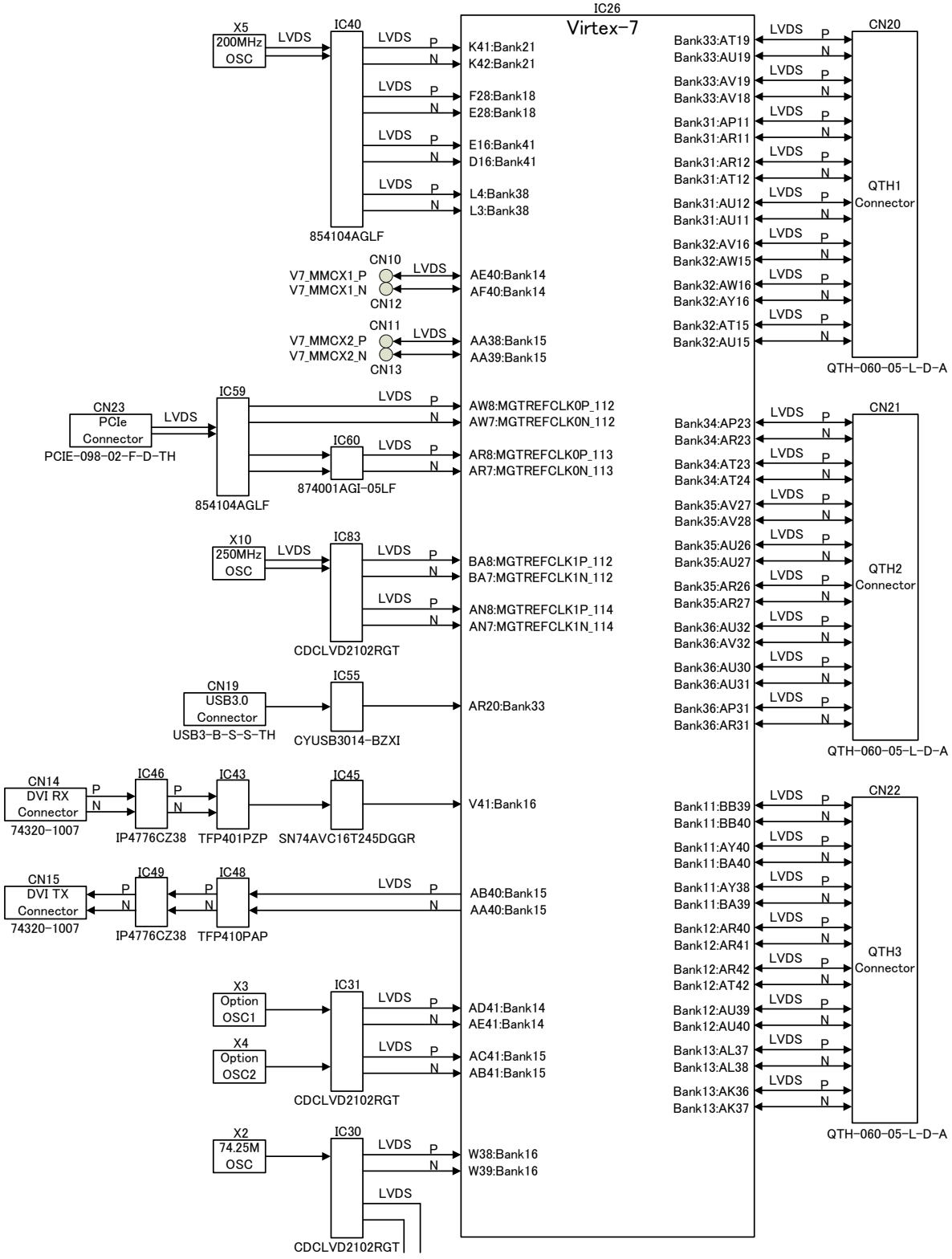
PM Bus Interface is used to configure the TI UCD9090 (power supply sequence and management) chip. For information about PM Bus, refer to the UCD9090 data sheet.

The TB-7V-2000T-LSI board has the already configured default PM Bus Interface to meet the FPGA specification requirements (no need to change the configuration).

For information about FPGA power supply sequence, refer to the relevant data sheet.

7.2. Clock Source

The TB-7V-2000T-LSI board provides the clock sources as shown in Figure 7-11.



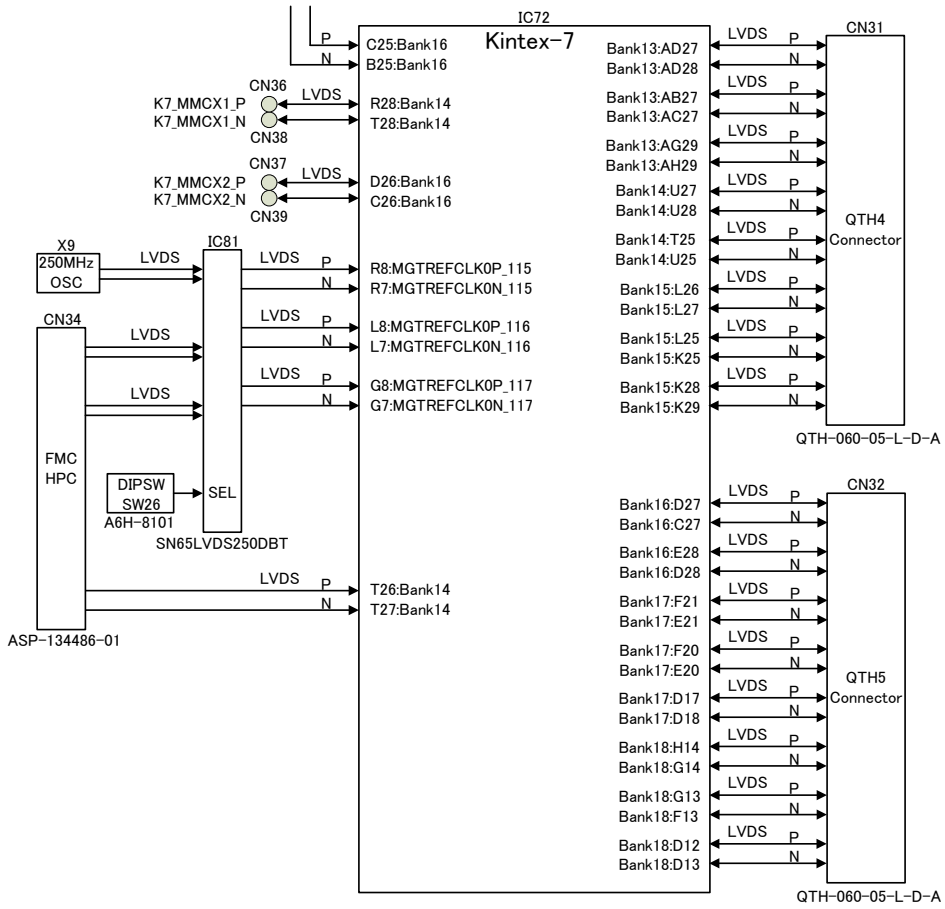


Figure 7-11 Clock Structure

Table 7-6 Clock Source

Connection	Signal Name	I/F	Pin No.	Remarks
X5(200MHz)	DDR3A_200MHz_P/N	LVDS	K41/K42	Via 1to4 buffer, DDR3 clock (system, iodelayctrl)
X5(200MHz)	DDR3B_200MHz_P/N	LVDS	F28/E28	Via 1to4 buffer, DDR3 clock (system, iodelayctrl)
X5(200MHz)	DDR3C_200MHz_P/N	LVDS	E16/D16	Via 1to4 buffer, DDR3 clock (system, iodelayctrl)
X5(200MHz)	DDR3D_200MHz_P/N	LVDS	L4/L3	Via 1to4 buffer, DDR3 clock (system, iodelayctrl)
X2(74.25MHz)	V7_CLK74M_P/N	LVDS	W38/W39	Via 1to2 differential buffer Virtex-7 clock
X3(Option OSC1)	V7_OSC1_P/N	LVDS	AD41/AE41	Via 1to2 differential buffer Virtex-7 clock
X4(Option OSC2)	V7_OSC2_P/N	LVDS	AC41/AB41	Via 1to2 differential buffer Virtex-7 clock

Connection	Signal Name	I/F	Pin No.	Remarks
CN10/12	V7_MMCX1_P/N	LVDS	AE40/AF40	Virtex-7 MMCX external clock
CN11/13	V7_MMCX2_P/N	LVDS	AA38/AA39	Virtex-7 MMCX external clock
X10(250MHz)	V7_CLK250M1_P/N	LVDS	BA8/BA7	Via 1to2 buffer MGT reference clock
X10(250MHz)	V7_CLK250M2_P/N	LVDS	AN8/AN7	Via 1to2 buffer MGT reference clock
CN23 (PCIe Connector)	PCIE_CLK100M_P/N	LVDS	AW8/AW7	Via 1to4 buffer MGT reference clock
CN23 (PCIe Connector)	PCIE_CLK125M_P/N	LVDS	AR8/AR7	Via 1to4 buffer and PCIe Jitter Attenuator MGT reference clock
CN19 (USB3.0 Connector)	USB_PCLK	CMOS	AR20	USB3.0 clock
CN14 (DVI_RX Connector)	V7_DVI_R_CLK	CMOS	V41	DVI_RX clock
CN15 (DVI_TX Connector)	DVI_T_CLK DVI_T_CLKN	LVDS	AB40 AA40	DVI_TX clock
CN20 (QTH1 Connector)	S1_LVDS_CLK0_P/N S1_LVDS14_CLK_P/N S1_LVDS15_CLK_P/N S1_LVDS30_CLK_P/N S1_LVDS31_CLK_P/N S1_LVDS46_CLK_P/N S1_LVDS47_CLK_P/N S1_LVDS_CLK1_P/N	LVDS	AR12/AT12 AP11/AR11 AU12/AU11 AV16/AW15 AW16/AY16 AT15/AU15 AT19/AU19 AV19/AV18	QTH1 IF clock
CN21 (QTH2 Connector)	S2_LVDS_CLK0_P/N S2_LVDS14_CLK_P/N S2_LVDS15_CLK_P/N S2_LVDS30_CLK_P/N S2_LVDS31_CLK_P/N S2_LVDS46_CLK_P/N S2_LVDS47_CLK_P/N S2_LVDS_CLK1_P/N	LVDS	AU26/AU27 AV27/AV28 AR26/AR27 AU32/AV32 AU30/AU31 AP31/AR31 AP23/AR23 AT23/AT24	QTH2 IF clock
CN22 (QTH3 Connector)	S3_LVDS_CLK0_P/N S3_LVDS14_CLK_P/N S3_LVDS15_CLK_P/N S3_LVDS30_CLK_P/N S3_LVDS31_CLK_P/N S3_LVDS46_CLK_P/N	LVDS	AY40/BA40 BB39/BB40 AY38/BA39 AR40/AR41 AR42/AT42 AU39/AU40	QTH3 IF clock

Connection	Signal Name	I/F	Pin No.	Remarks
CN22 (QTH3 Connector)	S3_LVDS47_CLK_P/N S3_LVDS_CLK1_P/N	LVDS	AL37/AL38 AK36/AK37	QTH3 IF clock
X2(74.25MHz)	K7_CLK74M_P/N	LVDS	C25/B25	1to2 via differential buffer Kintex-7 clock
CN36/38	K7_MMCX1_P/N	LVDS	R28/T28	Kintex-7 MMCX external clock
CN37/39	K7_MMCX2_P/N	LVDS	D26/C26	Kintex-7 MMCX external clock
X9(K7_CLK250M_P/N) or CN34 (HPC_GBTCLK0_M2C_P/N) or CN34 (HPC_GBTCLK1_M2C_P/N)	HPC_CLK_M115_P/N HPC_CLK_M116_P/N HPC_CLK_M117_P/N	LVDS	R8/R7 L8/L7 G8/G7	Via clock selector MGT reference clock
CN34(FMC_HPC)	HPC_CLK0_M2C_P/N	LVDS	T26/T27	HPC_LA IF clock
CN31 (QTH4 Connector)	S4_LVDS_CLK0_P/N S4_LVDS14_CLK_P/N S4_LVDS15_CLK_P/N S4_LVDS30_CLK_P/N S4_LVDS31_CLK_P/N S4_LVDS46_CLK_P/N S4_LVDS47_CLK_P/N S4_LVDS_CLK1_P/N	LVDS	AB27/AC27 AD27/AD28 AG29/AH29 L26/L27 L25/K25 K28/K29 T25/U25 U27/U28	QTH4 IF clock
CN32(QTH4 Connector)	S5_LVDS_CLK0_P/N S5_LVDS14_CLK_P/N S5_LVDS15_CLK_P/N S5_LVDS30_CLK_P/N S5_LVDS31_CLK_P/N S5_LVDS46_CLK_P/N S5_LVDS47_CLK_P/N S5_LVDS_CLK1_P/N	LVDS	F20/E20 F21/E21 D17/D18 H14/G14 G13/F13 D12/D13 E28/D28 D27/C27	QTH5 IF clock

7.3. Kintex-7 MGT Reference Clock Selector

TI's SN65LVDS250DBT is a 4-input 4-output differential clock selector.
Each output can select any of the input clock sources in accordance with the SW26 setting.
The TB-7V-2000T-LSI board does not use Channel 4 (4A, 4B, 4Y, 4Z, S40 and S41).
Thus, SW26-7 and -8 are reserved.

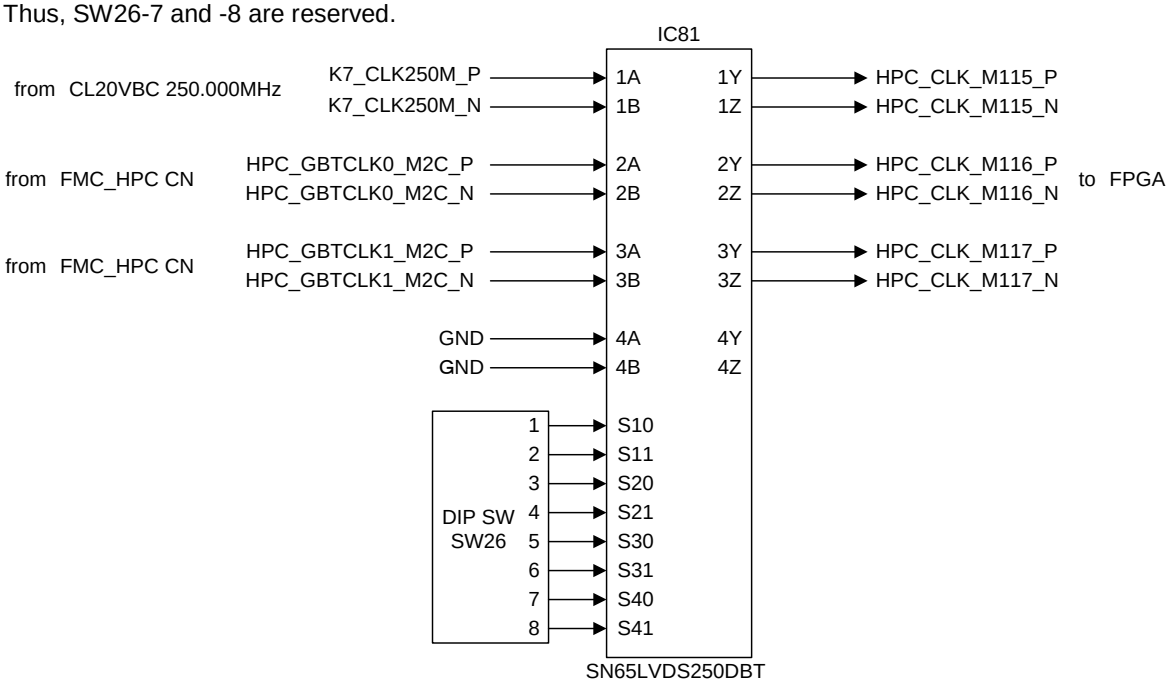


Figure 7-12 Strucure of Kintex-7 MGT Reference Clock Selector IC Peripherals

Table 7-7 Kintex-7 MGT Reference Clock Configuration Table

OUTPUT CHANNEL 1			OUTPUT CHANNEL 2			OUTPUT CHANNEL 3			OUTPUT CHANNEL 4 (Reserved)		
S10	S11	1Y/1Z	S20	S21	2Y/2Z	S30	S31	3Y/3Z	S40	S40	4Y/4Z
OFF	OFF	1A/1B	OFF	OFF	1A/1B	OFF	OFF	1A/1B	OFF	OFF	1A/1B
OFF	ON	2A/2B	OFF	ON	2A/2B	OFF	ON	2A/2B	OFF	ON	2A/2B
ON	OFF	3A/3B	ON	OFF	3A/3B	ON	OFF	3A/3B	ON	OFF	3A/3B
ON	ON	4A/4B	ON	ON	4A/4B	ON	ON	4A/4B	ON	ON	4A/4B

Example: To output K7_CLK250M_P/N to HPC_CLK_M115/117_P/N and HPC_GBTCLK0_M2C_P/N to HPC_CLK_M116_P/N, set the SW26 setting as shown in Table 7-8.

Table 7-8 SW26 Setting Table

SW26
1: OFF
2: OFF
3: OFF
4: ON
5: OFF
6: OFF
7: don't care
8: don't care

8. Virtex-7 Interface

8.1. DDR3 SDRAM

The TB-7V-2000T-LSI board is equipped with eight (8) ELPIDA's DDR3 SDRAMs (EDJ2116DEBG-xx-x). All addresses, commands and clocks are connected using the fly-by termination scheme that is used for SO-DIMM.
In addition, A14 is connected for expansion purposes.

■ Memory Specifications
2Gbit (16Mword x 16bit x 8bank)

■Address Structure
Bank＝3bit
Address＝14bit(Row address＝14bit / Column address＝10bit)

■ Data Bus Structure
Bidirectional data strobe (DQS) for transmission and reception, byte controlled
Data Mask (DM) is byte controlled.

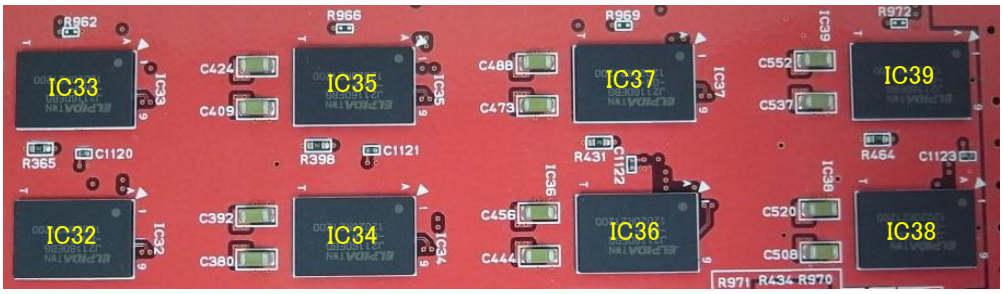


Figure 8-1 Onboard DDR3 SDRAMs

The DDR3 Memory is segmented into four (4) groups as shown in Figure 8-2.

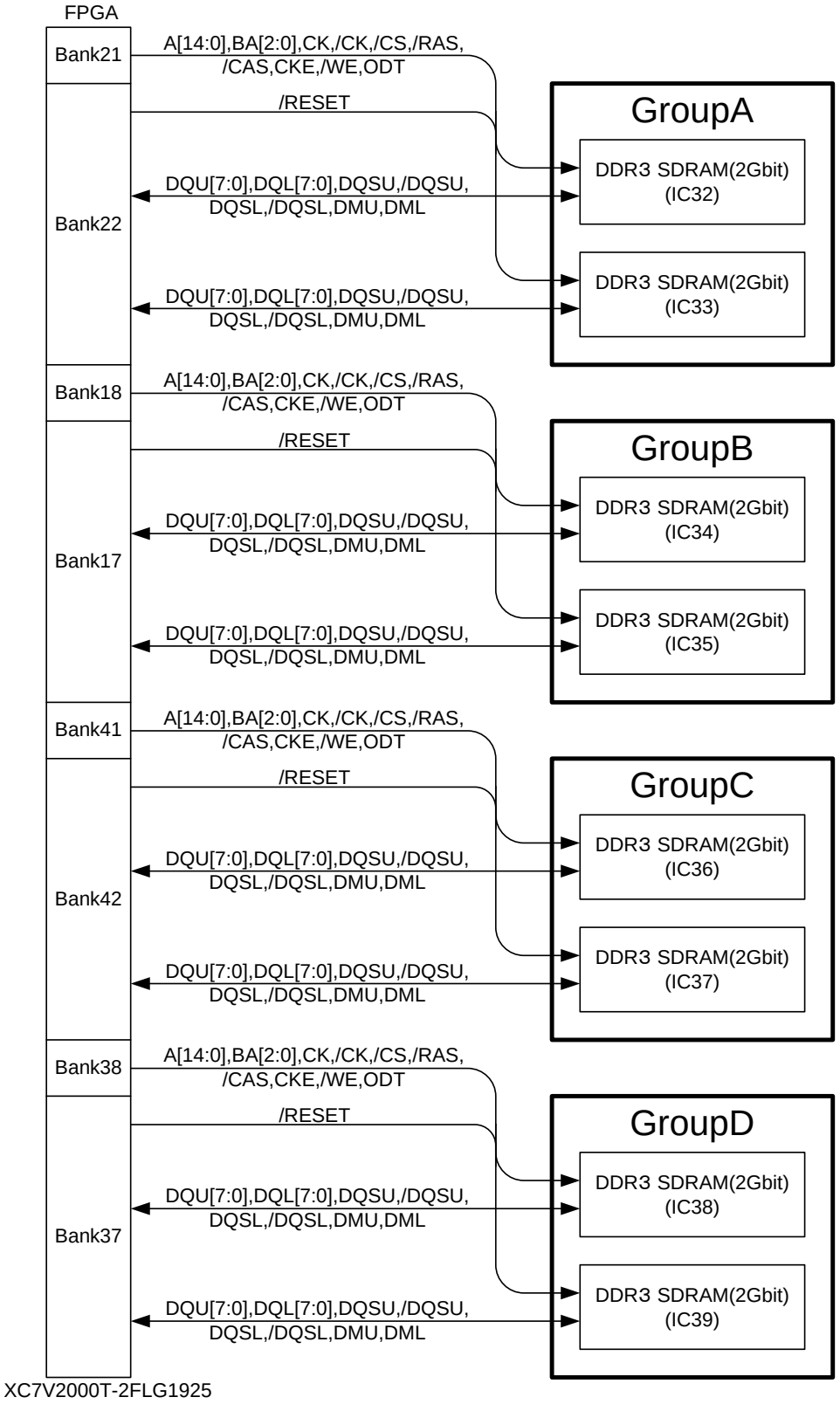


Figure 8-2 DDR3 SDRAM Connections

Table 8-1 DDR3 SDRAM and Virtex-7 Pin Assignment Table

DDR3	IC32		IC33		IC34		IC35	
Pin Name	Pin No.	Bank	Pin No.	Bank	Pin No.	Bank	Pin No.	Bank
A14	G39	21	G39	21	M27	18	M27	18
A13	G40	21	G40	21	L28	18	L28	18
A12	G34	21	G34	21	L27	18	L27	18
A11	G35	21	G35	21	K27	18	K27	18
A10	G36	21	G36	21	K28	18	K28	18
A9	G37	21	G37	21	J28	18	J28	18
A8	J38	21	J38	21	K26	18	K26	18
A7	H38	21	H38	21	J26	18	J26	18
A6	H36	21	H36	21	M25	18	M25	18
A5	H37	21	H37	21	M26	18	M26	18
A4	G41	21	G41	21	D28	18	D28	18
A3	G42	21	G42	21	D29	18	D29	18
A2	L39	21	L39	21	C27	18	C27	18
A1	L40	21	L40	21	C28	18	C28	18
A0	H42	21	H42	21	D26	18	D26	18
BA2	H43	21	H43	21	C26	18	C26	18
BA1	L38	21	L38	21	B26	18	B26	18
BA0	K38	21	K38	21	B27	18	B27	18
CK	J39	21	J39	21	L25	18	L25	18
/CK	H39	21	H39	21	K25	18	K25	18
CKE	M42	21	M42	21	G29	18	G29	18
ODT	L42	21	L42	21	F29	18	F29	18
/RAS	J41	21	J41	21	B25	18	B25	18
/CAS	H41	21	H41	21	A25	18	A25	18
/WE	K40	21	K40	21	A27	18	A27	18
/CS	J40	21	J40	21	A28	18	A28	18
/RESET	C39	22	C39	22	E23	17	E23	17
DQU7	C38	22	E43	22	F23	17	H21	17
DQU6	D38	22	F42	22	E22	17	J21	17
DQU5	E38	22	F44	22	F22	17	K21	17
DQU4	B37	22	F43	22	F25	17	K22	17
DQU3	C37	22	C44	22	G25	17	L22	17
DQU2	A38	22	C43	22	H24	17	M22	17
DQU1	A37	22	E42	22	J24	17	G22	17
DQU0	E37	22	E41	22	H23	17	H22	17
DQL7	F35	22	A39	22	R21	17	B24	17
DQL6	B36	22	B42	22	N23	17	A22	17
DQL5	C36	22	C42	22	P23	17	A23	17
DQL4	A34	22	B40	22	R22	17	D25	17
DQL3	B34	22	B39	22	T22	17	E25	17
DQL2	C34	22	D40	22	R23	17	C24	17
DQL1	D34	22	D39	22	T23	17	D24	17
DQL0	A35	22	C41	22	N24	17	C23	17
DQSU	F38	22	D43	22	G24	17	M24	17
/DQSU	F39	22	D44	22	F24	17	L24	17
DQSL	D35	22	B41	22	N22	17	C22	17
/DQSL	D36	22	A42	22	N21	17	B22	17
DMU	E36	22	F40	22	J23	17	L23	17
DML	B35	22	D41	22	P24	17	D23	17

DDR3	IC36		IC37		IC38		IC39	
Pin Name	Pin No.	Bank	Pin No.	Bank	Pin No.	Bank	Pin No.	Bank
A14	K15	41	K15	41	N9	38	N9	38
A13	J15	41	J15	41	N8	38	N8	38
A12	J14	41	J14	41	P6	38	P6	38
A11	H14	41	H14	41	N6	38	N6	38
A10	G15	41	G15	41	R5	38	R5	38
A9	G14	41	G14	41	P5	38	P5	38
A8	K16	41	K16	41	P10	38	P10	38
A7	J16	41	J16	41	P9	38	P9	38
A6	H17	41	H17	41	R7	38	R7	38
A5	G17	41	G17	41	R6	38	R6	38
A4	F14	41	F14	41	N4	38	N4	38
A3	F13	41	F13	41	N3	38	N3	38
A2	B14	41	B14	41	P4	38	P4	38
A1	A13	41	A13	41	P3	38	P3	38
A0	E13	41	E13	41	M2	38	M2	38
BA2	D13	41	D13	41	M1	38	M1	38
BA1	A15	41	A15	41	R1	38	R1	38
BA0	A14	41	A14	41	P1	38	P1	38
CK	H16	41	H16	41	P8	38	P8	38
/CK	G16	41	G16	41	N7	38	N7	38
CKE	F15	41	F15	41	L2	38	L2	38
ODT	E15	41	E15	41	K2	38	K2	38
/RAS	C14	41	C14	41	N2	38	N2	38
/CAS	C13	41	C13	41	N1	38	N1	38
/WE	D15	41	D15	41	R3	38	R3	38
/CS	D14	41	D14	41	R2	38	R2	38
/RESET	C9	42	C9	42	U4	37	U4	37
DQU7	D9	42	H9	42	U5	37	Y6	37
DQU6	C11	42	J9	42	V3	37	Y7	37
DQU5	C12	42	J11	42	V4	37	W8	37
DQU4	A9	42	K11	42	T2	37	Y8	37
DQU3	A10	42	F9	42	T3	37	AA7	37
DQU2	A12	42	G9	42	T4	37	AA8	37
DQU1	B12	42	J10	42	T5	37	AA9	37
DQU0	A8	42	K10	42	U1	37	AA10	37
DQL7	R11	42	H11	42	U10	37	AA3	37
DQL6	M12	42	G12	42	V9	37	AA4	37
DQL5	N12	42	H12	42	V10	37	AA5	37
DQL4	R12	42	F10	42	T7	37	W1	37
DQL3	T12	42	G10	42	T8	37	Y1	37
DQL2	R13	42	D10	42	R8	37	W5	37
DQL1	T13	42	E10	42	T9	37	Y5	37
DQL0	N13	42	D11	42	U6	37	W3	37
DQSU	B11	42	L12	42	V2	37	W6	37
/DQSU	B10	42	K12	42	V1	37	V6	37
DQSL	N11	42	F12	42	V8	37	Y3	37
/DQSL	M11	42	E12	42	V7	37	Y2	37
DMU	B9	42	J13	42	U2	37	W10	37
DML	P13	42	E11	42	U7	37	W4	37

8.2. QTH Connector

The TB-7V-2000T-LSI board is equipped with five SAMTEC's 120pin QTH connectors that allow high speed data connection to external devices. Each connector provides up to 56 pairs of LVDS signal connections, including 8 pairs of clock signals (or 119 single-pin connections).
As shown in Figure 8-3, Virtex-7 provides CN20, CN21 and CN22 connectors whose signal voltage level is fixed at 1.8V.

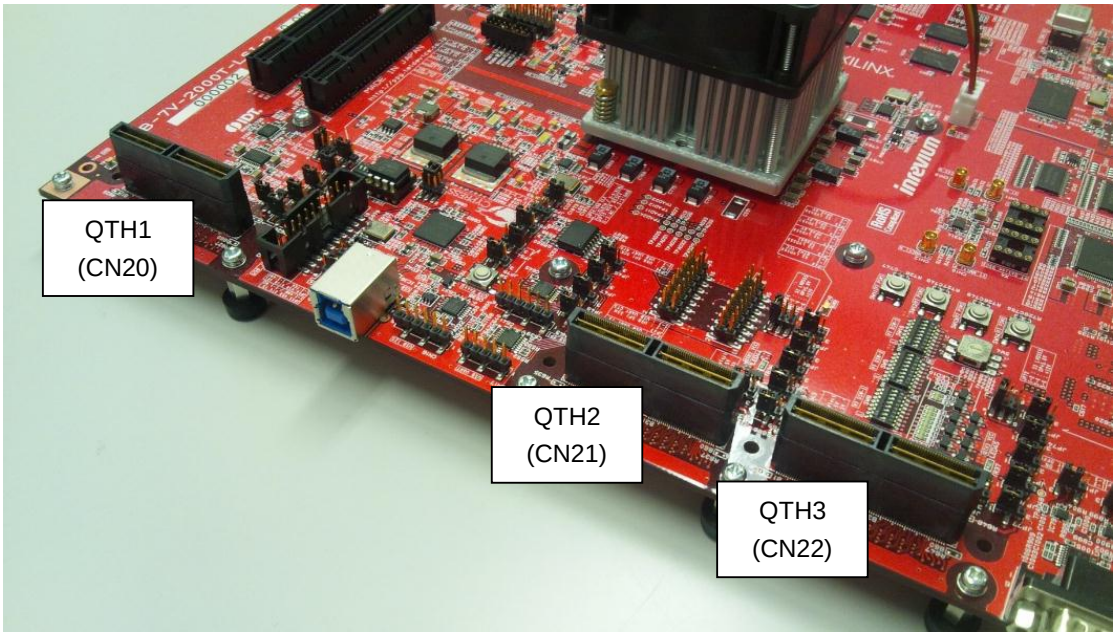


Figure 8-3 Virtex-7 QTH Connector

8.2.1. QTH1 Power Supply Pinout

H1 Pin
OP+3.3V power supply (currently not available due to non-implementation of R625).

H2 Pin
OP+3.3V power supply (currently not available due to non-implementation of R625).

B54 Pin
Any 5V, 12V or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-2.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R844).

Table 8-2 QTH1 B54 Pin Assignments

Supply Voltage	JP56
+12V	5-6
OP+5V	3-4
FPGA(Virtex-7) Single	1-2

B55 Pin

Either 5V or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-3.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1036).

Table 8-3 QTH1 B55 Pin Assignments

Supply Voltage	JP57
OP+5V	2-3
FPGA(Virtex-7)	1-2

B56 Pin

Either 5V or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-4.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1037).

Table 8-4 QTH1 B56 Pin Assignments

Supply Voltage	JP58
OP+5V	2-3
FPGA(Virtex-7)	1-2

B57 Pin

Either 5V or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-5.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1038).

Table 8-5 QTH1 B57 Pin Assignments

Supply Voltage	JP59
OP+5V	2-3
FPGA(Virtex-7)	1-2

B58 Pin

Either TRAD or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-6.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1039).

Table 8-6 QTH1 B58 Pin Assignments

Supply Voltage	JP60
TPAD38	2-3
FPGA(Virtex-7)	1-2

B59 Pin

Either QTH1_VCC or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-7. QTH1_VCC is selectable by the jumper JP62.

Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1040).

Table 8-7 QTH1 B59 Pin Assignments

Supply Voltage	JP61	JP62
QTH1_VCC(OP+2.5V)	2-3	1-2
QTH1_VCC(OP+3.3V)	2-3	2-3
FPGA(Virtex-7)	1-2	-

B60 Pin

Either 2.5V or 3.3V is selectable by setting the jumper as shown in Table 8-8.

Table 8-8 QTH1 B60 Pin Assignments

Supply Voltage	JP62
OP+2.5V	1-2
OP+3.3V	2-3

H7 Pin

The same voltage selection as B60 Pin is applicable. Currenty this pin is not used due to non-implementation of R627.

H8 Pin

The same voltage selection as B60 Pin is applicable. Currenty this pin is not used due to non-implementation of R628.

Table 8-9 QTH1 Connector (CN20) Pin Assignments

FPGA (Virtex-7)			Signal Name	QTH1 (CN20)				Signal Name	FPGA (Virtex-7)		
Bank	Pin#	Pin Name		Pair	Pin#	Pin#	Pair		Pin Name	Pin#	Bank
	-	-	-	-	H1	H2	-	-	-	-	
	AT12	IO_L12N_T1_MRCC_31	S1_LVDS_CLK0_N	N	B1	A1	N	S1_LVDS0_N	IO_L2N_T0_31	AJ10	
	AR12	IO_L12P_T1_MRCC_31	S1_LVDS_CLK0_P	P	B2	A2	P	S1_LVDS0_P	IO_L2P_T0_31	AJ11	
	AM10	IO_L5N_T0_31	S1_LVDS1_N	N	B3	A3	N	S1_LVDS2_N	IO_L4N_T0_31	AK12	
	AL10	IO_L5P_T0_31	S1_LVDS1_P	P	B4	A4	P	S1_LVDS2_P	IO_L4P_T0_31	AK13	
	AN11	IO_L9N_T1_DQS_31	S1_LVDS3_N	N	B5	A5	N	S1_LVDS4_N	IO_L1N_T0_31	AM11	
	AN12	IO_L9P_T1_DQS_31	S1_LVDS3_P	P	B6	A6	P	S1_LVDS4_P	IO_L1P_T0_31	AM12	
	AL12	IO_L3N_T0_DQS_31	S1_LVDS5_N	N	B7	A7	N	S1_LVDS6_N/VREF	IO_L6N_T0_VREF_31	AK10	
	AL13	IO_L3P_T0_DQS_31	S1_LVDS5_P	P	B8	A8	P	S1_LVDS6_P	IO_L6P_T0_31	AK11	
	AV11	IO_L14N_T2_SRCC_31	S1_LVDS7_N/VREF	N	B9	A9	N	S1_LVDS8_N	IO_L8N_T1_31	AT13	
	AV12	IO_L14P_T2_SRCC_31	S1_LVDS7_P	P	B10	A10	P	S1_LVDS8_P	IO_L8P_T1_31	AR13	
	AY10	IO_L17N_T2_31	S1_LVDS9_N	N	B11	A11	N	S1_LVDS10_N	IO_L7N_T1_31	AR10	
31	AW10	IO_L17P_T2_31	S1_LVDS9_P	P	B12	A12	P	S1_LVDS10_P	IO_L7P_T1_31	AP10	31
	AY11	IO_L16N_T2_31	S1_LVDS11_N	N	B13	A13	N	S1_LVDS12_N	IO_L15N_T2_DQS_31	AU10	
	AW11	IO_L16P_T2_31	S1_LVDS11_P	P	B14	A14	P	S1_LVDS12_P	IO_L15P_T2_DQS_31	AT10	
	AP13	IO_L10N_T1_31	S1_LVDS13_N	N	B15	A15	N	S1_LVDS14_N/CLK_N	IO_L11N_T1_SRCC_31	AR11	
	AN13	IO_L10P_T1_31	S1_LVDS13_P	P	B16	A16	P	S1_LVDS14_P/CLK_P	IO_L11P_T1_SRCC_31	AP11	
	AU11	IO_L13N_T2_MRCC_31	S1_LVDS15_N/CLK_N	N	B17	A17	N	S1_LVDS16_N	IO_L18N_T2_31	AY13	
	AU12	IO_L13P_T2_MRCC_31	S1_LVDS15_P/CLK_P	P	B18	A18	P	S1_LVDS16_P	IO_L18P_T2_31	AW13	
	BC11	IO_L20N_T3_31	S1_LVDS17_N	N	B19	A19	N	S1_LVDS18_N	IO_L21N_T3_DQS_31	BA12	
	BB11	IO_L20P_T3_31	S1_LVDS17_P	P	B20	A20	P	S1_LVDS18_P	IO_L21P_T3_DQS_31	AY12	
	BD10	IO_L22N_T3_31	S1_LVDS19_N	N	B21	A21	N	S1_LVDS20_N	IO_L23N_T3_31	BC12	
	BD11	IO_L22P_T3_31	S1_LVDS19_P	P	B22	A22	P	S1_LVDS20_P	IO_L23P_T3_31	BB12	
	BB10	IO_L19N_T3_VREF_31	S1_LVDS21_N/VREF	N	B23	A23	N	S1_LVDS22_N	IO_L24N_T3_31	BD13	
	BA10	IO_L19P_T3_31	S1_LVDS21_P	P	B24	A24	P	S1_LVDS22_P	IO_L24P_T3_31	BC13	

FPGA (Virtex-7)			Signal Name	QTH1 (CN20)				Signal Name	FPGA (Virtex-7)		
Bank	Pin#	Pin Name		Pair	Pin#	Pin#	Pair		Pin Name	Pin#	Bank
32	AP14	IO_L20N_T3_32	S1_LVDS23_N	N	B25	A25	N	S1_LVDS24_N/VREF	IO_L6N_T0_VREF_32	BA13	32
	AN14	IO_L20P_T3_32	S1_LVDS23_P	P	B26	A26	P	S1_LVDS24_P	IO_L6P_T0_32	BA14	
	BD14	IO_L2N_T0_32	S1_LVDS25_N	N	B27	A27	N	S1_LVDS26_N	IO_L4N_T0_32	BB14	
	BC14	IO_L2P_T0_32	S1_LVDS25_P	P	B28	A28	P	S1_LVDS26_P	IO_L4P_T0_32	BB15	
	BC16	IO_L3N_T0_DQS_32	S1_LVDS27_N	N	B29	A29	N	S1_LVDS28_N	IO_L5N_T0_32	BD15	
	BC17	IO_L3P_T0_DQS_32	S1_LVDS27_P	P	B30	A30	P	S1_LVDS28_P	IO_L5P_T0_32	BD16	
	-	-	TPAD34	-	H3	H4	-	TPAD35	-	-	
	-	-	TPAD36	-	H5	H6	-	TPAD37	-	-	
	BA17	IO_L7N_T1_32	S1_LVDS29_N	N	B31	A31	N	S1_LVDS30_N/CLK_N	IO_L11N_T1_SRCC_32	AW15	
	AY17	IO_L7P_T1_32	S1_LVDS29_P	P	B32	A32	P	S1_LVDS30_P/CLK_P	IO_L11P_T1_SRCC_32	AV16	
	AY16	IO_L12N_T1_MRCC_32	S1_LVDS31_N/CLK_N	N	B33	A33	N	S1_LVDS32_N	IO_L8N_T1_32	AW14	
	AW16	IO_L12P_T1_MRCC_32	S1_LVDS31_P/CLK_P	P	B34	A34	P	S1_LVDS32_P	IO_L8P_T1_32	AV14	
	BA15	IO_L9N_T1_DQS_32	S1_LVDS33_N	N	B35	A35	N	S1_LVDS34_N	IO_L10N_T1_32	AU14	
	AY15	IO_L9P_T1_DQS_32	S1_LVDS33_P	P	B36	A36	P	S1_LVDS34_P	IO_L10P_T1_32	AT14	
	AU16	IO_L14N_T2_SRCC_32	S1_LVDS35_N	N	B37	A37	N	S1_LVDS36_N	IO_L1N_T0_32	BB16	
	AU17	IO_L14P_T2_SRCC_32	S1_LVDS35_P	P	B38	A38	P	S1_LVDS36_P	IO_L1P_T0_32	BB17	
	AM16	IO_L19N_T3_VREF_32	S1_LVDS37_N/VREF	N	B39	A39	N	S1_LVDS38_N	IO_L16N_T2_32	AT17	
	AM17	IO_L19P_T3_32	S1_LVDS37_P	P	B40	A40	P	S1_LVDS38_P	IO_L16P_T2_32	AR17	
	AN16	IO_L17N_T2_32	S1_LVDS39_N	N	B41	A41	N	S1_LVDS40_N/VREF	IO_L18N_T2_32	AR15	
	AN17	IO_L17P_T2_32	S1_LVDS39_P	P	B42	A42	P	S1_LVDS40_P	IO_L18P_T2_32	AR16	
	AP15	IO_L15N_T2_DQS_32	S1_LVDS41_N	N	B43	A43	N	S1_LVDS42_N	IO_L24N_T3_32	AL14	
	AP16	IO_L15P_T2_DQS_32	S1_LVDS41_P	P	B44	A44	P	S1_LVDS42_P	IO_L24P_T3_32	AL15	
	AK15	IO_L21N_T3_DQS_32	S1_LVDS43_N	N	B45	A45	N	S1_LVDS44_N	IO_L22N_T3_32	AM14	
	AK16	IO_L21P_T3_DQS_32	S1_LVDS43_P	P	B46	A46	P	S1_LVDS44_P	IO_L22P_T3_32	AM15	
	AJ15	IO_L23N_T3_32	S1_LVDS45_N	N	B47	A47	N	S1_LVDS46_N/CLK_N	IO_L13N_T2_MRCC_32	AU15	
	AJ16	IO_L23P_T3_32	S1_LVDS45_P	P	B48	A48	P	S1_LVDS46_P/CLK_P	IO_L13P_T2_MRCC_32	AT15	

FPGA (Virtex-7)			Signal Name	QTH1 (CN20)				Signal Name	FPGA (Virtex-7)		
Bank	Pin#	Pin Name		Pair	Pin#	Pin#	Pair		Pin Name	Pin#	Bank
	AU19	IO_L11N_T1_SRCC_33	S1_LVDS47_N/CLK_N	N	B49	A49	N	S1_LVDS48_N	IO_L1N_T0_33	BC21	
	AT19	IO_L11P_T1_SRCC_33	S1_LVDS47_P/CLK_P	P	B50	A50	P	S1_LVDS48_P	IO_L1P_T0_33	BB21	
	BB20	IO_L2N_T0_33	S1_LVDS49_N	N	B51	A51	N	S1_LVDS50_N	IO_L3N_T0_DQS_33	BD20	
	BA20	IO_L2P_T0_33	S1_LVDS49_P	P	B52	A52	P	S1_LVDS50_P	IO_L3P_T0_DQS_33	BD21	
	AW21	IO_L7P_T1_33	S1_LVDS53	-	B53	A53	N	S1_LVDS51_N/VREF	IO_L6N_T0_VREF_33	BB19	
	AY18	IO_L8P_T1_33	S1_LVDS55/5V/12V	-	B54	A54	P	S1_LVDS51_P	IO_L6P_T0_33	BA19	
	BA18	IO_L8N_T1_33	S1_LVDS56/5V	-	B55	A55	N	S1_LVDS52_N	IO_L4N_T0_33	BD18	
33	AW20	IO_L9P_T1_DQS_33	S1_LVDS57/5V	-	B56	A56	P	S1_LVDS52_P	IO_L4P_T0_33	BC18	33
	AY20	IO_L9N_T1_DQS_33	S1_LVDS58/5V	-	B57	A57	N	S1_LVDS54_N	IO_L5N_T0_33	BD19	
	AW19	IO_L10P_T1_33	S1_LVDS59/TP	-	B58	A58	P	S1_LVDS54_P	IO_L5P_T0_33	BC19	
	AW18	IO_L10N_T1_33	S1_LVDS60/2.5V/3.3V	-	B59	A59	N	S1_LVDS_CLK1_N	IO_L12N_T1_MRCC_33	AV18	
	-	-	QTH1_VCC	-	B60	A60	P	S1_LVDS_CLK1_P	IO_L12P_T1_MRCC_33	AV19	
	-	-	(QTH1_VCC) *JP resistor not implemented	-	H7	H8	-	(QTH1_VCC) *JP resistor not implemented	-	-	

8.2.2. QTH2 Power Supply Pinout

H1 Pin

OP+3.3V power supply (currently not available due to non-implementation of R635).

H2 Pin

OP+3.3V power supply (currently not available due to non-implementation of R636).

B54 Pin

Any 5V, 12V or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-10.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1047).

Table 8-10 QTH2 B54 Pin Assignments

Supply Voltage	JP64
+12V	5-6
OP+5V	3-4
FPGA(Virtex-7)	1-2

B55 Pin

Either 5V or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-11.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1048).

Table 8-11 QTH2 B55 Pin Assignments

Supply Voltage	JP65
OP+5V	2-3
FPGA(Virtex-7)	1-2

B56 Pin

Either 5V or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-12.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1041).

Table 8-12 QTH2 B56 Pin Assignments

Supply Voltage	JP66
OP+5V	2-3
FPGA(Virtex-7)	1-2

B57 Pin

Either 5V or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-13.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1042).

Table 8-13 QTH2 B57 Pin Assignments

Supply Voltage	JP67
OP+5V	2-3
FPGA(Virtex-7)	1-2

B58 Pin

Either TRAD or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-14.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1045).

Table 8-14 QTH2 B58 Pin Assignments

Supply Voltage	JP68
TPAD38	2-3
FPGA(Virtex-7)	1-2

B59 Pin

Either QTH2_VCC or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-15.
QTH2_VCC is selectable by the jumper JP63.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1046).

Table 8-15 QTH2 B59 Pin Assignments

Supply Voltage	JP61	JP63
QTH2_VCC(OP+2.5V)	2-3	1-2
QTH2_VCC(OP+3.3V)	2-3	2-3
FPGA(Virtex-7)	1-2	-

B60 Pin

Either 2.5V or 3.3V is selectable by setting the jumper as shown in Table 8-16.

Table 8-16 QTH2 B60 Pin Assignments

Supply Voltage	JP63
OP+2.5V	1-2
OP+3.3V	2-3

H7 Pin

The same voltage selection as B60 Pin is applicable. Currenty this pin is not used due to non-implementation of R637.

H8 Pin

The same voltage selection as B60 Pin is applicable. Currenty this pin is not used due to non-implementation of R638.

Table 8-17 QTH2 Connector (CN21) Pin Assignments

FPGA (Virtex-7)			Signal Name	QTH2(CN21)				Signal Name	FPGA (Virtex-7)		
Bank	Pin#	Pin Name		Pair	Pin#	Pin#	Pair		Pin Name	Pin#	Bank
	-	-	-	-	H1	H2	-	-	-	-	
	AU27	IO_L12N_T1_MRCC_35	S2_LVDS_CLK0_N	N	B1	A1	N	S2_LVDS0_N	IO_L1N_T0_AD4N_35	BD26	
	AU26	IO_L12P_T1_MRCC_35	S2_LVDS_CLK0_P	P	B2	A2	P	S2_LVDS0_P	IO_L1P_T0_AD4P_35	BC26	
	BC29	IO_L2N_T0_AD12N_35	S2_LVDS1_N	N	B3	A3	N	S2_LVDS2_N	IO_L3N_T0_DQS_AD5N_35	BB27	
	BB29	IO_L2P_T0_AD12P_35	S2_LVDS1_P	P	B4	A4	P	S2_LVDS2_P	IO_L3P_T0_DQS_AD5P_35	BB26	
	BD29	IO_L4N_T0_35	S2_LVDS3_N	N	B5	A5	N	S2_LVDS4_N	IO_L5N_T0_AD13N_35	BA28	
	BD28	IO_L4P_T0_35	S2_LVDS3_P	P	B6	A6	P	S2_LVDS4_P	IO_L5P_T0_AD13P_35	BA27	
	BA29	IO_L7N_T1_AD6N_35	S2_LVDS5_N	N	B7	A7	N	S2_LVDS6_N/VREF	IO_L6N_T0_VREF_35	BC28	
	AY28	IO_L7P_T1_AD6P_35	S2_LVDS5_P	P	B8	A8	P	S2_LVDS6_P	IO_L6P_T0_35	BC27	
	AT28	IO_L14N_T2_SRCC_35	S2_LVDS7_N/VREF	N	B9	A9	N	S2_LVDS8_N	IO_L8N_T1_AD14N_35	AY27	
	AT27	IO_L14P_T2_SRCC_35	S2_LVDS7_P	P	B10	A10	P	S2_LVDS8_P	IO_L8P_T1_AD14P_35	AY26	
	AW29	IO_L9N_T1_DQS_AD7N_35	S2_LVDS9_N	N	B11	A11	N	S2_LVDS10_N	IO_L10N_T1_AD15N_35	AW26	
35	AW28	IO_L9P_T1_DQS_AD7P_35	S2_LVDS9_P	P	B12	A12	P	S2_LVDS10_P	IO_L10P_T1_AD15P_35	AV26	35
	AR28	IO_L15N_T2_DQS_35	S2_LVDS11_N	N	B13	A13	N	S2_LVDS12_N	IO_L16N_T2_35	AU29	
	AP28	IO_L15P_T2_DQS_35	S2_LVDS11_P	P	B14	A14	P	S2_LVDS12_P	IO_L16P_T2_35	AT29	
	AP26	IO_L17N_T2_35	S2_LVDS13_N	N	B15	A15	N	S2_LVDS14_N/CLK_N	IO_L11N_T1_SRCC_35	AV28	
	AP25	IO_L17P_T2_35	S2_LVDS13_P	P	B16	A16	P	S2_LVDS14_P/CLK_P	IO_L11P_T1_SRCC_35	AV27	
	AR27	IO_L13N_T2_MRCC_35	S2_LVDS15_N/CLK_N	N	B17	A17	N	S2_LVDS16_N	IO_L18N_T2_35	AN28	
	AR26	IO_L13P_T2_MRCC_35	S2_LVDS15_P/CLK_P	P	B18	A18	P	S2_LVDS16_P	IO_L18P_T2_35	AN27	
	AL28	IO_L20N_T3_35	S2_LVDS17_N	N	B19	A19	N	S2_LVDS18_N	IO_L21N_T3_DQS_35	AM25	
	AK27	IO_L20P_T3_35	S2_LVDS17_P	P	B20	A20	P	S2_LVDS18_P	IO_L21P_T3_DQS_35	AL25	
	AK26	IO_L22N_T3_35	S2_LVDS19_N	N	B21	A21	N	S2_LVDS20_N	IO_L23N_T3_35	AM27	
	AJ26	IO_L22P_T3_35	S2_LVDS19_P	P	B22	A22	P	S2_LVDS20_P	IO_L23P_T3_35	AL27	
	AN26	IO_L19N_T3_VREF_35	S2_LVDS21_N/VREF	N	B23	A23	N	S2_LVDS22_N	IO_L24N_T3_35	AK25	
	AM26	IO_L19P_T3_35	S2_LVDS21_P	P	B24	A24	P	S2_LVDS22_P	IO_L24P_T3_35	AJ25	

FPGA (Virtex-7)			Signal Name	QTH2(CN21)				Signal Name	FPGA (Virtex-7)		
Bank	Pin#	Pin Name		Pair	Pin#	Pin#	Pair		Pin Name	Pin#	Bank
36	BD31	IO_L4N_T0_36	S2_LVDS23_N	N	B25	A25	N	S2_LVDS24_N/VREF	IO_L6N_T0_VREF_36	BB30	36
	BD30	IO_L4P_T0_36	S2_LVDS23_P	P	B26	A26	P	S2_LVDS24_P	IO_L6P_T0_36	BA30	
	BA33	IO_L5N_T0_36	S2_LVDS25_N	N	B27	A27	N	S2_LVDS26_N	IO_L3N_T0_DQS_36	BB32	
	BA32	IO_L5P_T0_36	S2_LVDS25_P	P	B28	A28	P	S2_LVDS26_P	IO_L3P_T0_DQS_36	BB31	
	BC32	IO_L2N_T0_36	S2_LVDS27_N	N	B29	A29	N	S2_LVDS28_N	IO_L1N_T0_36	BD33	
	BC31	IO_L2P_T0_36	S2_LVDS27_P	P	B30	A30	P	S2_LVDS28_P	IO_L1P_T0_36	BC33	
	-	-	TPAD39	-	H3	H4	-	TPAD40	-	-	
	-	-	TPAD41	-	H5	H6	-	TPAD42	-	-	
	AY33	IO_L7N_T1_36	S2_LVDS29_N	N	B31	A31	N	S2_LVDS30_N/CLK_N	IO_L11N_T1_SRCC_36	AV32	
	AW33	IO_L7P_T1_36	S2_LVDS29_P	P	B32	A32	P	S2_LVDS30_P/CLK_P	IO_L11P_T1_SRCC_36	AU32	
	AU31	IO_L12N_T1_MRCC_36	S2_LVDS31_N/CLK_N	N	B33	A33	N	S2_LVDS32_N	IO_L8N_T1_36	AY30	
	AU30	IO_L12P_T1_MRCC_36	S2_LVDS31_P/CLK_P	P	B34	A34	P	S2_LVDS32_P	IO_L8P_T1_36	AW30	
	AY32	IO_L9N_T1_DQS_36	S2_LVDS33_N	N	B35	A35	N	S2_LVDS34_N	IO_L10N_T1_36	AW31	
	AY31	IO_L9P_T1_DQS_36	S2_LVDS33_P	P	B36	A36	P	S2_LVDS34_P	IO_L10P_T1_36	AV31	
	AT32	IO_L14N_T2_SRCC_36	S2_LVDS35_N	N	B37	A37	N	S2_LVDS36_N	IO_L15N_T2_DQS_36	AT33	
	AR32	IO_L14P_T2_SRCC_36	S2_LVDS35_P	P	B38	A38	P	S2_LVDS36_P	IO_L15P_T2_DQS_36	AR33	
	AM32	IO_L19N_T3_VREF_36	S2_LVDS37_N/VREF	N	B39	A39	N	S2_LVDS38_N	IO_L16N_T2_36	AP33	
	AL32	IO_L19P_T3_36	S2_LVDS37_P	P	B40	A40	P	S2_LVDS38_P	IO_L16P_T2_36	AN33	
	AP30	IO_L17N_T2_36	S2_LVDS39_N	N	B41	A41	N	S2_LVDS40_N/VREF	IO_L18N_T2_36	AT30	
	AP29	IO_L17P_T2_36	S2_LVDS39_P	P	B42	A42	P	S2_LVDS40_P	IO_L18P_T2_36	AR30	
	AN32	IO_L20N_T3_36	S2_LVDS41_N	N	B43	A43	N	S2_LVDS42_N	IO_L21N_T3_DQS_36	AK31	
	AN31	IO_L20P_T3_36	S2_LVDS41_P	P	B44	A44	P	S2_LVDS42_P	IO_L21P_T3_DQS_36	AK30	
	AM31	IO_L22N_T3_36	S2_LVDS43_N	N	B45	A45	N	S2_LVDS44_N	IO_L23N_T3_36	AL30	
	AM30	IO_L22P_T3_36	S2_LVDS43_P	P	B46	A46	P	S2_LVDS44_P	IO_L23P_T3_36	AL29	
	AN29	IO_L24N_T3_36	S2_LVDS45_N	N	B47	A47	N	S2_LVDS46_N/CLK_N	IO_L13N_T2_MRCC_36	AR31	
	AM29	IO_L24P_T3_36	S2_LVDS45_P	P	B48	A48	P	S2_LVDS46_P/CLK_P	IO_L13P_T2_MRCC_36	AP31	

FPGA (Virtex-7)			Signal Name	QTH2(CN21)				Signal Name	FPGA (Virtex-7)		
Bank	Pin#	Pin Name		Pair	Pin#	Pin#	Pair		Pin Name	Pin#	Bank
	AR23	IO_L14N_T2_SRCC_34	S2_LVDS47_N/CLK_N	N	B49	A49	N	S2_LVDS48_N	IO_L24N_T3_34	AJ24	
	AP23	IO_L14P_T2_SRCC_34	S2_LVDS47_P/CLK_P	P	B50	A50	P	S2_LVDS48_P	IO_L24P_T3_34	AJ23	
	AM22	IO_L23N_T3_34	S2_LVDS49_N	N	B51	A51	N	S2_LVDS50_N	IO_L22N_T3_34	AL23	
	AL22	IO_L23P_T3_34	S2_LVDS49_P	P	B52	A52	P	S2_LVDS50_P	IO_L22P_T3_34	AK23	
	AN22	IO_L18P_T2_34	S2_LVDS53	-	B53	A53	N	S2_LVDS51_N/VREF	IO_L19N_T3_VREF_34	AM24	
	AN24	IO_L17P_T2_34	S2_LVDS55/5V/12V	-	B54	A54	P	S2_LVDS51_P	IO_L19P_T3_34	AL24	
	AP24	IO_L17N_T2_34	S2_LVDS56/5V	-	B55	A55	N	S2_LVDS52_N	IO_L21N_T3_DQS_34	AN21	
34	AR25	IO_L16P_T2_34	S2_LVDS57/5V	-	B56	A56	P	S2_LVDS52_P	IO_L21P_T3_DQS_34	AM21	34
	AT25	IO_L16N_T2_34	S2_LVDS58/5V	-	B57	A57	N	S2_LVDS54_N	IO_L20N_T3_34	AK22	
	AR22	IO_L15P_T2_DQS_34	S2_LVDS59/TP	-	B58	A58	P	S2_LVDS54_P	IO_L20P_T3_34	AK21	
	AT22	IO_L15N_T2_DQS_34	S2_LVDS60/2.5V/3.3V	-	B59	A59	N	S2_LVDS_CLK1_N	IO_L13N_T2_MRCC_34	AT24	
			QTH2_VCC	-	B60	A60	P	S2_LVDS_CLK1_P	IO_L13P_T2_MRCC_34	AT23	
	-	-	(QTH2_VCC) *JP resistor not implemented	-	H7	H8	-	(QTH2_VCC) *JP resistor not implemented	-	-	

8.2.3. QTH3 Power Supply Pinout

H1 Pin

OP+3.3V power supply (currently not available due to non-implementation of R645).

H2 Pin

OP+3.3V power supply (currently not available due to non-implementation of R646).

B54 Pin

Any 5V, 12V or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-18.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1053).

Table 8-18 QTH3 B54 Pin Assignments

Supply Voltage	JP72
+12V	5-6
OP+5V	3-4
FPGA(Virtex-7)	1-2

B55 Pin

Either 5V or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-19.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1054).

Table 8-19 QTH3 B55 Pin Assignments

Supply Voltage	JP73
OP+5V	2-3
FPGA(Virtex-7)	1-2

B56 Pin

Either 5V or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-20.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1049).

Table 8-20 QTH3 B56 Pin Assignments

Supply Voltage	JP74
OP+5V	2-3
FPGA(Virtex-7)	1-2

B57 Pin

Either 5V or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-21.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1050).

Table 8-21 QTH3 B57 Pin Assignments

Supply Voltage	JP75
OP+5V	2-3
FPGA(Virtex-7)	1-2

B58 Pin

Either TRAD or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-22.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1051).

Table 8-22 QTH3 B58 Pin Assignments

Supply Voltage	JP76
TPAD38	2-3
FPGA(Virtex-7)	1-2

B59 Pin

Either QTH3_VCC or FPGA (Virtex-7) is selectable by setting the jumper as shown in Table 8-23.
QTH3_VCC is selectable by the jumper JP70.
Currently the FPGA (Virtex-7) connection is not available due to non-implementation of R1052).

Table 8-23 QTH3 B59 Pin Assignments

Supply Voltage	JP61	JP70
QTH3_VCC(OP+2.5V)	2-3	1-2
QTH3_VCC(OP+3.3V)	2-3	2-3
FPGA(Virtex-7)	1-2	-

B60 Pin

Either 2.5V or 3.3V is selectable by setting the jumper as shown in Table 8-24.

Table 8-24 QTH3 B60 Pin Assignments

Supply Voltage	JP70
OP+2.5V	1-2
OP+3.3V	2-3

H7 Pin

The same voltage selection as B60 Pin is applicable. Currenty this pin is not used due to non-implementation of R647.

H8 Pin

The same voltage selection as B60 Pin is applicable. Currenty this pin is not used due to non-implementation of R648.

Table 8-25 QTH3 Connector (CN22) Pin Assignments

FPGA (Virtex-7)			Signal Name	QTH3(CN22)				Signal Name	FPGA (Virtex-7)		
Bank	Pin#	Pin Name		Pair	Pin#	Pin#	Pair		Pin Name	Pin#	Bank
	-	-	-	-	H1	H2	-	-	-	-	
	BA40	IO_L12N_T1_MRCC_11	S3_LVDS_CLK0_N	N	B1	A1	N	S3_LVDS0_N	IO_L1N_T0_11	AW41	
	AY40	IO_L12P_T1_MRCC_11	S3_LVDS_CLK0_P	P	B2	A2	P	S3_LVDS0_P	IO_L1P_T0_11	AW40	
	BA43	IO_L2N_T0_11	S3_LVDS1_N	N	B3	A3	N	S3_LVDS2_N	IO_L3N_T0_DQS_11	AW44	
	AY43	IO_L2P_T0_11	S3_LVDS1_P	P	B4	A4	P	S3_LVDS2_P	IO_L3P_T0_DQS_11	AW43	
	BB44	IO_L4N_T0_11	S3_LVDS3_N	N	B5	A5	N	S3_LVDS4_N	IO_L5N_T0_11	AY42	
	BA44	IO_L4P_T0_11	S3_LVDS3_P	P	B6	A6	P	S3_LVDS4_P	IO_L5P_T0_11	AY41	
	BB35	IO_L22N_T3_11	S3_LVDS5_N	N	B7	A7	N	S3_LVDS6_N/VREF	IO_L6N_T0_VREF_11	BB42	
	BA35	IO_L22P_T3_11	S3_LVDS5_P	P	B8	A8	P	S3_LVDS6_P	IO_L6P_T0_11	BA42	
	BA38	IO_L14N_T2_SRCC_11	S3_LVDS7_N/VREF	N	B9	A9	N	S3_LVDS8_N	IO_L16N_T2_11	BC37	
	BA37	IO_L14P_T2_SRCC_11	S3_LVDS7_P	P	B10	A10	P	S3_LVDS8_P	IO_L16P_T2_11	BB37	
	BD34	IO_L23N_T3_11	S3_LVDS9_N	N	B11	A11	N	S3_LVDS10_N	IO_L17N_T2_11	BD38	
11	BC34	IO_L23P_T3_11	S3_LVDS9_P	P	B12	A12	P	S3_LVDS10_P	IO_L17P_T2_11	BC38	11
	AW39	IO_L15N_T2_DQS_11	S3_LVDS11_N	N	B13	A13	N	S3_LVDS12_N	IO_L10N_T1_11	BD39	
	AW38	IO_L15P_T2_DQS_11	S3_LVDS11_P	P	B14	A14	P	S3_LVDS12_P	IO_L10P_T1_11	BC39	
	AY35	IO_L20N_T3_11	S3_LVDS13_N	N	B15	A15	N	S3_LVDS14_N/CLK_N	IO_L11N_T1_SRCC_11	BB40	
	AW35	IO_L20P_T3_11	S3_LVDS13_P	P	B16	A16	P	S3_LVDS14_P/CLK_P	IO_L11P_T1_SRCC_11	BB39	
	BA39	IO_L13N_T2_MRCC_11	S3_LVDS15_N/CLK_N	N	B17	A17	N	S3_LVDS16_N	IO_L8N_T1_11	BD41	
	AY38	IO_L13P_T2_MRCC_11	S3_LVDS15_P/CLK_P	P	B18	A18	P	S3_LVDS16_P	IO_L8P_T1_11	BD40	
	BD36	IO_L21N_T3_DQS_11	S3_LVDS17_N	N	B19	A19	N	S3_LVDS18_N	IO_L7N_T1_11	BC41	
	BD35	IO_L21P_T3_DQS_11	S3_LVDS17_P	P	B20	A20	P	S3_LVDS18_P	IO_L7P_T1_11	BB41	
	BC36	IO_L24N_T3_11	S3_LVDS19_N	N	B21	A21	N	S3_LVDS20_N	IO_L9N_T1_DQS_11	BC43	
	BB36	IO_L24P_T3_11	S3_LVDS19_P	P	B22	A22	P	S3_LVDS20_P	IO_L9P_T1_DQS_11	BC42	
	BB34	IO_L19N_T3_VREF_11	S3_LVDS21_N/VREF	N	B23	A23	N	S3_LVDS22_N	IO_L18N_T2_11	AY37	
	BA34	IO_L19P_T3_11	S3_LVDS21_P	P	B24	A24	P	S3_LVDS22_P	IO_L18P_T2_11	AY36	

FPGA (Virtex-7)			Signal Name	QTH3(CN22)				Signal Name	FPGA (Virtex-7)		
Bank	Pin#	Pin Name		Pair	Pin#	Pin#	Pair		Pin Name	Pin#	Bank
12	AV37	IO_L24N_T3_12	S3_LVDS23_N	N	B25	A25	N	S3_LVDS24_N/VREF	IO_L6N_T0_VREF_12	AP36	12
	AV36	IO_L24P_T3_12	S3_LVDS23_P	P	B26	A26	P	S3_LVDS24_P	IO_L6P_T0_12	AN36	
	AV34	IO_L22N_T3_12	S3_LVDS25_N	N	B27	A27	N	S3_LVDS26_N	IO_L21N_T3_DQS_12	AU37	
	AU34	IO_L22P_T3_12	S3_LVDS25_P	P	B28	A28	P	S3_LVDS26_P	IO_L21P_T3_DQS_12	AU36	
	AU35	IO_L20N_T3_12	S3_LVDS27_N	N	B29	A29	N	S3_LVDS28_N	IO_L5N_T0_12	AR36	
	AT35	IO_L20P_T3_12	S3_LVDS27_P	P	B30	A30	P	S3_LVDS28_P	IO_L5P_T0_12	AR35	
	-	-	TPAD44	-	H3	H4	-	TPAD45	-	-	
	-	-	TPAD46	-	H5	H6	-	TPAD47	-	-	
	AP40	IO_L7N_T1_12	S3_LVDS29_N	N	B31	A31	N	S3_LVDS30_N/CLK_N	IO_L11N_T1_SRCC_12	AR41	
	AN39	IO_L7P_T1_12	S3_LVDS29_P	P	B32	A32	P	S3_LVDS30_P/CLK_P	IO_L11P_T1_SRCC_12	AR40	
	AT42	IO_L12N_T1_MRCC_12	S3_LVDS31_N/CLK_N	N	B33	A33	N	S3_LVDS32_N	IO_L8N_T1_12	AP44	
	AR42	IO_L12P_T1_MRCC_12	S3_LVDS31_P/CLK_P	P	B34	A34	P	S3_LVDS32_P	IO_L8P_T1_12	AP43	
	AP41	IO_L9N_T1_DQS_12	S3_LVDS33_N	N	B35	A35	N	S3_LVDS34_N	IO_L10N_T1_12	AT43	
	AN41	IO_L9P_T1_DQS_12	S3_LVDS33_P	P	B36	A36	P	S3_LVDS34_P	IO_L10P_T1_12	AR43	
	AT40	IO_L14N_T2_SRCC_12	S3_LVDS35_N	N	B37	A37	N	S3_LVDS36_N	IO_L15N_T2_DQS_12	AV41	
	AT39	IO_L14P_T2_SRCC_12	S3_LVDS35_P	P	B38	A38	P	S3_LVDS36_P	IO_L15P_T2_DQS_12	AU41	
	AT38	IO_L19N_T3_VREF_12	S3_LVDS37_N/VREF	N	B39	A39	N	S3_LVDS38_N	IO_L16N_T2_12	AU44	
	AT37	IO_L19P_T3_12	S3_LVDS37_P	P	B40	A40	P	S3_LVDS38_P	IO_L16P_T2_12	AT44	
	AV42	IO_L17N_T2_12	S3_LVDS39_N	N	B41	A41	N	S3_LVDS40_N/VREF	IO_L18N_T2_12	AV44	
	AU42	IO_L17P_T2_12	S3_LVDS39_P	P	B42	A42	P	S3_LVDS40_P	IO_L18P_T2_12	AV43	
	AP39	IO_L4N_T0_12	S3_LVDS41_N	N	B43	A43	N	S3_LVDS42_N	IO_L3N_T0_DQS_12	AP35	
	AP38	IO_L4P_T0_12	S3_LVDS41_P	P	B44	A44	P	S3_LVDS42_P	IO_L3P_T0_DQS_12	AP34	
	AR38	IO_L1N_T0_12	S3_LVDS43_N	N	B45	A45	N	S3_LVDS44_N	IO_L23N_T3_12	AV39	
	AR37	IO_L1P_T0_12	S3_LVDS43_P	P	B46	A46	P	S3_LVDS44_P	IO_L23P_T3_12	AV38	
	AN38	IO_L2N_T0_12	S3_LVDS45_N	N	B47	A47	N	S3_LVDS46_N/CLK_N	IO_L13N_T2_MRCC_12	AU40	
	AN37	IO_L2P_T0_12	S3_LVDS45_P	P	B48	A48	P	S3_LVDS46_P/CLK_P	IO_L13P_T2_MRCC_12	AU39	

FPGA (Virtex-7)			Signal Name	QTH3(CN22)				Signal Name	FPGA (Virtex-7)		
Bank	Pin#	Pin Name		Pair	Pin#	Pin#	Pair		Pin Name	Pin#	Bank
	AL37	IO_L11P_T1_SRCC_13	S3_LVDS47_N/CLK_N	N	B49	A49	N	S3_LVDS48_N	IO_L1N_T0_13	AK41	
	AL38	IO_L11N_T1_SRCC_13	S3_LVDS47_P/CLK_P	P	B50	A50	P	S3_LVDS48_P	IO_L1P_T0_13	AJ41	
	AH44	IO_L2N_T0_13	S3_LVDS49_N	N	B51	A51	N	S3_LVDS50_N	IO_L3N_T0_DQS_13	AK43	
	AH43	IO_L2P_T0_13	S3_LVDS49_P	P	B52	A52	P	S3_LVDS50_P	IO_L3P_T0_DQS_13	AK42	
	AH36	IO_L7P_T1_13	S3_LVDS53	-	B53	A53	N	S3_LVDS51_N/VREF	IO_L6N_T0_VREF_13	AJ40	
	AH37	IO_L8P_T1_13	S3_LVDS55/5V/12V	-	B54	A54	P	S3_LVDS51_P	IO_L6P_T0_13	AJ39	
	AH38	IO_L8N_T1_13	S3_LVDS56/5V	-	B55	A55	N	S3_LVDS52_N	IO_L4N_T0_13	AJ44	
13	AM36	IO_L9P_T1_DQS_13	S3_LVDS57/5V	-	B56	A56	P	S3_LVDS52_P	IO_L4P_T0_13	AJ43	13
	AM37	IO_L9N_T1_DQS_13	S3_LVDS58/5V	-	B57	A57	N	S3_LVDS54_N	IO_L5N_T0_13	AL40	
	AJ38	IO_L10P_T1_13	S3_LVDS59/TP	-	B58	A58	P	S3_LVDS54_P	IO_L5P_T0_13	AK40	
	AK38	IO_L10N_T1_13	S3_LVDS60/2.5V/3.3V	-	B59	A59	N	S3_LVDS_CLK1_N	IO_L12N_T1_MRCC_13	AK37	
			QTH3_VCC	-	B60	A60	P	S3_LVDS_CLK1_P	IO_L12P_T1_MRCC_13	AK36	
	-	-	(QTH3_VCC) *JP resistor not implemented	-	H7	H8	-	(QTH3_VCC) *JP resistor not implemented	-	-	

8.3. PCI Express / GTX Connector

The TB-7V-2000T-LSI board is equipped with two SAMTEC's "x8"(8Lane) connectors.
The CN23 can be used as a PCI Express connector and the CN24 as a GTX connector.
(the CN24 cannot be used a PCI Express connector).

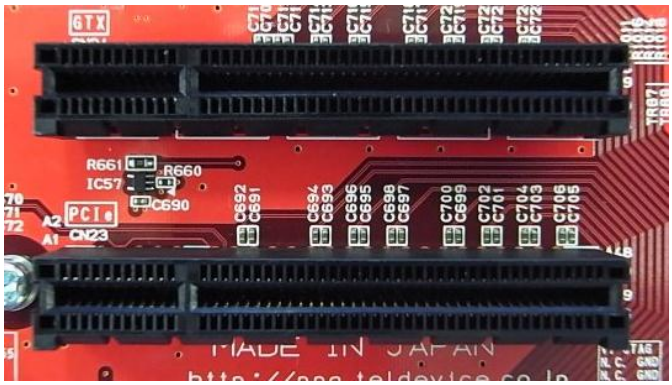


Figure 8-4 PCI Express Connector [CN23] / GTX Connector [CN24]

The following table lists the signal connections between the FPGA (Virtex-7) and the PCI Express Connector [CN23].

Table 8-26 Virtex-7 - PCI Express Connector [CN23] Signal Connections

PCI Express Connector1(CN23)		Signal Name	FPGA (Virtex-7)	
Pin No.	Pin Name		Pin No.	MGT_BANK
B14	PETp0	PCIE1_RX0_P	AP6	113
B15	PETn0	PCIE1_RX0_N	AP5	
A16	PERp0	PCIE1_TX0_P	AP2	
A17	PERn0	PCIE1_TX0_N	AP1	
B19	PETp1	PCIE1_RX1_P	AR4	
B20	PETn1	PCIE1_RX1_N	AR3	
A21	PERp1	PCIE1_TX1_P	AT2	
A22	PERn1	PCIE1_TX1_N	AT1	
B23	PETp2	PCIE1_RX2_P	AT6	
B24	PETn2	PCIE1_RX2_N	AT5	
A25	PERp2	PCIE1_TX2_P	AU4	
A26	PERn2	PCIE1_TX2_N	AU3	
B27	PETp3	PCIE1_RX3_P	AV6	
B28	PETn3	PCIE1_RX3_N	AV5	
A29	PERp3	PCIE1_TX3_P	AV2	
A30	PERn3	PCIE1_TX3_N	AV1	
B33	PETp4	PCIE1_RX4_P	AW4	112
B34	PETn4	PCIE1_RX4_N	AW3	
A35	PERp4	PCIE1_TX4_P	AY2	
A36	PERn4	PCIE1_TX4_N	AY1	
B37	PETp5	PCIE1_RX5_P	AY6	
B38	PETn5	PCIE1_RX5_N	AY5	
A39	PERp5	PCIE1_TX5_P	BA4	
A40	PERn5	PCIE1_TX5_N	BA3	
B41	PETp6	PCIE1_RX6_P	BB6	
B42	PETn6	PCIE1_RX6_N	BB5	
A43	PERp6	PCIE1_TX6_P	BB2	
A44	PERn6	PCIE1_TX6_N	BB1	
B45	PETp7	PCIE1_RX7_P	BD6	
B46	PETn7	PCIE1_RX7_N	BD5	
A47	PERp7	PCIE1_TX7_P	BC4	
A48	PERn7	PCIE1_TX7_N	BC3	

Table 8-27 shows the PCI Express Connector pin assignments.

Table 8-27 PCI Express Connector [CN23] Pin Assignments

CN23 B Side	Pin Name	Signal	CN23 A Side	Pin Name	Signal
B1	+12 V	-	A1	PRSNT1#	(PCIe1 PRSNT SEL)
B2	+12 V	-	A2	+12 V	-
B3	+12 V	-	A3	+12 V	-
B4	GND	GND	A4	GND	GND
B5	SMCLK	-	A5	JTAG2_TCK	-
B6	SMDAT	-	A6	JTAG3_TDI	-
B7	GND	GND	A7	JTAG4_TDO	-
B8	+3.3 V	-	A8	JTAG5_TMS	-
B9	JTAG1_TRST#	-	A9	+3.3 V	-
B10	+3.3 Vaux	-	A10	+3.3 V	-
B11	WAKE#	-	A11	PERST#	PCIE1_RESET_B
B12	RSVD_B12	-	A12	GND	GND
B13	GND	GND	A13	REFCLK+	PCIE1_REFCLK_P
B14	PETp0	PCIE1_RX0_P	A14	REFCLK-	PCIE1_REFCLK_N
B15	PETn0	PCIE1_RX0_N	A15	GND	GND
B16	GND	GND	A16	PERp0	PCIE1_TX0_P
B17	PRSNT2#	(PCIe1 PRSNT SEL)	A17	PERn0	PCIE1_TX0_N
B18	GND	GND	A18	GND	GND
B19	PETp1	PCIE1_RX1_P	A19	RSVD_A19	-
B20	PETn1	PCIE1_RX1_N	A20	GND	GND
B21	GND	GND	A21	PERp1	PCIE1_TX1_P
B22	GND	GND	A22	PERn1	PCIE1_TX1_N
B23	PETp2	PCIE1_RX2_P	A23	GND	GND
B24	PETn2	PCIE1_RX2_N	A24	GND	GND
B25	GND	GND	A25	PERp2	PCIE1_TX2_P
B26	GND	GND	A26	PERn2	PCIE1_TX2_N
B27	PETp3	PCIE1_RX3_P	A27	GND	GND
B28	PETn3	PCIE1_RX3_N	A28	GND	GND
B29	GND	GND	A29	PERp3	PCIE1_TX3_P
B30	RSVD_B30	-	A30	PERn3	PCIE1_TX3_N
B31	PRSNT2#	(PCIe1 PRSNT SEL)	A31	GND	GND
B32	GND	GND	A32	RSVD_A32	-
B33	PETp4	PCIE1_RX4_P	A33	RSVD_A33	-
B34	PETn4	PCIE1_RX4_N	A34	GND	GND
B35	GND	GND	A35	PERp4	PCIE1_TX4_P
B36	GND	GND	A36	PERn4	PCIE1_TX4_N
B37	PETp5	PCIE1_RX5_P	A37	GND	GND
B38	PETn5	PCIE1_RX5_N	A38	GND	GND
B39	GND	GND	A39	PERp5	PCIE1_TX5_P
B40	GND	GND	A40	PERn5	PCIE1_TX5_N
B41	PETp6	PCIE1_RX6_P	A41	GND	GND

CN23 B Side	Pin Name	Signal	CN23 A Side	Pin Name	Signal
B42	PETn6	PCIE1_RX6_N	A42	GND	GND
B43	GND	GND	A43	PERp6	PCIE1_TX6_P
B44	GND	GND	A44	PERn6	PCIE1_TX6_N
B45	PETp7	PCIE1_RX7_P	A45	GND	GND
B46	PETn7	PCIE1_RX7_N	A46	GND	GND
B47	GND	GND	A47	PERp7	PCIE1_TX7_P
B48	PRSNT2#	(PCIe1 PRSNT SEL)	A48	PERn7	PCIE1_TX7_N
B49	GND	GND	A49	GND	GND

Table 8-28 shows the signal connections between FPGA (Virtex-7) and GTX connector [CN24].

Table 8-28 Signal Connections between Virtex-7 and GTX Connector [CN24]

GTX Connector(CN24)		Signal Name	FPGA (Virtex-7)	
Pin No.	Pin Name		Pin No.	MGT_BANK
B14	PETp0	GTX_TX0_P	AD2	115
B15	PETn0	GTX_TX0_N	AD1	
A16	PERp0	GTX_RX0_P	AD6	
A17	PERn0	GTX_RX0_N	AD5	
B19	PETp1	GTX_TX1_P	AE4	
B20	PETn1	GTX_TX1_N	AE3	
A21	PERp1	GTX_RX1_P	AE8	
A22	PERn1	GTX_RX1_N	AE7	
B23	PETp2	GTX_TX2_P	AF2	
B24	PETn2	GTX_TX2_N	AF1	
A25	PERp2	GTX_RX2_P	AF6	
A26	PERn2	GTX_RX2_N	AF5	
B27	PETp3	GTX_TX3_P	AG4	
B28	PETn3	GTX_TX3_N	AG3	
A29	PERp3	GTX_RX3_P	AH6	
A30	PERn3	GTX_RX3_N	AH5	
B33	PETp4	GTX_TX4_P	AH2	114
B34	PETn4	GTX_TX4_N	AH1	
A35	PERp4	GTX_RX4_P	AJ4	
A36	PERn4	GTX_RX4_N	AJ3	
B37	PETp5	GTX_TX5_P	AK2	
B38	PETn5	GTX_TX5_N	AK1	
A39	PERp5	GTX_RX5_P	AK6	
A40	PERn5	GTX_RX5_N	AK5	
B41	PETp6	GTX_TX6_P	AL4	
B42	PETn6	GTX_TX6_N	AL3	
A43	PERp6	GTX_RX6_P	AM6	
A44	PERn6	GTX_RX6_N	AM5	
B45	PETp7	GTX_TX7_P	AM2	
B46	PETn7	GTX_TX7_N	AM1	
A47	PERp7	GTX_RX7_P	AN4	
A48	PERn7	GTX_RX7_N	AN3	

Table 8-29 shows the GTX connector pin assignments.

Table 8-29 GTX Connector [CN24] Pin Assignments

CN24 B Side	Pin Name	Signal	CN24 A Side	Pin Name	Signal
B1	+12 V	-	A1	PRSNT1#	-
B2	+12 V	-	A2	+12 V	-
B3	+12 V	-	A3	+12 V	-
B4	GND	GND	A4	GND	GND
B5	SMCLK	-	A5	JTAG2_TCK	-
B6	SMDAT	-	A6	JTAG3_TDI	-
B7	GND	GND	A7	JTAG4_TDO	-
B8	+3.3 V	-	A8	JTAG5_TMS	-
B9	JTAG1_TRST#	-	A9	+3.3 V	-
B10	+3.3 Vaux	-	A10	+3.3 V	-
B11	WAKE#	-	A11	PERST#	-
B12	RSVD_B12	-	A12	GND	GND
B13	GND	GND	A13	REFCLK+	-
B14	PETp0	GTX_TX0_P	A14	REFCLK-	-
B15	PETn0	GTX_TX0_N	A15	GND	GND
B16	GND	GND	A16	PERp0	GTX_RX0_P
B17	PRSNT2#	-	A17	PERn0	GTX_RX0_N
B18	GND	GND	A18	GND	GND
B19	PETp1	GTX_TX1_P	A19	RSVD_A19	-
B20	PETn1	GTX_TX1_N	A20	GND	GND
B21	GND	GND	A21	PERp1	GTX_RX1_P
B22	GND	GND	A22	PERn1	GTX_RX1_N
B23	PETp2	GTX_TX2_P	A23	GND	GND
B24	PETn2	GTX_TX2_N	A24	GND	GND
B25	GND	GND	A25	PERp2	GTX_RX2_P
B26	GND	GND	A26	PERn2	GTX_RX2_N
B27	PETp3	GTX_TX3_P	A27	GND	GND
B28	PETn3	GTX_TX3_N	A28	GND	GND
B29	GND	GND	A29	PERp3	GTX_RX3_P
B30	RSVD_B30	-	A30	PERn3	GTX_RX3_N
B31	PRSNT2#	-	A31	GND	GND
B32	GND	GND	A32	RSVD_A32	-
B33	PETp4	GTX_TX4_P	A33	RSVD_A33	-
B34	PETn4	GTX_TX4_N	A34	GND	GND
B35	GND	GND	A35	PERp4	GTX_RX4_P
B36	GND	GND	A36	PERn4	GTX_RX4_N
B37	PETp5	GTX_TX5_P	A37	GND	GND
B38	PETn5	GTX_TX5_N	A38	GND	GND
B39	GND	GND	A39	PERp5	GTX_RX5_P
B40	GND	GND	A40	PERn5	GTX_RX5_N
B41	PETp6	GTX_TX6_P	A41	GND	GND

CN24 B Side	Pin Name	Signal	CN24 A Side	Pin Name	Signal
B42	PETn6	GTX_TX6_N	A42	GND	GND
B43	GND	GND	A43	PERp6	GTX_RX6_P
B44	GND	GND	A44	PERn6	GTX_RX6_N
B45	PETp7	GTX_TX7_P	A45	GND	GND
B46	PETn7	GTX_TX7_N	A46	GND	GND
B47	GND	GND	A47	PERp7	GTX_RX7_P
B48	PRSNT2#	-	A48	PERn7	GTX_RX7_N
B49	GND	GND	A49	GND	GND

8.4. USB3.0

The TB-7V-2000T-LSI board is equipped with a Cypress USB Super Speed Peripherals equivalent CYUSB3014 and a SAMTEC USB3.0 TYPE-B connector. In addition, it is also equipped with I2S interface, I2C interface, RS232C interface, RS232C pin header and SPI Flash for firmware storage.

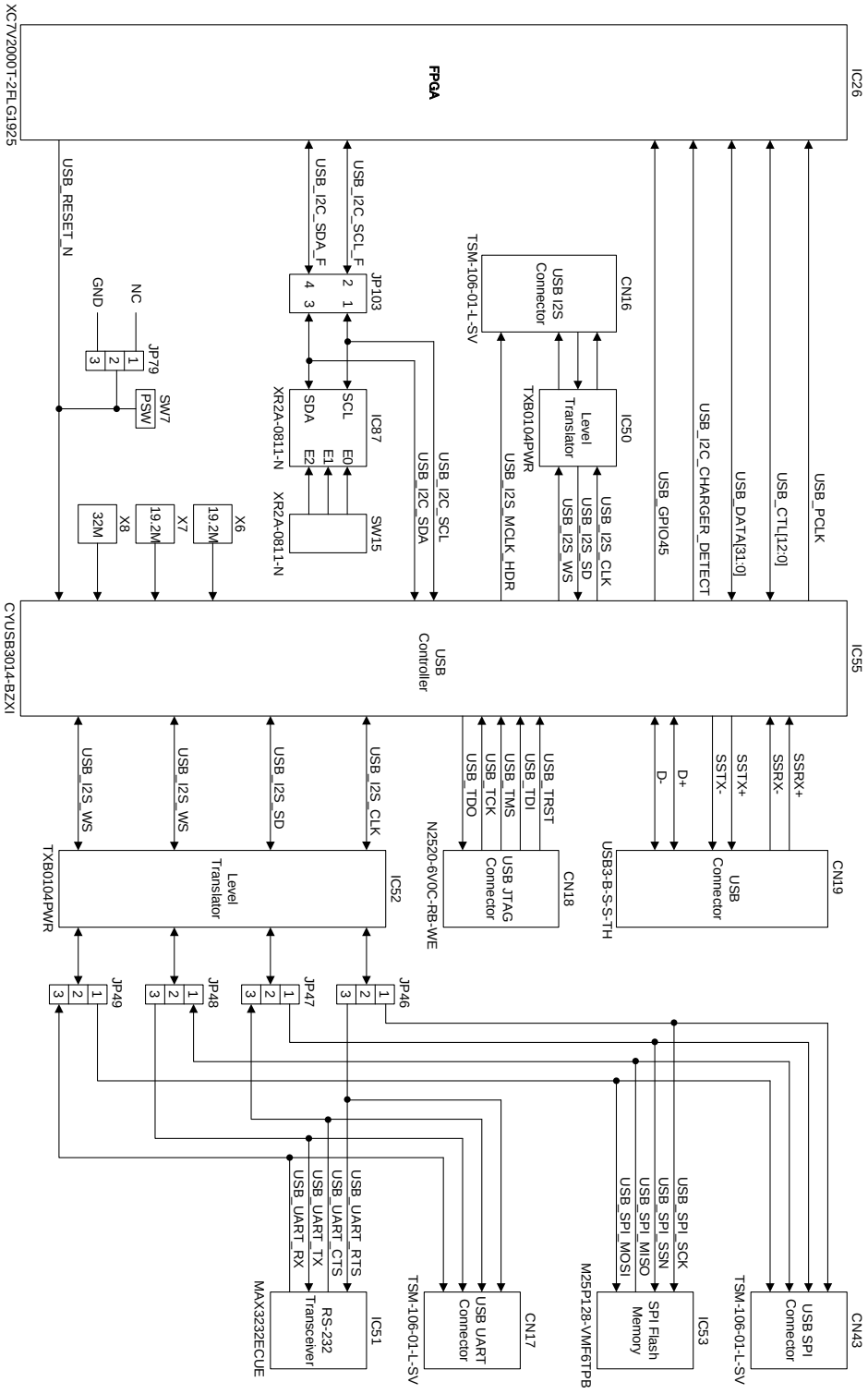


Figure 8-5 USB3.0 Structure

Table 8-30 shows the signal connections between FPGA (Virtex-7) and USB3.0Controller.

Table 8-30 USB3.0 Controller Pin Assignments

(IC55) Pin Name	Signal Name	FPGA(Virtex-7)	
		Pin No.	Bank
RESET#	USB_RESET_N	AU24	34
INT#	USB_INT_N	AU25	
O60	USB_I2C_CHARGER_DETECT	AJ21	
GPIO29	USB_CTL12	AY23	
GPIO28	USB_CTL11	AY22	
GPIO27	USB_CTL10	AV22	
GPIO26	USB_CTL9	AU22	
GPIO25	USB_CTL8	BA25	
GPIO24	USB_CTL7	AY25	
GPIO23	USB_CTL6	AW23	
GPIO22	USB_CTL5	AV23	
GPIO21	USB_CTL4	BA23	
GPIO20	USB_CTL3	BA22	
GPIO19	USB_CTL2	BD23	
GPIO18	USB_CTL1	BC23	
GPIO17	USB_CTL0	BC22	
GPIO49	USB_DATA31	BB22	
GPIO48	USB_DATA30	BD25	
GPIO47	USB_DATA29	BD24	
GPIO46	USB_DATA28	BB25	
GPIO44	USB_DATA27	BA24	
GPIO43	USB_DATA26	BC24	
GPIO42	USB_DATA25	BB24	
GPIO41	USB_DATA24	AW25	
GPIO40	USB_DATA23	AJ18	33
GPIO39	USB_DATA22	AM19	
GPIO38	USB_DATA21	AL19	
GPIO37	USB_DATA20	AJ19	
GPIO36	USB_DATA19	AJ20	
GPIO35	USB_DATA18	AL20	
GPIO34	USB_DATA17	AK20	
GPIO33	USB_DATA16	AL17	
GPIO15	USB_DATA15	AK17	
GPIO14	USB_DATA14	AN19	
GPIO13	USB_DATA13	AM20	
GPIO12	USB_DATA12	AL18	
GPIO11	USB_DATA11	AK18	
GPIO10	USB_DATA10	AT18	
GPIO9	USB_DATA9	AR18	
GPIO8	USB_DATA8	AP19	

(IC55) Pin Name	Signal Name	FPGA(Virtex-7)	
		Pin No.	Bank
GPIO7	USB_DATA7	AP20	33
GPIO6	USB_DATA6	AP18	
GPIO5	USB_DATA5	AN18	
GPIO4	USB_DATA4	AR21	
GPIO3	USB_DATA3	AP21	
GPIO2	USB_DATA2	AU20	
GPIO1	USB_DATA1	AU21	
GPIO0	USB_DATA0	AT20	
GPIO16	USB_PCLK	AR20	
GPIO45	USB_GPIO45	AV21	

8.4.1. USB3.0 TYPE-B Connector

The TB-7V-2000T-LSI board is equipped with one SAMTEC USB3.0 TYPE-B connector.

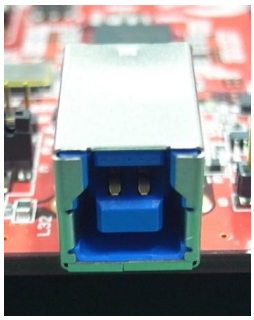


Figure 8-6 USB3.0 TYPE-B Connector

8.4.2. I2S Connector

The TB-7V-2000T-LSI board is equipped with one I2S interface that is connected to the CYUSB3014.

Figure 8-7 I2S Connector

Table 8-31 I2S Connector Pin Assignments

Device		Signal Name
Name	Pin No.	
CN16 (I2S Connector)	1	V7_VCC+3.3V
	2	USB_I2S_CLK_HDR
	3	USB_I2S_SD_ HDR
	4	USB_I2S_ WS_HDR
	5	USB_I2S_MCLK_HDR
	6	GND

8.4.3. SPI Connector and SPI Flash Memory

The TB-7V-2000T-LSI board is equipped with one SPI connector that is connected to the CYUSB3014. It is also equipped with one SPI Flash Memory for firmware storage.

*Either SPI or RS232C can be used. For more information, refer to the section “IFSELJumper”.

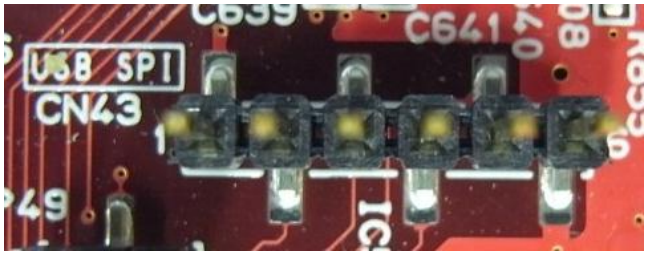


Figure 8-8 Onboard SPI Connector

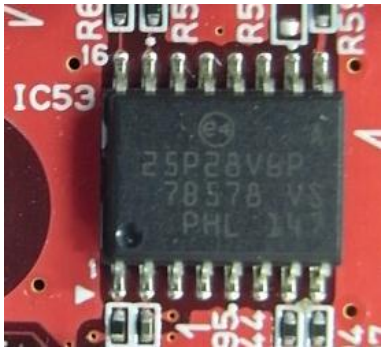


Figure 8-9 Onboard SPI Flash Memory

Table 8-32 SPI Connector Pin Assignments

Device		Signal Name
Name	Pin No.	
CN43	1	V7_VCC+3.3V
	2	USB_SPI_MOSI
	3	USB_SPI_MISO
	4	USB_SPI_SCK
	5	USB_SPI_SSN
	6	GND

8.4.4. I2C Interface

The TB-7V-2000T-LSI board is equipped with one I2C interface that is connected to the CYUSB3014 and the FPGA (Virtex-7). I2C device addresses E0 through E2 can be defined using SW15.

*I2C device is not implemented (only socket is provided).

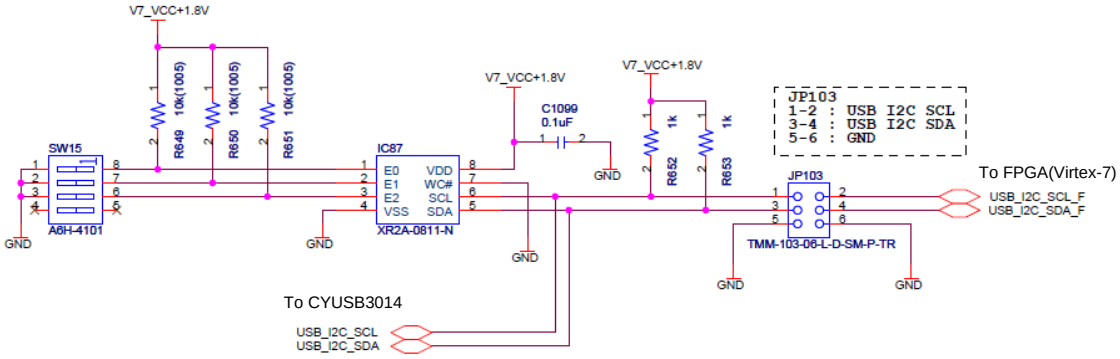


Figure 8-10 I2C Interface Structure

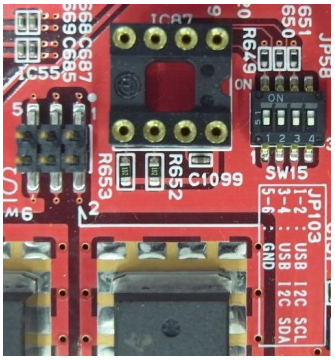


Figure 8-11 Onboard I2C Interface

Table 8-33 SW Pin Assignments for I2C Device Configuration

SW15	
Pin No.	Signal Name
bit1	IC87 E0 pin (SW ON=Low, OFF=High)
bit2	IC87 E1 pin (SW ON=Low, OFF=High)
bit2	IC87 E2 pin (SW ON=Low, OFF=High)
bit3	Reserved

To allow access to IC87 via FPGA (Virtex-7), short JP103 as shown in Table 8-34.

Table 8-34 Jumper Settings for FPGA Access

JP103	
Pin No.	Signal Name
1-2	USB_I2S_SCL_ F
3-4	USB_I2S_SDA_ F

8.4.5. RS232C Connector

The TB-7V-2000T-LSI board is equipped with a RS232C interface that is connected to the CYUSB3014.
*Either SPI or RS232C can be used. For more information, refer to the section “IFSELJumper”.

Figure 8-12 RS232C Connector

Table 8-35 RS232C Connector Pin Assignments

Device		Signal Name
Name	Pin No.	
CN17	1	CN_USB_UART_TXD
	2	CN_USB_UART_RXD
	3	CN_USB_UART_RTS
	4	CN_USB_UART_CTS
	5	GND

8.4.6. IFSEL Jumpers

The TB-7V-2000T-LSI board is equipped with four IFSEL jumpers that are used to select either SPI or RS232C interface on the CYUSB3014.

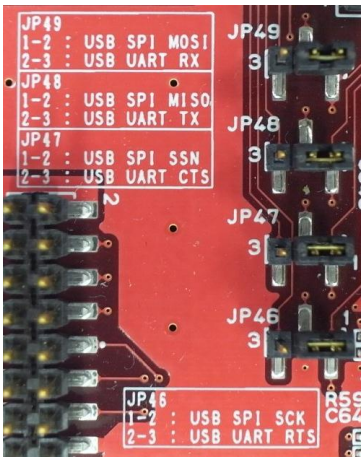


Figure 8-13 Onboard IFSEL Jumpers

Table 8-36 IFSEL Jumper Settings

JP46,JP47,JP48,JP49	IF SEL
1-2	SPI
3-4	RS232C

8.4.7. USB JTAG Connector

The TB-7V-2000T-LSI board is equipped with a CYUSB3014 dedicated JTAG connector.

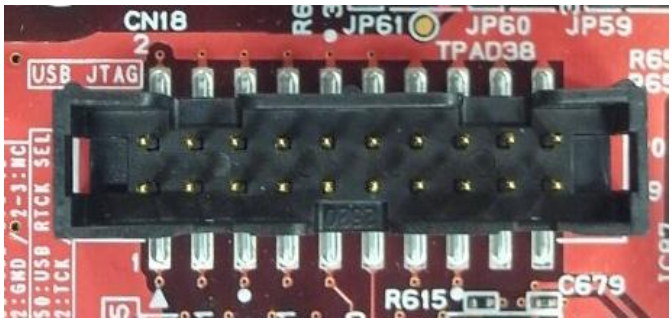


Figure 8-14 Onboard USB JTAG Connector

Table 8-37 USB JTAG Connector Pin Assignments

CN18		VCC / GND / N.C.	IC55 (CYUSB3014)	
Pin No.	Pin Name		Pin Name	Pin No.
1	VT_REF	USB_VIO+1.8V	-	-
2	V_SUPPLY	USB_VIO+1.8V	-	-
3	N_TRST		TRST#	B11
4	GND1	GND	-	-
5	TDI		TDI	E7
6	GND2	GND	-	-
7	TMS		TMS	E8
8	GND3	GND	-	-
9	TCK		TCK	F6
10	GND4	GND	-	-
11	RTCK	*1	-	-
12	GND5	GND	-	-
13	TDO		TDO	C10
14	GND6	GND	-	-
15	N_SRST	USB_VIO+1.8V	-	-
16	GND7	GND	-	-
17	DBGRQ	N.C.	-	-
18	GND8	GND	-	-
19	DBGACK	N.C.	-	-
20	GND9	GND	-	-

*1: Type of RTCK can be selected using a JP50.

Table 8-38 RTCK SEL Jumper Settings

JP50	RTCK SEL
1-2	TCK
2-3	GND

8.4.8. PMODE Jumpers

The TB-7V-2000T-LSI board is equipped with three PMODE jumpers that are used to select type of PMODE of CYUSB3014.

Figure 8-15 Onboard PMODE Jumpers

Table 8-39 PMODE Jumper Settings

JP53	JP52	JP51	PMODE
NC	2-3	2-3	Sync ADMUX(16bit)
NC	2-3	1-2	Async ADMUX(16bit)
NC	1-2	1-2	USB*
NC	2-3	NC	Async SRAM(16bit)
NC	1-2	NC	I2C => USB*
1-2	NC	NC	I2C*
2-3	NC	1-2	USB => USB*

*Only these modes are supported by the board.

8.4.9. CLK Jumper

The boad is equipped with a CLK jumper [JP54] that is used to set CYUSB3014 [IC55] input clock.

*Be sure to set JP54 either to CLKIN or XTAL.

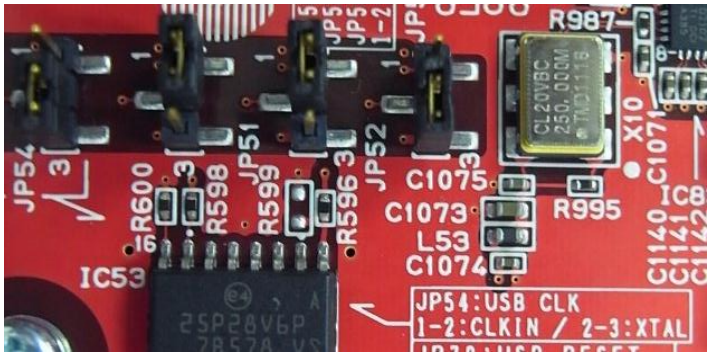


Figure 8-16 Onboard CLK Jumper [JP54]

Table 8-40 CLK Jumper [JP54] Settings

JP54	CLK SEL
1-2	CLKIN
2-3	XTAL

8.4.10. OTG_ID

The TB-7V-2000T-LSI board is equipped with an OTG ID jumper [JP55] that is used to set CYUSB3014 [IC55] OTG_ID input.

Figure 8-17 Onboard OTG ID Jumper [JP55]

Table 8-41 OTG ID Jumper [JP55] Settings

JP55	OTG ID SEL
1-2	GND
2-3	NC

8.4.11. Reset

The TB-7V-2000T-LSI board will allow the user to control the CYUSB3014 [IC55] reset either by Push SW, Jumper or Virtex-7 [IC26].

- SW7: Pressing and holding the switch (causing the output to go LOW) will assert the CYUSB3014 [IC55] reset.
- JP79: Shorting pin #2 and #3 will assert the CYUSB3014 [IC55] reset.
- Virtex-7 [IC26]: The CYUSB3014 [IC55] reset can be controlled by AU24 pin, Bank34 on Virtex-7 [IC26].

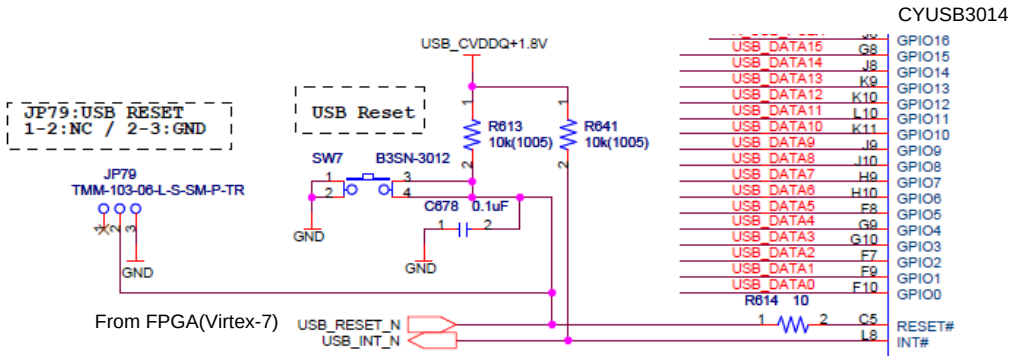


Figure 8-18 Reset Structure

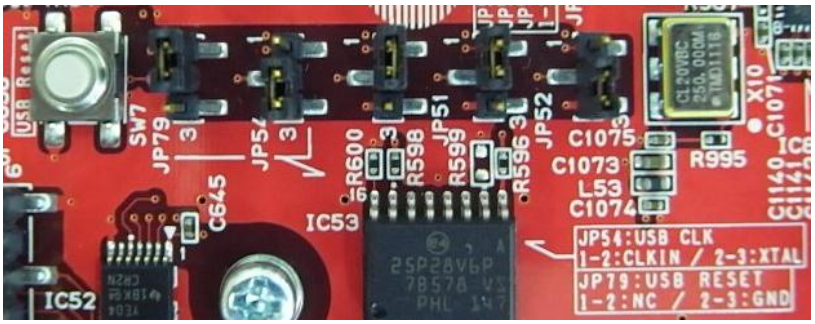


Figure 8-19 Onboard Reset Circuits

8.5. DVI

The TB-7V-2000T-LSI board is equipped with single mode DVI Tx and DVI Rx.

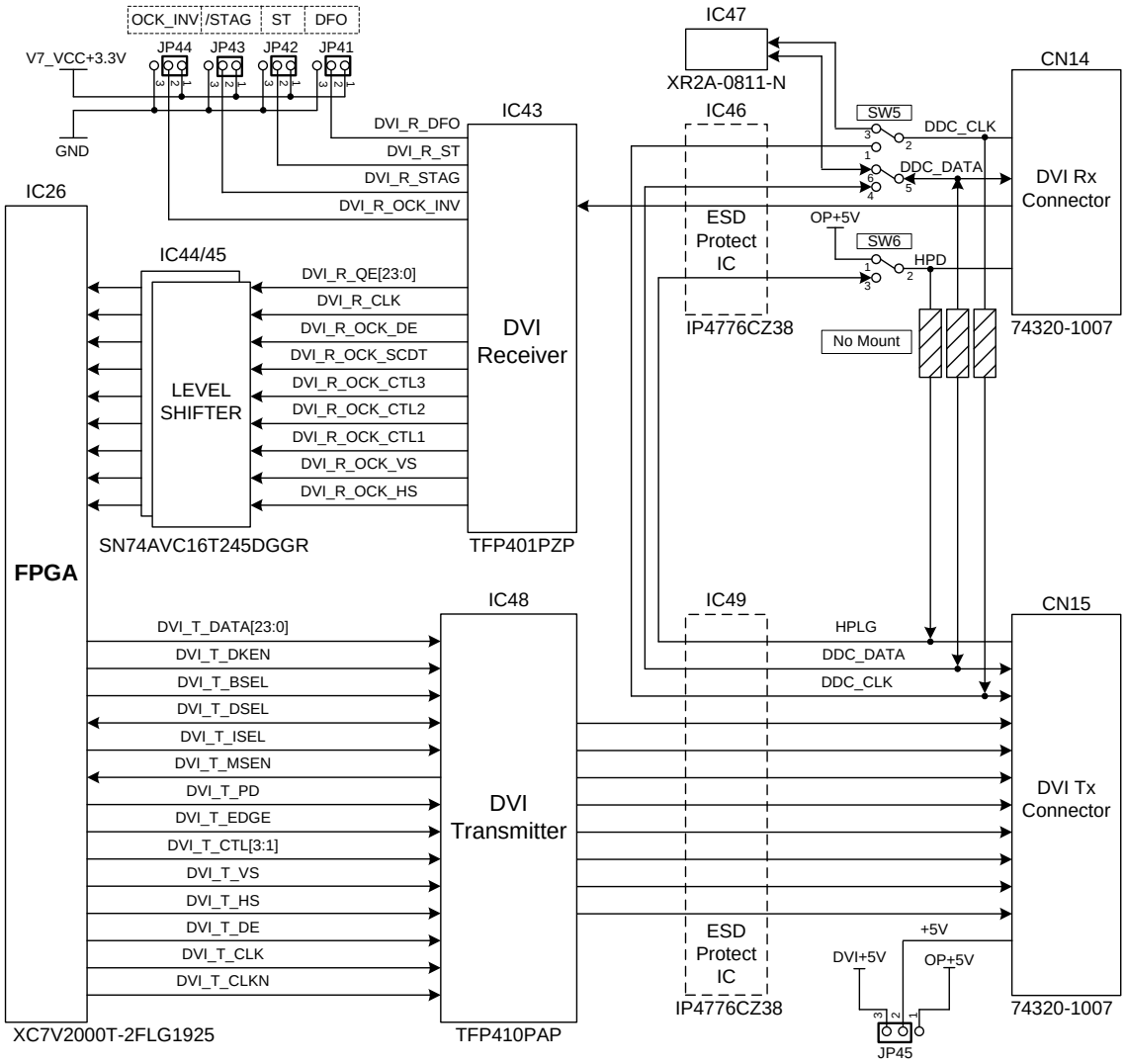


Figure 8-20 DVI Interface Structure (Rx/Tx)

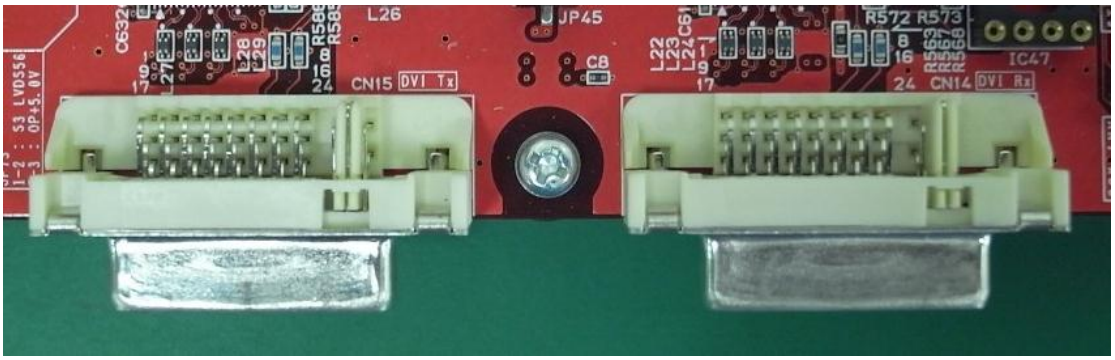


Figure 8-21 Onboard DVI Interface (Rx/Tx)

8.5.1. DVI_Rx

The TB-7V-2000T-LSI board is equipped with an external input dedicated DVI interface.

*For information on how to configure the DVI Receiver and JP41, JP42, JP43 and JP44, refer to the TI's TFP401PZP Data Sheet. Information on SW5 and SW6 will be described later in this section.

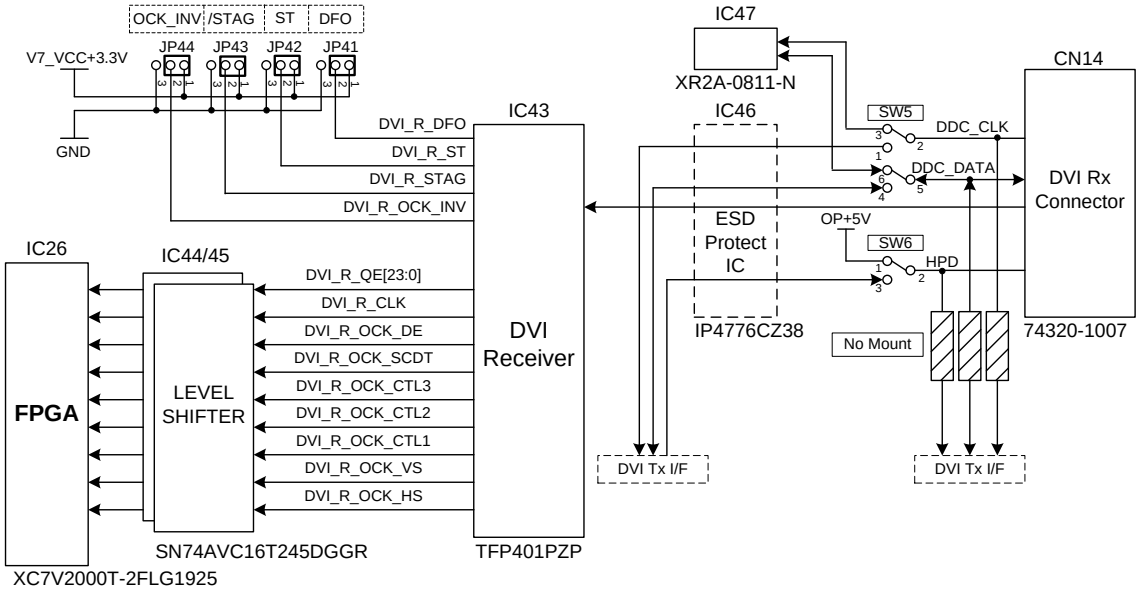


Figure 8-22 DVI Interface Structure (Rx)

Table 8-42 shows the signal connections between SN74AVC16T245DGGR and FPGA (Virtex-7).

Table 8-42 DVI Rx Pin Assignments

Device		FPGA (Virtex-7)		
Name	Signal Name	Pin No.	Bank	Level
IC44	V7_DVI_R_QE0	W33	16	1.8V
	V7_DVI_R_QE1	W34		
	V7_DVI_R_QE2	Y35		
	V7_DVI_R_QE3	Y36		
	V7_DVI_R_QE4	Y42		
	V7_DVI_R_QE5	Y43		
	V7_DVI_R_QE6	Y38		
	V7_DVI_R_QE7	Y37		
	V7_DVI_R_QE8	W36		
	V7_DVI_R_QE9	W35		
	V7_DVI_R_QE10	V39		
	V7_DVI_R_QE11	V38		
	V7_DVI_R_QE12	U42		
	V7_DVI_R_QE13	U41		
	V7_DVI_R_QE14	U40		
	V7_DVI_R_QE15	U39		

Device		FPGA (Virtex-7)		
Name	Signal Name	Pin No.	Bank	Level
IC45	V7_DVI_R_QE16	V37	16	1.8V
	V7_DVI_R_QE17	U37		
	V7_DVI_R_QE18	V36		
	V7_DVI_R_QE19	U36		
	V7_DVI_R_QE20	U35		
	V7_DVI_R_QE21	V34		
	V7_DVI_R_QE22	U34		
	V7_DVI_R_QE23	V33		
	V7_DVI_R_CLK	V41		
	V7_DVI_R_CTL1	W44		
	V7_DVI_R_CTL2	W43		
	V7_DVI_R_CTL3	V44		
	V7_DVI_R_DE	V43		
	V7_DVI_R_VS	V32		
	V7_DVI_R_HS	V31		
	V7_DVI_R_SCDT	U30		

8.5.2. DVI_Tx

The TB-7V-2000T-LSI board is equipped with an external output dedicated DVI interface.

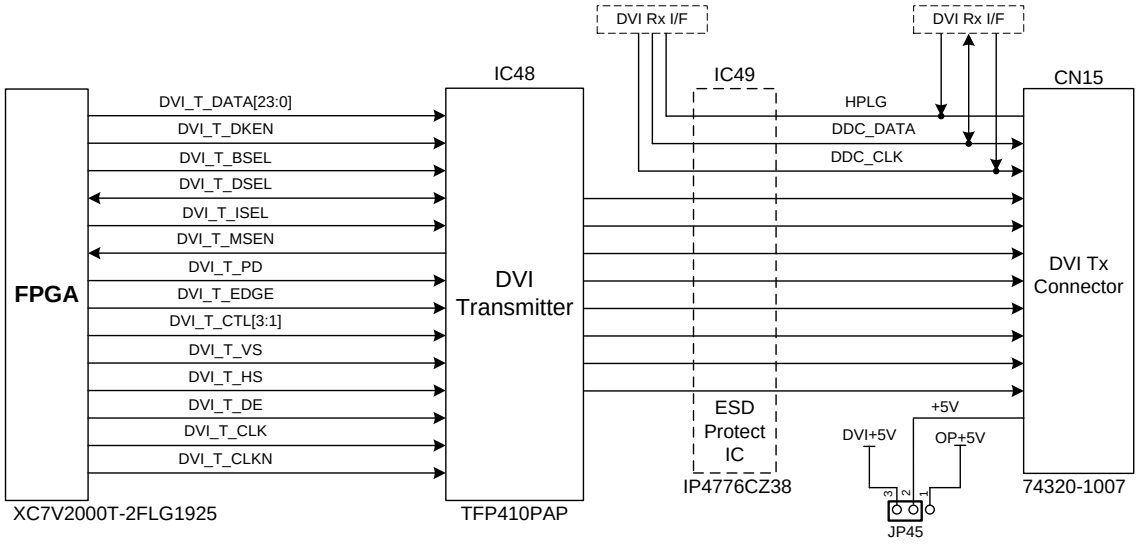


Figure 8-23 DVI Interface Structure (Tx)

Table 8-43 shows the signal connections between TFP410PAP and FPGA (Virtex-7).

Table 8-43 DVI Tx Pin Assignments

Device		FPGA (Virtex-7)		
Name	Signal Name	Pin No.	Bank	Level
IC48	DVI_T_DATA0	AA37	15	1.8V
	DVI_T_DATA1	AB39		
	DVI_T_DATA2	AB35		
	DVI_T_DATA3	AB42		
	DVI_T_DATA4	AB34		
	DVI_T_DATA5	AB37		
	DVI_T_DATA6	AA34		
	DVI_T_DATA7	AB36		
	DVI_T_DATA8	AA33		
	DVI_T_DATA9	AC34		
	DVI_T_DATA10	AA32		
	DVI_T_DATA11	AC36		
	DVI_T_DATA12	AC37		
	DVI_T_DATA13	AD38		
	DVI_T_DATA14	AD36		
	DVI_T_DATA15	AC38		
	DVI_T_DATA16	AD35		
	DVI_T_DATA17	AD39		
	DVI_T_DATA18	AD34		
	DVI_T_DATA19	AD40		
	DVI_T_DATA20	AC33		
	DVI_T_DATA21	AC39		
	DVI_T_DATA22	AD33		
	DVI_T_DATA23	AC42		
	DVI_T_CTL1	AB29		
	DVI_T_CTL2	AB44		
	DVI_T_CTL3	AC44		
	DVI_T_VS	AB31		
	DVI_T_HS	AC43		
	DVI_T_DE	AC32		
	DVI_T_DSEL	AA42		
	DVI_T_EDGE	AA43		
	DVI_T_PD	AB30		
	DVI_T_MSEN	AA44		
	DVI_T_DKEN	AA29		
	DVI_T_BSEL	AA30		
	DVI_T_ISEL	AC31		
	DVI_T_CLK	AB40		
	DVI_T_CLKN	AA40		

8.5.3. DVI_Rx- DVI_Tx Connections

SW5 and SW6 allow the user to switch the DVI_Rx- DVI_Tx connections.

Figure 8-24 shows the SW5/SW6 structure.

SW5: DDC switchover

SW6: Hot-Plug switchover

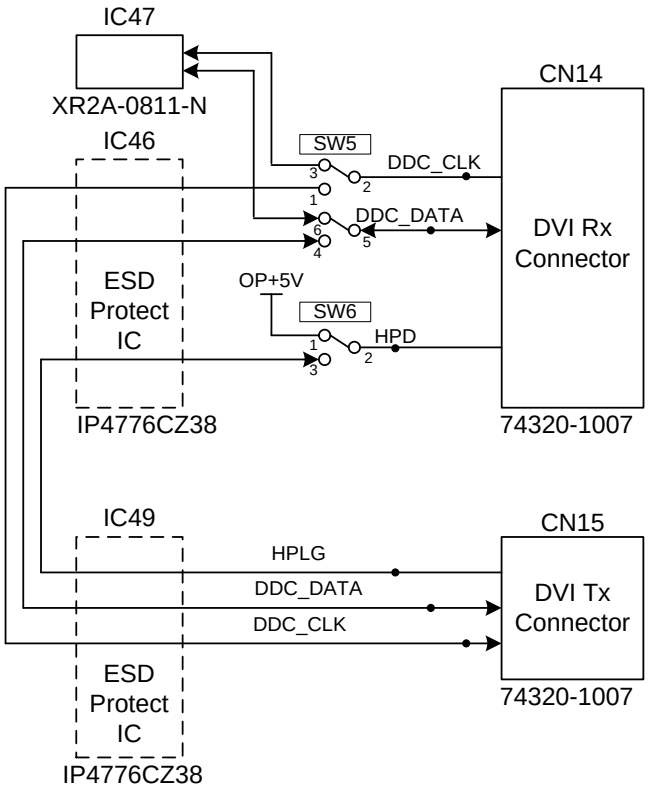


Figure 8-24 SW5/SW6 Structure

Figure 8-25 Onboard SW5 and SW6

*The SW5 and SW6 settings may be a little difficult.

In the above figure, short the pins as follows:

SW5: 2-1 and 5-4 (simultaneously switching DVI_Rx- DVI_Tx connections)

SW6: 2-3

Table 8-44 DVI_Rx- DVI_Tx Connections

Connecter		Pin Description	Device Name		Connect Destination
Name	Pin No.				
CN14 (DVI_Rx CN)	6	DDC_CLK	SW5	2-3	EEPROM
				2-1	(DVI_Tx CN) Pin No.6
	7	DDC_DATA		5-6	EEPROM
				5-4	(DVI_Tx CN) Pin No.7
	16	HPD	SW6	2-1	OP+5V
				2-3	(DVI_Tx CN) Pin No.16

8.6. RS-232C

The TB-7V-2000T-LSI board is equipped with a RS-232C interface for external communication purposes.

FPGA connections can be switched using jumpers.

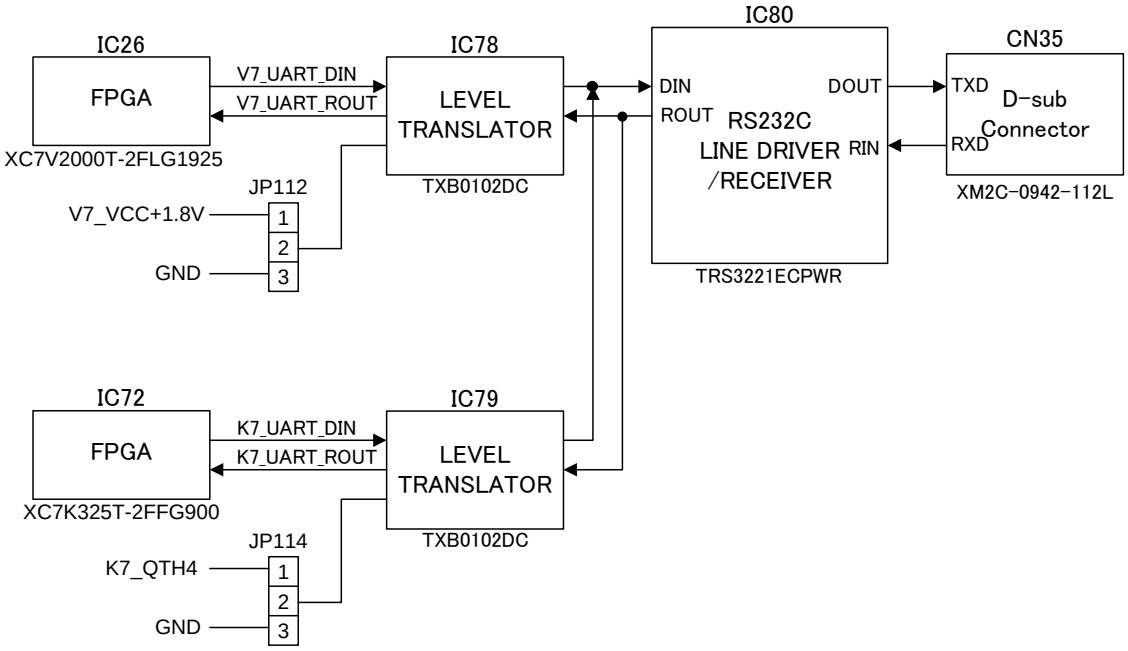


Figure 8-26 RS-232C Structure

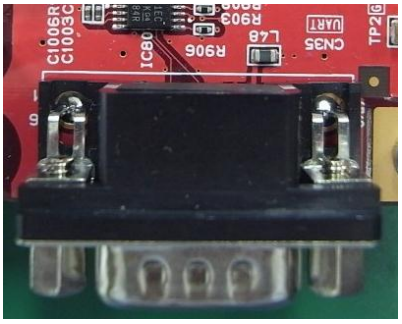


Figure 8-27 Onboard D-sub Connector

Table 8-45 FPGA Signal Connections

FPGA	Pin No.	Signal Name	Bank	Level
Virtex-7	AD29	V7_UART_DIN	15	1.8V
	AB32	V7_UART_ROUT		
Kintex-7	T20	K7_UART_DIN	14	1.8V/2.5V/3.3V
	T21	K7_UART_ROUT		

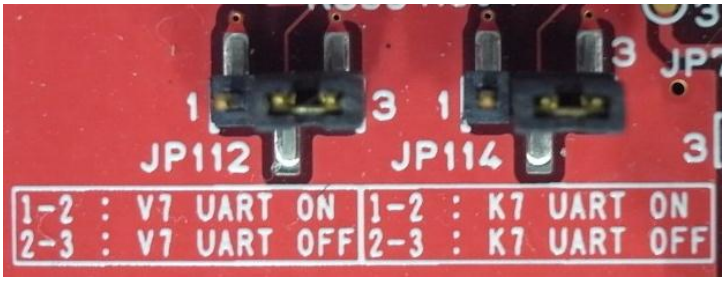


Figure 8-28 Onboard FPGA Switching Jumpers

Table 8-46 FPGA(Virtex-7) Switching Jumper Settings

JP112	FPGA SEL
1-2	V7 UART ON
2-3	V7 UART OFF

Table 8-47 FPGA(Kintex-7) Switching Jumper Setting

JP114	FPGA SEL
1-2	K7 UART ON
2-3	K7 UART OFF

*Do not attempt to turn on Virtex-7 UART and Kintex-7 UART simultaneously.

8.7. PinHeader

The TB-7V-2000T-LSI board is equipped with two 16-pin pinheaders (of them, 12 pins are used for FPGA signal connections).

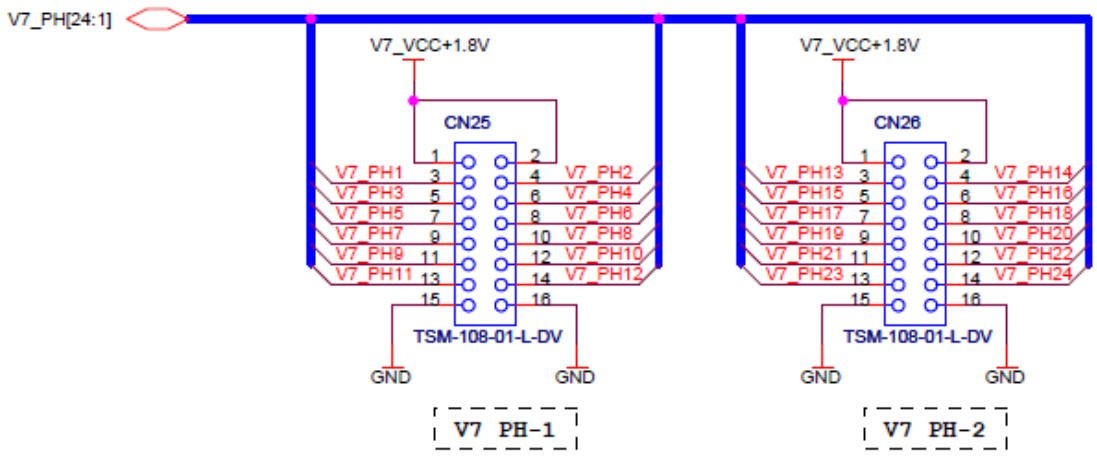


Figure 8-29 PinHeader Structure

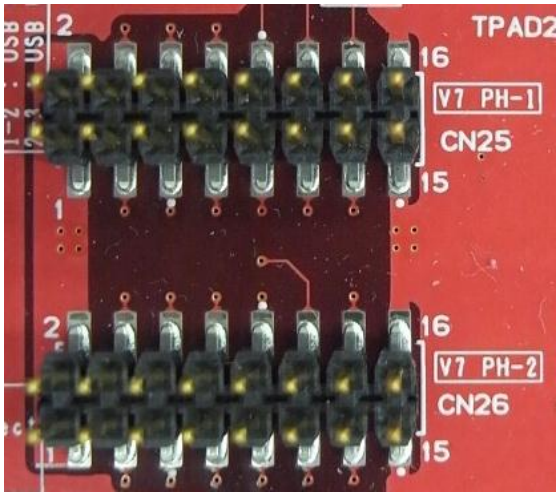


Figure 8-30 Onboard PinHeaders

Table 8-48 PinHeader (CN25) Pin Assignments

FPGA(Virtex-7)		PinHeader CN25				FPGA(Virtex-7)	
Bank	Pin No.	Signal Name	Pin No.		Signal Name	Pin No.	Bank
-	-	V7_VCC+1.8V	1	2	V7_VCC+1.8V	-	-
14	AH29	V7_PH1	3	4	V7_PH2	AF29	14
14	AF30	V7_PH3	5	6	V7_PH4	AJ29	14
14	AJ30	V7_PH5	7	8	V7_PH6	AG31	14
14	AH31	V7_PH7	9	10	V7_PH8	AJ28	14
15	AA35	V7_PH9	11	12	V7_PH10	AB28	15
16	U32	V7_PH11	13	14	V7_PH12	Y40	16
-	-	GND	15	16	GND	-	-

Table 8-49 PinHeader (CN26) Pin Assignments

FPGA(Virtex-7)		PinHeader CN26				FPGA(Virtex-7)	
Bank	Pin No.	Signal Name	Pin No.		Signal Name	Pin No.	Bank
-	-	V7_VCC+1.8V	1	2	V7_VCC+1.8V	-	-
16	W40	V7_PH13	3	4	V7_PH14	V42	16
16	Y41	V7_PH15	5	6	V7_PH16	W41	16
16	U31	V7_PH17	7	8	V7_PH18	Y32	16
16	Y33	V7_PH19	9	10	V7_PH20	W30	16
16	W31	V7_PH21	11	12	V7_PH22	Y30	16
16	Y31	V7_PH23	13	14	V7_PH24	W29	16
-	-	GND	15	16	GND	-	-

8.8. DipSW

The TB-7V-2000T-LSI board is equipped with three 8-position DIPSWs for Virtex-7.
When the DIPSW is switched on, then there is “low” level on FPGA input.

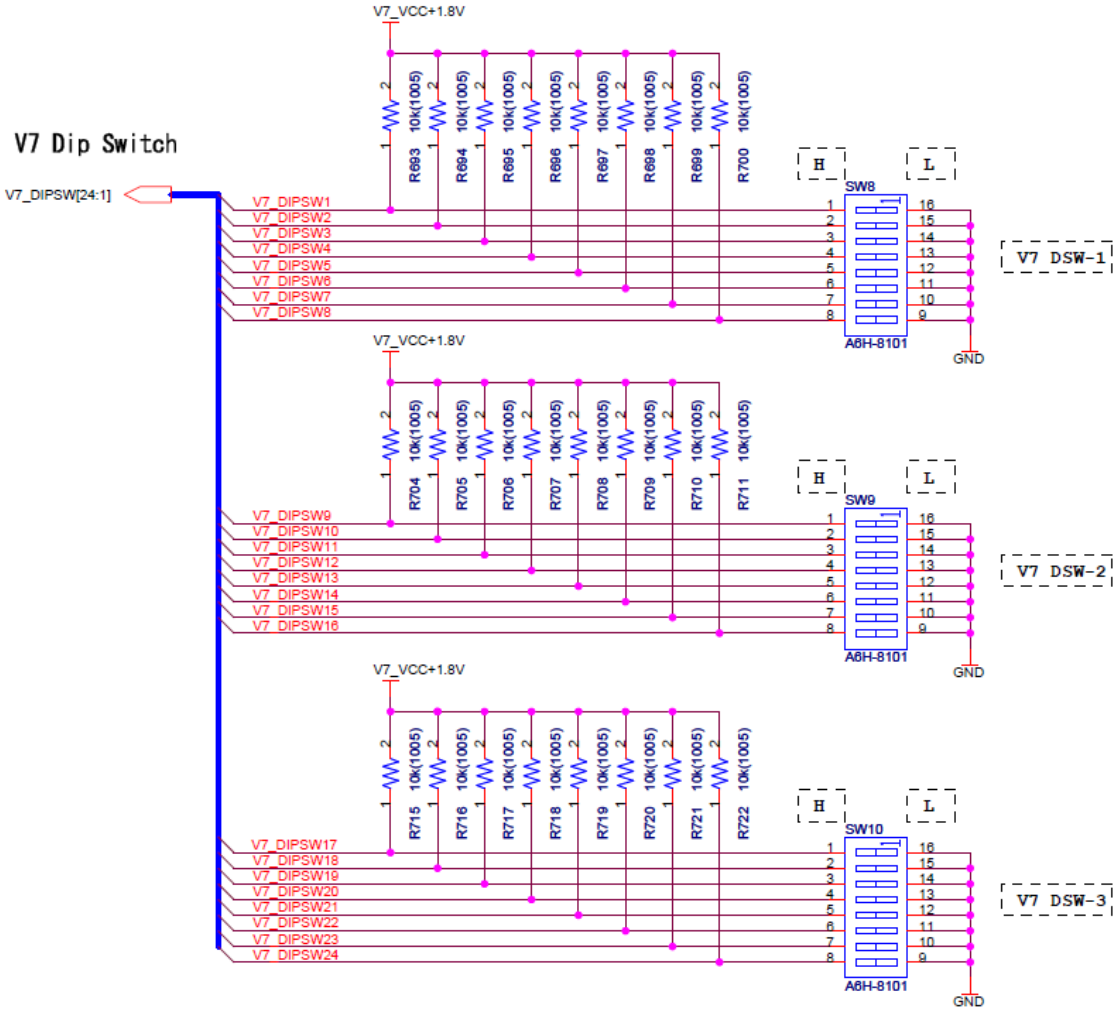


Figure 8-31 Virtex-7 DIPSW Structure

Figure 8-32 Onboard DIPSWs

Table 8-50 Virtex-7 DIPSW Pin Assignments

Device			FPGA(Virtex-7)		
Name	Pin No.	Signal Name	Pin No.	Bank	Level
SW8	1	V7_DIPSW1	AH32	13	1.8V
	2	V7_DIPSW2	AH33		
	3	V7_DIPSW3	AJ33		
	4	V7_DIPSW4	AL33		
	5	V7_DIPSW5	AM34		
	6	V7_DIPSW6	AL34		
	7	V7_DIPSW7	AM35		
	8	V7_DIPSW8	AL35		
	9-16	GND	-	-	-
SW9	1	V7_DIPSW9	AM39	13	1.8V
	2	V7_DIPSW10	AL39		
	3	V7_DIPSW11	AM40		
	4	V7_DIPSW12	AN42		
	5	V7_DIPSW13	AN43		
	6	V7_DIPSW14	AN44		
	7	V7_DIPSW15	AM41		
	8	V7_DIPSW16	AM42		
	9-16	GND	-	-	-
SW10	1	V7_DIPSW17	AM44	13	1.8V
	2	V7_DIPSW18	AL42		
	3	V7_DIPSW19	AL43		
	4	V7_DIPSW20	AL44		
	5	V7_DIPSW21	AK33		
	6	V7_DIPSW22	AK35		
	7	V7_DIPSW23	AJ34		
	8	V7_DIPSW24	AJ35		
	9-16	GND	-		

8.9. PushSW

The TB-7V-2000T-LSI board is equipped with four PushSws for Virtex-7.
When the PushSW is pressed down, then there is “low” level on FPGA input.

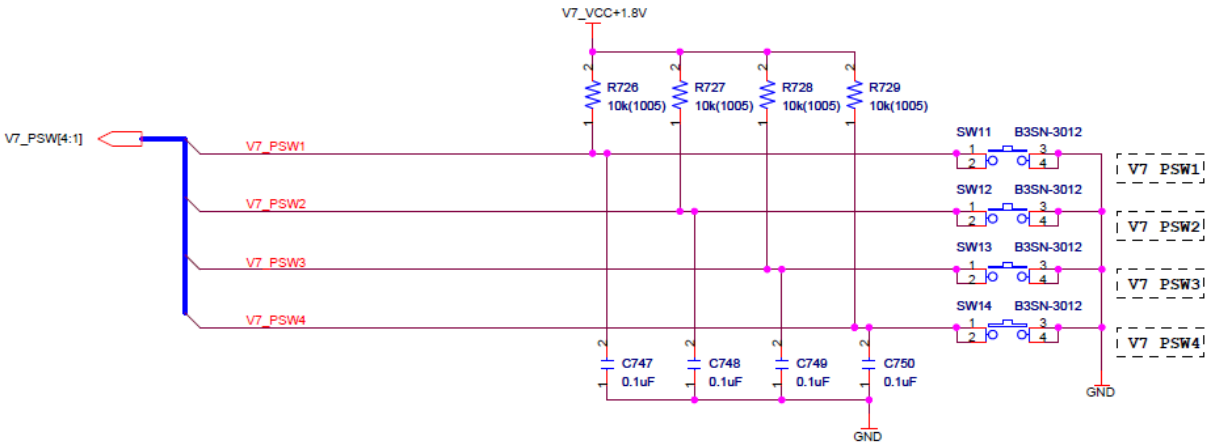


Figure 8-33 Virtex-7 PushSW Sructure

Figure 8-34 Onboard PushSWs

Table 8-51 Virtex-7 PushSW Pin Assignments

Device		FPGA(Virtex-7)		
Name	Signal Name	Pin No.	Bank	Level
SW11	V7_PSW1	AD31	15	1.8V
SW12	V7_PSW2	AE36	14	
SW13	V7_PSW3	AE35		
SW14	V7_PSW4	AG39		

8.10. Rotary SW

The TB-7V-2000T-LSI board is equipped with one Rotary SW.

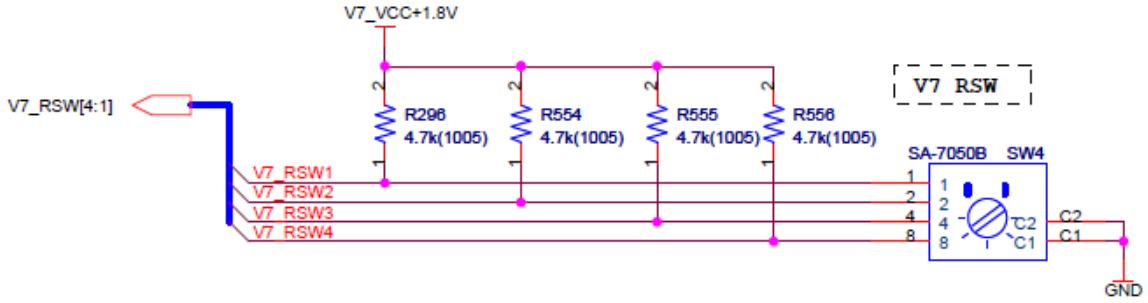


Figure 8-35 Rotary SW Structure

Figure 8-36 Onboard Rotary SW

Table 8-52 Rotary SW Pin Assignments

Device (SW4)		FPGA (Virtex-7)		
Pin No.	Signal Name	Pin No.	Bank	Level
1	V7_RSW1	AF39	14	1.8V
2	V7_RSW2	AG40		
4	V7_RSW3	AE42		
8	V7_RSW4	AF42		

Table 8-53 Rotary SW Output Signal Values

Device (SW4)		Device (SW4)	
SW Value	Signal Value	SW Value	Signal Value
0	V7_RSW[4:1] = 4'b1111	8	V7_RSW[4:1] = 4'b0111
1	V7_RSW[4:1] = 4'b1110	9	V7_RSW[4:1] = 4'b0110
2	V7_RSW[4:1] = 4'b1101	A	V7_RSW[4:1] = 4'b0101
3	V7_RSW[4:1] = 4'b1100	B	V7_RSW[4:1] = 4'b0100
4	V7_RSW[4:1] = 4'b1011	C	V7_RSW[4:1] = 4'b0011
5	V7_RSW[4:1] = 4'b1010	D	V7_RSW[4:1] = 4'b0010
6	V7_RSW[4:1] = 4'b1001	E	V7_RSW[4:1] = 4'b0001
7	V7_RSW[4:1] = 4'b1000	F	V7_RSW[4:1] = 4'b0000

8.11. LED

The TB-7V-2000T-LSI board is equipped with ten LEDs for Virtex-7.
Each LED will light up when the corresponding FPGA output pin is driven “High”.

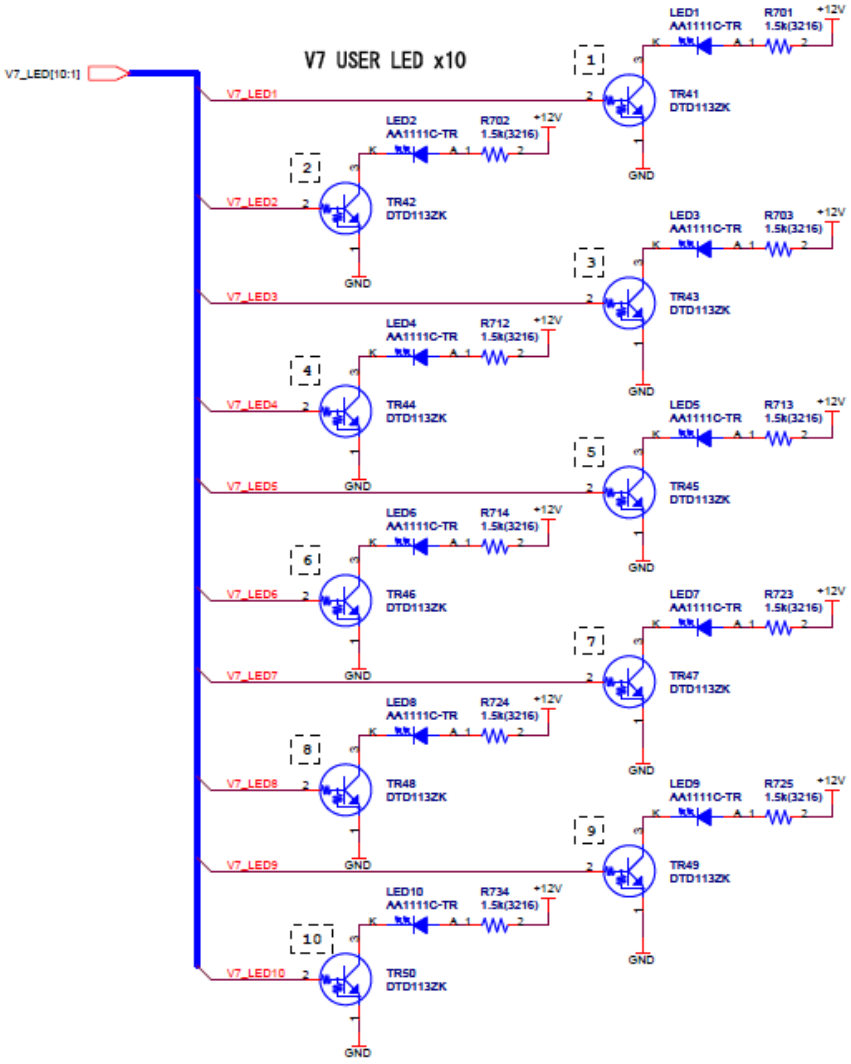


Figure 8-37 Virtex-7 LED Structure

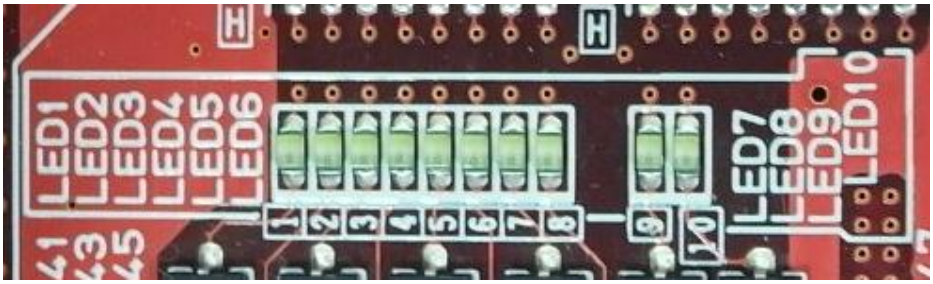


Figure 8-38 Onboard LEDs

Table 8-54 Virtex-7 LED Pin Assignments

Device		FPGA (Virtex-7)		
Name	Signal Name	Pin No.	Bank	Level
LED1	V7_LED1	AH42	14	1.8V
LED2	V7_LED2	AH28		
LED3	V7_LED3	AG29		
LED4	V7_LED4	AG30		
LED5	V7_LED5	AG44		
LED6	V7_LED6	AE30		
LED7	V7_LED7	AF43		
LED8	V7_LED8	AF44		
LED9	V7_LED9	AE31		
LED10	V7_LED10	AE43		

8.12. Single Digit LED

The TB-7V-2000T-LSI board is equipped with two Single digit LEDs.
Each Single digit LED will light up when the corresponding FPGA output pin is driven “High”.
Figure 8-39 shows the LED64 structure. Similar figure applies to the LED65 structure.

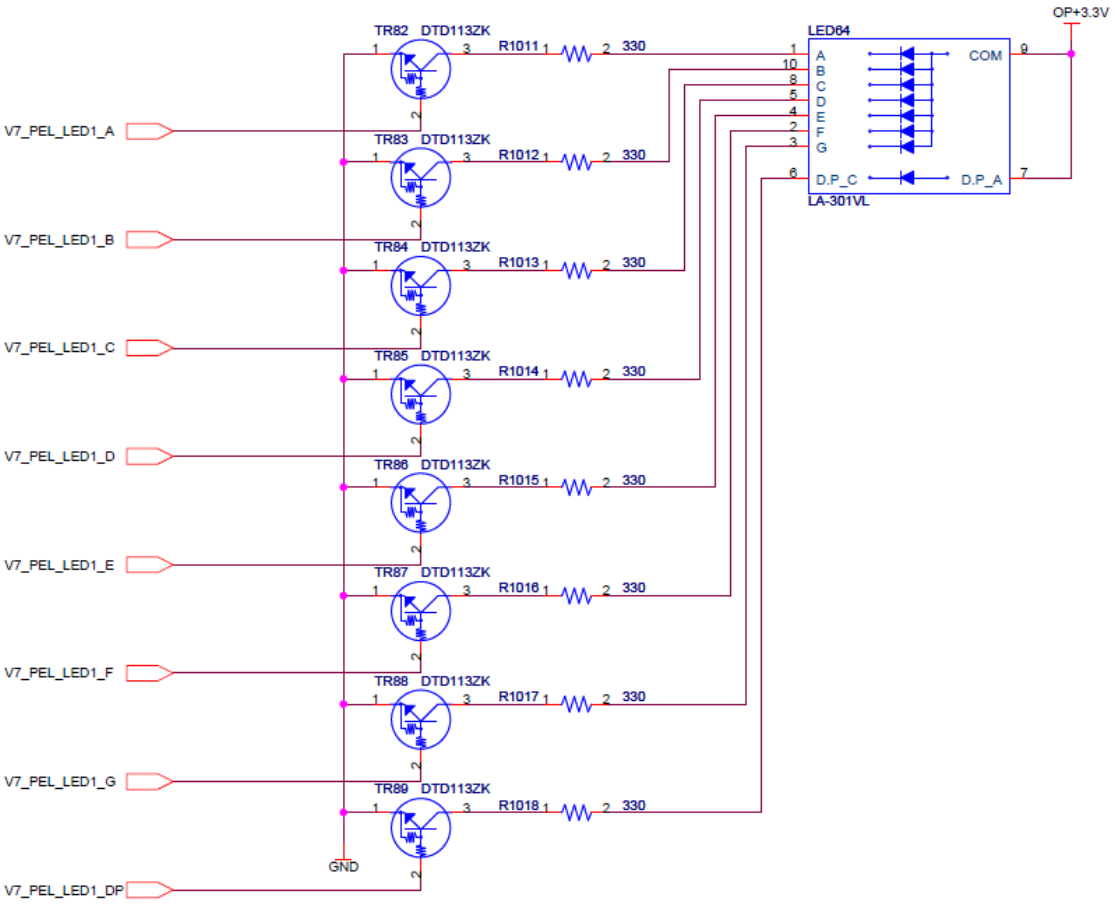


Figure 8-39 Single Digit LED(LED64) Structure

Figure 8-40 Onboard Single Digit LEDs

Table 8-55 Single Digit LED(LED64) Pin Assignments

Device			FPGA(Virtex-7)		
Name	Pin No.	Signal Name	Pin No.	Bank	Level
LED64	1	V7_PEL_LED1_A	T25	18	1.5V
	2	V7_PEL_LED1_F	T27		
	3	V7_PEL_LED1_G	R27		
	4	V7_PEL_LED1_E	P26		
	5	V7_PEL_LED1_D	R26		
	6	V7_PEL_LED1_DP	N26		
	7	OP+3.3V	-		
	8	V7_PEL_LED1_C	R28		
	9	OP+3.3V	-		
	10	V7_PEL_LED1_B	T28		

Table 8-56 Single Digit LED(LED65) Pin Assignments

Device			FPGA(Virtex-7)		
Name	Pin No.	Signal Name	Pin No.	Bank	Level
LED65	1	V7_PEL_LED2_A	N27	18	1.5V
	2	V7_PEL_LED2_F	H27		
	3	V7_PEL_LED2_G	H28		
	4	V7_PEL_LED2_E	P25		
	5	V7_PEL_LED2_D	R25		
	6	V7_PEL_LED2_DP	G27		
	7	OP+3.3V	-		
	8	V7_PEL_LED2_C	N28		
	9	OP+3.3V	-		
	10	V7_PEL_LED2_B	P28		

8.13. XADC Pin Header

The TB-7V-2000T-LSI board is equipped with a 14-pin PinHeader for Virtex7 XADC.
If a dedicated differential analog input (VP_0,VN_0) is used, do not implement R283 and R284.
If a thermal diode (DXP_0, DXN_0) is used, do not implement R286 and R287.

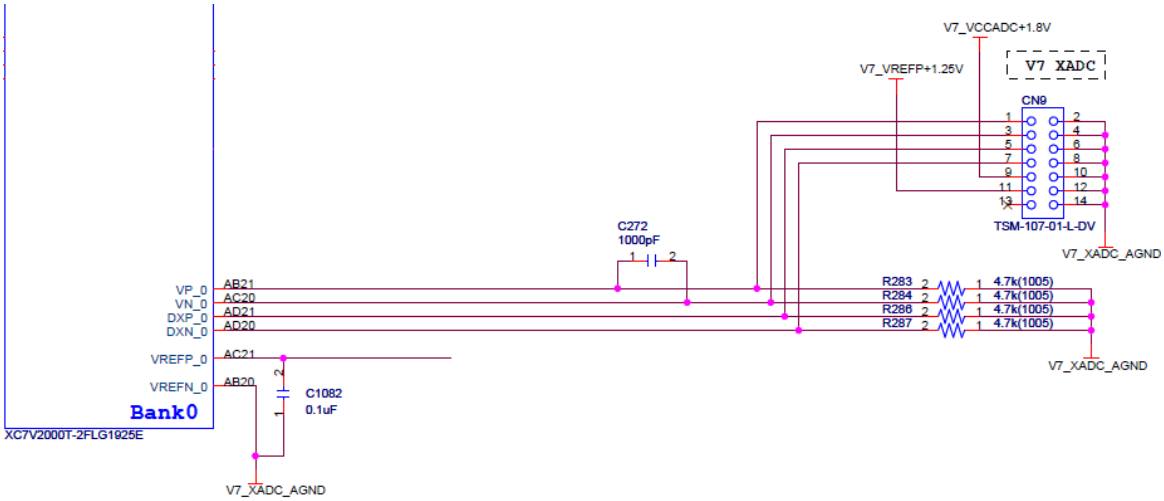


Figure 8-41 Virtex-7 XADC PinHeader Structure

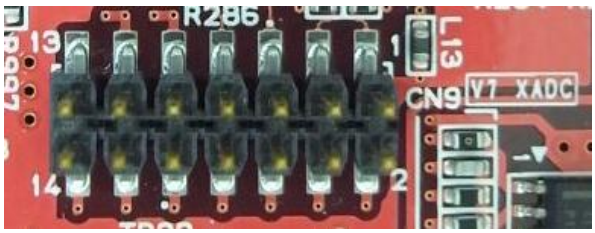


Figure 8-42 Onboard XADC PinHeader

Table 8-57 Virtex-7 XADC PinHeader Pin Assignments

FPGA		PinHeader(CN9)			
Bank No.	Pin No.	Signal Name	Pin No.		Signal Name
0	AB21	VP	1	2	V7_XADC_AGND
0	AC20	VN	3	4	V7_XADC_AGND
0	AD21	DXP	5	6	V7_XADC_AGND
0	AD20	DXN	7	8	V7_XADC_AGND
-	-	V7_VCCADC+1.8V	9	10	V7_XADC_AGND
-	-	V7_VREFP+1.25V	11	12	V7_XADC_AGND
-	-	-	13	14	V7_XADC_AGND

8.14. Battery Control

The TB-7V-2000T-LSI board is equipped with a battery control circuit on the solder side. By default, the battery socket is not implemented.

The battery is connected to the Virtex-7 VCCVBATT(AB1) pin.

Use a “CR1220” size of button battery.

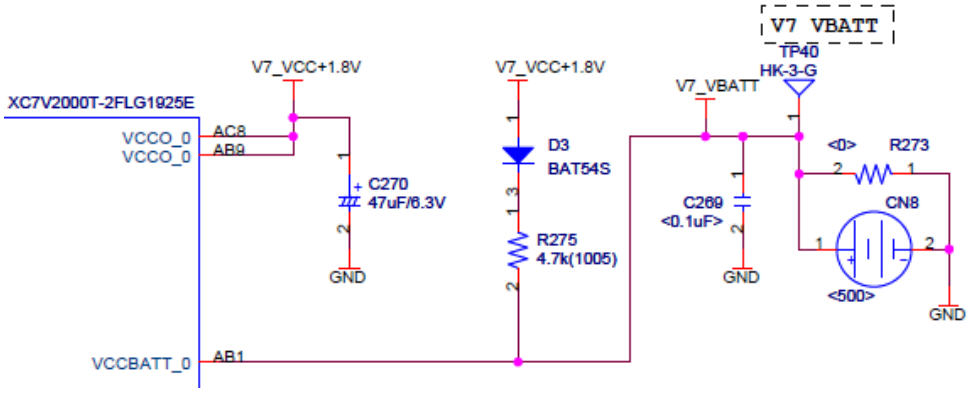


Figure 8-43 Virtex-7 Battery Structure

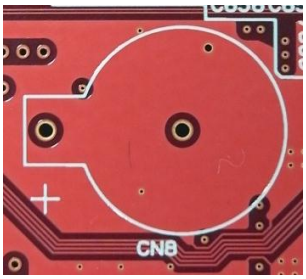


Figure 8-44 Onboard Battery

8.15. Virtex-7 Config Micro SD/NAND Flash

The TB-7V-2000T-LSI board is equipped with one NAND Flash for Virtex-7 configuration file storage and one Micro SD socket that allow configuration from Micro SD Card and NAND Flash.
It is also equipped with Spartan-3AN for configuration control.
For information about configuration method, refer to the relevant “TB-7V-200T-LSI_uSD_CONF_ UserManual***.pdf”.

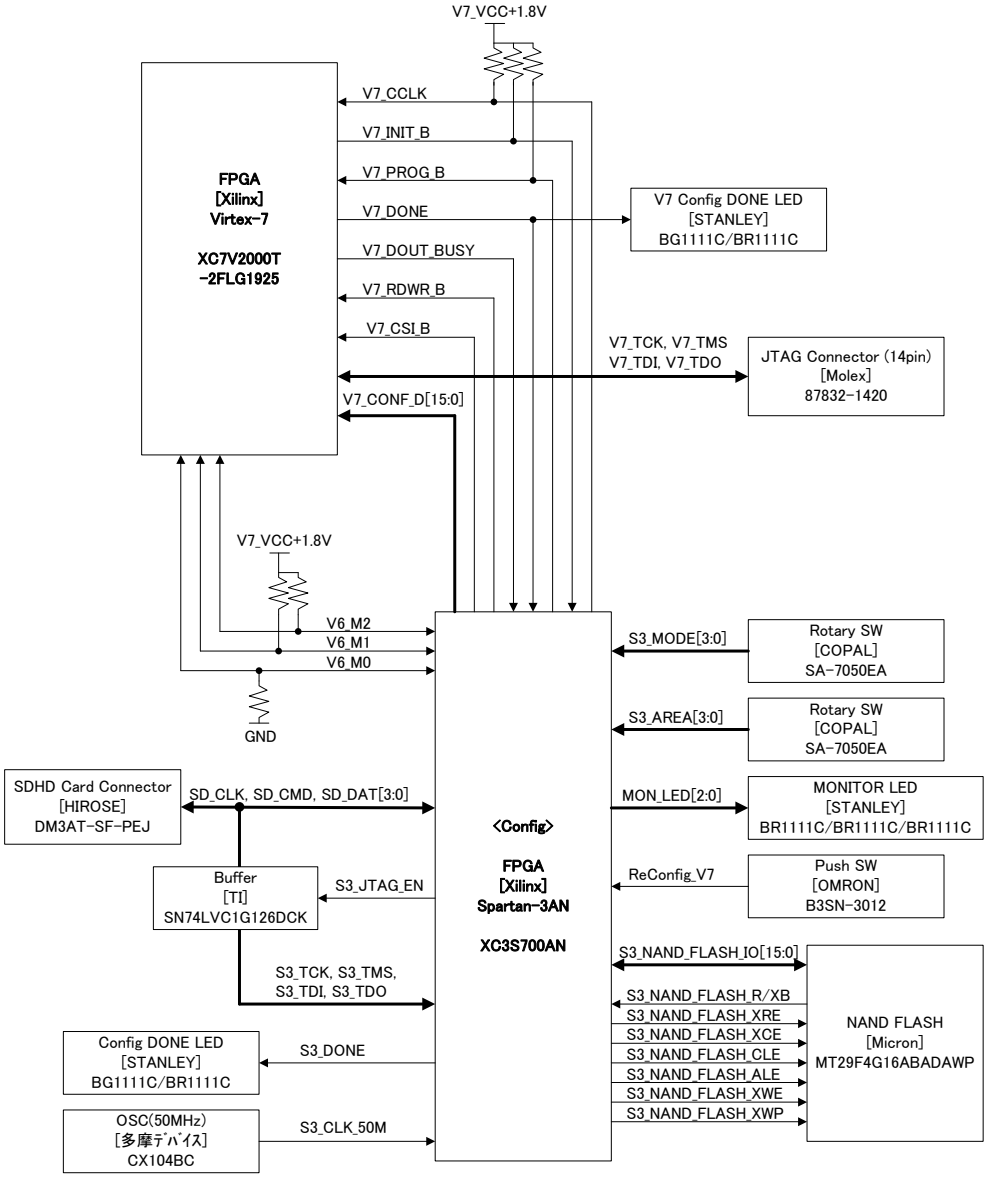


Figure 8-45 Virtex-7 Configuration Circuit Structure

*Spartan-3AN has a dedicated design that has been written prior to shipment. Thus, the user does not need to change it.

*Before attempting MicroSD Card insertion and removal, be sure to power off the board.

9. Kintex-7 Interfae

9.1. QTH Connector

The TB-7V-2000T-LSI board is equipped with five SAMTEC 120-pin QTH connectors that allow high speed data connection to external devices. Each connector provides up to 56 pairs of LVDS signal connections, including 8 pairs of clock signals (or 119 single-pin connections).

As shown in Figure 9-1, Virtex-7 provides two connectors CN31 and CN32. These connectors allow for the selection of 1.8V, 2.5V or 3.3V signal voltage level.

In addition, CN31 and CN32 allow switchover to IIC.

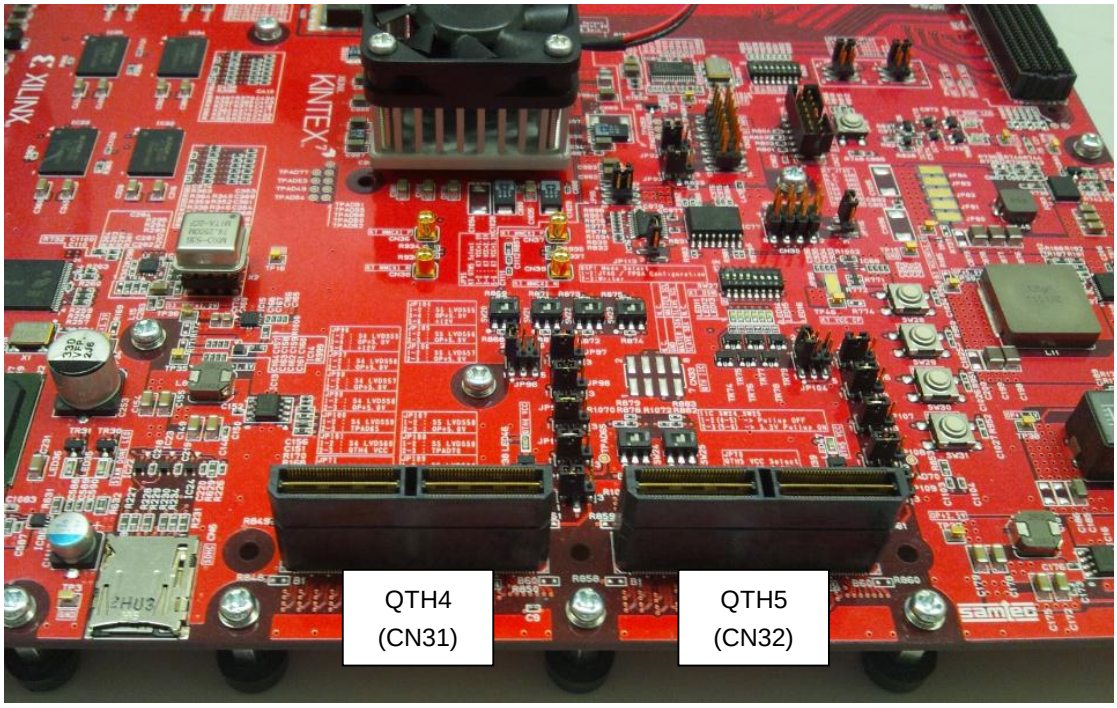


Figure 9-1 Kintex-7 QTH Connector

Table 9-1 Voltage Selection for Kintex-7 Banks and Peripheral Devices

Bank	Connected Device	Voltage	Voltage Selection			
			JP No.	1.8V	2.5V	3.3V
HR13/14/15	FMC_HPC(CN34) QTH4(CN31) QSPI,DSW, UART	Variable (1.8V/2.5V/3.3V)	JP94	1-2	3-4	5-6
			JP102	1-2	3-4	5-6
HR16/17/18	FMC_HPC(CN34) QTH5(CN32) LED,PSW	Variable (1.8V/2.5V/3.3V)	JP95	1-2	2-3	5-6

Be sure to set JP94 and JP102 to the same pin settings.

By default, all the above voltage setting is fixed at 1.8V.

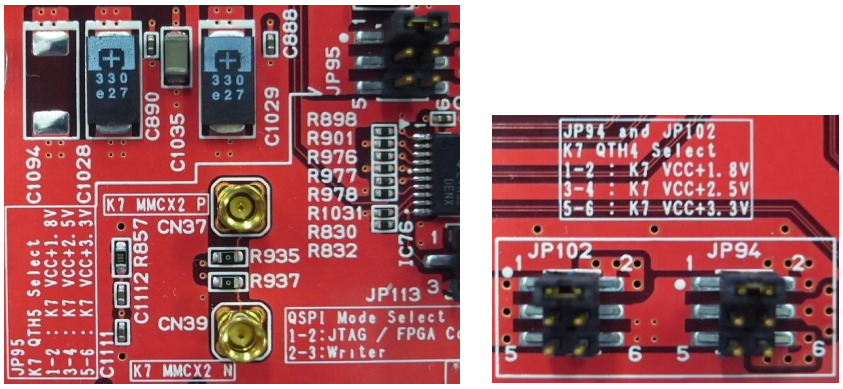


Figure 9-2 Bank Voltage Setting Location on FPGA (Kintex-7)

9.1.1. QTH4 Power Supply Pins

H1 Pin

OP+3.3V power supply (currently not available due to non-implementation of R848).

H2 Pin

OP+3.3V power supply (currently not available due to non-implementation of R849).

B54 Pin

Any 5V, 12V or FPGA (Kintex-7) is selectable by setting the jumper as shown in Table 9-2.
Currently the FPGA (Kintex-7) connection is not available due to non-implementation of R1059).

Table 9-2 QTH4 B54 Pin Assignments

Supply Voltage	JP96
+12V	5-6
OP+5V	3-4
FPGA(Kintex -7)	1-2

B55 Pin

Either 5V or FPGA (Kintex-7) is selectable by setting the jumper as shown in Table 9-3.
Currently the FPGA (Kintex-7) connection is not available due to non-implementation of R1060).

Table 9-3 QTH4 B55 Pin Assignments

Supply Voltage	JP97
OP+5V	2-3
FPGA(Kintex -7)	1-2

B56 Pin

Either 5V or FPGA (Kintex-7) is selectable by setting the jumper as shown in Table 9-4.
Currently the FPGA (Kintex-7) connection is not available due to non-implementation of R1055).

Table 9-4 QTH4 B56 Pin Assignments

Supply Voltage	JP98
OP+5V	2-3
FPGA(Kintex -7)	1-2

B57 Pin

Either 5V or FPGA (Kintex-7) is selectable by setting the jumper as shown in Table 9-5.
Currently the FPGA (Kintex-7) connection is not available due to non-implementation of R1056).

Table 9-5 QTH4 B57 Pin Assignments

Supply Voltage	JP99
OP+5V	2-3
FPGA(Kintex-7)	1-2

B58 Pin

Either TRAD or FPGA (Kintex-7) is selectable by setting the jumper as shown in Table 9-6.
Currently the FPGA (Kintex-7) connection is not available due to non-implementation of R1057).

Table 9-6 QTH4 B58 Pin Assignments

Supply Voltage	JP100
TPAD38	2-3
FPGA(Kintex-7)	1-2

B59 Pin

Either QTH4_VCC or FPGA (Kintex-7) is selectable by setting the jumper as shown in Table 9-7.
QTH4_VCC is selectable by the jumper JP71.
Currently the FPGA (Kintex-7) connection is not available due to non-implementation of R1058).

Table 9-7 QTH4 B59 Pin Assignments

Supply Voltage	JP61	JP71
QTH4_VCC(OP+2.5V)	2-3	1-2
QTH4_VCC(OP+3.3V)	2-3	2-3
FPGA(Kintex-7)	1-2	-

B60 Pin

Either 2.5V or 3.3V is selectable by setting the jumper as shown in Table 9-8.

Table 9-8 QTH4 B60 Pin Assignments

Supply Voltage	JP71
OP+2.5V	1-2
OP+3.3V	2-3

H7 Pin

The same voltage selection as B60 Pin is applicable. Currenty this pin is not used due to non-implementation of R850.

H8 Pin

The same voltage selection as B60 Pin is applicable. Currenty this pin is not used due to non-implementation of R851.

Table 9-9 QTH4 Connector (CN31) Pin Assignments

FPGA (Kintex-7)			Signal Name	QTH4 (CN31)				Signal Name	FPGA (Kintex-7)		
Bank	Pin#	Pin Name		Pair	Pin#	Pin#	Pair		Pin Name	Pin#	Bank
	-	-	-	-	H1	H2	-	-	-	-	
	AC27	IO_L12N_T1_MRCC_13	S4_LVDS_CLK0_N	N	B1	A1	N	S4_LVDS0_N	IO_L1N_T0_13	AA26	
	AB27	IO_L12P_T1_MRCC_13	S4_LVDS_CLK0_P	P	B2	A2	P	S4_LVDS0_P	IO_L1P_T0_13	Y26	
	W28	IO_L2N_T0_13	S4_LVDS1_N	N	B3	A3	N	S4_LVDS2_N	IO_L3N_T0_DQS_13	AA28	
	W27	IO_L2P_T0_13	S4_LVDS1_P	P	B4	A4	P	S4_LVDS2_P	IO_L3P_T0_DQS_13	Y28	
	Y29	IO_L4N_T0_13	S4_LVDS3_N	N	B5	A5	N	S4_LVDS4_N	IO_L5N_T0_13	AB28	
	W29	IO_L4P_T0_13	S4_LVDS3_P	P	B6	A6	P	S4_LVDS4_P	IO_L5P_T0_13	AA27	
	AC30	IO_L7N_T1_13	S4_LVDS5_N	N	B7	A7	N	S4_LVDS6_N/VREF	IO_L6N_T0_VREF_13	AB25	
	AC29	IO_L7P_T1_13	S4_LVDS5_P	P	B8	A8	P	S4_LVDS6_P	IO_L6P_T0_13	AA25	
	AF28	IO_L14N_T2_SRCC_13	S4_LVDS7_N/VREF	N	B9	A9	N	S4_LVDS8_N	IO_L8N_T1_13	AA30	
	AE28	IO_L14P_T2_SRCC_13	S4_LVDS7_P	P	B10	A10	P	S4_LVDS8_P	IO_L8P_T1_13	Y30	
	AE29	IO_L9N_T1_DQS_13	S4_LVDS9_N	N	B11	A11	N	S4_LVDS10_N	IO_L10N_T1_13	AB30	
13	AD29	IO_L9P_T1_DQS_13	S4_LVDS9_P	P	B12	A12	P	S4_LVDS10_P	IO_L10P_T1_13	AB29	13
	AK30	IO_L15N_T2_DQS_13	S4_LVDS11_N	N	B13	A13	N	S4_LVDS12_N	IO_L16N_T2_13	AF30	
	AK29	IO_L15P_T2_DQS_13	S4_LVDS11_P	P	B14	A14	P	S4_LVDS12_P	IO_L16P_T2_13	AE30	
	AJ29	IO_L17N_T2_13	S4_LVDS13_N	N	B15	A15	N	S4_LVDS14_N/CLK_N	IO_L11N_T1_SRCC_13	AD28	
	AJ28	IO_L17P_T2_13	S4_LVDS13_P	P	B16	A16	P	S4_LVDS14_P/CLK_P	IO_L11P_T1_SRCC_13	AD27	
	AH29	IO_L13N_T2_MRCC_13	S4_LVDS15_N/CLK_N	N	B17	A17	N	S4_LVDS16_N	IO_L18N_T2_13	AH30	
	AG29	IO_L13P_T2_MRCC_13	S4_LVDS15_P/CLK_P	P	B18	A18	P	S4_LVDS16_P	IO_L18P_T2_13	AG30	
	AK28	IO_L20N_T3_13	S4_LVDS17_N	N	B19	A19	N	S4_LVDS18_N	IO_L21N_T3_DQS_13	AG28	
	AJ27	IO_L20P_T3_13	S4_LVDS17_P	P	B20	A20	P	S4_LVDS18_P	IO_L21P_T3_DQS_13	AG27	
	AH27	IO_L22N_T3_13	S4_LVDS19_N	N	B21	A21	N	S4_LVDS20_N	IO_L23N_T3_13	AF27	
	AH26	IO_L22P_T3_13	S4_LVDS19_P	P	B22	A22	P	S4_LVDS20_P	IO_L23P_T3_13	AF26	
	AD26	IO_L19N_T3_VREF_13	S4_LVDS21_N/VREF	N	B23	A23	N	S4_LVDS22_N	IO_L24N_T3_13	AK26	
	AC26	IO_L19P_T3_13	S4_LVDS21_P	P	B24	A24	P	S4_LVDS22_P	IO_L24P_T3_13	AJ26	

FPGA (Kintex-7)			Signal Name	QTH4 (CN31)				Signal Name	FPGA (Kintex-7)		
Bank	Pin#	Pin Name		Pair	Pin#	Pin#	Pair		Pin Name	Pin#	Bank
15	J24	IO_L1N_T0_AD0N_15	S4_LVDS23_N	N	B25	A25	N	S4_LVDS24_N/VREF	IO_L6N_T0_VREF_15	L20	15
	J23	IO_L1P_T0_AD0P_15	S4_LVDS23_P	P	B26	A26	P	S4_LVDS24_P	IO_L6P_T0_15	M20	
	L23	IO_L2N_T0_AD8N_15	S4_LVDS25_N	N	B27	A27	N	S4_LVDS26_N/C_M_SDA	IO_L3N_T0_DQS_AD1N_15	K24	
	L22	IO_L2P_T0_AD8P_15	S4_LVDS25_P	P	B28	A28	P	S4_LVDS26_P	IO_L3P_T0_DQS_AD1P_15	K23	
	K21	IO_L4N_T0_AD9N_15	S4_LVDS27_N	N	B29	A29	N	S4_LVDS28_N/C_M_SCL	IO_L5N_T0_AD2N_15	J22	
	L21	IO_L4P_T0_AD9P_15	S4_LVDS27_P	P	B30	A30	P	S4_LVDS28_P	IO_L5P_T0_AD2P_15	J21	
	-	-	TPAD61	-	H3	H4	-	TPAD62	-	-	
	-	-	TPAD63	-	H5	H6	-	TPAD64	-	-	
	H29	IO_L7N_T1_AD10N_15	S4_LVDS29_N	N	B31	A31	N	S4_LVDS30_N/CLK_N/F_S_SDA	IO_L11N_T1_SRCC_AD12N_15	L27	
	J29	IO_L7P_T1_AD10P_15	S4_LVDS29_P	P	B32	A32	P	S4_LVDS30_P/CLK_P	IO_L11P_T1_SRCC_AD12P_15	L26	
	K25	IO_L12N_T1_MRCC_AD5N_15	S4_LVDS31_N/CLK_N	N	B33	A33	N	S4_LVDS32_N/C_S_SCL	IO_L8N_T1_AD3N_15	J28	
	L25	IO_L12P_T1_MRCC_AD5P_15	S4_LVDS31_P/CLK_P	P	B34	A34	P	S4_LVDS32_P	IO_L8P_T1_AD3P_15	J27	
	K30	IO_L9N_T1_DQS_AD11N_15	S4_LVDS33_N	N	B35	A35	N	S4_LVDS34_N	IO_L10N_T1_AD4N_15	J26	
	L30	IO_L9P_T1_DQS_AD11P_15	S4_LVDS33_P	P	B36	A36	P	S4_LVDS34_P	IO_L10P_T1_AD4P_15	K26	
	L28	IO_L14N_T2_SRCC_15	S4_LVDS35_N	N	B37	A37	N	S4_LVDS36_N	IO_L15N_T2_DQS_ADV_B_15	M30	
	M28	IO_L14P_T2_SRCC_15	S4_LVDS35_P	P	B38	A38	P	S4_LVDS36_P	IO_L15P_T2_DQS_15	M29	
	N20	IO_L19N_T3_A21_VREF_15	S4_LVDS37_N/VREF	N	B39	A39	N	S4_LVDS38_N	IO_L16N_T2_A27_15	M27	
	N19	IO_L19P_T3_A22_15	S4_LVDS37_P	P	B40	A40	P	S4_LVDS38_P	IO_L16P_T2_A28_15	N27	
	N30	IO_L17N_T2_A25_15	S4_LVDS39_N	N	B41	A41	N	S4_LVDS40_N/VREF	IO_L18N_T2_A23_15	N26	
	N29	IO_L17P_T2_A26_15	S4_LVDS39_P	P	B42	A42	P	S4_LVDS40_P	IO_L18P_T2_A24_15	N25	
	N22	IO_L20N_T3_A19_15	S4_LVDS41_N	N	B43	A43	N	S4_LVDS42_N	IO_L21N_T3_DQS_A18_15	N24	
	N21	IO_L20P_T3_A20_15	S4_LVDS41_P	P	B44	A44	P	S4_LVDS42_P	IO_L21P_T3_DQS_15	P23	

FPGA (Kintex-7)			Signal Name	QTH4 (CN31)				Signal Name	FPGA (Kintex-7)		
Bank	Pin#	Pin Name		Pair	Pin#	Pin#	Pair		Pin Name	Pin#	Bank
	P22	IO_L22N_T3_A16_15	S4_LVDS43_N	N	B45	A45	N	S4_LVDS44_N	IO_L23N_T3_FWE_B_15	M25	
	P21	IO_L22P_T3_A17_15	S4_LVDS43_P	P	B46	A46	P	S4_LVDS44_P	IO_L23P_T3_FOE_B_15	M24	
	M23	IO_L24N_T3_RS0_15	S4_LVDS45_N	N	B47	A47	N	S4_LVDS46_N/CLK_N	IO_L13N_T2_MRCC_15	K29	
	M22	IO_L24P_T3_RS1_15	S4_LVDS45_P	P	B48	A48	P	S4_LVDS46_P/CLK_P	IO_L13P_T2_MRCC_15	K28	
14	U25	IO_L14N_T2_SRCC_14	S4_LVDS47_N/CLK_N	N	B49	A49	N	S4_LVDS48_N	IO_L15N_T2_DQS_DOUT_CSO_B_14	U30	14
	T25	IO_L14P_T2_SRCC_14	S4_LVDS47_P/CLK_P	P	B50	A50	P	S4_LVDS48_P	IO_L15P_T2_DQS_RDWR_B_14	U29	
	V27	IO_L16N_T2_A15_D31_14	S4_LVDS49_N	N	B51	A51	N	S4_LVDS50_N	IO_L17N_T2_A13_D29_14	V30	
	V26	IO_L16P_T2_CSI_B_14	S4_LVDS49_P	P	B52	A52	P	S4_LVDS50_P	IO_L17P_T2_A14_D30_14	V29	
	U22	IO_L21P_T3_DQS_14	S4_LVDS53	-	B53	A53	N	S4_LVDS51_N/VREF	IO_L19N_T3_A09_D25_VREF_14	V20	
	V21	IO_L22P_T3_A05_D21_14	S4_LVDS55/5V/12V	-	B54	A54	P	S4_LVDS51_P	IO_L19P_T3_A10_D26_14	V19	
	V22	IO_L22N_T3_A04_D20_14	S4_LVDS56/5V	-	B55	A55	N	S4_LVDS52_N	IO_L18N_T2_A11_D27_14	W26	
	U24	IO_L23P_T3_A03_D19_14	S4_LVDS57/5V	-	B56	A56	P	S4_LVDS52_P	IO_L18P_T2_A12_D28_14	V25	
	V24	IO_L23N_T3_A02_D18_14	S4_LVDS58/5V	-	B57	A57	N	S4_LVDS54_N	IO_L20N_T3_A07_D23_14	W24	
	W21	IO_L24P_T3_A01_D17_14	S4_LVDS59/TP	-	B58	A58	P	S4_LVDS54_P	IO_L20P_T3_A08_D24_14	W23	
	W22	IO_L24N_T3_A00_D16_14	S4_LVDS60/2.5V/3.3V	-	B59	A59	N	S4_LVDS_CLK1_N	IO_L13N_T2_MRCC_14	U28	
			QTH4_VCC	-	B60	A60	P	S4_LVDS_CLK1_P	IO_L13P_T2_MRCC_14	U27	
	-	-	(QTH4_VCC) *JP resistor not implemented	-	H7	H8	-	(TH4_VCC) *JP resistor not implemented	-	-	

9.1.2. Switchover of desctination (Kintex-7/CN33) to which the QTH4 connector is connected

The IIC signal destination of the QTH connector can be switched using SW20 and SW21.

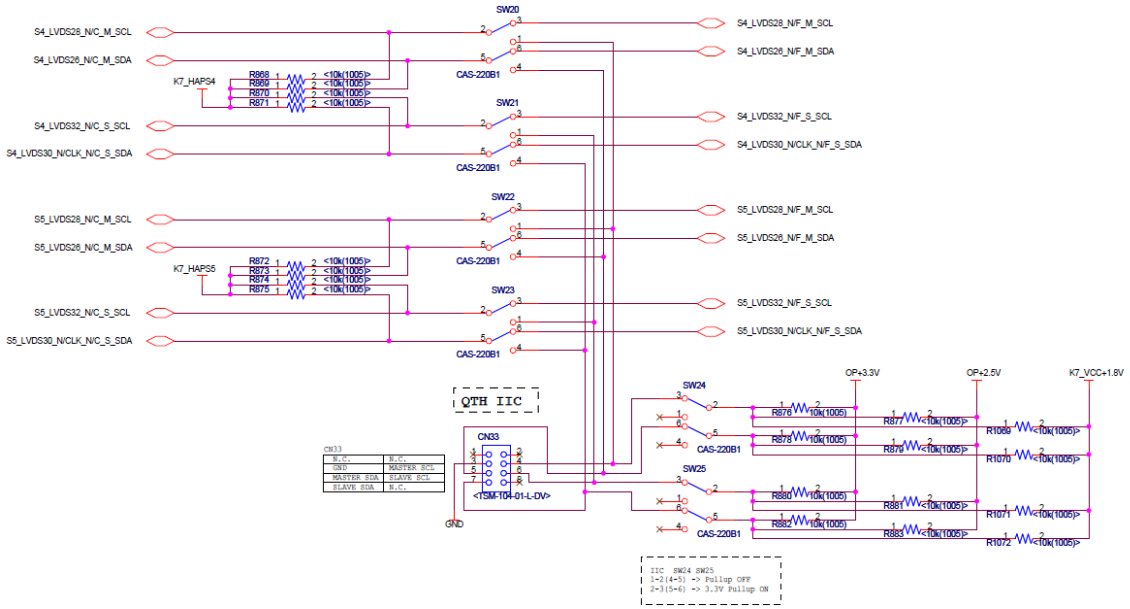


Figure 9-3 Structure of switchover of destination (Kintex-7/IIC) to which the QTH4 connector is connected

Table 9-10 Switchover of desctination (Kintex-7/CN33) to which the QTH4 connector is connected

QTH4 CN Pin No.	Device Name		Connect Destination
A29	SW20	2-3	FPGA(Kintex-7): J22
		2-1	CN33: 4pin
A27		5-6	FPGA(Kintex-7): K24
		5-4	CN33: 5pin
A33	SW21	2-3	FPGA(Kintex-7): J28
		2-1	CN33: 6pin
A31		5-6	FPGA(Kintex-7): L27
		5-4	CN33: 7pin

*CN33 is not implemented.

The IIC Pullup ON/OFF switchover can be controlled using SW24 and SW25.
The 1.8V/2.5V/3.3V Pullup selection is also allowed.

Table 9-11 IIC Pullup On/OFF Switchover

Connecter Name	Device Name		Action
CN33	SW24 SW25	1-2 4-5	Pullup OFF
		2-3 5-6	3.3V Pullup ON

In addition, the above 3.3V Pullup mode can be switched to 1.8V or 2.5V Pullup mode.
In order to do that, remove a currently implemented 3.3V Pullup resistor and then implement a 1.8V or 2.5V Pullup resistor. (By default, the 1.8V/2.5V Pullup resistor is not implemented).

9.1.3. QTH5 Power Supply Pinout

H1 Pin

OP+3.3V power supply (currently not available due to non-implementation of R858).

H2 Pin

OP+3.3V power supply (currently not available due to non-implementation of R859).

B54 Pin

Any 5V, 12V or FPGA (Kintex-7) is selectable by setting the jumper as shown in Table 9-12.
Currently the FPGA (Kintex-7) connection is not available due to non-implementation of R1065).

Table 9-12 QTH5 B54 Pin Assignments

Supply Voltage	JP104
+12V	5-6
OP+5V	3-4
FPGA(Kintex -7)	1-2

B55 Pin

Either 5V or FPGA (Kintex-7) is selectable by setting the jumper as shown in Table 9-13.
Currently the FPGA (Kintex-7) connection is not available due to non-implementation of R1066).

Table 9-13 QTH5 B5 Pin Assignments

Supply Voltage	JP105
OP+5V	2-3
FPGA(Kintex -7)	1-2

B56 Pin

Either 5V or FPGA (Kintex-7) is selectable by setting the jumper as shown in Table 9-14.
Currently the FPGA (Kintex-7) connection is not available due to non-implementation of R1062).

Table 9-14 QTH5 B5 Pin Assignments

Supply Voltage	JP106
OP+5V	2-3
FPGA(Kintex -7)	1-2

B57 Pin

Either 5V or FPGA (Kintex-7) is selectable by setting the jumper as shown in Table 9-15.
Currently the FPGA (Kintex-7) connection is not available due to non-implementation of R1061).

Table 9-15 QTH5 B57 Pin Assignments

Supply Voltage	JP107
OP+5V	2-3
FPGA(Kintex -7)	1-2

B58 Pin

Either TRAD or FPGA (Kintex-7) is selectable by setting the jumper as shown in Table 9-16.
Currently the FPGA (Kintex-7) connection is not available due to non-implementation of R1063).

Table 9-16 QTH5 B5 Pin Assignments

Supply Voltage	JP108
TPAD38	2-3
FPGA(Kintex -7)	1-2

B59 Pin

Either QTH5_VCC or FPGA (Kintex-7) is selectable by setting the jumper as shown in Table 9-17.
QTH5_VCC is selectable by the jumper JP78.
Currently the FPGA (Kintex-7) connection is not available due to non-implementation of R1064).

Table 9-17 QTH5 B59 Pin Assignments

Supply Voltage	JP61	JP78
QTH5_VCC(OP+2.5V)	2-3	1-2
QTH5_VCC(OP+3.3V)	2-3	2-3
FPGA(Kintex-7)	1-2	-

BB60 Pin

Either 2.5V or 3.3V is selectable by setting the jumper as shown in Table 9-18.

Table 9-18 QTH5 B6 Pin Assignments

Supply Voltage	JP78
OP+2.5V	1-2
OP+3.3V	2-3

H7 Pin

The same voltage selection as B60 Pin is applicable. Currenty this pin is not used due to non-implementation of R860.

H8 Pin

The same voltage selection as B60 Pin is applicable. Currenty this pin is not used due to non-implementation of R861.

Table 9-19 QTH5 Connector (CN32) Pin Assignments

FPGA (Kintex-7)			Signal Name	QTH5 (CN32)				Signal Name	FPGA (Kintex-7)		
Bank	Pin#	Pin Name		Pair	Pin#	Pin#	Pair		Pin Name	Pin#	Bank
	-	-	-	-	H1	H2	-	-	-	-	
	E20	IO_L12N_T1_MRCC_17	S5_LVDS_CLK0_N	N	B1	A1	N	S5_LVDS0_N	IO_L1N_T0_17	J18	
	F20	IO_L12P_T1_MRCC_17	S5_LVDS_CLK0_P	P	B2	A2	P	S5_LVDS0_P	IO_L1P_T0_17	K18	
	G20	IO_L2N_T0_17	S5_LVDS1_N	N	B3	A3	N	S5_LVDS2_N	IO_L3N_T0_DQS_17	H17	
	H20	IO_L2P_T0_17	S5_LVDS1_P	P	B4	A4	P	S5_LVDS2_P	IO_L3P_T0_DQS_17	J17	
	H19	IO_L4N_T0_17	S5_LVDS3_N	N	B5	A5	N	S5_LVDS4_N	IO_L5N_T0_17	L18	
	J19	IO_L4P_T0_17	S5_LVDS3_P	P	B6	A6	P	S5_LVDS4_P	IO_L5P_T0_17	L17	
	H22	IO_L7N_T1_17	S5_LVDS5_N	N	B7	A7	N	S5_LVDS6_N/VREF	IO_L6N_T0_VREF_17	K20	
	H21	IO_L7P_T1_17	S5_LVDS5_P	P	B8	A8	P	S5_LVDS6_P	IO_L6P_T0_17	K19	
	D19	IO_L14N_T2_SRCC_17	S5_LVDS7_N/VREF	N	B9	A9	N	S5_LVDS8_N	IO_L8N_T1_17	C21	
	E19	IO_L14P_T2_SRCC_17	S5_LVDS7_P	P	B10	A10	P	S5_LVDS8_P	IO_L8P_T1_17	D21	
	F22	IO_L9N_T1_DQS_17	S5_LVDS9_N	N	B11	A11	N	S5_LVDS10_N	IO_L10N_T1_17	C22	
17	G22	IO_L9P_T1_DQS_17	S5_LVDS9_P	P	B12	A12	P	S5_LVDS10_P	IO_L10P_T1_17	D22	17
	C16	IO_L15N_T2_DQS_17	S5_LVDS11_N	N	B13	A13	N	S5_LVDS12_N	IO_L16N_T2_17	F18	
	D16	IO_L15P_T2_DQS_17	S5_LVDS11_P	P	B14	A14	P	S5_LVDS12_P	IO_L16P_T2_17	G18	
	B17	IO_L17N_T2_17	S5_LVDS13_N	N	B15	A15	N	S5_LVDS14_N/CLK_N	IO_L11N_T1_SRCC_17	E21	
	C17	IO_L17P_T2_17	S5_LVDS13_P	P	B16	A16	P	S5_LVDS14_P/CLK_P	IO_L11P_T1_SRCC_17	F21	
	D18	IO_L13N_T2_MRCC_17	S5_LVDS15_N/CLK_N	N	B17	A17	N	S5_LVDS16_N	IO_L18N_T2_17	F17	
	D17	IO_L13P_T2_MRCC_17	S5_LVDS15_P/CLK_P	P	B18	A18	P	S5_LVDS16_P	IO_L18P_T2_17	G17	
	A17	IO_L20N_T3_17	S5_LVDS17_N	N	B19	A19	N	S5_LVDS18_N	IO_L21N_T3_DQS_17	A21	
	A16	IO_L20P_T3_17	S5_LVDS17_P	P	B20	A20	P	S5_LVDS18_P	IO_L21P_T3_DQS_17	A20	
	A18	IO_L22N_T3_17	S5_LVDS19_N	N	B21	A21	N	S5_LVDS20_N	IO_L23N_T3_17	A22	
	B18	IO_L22P_T3_17	S5_LVDS19_P	P	B22	A22	P	S5_LVDS20_P	IO_L23P_T3_17	B22	
	B20	IO_L19N_T3_VREF_17	S5_LVDS21_N/VREF	N	B23	A23	N	S5_LVDS22_N	IO_L24N_T3_17	B19	
	C20	IO_L19P_T3_17	S5_LVDS21_P	P	B24	A24	P	S5_LVDS22_P	IO_L24P_T3_17	C19	

FPGA (Kintex-7)			Signal Name	QTH5 (CN32)				Signal Name	FPGA (Kintex-7)		
Bank	Pin#	Pin Name		Pair	Pin#	Pin#	Pair		Pin Name	Pin#	Bank
	K16	IO_L1N_T0_18	S5_LVDS23_N	N	B25	A25	N	S5_LVDS24_N/VREF	IO_L6N_T0_VREF_18	K11	
	L16	IO_L1P_T0_18	S5_LVDS23_P	P	B26	A26	P	S5_LVDS24_P	IO_L6P_T0_18	L11	
	K15	IO_L2N_T0_18	S5_LVDS25_N	N	B27	A27	N	S5_LVDS26_N/C_M_SDA	IO_L3N_T0_DQS_18	L13	
	L15	IO_L2P_T0_18	S5_LVDS25_P	P	B28	A28	P	S5_LVDS26_P	IO_L3P_T0_DQS_18	L12	
	J13	IO_L4N_T0_18	S5_LVDS27_N	N	B29	A29	N	S5_LVDS28_N/C_M_SCL	IO_L5N_T0_18	J14	
	K13	IO_L4P_T0_18	S5_LVDS27_P	P	B30	A30	P	S5_LVDS28_P	IO_L5P_T0_18	K14	
	-	-	TPAD66	-	H3	H4	-	TPAD67	-	-	
	-	-	TPAD68	-	H5	H6	-	TPAD69	-	-	
	G15	IO_L7N_T1_18	S5_LVDS29_N	N	B31	A31	N	S5_LVDS30_N/CLK_N/C_S_SDA	IO_L11N_T1_SRCC_18	G14	
	H15	IO_L7P_T1_18	S5_LVDS29_P	P	B32	A32	P	S5_LVDS30_P/CLK_P	IO_L11P_T1_SRCC_18	H14	
	F13	IO_L12N_T1_MRCC_18	S5_LVDS31_N/CLK_N	N	B33	A33	N	S5_LVDS32_N/C_S_SCL	IO_L8N_T1_18	J12	
	G13	IO_L12P_T1_MRCC_18	S5_LVDS31_P/CLK_P	P	B34	A34	P	S5_LVDS32_P	IO_L8P_T1_18	J11	
18	H16	IO_L9N_T1_DQS_18	S5_LVDS33_N	N	B35	A35	N	S5_LVDS34_N	IO_L10N_T1_18	H12	18
	J16	IO_L9P_T1_DQS_18	S5_LVDS33_P	P	B36	A36	P	S5_LVDS34_P	IO_L10P_T1_18	H11	
	E13	IO_L14N_T2_SRCC_18	S5_LVDS35_N	N	B37	A37	N	S5_LVDS36_N	IO_L15N_T2_DQS_18	B12	
	F12	IO_L14P_T2_SRCC_18	S5_LVDS35_P	P	B38	A38	P	S5_LVDS36_P	IO_L15P_T2_DQS_18	C12	
	E16	IO_L19N_T3_VREF_18	S5_LVDS37_N/VREF	N	B39	A39	N	S5_LVDS38_N	IO_L16N_T2_18	E11	
	F15	IO_L19P_T3_18	S5_LVDS37_P	P	B40	A40	P	S5_LVDS38_P	IO_L16P_T2_18	F11	
	A12	IO_L17N_T2_18	S5_LVDS39_N	N	B41	A41	N	S5_LVDS40_N/VREF	IO_L18N_T2_18	C11	
	A11	IO_L17P_T2_18	S5_LVDS39_P	P	B42	A42	P	S5_LVDS40_P	IO_L18P_T2_18	D11	
	E15	IO_L20N_T3_18	S5_LVDS41_N	N	B43	A43	N	S5_LVDS42_N	IO_L21N_T3_DQS_18	C14	
	E14	IO_L20P_T3_18	S5_LVDS41_P	P	B44	A44	P	S5_LVDS42_P	IO_L21P_T3_DQS_18	D14	
	A13	IO_L22N_T3_18	S5_LVDS43_N	N	B45	A45	N	S5_LVDS44_N	IO_L23N_T3_18	B15	
	B13	IO_L22P_T3_18	S5_LVDS43_P	P	B46	A46	P	S5_LVDS44_P	IO_L23P_T3_18	C15	
	A15	IO_L24N_T3_18	S5_LVDS45_N	N	B47	A47	N	S5_LVDS46_N/CLK_N	IO_L13N_T2_MRCC_18	D13	
	B14	IO_L24P_T3_18	S5_LVDS45_P	P	B48	A48	P	S5_LVDS46_P/CLK_P	IO_L13P_T2_MRCC_18	D12	

FPGA (Kintex-7)			Signal Name	QTH5 (CN32)				Signal Name	FPGA (Kintex-7)		
Bank	Pin#	Pin Name		Pair	Pin#	Pin#	Pair		Pin Name	Pin#	Bank
16	D28	IO_L14N_T2_SRCC_16	S5_LVDS47_N/CLK_N	N	B49	A49	N	S5_LVDS48_N	IO_L15N_T2_DQS_16	B29	16
	E28	IO_L14P_T2_SRCC_16	S5_LVDS47_P/CLK_P	P	B50	A50	P	S5_LVDS48_P	IO_L15P_T2_DQS_16	C29	
	C30	IO_L16N_T2_16	S5_LVDS49_N	N	B51	A51	N	S5_LVDS50_N	IO_L17N_T2_16	A30	
	D29	IO_L16P_T2_16	S5_LVDS49_P	P	B52	A52	P	S5_LVDS50_P	IO_L17P_T2_16	B30	
	G27	IO_L21P_T3_DQS_16	S5_LVDS53	-	B53	A53	N	S5_LVDS51_N/VREF	IO_L19N_T3_VREF_16	H25	
	G29	IO_L22P_T3_16	S5_LVDS55/5V/12V	-	B54	A54	P	S5_LVDS51_P	IO_L19P_T3_16	H24	
	F30	IO_L22N_T3_16	S5_LVDS56/5V	-	B55	A55	N	S5_LVDS52_N	IO_L18N_T2_16	E30	
	H26	IO_L23P_T3_16	S5_LVDS57/5V	-	B56	A56	P	S5_LVDS52_P	IO_L18P_T2_16	E29	
	H27	IO_L23N_T3_16	S5_LVDS58/5V	-	B57	A57	N	S5_LVDS54_N	IO_L20N_T3_16	F28	
	H30	IO_L24P_T3_16	S5_LVDS59/TP	-	B58	A58	P	S5_LVDS54_P	IO_L20P_T3_16	G28	
	G30	IO_L24N_T3_16	S5_LVDS60/2.5V/3.3V	-	B59	A59	N	S5_LVDS_CLK1_N	IO_L13N_T2_MRCC_16	C27	
			QTH5_VCC	-	B60	A60	P	S5_LVDS_CLK1_P	IO_L13P_T2_MRCC_16	D27	
	-	-	(QTH5_VCC) *JP resistor not implemented	-	H7	H8	-	(QTH5_VCC) *JP resistor not implemented	-	-	

9.1.4. Switchover of desctination (Kintex-7/IIC) to which the QTH5 connector is connected

The connection destination of the QTH5 connector can be switched using SW22 and SW23.

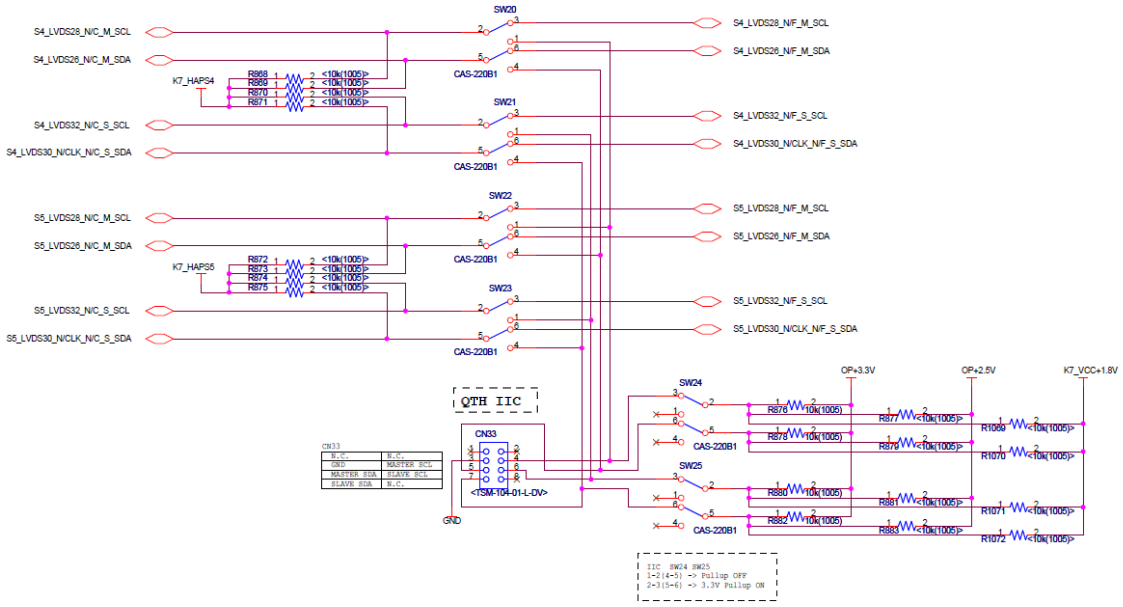


Figure 9-4 Structure of switchover of destination (Kintex-7/IIC) to which the QTH5 connector is connected

Table 9-20 Switchover of destination (Kintex-7/CN33) to which the QTH5 connector is connected

QTH5 CN Pin No.	Device Name		Connect Destination
A29	SW22	2-3	FPGA(Kintex-7): J14
		2-1	CN33: 4pin
A27		5-6	FPGA(Kintex-7): L13
		5-4	CN33: 5pin
A33	SW23	2-3	FPGA(Kintex-7): J12
		2-1	CN33: 6pin
A31		5-6	FPGA(Kintex-7): G14
		5-4	CN33: 7pin

*CN33 is not implemented.

The IIC Pullup ON/OFF switchover can be controlled using SW24 and SW25.
The 1.8V/2.5V/3.3V Pullup selection is also allowed.

Table 9-21 IIC Pullup On/Off Switchover

Connecter Name	Device Name		Action
CN33	SW24 SW25	1-2 4-5	Pullup OFF
		2-3 5-6	3.3V Pullup ON

In addition, the above 3.3V Pullup mode can be switched to 1.8V or 2.5V Pullup mode.
In order to do that, remove a currently implemented 3.3V Pullup resistor and then implement a 1.8V or 2.5V Pullup resistor. (By default, the 1.8V/2.5V Pullup resistor is not implemented).

9.2. FMC Connector

The TB-7V-2000T-LSI board is equipped with one SAMTEC's FMC Connector that is connected to the Kintex-7. Figure 9-5 shows the High-Pin Count Pin Assignments.

High-Pin Count: One (CN34) Note that all HPC and LPC pins are not connected to the FPGA.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure 9-5 HPC (High-Pin Count) Pin Assignments

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure 9-6 LPC (Low-Pin Count) Pin Assignments

9.2.1. HPC Connector (High-Pin Count)

The following shows the HPC interface requirements.

High Speed:	TX 10ch + RX 10ch + 2 Clock Sources (4 pins)
Low Speed:	LA: 5-Pair (10 pins) + 1 Clock Source (2 pins)

The subsequent pages list the HPC connector pin assignments with FPGA.

Table 9-22 HPC Connector (CN34) Pin Assignments

Bank	Pin#	A		B	Pin#	Bank
		GND	1	RES1		
MGTXRXP1_115	Y6	DP1_M2C_P	2	GND		
MGTXRXN1_115	Y5	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	H6	MGTXRXP1_117
		GND	5	DP9_M2C_N	H5	MGTXRXN1_117
MGTXRXP2_115	W4	DP2_M2C_P	6	GND		
MGTXRXN2_115	W3	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	K6	MGTXRXP0_117
		GND	9	DP8_M2C_N	K5	MGTXRXN0_117
MGTXRXP3_115	V6	DP3_M2C_P	10	GND		
MGTXRXN3_115	V5	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	M6	MGTXRXP3_116
		GND	13	DP7_M2C_N	M5	MGTXRXN3_116
MGTXRXP0_116	T6	DP4_M2C_P	14	GND		
MGTXRXN0_116	T5	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	P6	MGTXRXP2_116
		GND	17	DP6_M2C_N	P5	MGTXRXN2_116
MGTXRXP1_116	R4	DP5_M2C_P	18	GND		
MGTXRXN1_116	R3	DP5_M2C_N	19	GND		
		GND	20	*1	*1	*1
		GND	21	*1	*1	*1
MGTXTXP1_115	V2	DP1_C2M_P	22	GND		
MGTXTXN1_115	V1	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	J4	MGTXTXP1_117
		GND	25	DP9_C2M_N	J3	MGTXTXN1_117
MGTXTXP2_115	U4	DP2_C2M_P	26	GND		
MGTXTXN2_115	U3	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	K2	MGTXTXP0_117
		GND	29	DP8_C2M_N	K1	MGTXTXN0_117
MGTXTXP3_115	T2	DP3_C2M_P	30	GND		
MGTXTXN3_115	T1	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	L4	MGTXTXP3_116
		GND	33	DP7_C2M_N	L3	MGTXTXN3_116
MGTXTXP0_116	P2	DP4_C2M_P	34	GND		
MGTXTXN0_116	P1	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	M2	MGTXTXP2_116
		GND	37	DP6_C2M_N	M1	MGTXTXN2_116
MGTXTXP1_116	N4	DP5_C2M_P	38	GND		
MGTXTXN1_116	N3	DP5_C2M_N	39	GND		
		GND	40	RES0		

*1: GBTCLK0/1_M2C_P,N

Three management tiles of reference clock pins can be located by setting the IC81(SN65LVDS250DBT). For more information about the setting, refer to the “7.3. Kintex-7 MGT Reference Clock Selector”.

Bank	Pin#	C		D	Pin#	Bank
		GND	1	*5 PG_C2M		
MGTXTXP0_115	Y2	DP0_C2M_P	2	GND		
MGTXTXN0_115	Y1	DP0_C2M_N	3	GND		
		GND	4	*1	*1	*1
		GND	5	*1	*1	*1
MGTXRXP0_115	AA4	DP0_M2C_P	6	GND		
MGTXRXN0_115	AA3	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC		
		GND	9	LA01_N_CC		
		LA06_P	10	GND		
		LA06_N	11	LA05_P		
		GND	12	LA05_N		
		GND	13	GND		
		LA10_P	14	LA09_P		
		LA10_N	15	LA09_N		
		GND	16	GND		
		GND	17	LA13_P		
		LA14_P	18	LA13_N		
		LA14_N	19	GND		
		GND	20	LA17_P_CC		
		GND	21	LA17_N_CC		
		LA18_P_CC	22	GND		
		LA18_N_CC	23	LA23_P		
		GND	24	LA23_N		
		GND	25	GND		
		LA27_P	26	LA26_P		
		LA27_N	27	LA26_N		
		GND	28	GND		
		GND	29	TCK		
		*2 SCL	30	*4 TDI		
		*2 SDA	31	*4 TDO		
		GND	32	*6 3P3VAUX		
		GND	33	TMS		
		*3 GA0	34	TRST_L		
		*6 12P0V	35	*3 GA1		
		GND	36	*6 3P3V		
		*6 12P0V	37	GND		
		GND	38	*6 3P3V		
		*6 3P3V	39	GND		
		GND	40	*6 3P3V		

Bank	Pin#	E		F	Pin#	Bank
		GND	1	*5 PG M2C		
		HA01_P_CC	2	GND		
		HA01_N_CC	3	GND		
		GND	4	HA00_P_CC		
		GND	5	HA00_N_CC		
		HA05_P	6	GND		
		HA05_N	7	HA04_P		
		GND	8	HA04_N		
		HA09_P	9	GND		
		HA09_N	10	HA08_P		
		GND	11	HA08_N		
		HA13_P	12	GND		
		HA13_N	13	HA12_P		
		GND	14	HA12_N		
		HA16_P	15	GND		
		HA16_N	16	HA15_P		
		GND	17	HA15_N		
		HA20_P	18	GND		
		HA20_N	19	HA19_P		
		GND	20	HA19_N		
		HB03_P	21	GND		
		HB03_N	22	HB02_P		
		GND	23	HB02_N		
		HB05_P	24	GND		
		HB05_N	25	HB04_P		
		GND	26	HB04_N		
		HB09_P	27	GND		
		HB09_N	28	HB08_P		
		GND	29	HB08_N		
		HB13_P	30	GND		
		HB13_N	31	HB12_P		
		GND	32	HB12_N		
	-	HB19_P	33	GND		
	-	HB19_N	34	HB16_P	-	
		GND	35	HB16_N	-	
	-	HB21_P	36	GND		
	-	HB21_N	37	HB20_P	-	
		GND	38	HB20_N	-	
		*6 VADJ	39	GND		
		GND	40	*6 VADJ		

Bank	Pin#	G		H	Pin#	Bank
		GND	1	*7 VREF_A_M2C		
		CLK1_M2C_P	2	*5 PRSNT_M2C_L		
		CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	T26	16
		GND	5	CLK0_M2C_N	T27	16
16	B23	LA00_P_CC	6	GND		
16	A23	LA00_N_CC	7	LA02_P		
		GND	8	LA02_N		
		LA03_P	9	GND		
		LA03_N	10	LA04_P	F25	16
		GND	11	LA04_N	E25	16
16	E23	LA08_P	12	GND		
16	D23	LA08_N	13	LA07_P	F26	16
		GND	14	LA07_N	E26	16
		LA12_P	15	GND		
		LA12_N	16	LA11_P	E24	16
		GND	17	LA11_N	D24	16
		LA16_P	18	GND		
		LA16_N	19	LA15_P		
		GND	20	LA15_N		
		LA20_P	21	GND		
		LA20_N	22	LA19_P		
		GND	23	LA19_N		
		LA22_P	24	GND		
		LA22_N	25	LA21_P		
		GND	26	LA21_N		
		LA25_P	27	GND		
		LA25_N	28	LA24_P		
		GND	29	LA24_N		
		LA29_P	30	GND		
		LA29_N	31	LA28_P		
		GND	32	LA28_N		
		LA31_P	33	GND		
		LA31_N	34	LA30_P		
		GND	35	LA30_N		
		LA33_P	36	GND		
		LA33_N	37	LA32_P		
		GND	38	LA32_N		
		*6 VADJ	39	GND		
		GND	40	*6 VADJ		

Bank	Pin#	J		K	Pin#	Bank
		GND	1	*7 VREF_B_M2C		
		CLK3_M2C_P	2	GND		
		CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P		
		GND	5	CLK2_M2C_N		
	-	HA03_P	6	GND		
	-	HA03_N	7	HA02_P		
		GND	8	HA02_N		
	-	HA07_P	9	GND		
	-	HA07_N	10	HA06_P		
		GND	11	HA06_N		
	-	HA11_P	12	GND		
	-	HA11_N	13	HA10_P		
		GND	14	HA10_N		
	-	HA14_P	15	GND		
	-	HA14_N	16	HA17_P_CC		
		GND	17	HA17_N_CC		
	-	HA18_P	18	GND		
	-	HA18_N	19	HA21_P		
		GND	20	HA21_N		
	-	HA22_P	21	GND		
	-	HA22_N	22	HA23_P		
		GND	23	HA23_N		
	-	HB01_P	24	GND		
	-	HB01_N	25	HB00_P_CC		
		GND	26	HB00_N_CC		
	-	HB07_P	27	GND		
	-	HB07_N	28	HB06_P_CC		
		GND	29	HB06_N_CC		
	-	HB11_P	30	GND		
	-	HB11_N	31	HB10_P		
		GND	32	HB10_N		
	-	HB15_P	33	GND		
	-	HB15_N	34	HB14_P		
		GND	35	HB14_N		
	-	HB18_P	36	GND		
	-	HB18_N	37	HB17_P_CC	-	
		GND	38	HB17_N_CC	-	
		*8 VIO_B_M2C	39	GND		
		GND	40	*8 VIO_B_M2C		

***2 SCL,SDA**

The TB-7V-2000T-LSI board is equipped with test points and a pullup function to realize I2C communications with FMC mezzanine Card. By default, the pullup resistor is not implemented.

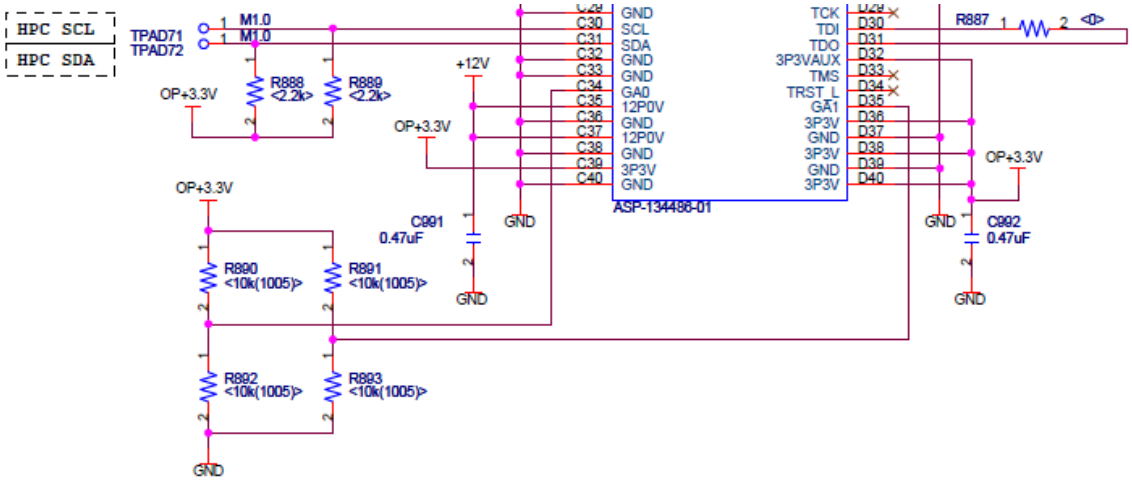


Figure 9-7 SDA,SCL,GA1/0 TDI/TDO Circuit Structure

***3 GA[1:0]**

This circuit is provided for notification of ID data to the FMC mezzanine card.
By default, it is set to “Open”.

***4 TDI,TDO**

This circuit allows for JTAG loopback communications from the FMC mezzanine card.
By default, this loopback function is not provided due to the non-implementation of a R887 resistor.

***5 PG_C2M,PG_M2C,PRSNT_M2C_L**

This circuit allows for signal level output to the FMC mezzanine card.
A similar circuit is provided on the F and H pin of the FMC connector.
By default, it is set to “Open”.
The PG_M2C, PRSNT_M2C_L also has the same structure.

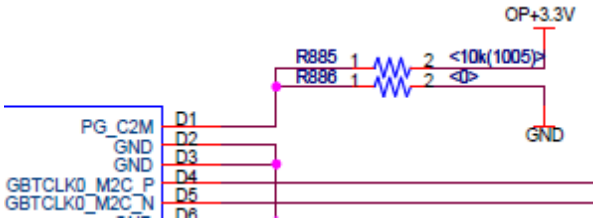


Figure 9-8 PG_C2M Circuit Structure

Table 9-23 PG_C2M,PG_M2C,PRSNT_M2C_L Level Settings

Pin No.	Signal	Level Setting	
		H (P/S)	L (GND)
D1	PG_C2M	R885	R886
F1	PG_M2C	R894	R895
H2	PRSNT_M2C_L	R896	R897

***6 Power Supply**

The TB-7V-2000T-LSI board provides “12V” to 12P0V-pin and “3.3” to 3P3V and 3P3VAUX-pin.
“2.5V” is provided to VADJ-pin.

***7 VREF_A_M2C,VREF_B_M2C**

The TB-7V-2000T-LSI board is equipped with a TPAD73 test pad to monitor the “VREF_A_M2C” on H1-pin and a TRAD74 test pad to monitor “VREF_B_M2C” on K1-pin.

***8 VIO_B_M2C**

The TB-7V-2000T-LSI board is equipped with a TP51 test pad to monitor “VIO_B_M2C” on J39 and K40 pins.

9.3. RS-232C

The TB-7V-2000T-LSI board is equipped with a RS-232C interface that allows the connection to an external device.

The FPGA connection is enabled through the use of onboard jumpers.

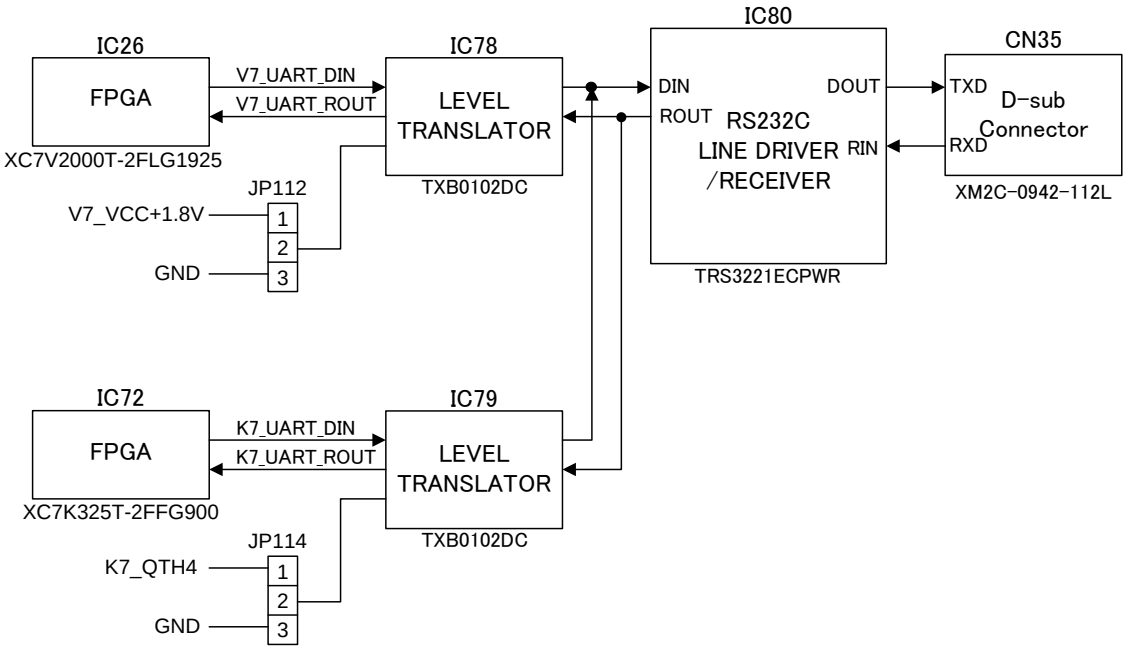


Figure 9-9 RS-232C Circuit Structure

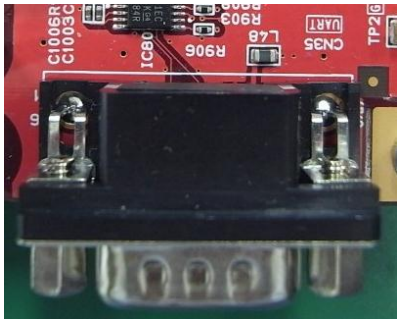


Figure 9-10 Onboad D-sub Connector

Table 9-24 FPGA Signal Connections

FPGA	Pin No.	Signal Name	Bank	Level
Virtex-7	AD29	V7_UART_DIN	15	1.8V
	AB32	V7_UART_ROUT		
Kintex-7	T20	K7_UART_DIN	14	1.8V/2.5V/3.3V
	T21	K7_UART_ROUT		

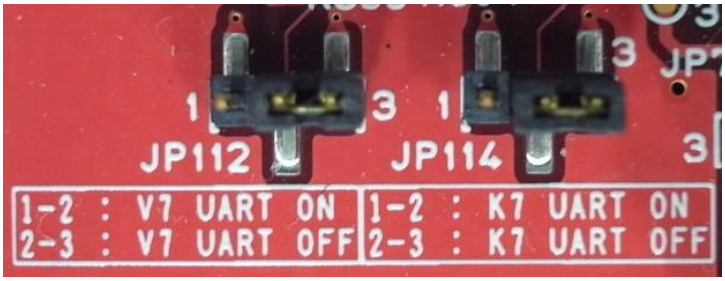


Figure 9-11 Onboard FPGA Connectivity Jumpers

Table 9-25 FPGA (Virtex-7) Connectdivity Jumper Settings

JP112	FPGA SEL
1-2	V7 UART ON
2-3	V7 UART OFF

Table 9-26 FPGA (Kintex-7) Connectivity Jumper Settings

JP114	FPGA SEL
1-2	K7 UART ON
2-3	K7 UART OFF

*Do not turn on the UART on Virtex-7 and the UART on Kintex-7 simultaneously.

9.4. DipSW

The TB-7V-2000T-LSI board is equipped with one 8-position DIPSW for Kintex-7.
When the DIPSW is switched on, then there is “low” level on FPGA input.

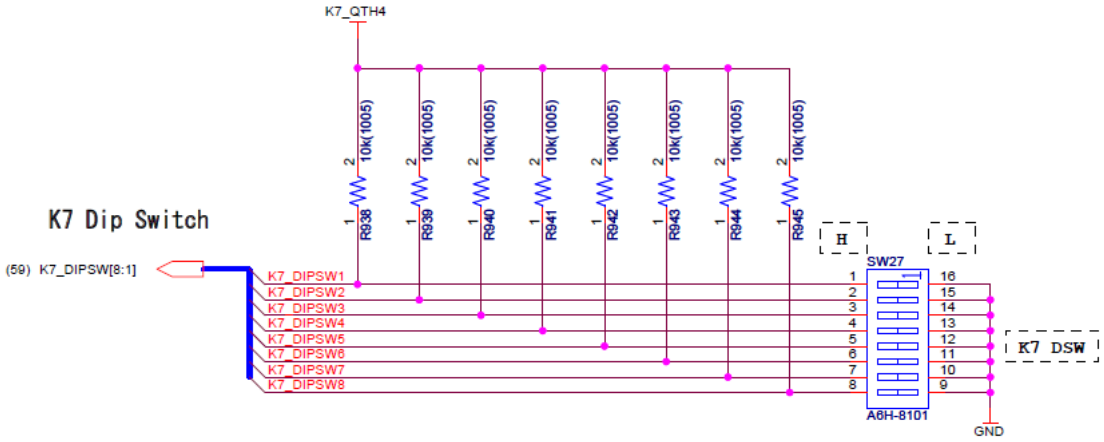


Figure 9-12 Onboad Kintex-7 dedicated DIPSW

Table 9-27 Kintex-7 Dedicted DIPSW Pin Assignments

Device			FPGA(Kintex-7)		
Name	Pin No.	Signal Name	Pin No.	Bank	Level
SW27	1	K7_DIPSW1	U20	13	1.8V/2.5V/3.3V
	2	K7_DIPSW2	P29		
	3	K7_DIPSW3	R29		
	4	K7_DIPSW4	P27		
	5	K7_DIPSW5	P28		
	6	K7_DIPSW6	R30		
	7	K7_DIPSW7	T30		
	8	K7_DIPSW8	P26		
	9-16	GND	-	-	-

9.5. PushSW

The boad is equipped with four Kintex-7 dedicated PushSW.

When the PushSW is pressed down, then there is “low” level on FPGA input.

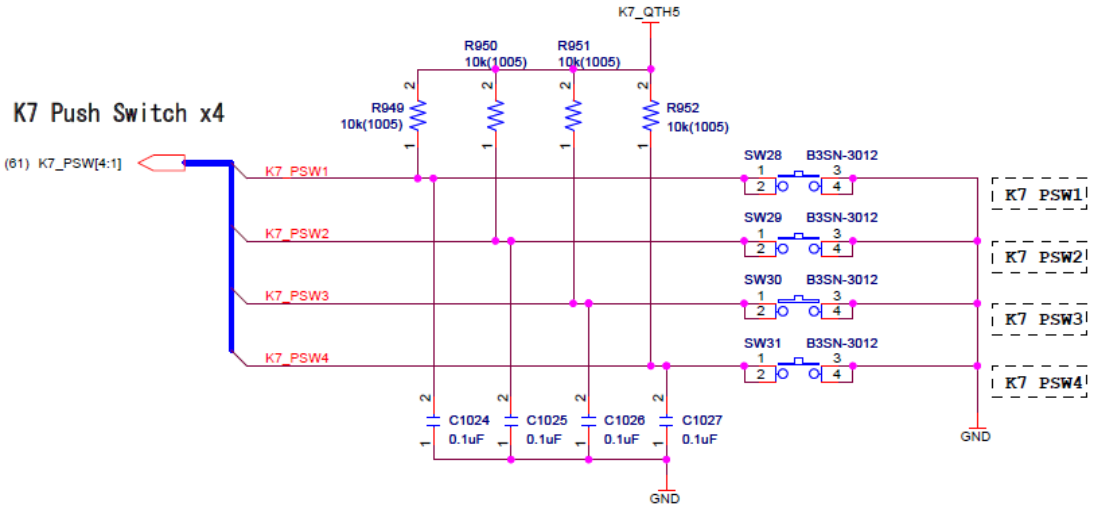


Figure 9-13 Kintex-7 Dedicated PushSW Structure

Figure 9-14 Onboard PushSWs

Table 9-28 Kintex-7 Dedicated PushSW Pin Assignments

Device		FPGA(Kintex-7)		
Name	Signal Name	Pin No.	Bank	Level
SW28	K7_PSW1	G23	16	1.8V/2.5V/3.3V
SW29	K7_PSW2	G24		
SW30	K7_PSW3	B27		
SW31	K7_PSW4	A27		

9.6. LED

The TB-7V-2000T-LSI board is equipped with six Kintex-7 dedicated LEDs.
Each LED will light up when the corresponding FPGA output pin is driven “High”.

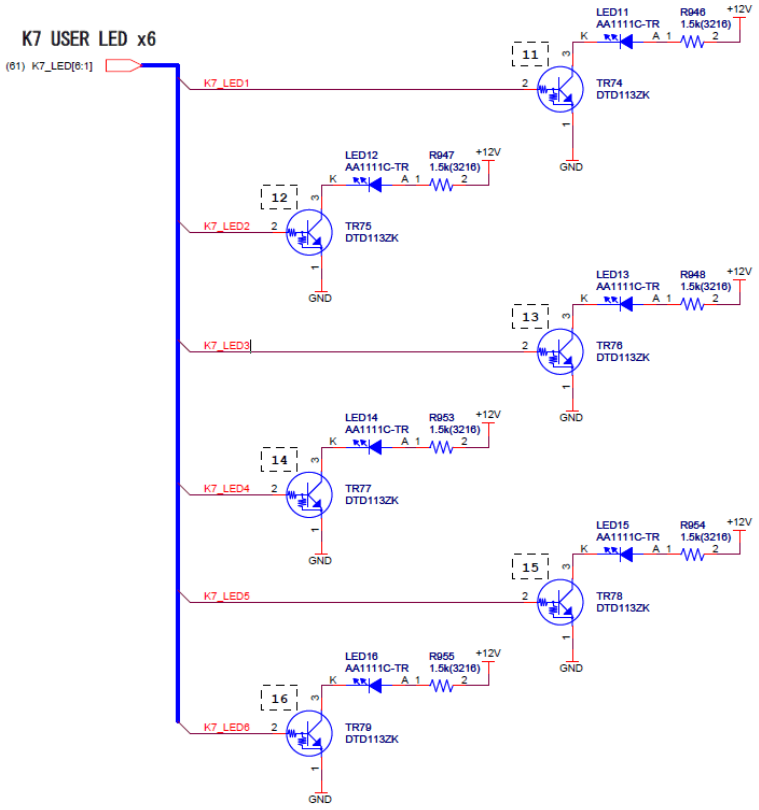


Figure 9-15 Kintex-7 Dedicated LED Structure

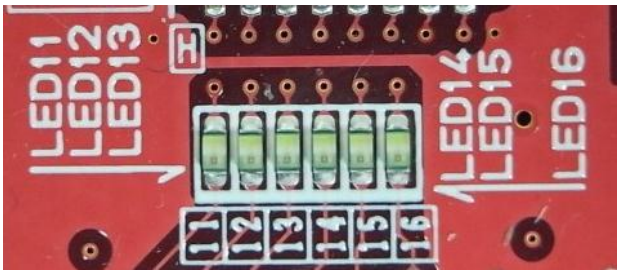


Figure 9-16 Onboard Kintex-7 Dedicated LEDs

Table 9-29 Kintex-7 Dedicated LED Pin Assignments

Device		FPGA (Kintex-7)		
Name	Signal Name	Pin No.	Bank	Level
LED11	K7_LED1	C24	16	1.8V/2.5V/3.3V
LED12	K7_LED2	B24		
LED13	K7_LED3	B28		
LED14	K7_LED4	A28		
LED15	K7_LED5	A25		
LED16	K7_LED6	A26		

9.7. XADC Dedicated Pin Header

The TB-7V-2000T-LSI board is equipped with a Kintex-7 XADC dedicated 14-pin PinHeader.

In the case of using a dedicated differential analog input (VP_0,VN_0), do not implement R819 and R820. While, in the case of using a thermal diode (DXP_0, DXN_0), do not implement R821 and R822.

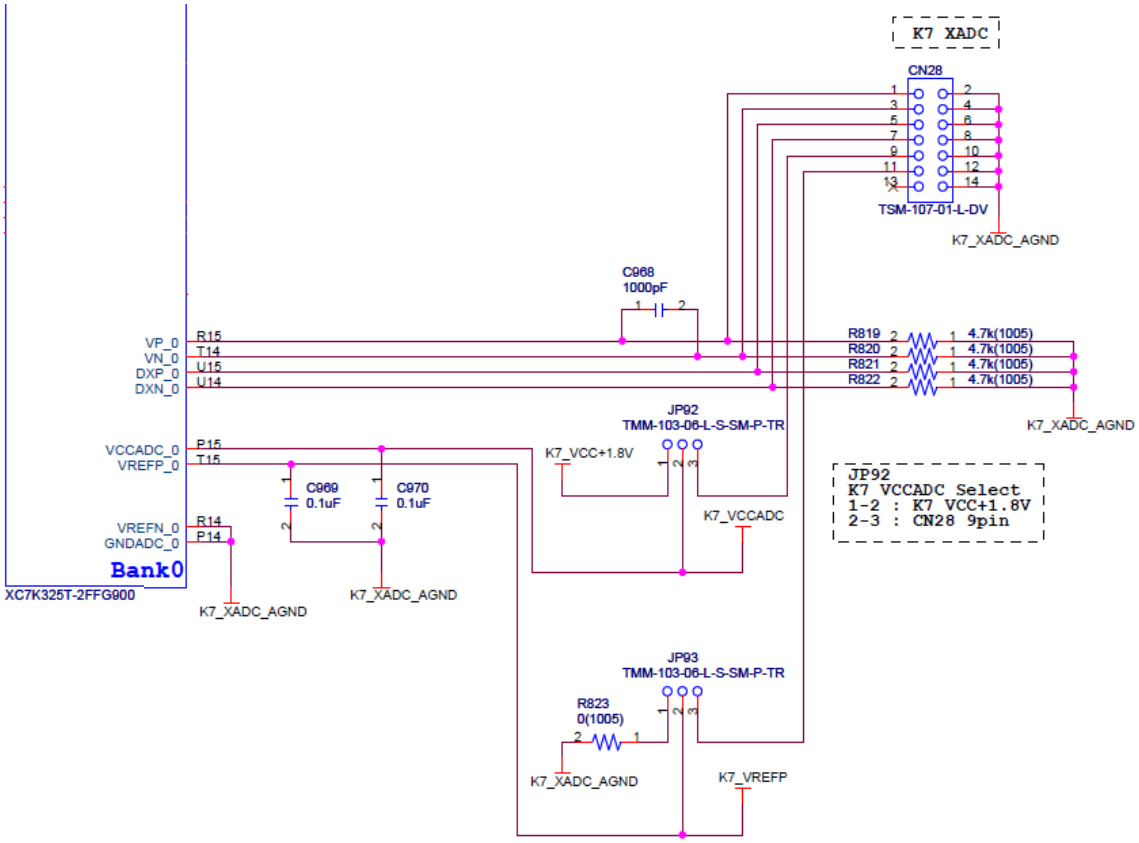


Figure 9-17 Kintex-7 XADC Dedicated PinHeader Sructure

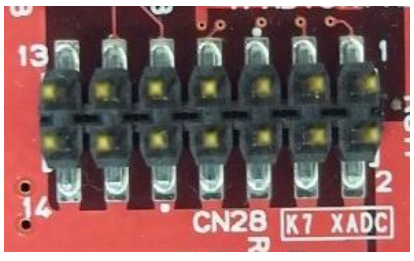


Figure 9-18 Onboard XADC Dedicated PinHeader

Table 9-30 Kintex-7 XADC Dedicated PinHeader Pin Assignments

FPGA		PinHeader(CN28)			
Bank No.	Pin No.	Signal Name	Pin No.		Signal Name
0	R15	VP	1	2	K7_XADC_AGND
0	T14	VN	3	4	K7_XADC_AGND
0	U15	DXP	5	6	K7_XADC_AGND
0	U14	DXN	7	8	K7_XADC_AGND
-	-	VCCADC Power supply	9	10	K7_XADC_AGND
-	-	VREFP Power supply	11	12	K7_XADC_AGND
-	-	-	13	14	K7_XADC_AGND

9.8. Battery Control

The TB-7V-2000T-LSI board is equipped with a battery control circuit on the solder side. By default, the battery socket is not implemented.

The battery is connected to the Kintex-7 VCCVBATT (C10) pin.

Use a “CR1220” size of button battery.

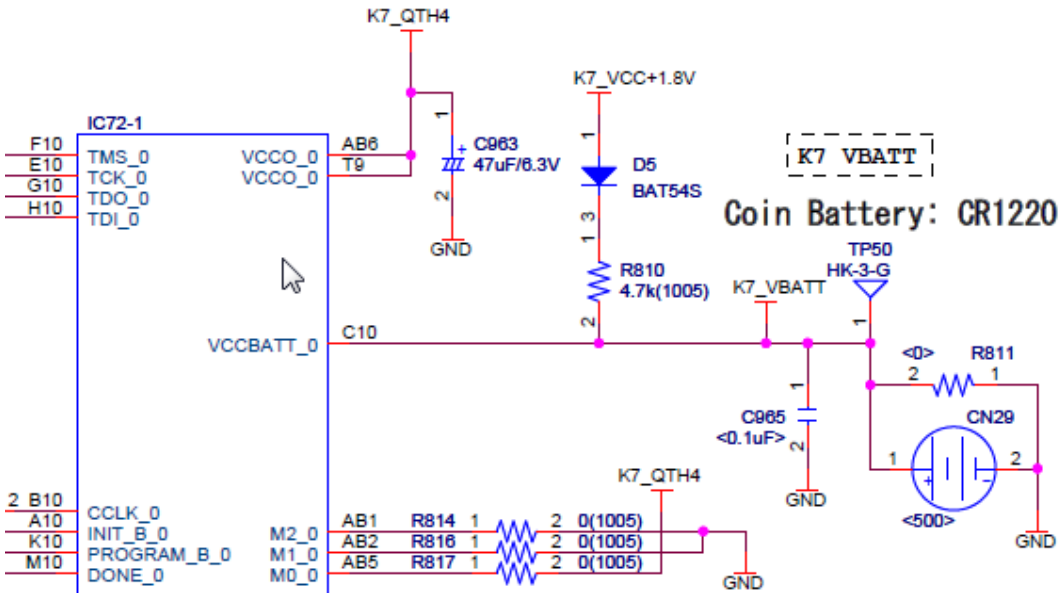


Figure 9-19 Kintex-7 Battery Structure

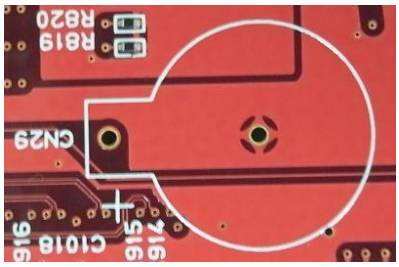


Figure 9-20 Onboard Kintex-7 Battery

9.9. Quad SPI Flash

The TB-7V-2000T-LSI board is equipped with a 128-Mbyte QSPI flash memory for Kintex-7 configuration that is connected to the FPGA via a level shiftor.
For information about configurationmethod, refer to Section 11.

Table 9-31 QSPI Flash Memory for Configuration

Signal name	CF_D0	CF_D1	CF_D2	CF_D3	CF_FCS_B
FPGA Pin#	P24	R25	R20	R21	U19

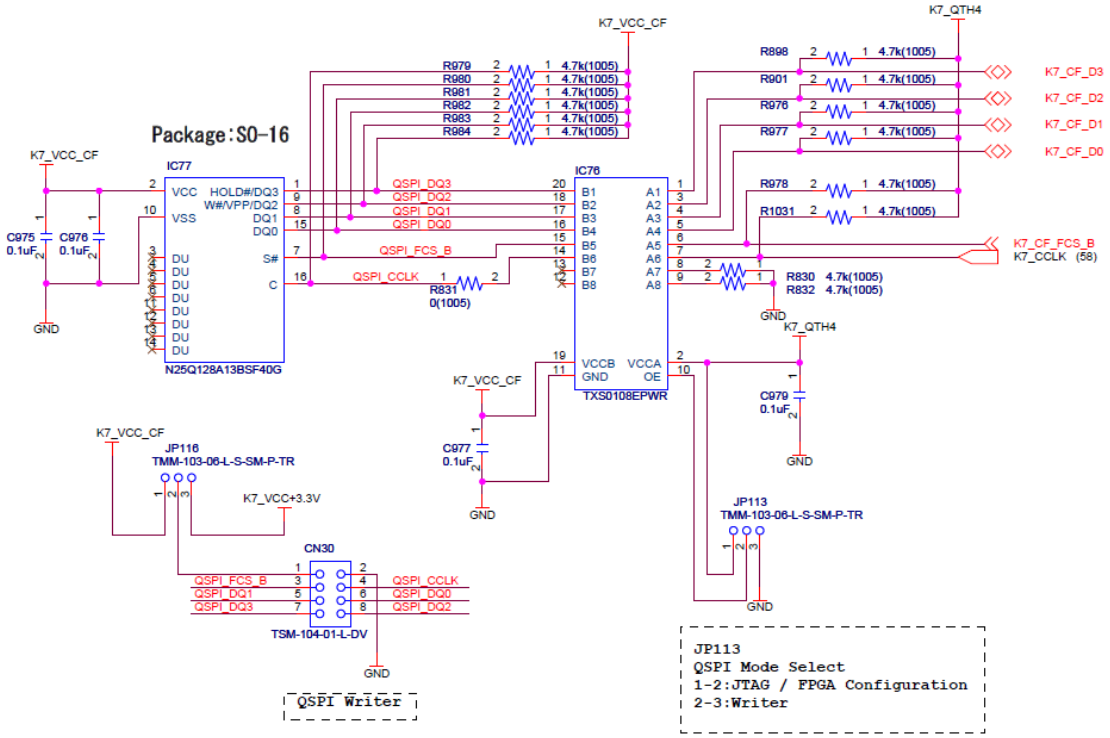


Figure 9-21 QSPI Flash Memory Structure

10. Virtex-7 and Kintex-7 Interconnection

Virtex-7 [IC26] and Kintex-7 [IC72] are interconnected on the board using 4 Banks.
The interface is 1.8V. Note that Bank12 (HR) on Kintex-7 [IC72] does not support differential signals. So, only 3 Banks are used for the differential signal interface.

The following shows the number of signal lines per 1Bank.

- Clock Source: 4
- Data: 20 (differential) and 2 (single)

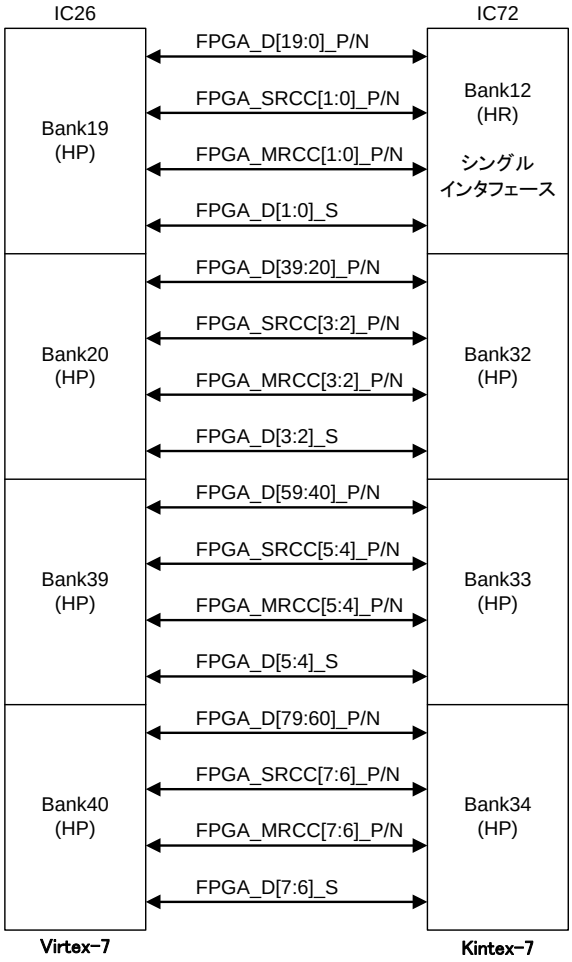


Figure 10-1 FPGA Interconnections

Table 10-1 shows the pin assignments for Virtex-7 [IC26] and Kintex-7 [IC72] interconnection.

Table 10-1 Pin Assignments for FPGA Interconnection ([IC26] Bank19 - [IC72] Bank12)

Virtex-7 [IC26]		Signal Name	Kintex-7 [IC72]	
Bank	Pin No.		Pin No.	Bank
19	M30	FPGA_D0_P	AB22	12
	M31	FPGA_D0_N	AB23	
	L32	FPGA_D1_P	AB24	
	L33	FPGA_D1_N	AC25	
	N29	FPGA_D2_P	Y21	
	M29	FPGA_D2_N	AA21	
	N32	FPGA_D3_P	Y23	
	N33	FPGA_D3_N	Y24	
	L29	FPGA_D4_P	AA20	
	L30	FPGA_D4_N	AB20	
	N31	FPGA_D5_P	AA22	
	M32	FPGA_D5_N	AA23	
	D33	FPGA_D6_P	AG22	
	C33	FPGA_D6_N	AH22	
	G31	FPGA_D7_P	AG25	
	G32	FPGA_D7_N	AH25	
	C32	FPGA_D8_P	AJ22	
	B32	FPGA_D8_N	AJ23	
	F33	FPGA_D9_P	AF20	
	E33	FPGA_D9_N	AF21	
	A32	FPGA_D10_P	AJ24	
	A33	FPGA_D10_N	AK25	
	B30	FPGA_D11_P	AK23	
	B31	FPGA_D11_N	AK24	
	A29	FPGA_D12_P	AH21	
	A30	FPGA_D12_N	AJ21	
	C29	FPGA_D13_P	AG20	
	B29	FPGA_D13_N	AH20	
	H31	FPGA_D14_P	AE25	
	H32	FPGA_D14_N	AF25	
	J33	FPGA_D15_P	AC22	
	H33	FPGA_D15_N	AD22	
	K30	FPGA_D16_P	AC20	
	J30	FPGA_D16_N	AC21	
	K31	FPGA_D17_P	AK20	
	J31	FPGA_D17_N	AK21	
	K32	FPGA_D18_P	AC24	
	K33	FPGA_D18_N	AD24	
	H29	FPGA_D19_P	AD21	
	G30	FPGA_D19_N	AE21	

Virtex-7 [IC26]		Signal Name	Kintex-7 [IC72]	
Bank	Pin No.		Pin No.	Bank
19	F32	FPGA_SRCC0_P	AG24	12
	E32	FPGA_SRCC0_N	AH24	
	F30	FPGA_SRCC1_P	AE23	
	E30	FPGA_SRCC1_N	AF23	
	E31	FPGA_MRCC0_P	AF22	
	D31	FPGA_MRCC0_N	AG23	
	D30	FPGA_MRCC1_P	AD23	
	C31	FPGA_MRCC1_N	AE24	
	P29	FPGA_D0_S	Y20	
	J29	FPGA_D1_S	AE20	

Table 10-2 Pin Assignments for FPGA Interconnection ([IC26] Bank20 - [IC72] Bank32)

Virtex-7 [IC26]		Signal Name	Kintex-7 [IC72]	
Bank	Pin No.		Pin No.	Bank
20	P35	FPGA_D20_P	AG15	32
	P36	FPGA_D20_N	AH15	
	N36	FPGA_D21_P	AE16	
	N37	FPGA_D21_N	AF16	
	T35	FPGA_D22_P	AJ19	
	R35	FPGA_D22_N	AK19	
	N38	FPGA_D23_P	AJ18	
	N39	FPGA_D23_N	AK18	
	R36	FPGA_D24_P	AH16	
	R37	FPGA_D24_N	AJ16	
	M39	FPGA_D25_P	AH17	
	M40	FPGA_D25_N	AJ17	
	T39	FPGA_D26_P	AB19	
	T40	FPGA_D26_N	AC19	
	N41	FPGA_D27_P	AG19	
	M41	FPGA_D27_N	AH19	
	T37	FPGA_D28_P	Y19	
	T38	FPGA_D28_N	Y18	
	P41	FPGA_D29_P	AC16	
	N42	FPGA_D29_N	AC15	
	P43	FPGA_D30_P	AB17	
	N43	FPGA_D30_N	AC17	
	T43	FPGA_D31_P	AA18	
	R43	FPGA_D31_N	AB18	
	P44	FPGA_D32_P	AD19	
	N44	FPGA_D32_N	AE19	
	U44	FPGA_D33_P	AA17	
	T44	FPGA_D33_N	AA16	
	T33	FPGA_D34_P	AK16	
	T34	FPGA_D34_N	AK15	
	P33	FPGA_D35_P	AF15	
	P34	FPGA_D35_N	AG14	
	R30	FPGA_D36_P	AC14	
	R31	FPGA_D36_N	AD14	
	R32	FPGA_D37_P	AE15	
	R33	FPGA_D37_N	AE14	
	T29	FPGA_D38_P	Y16	
	T30	FPGA_D38_N	Y15	
	P30	FPGA_D39_P	AA15	
	P31	FPGA_D39_N	AB15	

Virtex-7 [IC26]		Signal Name	Kintex-7 [IC72]	
Bank	Pin No.		Pin No.	Bank
20	P39	FPGA_SRCC2_P	AD17	32
	P40	FPGA_SRCC2_N	AD16	
	T42	FPGA_SRCC3_P	AF18	
	R42	FPGA_SRCC3_N	AG18	
	R38	FPGA_MRCC2_P	AF17	
	P38	FPGA_MRCC2_N	AG17	
	R40	FPGA_MRCC3_P	AD18	
	R41	FPGA_MRCC3_N	AE18	
	N34	FPGA_D2_S	Y14	
	T32	FPGA_D3_S	AB14	

Table 10-3 Pin Assignments for FPGA Interconnection ([IC26] Bank39 - [IC72] Bank33)

Virtex-7 [IC26]		Signal Name	Kintex-7 [IC72]	
Bank	Pin No.		Pin No.	Bank
39	F8	FPGA_D40_P	AK14	33
	E8	FPGA_D40_N	AK13	
	H8	FPGA_D41_P	AC12	
	H7	FPGA_D41_N	AC11	
	F7	FPGA_D42_P	AJ13	
	E7	FPGA_D42_N	AJ12	
	G7	FPGA_D43_P	AA13	
	G6	FPGA_D43_N	AB13	
	G5	FPGA_D44_P	AH14	
	F5	FPGA_D44_N	AJ14	
	J6	FPGA_D45_P	AA12	
	H6	FPGA_D45_N	AB12	
	C7	FPGA_D46_P	AH11	
	C6	FPGA_D46_N	AJ11	
	D8	FPGA_D47_P	AG13	
	C8	FPGA_D47_N	AH12	
	B6	FPGA_D48_P	AJ9	
	B5	FPGA_D48_N	AK9	
	B7	FPGA_D49_P	AK11	
	A7	FPGA_D49_N	AK10	
	C2	FPGA_D50_P	AD9	
	B2	FPGA_D50_N	AE9	
	A5	FPGA_D51_P	AF12	
	A4	FPGA_D51_N	AG12	
	D1	FPGA_D52_P	AD8	
	C1	FPGA_D52_N	AE8	
	B4	FPGA_D53_P	AG9	
	A3	FPGA_D53_N	AH9	
	G4	FPGA_D54_P	AE13	
	F4	FPGA_D54_N	AF13	
	H3	FPGA_D55_P	Y11	
	H2	FPGA_D55_N	Y10	
	F3	FPGA_D56_P	AB9	
	E3	FPGA_D56_N	AC9	
	G2	FPGA_D57_P	AA8	
	F2	FPGA_D57_N	AB8	
	E2	FPGA_D58_P	AB10	
	E1	FPGA_D58_N	AC10	
	H1	FPGA_D59_P	AA11	
	G1	FPGA_D59_N	AA10	

Virtex-7 [IC26]		Signal Name	Kintex-7 [IC72]	
Bank	Pin No.		Pin No.	Bank
39	E5	FPGA_SRCC4_P	AE10	33
	D5	FPGA_SRCC4_N	AF10	
	D4	FPGA_SRCC5_P	AE11	
	C4	FPGA_SRCC5_N	AF11	
	E6	FPGA_MRCC4_P	AG10	
	D6	FPGA_MRCC4_N	AH10	
	D3	FPGA_MRCC5_P	AD12	
	C3	FPGA_MRCC5_N	AD11	
	J8	FPGA_D4_S	Y13	
	H4	FPGA_D5_S	AD13	

Table 10-4 Pin Assignments for FPGA Interconnection ([IC26] Bank40-[IC72] Bank34)

Virtex-7 [IC26]		Signal Name	Kintex-7 [IC72]	
Bank	Pin No.		Pin No.	Bank
40	L17	FPGA_D60_P	AD2	34
	K17	FPGA_D60_N	AD1	
	L18	FPGA_D61_P	AF7	
	K18	FPGA_D61_N	AG7	
	J18	FPGA_D62_P	AE4	
	H18	FPGA_D62_N	AE3	
	M20	FPGA_D63_P	AJ6	
	L20	FPGA_D63_N	AK6	
	J19	FPGA_D64_P	AK5	
	H19	FPGA_D64_N	AK4	
	M19	FPGA_D65_P	AC2	
	L19	FPGA_D65_N	AC1	
	A19	FPGA_D66_P	AG2	
	A18	FPGA_D66_N	AH1	
	B20	FPGA_D67_P	AH2	
	A20	FPGA_D67_N	AJ2	
	C19	FPGA_D68_P	AF3	
	B19	FPGA_D68_N	AF2	
	C21	FPGA_D69_P	AJ1	
	B21	FPGA_D69_N	AK1	
	E21	FPGA_D70_P	AJ3	
	D21	FPGA_D70_N	AK3	
	K20	FPGA_D71_P	AD6	
	J20	FPGA_D71_N	AE6	
	G21	FPGA_D72_P	AG4	
	G20	FPGA_D72_N	AG3	
	F18	FPGA_D73_P	AE1	
	E18	FPGA_D73_N	AF1	
	P19	FPGA_D74_P	AH7	
	N19	FPGA_D74_N	AJ7	
	R20	FPGA_D75_P	AJ8	
	P20	FPGA_D75_N	AK8	
	T20	FPGA_D76_P	AF8	
	T19	FPGA_D76_N	AG8	
	T18	FPGA_D77_P	AC5	
	R18	FPGA_D77_N	AC4	
	T17	FPGA_D78_P	AC7	
	R17	FPGA_D78_N	AD7	
	P18	FPGA_D79_P	AD4	
	N18	FPGA_D79_N	AD3	

Virtex-7 [IC26]		Signal Name	Kintex-7 [IC72]	
Bank	Pin No.		Pin No.	Bank
40	D18	FPGA_SRCC6_P	AE5	34
	C18	FPGA_SRCC6_N	AF5	
	F20	FPGA_SRCC7_P	AH6	
	E20	FPGA_SRCC7_N	AH5	
	D20	FPGA_MRCC6_P	AF6	
	D19	FPGA_MRCC6_N	AG5	
	G19	FPGA_MRCC7_P	AH4	
	F19	FPGA_MRCC7_N	AJ4	
	M17	FPGA_D6_S	AC6	
	N17	FPGA_D7_S	AB7	

11. Generating a Kintex-7 Configuration File

11.1. How to Generate a Configuration File (bit file)

The following operations are described assuming that the user uses tool version “ISE14.2”. Similar setting procedure will be applied to 14.2 or later version.

Right click **Generate Programming File** on the Processes window and select **Process properties**. The Process Properties window will appear.

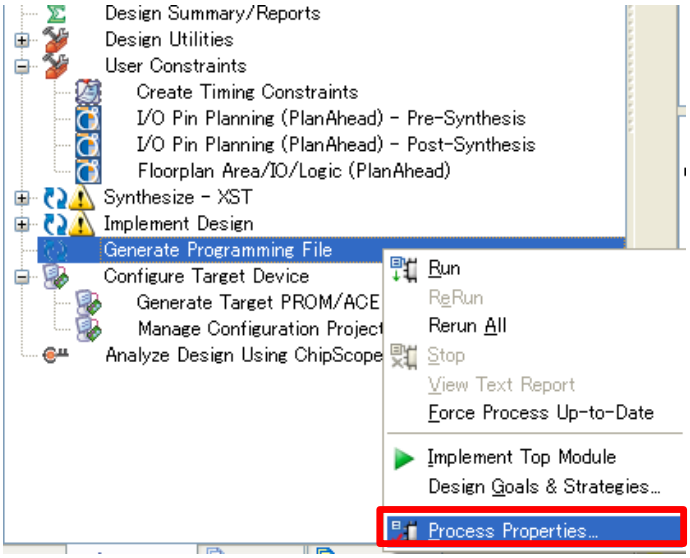


Figure 11-1 Process Properties Window

A QSPI Flash Memory is provided for configuration. Set the QSPI bus width to “4” in the Configuration Options settings that are used when generatingg a bit file.

Caution: Make sure that Property display level is set to Advanced.

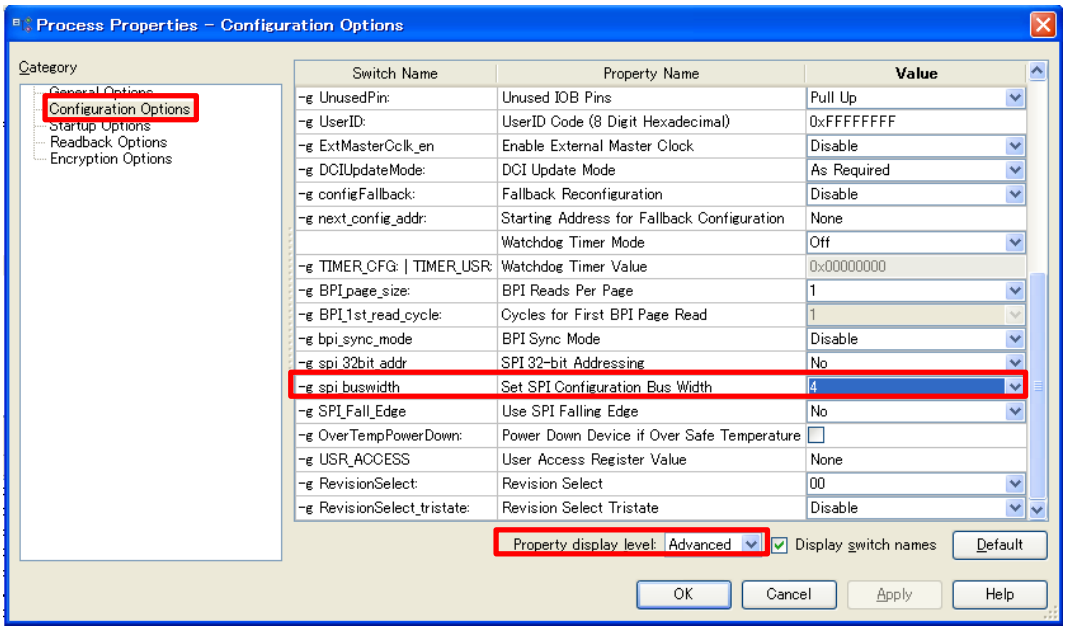


Figure 11-2 Options available when generating a bit file

11.2. Required Configuration Time

As for configuration using a Flash Memory, configuration time can be changed by selecting a desired configuration clock on ISE Tool.

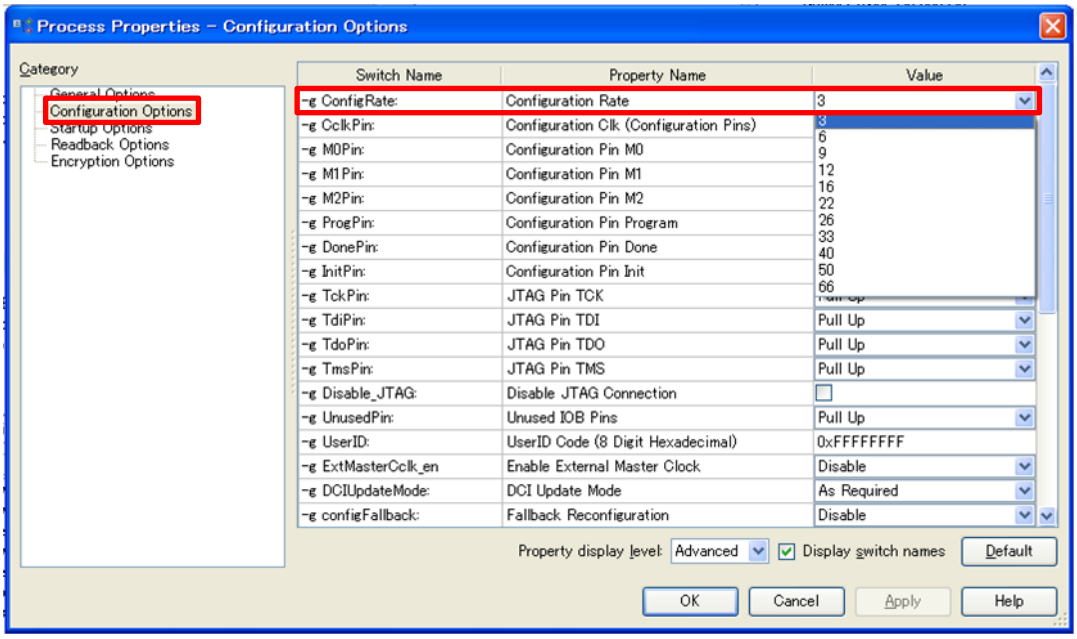


Figure 11-3 Changing Configuration Time

Estimated configuration time:
Configuration Rate = 3MHz: Configuration Time = approx.10 seconds
Configuration Rate = 16MHz: Configuration Time = approx. 2 seconds
Configuration Rate = 33MHz: Configuration Time = approx. 1 second

11.3. Unused Pin Settings

In the Configuration Options settings, set the unused pins to “Float” as shown in Figure 11-4.

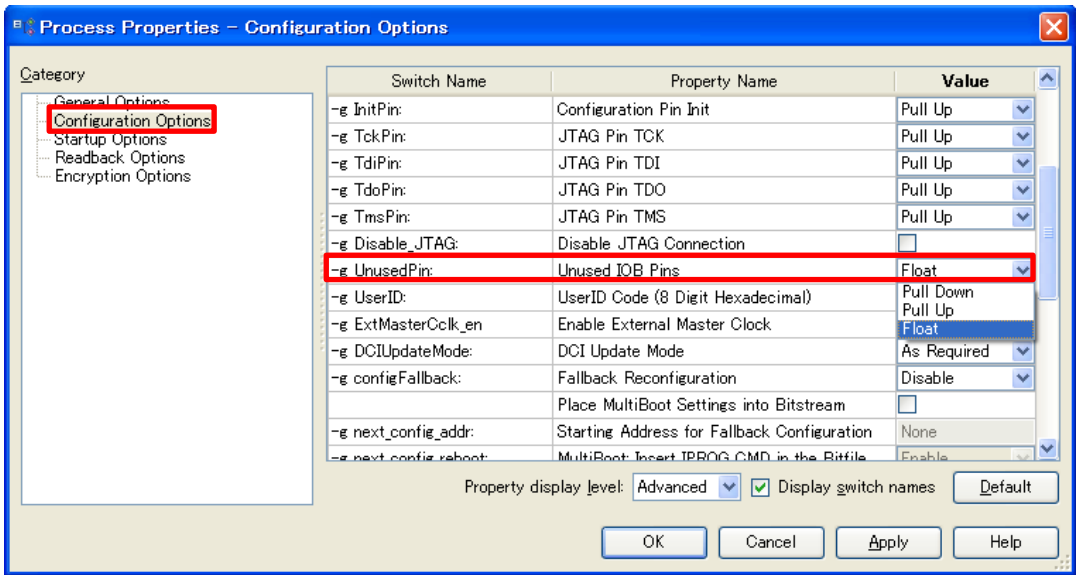


Figure 11-4 Unused Pin Settings

11.4. How to Generate a Configuration File (mcs file)

The following describes how to create a configuration file.

Generate a configuration file that is loaded to the Flash Memory in accordance with the following procedure.

1. Double click **Generate Target PROM/ACE File**.

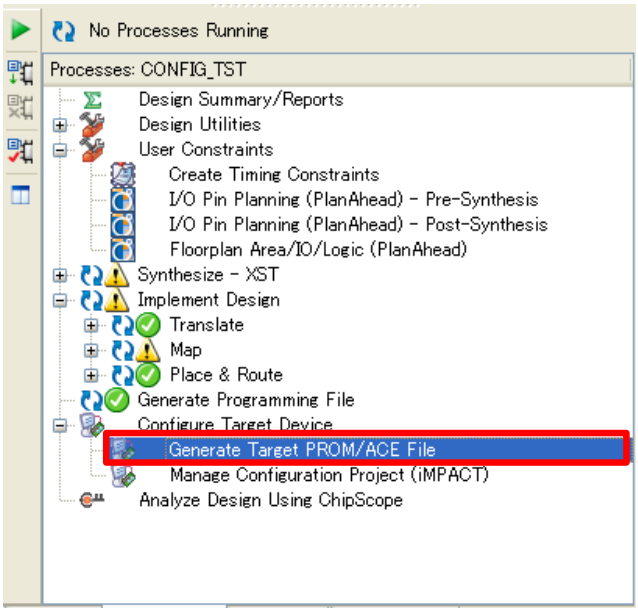


Figure 11-5 Generating a Configurtion File on ISE

2. If the following Warning message appears, click **OK**.

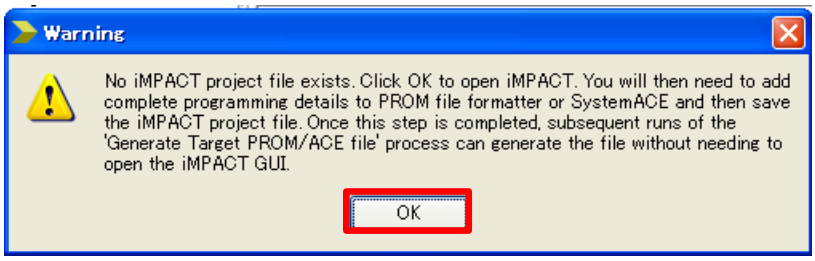


Figure 11-6 Warning Message

3. When iMPACT is started, double click **Create PROM File**.

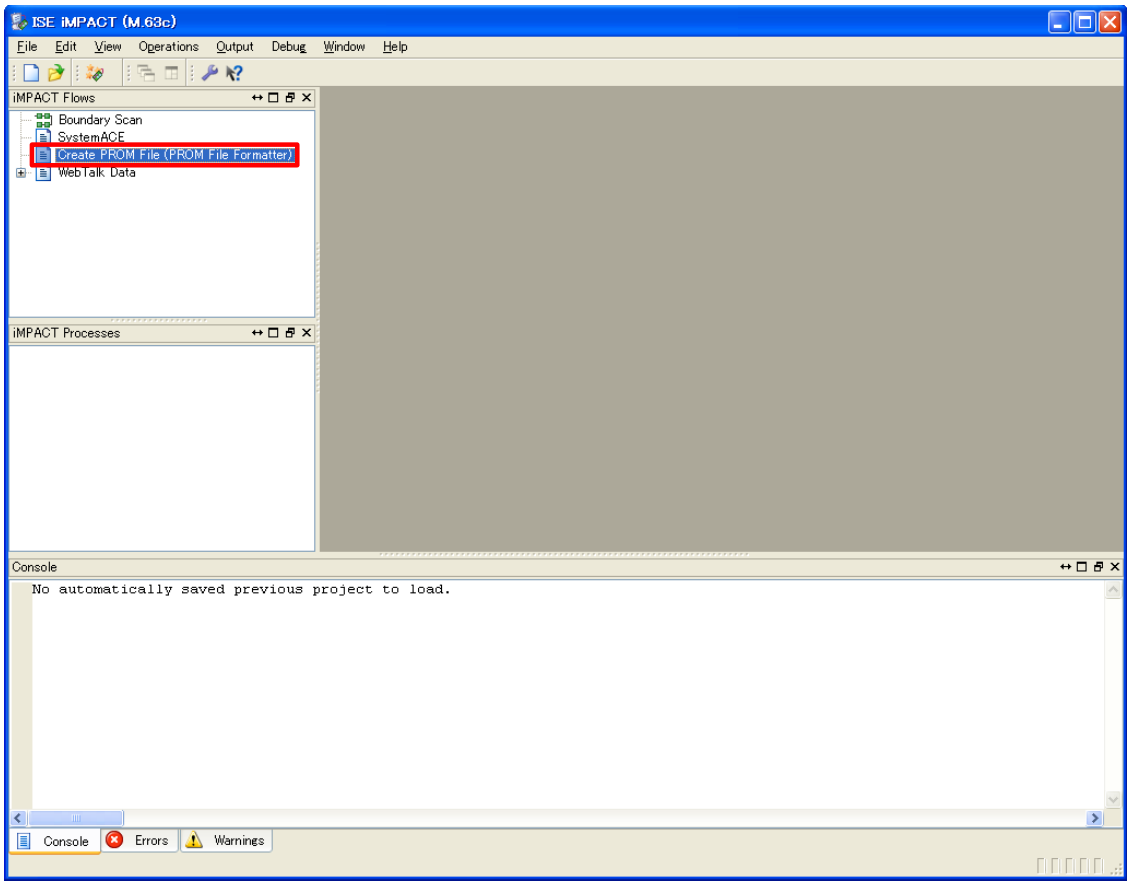


Figure 11-7 iMPACT Window - 1

4. Select **SPI Flash－Configure Single FPGA** and click an "**Arrow**".

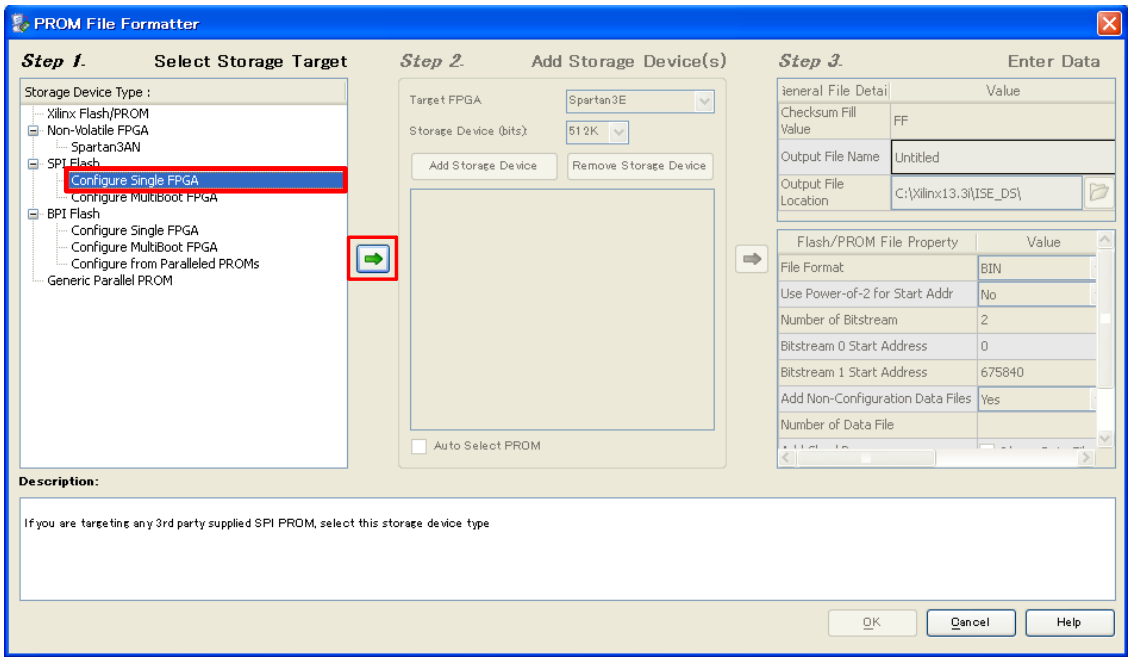


Figure 11-8 iMPACT Window - 2

5. Select **128M** in the Storage Device(bits) field and click **Add Storage Device**.

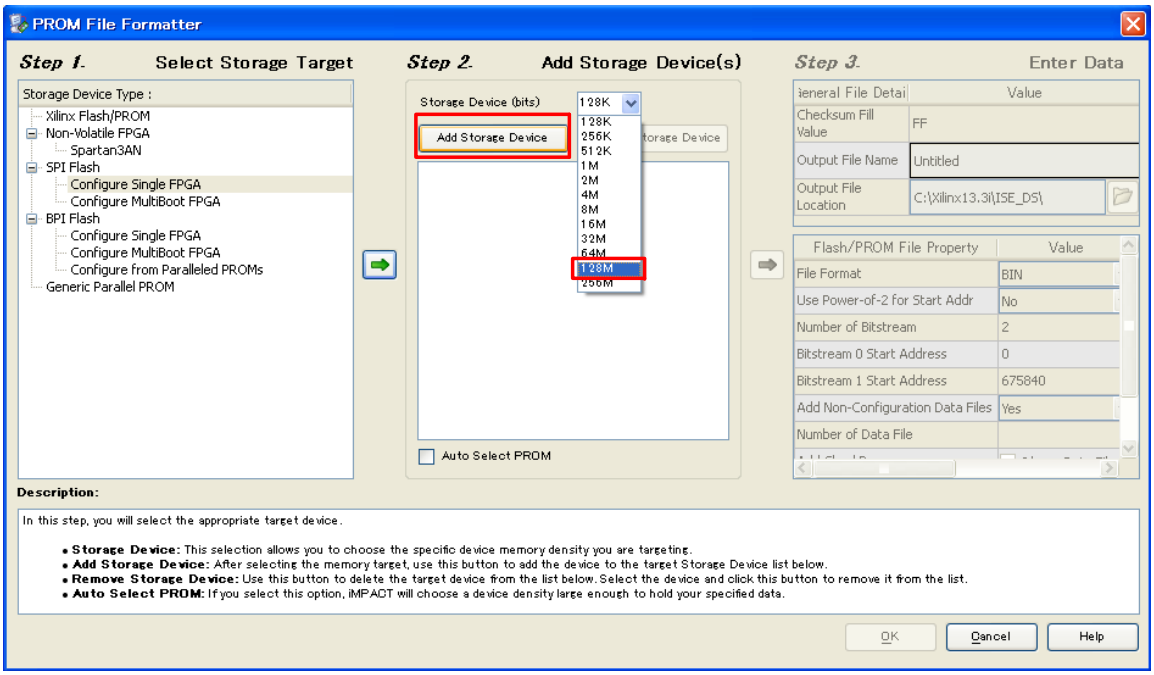


Figure 11-9 iMPACT Window - 3

6. After clicking an **Arrow**, enter your desired name (directory) in the **Output File Name** and the **Output File Location** field and click **OK**.

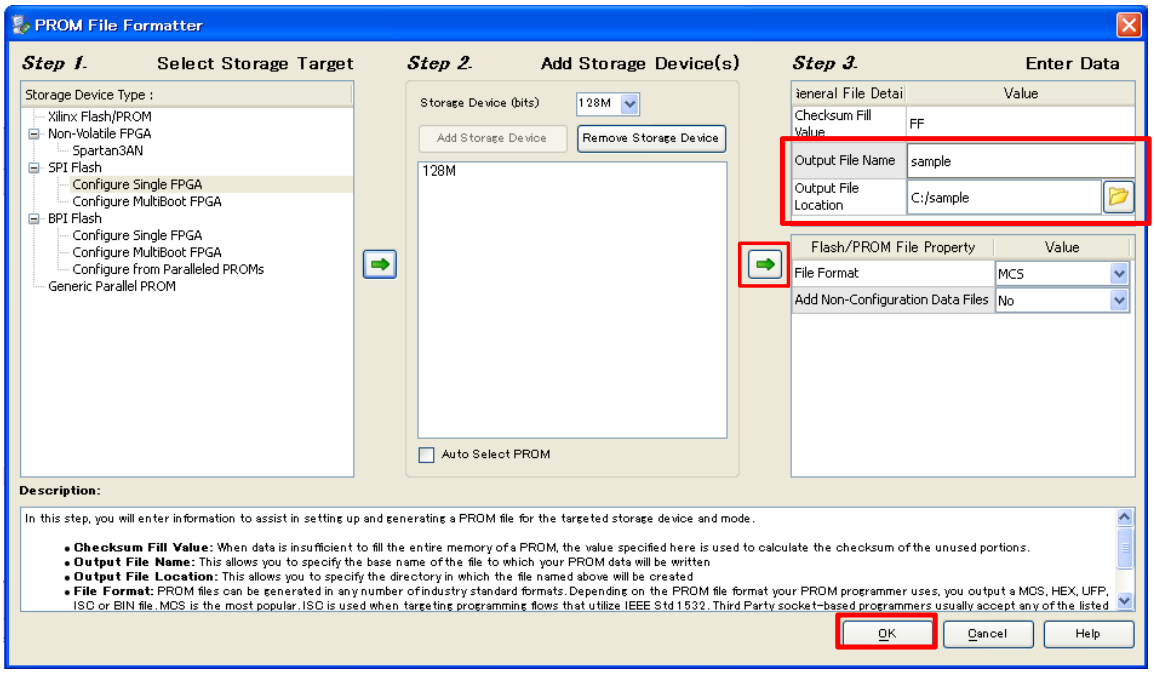


Figure 11-10 iMPACT Window - 4

7. Click **OK**.

Figure 11-11 iMPACT Window - 5

8. Choose a **bit file** to generate a configuration file.

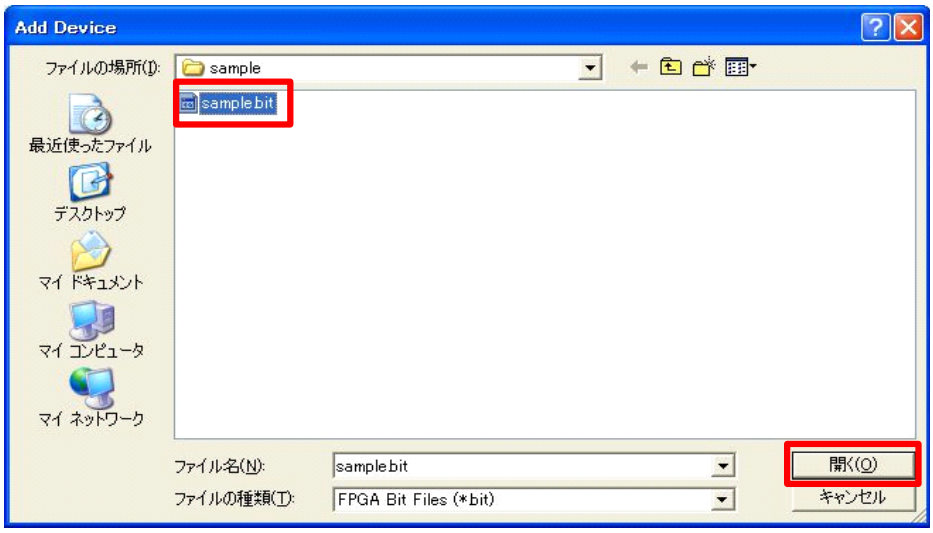


Figure 11-12 iMPACT Window - 6

9. Click **No**.

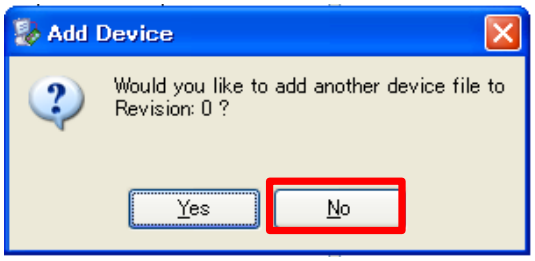


Figure 11-13 iMPACT Window - 7

10. Click **OK**.

Figure 11-14 iMPACT Window - 8

11. Doule click **Generate File**.

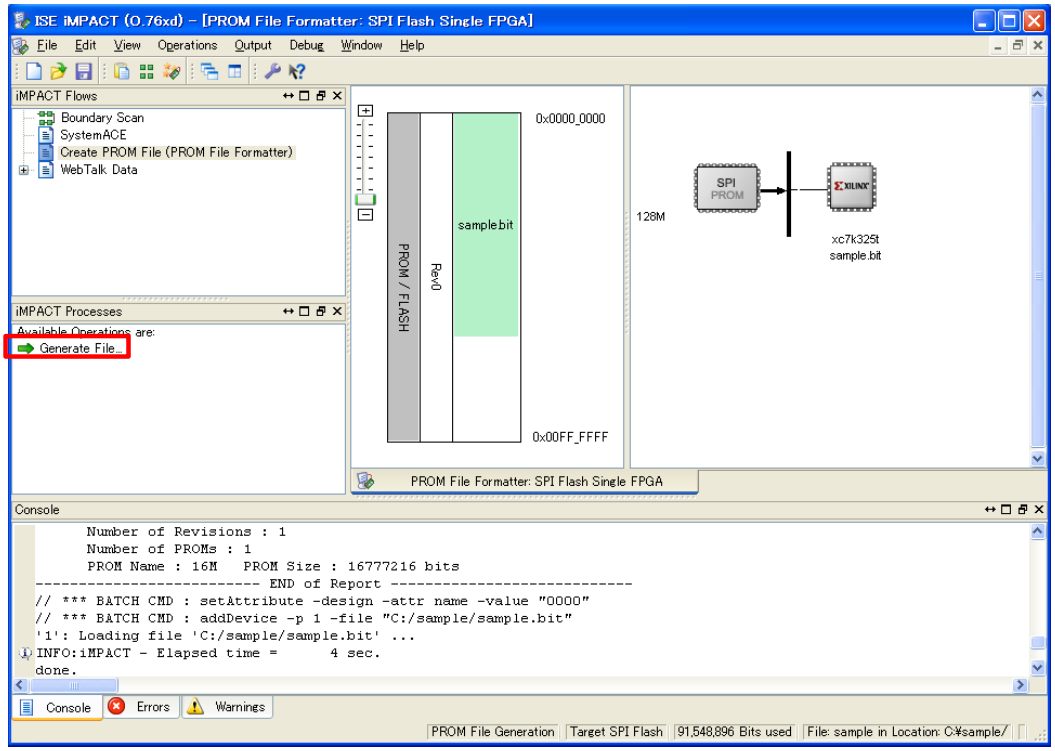


Figure 11-15 iMPACT Window - 9

12. When the configuration file is generated successfully, a **Generate Succeeded** message will appear.

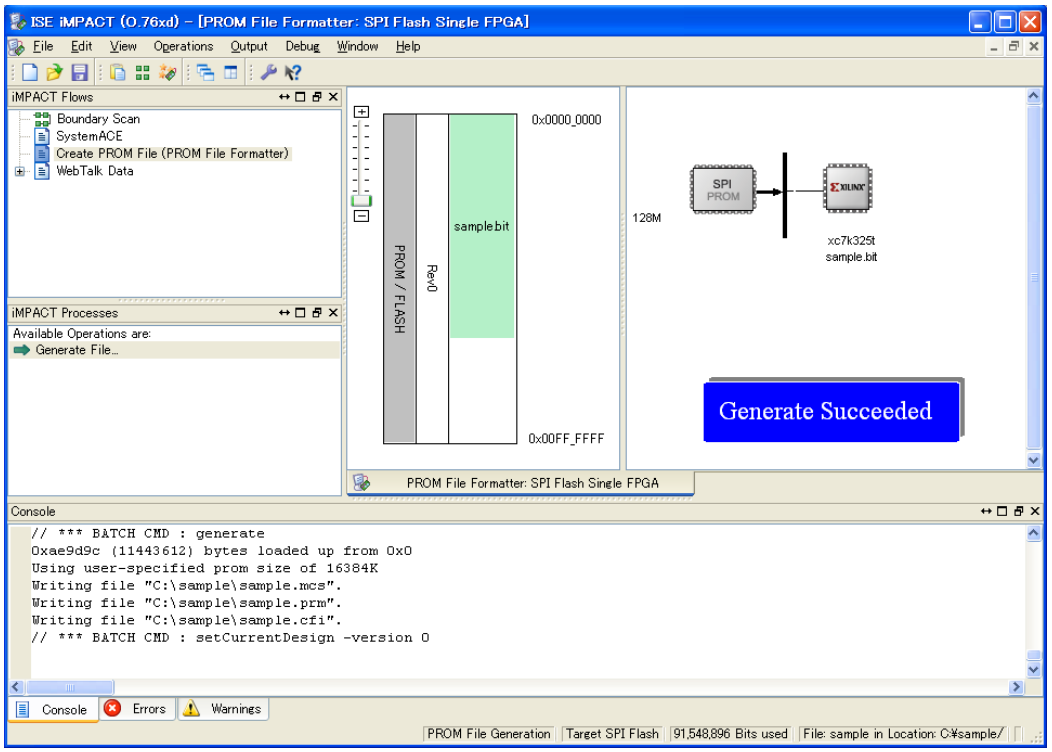


Figure 11-16 iMPACT Window – 10

11.5. Loading a Configuration File to Flash Memory

As shown in Figure 11-17, connect a Platform USB cable to the JTAG connector (CN27). Turn on the power switch of the board to run **iMPACT** and load a configuration file to the Flash memory.

Figure 11-17 Onboard JTAG Connector

1. Double click **Boundary Scan** and then click **InitializeChain** (indicated by an arrow).

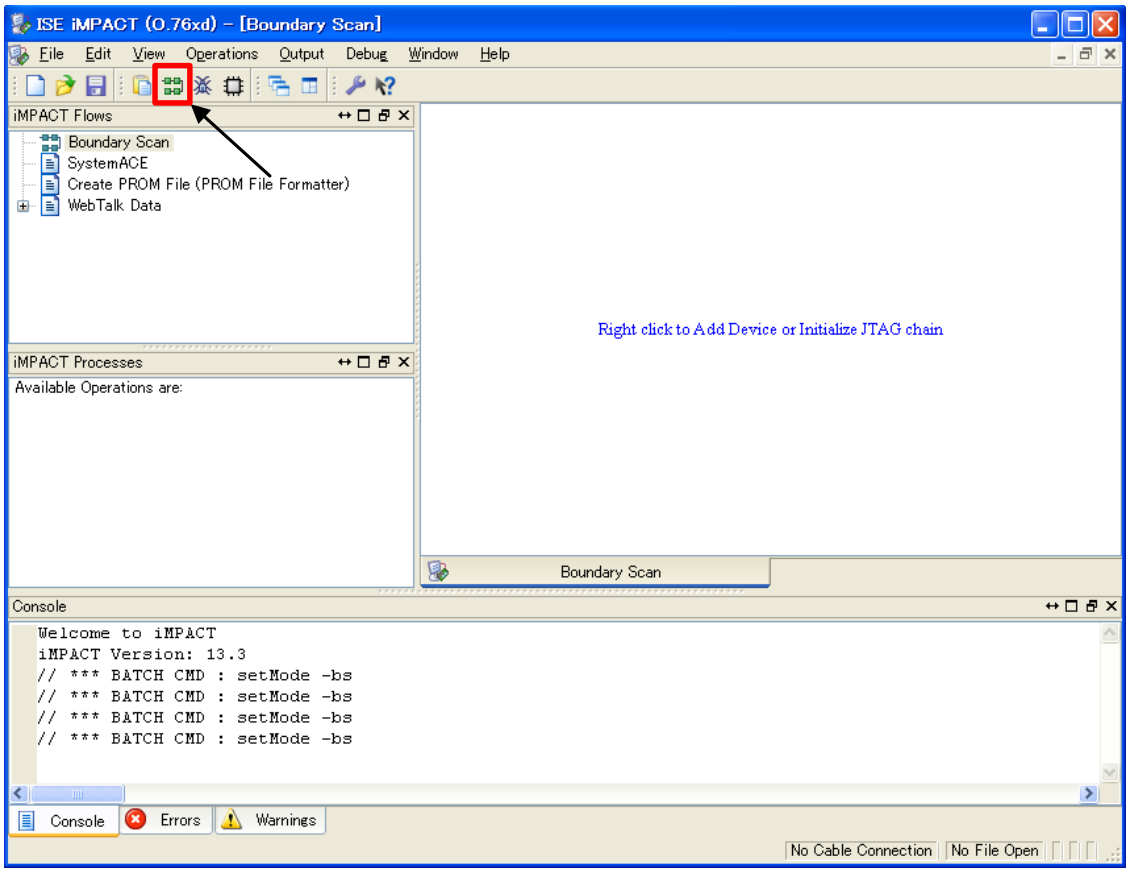


Figure 11-18 Loading a Configuration File to Device (1)

2. A bit/jed file configuration window will appear. Cancel it.
   Select **FPGA** and then right click to select **Add SPI/BPI Flash…**.

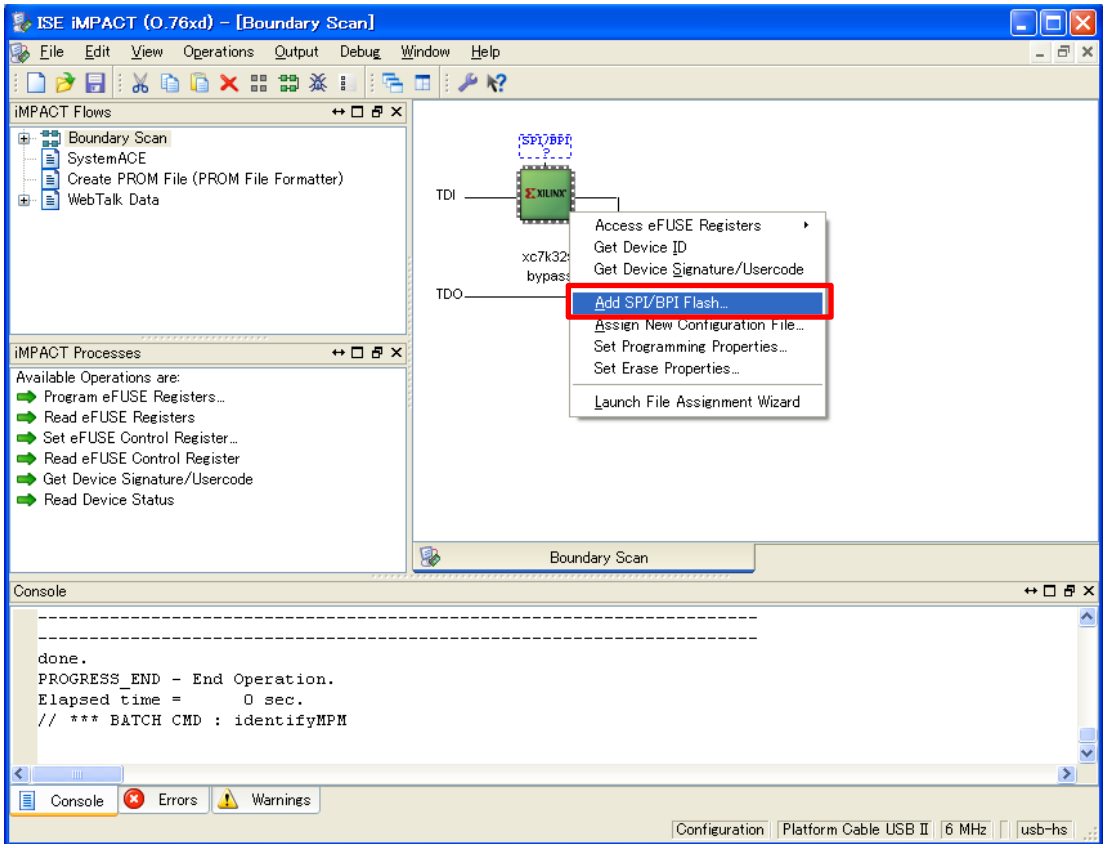


Figure 11-19 Loading a Configuration File to Device (2)

3. Choose a configuration file (xxx.mcs) you want to load to Flash Memory.

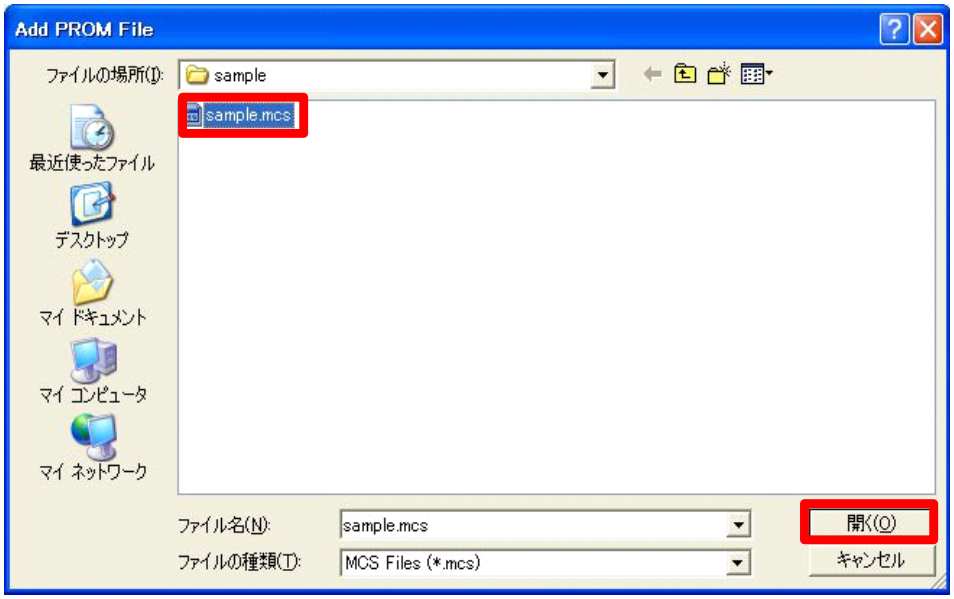


Figure 11-20 Loading a Configuration File to Device (3)

4. Select the onboard Flash of **N25Q128 1.8/3.3V**, set Data Width to **4**, and click **OK**.

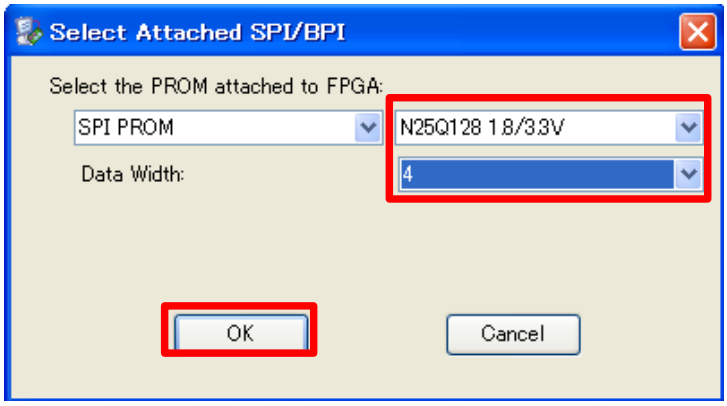


Figure 11-21 Loading a Configuration File to Device (4)

5. Double click **Program** on the iMPACT Processes window.

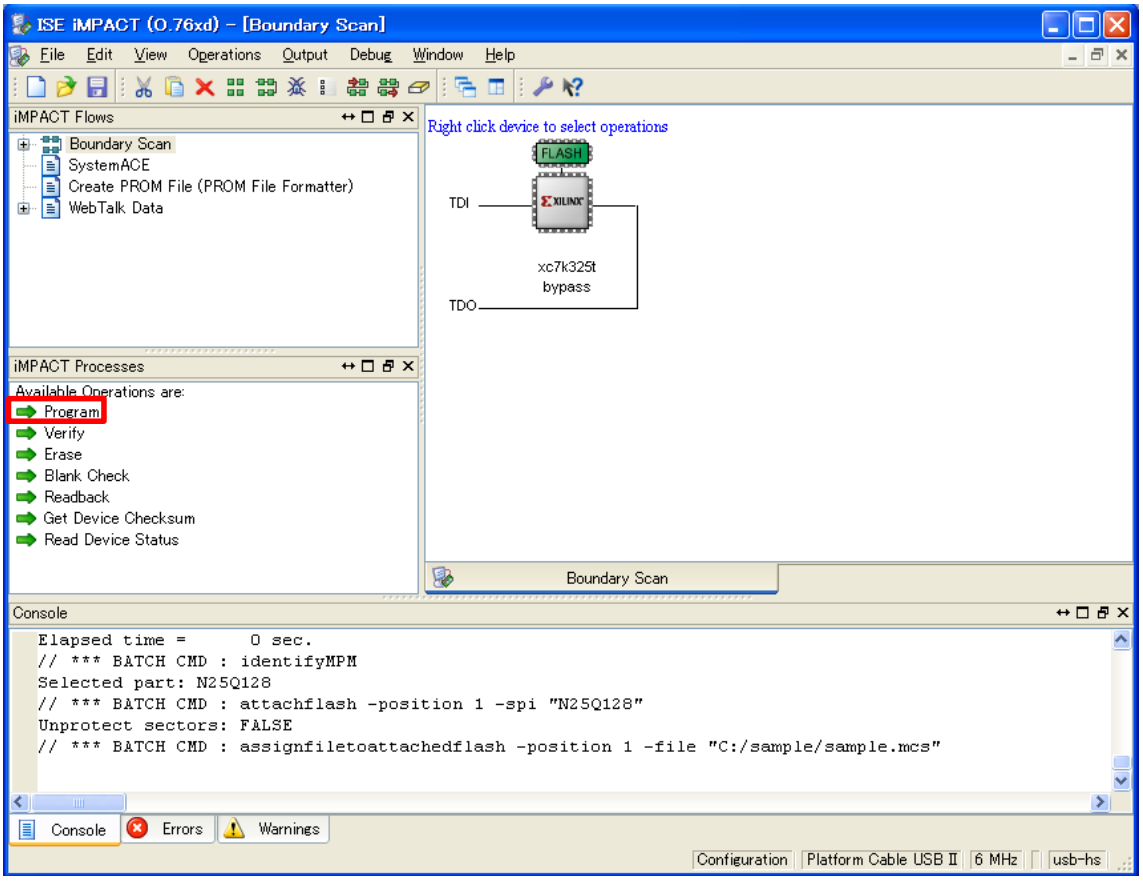


Figure 11-22 Loading a Configuration File to Device (5)

6. Click **OK**.

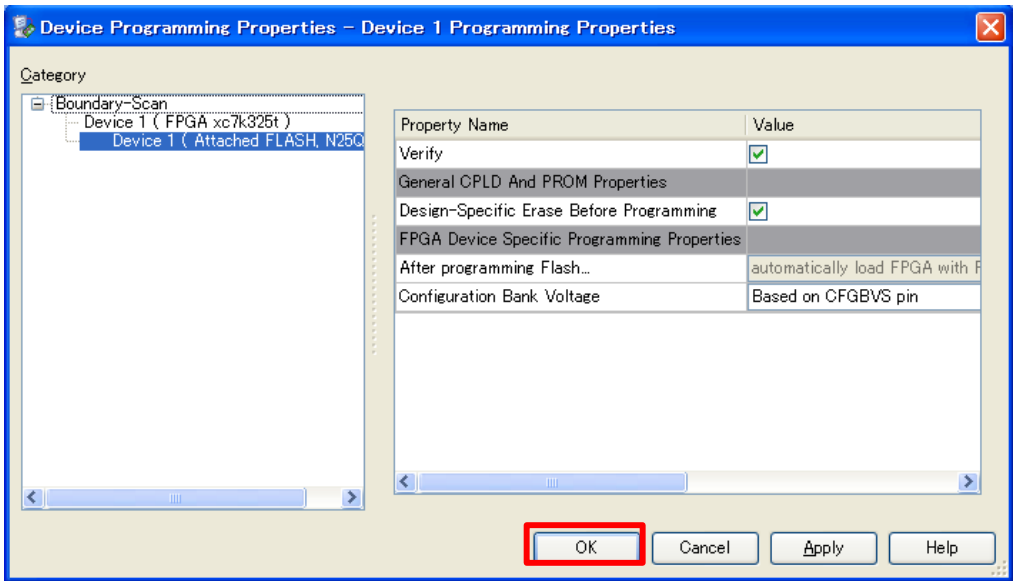


Figure 11-23 Loading a Configuration File to Device (6)

7. A load operation to Flash Memory will start.

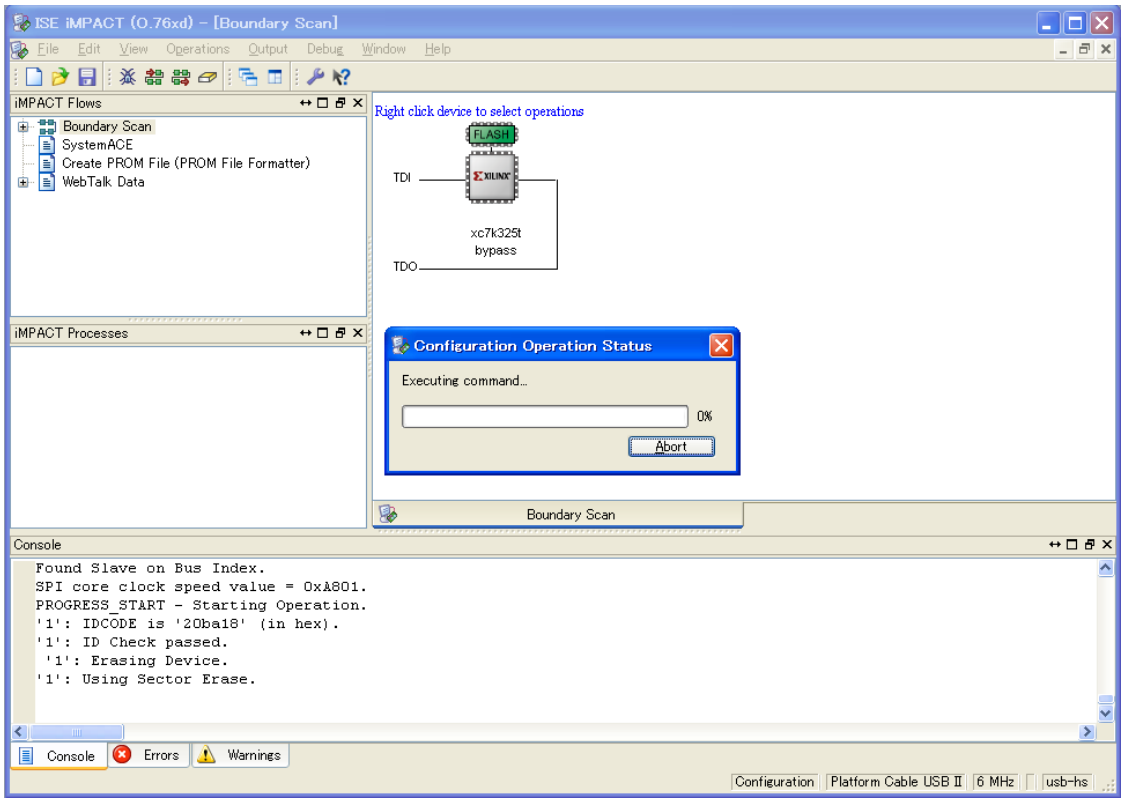


Figure 11-24 Loading a Configuration File to Device (7)

8. When the load operation is completed successfully, a **Program Succeeded** message will appear.

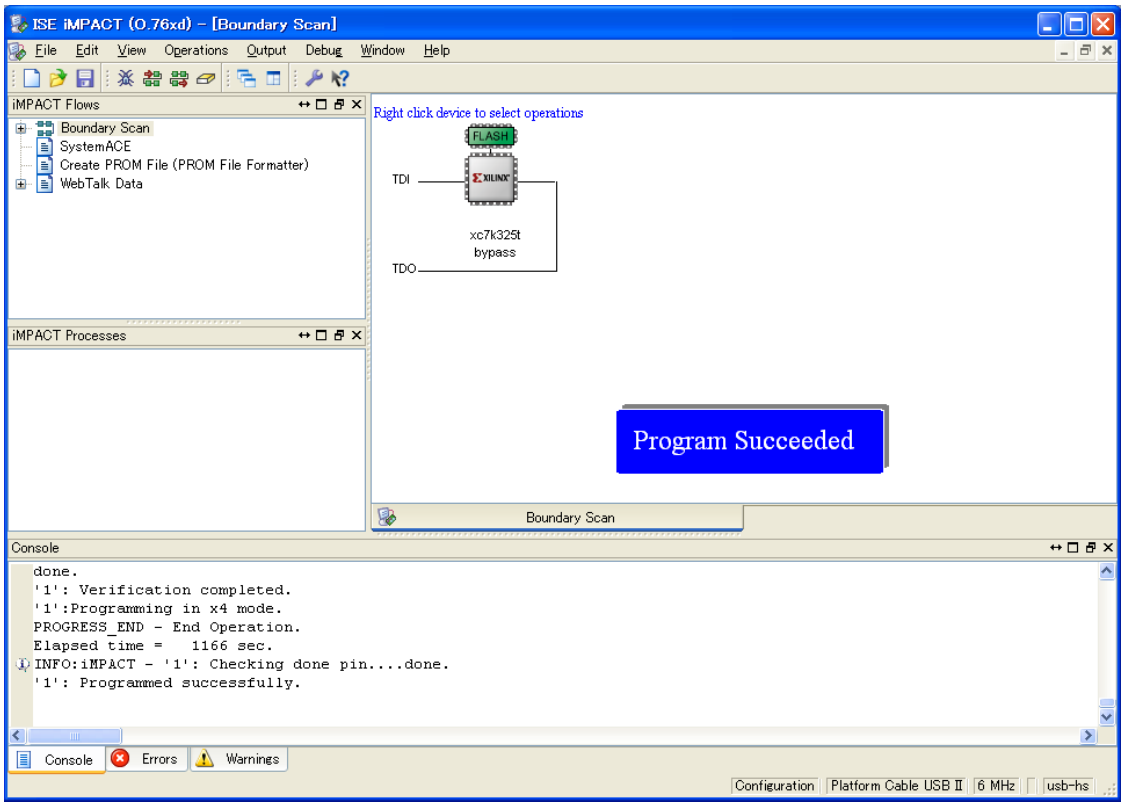


Figure 11-25 Loading a Configuration File to Device (8)

9. With the data loaded to Flash Memory, FPGA is configured using a QSPI. This configuration task can be performed either by turning the onboard power swich on or pressing down the reconfiguration switch (SW19) that is shown in Figure 11-26.

Figure 11-26 Onboard Reconfiguration Switch

10. LED58 and LED59 indicate the operational status of the FPGA configuration.
    LED58 (green): Configuration completed successfully
    LED59 (red): Configuration is in progress or an error has occurred

Figure 11-27 Configuration Status

12. QTH-FMC Conversion Board

The TB-7V-2000T-LSI board comes with a QTH-FMC conversion board that is used to connect the FMC Card to the QTH Connector.
This conversion board allows the FMC Card to be connected to the TB-7V-2000T-LSI board.

*This FMC Card allows for LPC only. FMCs with HPC connectors that use high speed I/Os on FPGA cannot be used (TB-FMCH-HDMI2 can be used).

* I/O voltage of 2.5V or 3.3V is not supported on Virtex-7. Only 1.8V FMC Card is allowed to connect to the QTH connectors (CN20, CN21 and CN22) on Virtex-7.

*I/O voltage of up to 3.3V is supported on Kintex-7. So, up to 3.3V FMC Card is allowed to connect to the QTH connectors (CN30 and CN31) on Kintex-7.

Figure 12-1 QTH-FMC Conversion Boards

Two types of conversion boards, “L” and “R”, are available. To connect the conversion boards to two QTH connectors (CN21/CN22 or CN31/CN32) that are located side by side, follow the following rules.

- CN21/CN31: “R-type” conversion board (TB-OP-FMCL-R)
- CN22/CN32: “L-type” conversion board (TB-OP-FMCL-L)
- CN20 allows for both “L” and “R”. To use USB JTAG (CN18), be sure to use “R-type” conversion board (TB-OP-FMCL-R).

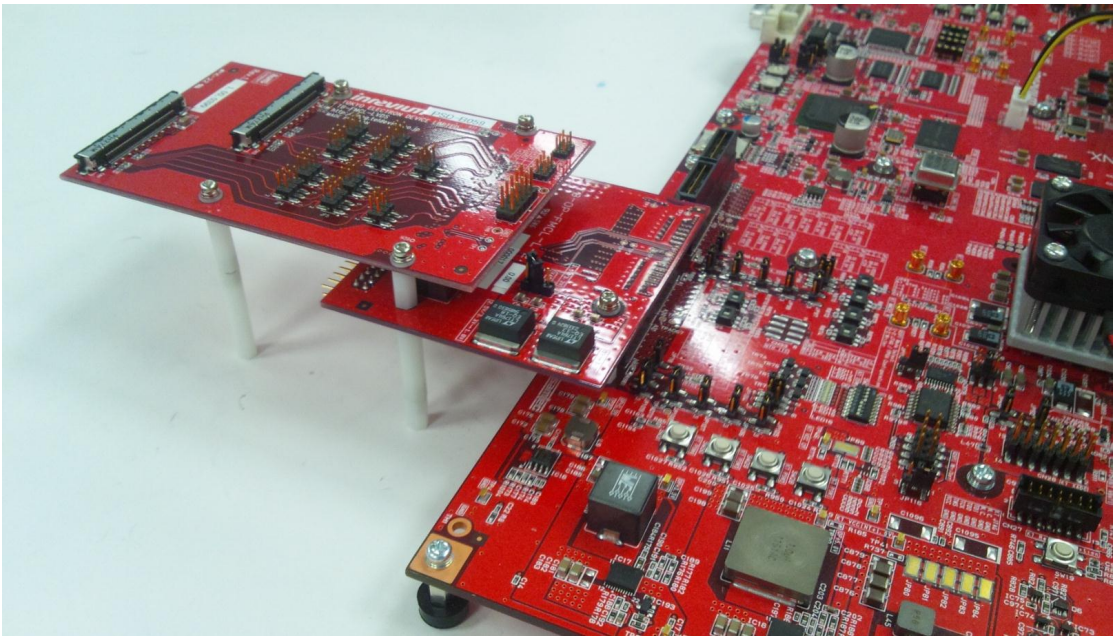


Figure 12-2 An Example of QTH-FMC Connection

12.1. Power Supply to FMC Card

For supplying power to the FMC Card, it is needed to set the jumpers on TB-7V-2000T-LSI in accordance with the following procedure.

12.1.1. 12V Power Supply

It is needed to supply +12V to the C35 and C37 pins on the FMC connector.
To enable this, short the jumper 5-6 for B54 swtching pin on the QTH connector that is connected to the QTH-FMC conversion board.

Table 12-1 Jumpers (Ref No.) for B54 Switching Pin on QTH Connector

QTH Connector	JP Ref.No.
Virtex-7 CN20	JP56
Virtex-7 CN21	JP64
Virtex-7 CN22	JP72
Kintex-7 CN31	JP96
Kintex-7 CN32	JP104

Table 12-2 Setting B54 Pin on QTH Connector to +12V

Supply	JP
+12V	5-6
OP+5V	3-4
FPGA Signal	1-2

12.1.2. 3.3V Power Supply

3.3V required by the FMC connector is generated on the conversion board using 5V that is supplied from the TB-7V-2000T-LSI board and supplied to each C39, D32, D36, D38 and D40 pin on the FMC connector.

In case of using a QTH-FMC conversion board, as the B55, B56 and B57 pins on the QTH connector are used for 5V power supply, short the jumper 2-3 for all B55, B56 and B57 switching pins on the QTH connector that is mounted on the TB-7V-2000T-LSI board so as to enable 5V power supply.

Table 12-3 Jumpers (Ref No.) for B55/B56/B57 Switching Pins on QTH Connector

QTH Connector	B55 JP	B56 JP	B57 JP
Virtex-7 CN20	JP57	JP58	JP59
Virtex-7 CN21	JP65	JP66	JP67
Virtex-7 CN22	JP73	JP74	JP75
Kintex-7 CN31	JP97	JP98	JP99
Kintex-7 CN32	JP105	JP106	JP107

Table 12-4 Setting All B55/B56/B57 Pins on QTH Connector to OP+5V

Supply	JP
OP+5V	2-3
FPGA Signal	1-2

*All B55, B56 and B57 signals are connected on the QTH-FMC conversion board. So, be sure to short the jumper 2-3 for all B55, B56 and B57 pins on the QTH connector.

12.1.3. VADJ Power Supply

Power supply to VADJ on the FMC Card is 3.3V/2.5V/1.8V selectable.

Tables 12-5 through 12-9 show the jumper settings on the TB-7V-2000T-LSI board and the QTH-FMC conversion board.

Table 12-5 JP Settings in Case of Using QTH1 (CN20)

Board	JP	VADJ=3.3V	VADJ=2.5V	VADJ=1.8V
TB-7V-2000T-LSI	JP61	2-3	2-3	2-3
	JP62	2-3	1-2	2-3
QTH-FMC Board	JP1	1-2	1-2	2-3

Table 12-6 JP Settings in Case of Using QTH2 (CN21)

Board	JP	VADJ=3.3V	VADJ=2.5V	VADJ=1.8V
TB-7V-2000T-LSI	JP69	2-3	2-3	2-3
	JP63	2-3	1-2	2-3
QTH-FMC Board	JP1	1-2	1-2	2-3

Table 12-7 JP Settings in Case of Using QTH3 (CN22)

Board	JP	VADJ=3.3V	VADJ=2.5V	VADJ=1.8V
TB-7V-2000T-LSI	JP77	2-3	2-3	2-3
	JP70	2-3	1-2	2-3
QTH-FMC Board	JP1	1-2	1-2	2-3

Table 12-8 JP Settings in Case of Using QTH4 (CN31)

Board	JP	VADJ=3.3V	VADJ=2.5V	VADJ=1.8V
TB-7V-2000T-LSI	JP101	2-3	2-3	2-3
	JP71	2-3	1-2	2-3
QTH-FMC Board	JP1	1-2	1-2	2-3

Table 12-9 JP Settings in Case of Using QTH5 (CN32)

Board	JP	VADJ=3.3V	VADJ=2.5V	VADJ=1.8V
TB-7V-2000T-LSI	JP109	2-3	2-3	2-3
	JP78	2-3	1-2	2-3
QTH-FMC Board	JP1	1-2	1-2	2-3

12.2. How to Attach Spacers

Figure 12-3 illustrates how to attach the spacers for the QTH-FMC conversion board and the FMC Card.

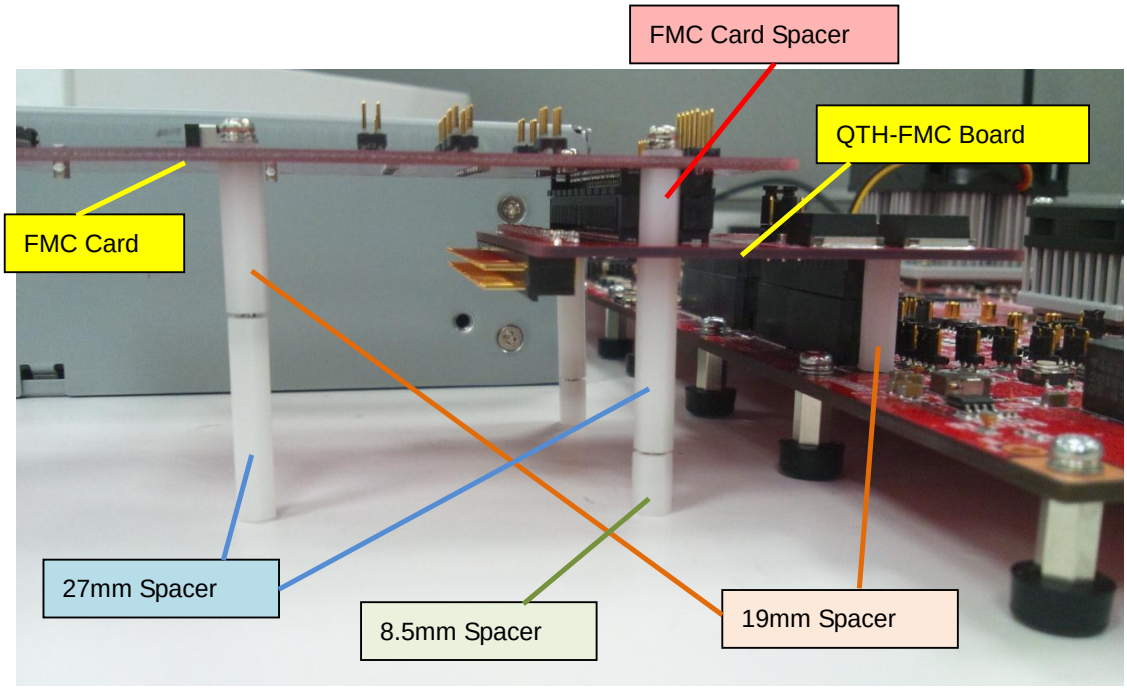


Figure 12-3 How to Attach Spacers

Use the accompanying long screws (10-mm type) to fix the TB-7V-2000T-LSI board and the QTH-FMC board with these spacers.

13. Default Switch Settings

Figure 13-1 illustrates the default switch settings indicated by blue box.

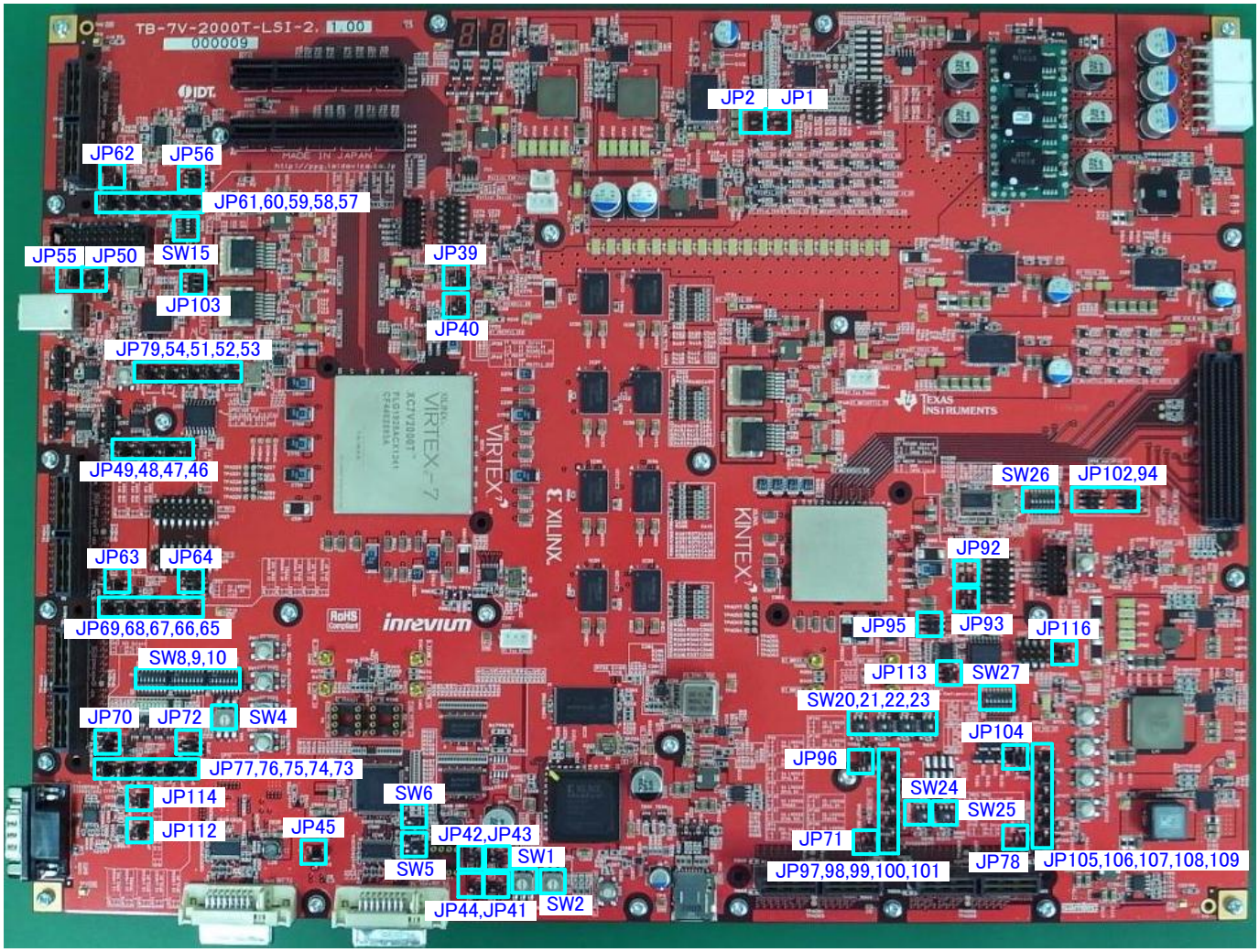


Figure 13-1 Default Switch Settings on Component Side of the Board

Table 13-1 Default Settings

No.	Silk No.	Initial Setting	Function
1	SW1	1	MicroSD Card=>FPGA(Virtex-7) Direct Transfer Mode
2	SW2	0	MicroSD Card Area Setting (Area Selection 0)
3	SW4	0	Virtex-7 User Rotary Switch
4	SW5	2-1, 5-4	DDC Switching (**DVI_Tx** / EEPROM)
5	SW6	2-3	Hot-Plug Switching (OP+5V / **DVI_Tx**)
6	SW8	ALL OFF	Virtex-7 User DIP Switch
7	SW9	ALL OFF	Virtex-7 User DIP Switch
8	SW10	ALL OFF	Virtex-7 User DIP Switch
9	SW20,21	2-3, 5-6	QTH4 Connector FPGA/IIC Switching (**FPGA** / IIC)

No.	Silk No.	Initial Setting	Function
10	SW22,23	2-3, 5-6	QTH5 Connector FPGA/IIC Switching (**FPGA** / IIC)
11	SW24,25	2-1, 5-4	IIC Power Supply Switching (3.3V / **non-supply**)
12	SW26	ALL OFF	Virtex-7 MGT Reference Clock Select Switch
13	SW27	ALL OFF	Kintex-7 User DIP Switch
14	JP1	OPEN	PMBUS_ADDR0 Setting (GND_90.9K,1% / GND_41.2K,1% / **non-supply**)
15	JP2	OPEN	PMBUS_ADDR1 Setting (GND_90.9K,1% / GND_41.2K,1% / **non-supply**)
16	JP39	1-2	Virtex-7 VCCADC Voltage Setting (**V7_VCC+1.8V** / V7_VCCADC+1.8V / non-supply)
17	JP40	1-2	Virtex-7 VREFP Voltage Setting (**V7_XADC_AGND** / V7_VREFP+1.25V / non-supply)
18	JP41	2-3	TFP401PZP_DFO Setting (V7_VCC+3.3V / **GND**)
19	JP42	2-3	TFP401PZP_ST Setting (V7_VCC+3.3V / **GND**)
20	JP43	2-3	TFP401PZP_/STAG Setting (V7_VCC+3.3V / **GND**)
21	JP44	2-3	TFP401PZP_OCK_INV Setting (V7_VCC+3.3V / **GND**)
22	JP45	2-3	DVI_Tx Connector +5V supply (OP+5.0V / **DVI+5V**)
23	JP46,47,48,49	1-2	USB SPI/UART Switching (**SPI** / UART)
24	JP50	OPEN	USB RTCK Switching (TCK / GND / **non-supply**)
25	JP51	1-2	USB PMODE1 Setting (**High** / Low / non-supply)
26	JP52	OPEN	USB PMODE2 Setting (High / Low / **non-supply**)
27	JP53	2-3	USB PMODE3 Setting (High / **Low** / non-supply)
28	JP54	2-3	USB CLK Setting (XTAL / **CLKIN**)
29	JP55	2-3	USB OTG ID Setting (GND / **non-supply**)
30	JP56	1-2	QTH1_B54pin Setting (**non-supply** / OP+5.0V / +12V)
31	JP57	1-2	QTH1_B55pin Setting (**non-supply** / OP+5.0V)
32	JP58	1-2	QTH1_B56pin Setting (**non-supply** / OP+5.0V)
33	JP59	1-2	QTH1_B57pin Setting (**non-supply** / OP+5.0V)
34	JP60	1-2	QTH1_B58pin Setting (**non-supply** / TPAD38)
35	JP61	1-2	QTH1_B59pin Setting (**non-supply** / QTH1_VCC)
36	JP62	1-2	QTH1_B60pin Setting (**OP+2.5V** / OP+3.3V)
37	JP63	1-2	QTH2_B60pin Setting (**OP+2.5V** / OP+3.3V)
38	JP64	1-2	QTH2_B54pin Setting (**non-supply** / OP+5.0V / +12V)
39	JP65	1-2	QTH2_B55pin Setting (**non-supply** / OP+5.0V)
40	JP66	1-2	QTH2_B56pin Setting (**non-supply** / OP+5.0V)
41	JP67	1-2	QTH2_B57pin Setting (**non-supply** / OP+5.0V)
42	JP68	1-2	QTH2_B58pin Setting (**non-supply** / TPAD43)
43	JP69	1-2	QTH2_B59pin Setting (**non-supply** / QTH2_VCC)
44	JP70	1-2	QTH3_B60pin Setting (**OP+2.5V** / OP+3.3V)
45	JP71	1-2	QTH4_B60pin Setting (**OP+2.5V** / OP+3.3V)
46	JP72	1-2	QTH3_B54pin Setting (**non-supply** / OP+5.0V / +12V)
47	JP73	1-2	QTH3_B55pin Setting (**non-supply** / OP+5.0V)
48	JP74	1-2	QTH3_B56pin Setting (**non-supply** / OP+5.0V)
49	JP75	1-2	QTH3_B57pin Setting (**non-supply** / OP+5.0V)
50	JP76	1-2	QTH3_B58pin Setting (**non-supply** / TPAD48)
51	JP77	1-2	QTH3_B59pin Setting (**non-supply** / QTH3_VCC)
52	JP78	1-2	QTH5_B60pin Setting (**OP+2.5V** / OP+3.3V)

No.	Silk No.	Initial Setting	Function
53	JP79	1-2	USB RESET (**non-supply** / GND)
54	JP92	1-2	Kintex-7 VCCADC Setting (**K7_VCC+1.8V** / CN28 9pin / non-supply)
55	JP93	1-2	Kintex-7 VREFP Setting (**K7_XADC_AGND** / CN28 11pin / non-supply)
56	JP94,102	1-2	Kintex-7 QTH4 VCCO Setting (**K7_VCC+1.8V** / K7_VCC+2.5V / K7_VCC+3.3V)
57	JP95	1-2	Kintex-7 QTH5 VCCO Setting (**K7_VCC+1.8V** / K7_VCC+2.5V / K7_VCC+3.3V)
58	JP96	1-2	QTH4_B54pin Setting (**non-supply** / OP+5.0V / +12V)
59	JP97	1-2	QTH4_B55pin Setting (**non-supply** / OP+5.0V)
60	JP98	1-2	QTH4_B56pin Setting (**non-supply** / OP+5.0V)
61	JP99	1-2	QTH4_B57pin Setting (**non-supply** / OP+5.0V)
62	JP100	1-2	QTH4_B58pin Setting (**non-supply** / TPAD65)
63	JP101	1-2	QTH4_B59pin Setting (**non-supply** / QTH4_VCC)
64	JP103	OPEN	USB I2C Setting (USB_I2C_SCL / USB_I2C_SDA / **non-supply**)
65	JP104	1-2	QTH5_B54pin Setting (**non-supply** / OP+5.0V / +12V)
66	JP105	1-2	QTH5_B55pin Setting (**non-supply** / OP+5.0V)
67	JP106	1-2	QTH5_B56pin Setting (**non-supply** / OP+5.0V)
68	JP107	1-2	QTH5_B57pin Setting (**non-supply** / OP+5.0V)
69	JP108	1-2	QTH5_B58pin Setting (**non-supply** / TPAD70)
70	JP109	1-2	QTH5_B59pin Setting (**non-supply** / QTH5_VCC)
71	JP112	2-3	Virtex-7 UART Setting (ON / **OFF**)
72	JP113	1-2	QSPI Mode Setting (**JTAG FPGA Configuration** / Writer)
73	JP114	2-3	Kintex-7 UART Setting (ON / **OFF**)
74	JP116	1-2	QSPI Writer CN Power Supply (**K7_VCC_CF** / K7_VCC+3.3V)

The bold/underlined characters in the Function field are default settings.

Two or more jumper settings should be set to the same position.

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