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Revisions

Rev	Description	Date	Approved
X1	Initial Draft	08/20/12	L. PUEBLA
A	Prototype Release	08/28/12	L. PUEBLA
B	Production Release	11/21/12	L. PUEBLA
C	Respin Release	01/21/13	L. PUEBLA
C1	D9 pop fix	01/29/13	L. PUEBLA

FRDM-K20D50M

freescale

Automotive, Industrial & Multi-Market Solutions Group
6501 William Cannon Drive West Austin, TX 78735-8598

ICAP Classification: FCP: FIUO: PUBI: X

Designer: RAFAEL DEL REY	Drawing Title: FRDM-K20D50M		
Drawn by: RAFAEL DEL REY	Page Title: TITLE PAGE		
Approved: LUIS PUEBLA	Size C	Document Number SCH-27720 | PDF: SPF-27720	Rev C1
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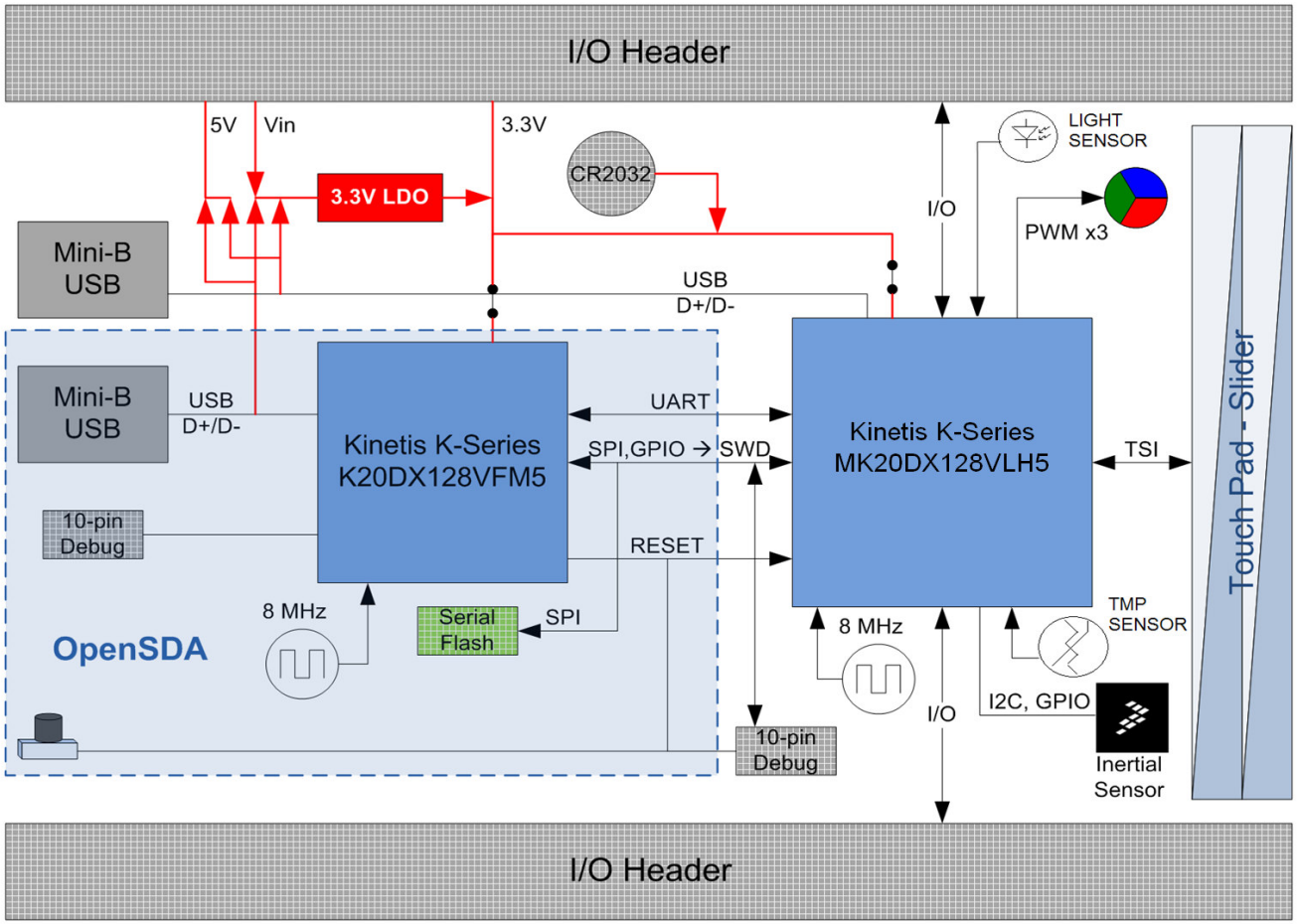
1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/8 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



Hashed blocks indicate optional items that will not be populated by default

freescale

ICAP Classification:	FCP: ___	FIUO:	PUBI: X
Drawing Title: FRDM-K20D50M			
Page Title: BLOCK DIAGRAM			
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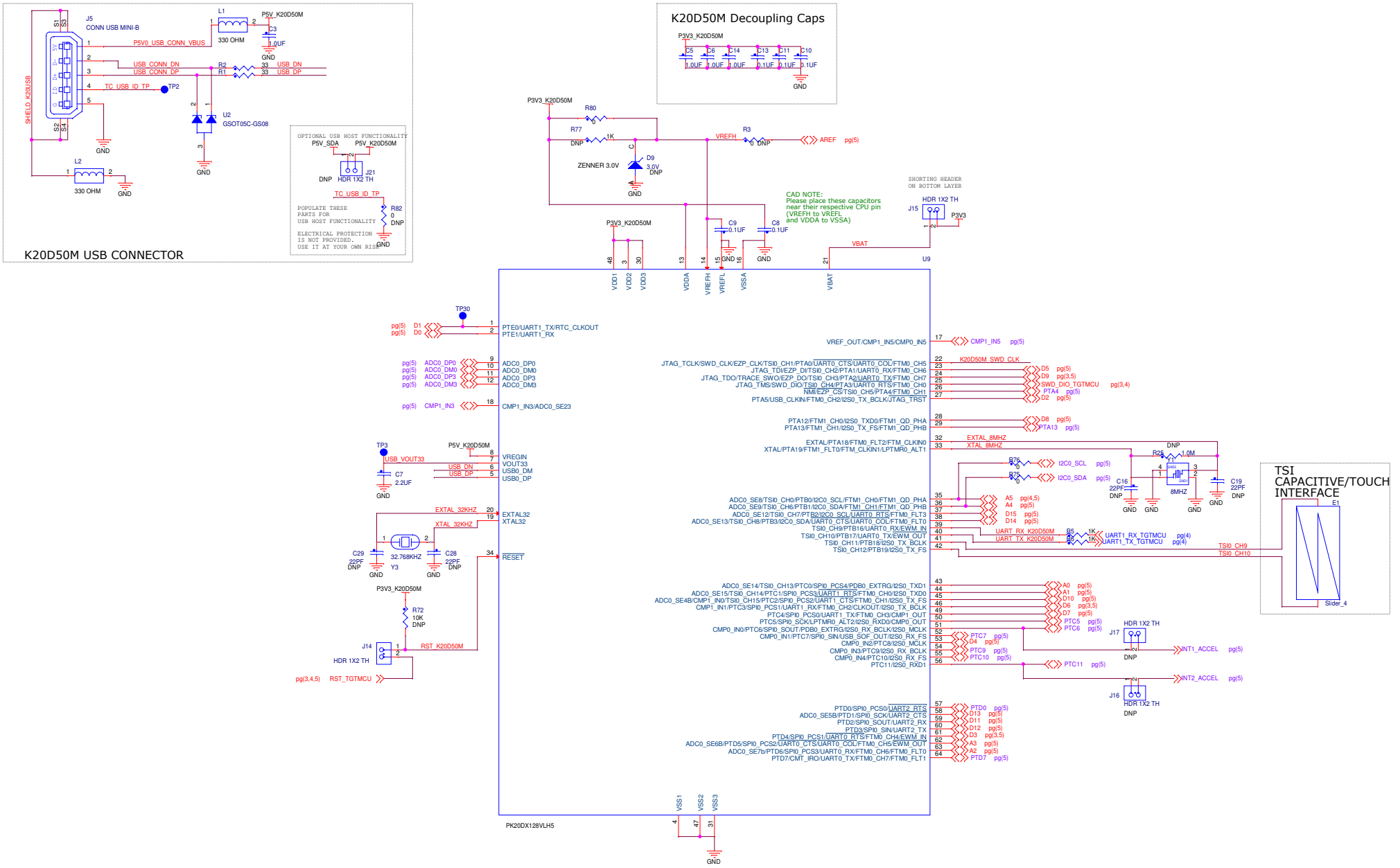

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ICAP Classification:	FCP: ___	FIUO:	PUBI: X

Drawing Title: **FRDM-K20D50M**

Page Title: **K20D MCU**

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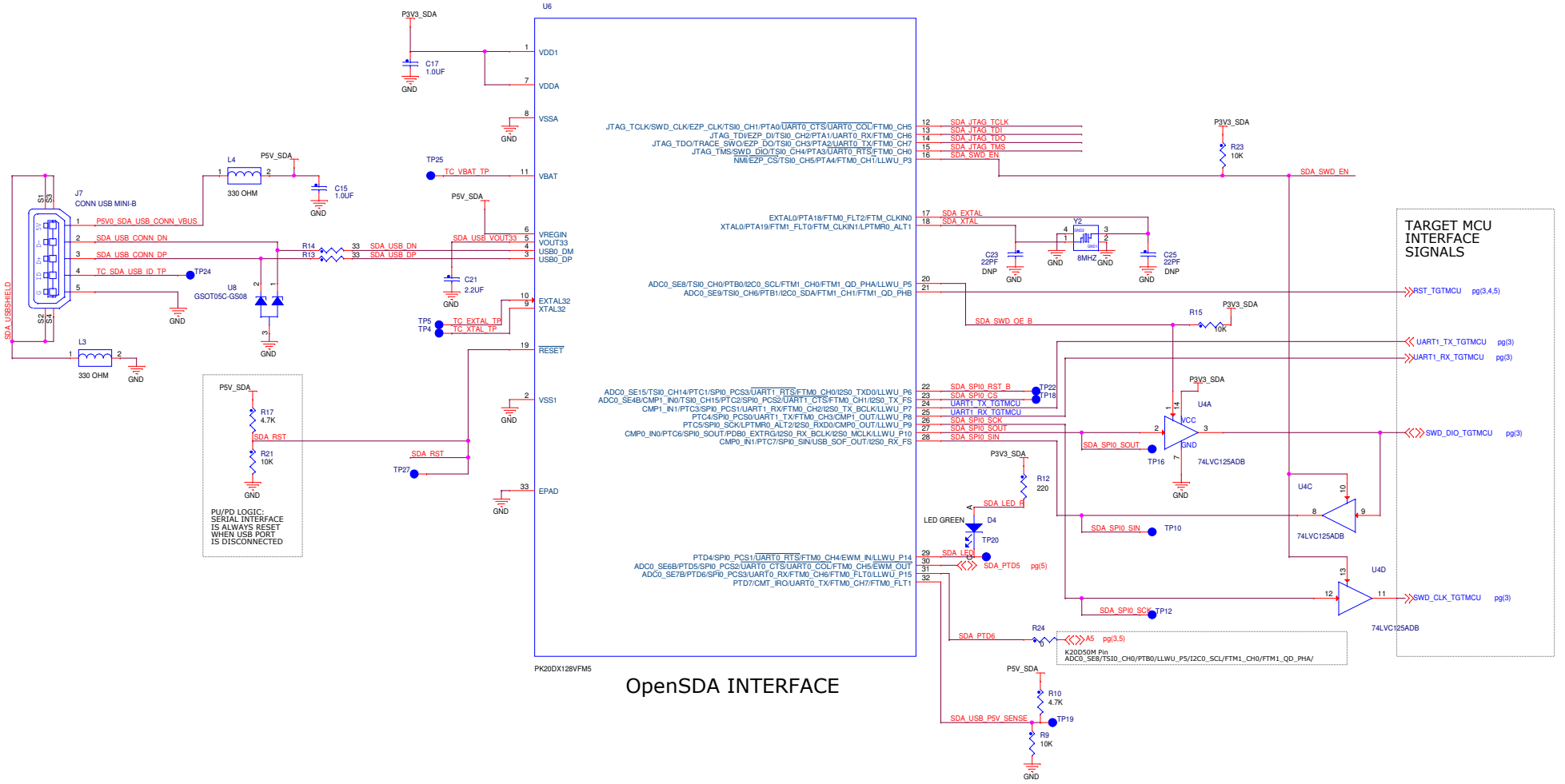
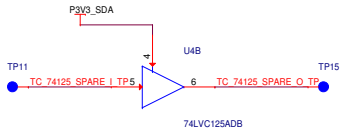
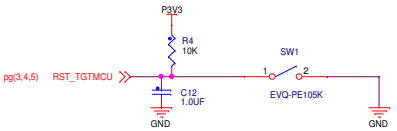


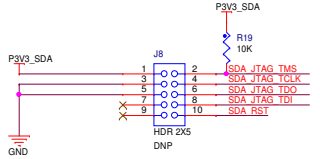
SPARE 74HC125 buffer



TARGET RESET AND BOOTLOADER PUSH BUTTON



OpenSDA INTERFACE JTAG CONNECTOR



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ICAP Classification:	FCP: ___	FIUO:	PUBI: X
Drawing Title:	FRDM-K20D50M		
Page Title:	OpenSDA interface		
Size: C	Document Number: SCH-27720 | PDF: SPF-27720		Rev: C1
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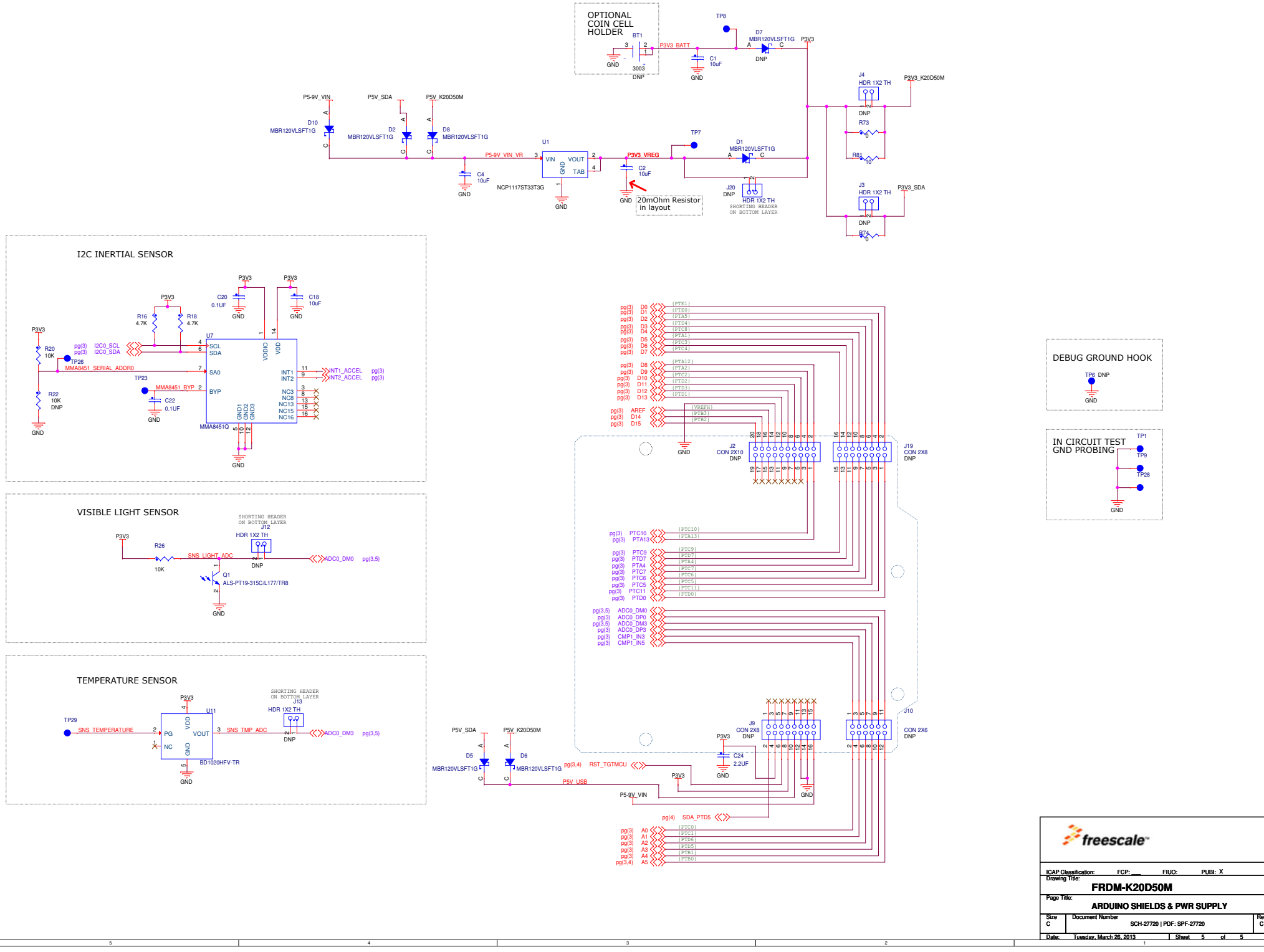

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ICAP Classification:	FCP: ___	FIUO:	PUBI: X

Drawing Title: **FRDM-K20D50M**

Page Title: **ARDUINO SHIELDS & PWR SUPPLY**

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