CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX850 Communications Controller

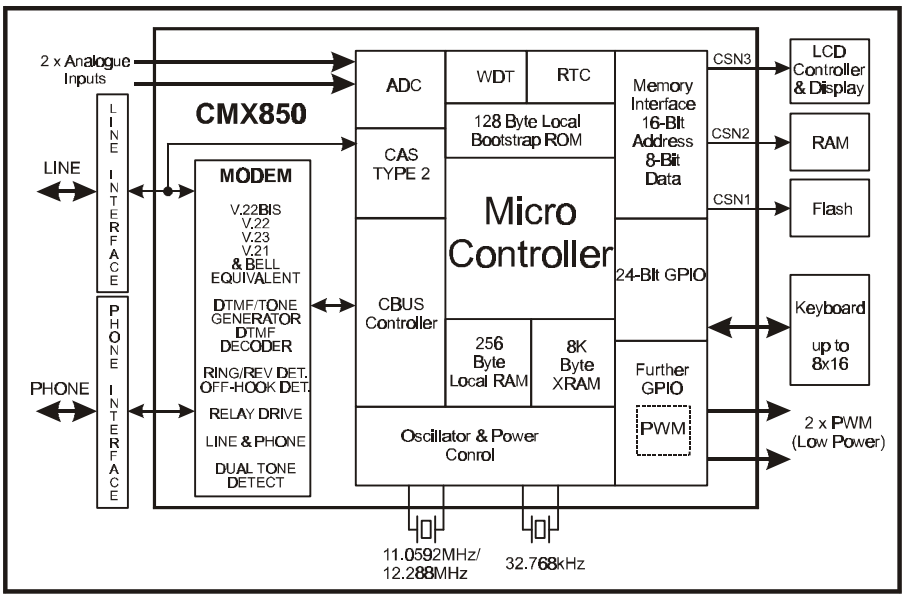
D/850/6 December 2003 Provisional Issue

Features

- 8051 µC with internal 8K XRAM and up to 35 GPIO
- 64K address, bank switchable to many Mbytes
- Interfaces for external RAM, LCD controller, etc.
- V.22bis, V.22, V.23, V.21 (and Bell) integral modem
- DTMF/Tones transmit and receive
- Line and Phone differential amplifiers
- Dual clocks with separate Xtals
- CLI/CIDCW Tones detection and generation
- Line reversal / Ring detection
- Off-hook detector
- Low power operation
- Advanced power management features
- Watchdog timer
- Real-time clock and alarm function
- Bootstrap ROM to reprogram external FLASH
- Customised memory versions available from CML
- Standard 8051 UART and timers
- 2 input 10-bit A to D converter
- Keyboard encoder (16 x 8 matrix max)
- 2 x low-power PWM outputs
- Programmable Tx DTMF twist
- Dedicated low-power FSK Rx for CLI
- Small footprint: 100-pin LQFP

Applications

- SMS and ADSI terminals
- Telemetry and meter reading systems
- Security systems
- Feature phones
- Routers
- EPOS terminals
- E-Mail and Internet appliances



1.1 Brief Description

This IC combines an extended function CMX860 with a full-function 8051 microcontroller (including UART and timer/counters), and has 8kbytes of RAM to form a powerful communications processor. Extended addressing offers page mode access to 4Mbytes of external FLASH memory. A 32.768kHz clock system allows a very low power interrupt-driven real time clock, watchdog timer and keyboard encoder. The device also includes a separate CAS tone detector and FSK receiver, two low power PWM outputs and a multiplexed 2-input 10-bit A to D converter with auto-convert and threshold detect. Advanced low power and sleep modes, including the ability to work from an on-chip RC oscillator, aid low battery consumption.

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1.2 Block Diagram

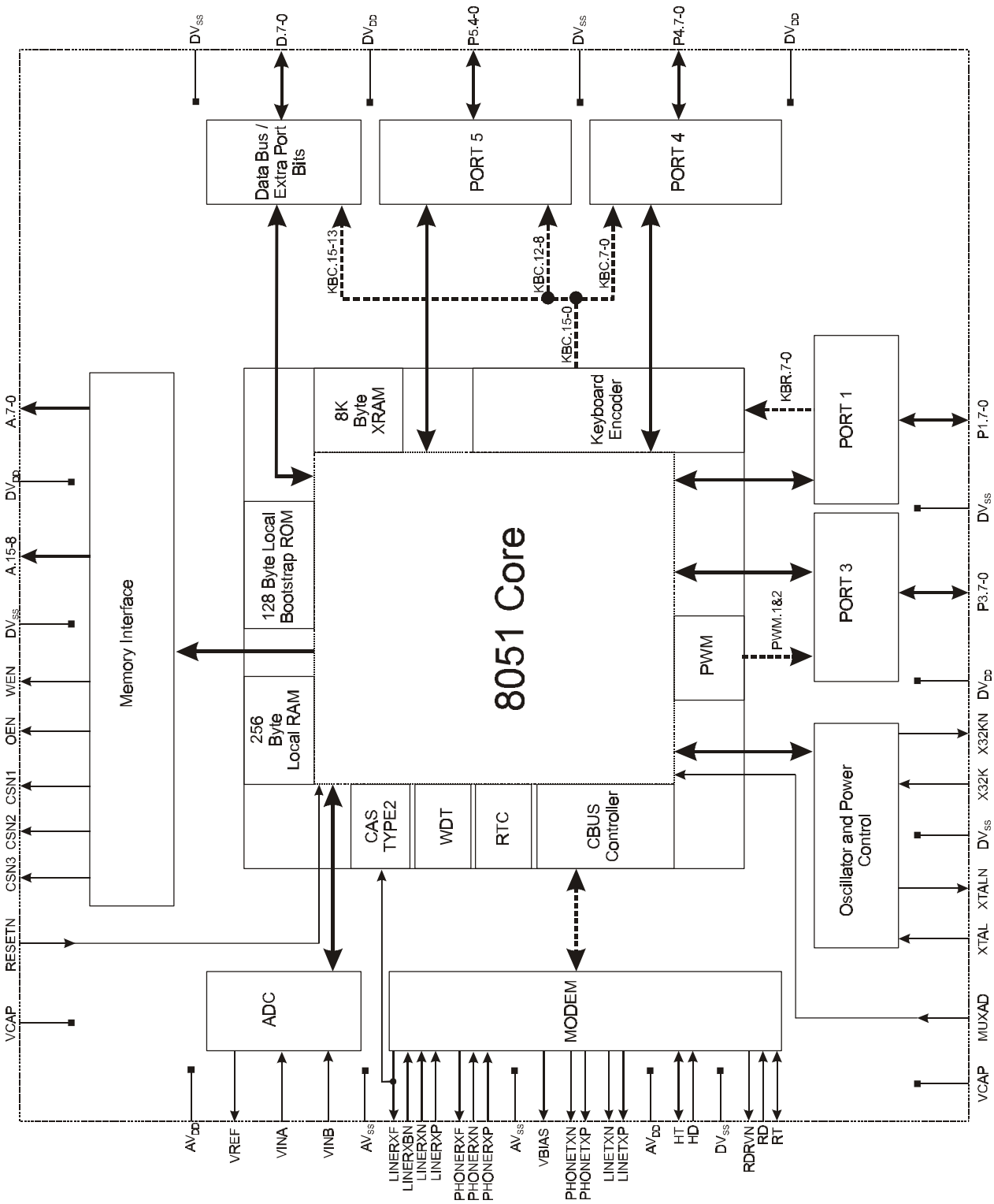


Figure 1 Block Diagram

1.3 Signal List

Package L8	Signal		Description
Pin No.	**Name**	**Type**	
1	VCAP	O/P	Decoupling capacitor
2	MUXAD	I/P	Multiplexed address/data bus select for external memory. Tie to DV_{SS} for non-multiplexed address/data. Tie to DV_{DD} for multiplexed address/data (frees up the D7-0 pins for alternative functions).
3	XTAL	I/P	The input to the 11.0592MHz or 12.288MHz oscillator circuit from the Xtal or external clock source.
4	XTALN	O/P	The output of the on-chip 11.0592MHz/12.288MHz Xtal oscillator circuit.
5	DV_{SS}	Power	The digital negative supply rail (ground).
6	X32K	I/P	The input to the 32.768kHz oscillator circuit from the Xtal.
7	X32KN	O/P	The output of the on-chip 32.768kHz Xtal oscillator circuit. Can also be used to output an internally derived 32.768kHz signal.
8	DV_{DD}	Power	The digital positive supply rail.
9	P3.0 (RXD)	BI	Port 3 bit 0. Alternative function is serial port (RS232) receive data.
10	P3.1 (TXD)	BI	Port 3 bit 1. Alternative function is serial port (RS232) transmit data.
11	P3.2 (INT0)	BI	Port 3 bit 2. Alternative function is Int0 interrupt input.
12	P3.3 (INT1)	BI	Port 3 bit 3. Alternative function is Int1 interrupt input.
13	P3.4 (T0)	BI	Port 3 bit 4. Alternative function is Timer 0 control input.
14	P3.5 (T1)	BI	Port 3 bit 5. Alternative function is Timer 1 control input.
15	P3.6 (PWM1)	BI	Port 3 bit 6. Alternative function is PWM 1 output.
16	P3.7 (PWM2)	BI	Port 3 bit 7. Alternative function is PWM 2 output.
17	DV_{SS}	Power	The digital negative supply rail (ground).
18	P1.0 (KBR.0)	BI	Port 1 bits 7-0. Alternative function is keyboard row input pins, bits 7-0.
19	P1.1 (KBR.1)	BI	
20	P1.2 (KBR.2)	BI	
21	P1.3 (KBR.3)	BI	
22	P1.4 (KBR.4)	BI	
23	P1.5 (KBR.5)	BI	
24	P1.6 (KBR.6)	BI	
25	P1.7 (KBR.7)	BI	
26	DV_{DD}	Power	The digital positive supply rail.
27	P4.0 (KBC.0)	BI	Port 4 bits 7-0. Alternative function is keyboard column drivers, bits 7-0. Unused column drivers remain as general-purpose port pins.
28	P4.1 (KBC.1)	BI	
29	P4.2 (KBC.2)	BI	
30	P4.3 (KBC.3)	BI	
31	P4.4 (KBC.4)	BI	
32	P4.5 (KBC.5)	BI	
33	P4.6 (KBC.6)	BI	
34	P4.7 (KBC.7)	BI	

Package L8	Signal		Description	
35	DV_{SS}	Power	The digital negative supply rail (ground).	
36	P5.0 (KBC.8)	BI	Port 5 bits 4-0. Alternative function is keyboard column drivers, bits 12-8. Unused column drivers remain as general-purpose port pins.	
37	P5.1 (KBC.9)	BI		
38	P5.2 (KBC.10)	BI		
39	P5.3 (KBC.11)	BI		
40	P5.4 (KBC.12)	BI		
41	DV_{DD}	Power	The digital positive supply rail.	
			With pin MUXAD tied to DV_{SS}:	*With pin MUXAD tied to DV_{DD}:*
42	D0 : *P5.5 (KBC.13)*	BI : *BI*	Bi-directional data bus for external memory.	Port 5 bits 7-5. Alternative function is keyboard column drivers, bits 15-13. Unused column drivers remain as general-purpose port pins.
43	D1 : *P5.6 (KBC.14)*	BI : *BI*		
44	D2 : *P5.7 (KBC.15)*	BI : *BI*		
45	D3 : *P0.0*	BI : *BI*		Port 0 bits 2-0.
46	D4 : *P0.1*	BI : *BI*		
47	D5 : *P0.2*	BI : *BI*		
48	D6 : *INT9*	BI : *I/P*		Super priority interrupt (active low). When configured as an interrupt, this pin should be fitted with a 100kΩ pullup resistor to DV_{DD} (not shown in Figure 2a), if driven by an open-drain driver.
49	D7 : *ALE*	BI : *O/P*		Address latch enable.
50	DV_{SS}	Power	The digital negative supply rail (ground).	
			With pin MUXAD tied to DV_{SS}:	*With pin MUXAD tied to DV_{DD}:*
51	A0 : *AD0*	O/P : *BI*	External memory interface address bus (LSB).	External memory interface multiplexed address (LSB) and data. While ALE is high, the LSB of the memory address is driven out. When ALE goes low, the pins change to a bi-directional data bus.
52	A1 : *AD1*	O/P : *BI*		
53	A2 : *AD2*	O/P : *BI*		
54	A3 : *AD3*	O/P : *BI*		
55	A4 : *AD4*	O/P : *BI*		
56	A5 : *AD5*	O/P : *BI*		
57	A6 : *AD6*	O/P : *BI*		
58	A7 : *AD7*	O/P : *BI*		
59	DV_{DD}	Power	The digital positive supply rail.	
60	A8	O/P	External memory interface address bus (MSB).	
61	A9	O/P		
62	A10	O/P		
63	A11	O/P		
64	A12	O/P		
65	A13	O/P		
66	A14	O/P		
67	A15	O/P		

Package L8	Signal		Description
68	DV_{SS}	Power	The digital negative supply rail (ground).
69	WEN	O/P	External memory read/~write control.
70	OEN	O/P	External memory output enable (active low).
71	CSN1	O/P	External memory chip select #1 (active low).
72	CSN2	O/P	External memory chip select #2 (active low).
73	CSN3	O/P	External memory chip select #3 (active low).
74	RESETN	I/P	Chip reset (active low). Requires an external 100k Ω pullup resistor to DV_{DD}.
75	VCAP	O/P	Decoupling capacitor
76	AV_{DD}	Power	The analogue positive supply rail. Levels and thresholds within the modem are proportional to this voltage.
77	VREF	O/P	A/D converter voltage reference output.
78	VINA	I/P	A/D converter input A. This input should be carefully decoupled to AV_{SS} to avoid instability in readings.
79	VINB	I/P	A/D converter input B. This input should be carefully decoupled to AV_{SS} to avoid instability in readings.
80	AV_{SS}	Power	The analogue negative supply rail (ground).
81	LINERXF	O/P	The output of the Line Rx Input Amplifier.
82	LINERXBN	I/P	An auxiliary inverting input to the Line Rx Input Amplifier, switched in parallel with LINERXN to boost gain.
83	LINERXN	I/P	The inverting input to the Line Rx Input Amplifier.
84	LINERXP	I/P	The non-inverting input to the Line Rx Input Amplifier.
85	PHONERXF	O/P	The output of the Phone Rx Input Amplifier.
86	PHONERXN	I/P	The inverting input to the Phone Rx Input Amplifier.
87	PHONERXP	I/P	The non-inverting input to the Phone Rx Input Amplifier.
88	AV_{SS}	Power	The analogue negative supply rail (ground).
89	V_{BIAS}	O/P	Internally generated bias voltage of approximately $AV_{SS}/2$, except when the device is in Powersave mode, when V_{BIAS} will discharge to AV_{SS}. Should be decoupled to AV_{SS} by a capacitor mounted close to the device pins.

Package L8	Signal		Description
90	PHONETXN	O/P	The inverted output of the Phone Tx Output Driver.
91	PHONETXP	O/P	The non-inverted output of the Phone Tx Output Driver.
92	LINETXN	O/P	The inverted output of the Line Tx Output Driver.
93	LINETXP	O/P	The non-inverted output of the Line Tx Output Driver.
94	AV_{DD}	Power	The analogue positive supply rail. Levels and thresholds within the modem are proportional to this voltage.
95	HT	BI	Open drain output and Schmitt trigger input forming part of the Hook signal detector. Connect to DV_{DD} if Hook Detector not used.
96	HD	I/P	Schmitt trigger input to the Hook signal detector. Connect to DV_{SS} if Hook Detector not used.
97	DV_{SS}	Power	The digital negative supply rail (ground).
98	RDRVN	O/P	Relay drive output, low resistance pull down to DV_{SS} when active, medium resistance pull up to DV_{DD} when inactive.
99	RD	I/P	Schmitt trigger input to the Ring signal detector. Connect to DV_{SS} if Ring Detector not used.
100	RT	BI	Open drain output and Schmitt trigger input forming part of the Ring signal detector. Connect to DV_{DD} if Ring Detector not used.

Notes: I/P = Input
O/P = Output
BI = Bi-directional

1.4 External Components

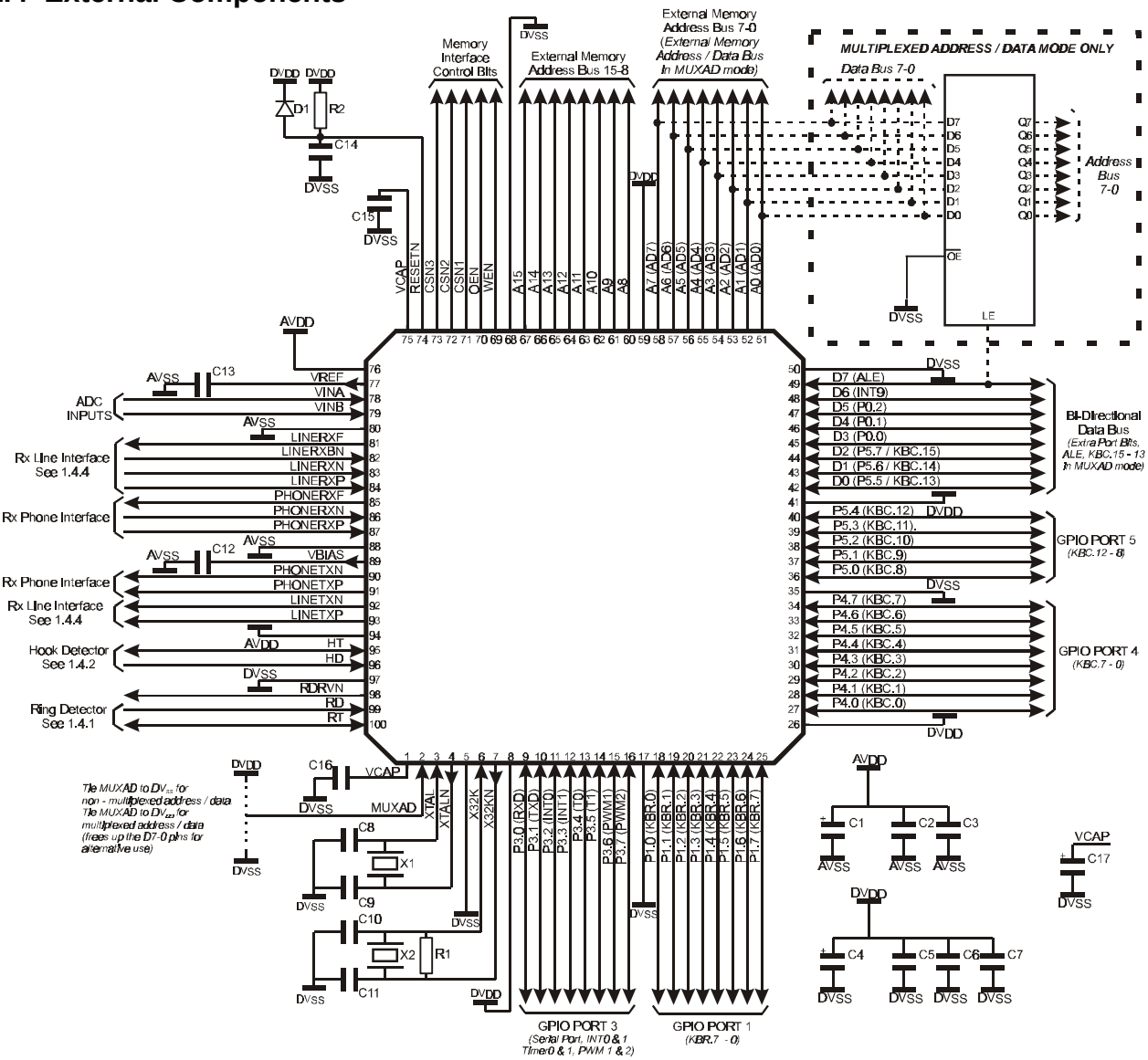


Figure 2a Recommended External Components for a Typical Application

C1, C4,C17	10µF	C2, C3, C12	100nF
C5, C6, C7,C15,C16	100nF	C8, C9	22pF
C10, C11 (optional see note)	18pF	C13	1nF
C14	1µF	D1	1N914
R1 (optional see note)	10MΩ	R2	100kΩ
X1	11.0592MHz or 12.288MHz	X2 (optional see note)	32.768kHz

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Note: The components C10, C11, R1 and X2 are optional, they are not required if the 32.768kHz clock is derived internally from the 11.0592MHz/12.288MHz system clock. See section 1.5.6 for details.

The CMX850 modem and ADC interfaces are capable of detecting and decoding small amplitude signals. To achieve this, DV_{DD}, AV_{DD} and V_{BIAS} should be decoupled and the receive path protected from extraneous in-band signals. It is recommended that the printed circuit board is laid out with AV_{SS} and DV_{SS} ground planes in the CMX850 area, as shown in Figure 2b, with provision to make a link between them close to the CMX850. To provide a low impedance connection to ground, the decoupling capacitors C1 – C7, C12, C13 and C15 – C17 must be mounted as close to the CMX850 as possible and connected directly to their respective ground plane. The use of surface mounted capacitors is recommended.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity. Apart from the decoupling capacitor shown (C12), no other loads are allowed. If V_{BIAS} needs to be used to set external analogue levels, it must be buffered with a high input impedance buffer.

VREF is the internal reference voltage generated for the ADC. For best ADC performance, it is recommended that a 1nF capacitor be placed on this pin and connected to AV_{SS}. The pin may also be used as a reference voltage externally (see section 1.5.8), however it is recommended that a maximum of 1µA is drawn from the pin. If more current is required externally, then a suitable buffer must be used.

The DV_{SS} to the Xtal oscillator capacitors C8 – C11 should be of low impedance and preferably be part of the DV_{SS} ground plane to ensure reliable start up. The resistor across the 32.768kHz Xtal should be 10MΩ for best performance. Using a smaller resistor will result in increased power consumption.

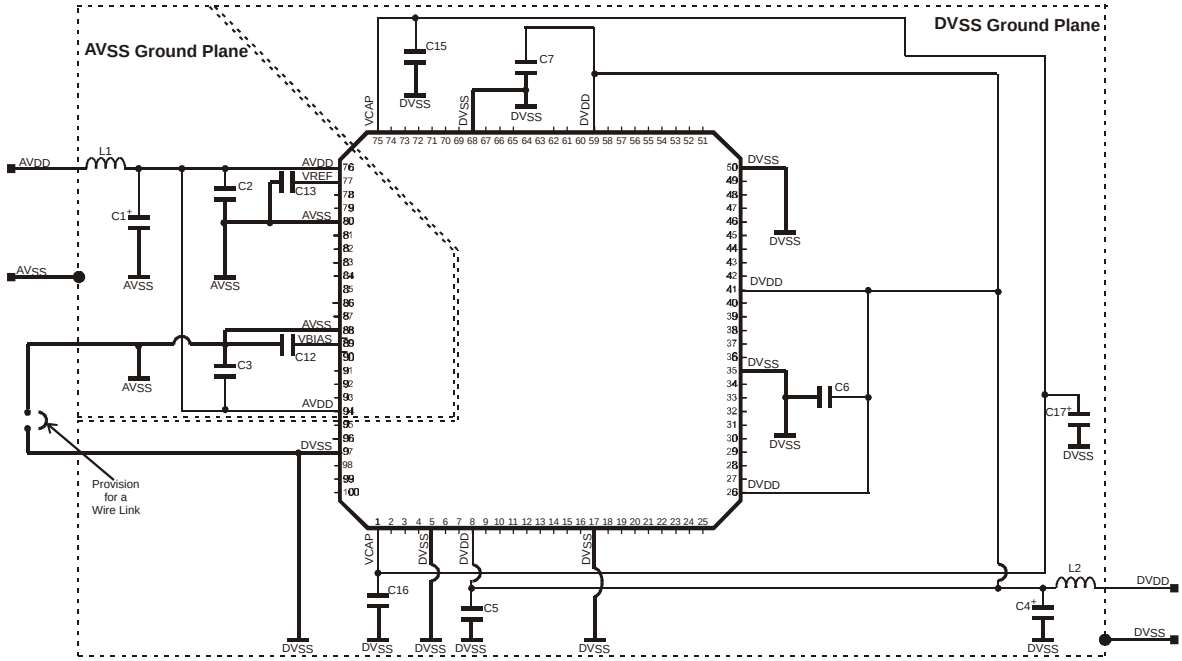


Figure 2b Recommended Power Supply Connections and De-coupling

C1, C4, C17	10µF	C2, C3, C12	100nF
C5, C6, C7,	100nF	C13	1nF
C15, C16	100nF		
L1	100nH (optional, see note)	L2	100nH (optional, see note)

Note: The inductors L1 and L2 can be omitted but this may degrade system performance.

1.4.1 Ring Detector Interface

Figure 3 shows how the Modem may be used to detect the large amplitude ringing signal voltage present on the 2-wire line at the start of an incoming telephone call.

The ring signal is usually applied at the subscriber's exchange as an ac voltage inserted in series with one of the telephone wires and will pass through either C20 and R20 or C21 and R21 to appear at the top end of R22 (point X in Figure 3) in a rectified and attenuated form.

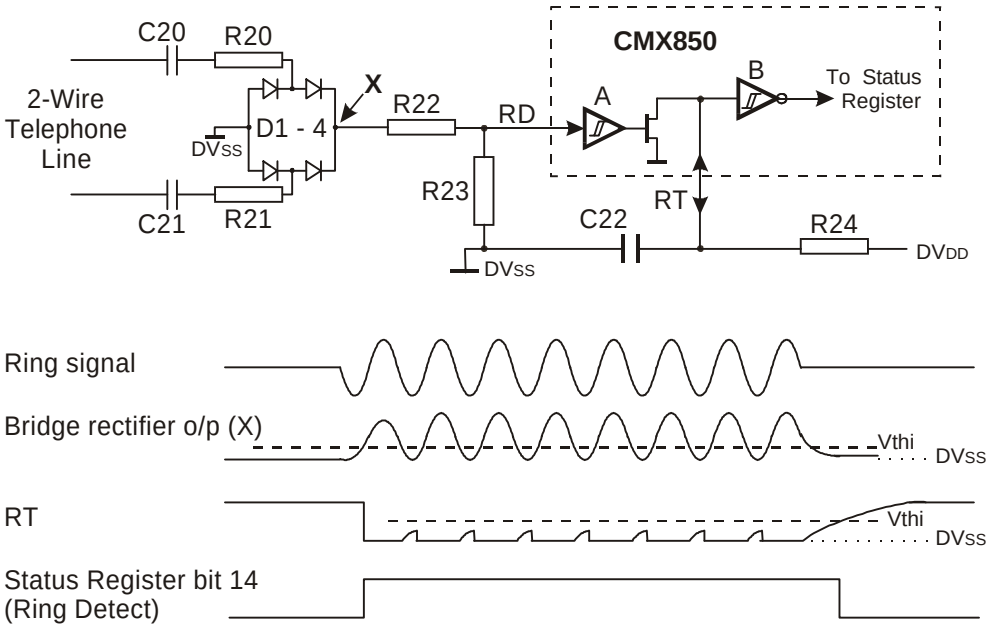
The signal at point X is further attenuated by the potential divider formed by R22 and R23 before being applied to the CMX850 RD input. If the amplitude of the signal appearing at RD is greater than the input threshold (Vthi) of Schmitt trigger 'A' then the N transistor connected to RT will be turned on, pulling the voltage at RT to DV_{SS} by discharging the external capacitor C22. The output of the Schmitt trigger 'B' will then go high, setting bit 14 (Ring Detect) of the modem's Status Register 1.

The minimum amplitude ringing signal that is certain to be detected is:

$$(0.7 + Vthi \times [R20 + R22 + R23] / R23) \times 0.707 \quad Vrms$$

where Vthi is the high-going threshold voltage of the Schmitt trigger A. See Figure 16.

With R20 - R22 all 470kΩ as Figure 3, then setting R23 to 68kΩ will guarantee detection of ringing signals of 40Vrms and above for DV_{DD} over the range 3V to 3.6V.



R20, 21, 22	470kΩ	C20, 21	0.1µF
R23	See text	C22	0.33µF
R24	470kΩ	D1-4	1N4004

Resistors ±5%, capacitors ±20%

Figure 3 Ring Signal Detector Interface Circuit

If the time constant of R24 and C22 is large enough then the voltage on RT will remain below the threshold of the 'B' Schmitt trigger for the duration of a ring cycle.

The time for the voltage on RT to charge from DV_{SS} towards DV_{DD} can be derived from the formula:

$$V_{RT} = DV_{DD} \times [1 - \exp(-t/(R24 \times C22))]$$

As the Schmitt trigger high-going input threshold voltage (Vthi) has a minimum value of 0.56 x DV_{DD}, then the Schmitt trigger B output will remain high for a time of at least 0.821 x R24 x C22 following a pulse at RD.

The values of R24 and C22 given in Figure 3 (470kΩ and 0.33µF) give a minimum RT charge time of 100 ms, which is adequate for ring frequencies of 10Hz or above.

Note that the circuit will also respond to a telephone line voltage reversal. If necessary the µC can distinguish between a Ring signal and a line voltage reversal by measuring the time that bit 14 of the modem's Status Register 1 (Ring Detect) is high.

If the Ring detect function is not used then pin RD should be connected to DV_{SS} and RT to DV_{DD}.

1.4.2 Hook Detector Interface

This is identical internally to the Ring Detector interface circuit and similar components could be used externally, with appropriate values, if hook detection is to be performed by detecting a voltage change across the tip and ring lines to the local phone.

1.4.3 RESETN pin

When this pin is taken low, it resets the CMX850, which includes the µC and modem. The reset to the modem performs the same operation as a C-BUS General Reset command. As a consequence the modem will enter the powersaved state. Refer to section 1.6.11.1 (General Reset Command) and 1.6.11.2 (General Control Register, Powerup bit) for further information. At the same time as the modem is reset, the µC and its SFRs will also be reset. No further accesses are made to external memory until the RESETN pin makes a low to high transition, when program execution will begin from either external memory or internal (local) BOOT ROM, depending on the duration of the RESETN pulse and the state of the V_{BIAS} pin during the low to high transition of the RESETN pin. See section 1.4.4 for a more detailed description of local BOOT ROM execution. On initial power-up, the CMX850 performs a power-on reset which is similar to taking the RESETN pin low.

The following SFR registers of the µC are not affected by the RESETN pin or a power-up reset. The reason for not resetting these bits is so that i) the real time clock doesn't stop when RESETN is asserted, ii) the user can tell if the watchdog timed out and caused the reset, and iii) established practice is maintained – in the case of the standard 8051 SFRs.

OBSCON b7..0:
These are cleared by a power-up reset, but are not affected by the RESETN pin.

WDTCON b2:
This bit is cleared by a power-up reset, but is not affected by the RESETN pin.

RTCCON b7 and b3:
These bits are not affected by either power-up reset or RESETN; they are indeterminate on power-up.

TIME0, 1, 2, 3 (all 32 bits):
These bits are not affected by either power-up reset or RESETN; they are indeterminate on power-up.

ALM0, 1, 2, 3 (all 32 bits):
These bits are not affected by either power-up reset or RESETN; they are indeterminate on power-up.

SBUF b7..0:
A standard 8051 µC register (UART data buffer). The bits of this register are not affected by either power-up reset or RESETN: they are indeterminate on power-up.

1.4.4 Local BOOT ROM

The CMX850 can be configured to execute the “thin stub” code, which resides in the on-chip BOOT ROM, instead of the normal program contained in the user’s external ROM. This “thin stub” code will download a “thick stub” code from the serial port, place it in XRAM and execute it. The template for the “thick stub” code is supplied by CML to enable customers to create a “thick stub” for the purposes of reprogramming FLASH memory, which the user may fit in place of external ROM. An 11.0592 MHz xtal must be used to obtain the standard 19,200 baud rate, in order to reprogram FLASH memory from the 8051 µC serial port. This baud rate is fixed by the "thin stub" code and the chip reset mechanism. It is not variable. Please contact CML Technical Support for details of suitable FLASH memories.

To execute the BOOT ROM program:

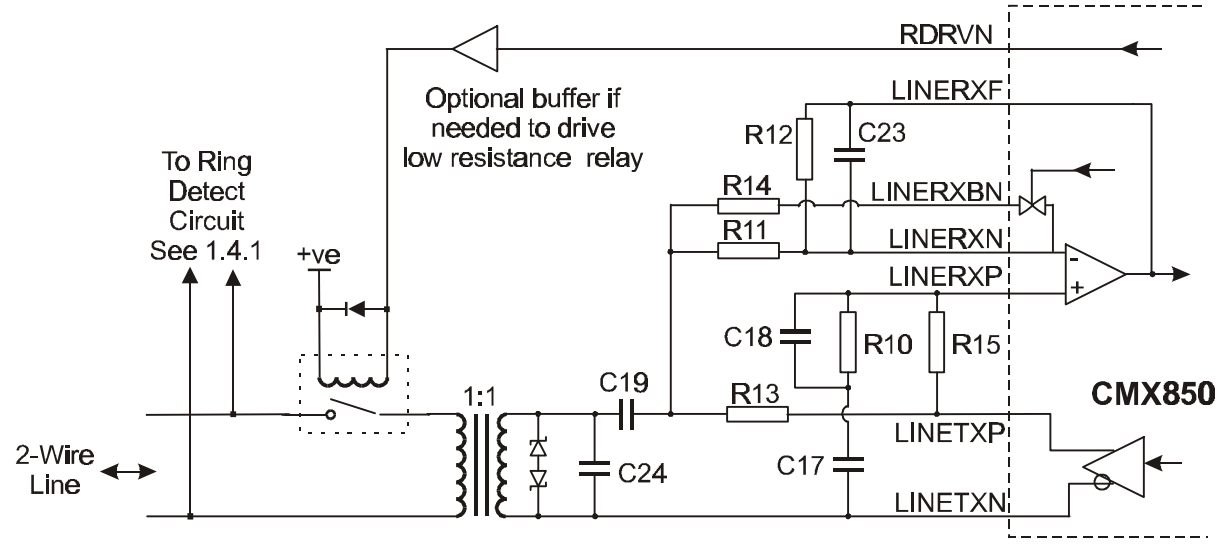
1. Make sure the device is powered up.
2. Apply reset by pulling the RESETN pin low for a minimum of two seconds.
3. While reset is active, short the V_{BIAS} pin to the analogue V_{DD} supply. This can be done with a wire link or an active device (the voltage on the V_{BIAS} pin must be no lower than $V_{DD} – 0.1V$). Note that while reset is active, the V_{BIAS} pin looks like a 50kΩ (nominal) resistor to V_{SS} in parallel with the off-chip decoupling capacitor.
4. Remove reset from the device by taking the RESETN pin high. The voltage on the V_{BIAS} pin must be held for at least 1µs. The device will then boot up from the internal BOOT ROM.
5. To get the device out of “BOOT ROM” mode it must be reset again with the connection between V_{BIAS} and V_{DD} removed (so that the voltage on the V_{BIAS} pin is less than ½V_{DD}). Alternatively, a reset pulse of less than 0.4 seconds will get the device out of “BOOT ROM” mode, whatever voltage is on the V_{BIAS} pin.

1.4.5 Line Interface

A line interface circuit is needed to provide dc isolation and to terminate the line.

2-Wire Line Interface

Figure 4a shows an interface for use with a USA 600Ω 2-wire line. The complex line termination is provided by R10, R13, C17, C18, C19 and C24, high frequency noise is attenuated by C23 and C24, while R11 and R12 set the receive signal level into the modem. R14 connects in parallel with R11 when enabled in the Analogue Signal Path Register. This is for the purpose of increasing gain, which is necessary to compensate for signal attenuation during on-hook CLI detection. Tx rejection into the Rx is provided by R15. For clarity, not all of the 2-wire line protection circuits have been shown. Components for use in other countries vary by country.



R10	180kΩ	C17	100nF
R11, 14	See text	C18	47pF (USA)
R12	100kΩ	C19	wire link (USA)
R13	600Ω	C23	100pF
R15	120kΩ	C24	33nF

Resistors ±5%, capacitors ±20%

Figure 4a 2-Wire Line Interface Circuit

The transmit line signal level is determined by the voltage swing between the TXP and TXN pins, less 6dB due to the line termination resistor R13, and less the loss in the line coupling transformer.

Allowing for 1dB loss in the transformer, then with the Tx Mode Register set for a Tx Level Control gain of 0dB the nominal transmit line levels will be:

	V_{DD} = 3.3V
QAM, DPSK and FSK Tx modes (no guard tone)	-9.2dBm
Single tone transmit mode	-9.2dBm
DTMF transmit mode	-5.2 and -7.2 dBm

For a line impedance of 600Ω, 0dBm = 775mVrms. See also section 1.7.1.3.

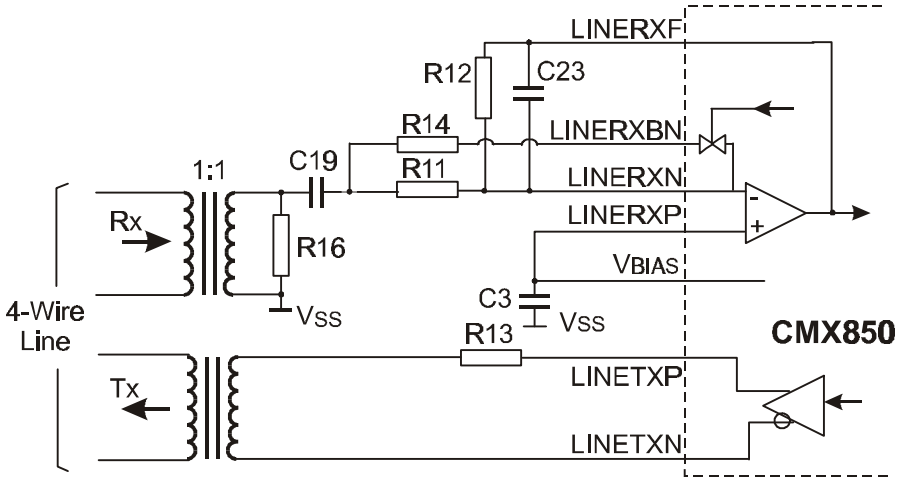
In the receive direction, the signal detection thresholds within the modem are proportional to V_{DD} and are affected by the Rx Gain Control gain setting in the Rx Mode Register. The signal level into the modem is affected by the line coupling transformer loss and the values of R11 and R12 of Figure 4a.

Assuming 1dB transformer loss, the Rx Gain Control programmed to 0dB and R12 = 100kΩ, then for correct operation (see section 1.7.1.3) the value of R11 should be equal to 500 / V_{DD} kΩ, i.e. 150kΩ at V_{DD} = 3.3V.

4-Wire Line Interface

Figure 4b shows a simplified interface for use with a 600Ω 4-wire line. The line terminations are provided by R13 and R16, high frequency noise is attenuated by C23 while R11 and R12 set the receive signal level into the modem. R14 connects in parallel with R11 when enabled in the Analogue Signal Path Register. This is for the purpose of increasing gain, which is necessary to compensate for signal attenuation during on-hook CLI detection.

Transmit and receive line level settings and the value of R11 and R14 are as for the 2-wire circuit.



R13, 16	600Ω	C3	100nF
R11, 14	See text	C19	33nF
R12	100kΩ	C23	100pF

Resistors ±5%, capacitors ±20%

Figure 4b Simplified 4-Wire Line Interface Circuit

1.5 Microcontroller Core

The CMX850 microcontroller core is software and cycle-timing compatible with the industry standard 80C51 and includes standard hardware such as a 256-byte local RAM, timer/counters, serial interface and interrupt controller. The microcontroller architecture is further enhanced by the addition of extra core functionality along with a comprehensive set of on-chip “peripheral” hardware. These are controlled by new registers mapped into the 8051’s Special Function Register space. These additional features include:

- Dual data pointers
- 8kbyte on-chip XRAM
- General-purpose ports (up to 35 pins) with explicit direction and open-drain control, and optional pull-up resistors
- External 64kbyte program address space, extendable using bank switching
- Four independently selectable XRAM source/destination areas, including on-chip XRAM and three off-chip areas accessible through separate chip select pins
- Optional “MOVX” wait state for slow external peripherals
- 8 extra interrupts
- Advanced oscillator and power saving controls
- C-BUS controller connected to on-chip DSP modem
- Keyboard encoder (up to 128 keys)
- Dual channel 10-bit ADC with threshold comparators and internal bandgap reference
- Real time clock and alarm
- Watchdog timer
- Dual pulse-width modulators
- Debugger support through the use of a super priority interrupt pin

This datasheet contains a detailed description of the features unique to the CMX850 device. For a more detailed description of the 8051 µC architecture, instruction set, timers, serial port, interrupts and CPU timing, reference should be made to Programmers Guides, Hardware Descriptions and similar documentation on the 8051 µC architecture, which is widely available. Please contact CML Technical Support in case of difficulty.

1.5.1 Special Function Register Memory Map

The CMX850 microcontroller's special function register (SFR) area contains the complete set of standard 8051 SFRs, along with the additional SFRs required to control the CMX850's extra hardware functions.

↓ Bit addressable — Standard 80C51 SFRs are shown in parentheses

(lsb)	'..... 000'	'..... 001'	'..... 010'	'..... 011'	'..... 100'	'..... 101'	'..... 110'	'..... 111'
$F8			MEMCON	RTCCON	TIME0	TIME1	TIME2	TIME3
$F0	(B)		WDTCON	WDTLD	ALM0	ALM1	ALM2	ALM3
$E8		CASDET	CBUSCON	CBUSBUF	KBCON	KBSTAT	KBBUF	
$E0	(ACC)		ADCCON1	ADCCON2	ADCBUFL	ADCBUFH	ADCTHRL	ADCTHRH
$D8	P5	P5DIR	P5OD	P5RES		PWMCON	PWM1	PWM2
$D0	(PSW)	FSKBUF						
$C8								
$C0	P4	P4DIR	P4OD	P4RES				
$B8	(IP)	IP_1						
$B0	(P3)	P3DIR	P3OD	P3RES				
$A8	(IE)	IE_1	ICON1A	ICON1B				
$A0	(P2)							
$98	(SCON)	(SBUF)			OSCCON	SPDCON	SPXMASK	PDXMASK
$90	(P1)	P1DIR	P1OD	P1RES	P0DIR			TESTCON
$88	(TCON)	(TMOD)	(TL0)	(TL1)	(TH0)	(TH1)		
$80	(P0)	(SP)	(DPL)	(DPH)	DPL1	DPH1	DPS	(PCON)

Table 1 Special Function Registers

The CMX850's SFRs are mapped into the local RAM address space between locations $80 and $FF, and are accessible by standard 8051 instructions which use direct addressing. SFRs whose address is divisible by 8 are also accessible using bit-addressing instructions. The TESTCON SFR is used for production test only and should not be written to under any circumstances. Similarly, any undefined addresses in the table should not be written to, otherwise device operation may become unpredictable.

1.5.2 Dual Data Pointer

The standard 8051 µC has a single 16-bit data pointer DPTR which can be used to address XRAM or program memory, using MOVX and MOVC instructions respectively. The DPTR register is also mapped into two 8-bit SFRs, DPL and DPH. The CMX850 has an additional 16-bit data pointer DPTR1 that can significantly speed up block moves by allowing 16-bit source and destination pointers to be maintained simultaneously. DPTR1 is mapped into SFR registers DPL1 and DPH1. A separate SFR register DPS is used to select between DPTR and DPTR1: all instructions that use the data pointer directly (INC DPTR; MOV DPTR,#data16; MOVC A,@A+DPTR; MOVX A,@DPTR; MOVX @DPTR,A) will be directed to whichever data pointer is currently selected by DPS. Swapping between the two data pointers can be easily achieved by using the increment instruction, INC, to toggle DPS bit 0.

1.5.2.1 DPTR Registers (DPL/DPH, DPL1/DPH1)

DPL: SFR Address $82
All bits cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
DPTR Low Byte							

DPH: SFR Address $83
All bits cleared to 0 on reset.

Bit:	7	6	5	4	3	2	1	0
	DPTR High Byte							

DPL1: SFR Address $84
All bits cleared to 0 on reset.

Bit:	7	6	5	4	3	2	1	0
	DPTR1 Low Byte							

DPH1: SFR Address $85
All bits cleared to 0 on reset.

Bit:	7	6	5	4	3	2	1	0
	DPTR1 High Byte							

1.5.2.2 Data Pointer Select Register (DPS)

DPS: SFR Address $86
Bit b0 is cleared to 0 on reset. Other bits are unused, and are 0.

Bit:	7	6	5	4	3	2	1	0
	Unused (always read as 0)							Data pointer select

DPS Register b0: Set to 0 to select DPTR, set to 1 to select DPTR1

1.5.3 I/O Ports

The 8051 µC port structure within the CMX850 has been enhanced by the addition of two extra byte-wide ports, port 4 and port 5. The ports have also been enhanced for low power operation by the addition of explicit port direction control registers, which means that port input pins consume no dc current when driven with a logic 0 (standard 8051 port inputs consume several tens of microamps of dc current per pin when driven with a logic 0). To further enhance flexibility, all of the port 1, 3, 4 and 5 pins can be individually configured as open-drain output drivers, and with optional pull-up resistors.

The port configuration within the CMX850 is shown in Table 2. Note that, in order for port bit P3.1 (TXD) to be used to output serial port data or clock pulses in mode 0-3, both the P3 output latch bit 1 *and* the P3DIR direction latch bit 1 must be loaded with a logic 1. Similarly, in order for port bit P3.0 (RXD) to be used to output serial port data in mode 0, both the P3 output latch bit 0 *and* the P3DIR direction latch bit 0 must be loaded with a logic 1.

Port	Function
Port 0	When the CMX850 is configured with a multiplexed external memory interface (pin MUXAD = 1), port 0 bits 2-0 are available as I/O pins. The remaining port 0 bits (7-3) are unused. Note that the port 0 pins do ***not*** have memory address/data driven onto them during an external memory access, as would happen on a standard 8051: the CMX850 external memory interface is completely separate from the port 0 circuit.
Port 1	Port 1 bits 7-0 are available as I/O pins. They are automatically configured as keyboard row input pins with pull-up resistors when the keyboard encoder is enabled.
Port 2	Port 2 bits 7-0 are not available directly as I/O pins, but the contents of the byte-wide port 2 output latch is used during MOVX A,@Ri and MOVX @Ri,A instructions to form the upper eight address bits on pins A15-8. This is done to maintain compatibility with the standard 8051 µC instruction set.
Port 3	Port 3 bits 7-0 are available as I/O pins. Each pin also has an alternative output function, as shown below. Pins P3.6 and P3.7 are automatically configured as an output when the associated PWM block is enabled. The other alternative pin functions require the correct pin direction to be explicitly configured using the P3DIR register. **Port** **Alternative function** P3.0 RXD (Serial port receive data) P3.1 TXD (Serial port transmit data) P3.2 Int0 (External interrupt 0) P3.3 Int1 (External interrupt 1) P3.4 T0 (Timer/counter 0 external input) P3.5 T1 (Timer/counter 1 external input) P3.6 PWM1 (Pulse-width modulator 1 output) P3.7 PWM2 (Pulse-width modulator 2 output)
Port 4	Port 4 bits 7-0 are available as I/O pins. Between one and eight port 4 pins are automatically configured as open-drain column drivers when the keyboard encoder is enabled, depending on the contents of the KBCON register.
Port 5	Port 5 bits 7-0 are available as I/O pins (bits 7-5 are only available if the CMX850 is configured with a multiplexed external memory interface). Up to eight port 5 pins are automatically configured as open-drain column drivers when the keyboard encoder is enabled, depending on the contents of the KBCON register.

Table 2 I/O Port Function

1.5.3.1 Port Data Registers (P0-P5)

The 8051 µC retains the standard port registers (P0, P1, P2, P3) as well as having two new ports, P4 and P5. Writing to these port SFRs loads the associated output data register, which gets driven onto those device pins that are configured as outputs. Reading from a port SFR will either read the contents of the port output data register, or read directly from the port pins, depending on which instruction is used. The instructions that read the data register rather than the pins are those that perform a read-modify-write operation on a port or a port bit (this is explained in more detail in any standard 8051 µC documentation).

P0: SFR Address $80
P1: SFR Address $90
P2: SFR Address $A0
P3: SFR Address $B0
P4: SFR Address $C0
P5: SFR Address $D8
All bits set to 1 on reset. These registers are bit addressable.

Bit:	7	6	5	4	3	2	1	0
	Bits 7-0 of the port data registers							

1.5.3.2 Port Direction Registers (P0DIR-P5DIR)

Ports 0, 1, 3, 4 and 5 each have a direction control register that allows individual port pins to be configured either as an input or an output. The bits should be cleared to a 0 for an input, or set to 1 for an output.

P0DIR: SFR Address $94
P1DIR: SFR Address $91
P3DIR: SFR Address $B1
P4DIR: SFR Address $C1
P5DIR: SFR Address $D9
All bits cleared to 0 on reset.

Bit:	7	6	5	4	3	2	1	0
	Bits 7-0 of the direction control register							

1.5.3.3 Port Open-Drain Registers (P1OD-P5OD)

Ports 1, 3, 4 and 5 each have an open-drain control register which allows individual port outputs to be configured either with a pull-up/pull-down driver or with an open-drain driver. The bits should be cleared to a 0 for an active pull-up/pull-down driver, or set to 1 for an open-drain driver. Note that if a pin is configured as an input by the port direction control register, then the pin driver will go into a high impedance state irrespective of the contents of the associated open-drain control register bit.

P1OD: SFR Address $92
P3OD: SFR Address $B2
P4OD: SFR Address $C2
P5OD: SFR Address $DA
All bits cleared to 0 on reset.

Bit:	7	6	5	4	3	2	1	0
	Bits 7-0 of the open-drain control register							

1.5.3.4 Port Res Pull-up Registers (P1RES-P5RES)

Ports 1, 3, 4 and 5 each have a resistor pull-up control register which allows individual port pins to be configured either with or without a pull-up resistor. The bits should be cleared to a 0 if no resistor is required, or set to 1 to connect a 50kΩ (nominal) resistor between the pin and DV_{DD}. A port pin should not be configured with a pull-up resistor at the same time as being configured as an output with active pull-up/pull-down drivers, otherwise power will be needlessly wasted when driving out a logic 0.

P1RES: SFR Address $93
P3RES: SFR Address $B3
P4RES: SFR Address $C3
P5RES: SFR Address $DB
All bits cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Bits 7-0 of the resistor pull-up control register							

1.5.4 Memory Interface

In addition to 256 bytes of scratchpad RAM, the CMX850 has 8kbytes of on-chip extension RAM (XRAM) and three separate 64k areas for off-chip memory and peripherals, accessible without glue logic via chip select pins CSN1, CSN2 and CSN3. External memory size can easily be increased to several megabytes by using a code-banking compiler along with a number of CMX850 port output pins as bank select bits.

The CSN1 pin is normally used during program instruction fetches, although there is an option to replace the bottom 8kbytes of off-chip program ROM with the on-chip XRAM, allowing short sections of temporary program code to be executed from the on-chip XRAM. This could be used, for instance, when the CMX850 is re-programming external FLASH memory.

MOVX read and write instructions can be independently directed to either the on-chip XRAM or any of the three off-chip memory areas, including the program ROM area (this allows the CMX850 to re-program external FLASH memory, if necessary). Combined with the dual data pointer architecture of the CMX850 microcontroller, this allows rapid block moves between any of the memory areas. The MOVX read and write instructions can also be independently stretched to allow access to slow memory or peripherals, without any external circuitry being required.

All off-chip accesses use the same 16-bit address bus and 8-bit data bus, along with output enable (OEN) and write enable (WEN) control pins. The address and data pins can be configured to be non-multiplexed by tying input pin MUXAD low (address output on pins A15-0, bi-directional data uses pins D7-0), or the data can be multiplexed with the lower eight address pins (A7-0) by tying input pin MUXAD high.

If configured with a multiplexed address/data bus, an external address latch (‘373 or '573 type) is required. Pin D7 becomes an address latch enable (ALE), and pins D6-0 are reassigned as an extra interrupt pin and general-purpose port bits. During the time when ALE is high, the least significant byte (LSB) of the 16-bit memory address is driven onto pins A7-0. When ALE goes low, the LSB of the memory address gets held in the external address latch, and the A7-0 pins change to a bi-directional data bus.

In order to minimise power consumption and EMI, the CMX850 only performs program memory reads when necessary, rather than doing continuous reads and discarding the unnecessary ones as on a standard 8051. This typically reduces the number of program read operations by 30% - 40%. Furthermore, when using a multiplexed address/data bus, unnecessary ALE pulses are inhibited.

The CMX850 data pins (D7-0 for non-multiplexed, or A7-0 for multiplexed) can be configured with weak bus-holding devices to prevent voltage drift on the pins during long periods of inactivity (e.g. when in idle/power down mode, or executing programs from entirely within on-chip XRAM). This can help reduce unnecessary current consumption in devices connected to the data bus.

The memory interface is configured using the MEMCON SFR.

1.5.4.1 Memory Control Register (MEMCON)

MEMCON: SFR Address $FA
All bits cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Enable bus-hold	Internal progam	MOVX write stretch	MOVX write destination		MOVX read stretch	MOVX read source	

MEMCON Register b7: Enable bus-hold

b7 = 1	Enable data pin bus-holding devices
b7= 0	Disable data pin bus-holding devices

MEMCON Register b6: Internal program

b6 = 1	On-chip XRAM mapped into bottom 8Kbytes of program memory
b6 = 0	Program memory is entirely off-chip

Allows temporary program code to be executed from on-chip XRAM. Note that any interrupt service routine vectors being used (these begin at locations $03 to $6B) should be duplicated in XRAM before setting this bit; alternatively the interrupts should be disabled. When MEMCON bit 6 is altered, even though the instruction that modifies it executes in the normal amount of time, there is an internal delay of 2 machine cycles before the switch between ROM and XRAM takes effect.

MEMCON bit 6 can be changed without any problems when program execution is taking place in external ROM at an address of $2000 or above. Changing MEMCON bit 6 when program execution is taking place in external ROM or internal XRAM at an address between $0000 and $1FFF requires some care to prevent disruption of the desired program flow.

MEMCON Register b5: MOVX write stretch

b5 = 1	MOVX write operations are stretched by one machine cycle (12 xtal cycles)
b5 = 0	MOVX write operations are not stretched

MEMCON Register b4-3: MOVX write destination

b4	b3	
0	0	MOVX write destination is on-chip XRAM
0	1	MOVX write destination is off-chip, using pin CSN1
1	0	MOVX write destination is off-chip, using pin CSN2
1	1	MOVX write destination is off-chip, using pin CSN3

MEMCON Register b2: MOVX read stretch

b2 = 1	MOVX read operations are stretched by one machine cycle (12 xtal cycles)
b2 = 0	MOVX read operations are not stretched

MEMCON Register b1-0: MOVX read source

b1	b0	
0	0	MOVX read source is on-chip XRAM
0	1	MOVX read source is off-chip, using pin CSN1
1	0	MOVX read source is off-chip, using pin CSN2
1	1	MOVX read source is off-chip, using pin CSN3

1.5.5 Interrupts

The 8051 µC interrupt logic has been extended, so that the original five interrupt sources (Int0, Timer0, Int1, Timer1, Serial) have been supplemented by eight new interrupt sources (Int2, Int3, Int4, Int5, Int6, Int7, Int8 and Int9). With the exception of Int9, these new interrupts are connected to the 8051 µC's on-chip peripheral hardware logic as shown in Table 3, so that the hardware can be interrupt driven. Int9 is a super priority interrupt, which can interrupt both low and high priority interrupts, and is available on a device pin when the CMX850 is configured with a multiplexed memory address/data bus. This pin may be driven by an external ROM emulator to assist with program debugging.

Interrupt signal	Hardware source	Vector address	Priority within level
Int2	CAS Detect	$33	1 (Highest)
(Int0)	Interrupt 0 input pin (P3.2)	$03	2
Int3	DSP Modem	$3B	3
(Timer0)	8051 timer 0	$0B	4
Int4	Keyboard encoder	$43	5
(Int1)	Interrupt 1 input pin (P3.3)	$13	6
Int5	A/D converter	$4B	7
(Timer1)	8051 timer 1	$1B	8
Int6	RTC time interrupt	$53	9
(Serial)	RI or TI from 8051 serial port	$23	10
Int7	RTC alarm interrupt	$5B	11
Int8	Watchdog timeout	$63	12 (Lowest)
Int9	Interrupt 9 input pin (D6)*	$6B	N/A (super priority)

* Note: D6 is only available as an interrupt with a multiplexed memory interface (pin MUXAD = 1)

Table 3 Interrupt structure

The "priority within level" structure is only used to resolve simultaneous interrupt requests of the same priority level. A low priority interrupt which is active cannot be interrupted by another low priority interrupt, but can be interrupted by a high priority interrupt or a super priority interrupt (Int9). A high priority interrupt which is active can only be interrupted by Int9.

The new interrupts operate in a similar way to the existing Int0 and Int1 interrupts. Two new SFRs (IE_1 and IP_1) allow the interrupts to be individually enabled and have their priority set, and new SFRs ICON1A and ICON1B allow the interrupts to be configured as falling-edge or low-level triggered. In particular, the existing global interrupt enable bit (IE register bit 7) can be used to disable all of the new interrupts ***with the exception of Int9***. It is recommended that the interrupts connected to the on-chip peripheral hardware (i.e. Int2 … Int8) be configured as low-level triggered, with the application software explicitly clearing the interrupts by using the relevant mechanism built into each hardware block. Note that pin D6 does not have an on-chip pull-up resistor, so if this pin is used as a super priority interrupt (Int9) and is driven from a device with an open-drain output driver, an external pull-up resistor will need to be added.

Further information about the Serial Port transmit/receive interrupt flags and the Int1-0 interrupt type control and edge flags can be found in the description of the SCON and TCON registers.

1.5.5.1 Interrupt Enable Registers (IE, IE_1)

IE: SFR Address $A8
Bits b7 and b4-0 cleared to 0 on reset. Bits b6-5 unused. This register is bit addressable.

Bit:

7	6	5	4	3	2	1	0
Global Interrupt enable (EA)	Unused (set to 0)	Unused (set to 0)	Serial port interrupt enable (ES)	Timer 1 interrupt enable (ET1)	Int1 (P3.3) interrupt enable (EX1)	Timer 0 interrupt enable (ET0)	Int0 (P3.2) interrupt enable (EX0)

IE bits 4-0 can be used to individually enable each of the five standard 8051 interrupts: setting a bit to 1 enables the interrupt, clearing the bit to 0 disables the interrupt. Furthermore, all CMX850 interrupts with the exception of Int9 (i.e. Serial, Timer 1-0, Int 8-0) can be globally disabled by writing 0 to register IE bit 7 (EA).

IE_1: SFR Address $A9
Bits b7-0 cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Int9 (pin D6) interrupt enable	Int8 interrupt enable *Watchdog*	Int7 interrupt enable *RTC alarm*	Int6 interrupt enable *RTC time*	Int5 interrupt enable *ADC*	Int4 interrupt enable *Keyboard*	Int3 interrupt enable *C-BUS*	Int2 interrupt enable *CAS Det.*

IE_1 bits 7-0 can be used to individually enable each of the eight new interrupts on the CMX850: setting a bit to 1 enables the interrupt, clearing the bit to 0 disables the interrupt.

1.5.5.2 Interrupt Priority Registers (IP, IP_1)

IP: SFR Address $B8
Bits b4-0 cleared to 0 on reset. Bits b7-5 unused. This register is bit addressable.

Bit:

7	6	5	4	3	2	1	0
Unused (set to 0)	Unused (set to 0)	Unused (set to 0)	Serial port interrupt priority (PS)	Timer 1 interrupt priority (PT1)	Int1 interrupt priority (PX1)	Timer 0 interrupt priority (PT0)	Int0 interrupt priority (PX0)

IP bits 4-0 can be used to set the priority level of the Serial Port, Timer1, Timer0, Int1 and Int0 interrupts: setting a bit to 1 configures the interrupt as high priority, clearing the bit to 0 configures the interrupt as low priority.

IP_1: SFR Address $B9
Bits b6-0 cleared to 0 on reset. Bit b7 unused.

Bit:

7	6	5	4	3	2	1	0
Unused (set to 0)	Int8 interrupt priority *Watchdog*	Int7 interrupt priority *RTC alarm*	Int6 interrupt priority *RTC time*	Int5 interrupt priority *ADC*	Int4 interrupt priority *Keyboard*	Int3 interrupt priority *C-BUS*	Int2 interrupt priority *CAS Det.*

IP_1 bits 6-0 can be used to set the priority level of interrupts Int8-2: setting a bit to 1 configures the interrupt as high priority, clearing the bit to 0 configures the interrupt as low priority. The Int9 interrupt is permanently configured with a super high priority, enabling it to interrupt any other currently active low or high priority interrupt.

1.5.5.3 Interrupt Control Registers (ICON1A/B)

Each of the new interrupt inputs in the 8051 µC has two associated control/status bits, residing in registers ICON1A and ICON1B. These operate in an identical way to the existing Int0 and Int1 control and status bits in the TCON register.

Type control: these bits are set to 1 or cleared to 0 by software to configure the interrupts as falling-edge or low-level triggered respectively. It is recommended that the type control bits for Int8-2 be cleared to 0, i.e. configured as low-level triggered.

Edge flag: when the interrupt is configured as falling-edge triggered, these bits are set to 1 by hardware to indicate that an edge has been detected, i.e. successive samples of the interrupt pin show a high in one machine cycle and a low in the next cycle, and will be cleared automatically when the service routine is called. When configured as low-level triggered interrupts, the edge flag will be updated once per cycle to reflect the state of the associated interrupt signal; the flag gets set to 1 if the interrupt line is active (i.e. low), and gets cleared to 0 if the interrupt line is inactive (high).

ICON1A: SFR Address $AA
All bits cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Int5 edge flag	Int5 type control	Int4 edge flag	Int4 type control	Int3 edge flag	Int3 type control	Int2 edge flag	Int2 type control

ICON1B: SFR Address $AB
All bits cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Int9 edge flag	Int9 type control	Int8 edge flag	Int8 type control	Int7 edge flag	Int7 type control	Int6 edge flag	Int6 type control

1.5.6 Oscillator and Power Management

Each main block of "peripheral" hardware surrounding the 8051 µC core (Modem, CAS detector, A/D converter, PWM, RTC, WDT, Keyboard encoder) can be individually power saved through their associated control register, as shown in the table below:

Function:		Controlled by:	Comment:
Oscillator Control	– 11.0592/12.288 MHz	OSCCON (9C) bits 4 and 5	
	– 32 kHz	OSCCON (9C) bit 1	
	– 5.5 MHz RC oscillator	OSCCON (9C) bits 4 and 5	
8051 µC Core	– powersave/active	PCON (87) bit 1	
	– idle mode	PCON (87) bit 2	
Auxiliary ADC		ADCCON1 (E2) bit 2 and ADCCON2 (E3) bits 1, 2 and 3	Needs System Clock to be active (9C bit 5)
CAS and FSK Detect		CASDET (E9) bit 7	Automatically powers up V_{BIAS} and Line Input Amplifier in the Modem. Also needs System Clock to be active (9C bit 5)
Keyboard Encoder		KBCON (EC) bits 6 and 7	
PWM Outputs		PWMCON (DD) bits 6 and 7	Needs System Clock to be active (9C bit 5)
Real Time Clock (RTC)		RTCCON (FB) bit 7	excludes 32 kHz oscillator
Watchdog Timer (WDT)		WDTCON (F2) bit 7	excludes 32 kHz oscillator

Function:		Controlled by:	Comment:
Modem Core:	– powersave/active	CBUS $E0 bit 8	addressed through: CBUSBUF (EB) bits 0 – 7 and CBUSCON (EA) bits 0 and 2
	– idle mode	CBUS $E0 bit 7	
	– CBUS interface		Always active
	– modem functions	CBUS $E0 bit 8	Needs System Clock to be active (9C bit 5)
	– output amplifiers	CBUS $E0 bit 8 and CBUS $EC bits 1 – 4	
	– input amplifiers	CBUS $E0 bit 8	
	– V_{BIAS} generator	CBUS $E0 bit 8	
	– RD, HD and RDRVN		Always active

Table 4 Powersave Functions

The CMX850 provides additional power management features, such as a low power RC oscillator and speed-control options for the 8051 clock, which allow the current consumption to be further reduced when the device is not fully operational (the standard 8051 Idle and Power Down modes of operation are also available). Further enhancements enable the 8051 µC to automatically exit from speed control or power down modes, without requiring a system reset.

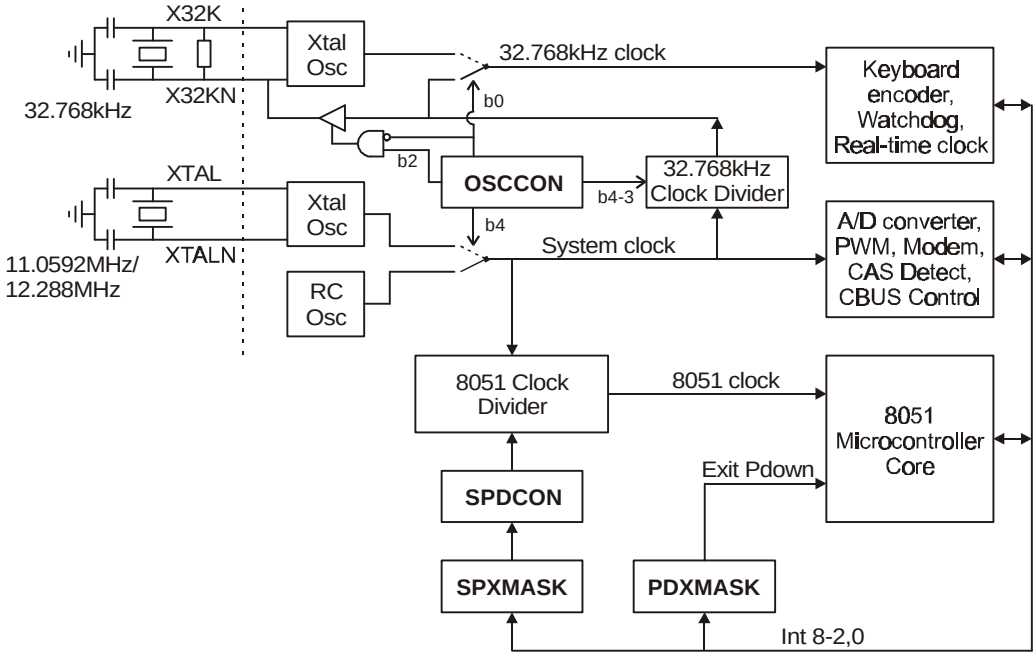


Figure 5 Oscillator and Power Management

1.5.6.1 Oscillator Control Register (OSCCON)

The OSCCON register allows the selection of the main system clock (external Xtal or low power 5.5MHz RC oscillator), the 32.768kHz reference (external Xtal or system clock sub-division), and whether the clocks are power-saved when the 8051 µC is in power down mode.

OSCCON: SFR Address $9C
All bits cleared to 0 when the device powers up. This register is not affected by the reset pin or a watchdog reset.

Bit:

7	6	5	4	3	2	1	0
General-purpose flag 1	General-purpose flag 0	System clock power down	System clock source select	System Xtal freq. select	32.768k clock output enable	32.768k clock power down	32.768k clock source select

OSCCON Register b7-6: General-purpose flags 1-0
These bits are available for use as general-purpose flags; they do not affect the operation of the CMX850 hardware. Because these bits are cleared to 0 at power up but are not affected by the reset signal, a particular use for one of them is as a “cold-start” indicator: software would initially examine the flag to see if it contains a 0, and if so run a power-up initialisation routine before setting the flag to 1. If the CMX850 is subsequently reset the flag would read back as a 1, allowing the software to take alternative action (e.g. checking for a watchdog timeout).

OSCCON Register b5: System clock power down
Controls whether the system clock (either the RC or Xtal oscillator) is power saved when the 8051 µC is in power down mode (power down mode is enabled by writing 1 to PCON bit 1). This depends on whether any of the peripheral blocks that use the system clock (i.e. Modem, CAS detector, A/D converter, PWM) need to remain active during 8051 power down.

b5 = 1	System clock remains active during 8051 power down
b5 = 0	System clock power saved during 8051 power down

OSCCON Register b4: System clock source select
Controls whether the system clock is derived from the on-chip RC oscillator or from an external Xtal reference. The RC oscillator has a nominal frequency of 5.5MHz but consumes much less power than the Xtal oscillator, and so can be used when performing background tasks. The frequency of the RC oscillator is not sufficiently accurate to allow data transfers through the modem or serial port, however. The CMX850 powers up with the RC oscillator selected.

When switching from the RC oscillator to the Xtal reference, there will be a delay while the Xtal oscillations build up (typically between 5ms and 20ms). In addition to this delay, the CMX850 waits for 2^{16} Xtal clock cycles to occur (~5ms – 6ms) during which time the system clock remains inactive. This ensures that the Xtal oscillations have been adequately established before proceeding. Note that the delay when switching back from the Xtal reference to the RC oscillator is typically less than 1µs.

b4 = 1	System clock source is external Xtal, RC oscillator is powered down
b4 = 0	System clock source is 5.5MHz RC oscillator, external Xtal is powered down

OSCCON Register b3: System crystal frequency select
This bit should be set according to the system Xtal frequency being used. It is used to select the division ratio when the 32.768kHz reference is being derived from the main system clock (see description of OSCCON bit 0), and is also used to configure the DSP modem's clock dividers. This bit must be set to the correct state before the modem is used.

b3 = 1	System Xtal frequency is 11.0592MHz
b3 = 0	System Xtal frequency is 12.288MHz

OSCCON Register b2: 32.768kHz clock output enable
This bit can be used to drive the 32.768kHz reference signal onto the X32KN pin for use by external circuitry. This can only be done if the 32.768kHz signal is derived from the main system clock; the function is disabled if using an external 32.768kHz Xtal reference (see description of OSCCON bit 0).

b2 = 1	Drive internal 32.768kHz reference onto X32KN pin (only if OSCCON bit 0 = 0)
b2 = 0	Do not drive internal 32.768kHz reference onto X32KN pin

OSCCON Register b1: 32.768kHz clock power down
Controls whether the 32.768kHz clock is power saved when the 8051 µC is in power down mode (power down mode is enabled by writing 1 to PCON bit 1). This depends on whether any of the peripheral blocks that use the 32.768kHz clock (i.e. RTC, WDT, Keyboard encoder) need to remain active during 8051 power down.

b1 = 1	32.768kHz clock remains active during 8051 power down
b1 = 0	32.768kHz clock power saved during 8051 power down

OSCCON Register b0: 32.768kHz clock source select
Controls whether the 32.768kHz clock is derived from a divided down main system clock (thus saving the expense of an external 32.768kHz Xtal), or uses the external Xtal (which allows the 32.768kHz clock to remain active while the system clock is powered down). If dividing down from the main system clock, the division ratio depends on whether an 11.0592MHz or 12.288MHz Xtal is used (see OSCCON bit 3), or whether the RC oscillator is selected. The accuracy of the 32.768kHz clock will only be as good as that of the selected reference source, which in the case of the RC oscillator is not good enough to maintain the correct time and date in the RC.

b0 = 1	32.768kHz clock source is external Xtal			
b0 = 0	32.768kHz clock derived from main system clock:			
	OSCCON b4	**OSCCON b3**	**System clock division ratio**	
	0	X	168¾	(Due to odd division ratios, derived clock edge will jitter slightly but frequency will be accurate)
	1	0	375	
	1	1	337½	

1.5.6.2 Speed Control Register (SPDCON)

The 8051 µC can be configured to run at a reduced internal clock speed, selectable through the SPDCON register, to allow software to continue executing but with substantially reduced power consumption. This is especially useful when combined with the low power RC oscillator option. Note that the 8051 µC clock speed reduction does not alter the speed of the system clock used by the modem, A/D converter, or PWM blocks, but these blocks can be separately power saved if necessary. Running the µC with a reduced clock speed will have a direct effect on the operation of the 8051 core's interrupt latency, serial port, and timers.

The 8051 µC clock can be selected to be a simple binary division of the main system clock, with division ratios selectable between ÷4 and ÷1024. However, because many external memory devices only enter low power standby mode when they are not being accessed, this simple binary division may not achieve the ultimate power saving possible. This is because the average time that the external memory is being accessed will not reduce. The 8051 µC speed control mechanism can therefore be configured into a new "burst mode", where the µC executes single complete instructions at a time at full speed, followed by longer periods of inactivity where the clock to the µC is halted and external memory is held in standby (CSN1/2/3 and OEN pins held high). The average instruction throughput in burst mode is identical to that in non-burst mode, but the average time for which the external memory is active is greatly reduced.

When in reduced speed mode or power down mode, the external data bus may float for considerable periods of time. This may cause unnecessary power consumption in devices connected to the data bus due to voltage drift on the bus pins. To avoid this, the memory interface can be configured with weak bus-holding devices to prevent this voltage drift (see description of MEMCON register).

The 8051 µC can be configured, using the SPXMASK register, to exit reduced speed mode automatically upon receiving an interrupt signal. This immediately causes the 8051 µC to begin clocking again at full speed.

SPDCON: SFR Address $9D
All bits cleared to 0 on reset, or upon automatic exit of reduced speed operation.

Bit:

7	6	5	4	3	2	1	0
Unused, always read as 0				Burst mode	8051 µC clock speed select		

SPDCON Register b7-4: Unused

SPDCON Register b3: Burst mode

b3 = 1	Burst mode enabled
b3 = 0	Burst mode disabled

SPDCON Register b7-4: 8051 µC clock speed select

b2	b1	b0	
0	0	0	8051 speed reduction disabled
0	0	1	8051 clock speed = divide by 4
0	1	0	8051 clock speed = divide by 16
0	1	1	8051 clock speed = divide by 64
1	0	0	8051 clock speed = divide by 256
1	0	1	8051 clock speed = divide by 1024
1	1	0	Reserved (do not use)
1	1	1	Reserved (do not use)

1.5.6.3 Speed Control Exit Register (SPXMASK)

This register can be configured to allow the 8051 µC to be brought immediately out of speed control mode when any interrupt input line to the µC (chosen from Int8-2 and Int0) goes active, i.e. low. To enable an interrupt to bring the 8051 µC out of speed control mode, its associated mask bit in the SPXMASK register must be set to a 1, otherwise it should be cleared to 0. Note that the µC can be brought out of speed control mode by an interrupt that is not enabled in the IE or IE_1 SFRs. This allows the speed control exit feature to be used even in systems that poll the peripheral hardware rather than have it interrupt driven.

When an interrupt goes active whose mask bit is set to 1, the SPDCON register bits are all immediately cleared to 0.

SPXMASK: SFR Address $9E
All bits cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Int8 exit mask	Int7 exit mask	Int6 exit mask	Int5 exit mask	Int4 exit mask	Int3 exit mask	Int2 exit mask	Int0 exit mask

1.5.6.4 Power Down Exit Register (PDXMASK)

This register can be configured to allow the 8051 µC to be brought immediately out of power down mode when any interrupt input line to the µC (chosen from Int8-2 and Int0) goes active, i.e. low. To enable an interrupt to bring the 8051 µC out of power down mode, its associated mask bit in the PDXMASK register must be set to a 1, otherwise it should be cleared to 0. Note that the µC can be brought out of power down mode by an interrupt that is not enabled in the IE or IE_1 SFRs. This allows the power down exit feature to be used even in systems that poll the peripheral hardware rather than have it interrupt driven.

When the 8051 µC is brought out of power down mode, register PCON bit 1 immediately gets cleared to 0 and the µC will then respond to any active, enabled interrupts. If no enabled interrupt is active, the µC will continue program execution from the instruction following the one that put it into power down mode.

Note that if the CMX850 system clock source is configured as an external Xtal that gets disabled in power down mode (see OSCCON register), it will take a number of milliseconds for the Xtal to start up again and stabilise before the system begins clocking. If a more rapid response during a power down exit is required, either the Xtal should remain running during power down or the system clock source should be configured to be the RC oscillator before power down mode is entered.

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PDXMASK: SFR Address $9F
All bits cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Int8 exit mask	Int7 exit mask	Int6 exit mask	Int5 exit mask	Int4 exit mask	Int3 exit mask	Int2 exit mask	Int0 exit mask

1.5.6.5 Power Control Register (PCON)

PCON: SFR Address $87
Bits b7 and b3-0 cleared to 0 on reset. Bits b6-4 unused.

Bit:

7	6	5	4	3	2	1	0
Double baud rate (SMOD)	Unused (set to 0)	Unused (set to 0)	Unused (set to 0)	General purpose flag (GF1)	General purpose flag (GF0)	Power Down bit (PD)	Idle Mode bit (IDL)

PCON Register b7: Double baud rate (SMOD)
If Timer 1 is used to generate the serial port baud rate and SMOD = 1, the baud rate is doubled when the serial port is used in modes 1, 2 or 3.

PCON Register b6-4: Unused

PCON Register b3-2: General purpose flags (GF1, GF0)

PCON Register b1: Power Down bit (PD)
Setting this bit activates Power Down operation in the 8051 µC (all activity within the 8051 CPU core and interrupt/serial port/timer logic is halted). It is possible to exit Power Down (i.e. clear PCON bit 1) by applying a hardware reset to the CMX850, or by activating an interrupt which has its associated mask bit in the PDXMASK register set (whether the interrupt is enabled or not).

PCON Register b0: Idle Mode bit (IDL)
Setting this bit activates Idle Mode operation in the 8051 µC (activity within the 8051 CPU core is halted, but the interrupt/serial port/timer logic remains active). It is possible to exit Idle Mode (i.e. clear PCON bit 0) by applying a hardware reset to the CMX850, or by activating an *enabled* interrupt.

If Power Down and Idle Mode are activated simultaneously, Power Down takes precedence.

1.5.7 Pulse Width Modulators

The CMX850 has two independent 8-bit Pulse Width Modulator (PWM) circuits, each with its own PWM data register (SFRs PWM1 and PWM2) and enable bit in the PWMCON SFR. When enabled, the PWM output is automatically driven onto the relevant device pin (the PWM 1 output is driven onto pin P3.6, the PWM 2 output is driven onto pin P3.7). This is done ***without*** altering the 8051's port control SFRs. Disabling a PWM causes its output pin to immediately revert to a general-purpose port function.

The output of each PWM block is a fixed frequency square wave with a duty cycle controlled by the contents of the PWM1 or PWM2 SFR. The square wave frequency is 1/255 of the main system clock, i.e. approximately 43.4kHz if using an 11.0592MHz crystal, 48.2kHz if using a 12.288 MHz crystal, or 21.6kHz (nominal) if using the on-chip RC oscillator. The PWM output duty cycle is equal to PWM1 (or PWM2) * (100/255)%: a value of $00 will cause a permanently low output, while a value of $FF will cause a permanently high output, and a value of $13 (for example) will cause a waveform with a duty cycle of

(19*100/255) = 7.45%. The PWM blocks can be used as simple D/A converters by smoothing the outputs with suitable off-chip low-pass filters.

The contents of the PWM1 or PWM2 registers are sampled only at the beginning of each cycle of the output square wave. The microcontroller is therefore able to update the PWM1 and PWM2 registers at any time without affecting the current cycle; the change will only be seen after the current cycle has completed.

1.5.7.1 PWM Control Register (PWMCON)

PWMCON: SFR Address $DD
Bits b7-6 are cleared to 0 on reset. Other bits are unused, and are 0.

Bit:

7	6	5	4	3	2	1	0
PWM2 enable	PWM1 enable	Unused, always read as 0					

PWMCON Register b7: PWM 2 Enable

b7 = 1	Enable PWM 2
b7 = 0	Disable and reduce power PWM 2

PWMCON Register b6: PWM 1 Enable

b6 = 1	Enable PWM 1
b6 = 0	Disable and reduce power PWM 1

PWMCON Register b5-0: Unused

1.5.7.2 PWM Data Registers (PWM1, PWM2)

PWM1: SFR Address $DE
All bits cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Duty cycle for PWM 1							

PWM2: SFR Address $DF
All bits cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Duty cycle for PWM 2							

1.5.8 Analogue to Digital Converter

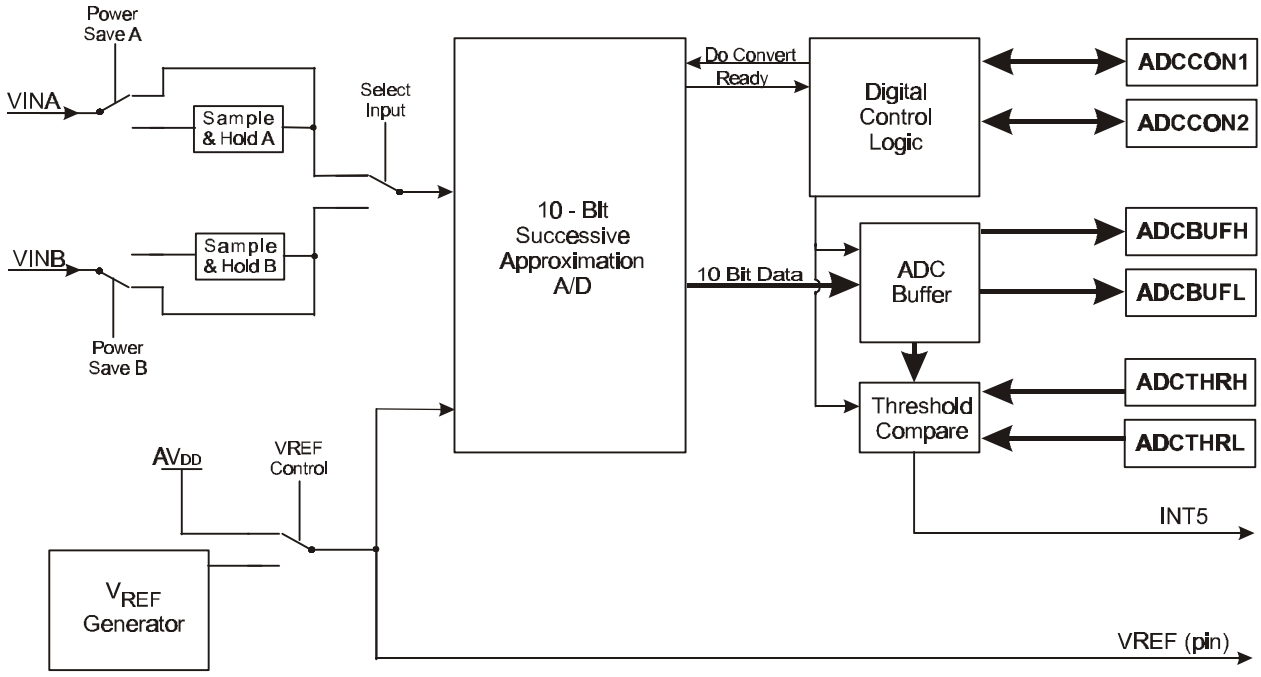


Figure 6 Analogue to Digital Converter Block Diagram

The Analogue to Digital Converter (ADC) is a 10-bit successive approximation type converter that produces an unsigned digital representation of an input voltage, selected from one of two input pins, in the range of AV_{SS} to V_{REF}. The ADC output data is stored in two SFRs, ADCBUFL and ADCBUFH. The ADC can be used to do one-shot conversions on command, or it can be used in a continuous convert mode with a selectable sample rate of up to approximately 20kHz. A digital comparator can also be enabled which will generate an interrupt request to the 8051 µC if the conversion value enters or leaves certain threshold levels, as set in the SFRs ADCTHRL and ADCTHRH. This can be used with continuous convert mode to automatically monitor a signal level, with no intervention by the 8051 µC being required.

Other features of the ADC include left- or right-hand justified conversion data, power saving features, optional on-chip track/hold circuits, and a choice between a bandgap-derived voltage reference (V_{REF} = 2.5V) or a supply reference ($V_{REF} = AV_{DD}$). The selected V_{REF} voltage is driven off chip for user reference through the VREF pin.

Note that VINA and VINB are sensitive analogue inputs, and should be carefully decoupled to AV_{SS} to reduce noise and instability in readings.

1.5.8.1 ADC Control Registers (ADCCON1/2)

The ADC has two control registers in the SFR space, ADCCON1 and ADCCON2.

When low power consumption is important and the ADC is not being used, the internal bandgap reference must be disabled by setting b2 of ADCCON1 to 0 and the track/hold circuits should both be disabled by setting b3 and b2 of ADCCON2 to 0. The 10-bit ADC converter circuit consumes no power between conversions.

ADCCON1: SFR Address $E2
All bits cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Threshold high interrupt clear	Threshold high interrupt status	Threshold low interrupt clear	Threshold low interrupt status	Inverted threshold mode	VREF control	Continuous convert enable	Manual start & status

ADCCON1 Register b7: Threshold high Interrupt clear
Writing a 1 to this bit clears ADCCON1 bit 6 (threshold high interrupt status). ADCCON1 bit 7 always reads back as a 0.

ADCCON1 Register b6: Threshold high interrupt status
At the end of each ADC conversion, bits 9-2 of the ADC output data are compared against the contents of the ADCTHRH register. Depending on the results of this comparison (see the description of the inverted threshold mode bit, ADCCON1 bit 3), this may cause the threshold high interrupt status bit to be set to 1. If this happens, the Int5 interrupt input of the 8051 µC is asserted (pulled low). Because both the threshold high and low interrupt bits are combined to drive a single interrupt line to the 8051 µC, this bit must be examined by software if it is necessary to determine which of the two threshold comparators caused the interrupt. The threshold high interrupt status bit is read-only, and can only be cleared by writing 1 to ADCCON1 bit 7.

b6 = 1	Threshold high interrupt active
b6 = 0	Threshold high interrupt inactive

ADCCON1 Register b5: Threshold low interrupt clear
Writing a 1 to this bit clears ADCCON1 bit 4 (threshold low interrupt status). ADCCON1 bit 5 always reads back as a 0.

ADCCON1 Register b4: Threshold low interrupt status
At the end of each ADC conversion, bits 9-2 of the ADC output data are compared against the contents of the ADCTHRL register. Depending on the results of this comparison (see the description of the inverted threshold mode bit, ADCCON1 bit 3), this may cause the threshold low interrupt status bit to be set to 1. If this happens, the Int5 interrupt input of the 8051 µC is asserted (pulled low). Because both the threshold high and low interrupt bits are combined to drive a single interrupt line to the 8051 µC, this bit must be examined by software if it is necessary to determine which of the two threshold comparators caused the interrupt. The threshold low interrupt status bit is read-only and can only be cleared by writing 1 to ADCCON1 bit 5.

b4 = 1	Threshold low interrupt active
b4 = 0	Threshold low interrupt inactive

ADCCON1 Register b3: Inverted threshold mode
This bit selects the conditions for setting the threshold high/low interrupt status bits at the end of an ADC conversion. It is possible to configure the comparators to indicate either when the ADC output value goes outside the range defined by ADCTHRL/ADCTHRH, or when the ADC output value enters that range (the most significant 8 bits of the ADC value are used in the comparison).

b3 = 1	Threshold high and low interrupt status both set to 1 if ADC value ≤ ADCTHRH and ≥ ADCTHRL
b3 = 0	Threshold high interrupt status set to 1 if ADC value > ADCTHRH Threshold low interrupt status set to 1 if ADC value < ADCTHRL

If ADCCON1 bit 3 = 1, then both threshold status bits (ADCCON1 bit 6 and bit 4) get set simultaneously, and must both be cleared to remove the interrupt.

It is possible to prevent the threshold high/low interrupt status bits from being set to 1 by setting ADCCON bit 3 to 0, ADCTHRH to $FF, and ADCTHRL to $00. If, however, it is desired to always generate an interrupt after a conversion (e.g. when in continuous convert mode), this can be done by setting ADCCON bit 3 to 0, and setting ADCTHRH ***lower*** than ADCTHRL.

ADCCON1 Register b2: VREF control
This bit is used to select the source of the ADC reference voltage; the selected source is also driven onto the VREF pin. If the internal track/hold circuitry is used in conjunction with AV_{DD} as a reference voltage, it may not be possible to obtain correct digital representations for input voltages that are very close to AV_{DD} itself.

b2 = 1	Use the on-chip 2.5V reference for the ADC
b2 = 0	Use AV_{DD} as the ADC voltage reference, and power save the on-chip 2.5V reference generator

ADCCON1 Register b1: Continuous convert enable
This bit is used to enable continuous convert operation, when the ADC will automatically perform conversions at a rate selected in the ADCCON2 register. This may be used in conjunction with the threshold high/low comparators to perform signal monitoring without loading the 8051 µC. If required, however, continuous convert can be used without the threshold comparator interrupt being enabled. In this case, the Status bit (ADCCON1 bit 0) will have to be polled to determine when each conversion ends. The data in the ADCBUFL and ADCBUFH registers can then be retrieved, before the next conversion begins.

b1 = 1	Continuous convert enabled
b1 = 0	Continuous convert disabled

ADCCON1 Register b0: Manual start and status
This bit is written with a 1 to start an ADC conversion (writing a 0 has no effect). It may then be read to determine when a conversion has completed, which will be within 156 cycles of the main system clock (equivalent to thirteen 8051 machine cycles or about 14.1µs if using an 11.0592MHz crystal): the status bit will read as a 1 while the conversion is taking place, and read as a 0 upon completion. During this time, the ADCBUFL and ADCBUFH registers will contain invalid data.

The status bit can also be monitored in continuous convert mode; it is set to 1 when a conversion is started, and cleared to 0 when it ends.

It is recommended that ADCCON1 bit 0 is not written with a 1 while continuous convert is enabled, since the timing of the conversions and power save operations may be affected. It may, however, be read from at any time to determine status.

ADCCON2: SFR Address $E3
All bits cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Output data left/right justify	Continuous convert sample rate			Power-save track/hold A	Power-save track/hold B	Auto power-save	Input select

ADCCON2 Register b7: Output data left/right justify
The output from the ADC is 10-bit, requiring two SFRs (ADCBUFL and ADCBUFH) to hold the data. The SFRs therefore contain 6 spare bits, which are set to 0. ADCCON2 bit 7 determines whether the 10-bit ADC conversion result is left- or right-justified within the ADCBUFL and ADCBUFH registers. If the ADC is required for 8-bit conversions only, set this bit to 0 (left-justified), and then only ADCBUFH needs to be read for the valid eight bit data, which is the most significant eight bits of the conversion.

b7 = 1	Right-justify ADC data:															
	ADCBUFH								ADCBUFL							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	(set to 0)						**ADC data bits 9-0**									

b7 = 0	Left-justify ADC data:															
	ADCBUFH								ADCBUFL							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	ADC data bits 9-0								(set to 0)							

ADCCON2 Register b6-4: Continuous convert sample rate
These three bits select the rate at which conversions are done when continuous convert is enabled.

b6	b5	b4	
0	0	1	Conversion rate = System clock frequency ÷ 8832
0	1	1	Conversion rate = System clock frequency ÷ 4416
1	0	1	Conversion rate = System clock frequency ÷ 2208
1	1	1	Conversion rate = System clock frequency ÷ 1104
X	X	0	Conversion rate = System clock frequency ÷ 552

ADCCON2 Register b3: Power-save track/hold A
This bit is used to explicitly enable the track/hold A circuit, or power save and bypass it if the track/hold function is not required or VINA is not being used. Track/hold A can also be power saved between manual conversions to minimise power consumption, in which case it should be enabled at least 25µs before a conversion is done on pin VINA. Power saving track/hold A using ADCCON2 bit 3 overrides the auto power save feature in continuous convert mode (see ADCCON2 bit 1). Hold mode is selected automatically at the start of a conversion. The track/hold circuit returns to Track mode when the conversion is complete.

b3 = 1	Enable track/hold A
b3 = 0	Power save and bypass track/hold A

ADCCON2 Register b2: Power-save track/hold B
This bit is used to explicitly enable the track/hold B circuit, or power save and bypass it if the track/hold function is not required or VINB is not being used. Track/hold B can also be power saved between manual conversions to minimise power consumption, in which case it should be enabled at least 25µs before a conversion is done on pin VINB. Power saving track/hold B using ADCCON2 bit 2 overrides the auto power save feature in continuous convert mode (see ADCCON2 bit 1). Hold mode is selected automatically at the start of a conversion. The track/hold circuit returns to Track mode when the conversion is complete.

b2 = 1	Enable track/hold B
b2 = 0	Power save and bypass track/hold B

ADCCON2 Register b1: Auto power save
This bit can be used to enable the auto power save feature when in continuous convert mode. This causes both track/hold circuits to power down between conversions, and power up again in time for each new conversion. To further save power when using continuous convert mode, the unused ADC input should have its track/hold circuit disabled using ADCCON2 bit 2 or 3.

b1 = 1	Enable auto power save for continuous convert mode
b1 = 0	Disable auto power save for continuous convert mode

ADCCON2 Register b0: Input select
Selects which of the two ADC input channels is used for a conversion. This bit should not be changed while a conversion is in progress, otherwise an invalid result will be obtained.

b0 = 1	Select pin VINB
b0 = 0	Select pin VINA

1.5.8.2 ADC Buffer Registers (ADCBUFL/H)

These two 8-bit buffer registers hold the 10-bit result from an ADC conversion. The data can be selected as left- or right-hand justified by using ADCCON2 bit 7. These registers are not cleared on reset; the data remains unknown until the first conversion is finished. The data is also invalid during each conversion.

ADCBUFL: SFR Address $E4

Bit:	7	6	5	4	3	2	1	0
Right justified:	ADC data bits 7-0							
Left justified:	ADC data bits 1-0		0	0	0	0	0	0

ADCBUFH: SFR Address $E5

Bit:	7	6	5	4	3	2	1	0
Right justified:	0	0	0	0	0	0	ADC data bits 9-8	
Left justified:	ADC data bits 9-2							

1.5.8.3 ADC Threshold Registers (ADCTHRL/H)

At the end of each ADC conversion, bits 9-2 of the ADC output data is compared against the contents of both the ADCTHRL and ADCTHRH registers, which may set the threshold high/low interrupt status bits (see the description of ADCCON1 bits 7-3).

ADCTHRL: SFR Address $E6
All bits cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
ADC low threshold value							

ADCTHRH: SFR Address $E7
All bits cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
ADC high threshold value							

1.5.9 C-BUS Controller

The C-BUS controller provides for the transfer of data and control between the 8051 µC and the DSP modem's internal registers over the C-BUS interface. The modem, described in full in section 1.6, has its own registers that must be accessed using the C-BUS controller to allow the modem to operate as required. Each transaction consists of a minimum of one byte sent from the µC, which may be followed by one or more data byte(s) sent from the µC to be written into one of the modem's Write Only Registers, or one or more byte(s) of data read out from one of the modem's Read Only Registers, as illustrated below.

The C-BUS controller is accessed by the 8051 µC through two SFRs, one for read/write data (CBUSBUF) and the other for control (CBUSCON). A transaction is initiated when the 8051 µC sets the C-BUS select bit in the CBUSCON register to 1. Command and data bytes may then be sent to the modem by writing to the CBUSBUF register, which the C-BUS controller automatically shifts out to the modem. At the same time, any reply data from the modem gets shifted back into the CBUSBUF register. To read a data byte from the modem, therefore, the 8051 µC must perform a dummy byte write to the CBUSBUF register after the initial write of a C-BUS Command to supply Reply Data. Reply data is stored in CBUSBUF every time a byte is written, but is only valid when reading a register. Setting the C-BUS select bit in the CBUSCON register to 0 terminates a transaction. The time between one transaction being terminated and another being initiated may be as small as a single 8051 machine cycle (i.e. 12 system clock cycles).

Data bytes may be written to the modem via the CBUSBUF register using back-to-back MOV instuctions. However, when reading a data byte from the modem, at least one machine cycle (e.g. a NOP instruction) must be inserted between the dummy CBUSBUF write and the CBUSBUF data read in order to give the modem time to respond. Failure to do this will result in corruption of the data being read from the modem.

The modem also generates an active low interrupt output signal, IRQN, which is configured through a C-BUS register within the modem. This IRQN signal is directly connected to the 8051 µC's Int3 interrupt input. This signal may also be polled by reading the CBUSCON register.

a) Single byte (General Reset $01)

```
MOV CBUSCON, #01h
MOV CBUSBUF, #01h
MOV CBUSCON, #00h
```

b) Write 8-bit reg (address $E3) with one data byte ($55)

```
MOV CBUSCON, #01h
MOV CBUSBUF, #0E3h
MOV CBUSBUF, #55h
MOV CBUSCON, #00h
```

c) Write 16-bit reg (address $E1) with 2 data bytes ($AC and $BC)

```
MOV CBUSCON, #01h
MOV CBUSBUF, #0E1h
MOV CBUSBUF, #0ACh
MOV CBUSBUF, #0BCh
MOV CBUSCON, #00h
```

d) Read 8-bit reg (address $E5) and store byte in Accumulator

```
MOV CBUSCON, #01h
MOV CBUSBUF, #0E5h
MOV CBUSBUF, #00h ; Dummy write
NOP
MOV A, CBUSBUF
MOV CBUSCON, #00h
```

e) Read 16-bit reg (address $E6) and store two bytes @R0

```
MOV CBUSCON, #01h
MOV CBUSBUF, #0E6h
MOV CBUSBUF, #00h ; Dummy write
NOP
MOV @R0, CBUSBUF
MOV CBUSBUF, #00h ; Dummy write
INC R0
MOV @R0, CBUSBUF
MOV CBUSCON, #00h
```

Table 5 Example of each of the five types of C-BUS transaction

1.5.9.1 C-BUS Control Register (CBUSCON)

CBUSCON: SFR Address $EA
b0 cleared to 0 on reset. b2-1 are read only.

Bit:

7	6	5	4	3	2	1	0
0	0	0	0	0	IRQ	X	C-BUS select

CBUSCON Register b7-3: Unused, set to 0

CBUSCON Register b2: IRQ
This bit is an inverted form of the IRQN output from the modem that is connected to the 8051 µC's Int3 interrupt input. This register bit is read-only.

b2 = 1	IRQN active
b2 = 0	IRQN inactive

CBUSCON Register b1: Reserved bit for internal use.
This bit is reserved for internal use; its value when read will be indeterminate.

CBUSCON Register b0: C-BUS select
This bit must be set active to enable a transaction between the 8051 µC and the modem, and taken inactive between transactions. A C-BUS transaction comprises a command byte being sent to the modem, followed by the transfer of up to two further bytes to/from the modem.

b0 = 1	C-BUS select active
b0 = 0	C-BUS select inactive

1.5.9.2 C-BUS Buffer Register (CBUSBUF)

CBUSBUF: SFR Address $EB
All bits are cleared to 0 on reset

Bit:

7	6	5	4	3	2	1	0
Bits 7-0 of buffer data							

CBUSBUF Register b7-0: C-BUS data buffer
Data written to this buffer immediately gets shifted out to the modem via the C-BUS interface, and is replaced by reply data from the modem. When reading data from the modem, an instruction (single cycle minimum) must be inserted between a CBUSBUF dummy write and the CBUSBUF data read.

1.5.10 Keyboard Encoder

The CMX850 keyboard encoder has the following features:

- Full N-key rollover, with key debounce and separate press/release indication.
- 8-character first-in first-out data buffer.
- Automatic sleep/wake-up option for low-power operation and reduced EMI.
- 8 row input pins with integral pull-up resistors.
- Between 1 and 13 column drive pins (up to 16 if using multiplexed memory interface).
- Fully autonomous operation, interrupt driven.

Enabling the keyboard encoder automatically configures the Port 1 (P1.7-0) pins as row inputs with pull-up resistors, and configures a user-selectable number of Port4 and Port5 pins as open-drain column drivers. This is done ***without*** altering the 8051's port control registers. Those port 4 and port 5 pins which are not configured as column drivers remain as general-purpose port pins. When the keyboard encoder is disabled, all column output and row input pins automatically revert to their previous general-purpose port functions.

The keyboard matrix scan period is approximately 9.3ms. The CMX850 keyboard encoder does not have an in-built facility for ghost key elimination or auto repeat generation. If these features are required, they should be performed in software by the 8051 µC.

The keyboard encoder is accessed through the KBCON, KBSTAT and KBBUF SFRs.

1.5.10.1 Keyboard Control Register (KBCON)

KBCON: SFR Address $EC
All bits are cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Enable	Auto-sleep enable	Debounce period		Number of column drivers			

KBCON Register b7: Enable

b7 = 1	Enable keyboard encoder (requires 32.768kHz clock to be active)
b7 = 0	Disable and powersave the keyboard encoder, and clear the data buffer

KBCON Register b6: Auto-sleep enable
The auto-sleep function enables the keyboard encoder to enter a low power mode after approximately 50ms of inactivity (i.e. no key pressed). The keyboard scanner automatically resumes operation when a key is pressed. Auto-sleep mode reduces power consumption and EMI in the CMX850.

b6 = 1	Enable auto-sleep
b6 = 0	Disable auto-sleep

KBCON Register b5-4: Debounce period
These bits determine for how long each key press/release is debounced before being registered. A debounce period of 3 scan cycles is normally adequate.

b5	b4	
0	0	Reserved
0	1	2 scan cycles
1	0	3 scan cycles
1	1	4 scan cycles

KBCON Register b3-0: Number of column drivers
These four bits determine how many column driver pins the keyboard encoder uses. The selected column driver pins are automatically configured as open-drain outputs when the keyboard encoder is enabled, and revert back to their previous configuration if the keyboard encoder is disabled.

b3	b2	b1	b0	
0	0	0	0	1 column driver (P4.0)
0	0	0	1	2 column drivers (P4.1-0)
0	0	1	0	3 column drivers (P4.2-0)
0	0	1	1	4 column drivers (P4.3-0)
0	1	0	0	5 column drivers (P4.4-0)
0	1	0	1	6 column drivers (P4.5-0)
0	1	1	0	7 column drivers (P4.6-0)
0	1	1	1	8 column drivers (P4.7-0)
1	0	0	0	9 column drivers (P5.0, P4.7-0)
1	0	0	1	10 column drivers (P5.1-0, P4.7-0)
1	0	1	0	11 column drivers (P5.2-0, P4.7-0)
1	0	1	1	12 column drivers (P5.3-0, P4.7-0)
1	1	0	0	13 column drivers (P5.4-0, P4.7-0)
1	1	0	1	14 column drivers (P5.5-0, P4.7-0)*
1	1	1	0	15 column drivers (P5.6-0, P4.7-0)*
1	1	1	1	16 column drivers (P5.7-0, P4.7-0)*

* Note: Port bits P5.7-5 are only available with a multiplexed memory interface (pin MUXAD = 1)

1.5.10.2 Keyboard Status Register (KBSTAT)

KBSTAT: SFR Address $ED

Bit:

7	6	5	4	3	2	1	0
Unused, always read as 0				Overflow clear	Overflow status	Sleep	Empty

KBSTAT Register b7-4: Unused

KBSTAT Register b3: Overflow clear
Writing a 1 to this bit clears KBSTAT bit 2 (overflow status). KBSTAT bit 3 always reads back as a 0.

KBSTAT Register b2: Overflow status (read-only)
This bit is set to a 1 if the 8-character keyboard data buffer KBBUF overflows, indicating that data has been lost. This register bit will then remain at logic 1 until it is cleared either by writing 1 to the overflow clear bit (KBSTAT bit 3) or by disabling the keyboard encoder using KBCON bit 7.

KBSTAT Register b1: Sleep indicator (read-only)
This bit is set to a 1 if the keyboard encoder is enabled but has entered sleep mode (this requires KBCON bit 6 to be set), otherwise the sleep indicator bit will be 0.

KBSTAT Register b0: Empty flag (read-only)
This bit will set to a 0 when the keyboard data buffer KBBUF contains information, indicating that one or more key presses or key releases have been detected, and is set to a 1 after all data has been read from KBBUF. This bit is connected to the 8051 µC's Int4 input, allowing the keyboard encoder to be interrupt driven. In this case, Int4 should be configured as a level interrupt rather than edge triggered.

1.5.10.3 Keyboard Buffer Register (KBBUF)

KBBUF: Read-only. SFR Address $EE
This read-only register contains information about the location of any key press or release that the keyboard encoder has detected. The keyboard encoder can buffer up to 8 characters; the data is retrieved by repeatedly reading the KBBUF register.

Bit:

7	6	5	4	3	2	1	0
Press / release	Row Address			Column address			

KBBUF Register b7: Key press/release indication

b7 = 1	Key press detected
b7 = 0	Key release detected

KBBUF Register b6-4: Row address
These bits indicate on which keyboard row a key press or release was detected (000 = row 0, 001 = row 1, etc).

KBBUF Register b3-0: Column address
These bits indicate on which keyboard column a key press or release was detected (0000 = column 0, 0001 = column 1, etc).

1.5.11 Watchdog Timer

The Watchdog Timer (WDT) can be used to monitor the operation of the CMX850 system. This is achieved by creating a regular WDT refresh within the software; if this refresh does not occur on time, the WDT will assume that the system has hung and will cause a system reset, preceded by an optional interrupt request to the 8051 µC.

The WDT is configured and controlled through two SFRs, WDTCON and WDTLD. The WDT can be programmed to have a wide range of timeout values: it uses the 32.768kHz reference clock, prescaled by 1, 8, 64 or 256, to increment a 16-bit counter. A watchdog timeout occurs when this counter reaches $FFFF and subsequently overflows. To prevent this happening, the application software should regularly refresh the watchdog, causing the upper eight bits of the counter to be preloaded from the WDTLD register (the lower eight bits of the counter are simultaneously reset to $00). By selecting the clock prescaler division ratio and the WDTLD register value, a timeout value of between approximately 0.0078 seconds and 8.5 minutes can be programmed. The actual timeout period in seconds can be calculated as:

Timeout period = (256-WDTLD)*Prescale/128 *(where Prescale = 1, 8, 64, or 256)*

When a WDT timeout occurs, the CMX850 will be reset immediately unless the WDT has been configured to first generate an interrupt. In that case, the active low Int8 input to the 8051 µC will be pulled down when a WDT timeout occurs. If the WDT is then not refreshed by software, the CMX850 will be reset after a further (Prescale *7.843) milliseconds, approximately. Note that if a WDT interrupt has occurred, a refresh must be performed *before* changing any of the other configuration bits in the WDTCON register; this can be done using an “ORL WDTCON,#02H” instruction. Failure to observe this precaution may cause a spurious reset to be triggered.

The optional WDT interrupt gives the µC chance to deal with a watchdog timeout before the entire chip is reset. The reset pulse generated by the WDT lasts for between three and four machine cycles.

Note that the WDT must be refreshed before being used for the first time after power up. This should be done after the WDTLD register is written and the WDT is enabled, but before the WDT is started.

1.5.11.1 Watchdog Control Register (WDTCON)

WDTCON: SFR Address $F2
WDTCON bit 2 is cleared to 0 only when the device powers up, all other bits are cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
WDT enable	WDT prescale		Delayed reset enable	0	Timeout status	Refresh	Start

WDTCON Register b7: WDT enable
The WDT enable bit is cleared to 0 whenever a reset occurs, whether from the RESETN pin or from a WDT timeout. This bit must be set to 1 to enable the clock to the WDT circuitry, which then allows the WDT to be started or refreshed.

b7 = 1	Enable WDT (requires 32.768kHz clock to be active)
b7 = 0	Disable and powersave the WDT

WDTCON Register b6-5: WDT prescale
These two bits are used to select the division ratio for the 32.768kHz clock prescaler which drives the watchdog timeout counter.

b6	b5	
0	0	Divide by 256
0	1	Divide by 64
1	0	Divide by 8
1	1	Divide by 1

WDTCON Register b4: Delayed reset enable
This bit is used to select whether a reset is generated immediately upon a WDT timeout, or whether an interrupt request is first generated. In either mode the timeout status bit is set when the timeout counter overflows and is only cleared by refreshing the WDT.

b4 = 1	Generate interrupt upon WDT timeout, then reset if the overflow is not subsequently cleared
b4 = 0	Generate reset upon WDT timeout

WDTCON Register b3: Unused, set to 0

WDTCON Register b2: Timeout status
The timeout status bit is set to 1 immediately that a WDT timeout occurs. It is not affected by a reset, but is cleared to 0 when the CMX850 first powers up (all other bits of WDTCON are cleared upon reset). This allows the software to determine whether a system reset was the result of a WDT timeout, so that appropriate action may be taken. Software can only clear the timeout status bit by refreshing the WDT.

b2 = 1	Timeout counter has overflowed
b2 = 0	No timeout has occurred

WDTCON Register b1: Refresh
Writing a 1 to this bit refreshes the WDT counter, i.e. it copies the value in the WDTLD register into the most significant eight bits of the WDT timeout counter, and sets the least significant eight bits to $00. Also, if the timeout status bit (WDTCON.2) happens to be 1, refreshing the WDT causes it to be cleared to 0. The refresh bit in the WDTCON register is automatically cleared to 0 after the refresh has happened, which occurs on the first edge of the 32.768kHz clock after the refresh bit is set to a 1.

WDTCON Register b0: Start
The bit is used to start or stop the WDT. To start the WDT, the WDTCON enable bit must be set to 1 and the 32.768kHz reference clock must be running.

b0 = 1	Start the WDT
b0 = 0	Stop the WDT

1.5.11.2 Watchdog Load Register (WDTLD)

WDTLD: SFR Address $F3
All bits are cleared to 0 on reset.

This register is used to store the most significant eight bits of the timeout counter preload value. The timeout counter is preloaded with this value when a WDT refresh is applied. The least significant eight bits of the timeout counter are always preloaded with $00.

Bit:

7	6	5	4	3	2	1	0
Bits 15 - 8 of timeout counter preload value							

1.5.12 Real Time Clock

The Real Time Clock (RTC) is an accurate long period timer that uses the 32.768kHz reference clock within the CMX850. The 32-bit binary rollover counter increments once per second, and is very suitable for storing a real time and date using an appropriate software algorithm. The RTC can also generate a regular interrupt request, the repetition rate being selectable between one sixteenth of a second and eight seconds. The RTC has an alarm feature, which is programmed using a separate 32-bit register.

1.5.12.1 RTC Control Register (RTCCON)

RTCCON: SFR Address $FB
This register enables and controls the RTC and allows the selection of the time interval between regular interrupts.

Bits 7 and 3 of this register are not affected by a reset. All other bits are cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
RTC enable	Prescale reset	Time interrupt clear	Time interrupt status	Clock disable	Time interrupt interval select		

RTCCON Register b7: RTC enable
This bit is used to enable the RTC. It is not affected by a reset; when the CMX850 powers up its value is unknown and it should be set or cleared as required.

b7 = 1	Enable the RTC
b7 = 0	Disable and powersave the RTC

RTCCON Register b6: Prescale reset
The RTC has an internal “fractions of a second” clock prescaler that divides down the 32.768kHz reference clock to provide pulses for the time interrupt request logic and a 1Hz reference signal for the RTC. This prescaler is normally free running, but can be reset and held using this register bit to allow the time value in the RTC to be precisely synchronised to an external time signal.

b6 = 1	Reset and hold internal clock prescaler at zero
b6 = 0	Allow the RTC clock prescaler to operate

RTCCON Register b5: Time interrupt clear
Writing a 1 to this bit clears RTCCON bit 4 (time interrupt status). RTCCON bit 5 always reads back as a 0.

RTCCON Register b4: Time interrupt status
This bit indicates whether a time interrupt has occurred. Its inverse is used to drive the (active low) Int6 interrupt line to the 8051 µC. The time interrupt status bit cannot be written directly by the 8051 µC, but it can be cleared by writing a 1 to RTCCON bit 5. If the time interrupt feature is not required, it should be disabled by clearing the time interrupt enable bit (IE_1 bit 4), and RTCCON bit 4 should be ignored.

b4 = 1	Selected time interval has elapsed, time interrupt active
b4 = 0	Time interrupt inactive

RTCCON Register b3: Clock disable
This bit can be used to prevent the main RTC time counter from incrementing. This is recommended when setting the TIME0/1/2/3 registers to prevent them from incrementing while being set. This bit does not affect the internal fractions of a second prescaler or the time interval interrupts. This bit is not affected by a reset; when the CMX850 powers up its value is unknown and it should be set or cleared as required.

b3 = 1	Prevent the RTC TIME registers from incrementing
b3 = 0	Allow the RTC TIME registers to increment

RTCCON Register b2-0: Time IRQ Interval Select
These 3 bits select the frequency of time interrupt requests.

b2	b1	b0	
0	0	0	Sixteenth of a second interval
0	0	1	Eighth of a second interval
0	1	0	Quarter of a second interval
0	1	1	Half of a second interval
1	0	0	One second interval
1	0	1	Two second interval
1	1	0	Four second interval
1	1	1	Eight second interval

1.5.12.2 RTC Time Registers (TIME0-TIME3)

The RTC stores the time in four SFRs: TIME0, TIME1, TIME2 and TIME3. Each register holds eight bits, with TIME0 holding the least significant eight bits and TIME3 holding the most significant eight bits.

RTC TIME0: SFR Address $FC
All bits unaffected by reset.

Bit:

7	6	5	4	3	2	1	0
Bits 7 - 0 of RTC TIME register							

RTC TIME1: SFR Address $FD
All bits unaffected by reset.

Bit:	7	6	5	4	3	2	1	0
	Bits 15 - 8 of RTC TIME register							

RTC TIME2: SFR Address $FE
All bits unaffected by reset.

Bit:	7	6	5	4	3	2	1	0
	Bits 23 - 16 of RTC TIME register							

RTC TIME3: SFR Address $FF
All bits unaffected by reset.

Bit:	7	6	5	4	3	2	1	0
	Bits 31 - 24 of RTC TIME register							

To use the clock features, bit 7 of RTCCON is set to 1 to enable the RTC. Then bit 3 of RTCCON is set to 1 to stop the clock counter. The four RTC TIME registers can now be written with the required value in seconds, which can be used to represent a time and date with a suitable software algorithm. Once the required value is stored, the clock can be started by clearing bit 3 of RTCCON. Once the time is set and the clock enabled the value stored will be incremented once every second. The RTC operation will not be suspended when a reset occurs as bits 7 and 3 of RTCCON are unaffected by a reset, so the time will continue to be incremented once every second.

If the prescale reset (RTCCON bit 6) is set to 1 before the clock is started, then immediately set back to 0 after the clock is started, the internal fractions of a second will be reset to zero and the first increment of the clock will occur after 1 second. However, if the time interrupt feature is already being used as described in the RTC Control Register section above, and it is required to be accurate and continuous, then the “fractions of a second” prescaler must remain running and the prescale reset must not be used. In this case the first increment of the clock will be synchronised to the already continuously running fractions of a second.

Note: to read the current 32-bit time value requires four reads, one from each of the four time registers. Since each read takes a finite time there is a small probability that the time value may be incremented between register reads, giving erroneous results. It is therefore recommended that the 32-bit time value be read repeatedly until two successive 32-bit results match (this will normally happen after the first pair of 32-bit reads). The value read will then be correct.

1.5.12.3 RTC Alarm Registers (ALM0-ALM3)

The RTC stores the alarm time in four SFRs: ALM0, ALM1, ALM2 and ALM3. Each register holds eight bits, with ALM0 holding the least significant eight bits and ALM3 holding the most significant eight bits. Using the alarm facility is simply a case of setting the required alarm time in ALM0…3. The RTC waits until the current 32-bit time value is equal to or greater than the 32-bit alarm time, then on the next active edge of the 32.768kHz clock will assert the Int7 interrupt line to the 8051 µC (i.e. drive it low). As it is recommended that Int7 be configured as a level sensitive interrupt, it is the responsibility of the interrupt service routine to clear the alarm interrupt request either by clearing IE_1 bit 5 or by writing a new 32-bit alarm value to the ALM0…3 SFRs (writing to any of the ALM0…3 registers negates the Int7 signal). If this is not done, the alarm interrupt will re-trigger upon exit of the service routine.

Note that a spurious interrupt request may be generated as the ALM0…3 registers are being updated by software, since four write operations are needed. It is therefore recommended that the alarm interrupt enable bit (IE_1 bit 5) be cleared whenever the ALM0…3 registers are being modified.

There is no status bit in RTCCON for the alarm interrupt signal, therefore should it be necessary to poll the alarm interrupt it must be done from the flag bit in the interrupt control register ICON1B.

ALM0: SFR Address $F4
All bits unaffected by reset.

Bit:	7	6	5	4	3	2	1	0
	Bits 7 - 0 of RTC ALM register							

ALM1: SFR Address $F5
All bits unaffected by reset.

Bit:	7	6	5	4	3	2	1	0
	Bits 15 - 8 of RTC ALM register							

ALM2: SFR Address $F6
All bits unaffected by reset.

Bit:	7	6	5	4	3	2	1	0
	Bits 23 - 16 of RTC ALM register							

ALM3: SFR Address $F7
All bits unaffected by reset.

Bit:	7	6	5	4	3	2	1	0
	Bits 31 - 24 of RTC ALM register							

1.5.13 CAS Tone and FSK Detector for CLI/CIDCW

The CAS (CPE alerting signal) tone and FSK detector circuit is driven from the CMX850's line input amplifier. It provides the ability to detect CAS tones (a burst of simultaneous 2130Hz and 2750Hz signals) or to receive FSK signals and to convert them to either bits or bytes of data. The detector operates with low power consumption and with improved Tone Alert performance in the presence of near-end signals, making it particularly suitable for off-hook CIDCW (Calling Identity on Call Waiting) detection.

Note that the CAS/FSK detector uses the same V_{BIAS} generator and line input amplifier as the modem, but is otherwise independent of the modem operation; both can be enabled simultaneously. This may be useful in certain applications, for example when it is necessary to simultaneously look for both DTMF and FSK signals.

The CAS/FSK detector is accessed through the CASDET and FSKBUF SFRs.

1.5.13.1 CAS Tone Detector

The detector will function as a CAS Tone Alert detector when the Mode bit (CASDET b6) is set to 0. When in this mode, the Detect bit (CASDET b0) will be set high while a Tone Alert signal is detected. If the Detect signal stays high for a time within the CAS qualifying time TqCAS (see section 1.7.1.3), then on the falling edge of the Detect signal the interrupt status bit in the CASDET SFR will go high. This also asserts the Int2 signal to the 8051 µC. The action of writing a 1 to the CAS Tone interrupt clear bit in CASDET generates a short pulse that clears the interrupt status bit. The TqCAS timing is selectable, allowing detection of up to 135 ms Tone Alert (CAS) signals, but is mainly optimised for detection of 75 to 85 ms Tone Alert (CAS) signals used in off-hook applications.

Note that Tton added to TqCAS determines the range of times for which the tones should be present for a CAS interrupt to be generated. The TqCAS time range is selected through the Tone Detect Window Control bits in the CASDET SFR. See section 1.7.1.3 for definitions of Tdon and Tdoff and TqCAS.

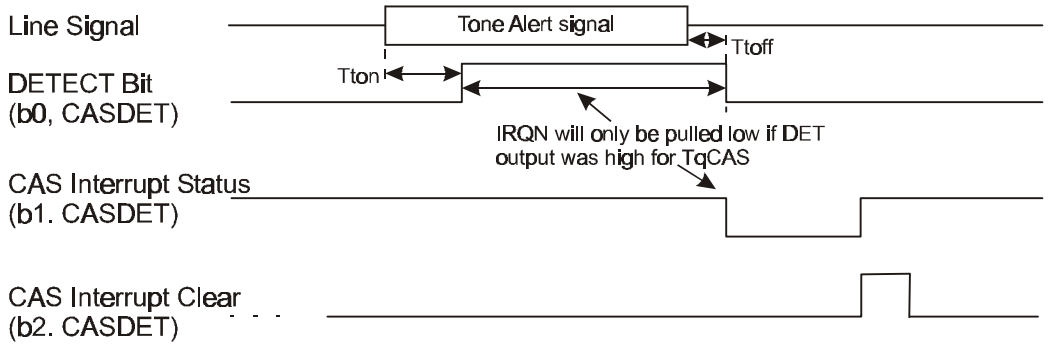


Figure 7a CAS Tone Alert Detector Operation

1.5.13.2 FSK Detector

The detector will function as a 1200 baud FSK receiver when the Mode bit (CASDET b6) is set to a 1. When in this mode, the detect bit (CASDET b0) will be set high when the FSK signal has exceeded a preset threshold for sufficient time. Amplitude and time hysteresis are used to reduce chattering on the detect bit in marginal conditions.

Note that in FSK receive mode the detector may also respond to non-FSK signals such as speech.

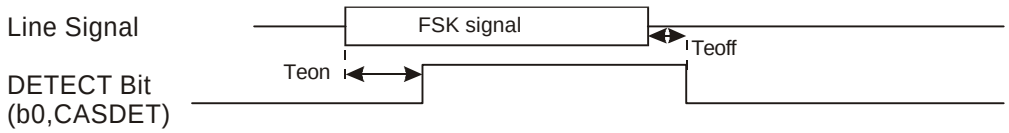


Figure 7b FSK Level Detector Operation

1.5.13.3 FSK Demodulator

When FSK mode is selected (CASDET b6 = 1) the received signal is processed by an FSK demodulator. What happens to the output of this demodulator depends on whether “bit” mode or “byte” mode operation is selected.

In bit mode (CASDET b3 = 1) the demodulator output is directly connected to b7 of FSKBUF and the interrupt status bit in the CASDET SFR is tied low (inactive). The user can therefore directly access the FSK signal by polling b7 of the FSKBUF register.

In byte mode (CASDET b3 = 0) the FSKBUF register will be indeterminate until the FSK retiming logic has extracted a valid character (8 data bits framed by a start and a stop bit). When a valid character has been received, the 8 data bits are loaded into FSKBUF and the interrupt status bit in the CASDET SFR goes high, which also asserts the Int2 signal to the 8051 µC. This alerts the user to read the FSKBUF register. As soon as FSKBUF has been read by the 8051 µC, the interrupt is immediately cleared, and the FSKBUF register will again become indeterminate until the next character is received. It should be noted that for correct operation it is necessary to read the FSKBUF register within approximately 8.3ms (the time of a complete character at 1200 baud) otherwise the data will be lost and replaced by the next valid byte of data.

If byte mode is enabled during an FSK Channel Seizure signal (a sequence of alternating mark and space bits) it will interpret the signal as valid receive characters, with values of 55 (hex). Similarly it may interpret speech or other signals as random characters.

1.5.13.4 Detect Control Register (CASDET)

CASDET: SFR Address $E9
All Bits are cleared to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Detector Enable	Mode = CAS (0)	CAS Tone Detect Window Control			CAS Interrupt clear	Interrupt status	Detect
	Mode = FSK (1)	0	0	Bit Mode Select	0		

CASDET Register b7: Detector enable
This bit is used to enable the CAS/FSK detector circuit, and to power up the V_{BIAS} generator and line input amplifier in the modem circuit (if not already powered up).

b7 = 1	Enable detector
b7 = 0	Disable and powersave the detector

CASDET Register b6: Mode Select
This bit is used to select either CAS Tone Alert Mode or FSK Receiver Mode. The state of this bit determines the function of the remaining bits in this register.

b6 = 1	FSK Receiver Mode
b6 = 0	CAS Tone Alert Mode

CASDET Register b5-3 (In CAS Mode): Tone Detect Window Control
CASDET Register b5-3 (In FSK Mode): Bit Mode Select

In CAS mode, the tones being detected are required to last between certain time limits before being considered as valid CAS tones. This time window can be programmed by these register bits to give nominal values, as shown below. The detect window will always start at 65 ms but can be configured to finish between 100 ms and 135 ms in 5 ms divisions.

In FSK mode these bits are used to configure the FSK demodulator into bit mode or byte mode (see description in section 1.5.13.3).

CAS MODE

b5	b4	b3	
0	0	0	Valid Detect Tone Length 65 – 100 ms
0	0	1	Valid Detect Tone Length 65 – 105 ms
0	1	0	Valid Detect Tone Length 65 – 110 ms
0	1	1	Valid Detect Tone Length 65 – 115 ms
1	0	0	Valid Detect Tone Length 65 – 120 ms
1	0	1	Valid Detect Tone Length 65 – 125 ms
1	1	0	Valid Detect Tone Length 65 – 130 ms
1	1	1	Valid Detect Tone Length 65 – 135 ms

FSK MODE

b5	b4	b3	
0	0	0	FSK byte mode
0	0	1	FSK bit mode

CASDET Register b2 (In CAS Mode): CAS interrupt clear
CASDET Register b2 (In FSK Mode): Unused, set to 0

In CAS mode, writing a 1 to this bit generates a short pulse that clears CASDET bit 1 (CAS interrupt status). CASDET bit 2 always reads back as a 0.

CASDET Register b1: Interrupt status (read-only)
In CAS Tone Alert mode this bit indicates whether CAS tones of the correct duration have been received. In FSK Receive mode it indicates that a complete byte is ready to read from FSKBUF (assuming byte mode has been selected). The inverse of this bit is used to drive the (active low) Int2 interrupt line to the 8051 µC. The Interrupt status bit cannot be written directly by the 8051 µC, but it can be cleared by writing a 1 to CASDET bit 2 in CAS Tone Alert Mode, or by reading the FSKBUF register in FSK Mode. The 8051 µC can enable or disable the the interrupt by setting or clearing the Int2 enable bit (IE_1 bit 0).

b1 = 1	Interrupt active (CAS tone detected with correct duration or FSK byte ready)
b1 = 0	Interrupt inactive

CASDET Register b0: Detect (read-only)
In CAS Tone Alert mode, this bit shows when valid CAS tones are being received, see figure 7a. In FSK Receive mode it shows when valid FSK tones are being received, see figure 7b. This bit can be monitored during a CLI message transaction to minimise falsing, as described in section 1.5.13.6.

b0 = 1	FSK signal or CAS tone pair present
b0 = 0	FSK signal or CAS tone pair not present

1.5.13.5 FSK Buffer Register (FSKBUF)

FSKBUF: Read-only. SFR Address $D1
All bits are cleared to 0 on reset.

Bit:

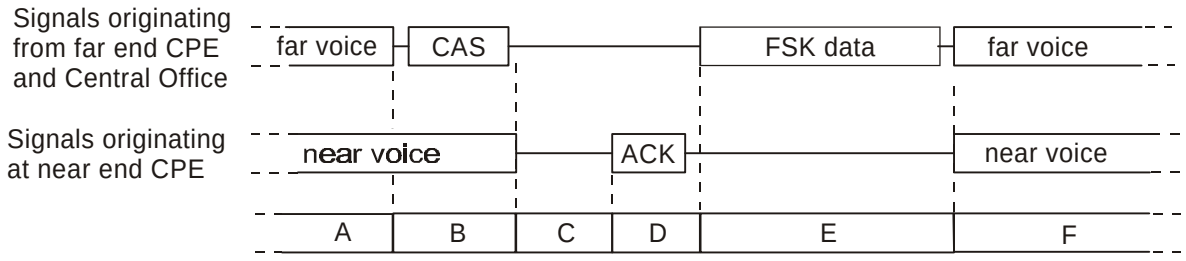
7	6	5	4	3	2	1	0
FSKBuffer Bit 7 or FSK Demodulator O/P	FSK Buffer Bits 6-0						

FSKBUF Register b7: FSK Buffer Bit 7 or FSK Demodulator Output
When using FSK bit mode, this bit is permanently connected to the FSK demodulator output. In byte mode, this bit will only be valid when a valid byte has been received. This bit will then hold bit 7 of the received byte until it has been read by the user, then the bit will become indeterminate until the next valid byte is stored.

FSKBUF Register b6-0: FSK Buffer Bits 6-0
These bits are only valid when FSK byte mode is enabled and the interrupt status bit (CASDET b1) is high to indicate that a valid FSK byte has been received. The received byte is stored in FSKBUF b7-0 until it is read by the 8051 µC (see section 1.5.13.3).

1.5.13.6 Example of Using the Detector for Off Hook operations

The CASDET block uses the V_{BIAS} generator and line input amplifier within the modem, but is otherwise independent of the modem operation. On receipt of a valid CAS Tone Alert, it will be necessary for the 8051 µC to "wake up" the modem and sent the necessary acknowledgement. In this example FSK data is sent from the Central Office, so either the modem or the alternative FSK demodulator can be used for the subsequent data reception. If it is not known whether FSK or DTMF is being used for the data transfer, then the modem can be set to receive DTMF while the CAS /FSK Detector is set to Mode 1 to receive FSK. An example of a message transaction is shown in figure 7c.



A. Normal conversation with both near and far end voice present.
B. Central Office mutes far end voice, sends CAS and becomes silent.

C. CAS Tone Alert detected and interrupt generated, which causes the CMX850 to mute near end voice, and check that no further CAS tones are detected for 50ms (to minimise falsing)
D. Modem set up to send ACK to Central Office to signal readiness to receive FSK data.
E. Central Office recognises ACK and sends FSK data. The CMX850 is set up to receive the FSK data.
F. The Transaction is complete. The CMX850 unmutes the near voice, and reverts back to its origianal mode, while the central office unmutes the far end voice, normal conversation returns.

Figure 7c Typical off-hook (Type 2) message transaction

1.5.14 8051 Accumulator, Flags and Stack Pointer

1.5.14.1 Accumulator Registers (A,B)

A (ACC): SFR Address $E0
All bits reset to 0 on reset. This register is bit addressable.

Bit:

7	6	5	4	3	2	1	0
Bits 7 – 0 of the A register							

The main accumulator register A is used in a large number of register-specific arithmetic, logical and data transfer instructions. No address byte is needed to point to it, the opcode itself does that. Instructions that refer to the main accumulator as A assemble as accumulator-specific instructions.

The A register is also mapped into the 8051 SFR space, and can be read or written using direct addressing. Instructions that refer to the accumulator as ACC will access the accumulator using direct addressing. For example, the instructions MOV R0,A and MOV R0,ACC will both copy the contents of the accumulator to register R0, but will assemble as different opcodes – in this example the main difference is that the instruction MOV R0,A assembles as a 1 byte opcode rather than 2, and executes in 1 machine cycle rather than 2.

B: SFR Address $F0
All bits reset to 0 on reset. This register is bit addressable.

Bit:

7	6	5	4	3	2	1	0
Bits 7 – 0 of the B register							

Register B is mapped into the 8051 SFR space, but is also used implicitly in the MUL AB and DIV AB instructions. The B register is commonly used by programmers as an auxiliary register to store temporary data.

1.5.14.2 Program Status Word Register (PSW)

PSW: SFR Address $D0
All bits reset to 0 on reset. This register is bit addressable.

Bit:

7	6	5	4	3	2	1	0
Carry flag (CY)	Auxiliary Carry flag (AC)	General purpose flag 0 (F0)	Register bank select 1 (RS1)	Register bank select 0 (RS0)	Overflow flag (OV)	General purpose flag 1 (F1)	Parity flag (P)

PSW Register b7: Carry flag (CY)
During ADD, ADDC or SUBB instructions, this bit gets set if there is a carry-out from bit 7, and cleared otherwise. The Carry flag is also affected by certain other arithmetic, logical and program branching instructions, and also acts as a single bit “accumulator” for a number of the Boolean manipulation instructions.

PSW Register b6: Auxiliary Carry flag (AC)
During ADD, ADDC or SUBB instructions, this bet gets set if there is a carry-out from bit 3, and cleared otherwise. Gets used by the DAA instruction.

PSW Register b5: General purpose flag 0 (F0)

PSW Register b4-3: Register Bank Select bits (RS1, RS0)
These bits are used to select one of the four register banks.

b4	b3	
0	0	Bank 0 selected, R0-7 mapped to hex address $00-$07
0	1	Bank 1 selected, R0-7 mapped to hex address $08-$0F
1	0	Bank 2 selected, R0-7 mapped to hex addresss $10-$17
1	1	Bank 3 selected, R0-7 mapped to hex address $18-$1F

PSW Register b2: Overflow flag (OV)
During ADD, ADDC or SUBB instructions, this bit gets set to indicate the sign of the result (i.e. ACC bit 7) is incorrect and is cleared otherwise. This assumes that the two operands are signed integers in the range –128 to 127. More specifically, an overflow occurs if there is a carry-out from bit 6 but not bit 7, or a carry-out from bit 7 but not bit 6. If the two operands are assumed to be unsigned integers in the range 0-255, the overflow flag can be ignored.

The overflow flag also gets set by the MUL AB instruction if the product is greater than 255, otherwise it is cleared. The DIV AB instruction always clears the overflow flag.

PSW Register b12: General purpose flag (F1)

PSW Register b0: Parity flag (P)
Set/cleared by hardware each instruction cycle to indicate an odd/even number of “1” bits in accumulator A.

1.5.14.3 Stack Point Register (SP)

SP: SFR Address $81
Bits b7-3 cleared to 0 on reset. Bits b2-0 set to 1 on reset.

Bit:

7	6	5	4	3	2	1	0
Bits 7 – 0 of the SP register							

The SP register is used as a pointer to the top of the stack area within the 256-byte local RAM. Temporary program data can be stored and retrieved from the stack using the PUSH and POP instructions. When data is pushed onto the stack, the stack pointer is incremented *before* the data is written. When data is popped off the stack, the stack pointer is decremented *after* the data is read. The stack also gets used to automatically store the 2-byte return address for subroutine calls and interrupt routines: the low-order byte of the return address gets pushed onto the stack first, then the high order byte.

Stack accesses use indirect addressing to the local RAM, which means that all 256 bytes of the local RAM can be utilised by the stack.

1.5.15 Timers and Serial Port

1.5.15.1 Timer/Counter Control Register (TCON)

TCON: SFR Address $88
All bits reset to 0 on reset. This register is bit addressable.

Bit:

7	6	5	4	3	2	1	0
Timer 1 overflow flag (TF1)	Timer 1 run control (TR1)	Timer 0 overflow flag (TF0)	Timer 0 run control (TR0)	Int1 edge flag (IE1)	Int1 type control (IT1)	Int0 edge flag (IE0)	Int0 type control (IT0)

TCON Regsiter b7: Timer 1 overflow flag (TF1)
The Timer 1 overflow flag gets set to 1 by hardware when Timer 1 overflows, and gets cleared automatically when the Timer 1 interrupt service routine is called.

TCON Register b6: Timer 1 run control bit (TR1)

b6 = 1	Turn Timer/Counter 1 on
b6 = 0	Turn Timer/Counter 1 off

TCON Register b5: Timer 0 overflow flag (TF0)
The Timer 0 overflow flag gets set to 1 by hardware when Timer 0 overflows, and gets cleared automatically when the Timer 0 interrupt service routine is called.

TCON Register b4: Timer 0 run control bit (TR0)

b4 = 1	Turn Timer/Counter 0 on
b4 = 0	Turn Timer/Counter 0 off

TCON Register b3: Int1 edge flag (IE1)
When Int1 is configured as falling edge triggered, this bit is set to 1 by hardware to indicate that an edge has been detected (i.e. successive samples of the Int1 pin show a high in one machine cycle and a low in the next cycle) and gets cleared automatically when the Int1 service routine is called. When configured as a low level triggered interrupt, the edge flag will be updated once per cycle to reflect the state of the Int1 pin; the flag gets set to 1 if the Int1 pin is active (i.e. low), and gets cleared to 0 if the Int1 pin is inactive (high).

TCON Register b2: Int1 type control (IT1)

b2 = 1	Int1 configured as a falling edge triggered interrupt
b2 = 0	Int1 configured as a low level triggered interrupt.

TCON Register b1: Int0 edge flag (IE0)
When Int0 is configured as falling edge triggered, this bit is set to 1 by hardware to indicate that an edge has been detected (i.e. successive samples of the Int0 pin show a high in one machine cycle and a low in the next cycle) and gets cleared automatically when the Int0 service routine is called. When configured as a low level triggered interrupt, the edge flag will be updated once per cycle to reflect the state of the Int0 pin: the flag gets set to 1 if the Int0 pin is active (i.e. low), and gets cleared by 0 if the Int0 pin is inactive (high).

TCON Register b0: Int0 type control (IT0)

b0 = 1	Int0 configured as a falling edge triggered interrupt
b0 = 0	Int0 configured as a low level triggered interrupt.

1.5.15.2 Timer/Counter Mode Register (TMOD)

TMOD: SFR Address $89
All bits reset to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Timer 1 gate	Timer 1 C/T control	Timer 1 mode select 1	Timer 1 mode select 0	Timer 0 gate	Timer 0 C/T control	Timer 0 mode select 1	Timer 0 mode select 0

TMOD Register b7: Timer 1 gate

b7 = 1	Timer/Counter 1 only runs while TCON.6 (TR1) = 1 and Int1 is high (hardware control)
b7 = 0	Timer/Counter 1 only runs while TCON.6 (TR1) = 1 (software control)

TMOD Register b6: Timer 1 C/T control

b6 = 1	Counter operation (input from T1 input pin)
b6 = 0	Timer operation (input from internal system clock)

TMOD Register b5-4: Timer 1 mode select

b5	b4	
0	0	13-bit timer/counter (TH1 = 8-bit counter, TL1 = 5-bit prescaler)
0	1	16-bit timer/counter
1	0	8-bit Auto-reload timer/counter (TH1 = reload value, TL1 = 8-bit counter)
1	1	Does not run

TMOD Register b3: Timer 0 gate

b3 = 1	Timer/Counter 0 only runs while TCON.4 (TR0) = 1 and Int0 is high (hardware control)
b3 = 0	Timer/Counter 0 only runs while TCON.4 (TR0) = 1 (software control)

TMOD Register b2: Timer 0 C/T control

b2 = 1	Counter operation (input from T0 to input pin)
b2 = 0	Timer operation (input from internal system clock)

TMOD Register b1-0: Timer 0 mode select

b1	b0	
0	0	13-bit timer/counter (TH0 = 8-bit counter, TL0 = 5-bit prescaler
0	1	16-bit timer/counter
1	0	8-bit Auto-reload timer (TH0 = reload value, TL0 = 8-bit counter)
1	1	Two 8-bit timers, TL0 and TH0: TL0 uses timer 0 control bits, TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1, TF1 and the Timer 1 interrupt.

1.5.15.3 Timer/Counter Registers (TL0, TL1, TH0, TH1)

TL0: SFR Address $8A - All bits reset to 0 in reset

Bit:

7	6	5	4	3	2	1	0
Timer/Counter 0 low byte							

TL1: SFR Address $8B
All bits reset to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Timer/Counter 1 low byte							

TH0: SFR Address $8C
All bits set to 0 on reset.

Bit:

7	6	5	4	3	2	1	0
Timer/Counter 0 high byte							

TH1: SFR Address $8D
All bits reset to 0 on reset

Bit:

7	6	5	4	3	2	1	0
Timer/Counter 1 high byte							

1.5.15.4 Serial Port Control Register (SCON)

SCON: SFR Address $98
All bits reset to 0 on reset. This register is bit addressable.

Bit:

7	6	5	4	3	2	1	0
Serial port mode select 0 (SM0)	Serial port mode select 1 (SM1)	Serial port mode select 2 (SM2)	Serial port receive enable (REN)	9th transmit data bit (TB8)	9th received data bit (RB8)	Transmit interrupt flag (TI)	Receive interrupt flag (RI)

SCON Register b7-6: Serial port mode select 0-1 (SM0, SM1)

b7	b6	
0	0	Serial port mode 0 (shift register, baud rate = $f_{osc}/12$)
0	1	Serial port mode 1 (8-bit UART, baud rate = variable)
1	0	Serial port mode 2 (9-bit UART, baud rate = $f_{osc}/64$ or $f_{osc}/32$)
1	1	Serial port mode 3 (9-bit UART, baud rate = variable)

In mode 1 or 3 the baud rate is generated by Timer 1, according to the formula

$$\text{Baud Rate} = (K * f_{osc}) / (32 * 12 * (256-TH1))$$

Where K = 1 if SMOD = 0, and K = 2 if SMOD = 1 (SMOD is bit 7 of the PCON register). The frequency of f_{osc} is that of the main xtal oscillator divided by the clock speed reduction programmed into bits 0-2 of the SPDCON register ($9D). f_{osc} is used to count or time the values programmed into Timer 0 and Timer 1.

SCON Register b5: Serial port mode select 2 (SM2)

Enables the multiprocessor communications feature in modes 2 and 3: if SM2 = 1 then RI will not be activated if the 9th received data bit (RB8) is 0. In mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In mode 0, SM2 should be 0.

SCON Register b4: Serial port receive enable (REN)

b4 = 1	Enable serial reception
b4 = 0	Disable serial reception

SCON Register b3: 9th transmitted data bit (TB8)

In modes 2 and 3, this is the 9th data bit that will be transmitted. Set or cleared by software as desired.

SCON Register b2: 9th received data bit (RB8)

In modes 2 and 3, this is the 9th data bit that was received. In mode 1, if SM2 = 0, this is the stop bit that was received. In mode 0, this bit is not used.

SCON Register b1: Transmit interrupt flag (TI)

Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in other modes, in any serial transmission. Must be cleared by software.

SCON Register b0: Receive interrupt flat (RI)

Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in other modes, in any serial reception (except see SM2). Must be cleared by software.

1.5.15.5 Serial Port Buffer Register (SBUF)

SBUF: SFR Address $99

All bits indeterminate on reset.

Bit:

7	6	5	4	3	2	1	0
Bits 7-0 of the SBUF register							

The serial port is full duplex, i.e. it can transmit and receive simultaneously. The transmit and receive registers are both accessed through the SBUF SFR. Reading SBUF will access the serial port receive register (the serial port has a one-byte deep receive buffer, allowing reception of a second byte to commence before the previously received byte has been read). Writing to SBUF initiates a serial port transmission.

1.6 Modem General Description

The Modem transmit and receive operating modes are independently programmable.

The transmit mode can be set to any one of the following:

V.22 bis modem. 2400bps QAM (Quadrature Amplitude Modulation).

V.22 and Bell 212A modem. 1200 or 600 bps DPSK (Differential Phase Shift Keying).

V.21 modem. 300bps FSK (Frequency Shift Keying).

Bell 103 modem. 300bps FSK.

V.23 modem. 1200 or 75 bps FSK.

Bell 202 modem. 1200 or 150 bps FSK.

DTMF transmit.

Single tone transmit (from a range of modem calling, answer and other tone frequencies)

User programmed tone or tone pair transmit (programmable frequencies and levels)

Disabled.

The receive mode can be set to any one of the following:

V.22 bis modem. 2400bps QAM.

V.22 and Bell 212A modem. 1200 or 600 bps DPSK.

V.21 modem. 300bps FSK.

Bell 103 modem. 300 bps FSK.

V.23 modem. 1200 or 75 bps FSK.

Bell 202 modem. 1200 or 150 bps FSK.

DTMF detect.

2100Hz and 2225Hz answer tone detect.

Call progress signal detect.

User programmed tone or tone pair detect.

Disabled.

The Modem may also be set into a Powersave mode which disables all circuitry except for the C-BUS interface, the Ring Detector and the Hook Detector.

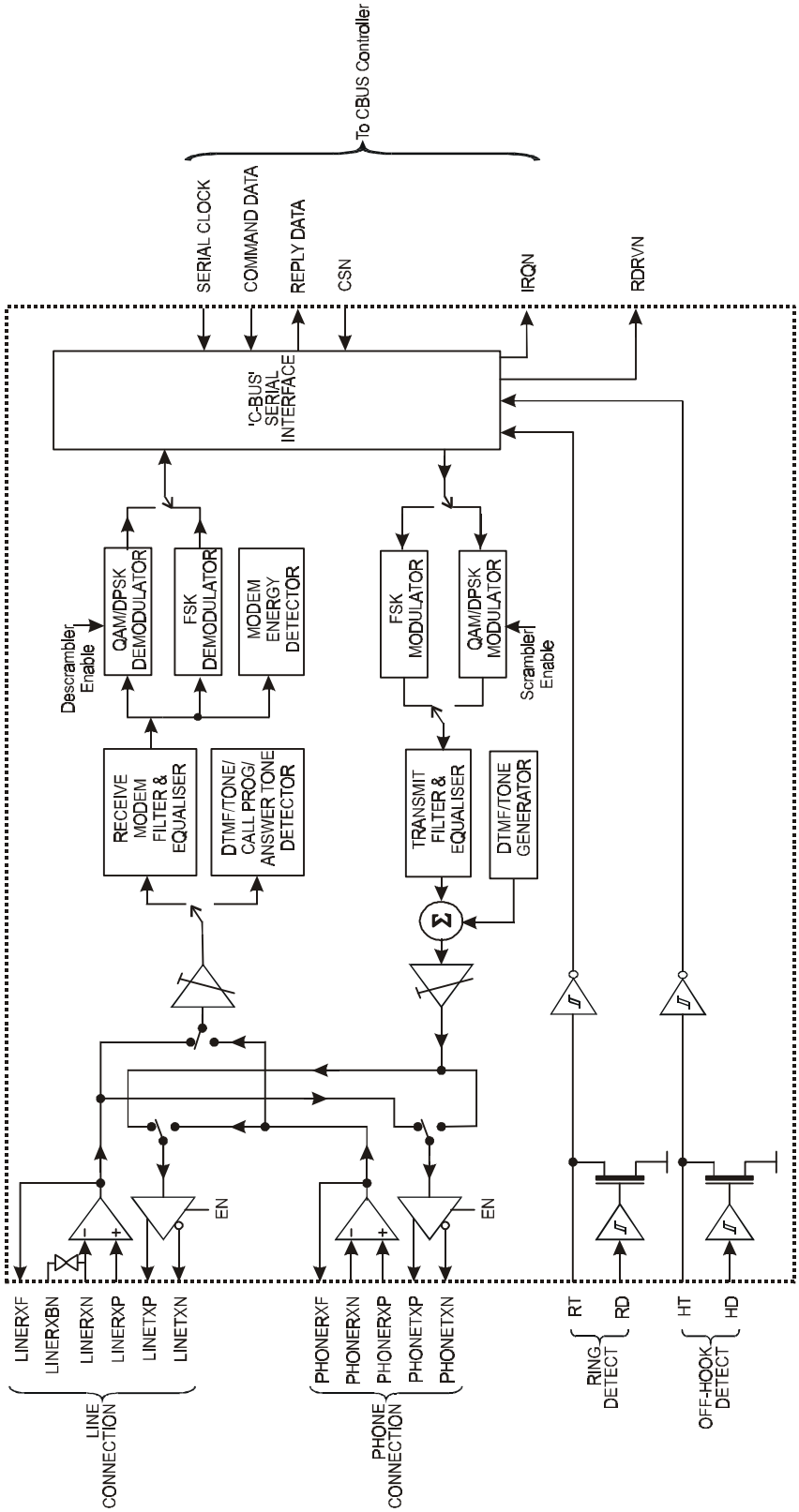


Figure 8 Modem Block Diagram

1.6.1 Tx USART

A flexible Tx USART is provided for all modem modes, meeting the requirements of V.14 for QAM and DPSK modems.

It can be programmed to transmit continuous patterns, Start-Stop characters or Synchronous Data.

In both Synchronous Data and Start-Stop modes the data to be transmitted is written by the µC into the 8-bit C-BUS Tx Data Register from which it is transferred to the Tx Data Buffer.

If Synchronous Data mode has been selected the 8 data bits in the Tx Data Buffer are transmitted serially, b0 being sent first.

In Start-Stop mode a single Start bit is transmitted, followed by 5, 6, 7 or 8 data bits from the Tx Data Buffer - b0 first - followed by an optional Parity bit then - normally - one or two Stop bits. The Start, Parity and Stop bits are generated by the USART as determined by the Tx Mode Register settings and are not taken from the Tx Data Register.

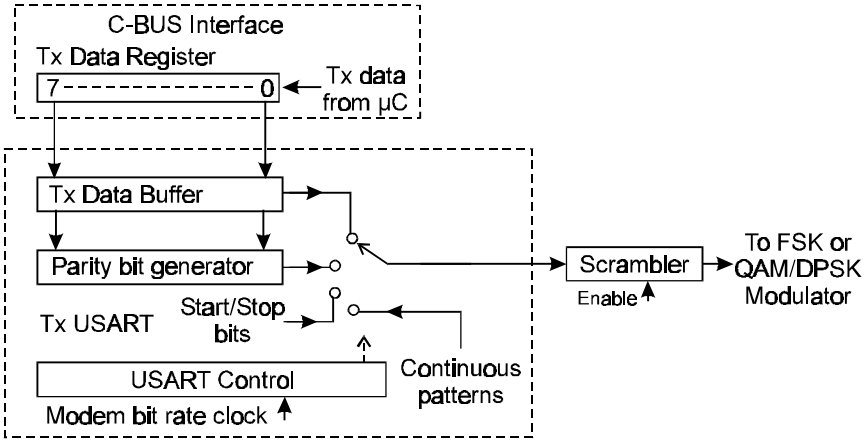


Figure 9a Tx USART

Every time the contents of the C-BUS Tx Data Register are transferred to the Tx Data Buffer the Tx Data Ready flag bit of Status Register 1 is set to 1 to indicate that a new value should be loaded into the C-BUS Tx Data Register. This flag bit is cleared to 0 when a new value is loaded into the Tx Data Register.

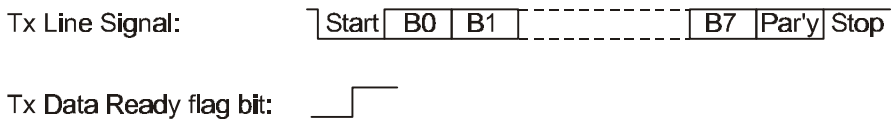


Figure 9b Tx USART Function (Start-Stop mode, 8 Data Bits + Parity)

If a new value is not loaded into the Tx Data Register in time for the next Tx Data Register to Tx Data Buffer transfer then Status Register 1 Tx Data Underflow bit will be set to 1. In this event the contents of the Tx Data Buffer will be re-transmitted if Synchronous Data mode has been selected, or if the Tx modem is in Start-Stop mode then a continuous Stop signal (1) will be transmitted until a new value is loaded into the Tx Data Register.

In all modes the transmitted bit and baud rates are the nominal rates for the selected modem type, with an accuracy determined by the accuracy of the system clock frequency, however for QAM and DPSK modes V.14 requires that Start-Stop characters can be transmitted at up to 1% overspeed (basic signalling rate

range) or 2.3% overspeed (extended signalling rate range) by deleting a Stop bit from no more than one out of every 8 (basic range) or 4 (extended range) consecutive transmitted characters.

To accommodate the V.14 requirement the Tx Data Register has been given two C-BUS addresses, $E3 and $E4. Data should normally be written to $E3.

In QAM or DPSK Start-Stop modes if data is written to $E4 then the programmed number of Stop bits will be reduced by one for that character. In this way the µC can delete transmitted Stop bits as needed.

In FSK Start-Stop modes, data written to $E4 will be transmitted with a 12.5% reduction in the length of the Stop bit at the end of that character.

In all Synchronous Data modes data written to $E4 will be treated as though it had been written to $E3.

The underspeed transmission requirement of V.14 is automatically met by the Modem as in Start-Stop mode it automatically inserts extra Stop bit(s) if it has to wait for new data to be loaded into the C-BUS Tx Data Register.

The optional V.22/V.22 bis compatible data scrambler can be programmed to invert the next input bit in the event of 64 consecutive ones appearing at its input. It uses the generating polynomial:

$$1 + x^{-14} + x^{-17}$$

1.6.2 FSK and QAM/DPSK Modulators

Serial data from the USART is fed via the optional scrambler to the FSK modulator if V.21, V.23, Bell 103 or Bell 202 mode has been selected or to the QAM/DPSK modulator for V.22, V.22 bis and Bell 212A modes.

The FSK modulator generates one of two frequencies according to the transmit mode and the value of current transmit data bit.

The QAM/DPSK modulator generates a carrier of 1200Hz (Low Band, Calling modem) or 2400Hz (High Band, Answering modem) which is modulated at 600 symbols/sec as described below:

600bps V.22 signals are transmitted as a +90° carrier phase change for a ‘0’ bit, +270° for ‘1’.

For V.22 and Bell 212A 1200bps DPSK the transmit data stream is divided into groups of two consecutive bits (dibits) which are encoded as a carrier phase change:

Dibit (left-hand bit is the first of the pair)	**Phase change**
00	+90°
01	0°
11	+270°
10	+180°

For V.22 bis 2400bps QAM the transmit data stream is divided into groups of 4 consecutive data bits. The first two bits of each group are encoded as a phase quadrant change and the last two bits define one of four elements within a quadrant:

First two bits of group (left-hand bit is the first of the pair)	Phase quadrant change
00	+90° (e.g. quadrant 1 to 2)
01	0° (no change of quadrant)
11	+270° (e.g. quadrant 1 to 4)
10	+180° (e.g. quadrant 1 to 3)

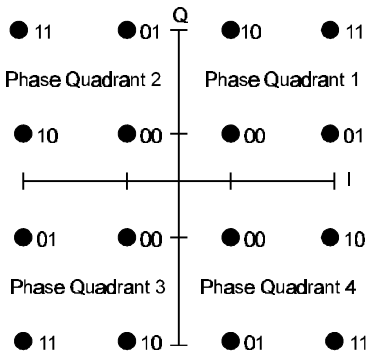


Figure 10 V.22 bis Signal Constellation

1.6.3 Tx Filter and Equaliser

The FSK or QAM/DPSK modulator output signal is fed through the Transmit Filter and Equaliser block which limits the out-of-band signal energy to acceptable limits. In 600, 1200 and 2400 bps FSK, DPSK and QAM modes this block includes a fixed compromise line equaliser which is automatically set for the particular modulation type and frequency band being employed. This fixed compromise line equaliser may be enabled or disabled by bit 10 of the General Control Register. The amount of Tx equalisation provided compensates for one quarter of the relative amplitude and delay distortion of ETS Test Line 1 over the frequency band used.

1.6.4 DTMF/Tone Generator

In DTMF/Tones mode this block generates DTMF signals or single or dual frequency tones. In QAM/DPSK modem modes it is used to generate the optional 550 or 1800Hz guard tone.

1.6.5 Tx Level Control and Output Drivers

The Modem generated signal (if present) from the FSK/DTMF/Tones Generator is passed through the programmable Tx Level Control before being passed to the switched paths controlled by the Analogue Signal Path Register. The Tx Output drivers have symmetrical outputs to provide sufficient line voltage swing at low values of AV_{DD} and to reduce harmonic distortion of the signal. The drivers can also transmit the signal from the other port (e.g. Phone Input to Line Driver) or can be independently set to V_{BIAS} or Powersaved – see the description of the Analogue Signal Path Register.

1.6.6 DTMF Decoder and Tone Detectors

In Rx Tones Detect mode the received signal, after passing through the Rx Gain Control block, is fed to the DTMF decoder and Programmable Tone Pair/Call Progress/Answer Tone detectors. The user may select one of four separate operations:

The DTMF decoder detects standard DTMF signals. A valid DTMF signal will set bit 5 of Status Register 1 to 1 for as long as the signal is detected. The DTMF signal is then decoded and output in bits 0 to 3 of Status Register 1.

The programmable tone pair detector includes two separate tone detectors (see Figure 15a). The first detector will set bit 6 of Status Register 1 for as long as a valid signal is detected, the second detector sets bit 7, and bit 10 of Status Register 1 will be set when both tones are detected. The frequency and bandwidth of each detector can be set in the Programming Register. Without programming, the default values in the Programming Register are set for the detection of 2130Hz and 2750Hz.

The Call Progress detector measures the amplitude of the signal at the output of a 275 Hz - 665 Hz bandpass filter and sets bit 10 of Status Register 1 to 1 when the signal level exceeds the measurement threshold.

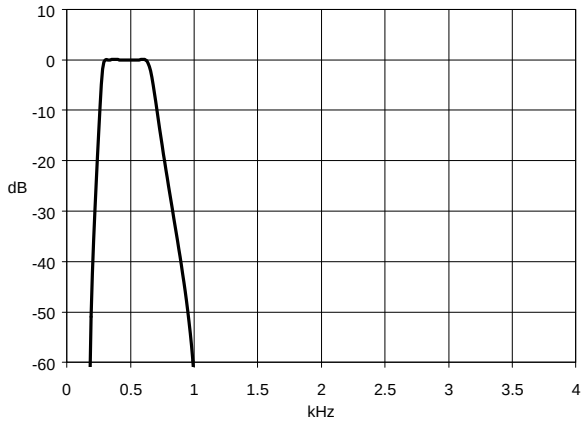


Figure 11a Response of the Call Progress Filter

The Answer Tone detector measures both amplitude and frequency of the received signal and sets bit 6 or bit 7 respectively of Status Register 1 when a valid 2225Hz or 2100Hz signal is received.

1.6.7 Rx Modem Filtering and Demodulation

When the receive part is operating as a modem, the received signal is fed to a bandpass filter to attenuate unwanted signals and to provide fixed compromise line equalisation for 600, 1200 and 2400 bps FSK, DPSK and QAM modes. The characteristics of the bandpass filter and equaliser are determined by the chosen receive modem type and frequency band. The line equaliser may be enabled or disabled by bit 10 of the General Control Register and compensates for one quarter of the relative amplitude and delay distortion of ETS Test Line 1.

The responses of these filters, including the line equaliser and the effect of external components used in Figures 4a and 4b, are shown in Figures 11b-e:

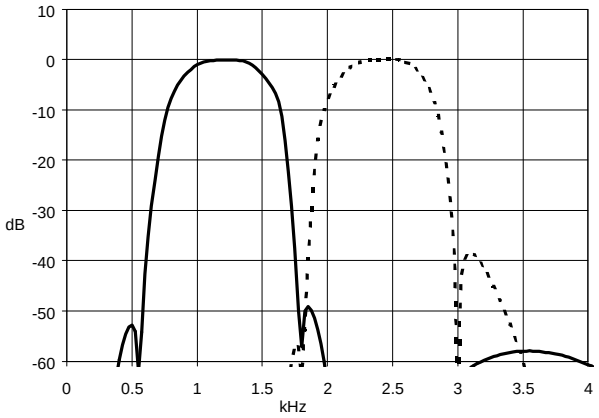


Figure 11b QAM/DPSK Rx Filters

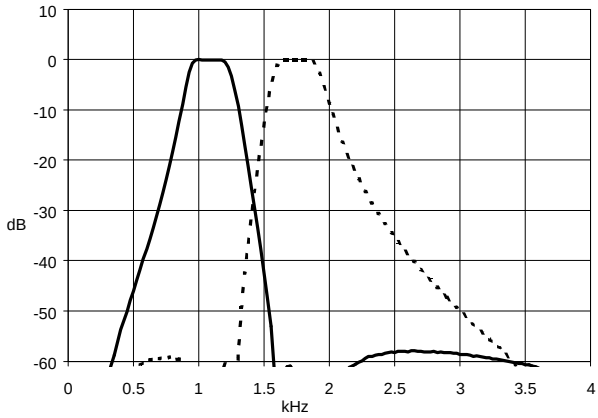


Figure 11c V.21 Rx Filters

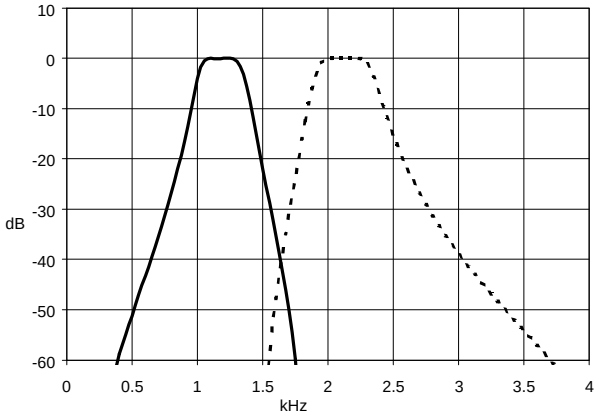


Figure 11d Bell 103 Rx Filters

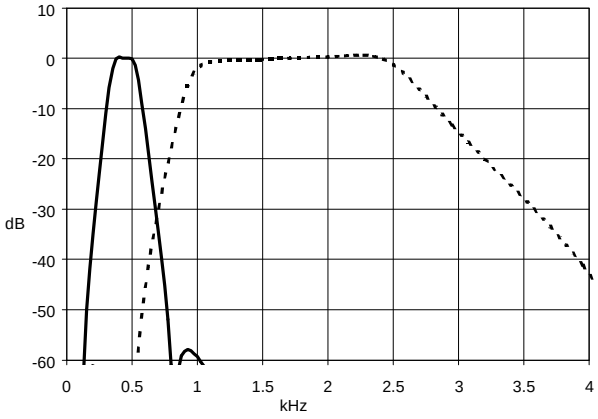


Figure 11e V.23/Bell 202 Rx Filters

The signal level at the output of the Receive Modem Filter and Equaliser is measured in the Modem Energy Detector block, compared to a threshold value, and the result controls bit 10 of Status Register 1.

The output of the Receive Modem Filter and Equaliser is also fed to the FSK or QAM/DPSK demodulator, depending on the selected modem type.

The FSK demodulator recognises individual frequencies as representing received '1' or '0' data bits.

The QAM/DPSK demodulator decodes QAM or DPSK modulation of a 1200Hz or 2400Hz carrier and is used for V.22, V.22 bis and Bell 212A modes. It includes an adaptive receive signal equaliser (auto-equaliser) that will automatically compensate for a wide range of line conditions in both QAM and DPSK modes. The auto-equaliser can provide a useful improvement in performance in 600 or 1200bps DPSK

modes as well as 2400bps QAM, so although it must be disabled at the start of a handshake sequence, it can be enabled as soon as scrambled 1200bps 1s have been detected.

Both FSK and QAM/DPSK demodulators produce a serial data bit stream which is fed to the Rx pattern detector, descrambler and USART block, see Figure 12a. In QAM/DPSK modes the demodulator input is also monitored for the V.22 bis handshake 'S1' signal.

The QAM/DPSK demodulator also estimates the received bit error rate by comparing the actual received signal against an ideal waveform. This estimate is placed in bits 2-0 of Status Register 1, see Figure 14.

1.6.8 Rx Modem Pattern Detectors and Descrambler

See Figure 12a.

The 1010.. pattern detector operates only in FSK modes and will set bit 9 of Status Register 1 when 32 bits of alternating 1's and 0's have been received.

The 'Continuous Unscrambled 1's' detector operates in all modem modes and sets bits 8 and 7 of Status Register 1 to '01' when 32 consecutive 1's have been received.

The descrambler operates only in DPSK/QAM modes and is enabled by setting bit 7 of the Rx Mode Register.

The 'Continuous Scrambled 1's' detector operates only in DPSK/QAM modes when the descrambler is enabled and sets bits 8 and 7 of Status Register 1 to '11' when 32 consecutive 1's appear at the output of the descrambler. To avoid possible ambiguity, the 'Scrambled 1's' detector is disabled when continuous unscrambled 1's are detected.

The 'Continuous 0's' detector sets bits 8 and 7 of Status Register 1 to '10' when NX consecutive 0's have been received, NX being 32 except when DPSK/QAM Start-Stop mode has been selected, in which case NX = 2N + 4 where N is the number of bits per character including the Start, Stop and any Parity bits.

All of these pattern detectors will hold the 'detect' output for 12 bit times after the end of the detected pattern unless the received bit rate or operating mode is changed, in which case the detectors are reset within 2 msec.

1.6.9 Rx Data Register and USART

A flexible Rx USART is provided for all modem modes, meeting the requirements of V.14 for QAM and DPSK modems. It can be programmed to treat the received data bit stream as Synchronous data or as Start-Stop characters.

In Synchronous mode the received data bits are all fed into the Rx Data Buffer which is copied into the C-BUS Rx Data Register after every 8 bits.

In Start-Stop mode the USART Control logic looks for the start of each character, then feeds only the required number of data bits (not parity) into the Rx Data Buffer. The parity bit (if used) and the presence of a Stop bit are then checked and the data bits in the Rx Data Buffer copied to the C-BUS Rx Data Register.

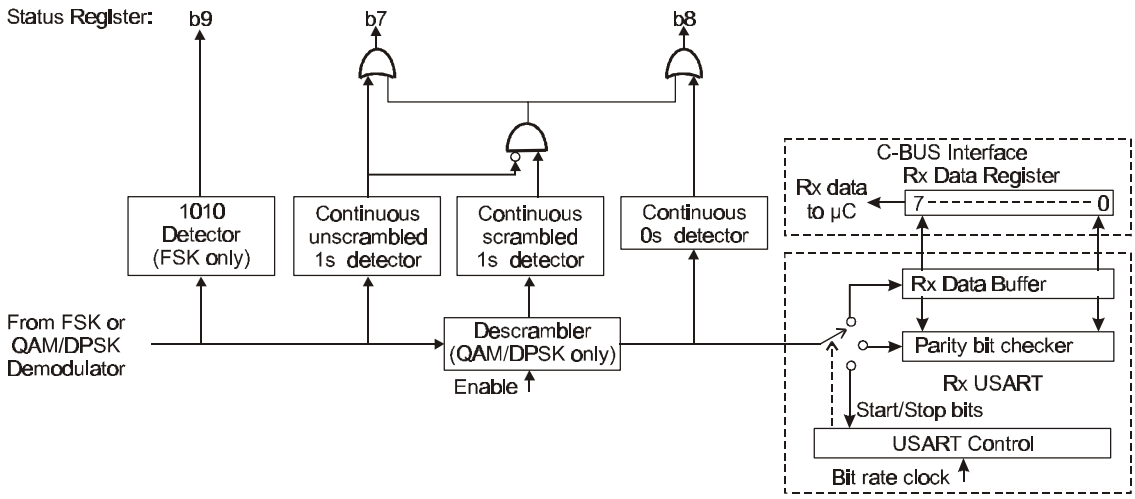


Figure 12a Rx Modem Data Paths

Whenever a new character is copied into the C-BUS Rx Data Register, the Rx Data Ready flag bit of Status Register 1 is set to '1' to prompt the µC to read the new data and, in Start-Stop mode, the Even Rx Parity flag bit of Status Register 1 is updated.

In Start-Stop mode, if the Stop bit is missing (received as a '0' instead of a '1') the received character will still be placed into the Rx Data Register and the Rx Data Ready flag bit set, but, unless allowed by the V.14 overspeed option described below, Status Register 1 Rx Framing Error bit will also be set to '1' and the USART will re-synchronise onto the next '1' – '0' (Stop – Start) transition. The Rx Framing Error bit will remain set until the next character has been received.

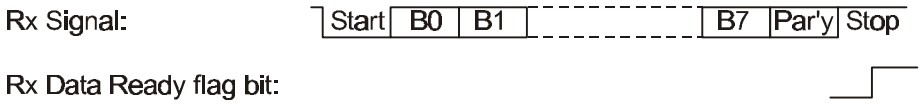


Figure 12b Rx USART Function (Start-Stop mode, 8 Data Bits + Parity)

If the µC has not read the previous data from the Rx Data Register by the time that new data is copied to it from the Rx Data Buffer then the Rx Data Overflow flag bit of Status Register 1 will be set to 1.

The Rx Data Ready flag and Rx Data Overflow bits are cleared to 0 when the Rx Data Register is read by the µC.

For QAM and DPSK Start-Stop modes, V.14 requires that the receive USART be able to cope with missing Stop bits; up to 1 missing Stop bit in every 8 consecutive received characters being allowed for the +1% overspeed (basic signalling rate) V.14 mode and 1 in 4 for the +2.3% overspeed (extended signalling rate) mode.

To accommodate the requirements of V.14, the Modem Rx Mode Register can be set for 0, +1% or +2.3% overspeed operation in QAM or DPSK Start-Stop modes. Missing Stop bits beyond those allowed by the selected overspeed option will set the Rx Framing Error flag bit of Status Register 1.

In order that received Break signals can be handled correctly in V.14 Rx overspeed mode, a received character which has all bits '0', including the Stop and any Parity bits, will always cause the Rx Framing Error bit to be set and the USART to re-synchronise onto the next '1' – '0' transition. Additionally the received Continuous 0s detector will respond when more than 2M + 3 consecutive '0's are received, where 'M' is the selected total number of bits per character including Stop and any Parity bits.

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1.6.10 Analogue Signal Routing

The routing of signals to and from the Line and Phone interfaces is performed by bits 0 to 5 of the Analogue Signal Path Register. Note that bits 6 and 7 of this register are reserved for future use and should be set to zero.

1.6.11 C-BUS Interface

This block provides for the transfer of data and control or status information between the Modem's internal registers and the µC over the C-BUS serial bus. This interface is controlled by the C-BUS Controller, which is part of the µC and is described in section 1.5.9.

The following C-BUS addresses and registers are used by the Modem:

General Reset Command (address only, no data).	Address $01
General Control Register, 16-bit write only.	Address $E0
Transmit Mode Register, 16-bit write-only.	Address $E1
Receive Mode Register, 16-bit write-only.	Address $E2
Transmit Data Register, 8-bit write only.	Address $E3 and $E4
Receive Data Register, 8-bit read-only.	Address $E5
Status Register 1, 16-bit read-only.	Address $E6
Status Register 2, 16-bit read-only.	Address $E7
Programming Register, 16-bit write-only.	Address $E8
Analogue Signal Path Register, 8-bit write-only.	Address $EC

Notes: 1. The C-BUS addresses $E9, $EA and $EB are allocated for production testing and should not be accessed in normal operation.

2. In several registers there are bit patterns whose function is not specified. These modes should not be accessed in normal operation and no guarantee is given that any use of these bits will be supported in the future.

1.6.11.1 General Reset Command

General Reset Command (no data) C-BUS address $01

This command resets the modem and clears all bits of the General Control, Analogue Signal Path, Programming, Transmit Mode and Receive Mode Registers and all bits of Status Register 1 except b14 and Status Register 2 except b8.

The clearing of the General Control Register will put the modem into Powersave. See the description of General Control Register b8 for the procedure on how to power-up the modem.

Whenever power is applied a General Reset command should be sent to the modem, after which the General Control Register should be set as required. The xtal frequency should also be configured using the 8051 OSCCON special function register before the modem is used.

1.6.11.2 General Control Register

General Control Register: 16-bit write-only. C-BUS address $E0

This register controls general features of the modem such as the Powersave mode, the IRQ mask bits and the Relay Drive output. It also allows the fixed compromise equalisers in the Tx and Rx signal paths to be disabled if desired.

All bits of this register are cleared to 0 by a General Reset command.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	Hook IRQ Mask	Equ	Rly drv	Pwr	Rst	Irqn en	IRQ Mask Bits					

General Control Register b15-12: Reserved, set to 0000

General Control Register b11: Hook Detect IRQ Mask bit
This bit affects the operation of the IRQ bit of Status Register 1 as described in section 1.6.11.8

General Control Register b10: Tx and Rx Fixed Compromise Equaliser
This bit allows the Tx and Rx fixed compromise equaliser in the modem transmit and receive filter blocks to be disabled.

b10 = 1	Disable equaliser
b10 = 0	Enable equaliser (1200bps modem mode)

General Control Register b9: Relay Drive
This bit directly controls the RDRVN output pin.

b9 = 1	RDRVN output pin pulled to DV_{SS}
b9 = 0	RDRVN output pin pulled to DV_{DD}

General Control Register b8: Powerup
This bit controls the internal power supply to most of the internal circuits, including the V_{BIAS} supply. Note that the General Reset command clears this bit, putting the device into Powersave mode.

b8 = 1	Device powered up normally
b8 = 0	Powersave mode (all circuits except Ring Detect, Hook Detect, RDRVN and C-BUS interface disabled)

When power is first applied to the device, the following powerup procedure should be followed to ensure correct operation.

i. (Power is applied to the device)
ii. Issue a General Reset command or momentarily set the RESETN pin low.
iii. Write to the General Control Register (address $E0) setting both the Powerup bit (b8) and the Reset bit (b7) to 1 – leave in this state for a minimum of about 20ms – it is required that the system clock initially runs for this time in order to clock the internal logic into a defined state. The device is now powered up, with the V_{BIAS} supply operating, but is otherwise not running any transmit or receive functions.
iv. Set the Xtal frequency to the correct one in the OSCCON register, if necessary see section 1.5.6.1
v. The device is now ready to be programmed as and when required. Examples:
- A General Reset command could be issued to clear all the registers and therefore powersave the device.
- The Reset bit in the General Control Register could be set to 0 as part of a routine to program all the relevant registers for setting up a particular operating mode.

When the modem is switched from Powersave mode to normal operation by setting the Powerup bit to 1, the Reset bit should also be set to 1 and should be held at 1 for about 20ms with the system clock running, allowing the V_{BIAS} supply to stabilise, before starting to use the transmitter or receiver.

General Control Register b7: Reset
Setting this bit to 1 resets the modem's internal circuitry, clearing all bits of the Analogue Signal Path, Programming, Transmit and Receive Mode Registers and b13-0 of Status Register 1.

b7 = 1	Internal circuitry in a reset condition.
b7 = 0	Normal operation

General Control Register b6: IRQNEN (IRQN Enable)
Setting this bit to 1 enables the Modems IRQN signal.

b6 = 1	IRQN driven low (to DV_{SS}) if the IRQ bit of Status Register 1 = 1
b6 = 0	IRQN disabled (set to 1)

General Control Register b5-0: IRQ Mask bits
These bits affect the operation of the IRQ bit of Status Register 1 as described in section 1.6.11.8

1.6.11.3 Transmit Mode Register

Transmit Mode Register: 16-bit write-only. C-BUS address $E1

This register controls the Modem transmit signal type and level. All bits of this register are cleared to 0 by a General Reset command, or when b7 (Reset) of the General Control Register is 1.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tx mode = modem				Tx level			Guard tone		Scrambler		Start-stop / synch data		# data bits / synch data source		
	Tx mode = DTMF/Tones				Tx level			DTMF twist				DTMF or Tone select				
	Tx mode = Disabled				Set to 0000 0000 0000											

Tx Mode Register b15-12: Tx mode

These 4 bits select the transmit operating mode.

b15	b14	b13	b12		
1	1	1	1	V.22 bis 2400 bps QAM	High band (Answering modem)
1	1	1	0	"	Low band (Calling modem)
1	1	0	1	V.22/Bell 212A 1200 bps DPSK	High band (Answering modem)
1	1	0	0	"	Low band (Calling modem)
1	0	1	1	V.22 600 bps DPSK	High band (Answering modem)
1	0	1	0	"	Low band (Calling modem)
1	0	0	1	V.21 300 bps FSK	High band (Answering modem)
1	0	0	0	"	Low band (Calling modem)
0	1	1	1	Bell 103 300 bps FSK	High band (Answering modem)
0	1	1	0	"	Low band (Calling modem)
0	1	0	1	V.23 FSK	1200 bps
0	1	0	0	"	75 bps
0	0	1	1	Bell 202 FSK	1200 bps
0	0	1	0	"	150 bps
0	0	0	1	DTMF / Tones	
0	0	0	0	Transmitter disabled	

Tx Mode Register b11-9: Tx level

These 3 bits set the gain of the Tx Level Control block.

b11	b10	b9	
1	1	1	0dB
1	1	0	-1.5dB
1	0	1	-3.0dB
1	0	0	-4.5dB
0	1	1	-6.0dB
0	1	0	-7.5dB
0	0	1	-9.0dB
0	0	0	-10.5dB

Tx Mode Register b8-7: Tx Guard tone (QAM, DPSK modes)
These 2 bits select the guard tone to be transmitted together with highband QAM or DPSK. Set both bits to 0 in FSK modes.

b8	b7	
1	1	Tx 550Hz guard tone
1	0	Tx 1800Hz guard tone
0	x	No Tx guard tone

Tx Mode Register b6-5: Tx Scrambler (QAM, DPSK modes)
These 2 bits control the operation of the Tx scrambler used in QAM and DPSK modes. Set both bits to 0 in FSK modes.

b6	b5	
1	1	Scrambler enabled, 64 ones detect circuit enabled (normal use)
1	0	Scrambler enabled, 64 ones detect circuit disabled
0	x	Scrambler disabled

Tx Mode Register b4-3: Tx Data Format (QAM, DPSK, FSK modes)
These two bits select Synchronous or Start-stop mode and the addition of a parity bit to transmitted characters in Start-stop mode.

b4	b3	
1	1	Synchronous mode
1	0	Start-stop mode, no parity
0	1	Start-stop mode, even parity bit added to data bits
0	0	Start-stop mode, odd parity bit added to data bits

Tx Mode Register b2-0: Tx Data and Stop bits (QAM, DPSK, FSK Start-Stop modes)
In Start-stop mode these three bits select the number of Tx data and stop bits.

b2	b1	b0	
1	1	1	8 data bits, 2 stop bits
1	1	0	8 data bits, 1 stop bit
1	0	1	7 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
0	1	0	6 data bits, 1 stop bit
0	0	1	5 data bits, 2 stop bits
0	0	0	5 data bits, 1 stop bit

Tx Mode Register b2-0: Tx Data source (QAM, DPSK, FSK Synchronous mode)
In Synchronous mode (b4-3 = 11) these three bits select the source of the data fed to the Tx FSK or QAM/DPSK scrambler and modulator.

b2	b1	b0	
1	x	x	Data bytes from Tx Data Buffer
0	1	1	Continuous 1s
0	1	0	Continuous 0s
0	0	x	Continuous V.22 bis handshake S1 pattern dibits ’00,11’ in DPSK and QAM modes, continuous alternating 1s and 0s in all other modes.

Tx Mode Register b8: DTMF Twist (DTMF mode)
If DTMF/Tones transmit mode has been selected (Tx Mode Register b15-12 = 0001) then set this bit to 0 and set the twist in b7-5 (000 default = +2.0dB).

Tx Mode Register b7-5: DTMF Twist (DTMF mode)
These 3 bits allow for adjustment of the DTMF twist to compensate for the frequency response of different external circuits. The CMX850 varies the twist by making changes to the upper tone group levels. Note that the twist cannot adjusted mid-tone.

b7	b6	b5	
0	0	0	+2.0dB twist – normal setting when external response is flat
0	0	1	+1.0dB twist
0	1	0	+1.5dB twist
0	1	1	+2.5dB twist
1	0	0	+3.0dB twist
1	0	1	+3.5dB twist
1	1	0	+4.0dB twist
1	1	1	+4.5dB twist – do not use in conjunction with the 0dB Tx level setting

Tx Mode Register b4-0: DTMF/Tones mode
If DTMF/Tones transmit mode has been selected (Tx Mode Register b15-12 = 0001) then b4-0 will select a DTMF signal or a fixed tone or one of four programmed tones or tone pairs for transmission.

b4 = 0: Tx fixed tone or programmed tone pair

b3	b2	b1	b0	Tone frequency (Hz)	
0	0	0	0	No tone	
0	0	0	1	697	
0	0	1	0	770	
0	0	1	1	852	
0	1	0	0	941	
0	1	0	1	1209	
0	1	1	0	1336	
0	1	1	1	1477	
1	0	0	0	1633	
1	0	0	1	1300	(Calling tone)
1	0	1	0	2100	(Answer tone)
1	0	1	1	2225	(Answer tone)
1	1	0	0	Tone pair TA	Programmed Tx tone or tone pair, see section 1.6.11.10
1	1	0	1	Tone pair TB	“
1	1	1	0	Tone pair TC	“
1	1	1	1	Tone pair TD	“

b4 = 1: Tx DTMF

b3	b2	b1	b0	Low frequency (Hz)	High frequency (Hz)	Keypad symbol
0	0	0	0	941	1633	D
0	0	0	1	697	1209	1
0	0	1	0	697	1336	2
0	0	1	1	697	1477	3
0	1	0	0	770	1209	4
0	1	0	1	770	1336	5
0	1	1	0	770	1477	6
0	1	1	1	852	1209	7
1	0	0	0	852	1336	8
1	0	0	1	852	1477	9
1	0	1	0	941	1336	0
1	0	1	1	941	1209	*
1	1	0	0	941	1477	#
1	1	0	1	697	1633	A
1	1	1	0	770	1633	B
1	1	1	1	852	1633	C

1.6.11.4 Receive Mode Register

Receive Mode Register: 16-bit write-only. C-BUS address $E2

This register controls the modem receive signal type and level.

All bits of this register are cleared to 0 by a General Reset command, or when b7 (Reset) of the General Control Register is 1.

Bit:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rx mode = modem				Rx level			Eq	Descrambl		Start-stop/Synch			No. of bits and parity		
Rx mode = Tones detect				Rx level			DTMF/Tones/Call Progress select								
Rx mode = Disabled				Set to 0000 0000 0000											

Rx Mode Register b15-12: Rx mode
These 4 bits select the receive operating mode.

b15	b14	b13	b12		
1	1	1	1	V.22 bis 2400 bps QAM	High band (Calling modem)
1	1	1	0	"	Low band (Answering modem)
1	1	0	1	V.22/Bell 212A 1200 bps DPSK	High band (Calling modem)
1	1	0	0	"	Low band (Answering modem)
1	0	1	1	V.22 600 bps DPSK	High band (Calling modem)
1	0	1	0	"	Low band (Answering modem)
1	0	0	1	V.21 300 bps FSK	High band (Calling modem)
1	0	0	0	"	Low band (Answering modem)
0	1	1	1	Bell 103 300 bps FSK	High band (Calling modem)
0	1	1	0	"	Low band (Answering modem)
0	1	0	1	V.23 FSK	1200 bps
0	1	0	0	"	75 bps
0	0	1	1	Bell 202 FSK	1200 bps
0	0	1	0	"	150 bps
0	0	0	1	DTMF, Programmed tone pair, Answer Tone, Call Progress detect	
0	0	0	0	Receiver disabled	

Rx Mode Register b11-9: Rx level
These three bits set the gain of the Rx Gain Control block.

b11	b10	b9	
1	1	1	0dB
1	1	0	-1.5dB
1	0	1	-3.0dB
1	0	0	-4.5dB
0	1	1	-6.0dB
0	1	0	-7.5dB
0	0	1	-9.0dB
0	0	0	-10.5dB

Rx Mode Register b8: Rx Auto-equalise (DPSK/QAM modem modes)
This bit controls the operation of the receive DPSK/QAM auto-equaliser. Set to 0 in FSK modes.

b8 = 1	Enable auto-equaliser
b8 = 0	DPSK mode: Auto-equaliser disabled QAM mode : Auto-equaliser settings frozen

Rx Mode Register b7-6: Rx Scrambler (DPSK/QAM modem modes)
These 2 bits control the operation of the Rx descrambler used in QAM and DPSK modes. Set both bits to 0 in FSK modes

b7	b6	
1	1	Descrambler enabled, 64 ones detect circuit enabled (normal use)
1	0	Descrambler enabled, 64 ones detect circuit disabled
0	x	Descrambler disabled

Rx Mode Register b5-3: Rx USART Setting (QAM, DPSK, FSK modem modes)
These three bits select the Rx USART operating mode. The 1% and 2.3% overspeed options apply to DPSK/QAM modes only.

b5	b4	b3	
1	1	1	Rx Synchronous mode
1	1	0	Rx Start-stop mode, no overspeed
1	0	1	Rx Start-stop mode, +1% overspeed (1 in 8 missing Stop bits allowed)
1	0	0	Rx Start-stop mode, +2.3% overspeed (1 in 4 missing Stop bits allowed)
0	x	x	Rx USART function disabled

Rx Mode Register b2-0: Rx Data bits and parity (QAM, DPSK, FSK Start-Stop modem modes)
In Start-stop mode these three bits select the number of data bits (plus any parity bit) in each received character. These bits are ignored in Synchronous mode.

b2	b1	b0	
1	1	1	8 data bits + parity
1	1	0	8 data bits
1	0	1	7 data bits + parity
1	0	0	7 data bits
0	1	1	6 data bits + parity
0	1	0	6 data bits
0	0	1	5 data bits + parity
0	0	0	5 data bits

Rx Mode Register b2-0: Tones Detect mode
In Tones Detect Mode (Rx Mode Register b15-12 = 0001) b8-3 should be set to 000000
Bits 2-0 select the detector type.

b2	b1	b0	
1	0	0	Programmable Tone Pair Detect
0	1	1	Call Progress Detect
0	1	0	2100, 2225Hz Answer Tone Detect
0	0	1	DTMF Detect
0	0	0	Disabled

1.6.11.5 Tx Data Register

Tx Data Register: 8-bit write-only. C-BUS address $E3

Bit:	7	6	5	4	3	2	1	0
	Data bits to be transmitted							

In Synchronous Tx data mode this register contains the next 8 data bits to be transmitted. Bit 0 is transmitted first.

In Tx Start-stop mode the specified number of data bits will be transmitted from this register (b0 first). A Start bit, a Parity bit (if required) and Stop bit(s) will be added automatically.

This register should only be written to when the Tx Data Ready bit of Status Register 1 is 1.

C-BUS address $E3 should normally be used, $E4 is for implementing the V.14 overspeed transmission requirement in Start-Stop mode, see section 1.6.1.

1.6.11.6 Rx Data Register

Rx Data Register: 8-bit read-only. C-BUS address $E5

Bit:	7	6	5	4	3	2	1	0
	Received data bits							

In unformatted Rx data mode this register contains 8 received data bits, b0 of the register holding the earliest received bit, b7 the latest.

In Rx Start-stop data mode this register contains the specified number of data bits from a received character, b0 holding the first received bit.

1.6.11.7 Analogue Signal Path Register

Analogue Signal Path Register: 8-bit write-only. C-BUS address $EC

This register controls the routing of the analogue signal paths and controls the output drivers.

Bit:	7	6	5	4	3	2	1	0
	0	0	Aux. Line RXN Enable	Line Driver Mode		Phone Driver Mode		Input Selector Control

Bits 7-6 of the Analogue Signal Path Register are reserved for future use and should be set to 0.

Analogue Signal Path Register b5: Auxiliary Line RXN enable
Enables the LINERXBN pin to be connected to the line Rx amp. inverting input (at the same time as the LINERXN pin). Used to increase gain, and compensate for signal attenuation during on-hook CLI detect.

b5 = 1	Aux. Line RXN enabled
b5 = 0	Aux. Line RXN disabled

Analogue Signal Path Register b4-3: Line Driver Mode
These bits control the complementary Line Driver and select the signal to be transmitted.

b4	b3	Line Driver Mode
0	0	Off / High Impedance
0	1	Transmit Phone-derived Signal
1	0	Transmit Modem Generated Signal
1	1	Transmit Bias Level

Analogue Signal Path Register b2-1: Phone Driver Mode
These bits control the complementary Phone Driver and select the signal to be transmitted.

b2	b1	Phone Driver Mode
0	0	Off / High Impedance
0	1	Transmit Line-derived Signal
1	0	Transmit Modem Generated Signal
1	1	Transmit Bias Level

Analogue Signal Path Register b0: Input Selector Control
This bit selects between the Line and Phone as inputs to the modem's decoders/detectors.

Note: both op-amps remain powered up even when not selected (unless device is powersaved).

b0 = 1	Line-derived signal to decoders/detectors
b0 = 0	Phone-derived signal to decoders/detectors

Notes:

1. 'Line-derived signal' means the signal at the output of the Line input op-amp. 'Phone-derived signal' means the signal at the output of the Phone input op-amp. The 'Modem Generated Signal' means the signal from the DTMF/Tones or FSK generators.

2. When the modem is put into Powersave by setting Bit 8 of the General Control Register to 1, the transmit drivers and receive op-amps are powersaved and their outputs go high impedance. The settings of the Analogue Signal Path Register are unaffected, however.

1.6.11.8 Status Register 1

Status Register 1: 16-bit read-only. C-BUS address $E6

Bits 15 and 13-0 of this register are cleared to 0 by a General Reset command, or when b7 (Reset) of the General Control Register is 1.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ	RD	PF	See below for uses of these bits												

The meanings of Status Register 1 bits 12-0 depend on whether the receive circuitry is in Modem or Tones Detect mode, as shown in Table 6.

Status Register 1 bits:

	Rx Modem modes	Rx Tones Detect modes	** IRQ Mask bit
b15	IRQ		
b14	Set to 1 on Ring Detect		b5
b13	Programming Flag bit. See section 1.6.11.10		b4
b12	Set to 1 on Tx data ready. Cleared by write to Tx Data Register		b3
b11	Set to 1 on Tx data underflow. Cleared by write to Tx Data Register		b3
b10	1 when energy is detected in Rx modem signal band	1 when energy is detected in Call Progress band or when both programmable tones are detected	b2
b9	1 when S1 pattern (double DPSK dibit 00,11) is detected in DPSK or QAM modes, or when '1010..' pattern is detected in FSK modes	0	b1
b8	See following table	0	b1
b7	See following table	1 when 2100Hz answer tone or the second programmable tone is detected	b1
b6	Set to 1 on Rx data ready. Cleared by read from Rx Data Register	1 when 2225Hz answer tone or the first programmable tone is detected	b0
b5	Set to 1 on Rx data overflow. Cleared by read from Rx Data Register	1 when DTMFcode is detected	b0
b4	Set to 1 on Rx framing error	0	-
b3	Set to 1 on even Rx parity	Rx DTMF code b3, see table	-
b2	QAM/DPSK Rx signal quality b2	Rx DTMF code b2	-
b1	QAM/DPSK Rx signal quality b1	Rx DTMF code b1	-
b0	QAM/DPSK Rx signal quality b0 or FSK frequency demodulator output	Rx DTMF code b0	-

Notes: ** This column shows the corresponding IRQ Mask bits in the General Control Register.

Table 6 Status Register 1 - Bit Allocations

Certain events of Status Register 1 bits 14-5 and Status Register 2 bit 8 will cause the IRQ bit b15 to be set to 1 if the corresponding IRQ Mask bit is 1. These events are:

for Status Register 1 Bit 14 (Ring Detect) and Bit 10 (Energy or Call Progress / Programmable Tones Detect) and Status Register 2 Bit 8 (Hook Detect), both positive-going (0 to 1) and negative-going (1 to 0) transitions,

for the remaining Status Register bits, only positive-going (0 to 1) transitions.

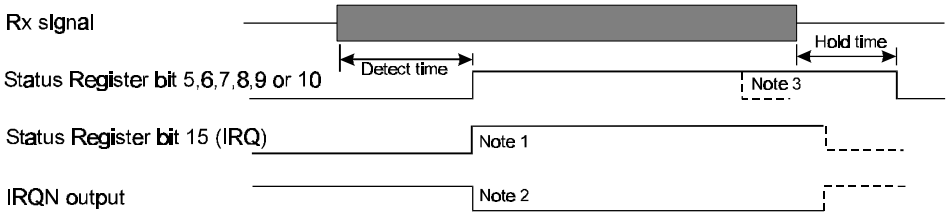
The IRQ bit is cleared by a read of Status Register 1 or Status Register 2 depending on the source of the IRQ, or a General Reset command or by setting b7 or b8 of the General Control Register to 1.

The operation of the data demodulator and pattern detector circuits within the modem does not depend on the state of the Rx energy detect function.

Decoding of Status Register 1 b8,7 in Rx Modem Modes (see also Figure 12a):

b8	b7	Descrambler disabled	Descrambler enabled (DPSK/QAM modes only)
1	1	-	Continuous scrambled 1s (see note)
1	0	Continuous unscrambled 0s	Continuous scrambled 0s
0	1	Continuous unscrambled 1s	Continuous unscrambled 1s
0	0	-	-

When the descrambler is enabled then detection of continuous unscrambled 1s will inhibit the continuous scrambled 1s detector.



Notes:
1. IRQ will go high only if appropriate IRQ Mask bit in General Control Register is set. The IRQ bit is cleared by a read of the Status Register.
2. IRQN o/p will go low when IRQ bit high if IRQNEN bit of General Control Register is set
3. In Rx Modem modes Status Register bits 5 and 6 are set by a Rx Data Ready or Rx Data Underflow event and cleared by a read of the Rx Data Register

Figure 13a Operation of Status Register 1 bits 5-10

The IRQN signal will be pulled low when the IRQ bit of Status Register 1 and the IRQNEN bit (b6) of the General Control Register are both 1.

Changes to Status Register 1 bits caused by a change of Tx or Rx operating mode can take up to 150µs to take effect.

In Powersave mode or when the Reset bit (b7) of the General Control Register is 1 the Ring Detect bit (b14) continues to operate.

The 'continuous 0' and 'continuous 1' detectors monitor the Rx signal after the QAM/DPSK descrambler, (see Figure 12a) and hence will detect continuous 1s or 0s if the descrambler is disabled, or continuous scrambled 1s or 0s if the descrambler is enabled.

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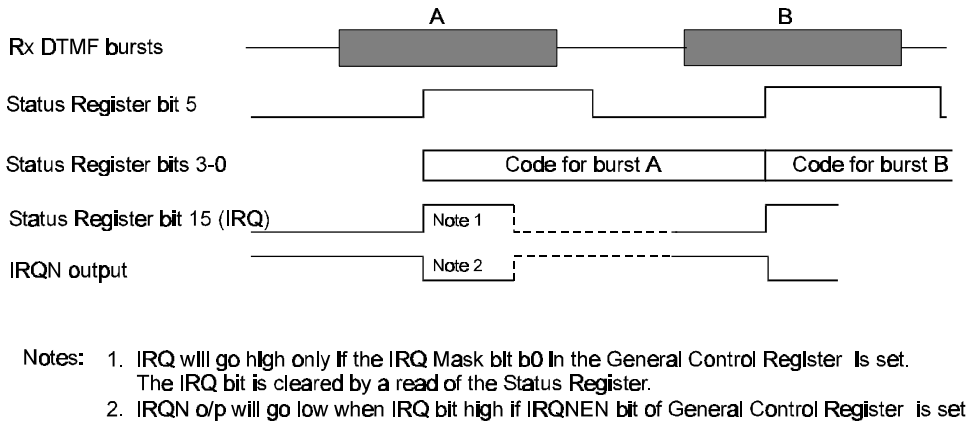
In QAM or DPSK Rx modem modes b2-0 of Status Register 1 contain a value indicative of the received signal BER, see Figure 14. In Rx FSK modem modes bits 2 and 1 will be zero and b0 will show the output of the frequency demodulator, updated at 8 times the nominal data rate.



Notes: 1. IRQ will go high only if the IRQ Mask bit b0 in the General Control Register is set. The IRQ bit is cleared by a read of the Status Register.
2. IRQN o/p will go low when IRQ bit high if IRQNEN bit of General Control Register is set

Figure 13b Operation of Status Register 1 in DTMF Rx Mode

b3	b2	b1	b0	Low frequency (Hz)	High frequency (Hz)	Keypad symbol
0	0	0	0	941	1633	D
0	0	0	1	697	1209	1
0	0	1	0	697	1336	2
0	0	1	1	697	1477	3
0	1	0	0	770	1209	4
0	1	0	1	770	1336	5
0	1	1	0	770	1477	6
0	1	1	1	852	1209	7
1	0	0	0	852	1336	8
1	0	0	1	852	1477	9
1	0	1	0	941	1336	0
1	0	1	1	941	1209	*
1	1	0	0	941	1477	#
1	1	0	1	697	1633	A
1	1	1	0	770	1633	B
1	1	1	1	852	1633	C

Table 7 Received DTMF Code: b3-0 of Status Register 1

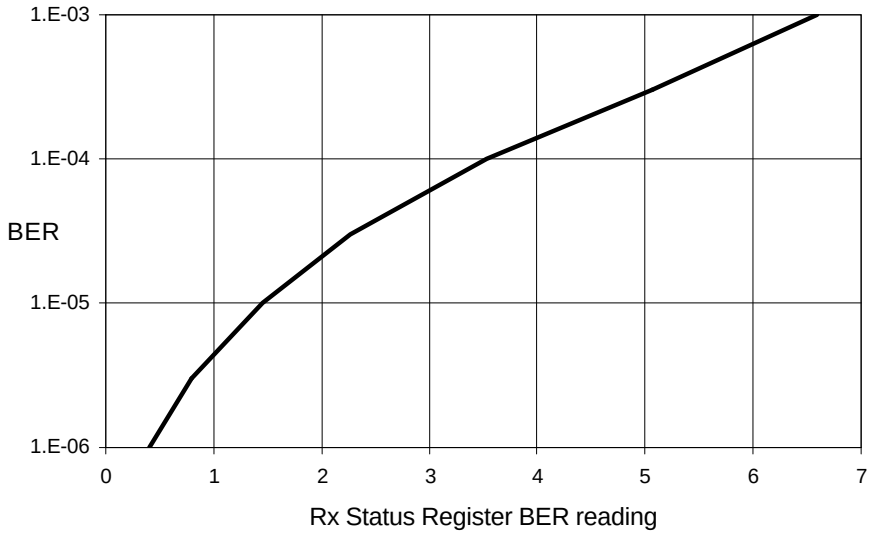


Figure 14 Typical Rx BER vs. Average Status Register 1 BER Reading (b2-0)

1.6.11.9 Status Register 2

Status Register 2: 16-bit read-only. C-BUS address $E7

Status Register 2 bits:

	Rx Modem modes	Rx Tones Detect modes	** IRQ Mask bit
b15-9	Reserved, will read as 0000000		-
b8	Set to 1 on Hook Detect		b11
b7-0	Reserved, will read as 00000000		-

Notes: ** This column shows the corresponding IRQ Mask bit in the General Control Register. A 0 to 1 transition on bit 8 Hook Detect will cause the IRQ bit b15 of Status Register 1 (see previous section) to be set to 1 if the corresponding IRQ Mask bit is 1. If the IRQ bit is generated by Status Register 2 bit 8, it will be cleared by reading Status Register 2 or a General Reset command or by setting b7 or b8 of the General Control Register to 1. Therefore it is recommended that both Status Register 1 and Status Register 2 are read to determine the source of an IRQ.

Table 8 Status Register 2 - Bit Allocations

1.6.11.10 Programming Register

Programming Register : 16-bit write-only. C-BUS address $E8

This register is used to program the transmit and receive programmed tone pairs by writing appropriate values to RAM locations within the modem. Note that these RAM locations are cleared by Powersave or Reset.

The Programming Register should only be written to when the Programming Flag bit (b13) of Status Register 1 is 1. The act of writing to the Programming Register clears the Programming Flag bit. When the programming action has been completed (normally within 150µs) the modem will set the bit back to 1.

When programming Transmit or Receive Tone Pairs, do not change the Transmit or Receive Mode Registers until programming is complete and the Programming Flag bit has returned to 1.

Transmit Tone Pair Programming

4 transmit tone pairs (TA to TD) can be programmed.

The frequency (max 3.4kHz) and level must be entered for each tone to be used.

Single tones are programmed by setting both level and frequency values to zero for one of the pair.

Programming is done by writing a sequence of up to seventeen 16-bit words to the Programming Register. The first word should be 32768 (8000 hex), the following 16-bit words set the frequencies and levels and are in the range 0 to 16383 (0-3FFF hex)

Word	Tone Pair	Value written	Default Setting
1		32768	
2	TA	Tone 1 frequency	
3	TA	Tone 1 level	
4	TA	Tone 2 frequency	
5	TA	Tone 2 level	
6	TB	Tone 1 frequency	
7	TB	Tone 1 level	
- - -	- - -	- - - - - - - - - -	
- - -	- - -	- - - - - - - - - -	
14	TD	Tone 1 frequency	2130 Hz
15	TD	Tone 1 level	-20 dBm
16	TD	Tone 2 frequency	2750 Hz
17	TD	Tone 2 level	-20 dBm

The Frequency values to be entered are calculated from the formula:

Value to be entered = desired frequency (Hz) * 3.414

i.e. for 1kHz the value to be entered is 3414 (or 0D56 in Hex).

The Level values to be entered are calculated from the formula:

Value to be entered = desired Vrms * 93780 / AV_{DD}

i.e. for 0.5Vrms at AV_{DD} = 3.0V, the value to be entered is 15630 (3D0E in Hex)

Note that allowance should be made for the transmit signal filtering in the modem which attenuates the output signal for frequencies above 2kHz by 0.25dB at 2.5kHz, by 1dB at 3kHz and by 2.2dB at 3.4kHz.

Receive Tone Pair Programming

The programmable tone pair detector is implemented as shown in Figure 15a. The filters are 4th order IIR sections. The frequency detectors measure the time taken for a programmable number of complete input signal cycles and compare this time against programmable upper and lower limits.

NB. If this register is not programmed, the detector will be configured to operate in its default mode, which is for the detection of 2130 Hz ± 20 Hz and 2750 Hz ± 30 Hz tones.

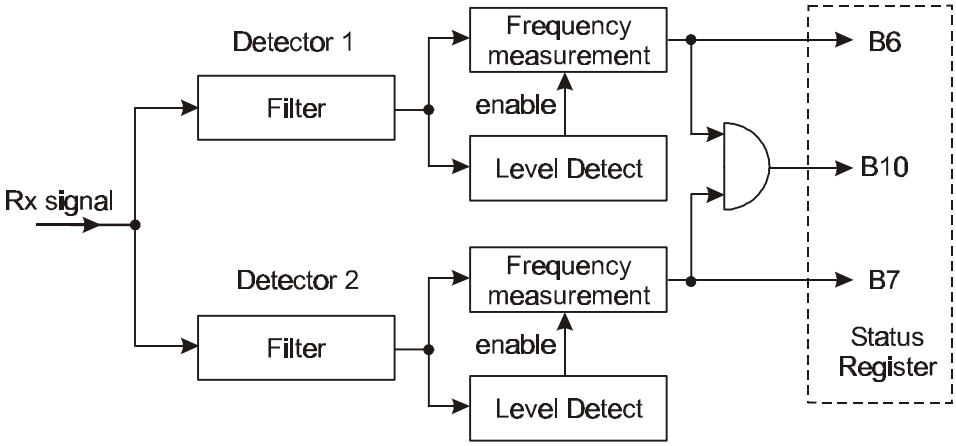


Figure 15a Programmable Tone Detectors

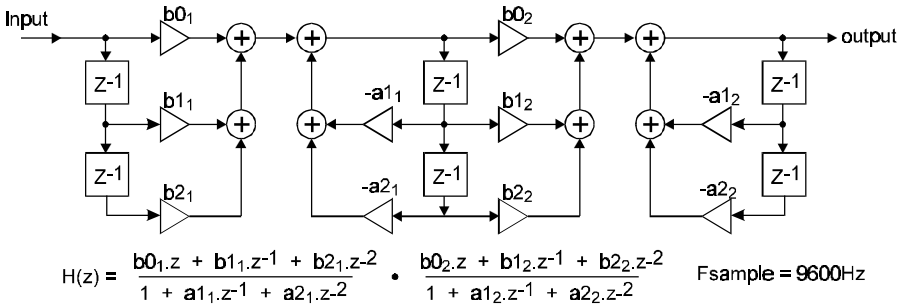


Figure 15b Filter Implementation

Programming is done by writing a sequence of twenty-seven 16-bit words to the Programming Register. The first word should be 32769 (8001 hex), the following twenty-six 16-bit words set the frequencies and levels and are in the range 0 to 32767 (0000-7FFF hex).

Word	Value written	Word	Value written
1	32769		
2	Filter #1 coefficient $b2_1$	15	Filter #2 coefficient $b2_1$
3	Filter #1 coefficient $b1_1$	16	Filter #2 coefficient $b1_1$
4	Filter #1 coefficient $b0_1$	17	Filter #2 coefficient $b0_1$
5	Filter #1 coefficient $a2_1$	18	Filter #2 coefficient $a2_1$
6	Filter #1 coefficient $a1_1$	19	Filter #2 coefficient $a1_1$
7	Filter #1 coefficient $b2_2$	20	Filter #2 coefficient $b2_2$
8	Filter #1 coefficient $b1_2$	21	Filter #2 coefficient $b1_2$
9	Filter #1 coefficient $b0_2$	22	Filter #2 coefficient $b0_2$
10	Filter #1 coefficient $a2_2$	23	Filter #2 coefficient $a2_2$
11	Filter #1 coefficient $a1_2$	24	Filter #2 coefficient $a1_2$
12	Freq measurement #1 ncycles	25	Freq measurement #2 ncycles
13	Freq measurement #1 mintime	26	Freq measurement #2 mintime
14	Freq measurement #1 maxtime	27	Freq measurement #2 maxtime

The coefficients are entered as 15-bit signed (two's complement) integer values (the most significant bit of the 16-bit word entered should be zero) calculated as 8192 * coefficient value from the user's filter design program (i.e. this allows for filter design values of -1.9999 to +1.9999).

The design of the IIR filters should make allowance for the fixed receive signal filtering in the Modem which has a low pass characteristic above 1.5kHz of 0.4dB at 2kHz, 1.2dB at 2.5kHz, 2.6dB at 3kHz and 4.1dB at 3.4kHz.

'ncycles' is the number of signal cycles for the frequency measurement.

'mintime' is the smallest acceptable time for ncycles of the input signal expressed as the number of 9.6kHz timer clocks. i.e. 'mintime' = 9600 * ncycles / high frequency limit

'maxtime' is the highest acceptable time for ncycles of the input signal expressed as the number of 9.6kHz timer clocks. i.e. 'maxtime' = 9600 * ncycles / low frequency limit

The level detectors include hysteresis. The threshold levels - measured at a 2-wire line interface with unity gain filters, using typical line interface circuits, 1.0 dB line coupling loss and with the Rx Gain Control block set to 0dB - are nominally:

'Off' to 'On'	-44.5dBm
'On' to 'Off'	-47.0dBm

Note that if any changes are made to the programmed values while the Modem is running in Programmed Tone Detect mode they will not take effect until the Modem is next switched into Programmed Tone Detect mode.

1.6.11.11 Other Registers

C-BUS addresses $E9, $EA and $EB are reserved and should not be accessed.

1.7 Performance Specification

1.7.1 Electrical Performance

1.7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (AV_{DD} - AV_{SS}) or (DV_{DD} - DV_{SS})	-0.3	4.0	V
Voltage on any pin (except VCAP) to AV_{SS} or DV_{SS}	-0.3	V_{DD} + 0.3	V
Voltage between AV_{SS} and DV_{SS}		±50	mV
Voltage between AV_{DD} and DV_{DD}		±300	mV
Current into or out of AV_{SS}, DV_{SS}, AV_{DD} or DV_{DD} pins	-50	+50	mA
Current into RDRVN pin (RDRVN pin low)		+50	mA
Current into or out of any other pin	-20	+20	mA

L8 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		1300	mW
... Derating		27	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

1.7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (AV_{DD} - AV_{SS}) or (DV_{DD} - DV_{SS})		3.0	3.6	V
Rise time (10% - 90%)			25	ms
Operating Temperature		-40	+85	°C
Xtal Frequency		0	12.5	MHz

1.7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = AV_{DD} = DV_{DD} = 3.0V to 3.6V at Tamb = -40 to +85°C, V_{SS} = AV_{SS} = DV_{SS}
Xtal Frequency = 11.0592 or 12.288MHz ± 0.01% (100ppm)[1], 0dBm corresponds to 775mVrms.

DC Parameters		Notes	Min.	Typ.	Max.	Units
I_{DD}	(Zero-Power Mode)	1, 2	-	6	60	µA
	(11.0592 MHz Xtal operating, Idle Mode)	1, 2	-	0.8	-	mA
	(32.768 kHz Xtal operating, Idle Mode)	1, 2	-	7	-	µA
	(5.5 MHz RC Oscillator only, Idle Mode)	1, 2	-	320	-	µA
	(ADC only, excluding 11.0592 MHz Xtal)	1, 3	-	330	-	µA
	(CAS Detector and FSK Receiver only, excluding 11.0592MHz Xtal)	1	-	350	-	µA
	(Keyboard encoder only, no auto-sleep, no key pressed, excluding 32.768 kHz Xtal)	1	-	7	-	µA
	(PWM only, one output at 50%, excluding 11.0592 MHz Xtal)	1	-	30	-	µA
	(Real Time Clock [RTC] only, excluding 32.768 kHz Xtal)	1	-	6	-	µA
	(Watchdog Timer [WDT] only, excluding 32.768 kHz Xtal)	1	-	6	-	µA
	(Modem [Rx, Tx, C-BUS and signal paths] operating, excluding 8051 Core)	1	-	3.5	-	mA
	(8051 Core operating, excluding Modem)	1	-	3.1	-	mA
	(8051 Core operating, including Modem)	1	-	6.6	16.0	mA
Logic '1' Input Level		4	70%	-	-	DV_{DD}
Logic '0' Input Level		4	-	-	30%	DV_{DD}
Logic Input Leakage Current (Vin = 0 to DV_{DD}), (excluding XTAL/CLOCK inputs)			-1.0	-	+1.0	µA
Output Logic '1' Level - Ports 1, 3, 4, 5 and pin X32KN (configured as output) @ I_{OH} = 1 mA			80%	-	-	DV_{DD}
Output Logic '0' Level - Ports 1, 3, 4, 5 and pin X32KN (configured as output) @ I_{OL} = -1.5 mA			-	-	0.4	V
Output Logic '1' Level - D7-0, A15-0, WEN, OEN, CSN1, CSN2, CSN3 @ I_{OH} = 2 mA			80%	-	-	DV_{DD}
Output Logic '0' Level - D7-0, A15-0, WEN, OEN, CSN1, CSN2, CSN3 @ I_{OL} = -3 mA			-	-	0.4	V
Schmitt triggers input high-going threshold (Vthi) (see Figure 16)			$0.56DV_{DD}$	-	$0.56DV_{DD}$ + 0.6V	V
Schmitt triggers input low-going threshold (Vtlo) (see Figure 16)			$0.44DV_{DD}$ - 0.6V	-	$0.44DV_{DD}$	V
RDRVN 'ON' resistance to DV_{SS} (DV_{DD}= 3.3V)			-	50	70	Ω
RDRVN 'OFF' resistance to DV_{DD} (DV_{DD}= 3.3V)			-	1170	3000	Ω
Port pull-up and Data pin bushold resistance			25	50	85	kΩ

XTAL/CLOCK Input (timing for an external clock input to XTAL pin only)	Notes	Min.	Typ.	Max.	Units
'High' Pulse Width		30	-	-	ns
'Low' Pulse Width		30	-	-	ns

[1] Only 11.0592MHz supports a standard 19,200 serial port baud rate when executing on-chip BOOT ROM. See section 1.4.4 Local BOOT ROM.

Transmit QAM and DPSK Modes (V.22, Bell 212A, V.22 bis)	Notes	Min.	Typ.	Max.	Units
Carrier frequency, high band	5	-	2400	-	Hz
Carrier frequency, low band	5	-	1200	-	Hz
Baud rate	6	-	600	-	Baud
Bit rate (V.22, Bell 212A)	6	-	1200/600	-	bps
Bit rate (V.22 bis)	6	-	2400	-	bps
550Hz guard tone frequency		548	550	552	Hz
550Hz guard tone level wrt data signal		-4.0	-3.0	-2.0	dB
1800Hz guard tone frequency		1797	1800	1803	Hz
1800Hz guard tone level wrt data signal		-7.0	-6.0	-5.0	dB

Transmit V.21 FSK Mode	Notes	Min.	Typ.	Max.	Units
Baud rate	6	-	300	-	Baud
Mark (logical 1) frequency, high band		1647	1650	1653	Hz
Space (logical 0) frequency, high band		1847	1850	1853	Hz
Mark (logical 1) frequency, low band		978	980	982	Hz
Space (logical 0) frequency, low band		1178	1180	1182	Hz

Transmit Bell 103 FSK Mode	Notes	Min.	Typ.	Max.	Units
Baud rate	6	-	300	-	Baud
Mark (logical 1) frequency, high band		2222	2225	2228	Hz
Space (logical 0) frequency, high band		2022	2025	2028	Hz
Mark (logical 1) frequency, low band		1268	1270	1272	Hz
Space (logical 0) frequency, low band		1068	1070	1072	Hz

Transmit V.23 FSK Mode	Notes	Min.	Typ.	Max.	Units
Baud rate	6	-	1200/75	-	Baud
Mark (logical 1) frequency, 1200 baud		1298	1300	1302	Hz
Space (logical 0) frequency, 1200 baud		2097	2100	2103	Hz
Mark (logical 1) frequency, 75 baud		389	390	391	Hz
Space (logical 0) frequency, 75 baud		449	450	451	Hz

Transmit Bell 202 FSK Mode	Notes	Min.	Typ.	Max.	Units
Baud rate	6	-	1200/150	-	Baud
Mark (logical 1) frequency, 1200 baud		1198	1200	1202	Hz
Space (logical 0) frequency, 1200 baud		2197	2200	2203	Hz
Mark (logical 1) frequency, 150 baud		386	387	388	Hz
Space (logical 0) frequency, 150 baud		486	487	488	Hz

DTMF/Single Tone Transmit	Notes	Min.	Typ.	Max.	Units
Tone frequency accuracy		-0.2	-	+0.2	%
Distortion	7	-	1.0	2.0	%

Transmit Output Level	Notes	Min.	Typ.	Max.	Units
Modem and Single Tone modes	7	-3.2	-2.2	-1.2	dBm
DTMF mode, Low Group tones	7	-1.2	-0.2	+0.8	dBm
DTMF: level of High Group tones wrt Low Group	7	+1.0	+2.0	+3.0	dB
Tx output buffer gain control accuracy	7	-0.25	-	+0.25	dB

Receive QAM and DPSK Modes (V.22, Bell 212A, V.22 bis)	Notes	Min.	Typ.	Max.	Units
Carrier frequency (high band)		2392	2400	2408	Hz
Carrier frequency (low band)		1192	1200	1208	Hz
Baud rate	9	-	600	-	Baud
Bit rate (V.22, Bell 212A)	9	-	1200/600	-	bps
Bit rate (V.22 bis)	9	-	2400	-	bps

Receive V.21 FSK Mode	Notes	Min.	Typ.	Max.	Units
Acceptable baud rate		297	300	303	Baud
Mark (logical 1) frequency, high band		1638	1650	1662	Hz
Space (logical 0) frequency, high band		1838	1850	1862	Hz
Mark (logical 1) frequency, low band		968	980	992	Hz
Space (logical 0) frequency, low band		1168	1180	1192	Hz

Receive Bell 103 FSK Mode	Notes	Min.	Typ.	Max.	Units
Acceptable baud rate		297	300	303	Baud
Mark (logical 1) frequency, high band		2213	2225	2237	Hz
Space (logical 0) frequency, high band		2013	2025	2037	Hz
Mark (logical 1) frequency, low band		1258	1270	1282	Hz
Space (logical 0) frequency, low band		1058	1070	1082	Hz

Receive V.23 FSK Mode	Notes	Min.	Typ.	Max.	Units
1200 baud					
Acceptable baud rate		1188	1200	1212	Baud
Mark (logical 1) frequency		1280	1300	1320	Hz
Space (logical 0) frequency		2080	2100	2120	Hz
75 baud					
Acceptable baud rate		74	75	76	Baud
Mark (logical 1) frequency		382	390	398	Hz
Space (logical 0) frequency		442	450	458	Hz

Receive Bell 202 FSK Mode	Notes	Min.	Typ.	Max.	Units
1200 baud					
Acceptable baud rate		1188	1200	1212	Baud
Mark (logical 1) frequency		1180	1200	1220	Hz
Space (logical 0) frequency		2180	2200	2220	Hz
150 baud					
Acceptable baud rate		148	150	152	Baud
Mark (logical 1) frequency		377	387	397	Hz
Space (logical 0) frequency		477	487	497	Hz

Rx Modem Signal	Notes	Min.	Typ.	Max.	Units
Signal level	10	-45.0	-	-9.0	dBm
Signal to Noise Ratio (noise flat 300-3400Hz)		20.0	-	-	dB

Rx Modem S1 Pattern Detector (DPSK and QAM modes)	Notes	Min.	Typ.	Max.	Units
Will detect S1 pattern lasting for		90.0	-	-	ms
Will not detect S1 pattern lasting for				72.0	
Hold time (minimum detector 'On' time)		5.0	-	-	ms

Rx Modem Continuous 1s and 1010.. Pattern Detectors	Notes	Min.	Typ.	Max.	Units
Turn on time		32	-	40	bit-times
Turn off time		12	-	20	bit-times

Rx Modem Energy Detector	Notes	Min.	Typ.	Max.	Units
Detect threshold ('Off' to 'On)	10,11	-	-	-43.0	dBm
Undetect threshold ('On' to 'Off')	10,11	-48.0	-	-	dBm
Hysteresis	10,11	2.0	-	-	dB
Detect ('Off' to 'On') response time					
1200 baud FSK mode	10,11	8.0	-	30.0	ms
150 and 75 baud FSK modes	10,11	16.0	-	60.0	ms
Undetect ('On' to 'Off') response time					
1200 baud FSK mode	10,11	10.0	-	40.0	ms
150 and 75 baud FSK modes	10,11	20.0	-	80.0	ms

Rx Answer Tone Detectors	Notes	Min.	Typ.	Max.	Units
Detect threshold ('Off' to 'On)	10, 12	-	-	-43.0	dBm
Undetect threshold ('On' to 'Off')	10, 12	-48.0	-	-	dBm
Detect ('Off' to 'On') response time	10, 12	30.0	33.0	45.0	ms
Undetect ('On' to 'Off') response time	10, 12	7.0	18.0	25.0	ms
2100Hz detector					
'Will detect' frequency		2050	-	2160	Hz
'Will not detect' frequency		-	-	2000	Hz
2225Hz detector					
'Will detect' frequency		2160	-	2285	Hz
'Will not detect' frequency		2335	-	-	Hz

Rx Call Progress Energy Detector	Notes	Min.	Typ.	Max.	Units
Bandwidth (-3dB points) See Figure 11a		275	-	665	Hz
Detect threshold ('Off' to 'On)	10,13	-	-	-37.0	dBm
Undetect threshold ('On' to 'Off')	10,13	-42.0	-	-	dBm
Detect ('Off' to 'On') response time	10,13	30.0	36.0	45.0	ms
Undetect ('On' to 'Off') response time	10,13	6.0	8.0	50.0	ms

Receive Input Amplifier	Notes	Min.	Typ.	Max.	Units
Input impedance (at 100Hz)		10.0			MΩ
Open loop gain (at 100Hz)			10000		V/V
Rx Gain Control Block accuracy		-0.25		+0.25	dB

DTMF Decoder	Notes	Min.	Typ.	Max.	Unit
Valid input signal levels (each tone of composite signal)	10	-30.0	-	0	dBm
Not decode level (either tone of composite signal)	10	-	-	-36.0	dBm
Twist = High Tone/Low Tone		-10.0	-	6.0	dB
Frequency Detect Bandwidth		±1.8	-	±3.5	%
Max level of low frequency noise (i.e dial tone)					
Interfering signal frequency <= 550Hz	14	-	-	0	dB
Interfering signal frequency <= 450Hz	14	-	-	10.0	dB
Interfering signal frequency <= 200Hz	14	-	-	20.0	dB
Max. noise level with respect to the signal	14,15	-	-	-10.0	dB
DTMF detect response time		-	-	40.0	ms
DTMF de-response time		-	-	30.0	ms
Status Register b5 high time		14.0	-	-	ms
'Will Detect' DTMF signal duration		40.0	-	-	ms
'Will Not Detect' DTMF signal duration		-	25.0	-	ms
Pause length detected		30.0	-	-	ms
Pause length ignored		-	-	15.0	ms

Tone Alert (CAS) Detector	Notes	Min.	Typ.	Max.	Units
'Low' Tone nominal frequency			2130		Hz
'Low' Tone nominal frequency			2750		Hz
Start of Tone Alert signal to DET high time (Tton)			55.0		ms
End of Tone Alert signal to DET high time (Ttoff)		0.5		17.0	ms
DET high time to ensure interrupt status bit in CASDET goes high (TqCAS)	16	8.0		45.0 to 80.0	ms
To Ensure Detection					
'Low' Tone frequency tolerance				±0.5	%
'High' Tone frequency tolerance				±0.5	%
Level (per tone)		-40.0		-2.2	dBV
2750Hz tone level wrt 2130Hz tone level		-6.0		+6.0	dB
Signal to Noise ratio		20.0			dB
Dual Tone burst duration for DET output		75			ms
Dual Tone burst duration to ensure interrupt status bit goes high.	16	75		85 to 120	ms
To Ensure non-detection					
'Low' Tone frequency tolerance		±75			Hz
'High' Tone frequency tolerance		±95			Hz
Level (total)				-46.0	dBV
Dual Tone burst duration				45.0	ms

FSK Receiver	Notes	Min.	Typ.	Max.	Units
Transmission Rate		1188	1200	1212	Baud
V23 Mark (logical 1) frequency		1280	1300	1320	Hz
V23 Space (logical 0) frequency		2068	2100	1320	Hz
Bell202 Mark (logical 1) frequency		1188	1200	1212	Hz
Bell202 Space (logical 0) frequency		2178	2200	2222	Hz
Valid input level range		-40.0		-8.0	dBV
Acceptable twist (mark level wrt space level)					
V23		-6.0		+6.0	dB
Bell202		-10.0		+10.0	dB
Acceptable Signal to Noise ratio					
V23	15	20.0			dB
Bell202	15	30.0			dB
Level Detector 'on' threshold level				-40.0	dBV
Level Detector 'off' to 'on' time (Fig 7b Teon)				25.0	ms
Level Detector 'on' to 'off' time (Fig 7b Teoff)		8.0			ms

Analogue to Digital Convertor (excluding track/hold)	Notes	Min.	Typ.	Max.	Units
Resolution			10		Bits
Conversion Time	17		156		System Clock Cycles
Integral non-linearity	18			2	LSBs
Differential non-linearity	19			1	LSBs
Zero Error		-20		20	mV
VRef Generator Power Up Time (after enable)				100	µs
VRef Generator Voltage Output		2.25	2.5	2.75	V

RC Oscillator	Notes	Min.	Typ.	Max.	Units
Frequency		2.5	5.5	9.5	MHz
Start-up time			0.5	4	µs

Notes:

1. At AV_{DD} = DV_{DD} = 3.3V and Tamb = 25°C, not including any current drawn from the CMX850 pins by external circuitry other than X1, X2, C8, C9, C10, and C11.
2. All logic inputs at DV_{SS} except for RESETN, HT, RT and inputs which are at DV_{DD}.
3. Continuous conversion at maximum rate, with internal reference and threshold compare.
4. Excluding RESETN, RD, RT, HD and HT pins.
5. % carrier frequency accuracy is the same as XTAL/CLOCK % frequency accuracy.
6. Tx signal % baud or bit rate accuracy is the same as XTAL/CLOCK % frequency accuracy.
7. Measured across the line using the components recommended in section 1.4.4 with Tx Level Control gain set to 0dB, at AV_{DD} = 3.3V (levels are proportional to AV_{DD}).
   Level measurements for all modem modes are performed with random transmitted data and without any guard tone. 0dBm = 775mVrms. DTMF twist set to +2.0dB.
8. Measured on the 2-wire line using the line interface circuits described in section 1.4.4 with the Tx line signal level set to -10dBm for FSK or single tones, -6dBm and -8dBm for DTMF tones. Excludes any distortion due to external components required for line coupling.
9. These are the bit and baud rates of the line signal, the acceptable tolerance is ±0.01%.
10. Rx 2-wire line signal level assuming 1dB loss in line coupling components with Rx Gain Control block set to 0dB and external components recommended in section 1.4.4.
11. Thresholds and times measured with continuous binary '1' for all FSK modes. Fixed compromise line equaliser enabled. Signal switched between off and -33dBm.
12. 'Typical' value refers to 2100Hz or 2225Hz signal switched between off and -33dBm. Times measured with respect to the received line signal.
13. 'Typical' values refers to 400Hz signal switched between off and -33dBm.
14. Referenced to DTMF tone of lower amplitude.
15. Flat Gaussian Noise in 300-3400Hz band.
16. This depends upon the Tone Detect Window Control Bits. (see section 1.5.13)
17. Actual Time dependant on the clock frequency selected and XTAL used for the System Clock.
18. Integral non-linearity is defined as the width difference between an actual code midpoint and the line of best fit through all code midpoints, divided by the width of an ideal LSB.
19. Differential non-linearity is defined as the difference between adjacent code midpoints and the width of an ideal LSB, divided by the width of an ideal LSB.
20. Increased by $12T_{CLCL}$ when a "stretch" cycle is selected.

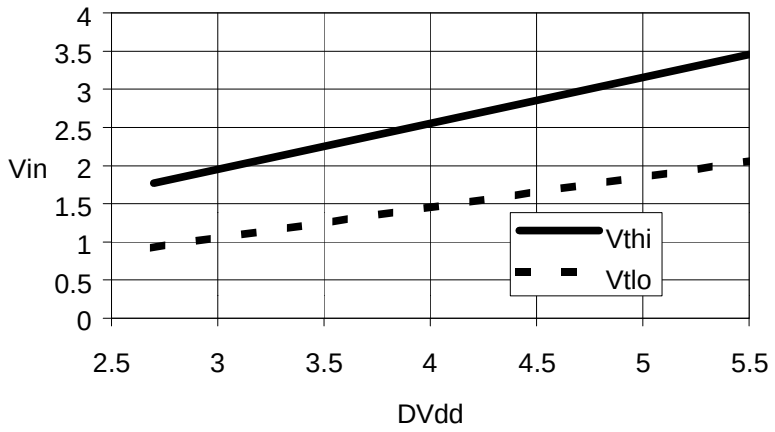


Figure 16 Typical Schmitt Trigger Input Voltage Thresholds vs. DV_{DD}

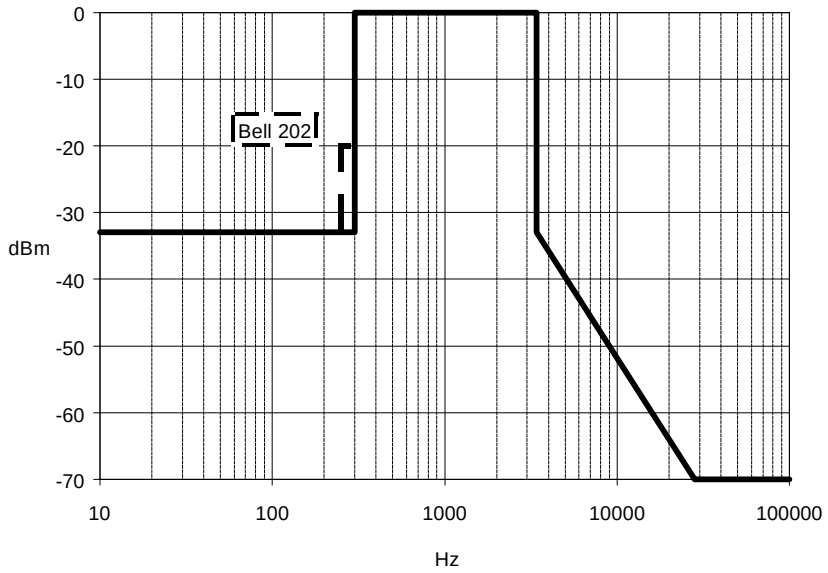
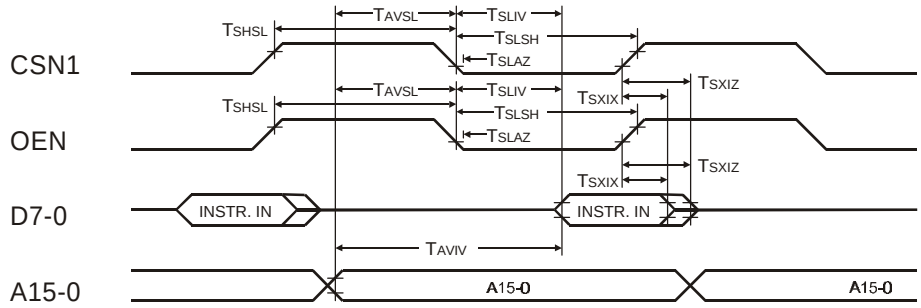


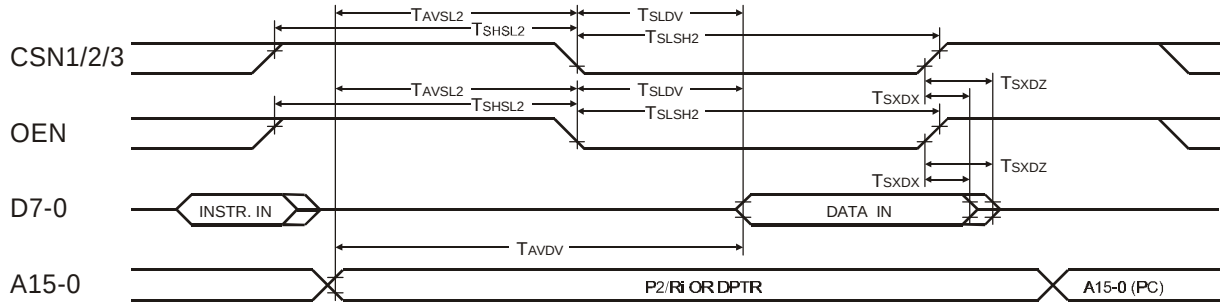
Figure 17 Maximum Out of Band Tx Line Energy Limits (see note 8)

1.7.1.3 Operating Characteristics (continued)

EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA READ CYCLE



EXTERNAL DATA WRITE CYCLE

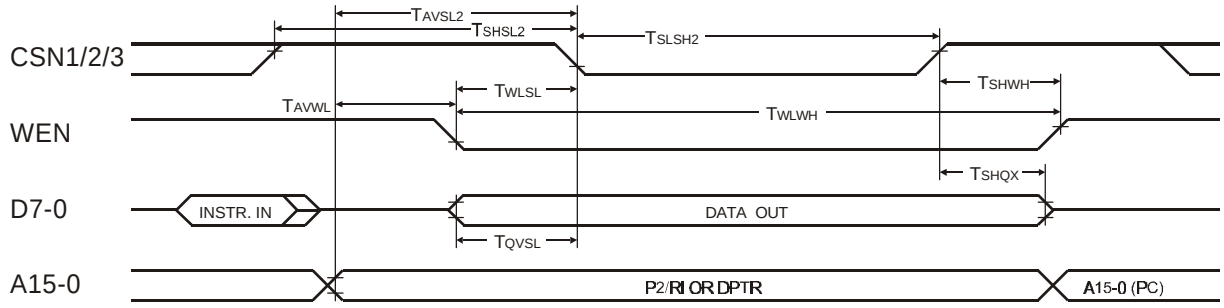
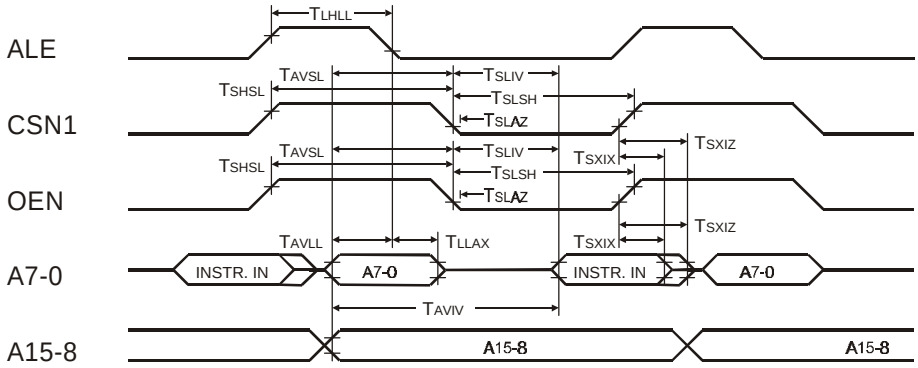


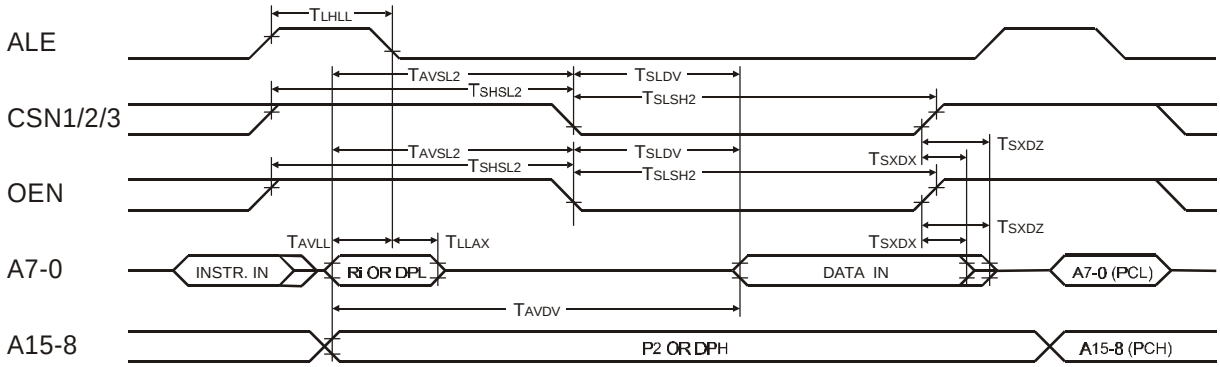
Figure 18 Non-Multiplexed Memory Interface Timing Diagrams

1.7.1.3 Operating Characteristics (continued)

EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA READ CYCLE



EXTERNAL DATA WRITE CYCLE

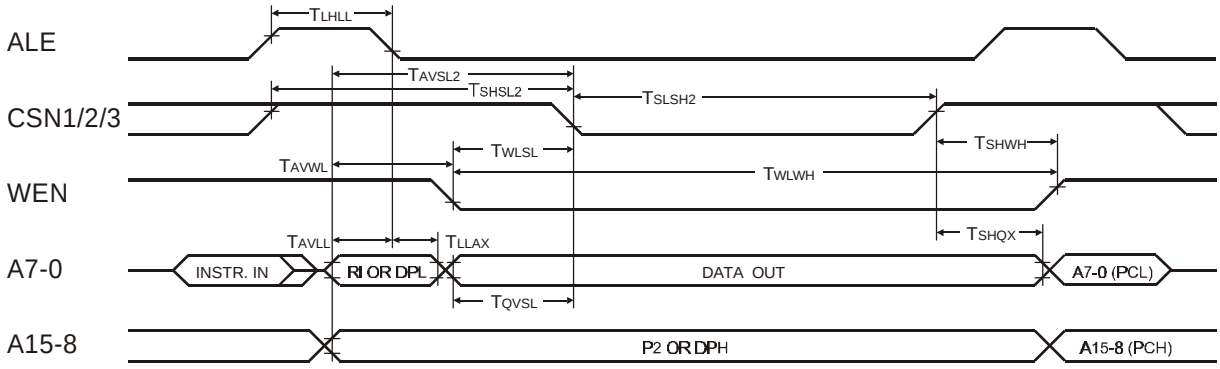


Figure 19 Multiplexed Memory Interface Timing Diagrams

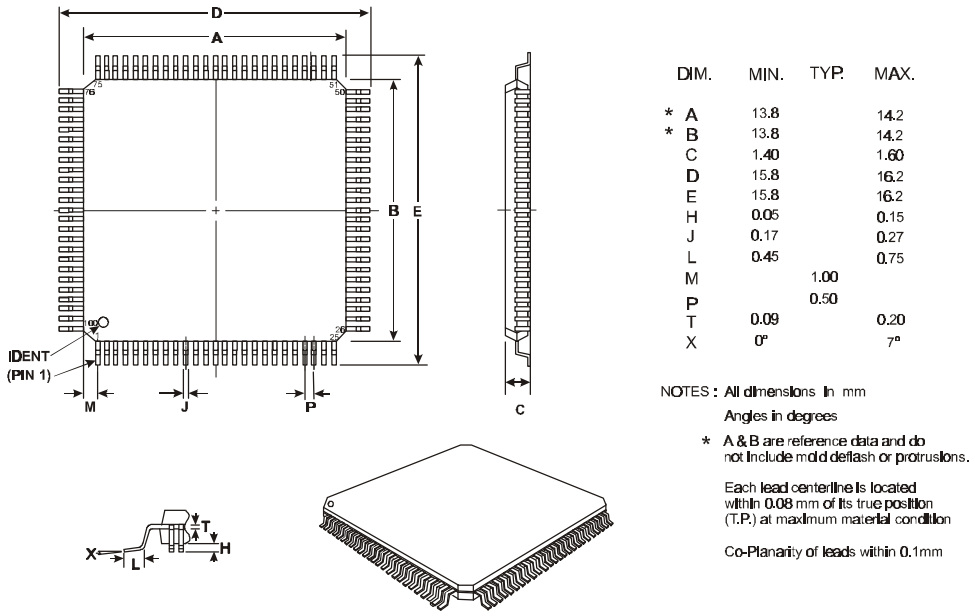
1.7.1.3 Operating Characteristics (continued)

For the following conditions unless otherwise specified:

Pin capacitance = 50pF
V_{DD} = 3.0V to 3.6V, Tamb = - 40°C to +85°C

Symbol	Parameter	Notes	Min.	Max.	Units
T_{CLCL}	Oscillator period		80		ns
T_{AVDV}	Address valid to valid data in	20		$9T_{CLCL}$-175	ns
T_{AVIV}	Address valid to valid instruction in			$5T_{CLCL}$-115	ns
T_{AVLL}	Address valid to ALE low		T_{CLCL}-40		ns
T_{AVSL}	Address valid to CSN1 or OEN low (instruction)		$2T_{CLCL}$-130		ns
T_{AVSL2}	Address valid to CSN1/2/3 or OEN low (data)		$4T_{CLCL}$-130		ns
T_{AVWL}	Address valid to WEN low		$2T_{CLCL}$-130		ns
T_{LHLL}	ALE pulse width		$2T_{CLCL}$-40		ns
T_{LLAX}	Address hold after ALE low		T_{CLCL}-30		ns
T_{QVSL}	Data valid to CSN1/2/3 low		$2T_{CLCL}$-50		ns
T_{SHQX}	Data hold after CSN1/2/3 high		$2T_{CLCL}$-50		ns
T_{SHSL}	CSN1 or OEN high (instruction)		$3T_{CLCL}$-40		ns
T_{SHSL2}	CSN1/2/3 or OEN high (data)		$5T_{CLCL}$-40		ns
T_{SHWH}	WEN hold after CSN1/2/3 high		$2T_{CLCL}$-40		ns
T_{SLAZ}	CSN1 or OEN low to address float			10	ns
T_{SLDV}	CSN1/2/3 or OEN to valid data in	20		$5T_{CLCL}$-175	ns
T_{SLIV}	CSN1 or OEN to valid instruction in			$3T_{CLCL}$-115	ns
T_{SLSH}	CSN1 or OEN pulse width (instruction)		$3T_{CLCL}$-40		ns
T_{SLSH2}	CSN1/2/3 or OEN pulse width (data)	20	$6T_{CLCL}$-40		ns
T_{SXDX}	Data hold after CSN1/2/3 or OEN transition		0		ns
T_{SXDZ}	Data float after CSN1/2/3 or OEN transition			$2T_{CLCL}$-60	ns
T_{SXIX}	Instruction hold after CSN1 or OEN transition		0		ns
T_{SXIZ}	Instruction float after CSN1 or OEN transition			T_{CLCL}-25	
T_{WLSL}	WEN low to CSN1/2/3 low		$2T_{CLCL}$-40		ns
T_{WLWH}	WEN pulse width	20	$10T_{CLCL}$-40		ns

1.7.2 Packaging



DIM.	MIN.	TYP.	MAX.
* A	13.8		14.2
* B	13.8		14.2
C	1.40		1.60
D	15.8		16.2
E	15.8		16.2
H	0.05		0.15
J	0.17		0.27
L	0.45		0.75
M		1.00	
P		0.50	
T	0.09		0.20
X	0°		7°

NOTES : All dimensions in mm
Angles in degrees

* A & B are reference data and do not include mold deflash or protrusions.

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition

Co-Planarity of leads within 0.1mm

Figure 20 100-pin LQFP (L8) Mechanical Outline: *Order as part no. CMX850L8*

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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