

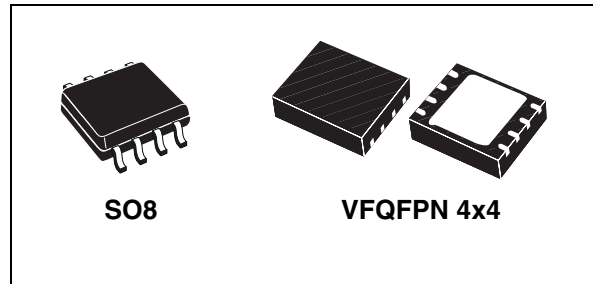
4 A peak step-down switching regulator

Features

- 4 A peak output current
- 4.0 V to 18 V input voltage
- Output voltage adjustable from 0.8 V
- 850 kHz switching frequency
- Internal soft-start
- Integrated 95 mΩ and 69 mΩ Power MOSFETs
- All ceramic capacitor
- Power Good or enable
- Cycle by cycle current limiting
- Current fold back short circuit protection
- VFQFPN4x4-8L, HSOP-8 and SO-8 and packages

Applications

- μ P/ASIC/DSP/FPGA core and I/O supplies
- Point of load for: STB, TVs, DVD
- Optical storage, Hard disk drive, Printers, Audio/Graphic cards



Description

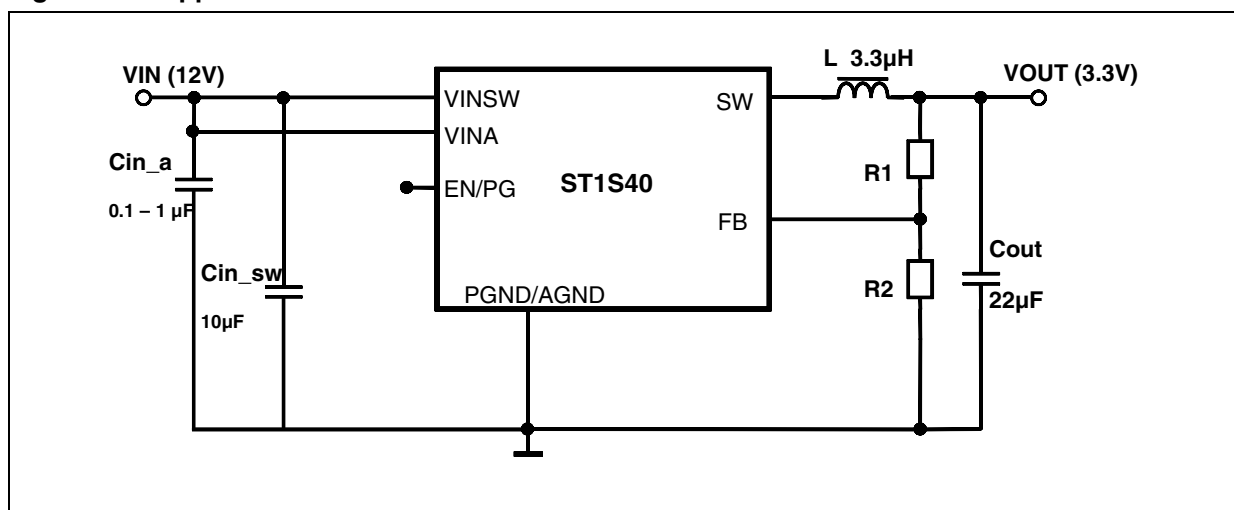
The ST1S40 is an internally compensated 850 kHz fixed-frequency PWM synchronous step-down regulator. ST1S40 operates from 4.0 V to 18 V input, while it regulates an output voltage as low as 0.8 V and up to V_{IN} .

The ST1S40 integrates 95 mΩ high side switch and 69 mΩ synchronous rectifier allowing very high efficiency with very low output voltages.

The peak current mode control with internal compensation delivers very compact solution with a minimum component count.

The ST1S40 is available in VFQFPN 4mm x 4mm 8 leads package, HSOP-8 and standard SO-8.

Figure 1. Application circuit



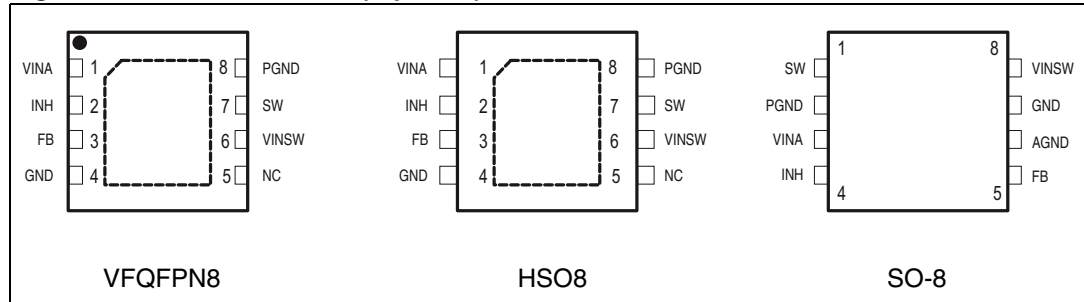
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1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

N.		Type	Description
VFQFPN and HSOP8	S08-BW		
1	3	VINA	Unregulated DC input voltage
2	4	EN/PG	Enable input. With EN higher than 1.2V the device in ON and with EN lower than 0.4V the device is OFF (ST1S40lxx). Open drain Power Good (POR) pin. It is released (open drain) when the output voltage is higher than $0.92 \cdot V_{OUT}$. If the output voltage is below $0.92 \cdot V_{OUT}$, the PG pin goes to low impedance immediately. If PG is not used, it can be left floating or to GND (ST1S40xx).
3	5	FB	Feedback input. Connecting the output voltage directly to this pin the output voltage is regulated at 0.8V. To have higher regulated voltages an external resistor divider is required from Vout to FB pin.
4	6	AGND	Ground
5	-	NC	
6	8	VINSW	Power input voltage
7	1	SW	Regulator output switching pin
8	2	PGND	Power ground
-	7		Ground

2 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{INSW}	Power input voltage	-0.3 to 20	V
V_{INA}	Input voltage	-0.3 to 20	
V_{EN}	Enable voltage	-0.3 to V_{INA}	
V_{SW}	Output switching voltage	-1 to V_{IN}	
V_{PG}	Power Good	-0.3 to V_{IN}	
V_{FB}	Feedback voltage	-0.3 to 2.5	
I_{FB}	FB current	-1 to +1	mA
P_{TOT}	Power dissipation at $T_A < 60^\circ\text{C}$	2,25 (HSOP8/DFN4x4); 1,6 SO8-BW	W
T_{OP}	Operating Junction temperature range	-40 to 125	$^\circ\text{C}$
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$

3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Maximum thermal resistance junction-ambient ⁽¹⁾	VFQFPN	40
		HSOP8	40
		SO8-BW	55
			$^\circ\text{C}/\text{W}$

1. Package mounted on demonstration board.

4 Electrical characteristics

$T_J=25\text{ }^\circ\text{C}$, $V_{CC}=12\text{ V}$, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
V_{IN}	Operating input voltage range	(1)	4		18	V
V_{INON}	Turn on V_{CC} threshold	(1)		2.9		
V_{INHYS}	Threshold hysteresis	(1)		0.250		
R_{DSON-P}	High side switch on resistance	$I_{SW}=750\text{mA}$		95		$\text{m}\Omega$
R_{DSON-N}	Low side switch on resistance	$I_{SW}=750\text{mA}$		69		$\text{m}\Omega$
I_{LIM}	Maximum limiting current	(2)	4.0		6.0	A
Oscillator						
F_{SW}	Switching frequency		0.7	0.85	1	MHz
D_{MAX}	Maximum Duty Cycle	(2)	100			%
Dynamic characteristics						
V_{FB}	Feedback voltage		0.784	0.8	0.816	V
		(1)	0.776	0.8	0.824	
$\%V_{OUT}/\Delta I_{OUT}$	Reference load regulation	$I_{SW}=10\text{mA}$ to I_{LIM} (2)		0.5		%
$\%V_{OUT}/\Delta V_{IN}$	Reference line regulation	$V_{IN}=4.0\text{V}$ to 18V (2)		0.4		%
DC characteristics						
I_Q	Quiescent current	Duty Cycle=0, no load $V_{FB}=1.2\text{V}$		1.5	2.5	mA
I_{QST-BY}	Total stand-by quiescent current	OFF		2	15	μA
IFB	FB bias current			50		
Enable						
V_{EN}	EN threshold voltage	Device ON level	1.2			V
		Device OFF level			0.4	
I_{EN}	EN current			2		μA

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
Power Good						
PG	PG threshold			92		%V _{FB}
	PG output voltage low	Isink=6 mA open drain			400	mV
Soft start						
T _{SS}	Soft start duration			1		ms
Protection						
T _{SHDN}	Thermal shutdown			150		°C
	Hysteresis			15		

1. Specification referred to T_J from -40 to +125°C. Specification in the -40 to +125°C temperature range are assured by design, characterization and statistical correlation.
2. Guaranteed by design.

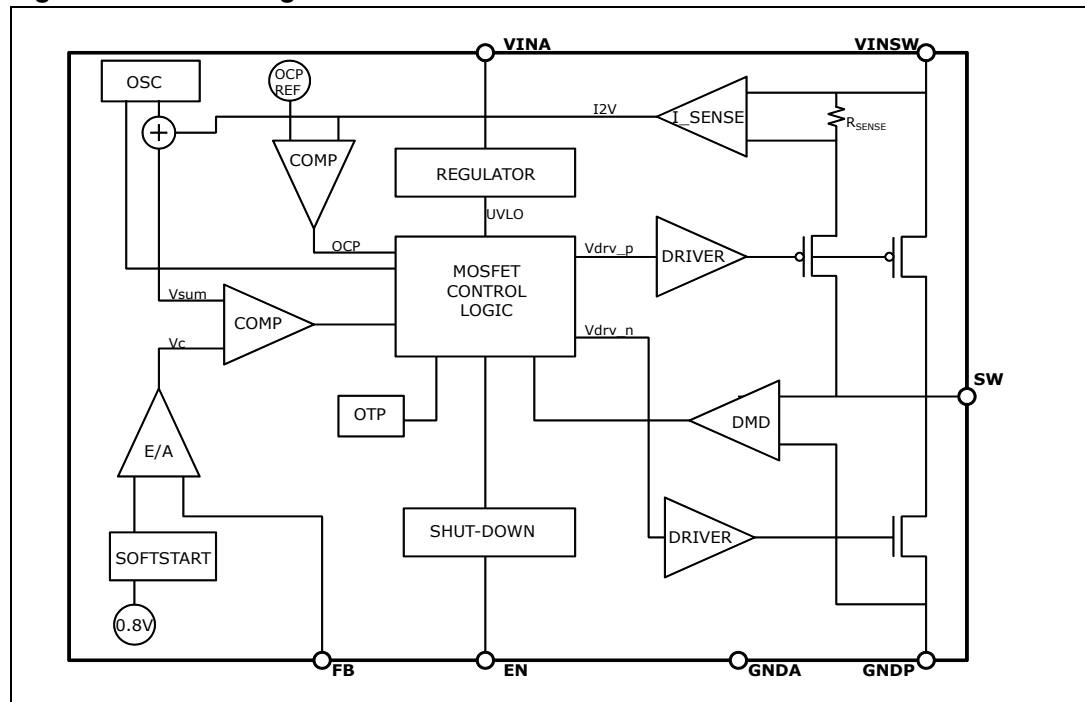
5 Functional description

The ST1S40 is based on a “peak current mode”, constant frequency control. The output voltage V_{OUT} is sensed by the feedback pin (FB) compared to an internal reference (0.8V) providing an error signal that, compared to the output of the current sense amplifier, controls the ON and OFF time of the power switch.

The main internal blocks are shown in the block diagram in [Figure 3](#). They are:

- A fully integrated oscillator that provides the internal clock and the ramp for the slope compensation avoiding sub harmonic instability
- The soft start circuitry to limit inrush current during the start up phase.
- The Transconductance Error Amplifier with integrated compensation network
- The pulse width modulator and the relative logic circuitry necessary to drive the internal power switches.
- The drivers for embedded p-channel and n-channel power MOSFET switches.
- The high side current sensing block.
- The low side current sense to implement diode emulation.
- A voltage monitor circuitry (UVLO) that checks the input and internal voltages.
- A thermal shutdown block, to prevent thermal run away.

Figure 3. Block diagram



6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 5. VFQFPN8 (4x4x1.08mm) mechanical data

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1		0.02	0.05		0.0008	0.0020
A3		0.20			0.0079	
b	0.23	0.30	0.38	0.009	0.0117	0.0149
D	3.90	4.00	4.10	0.153	0.157	0.161
D2	2.82	3.00	3.23	0.111	0.118	0.127
E	3.90	4.00	4.10	0.153	0.157	0.161
E2	2.05	2.20	2.30	0.081	0.087	0.091
e		0.80			0.031	
L	0.40	0.50	0.60	0.016	0.020	0.024

Figure 4. Package dimensions

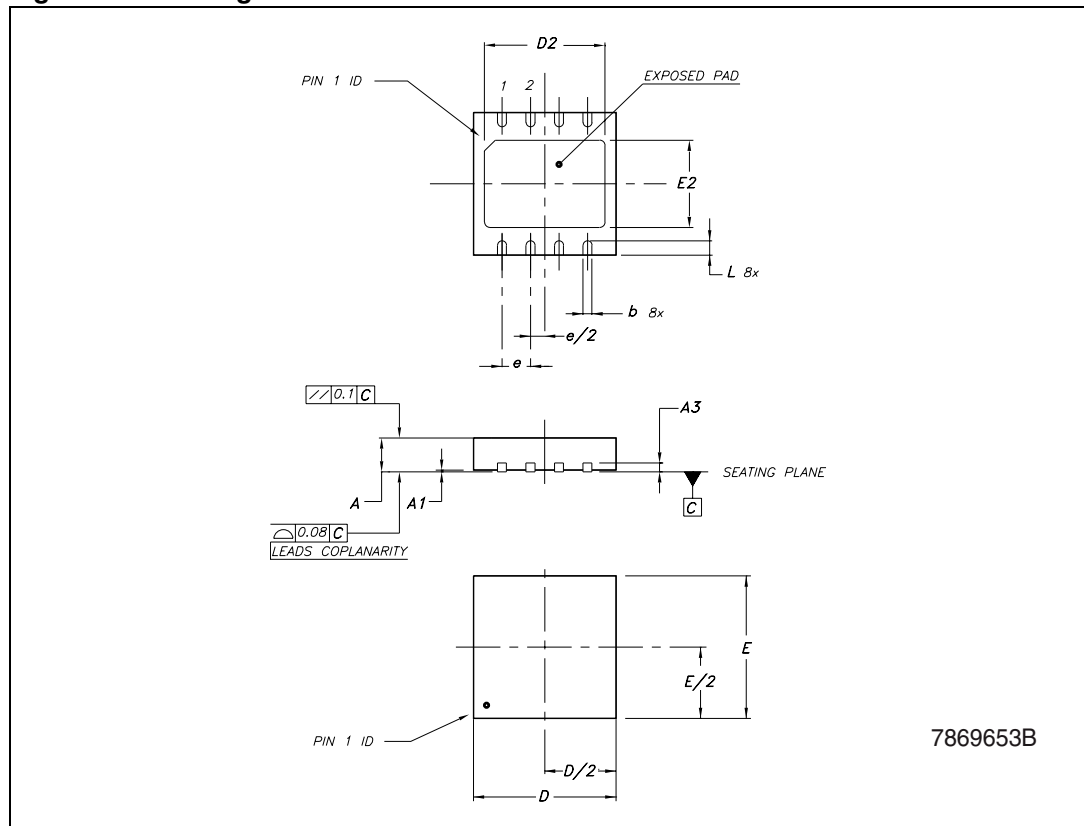


Table 6. SO8-BW Mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.001
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.01
D ⁽¹⁾	4.80		5.00	0.1890	0.1929	0.1969
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.0098		0.0197
L	0.40		1.27	0.0157		0.0500
k	0°(min.), 8° (max.)					
ddd			0.10			0.0039

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

Figure 5. Package dimensions

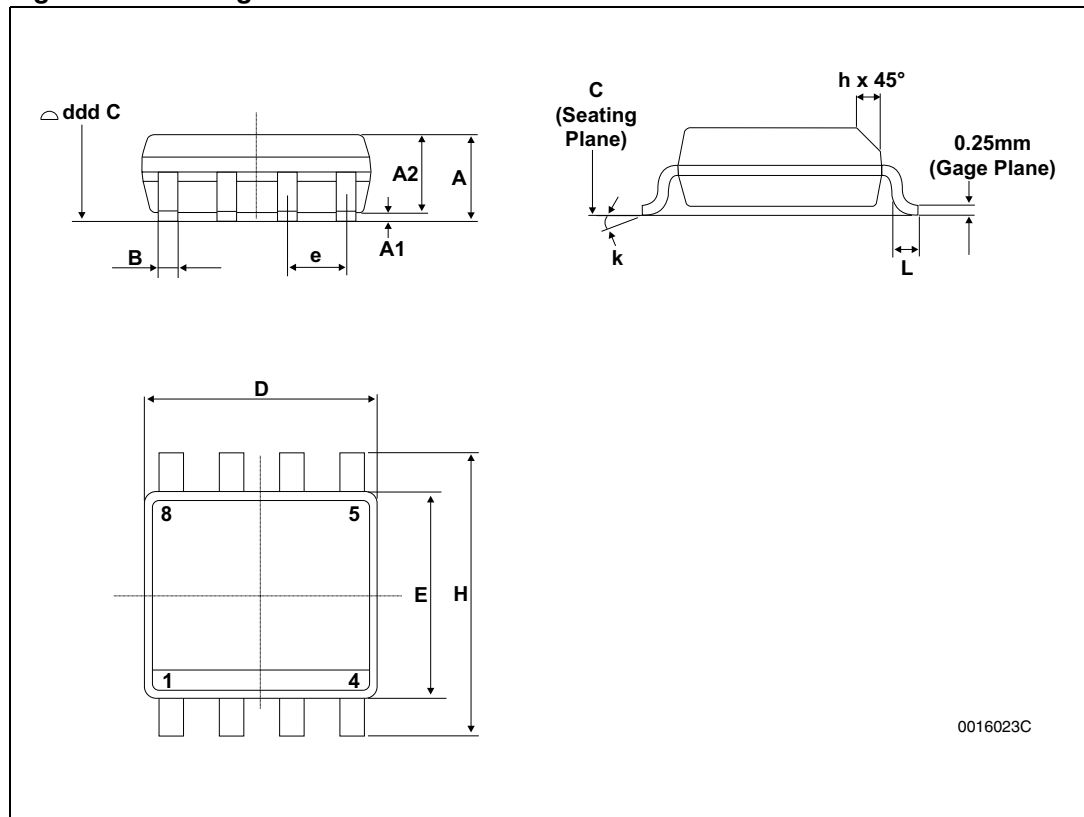
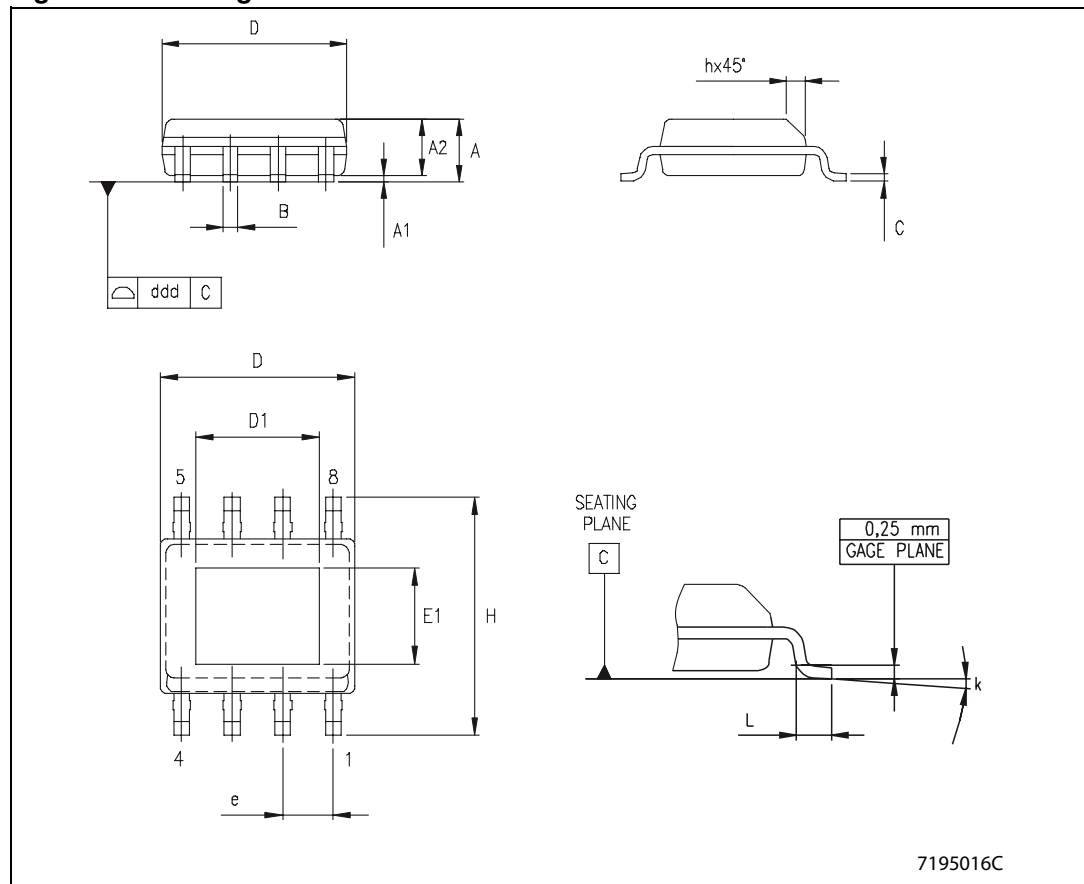


Table 7. HSOP8 Mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.70			0.0669
A1	0.00		0.15		0.00	0.0059
A2	1.25			0.0492		
b	0.31		0.51	0.0122		0.0201
c	0.17		0.25	0.0067		0.0098
D	4.80	4.90	5.00	0.1890	0.1929	0.1969
E	5.80	6.00	6.20	0.2283		0.2441
E1	3.80	3.90	4.00	0.1496		0.1575
e		1.27				
h	0.25		0.50	0.0098		0.0197
L	0.40		1.27	0.0157		0.0500
k	0		8			0.3150
ccc			0.10			0.0039

Figure 6. Package dimensions



7 Order codes

Table 8. Ordering information

Order codes	Package	Function
ST1S40IPUR	VFQFPN 4x4 8L	Enable
ST1S40IPHR	HSOP8	
ST1S40IDR	SO8-BW	
ST1S40PUR	VFQFPN 4x4 8L	Power Good
ST1S40PHR	HSOP8	
ST1S40DR	SO8-BW	

8 Revision history

Table 9. Document revision history

Date	Revision	Changes
15-Dec-2010	1	First release
04-Mar-2011	2	Updated Table 1 , Table 2 , Table 3 and Table 8 .

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