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Revisions

Rev	Description	Date	Approved
x1	A70 release placement	23 May 11	TTC
x2	preliminary schematics	27 May 11	TTC
A	Prototype release	22 Jul 11	TTC
AX1	Rev B changes 1.U53- Switch from socketed to non-socketed processor 2.SPI port connections added on secondary connector 3. Zero ohms R added on PTC16 and PTC17 to allow for disconnect from NAND. 4.FB_AD[31:24] is connected with EBI_D[7:0] on the primary. 5. Push button labels are placed at PTD0,PTE26 6. VrefH, VrefL are removed from Primary elevator connector. 7.LCD_Contrast tied at PTC18. 8.PTD0,PTD1 nets of U8 are renamed 9.Primary connector pin B21 is connected to PTE19, A9 is connected to PTE18 10.L3(IND_0805) is replaced with R143(R0805) zero ohms resistor Schematics Alignment	24 Oct 11	Peter, Melissa
B	A085 Release	27 Oct 11	
B1	A085 Release - MCU Marketing part number updated as per MCO30515	3 Nov 11	Peter

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Microcontroller Solutions Group

6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: FCP: FIUO: X PUBI:

Designer: K.S Chelvi	Drawing Title: **TWR-K70F120M**	
Drawn by: K.S Chelvi	Page Title: **Table of Contents/Revisions**	
Approved: Peter/Melissa	Size C	Document Number SCH-27166 PDF: SPF-27166 — Rev B1
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1. Unless Otherwise Specified:
   All resistors are in ohms
   All capacitors are in uF
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Power & Ground Nets

NET	VOLTAGE	DESCRIPTION
P5V_USB	5V	Primary input power. Filtered from USB connector. Input to USB power switch.
P5V_SW	5V	Output of USB power switch controlled by the 5V_EN signal from the JM60 MCU. Used by OSBDM voltage translation circuits.
P5V_TRG_USB	5V	Output of USB power switch controlled by the VTRG_EN signal from the JM60 MCU. Provides input to regulator.
P3V3	3.3V	Output of regulator using USB power input (P5V_TRG_USB).
P3V3_MCU	3.3V	MCU digital power. Filtered from P3V3.
VDDA	3.3V	VDDA power for MCU and analog circuits. Filtered from P3V3_MCU.
VREFH	3.3V	Upper reference voltage for ADC on the MCU. Filtered from VDDA.
VREFL	0V	Lower reference voltage for ADC on the MCU. Filtered from VSSA.
VSSA	0V	VSSA power for MCU and analog circuits. Filtered from GND.
GND	0V	Digital Ground.
VDD_INT	3.3V	MCU Internal supply
VREF_DDR2	0.9V	DDR2 VREF = VDDQ/2 supply for MCU and SDRAM
VTT_DDR2	0.9V	DDR2 VTT= VDDQ/2 termination supply for MCU and SDRAM
VDD_1V8	1.8V	DDR2 VDDQ supply for MCU and SDRAM

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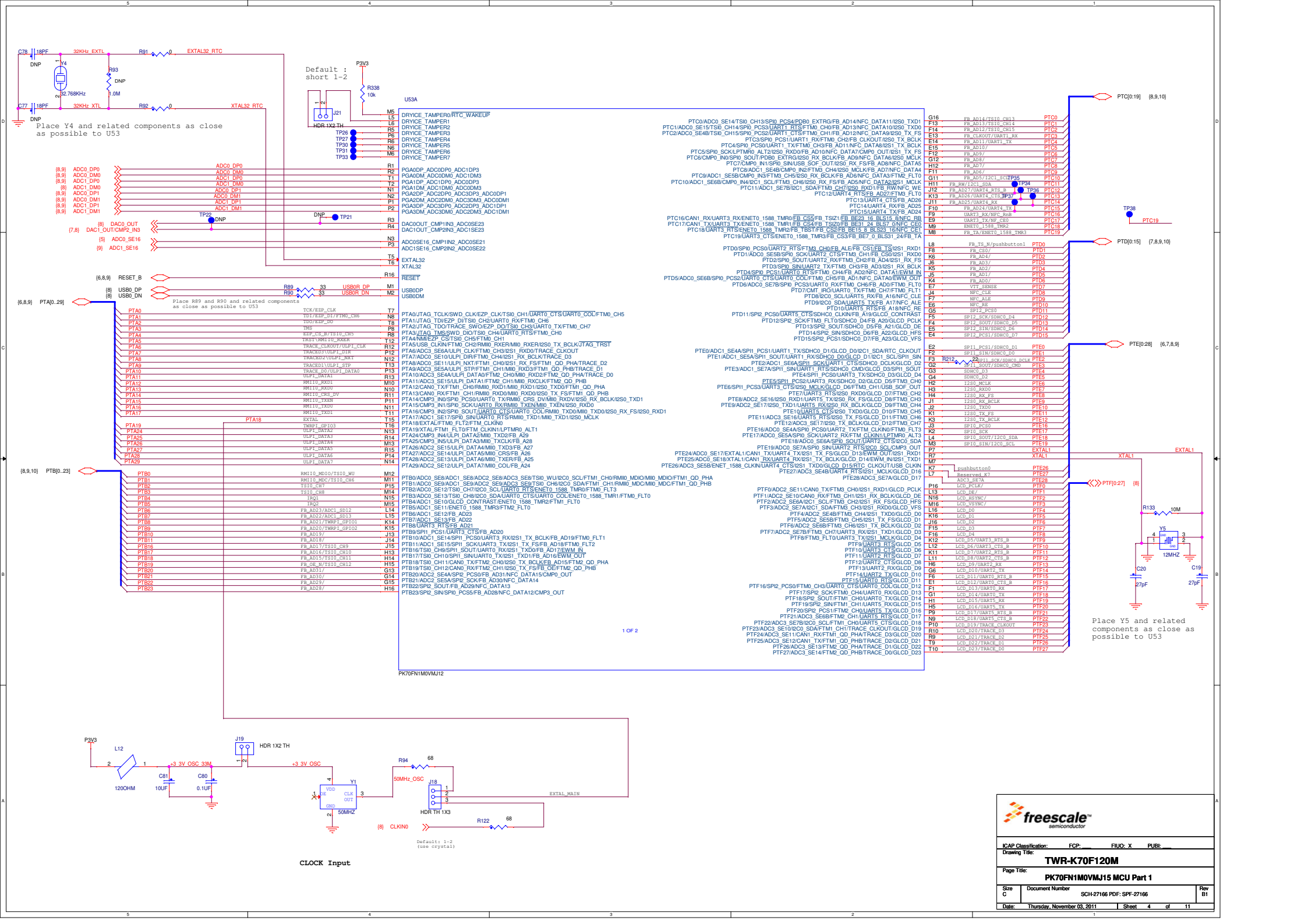
Place Y4 and related components as close as possible to U53
Default : short 1-2
Place R89 and R90 and related components as close as possible to U53
Place Y5 and related components as close as possible to U53
CLOCK Input
U53A
PK70FN1M0VMJ12
1 OF 2
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ICAP Classification: FCP: ___ FIUO: X PUBI: ___
Drawing Title: TWR-K70F120M
Page Title: PK70FN1M0VMJ15 MCU Part 1
Size C
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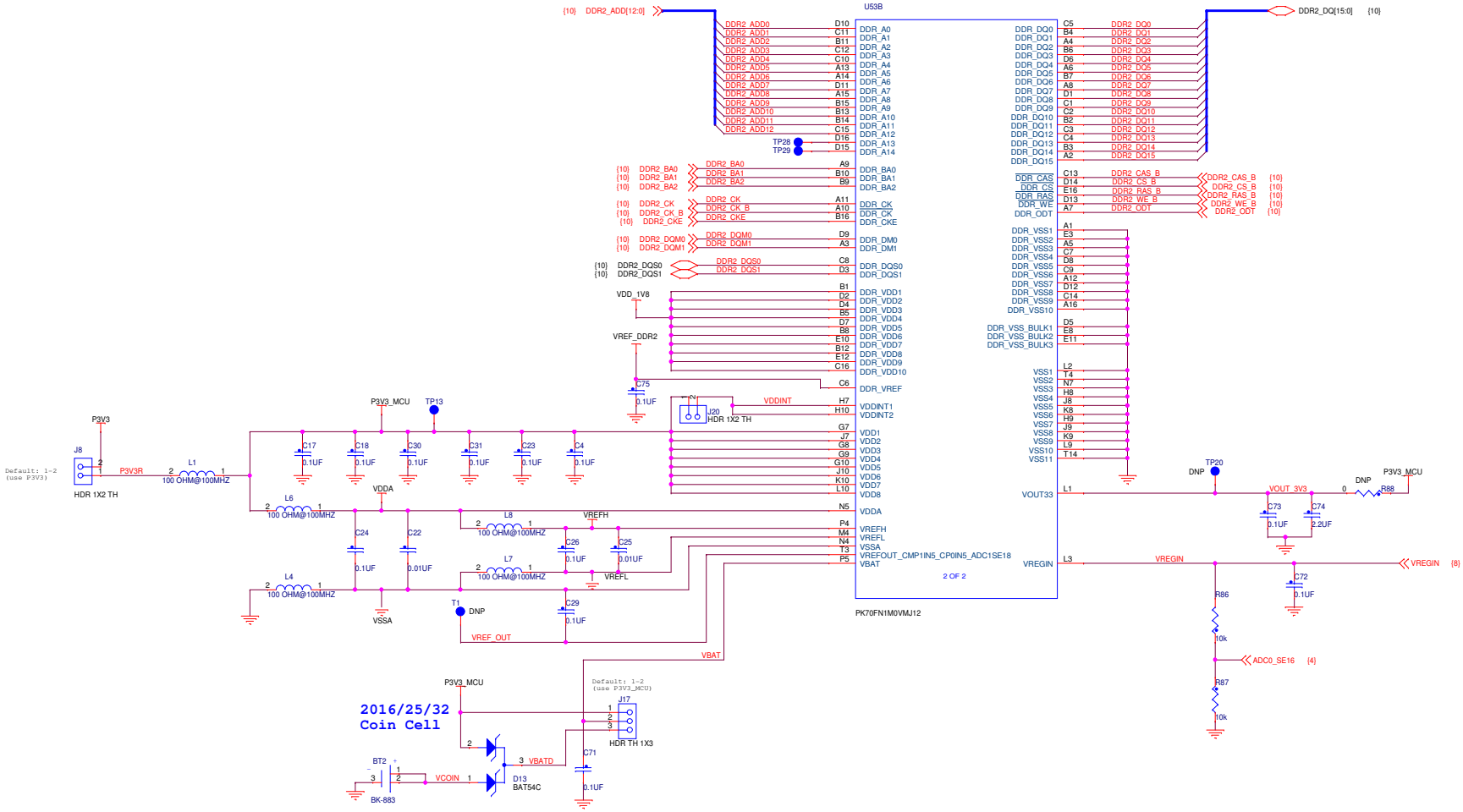

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **TWR-K70F120M**

Page Title: **PK70FN1M0VMJ15 MCU Part 2**

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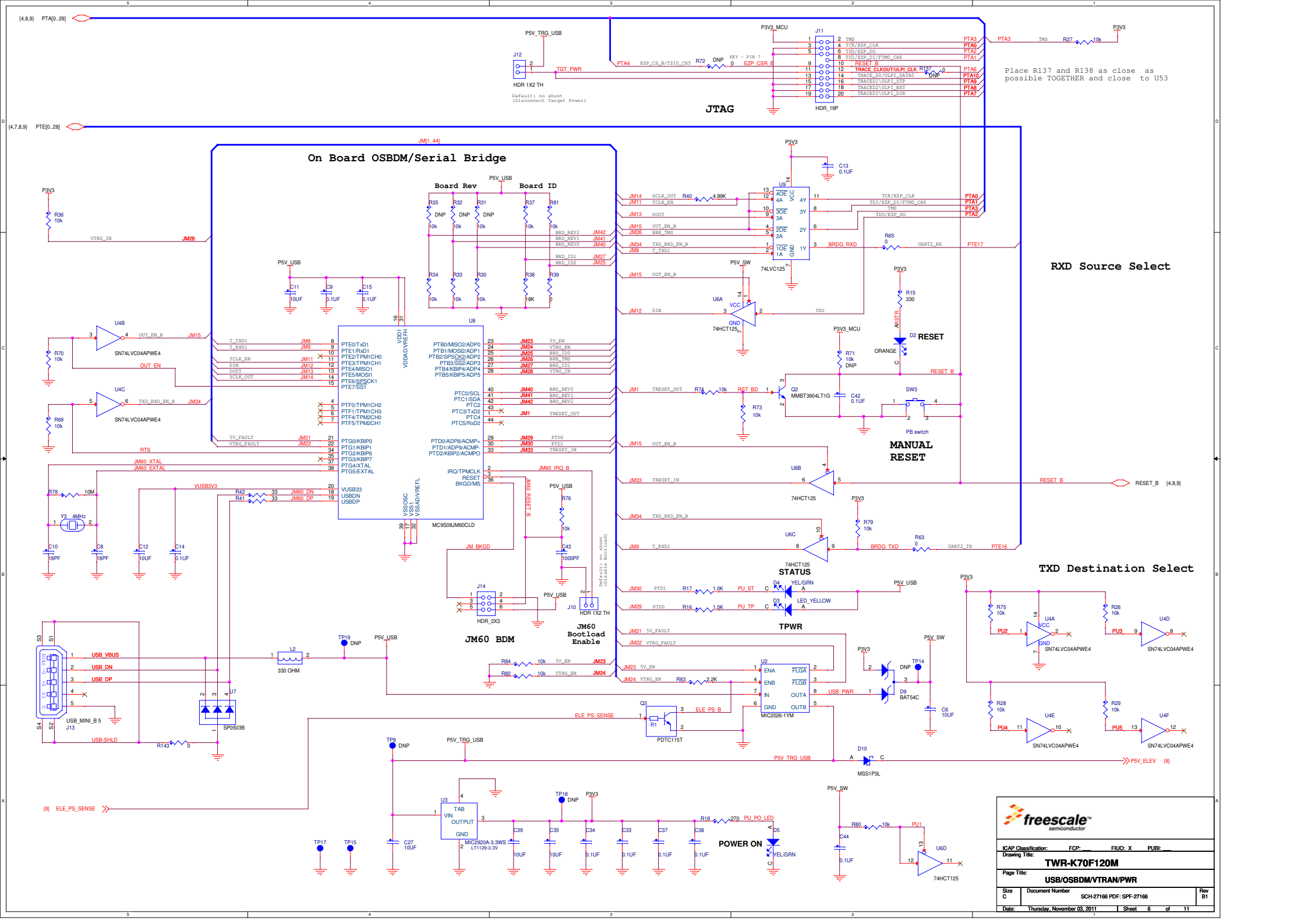
JTAG
On Board OSBDM/Serial Bridge
RXD Source Select
TXD Destination Select
MANUAL RESET
STATUS
TPWR
JM60 BDM
JM60 Bootload Enable
POWER ON
Board Rev
Board ID
Place R137 and R138 as close as possible TOGETHER and close to U53
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TWR-K70F120M
USB/OSBDM/VTRAN/PWR
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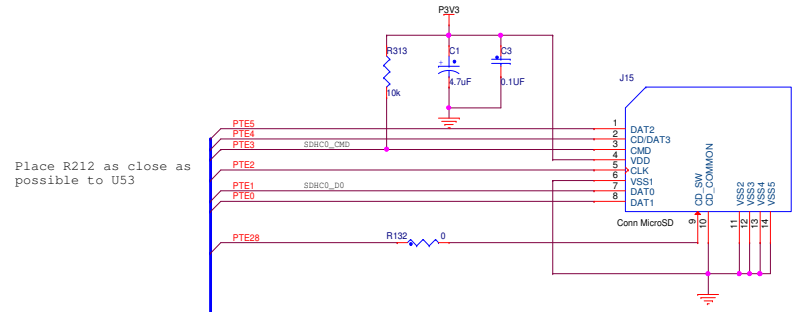
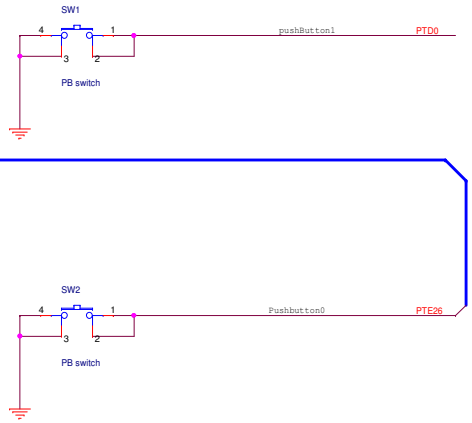
MICRO SD INTERFACE

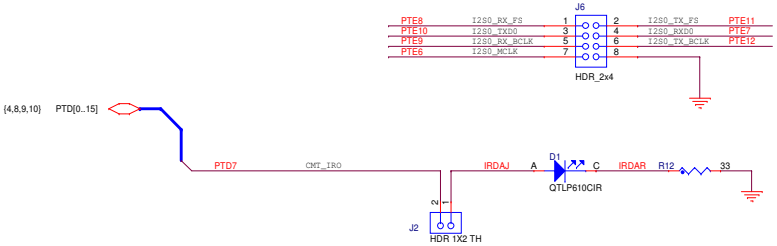


PUSH BUTTON

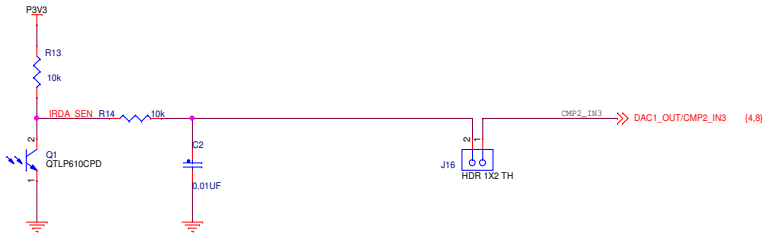


NOTE: Don't pushbutton if Flexbus or I2S1 is used

I2S SAI HEADER



IRDA



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Drawing Title: **TWR-K70F120M**

Page Title: **Peripherals**

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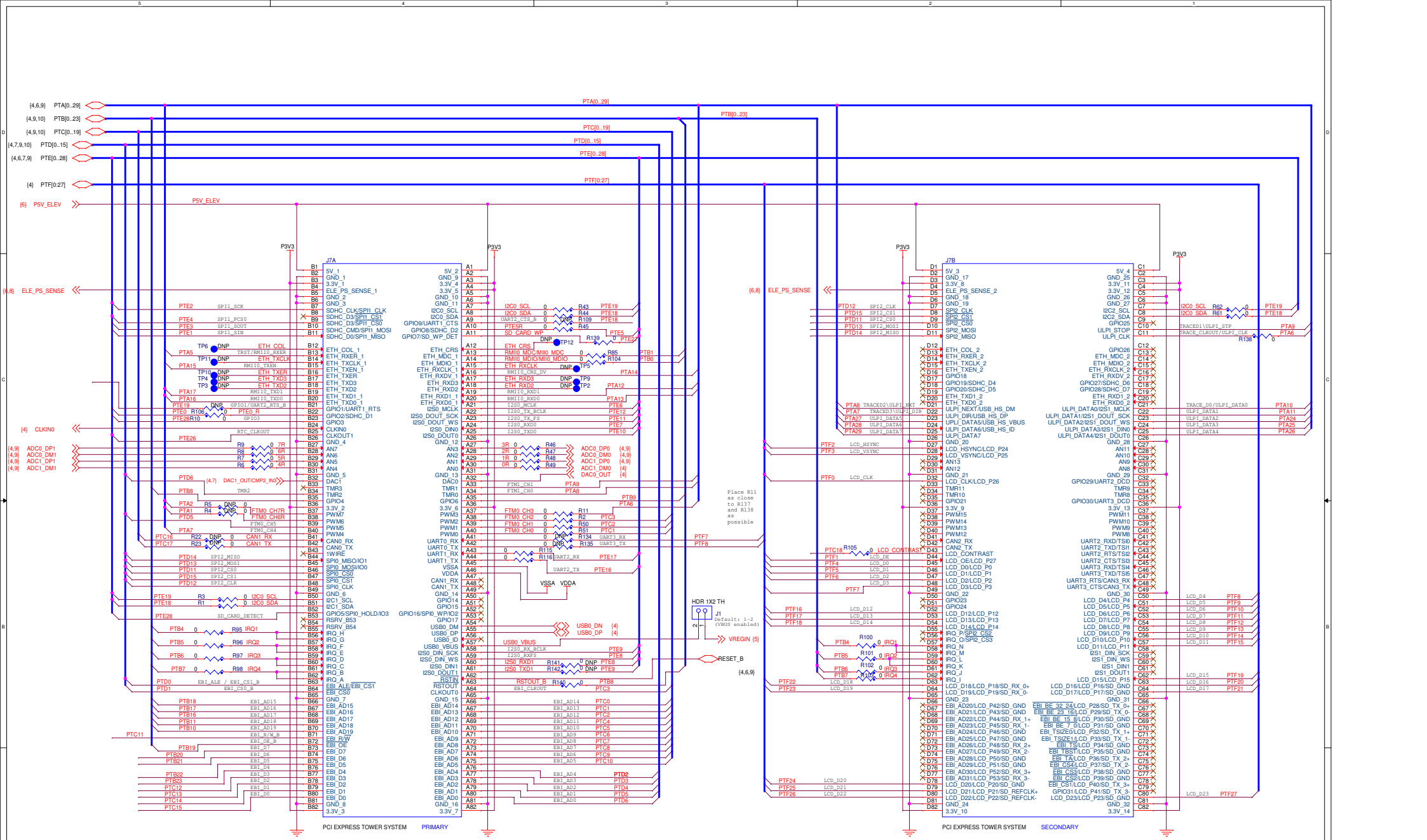

Notes:
Place R107,R108 near to J7B
Place these R, If flow control needs to be tested, and remove R43,R44

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Drawing Title:	TWR-K70F120M		
Page Title:	Elevator Connector		
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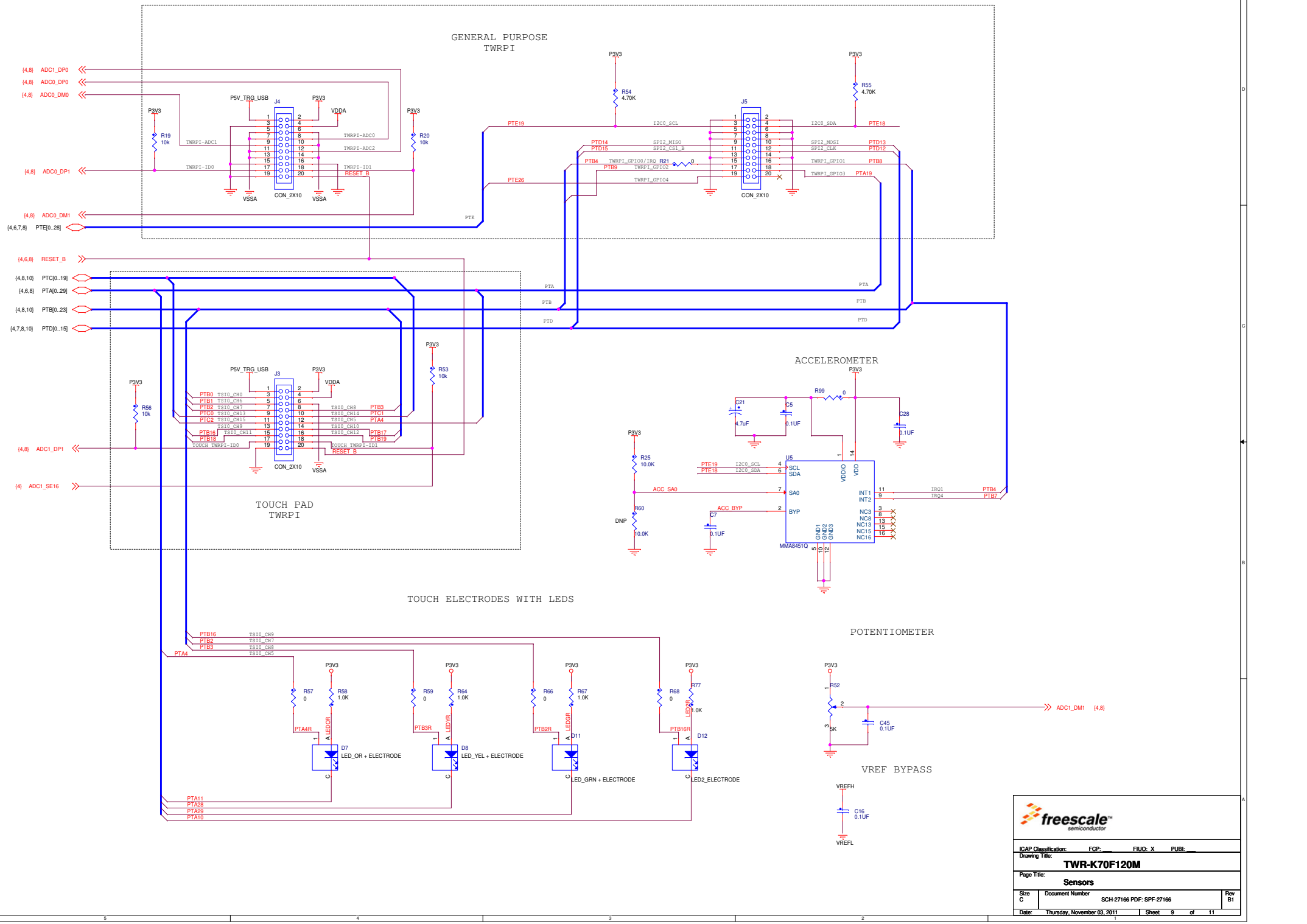

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ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___
Drawing Title:	TWR-K70F120M		
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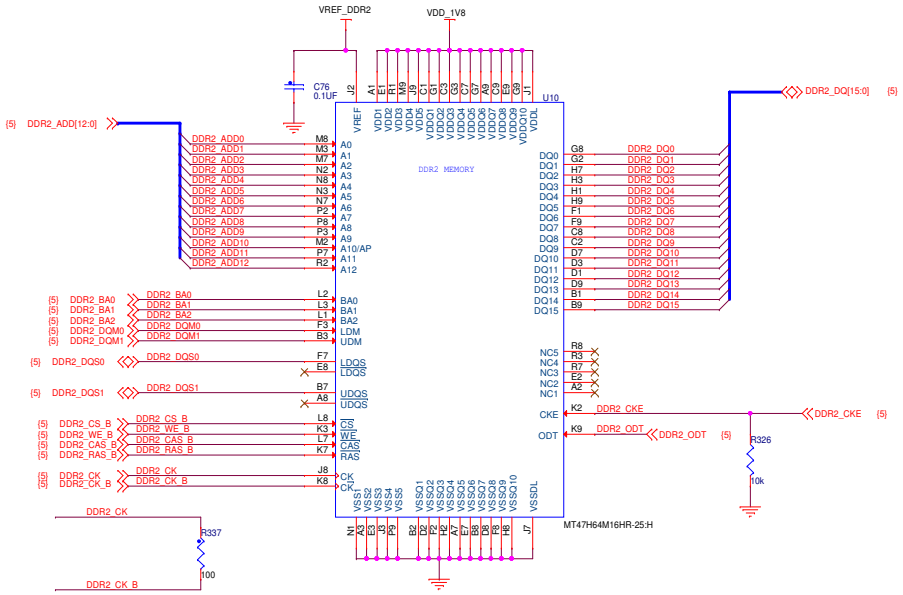
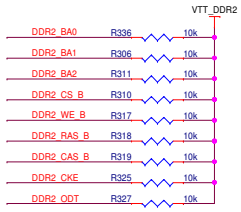
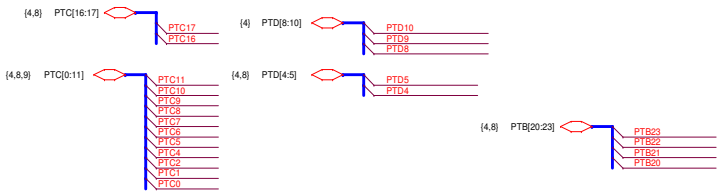
DDR-2 MEMORIES AND TERMINATIONS

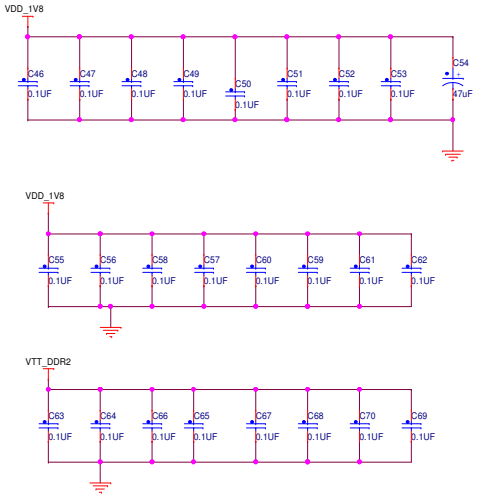




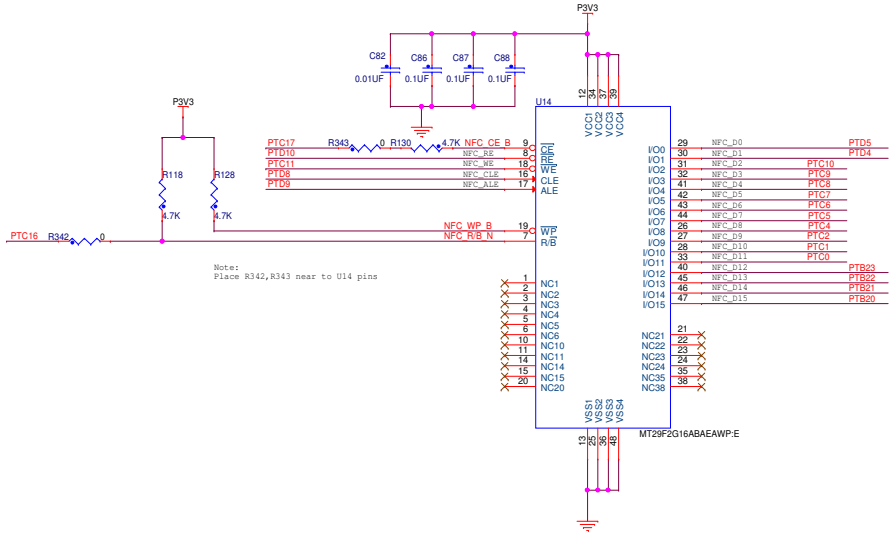


Note:

Place the DDR2 CLK Termination resistor R337 close the Chips



NAND FLASH



ICAP Classification:	FCP: __	FIUO: X	PUBI: __
Drawing Title:	TWR-K70F120M		
Page Title:	DDR2 SDRAM, NAND FLASH		
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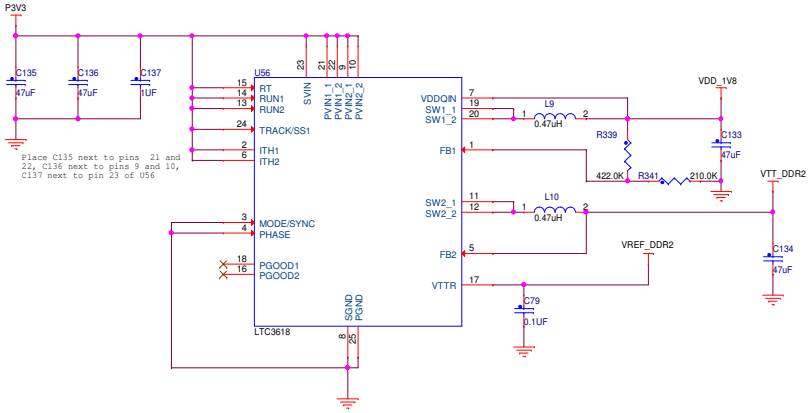
DDR-2 TERMINATION REG (3A)



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