



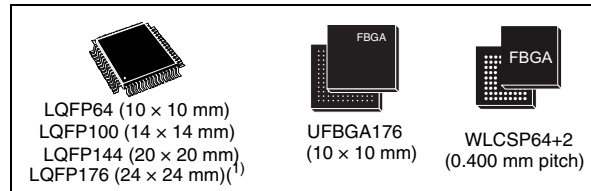
STM32F215xx STM32F217xx

ARM-based 32-bit MCU, 150MIPs, up to 1MB Flash/128+4KB RAM, crypto, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 15 comm. interfaces & camera

Preliminary data

Features

- Core: ARM 32-bit Cortex™-M3 CPU with Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution performance from Flash memory, frequency up to 120 MHz, memory protection unit, 150 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1)
- Memories
 - Up to 1 Mbyte of Flash memory
 - Up to 128 + 4 Kbytes of SRAM
 - Flexible static memory controller that supports Compact Flash, SRAM, PSRAM, NOR and NAND memories
 - LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
 - 1.8 to 3.6 V application supply and I/Os
 - POR, PDR, PVD and BOR
 - 4 to 26 MHz crystal oscillator
 - Internal 16 MHz factory-trimmed RC (1% accuracy)
 - 32 kHz oscillator for RTC with calibration
 - Internal 32 kHz RC with calibration
- Low power
 - Sleep, Stop and Standby modes
 - V_{BAT} supply for RTC, 20 × 32 bit backup registers, and optional 4 KB backup SRAM
- 3 × 12-bit, 0.5 μs A/D converters
 - up to 24 channels
 - up to 6 MSPS in triple interleaved mode
- 2 × 12-bit D/A converters
- General-purpose DMA
 - 16-stream DMA controller with centralized FIFOs and burst support
- Up to 17 timers
 - Up to twelve 16-bit and two 32-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- Debug mode
 - Serial wire debug (SWD) & JTAG interfaces
 - Cortex-M3 Embedded Trace Macrocell™



1. Package not in production (for development only).
- Up to 140 I/O ports with interrupt capability:
 - Up to 136 fast I/Os up to 60 MHz
 - Up to 138 5 V-tolerant I/Os
 - Up to 15 communication interfaces
 - Up to 3 × I²C interfaces (SMBus/PMBus)
 - Up to 4 USARTs and 2 UARTs (7.5 Mbit/s, ISO 7816 interface, LIN, IrDA, modem control)
 - Up to 3 SPIs (30 Mbit/s), 2 with muxed I²S to achieve audio class accuracy via audio PLL or external PLL
 - 2 × CAN interfaces (2.0B Active)
 - SDIO interface
 - Advanced connectivity
 - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
 - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
 - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
 - 8- to 14-bit parallel camera interface: up to 27 Mbyte/s at 27 MHz or 48 Mbyte/s at 48 MHz
 - Cryptographic acceleration
 - Hardware acceleration for AES 128, 192, 256, Triple DES, HASH (MD5, SHA-1)
 - Analog true random number generator
 - CRC calculation unit, 96-bit unique ID
 - Analog true random number generator

Table 1. Device summary

| Reference | Part number |
|-------------|--|
| STM32F215xx | STM32F215RG, STM32F215VG, STM32F215ZG, STM32F215RE, STM32F215VE, STM32F215ZE |
| STM32F217xx | STM32F217VG, STM32F217IG, STM32F217ZG, STM32F217VE, STM32F217IE, STM32F217ZE |

Contents

- 1 Introduction 9**
- 2 Description 10**
 - 2.1 Full compatibility throughout the family 13
 - 2.2 Device overview 15
 - 2.2.1 ARM® Cortex™-M3 core with embedded Flash and SRAM 16
 - 2.2.2 Memory protection unit 16
 - 2.2.3 Adaptive real-time memory accelerator (ART Accelerator™) 16
 - 2.2.4 Embedded Flash memory 16
 - 2.2.5 CRC (cyclic redundancy check) calculation unit 17
 - 2.2.6 True random number generator (RNG) 17
 - 2.2.7 Embedded SRAM 17
 - 2.2.8 Multi-AHB bus matrix 17
 - 2.2.9 DMA 18
 - 2.2.10 FSMC (flexible static memory controller) 18
 - 2.2.11 Nested vectored interrupt controller (NVIC) 19
 - 2.2.12 External interrupt/event controller (EXTI) 19
 - 2.2.13 Clocks and startup 19
 - 2.2.14 Boot modes 20
 - 2.2.15 Power supply schemes 20
 - 2.2.16 Power supply supervisor 20
 - 2.2.17 Voltage regulator 20
 - 2.2.18 Real-time clock (RTC), backup SRAM and backup registers 23
 - 2.2.19 Low-power modes 23
 - 2.2.20 V_{BAT} operation 24
 - 2.2.21 Timers and watchdogs 24
 - 2.2.22 Basic timers TIM6 and TIM7 26
 - 2.2.23 Independent watchdog 26
 - 2.2.24 Window watchdog 26
 - 2.2.25 SysTick timer 27
 - 2.2.26 I²C bus 27
 - 2.2.27 Universal synchronous/asynchronous receiver transmitters (UARTs/USARTs) 27
 - 2.2.28 Serial peripheral interface (SPI) 28

| | | |
|----------|---|-----------|
| 2.2.29 | Inter-integrated sound (I ² S) | 28 |
| 2.2.30 | SDIO | 28 |
| 2.2.31 | Ethernet MAC interface with dedicated DMA and IEEE 1588 support | 29 |
| 2.2.32 | Controller area network (CAN) | 29 |
| 2.2.33 | Universal serial bus on-the-go full-speed (OTG_FS) | 29 |
| 2.2.34 | Universal serial bus on-the-go high-speed (OTG_HS) | 30 |
| 2.2.35 | Audio PLL (PLLI2S) | 30 |
| 2.2.36 | Digital camera interface (DCMI) | 31 |
| 2.2.37 | Cryptographic acceleration | 31 |
| 2.2.38 | GPIOs (general-purpose inputs/outputs) | 31 |
| 2.2.39 | ADCs (analog-to-digital converters) | 32 |
| 2.2.40 | DAC (digital-to-analog converter) | 32 |
| 2.2.41 | Temperature sensor | 32 |
| 2.2.42 | Serial wire JTAG debug port (SWJ-DP) | 33 |
| 2.2.43 | Embedded Trace Macrocell™ | 33 |
| 3 | Pinouts and pin description | 34 |
| 4 | Memory mapping | 54 |
| 5 | Electrical characteristics | 55 |
| 5.1 | Parameter conditions | 55 |
| 5.1.1 | Minimum and maximum values | 55 |
| 5.1.2 | Typical values | 55 |
| 5.1.3 | Typical curves | 55 |
| 5.1.4 | Loading capacitor | 55 |
| 5.1.5 | Pin input voltage | 55 |
| 5.1.6 | Power supply scheme | 56 |
| 5.1.7 | Current consumption measurement | 56 |
| 5.2 | Absolute maximum ratings | 57 |
| 5.3 | Operating conditions | 58 |
| 5.3.1 | General operating conditions | 58 |
| 5.3.2 | Operating conditions at power-up / power-down (regulator not bypassed) | 60 |
| 5.3.3 | Operating conditions at power-up / power-down in regulator bypass mode | 61 |
| 5.3.4 | Embedded reset and power control block characteristics | 61 |
| 5.3.5 | Supply current characteristics | 62 |

| | | |
|-------------------|---|------------|
| 5.3.6 | External clock source characteristics | 69 |
| 5.3.7 | Internal clock source characteristics | 73 |
| 5.3.8 | Wakeup time from low-power mode | 73 |
| 5.3.9 | PLL characteristics | 74 |
| 5.3.10 | PLL spread spectrum clock generation (SSCG) characteristics | 75 |
| 5.3.11 | Memory characteristics | 77 |
| 5.3.12 | EMC characteristics | 78 |
| 5.3.13 | Absolute maximum ratings (electrical sensitivity) | 79 |
| 5.3.14 | I/O port characteristics | 80 |
| 5.3.15 | NRST pin characteristics | 84 |
| 5.3.16 | TIM timer characteristics | 85 |
| 5.3.17 | Communications interfaces | 87 |
| 5.3.18 | 12-bit ADC characteristics | 100 |
| 5.3.19 | DAC electrical specifications | 104 |
| 5.3.20 | Temperature sensor characteristics | 106 |
| 5.3.21 | V _{BAT} monitoring characteristics | 106 |
| 5.3.22 | Embedded reference voltage | 106 |
| 5.3.23 | FSMC characteristics | 107 |
| 5.3.24 | Camera interface (DCMI) timing specifications | 125 |
| 5.3.25 | SD/SDIO MMC card host interface (SDIO) characteristics | 126 |
| 5.3.26 | RTC characteristics | 127 |
| 6 | Package characteristics | 128 |
| 6.1 | Package mechanical data | 128 |
| 6.2 | Thermal characteristics | 135 |
| 7 | Part numbering | 136 |
| Appendix A | Application block diagrams | 137 |
| A.1 | Main applications versus package | 137 |
| A.2 | Application example with regulator off. | 138 |
| A.3 | USB OTG full speed (FS) interface solutions | 139 |
| A.4 | USB OTG high speed (HS) interface solutions | 140 |
| A.5 | Complete audio player solutions | 142 |
| | Revision history | 145 |

List of tables

| | | |
|-----------|--|----|
| Table 1. | Device summary | 1 |
| Table 2. | STM32F215xx and STM32F217xx: features and peripheral counts. | 11 |
| Table 3. | Timer feature comparison. | 24 |
| Table 4. | USART feature comparison | 27 |
| Table 5. | STM32F21x pin and ball definitions | 39 |
| Table 6. | Alternate function mapping | 49 |
| Table 7. | Voltage characteristics | 57 |
| Table 8. | Current characteristics | 57 |
| Table 9. | Thermal characteristics. | 58 |
| Table 10. | General operating conditions | 58 |
| Table 11. | Limitations depending on the operating power supply range | 59 |
| Table 12. | Operating conditions at power-up / power-down (regulator not bypassed) | 60 |
| Table 13. | Operating conditions at power-up / power-down in regulator bypass mode | 61 |
| Table 14. | Embedded reset and power control block characteristics. | 61 |
| Table 15. | Typical and maximum current consumption in Run mode, code with data processing running from Flash | 63 |
| Table 16. | Typical and maximum current consumption in Run mode, code with data processing running from RAM | 64 |
| Table 17. | Typical and maximum current consumption in Sleep mode | 64 |
| Table 18. | Typical and maximum current consumptions in Stop mode | 65 |
| Table 19. | Typical and maximum current consumptions in Standby mode | 65 |
| Table 20. | Typical and maximum current consumptions in VBAT mode | 66 |
| Table 21. | Peripheral current consumption | 67 |
| Table 22. | High-speed external user clock characteristics. | 69 |
| Table 23. | Low-speed external user clock characteristics | 69 |
| Table 24. | HSE 4-26 MHz oscillator characteristics | 71 |
| Table 25. | LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz) | 72 |
| Table 26. | HSI oscillator characteristics | 73 |
| Table 27. | LSI oscillator characteristics | 73 |
| Table 28. | Low-power mode wakeup timings | 74 |
| Table 29. | Main PLL characteristics. | 74 |
| Table 30. | PLLI2S (audio PLL) characteristics | 74 |
| Table 31. | SSCG parameters constraint | 75 |
| Table 32. | Flash memory characteristics | 77 |
| Table 33. | Flash memory programming. | 77 |
| Table 34. | Flash memory programming with V_{PP} | 77 |
| Table 35. | Flash memory endurance and data retention. | 78 |
| Table 36. | EMS characteristics | 78 |
| Table 37. | EMI characteristics | 79 |
| Table 38. | ESD absolute maximum ratings | 80 |
| Table 39. | Electrical sensitivities | 80 |
| Table 40. | I/O static characteristics | 80 |
| Table 41. | Output voltage characteristics | 82 |
| Table 42. | I/O AC characteristics | 82 |
| Table 43. | NRST pin characteristics | 84 |
| Table 44. | Characteristics of TIMx connected to the APB1 domain | 85 |
| Table 45. | Characteristics of TIMx connected to the APB2 domain | 86 |

| | | |
|-----------|--|-----|
| Table 46. | I ² C characteristics | 87 |
| Table 47. | SCL frequency (f _{PCLK1} = 30 MHz, V _{DD} = 3.3 V) | 88 |
| Table 48. | SPI characteristics | 89 |
| Table 49. | I ² S characteristics | 92 |
| Table 50. | USB OTG FS startup time | 94 |
| Table 51. | USB OTG FS DC electrical characteristics | 94 |
| Table 52. | USB OTG FS electrical characteristics | 96 |
| Table 53. | Clock timing parameters | 96 |
| Table 54. | ULPI timing | 97 |
| Table 55. | Ethernet DC electrical characteristics | 97 |
| Table 56. | Dynamics characteristics: Ethernet MAC signals for SMI | 98 |
| Table 57. | Dynamics characteristics: Ethernet MAC signals for RMII | 98 |
| Table 58. | Dynamics characteristics: Ethernet MAC signals for MII | 99 |
| Table 59. | ADC characteristics | 100 |
| Table 60. | ADC accuracy | 101 |
| Table 61. | DAC characteristics | 104 |
| Table 62. | TS characteristics | 106 |
| Table 63. | V _{BAT} monitoring characteristics | 106 |
| Table 64. | Embedded internal reference voltage | 106 |
| Table 65. | Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings | 108 |
| Table 66. | Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings | 109 |
| Table 67. | Asynchronous multiplexed PSRAM/NOR read timings | 110 |
| Table 68. | Asynchronous multiplexed PSRAM/NOR write timings | 111 |
| Table 69. | Synchronous multiplexed NOR/PSRAM read timings | 113 |
| Table 70. | Synchronous multiplexed PSRAM write timings | 115 |
| Table 71. | Synchronous non-multiplexed NOR/PSRAM read timings | 116 |
| Table 72. | Synchronous non-multiplexed PSRAM write timings | 117 |
| Table 73. | Switching characteristics for PC Card/CF read and write cycles | 122 |
| Table 74. | Switching characteristics for NAND Flash read and write cycles | 125 |
| Table 75. | DCMI characteristics | 125 |
| Table 76. | SD / MMC characteristics | 126 |
| Table 77. | RTC characteristics | 127 |
| Table 78. | LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data | 129 |
| Table 79. | WLCSP64+2 - 0.400 mm pitch wafer level chip size package mechanical data | 130 |
| Table 80. | LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data | 131 |
| Table 81. | LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data | 132 |
| Table 82. | LQFP176 - Low profile quad flat package 24 x 24 x 1.4 mm package mechanical data | 133 |
| Table 83. | UFPGA176+25 - ultra thin fine pitch ball grid array 10 x 10 x 0.6 mm mechanical data | 134 |
| Table 84. | Package thermal characteristics | 135 |
| Table 85. | Ordering information scheme | 136 |
| Table 86. | Main applications versus package for STM32F217xx microcontrollers | 137 |
| Table 87. | Document revision history | 145 |

List of figures

| | | |
|------------|--|-----|
| Figure 1. | Compatible board design: LQFP144 | 13 |
| Figure 2. | Compatible board design: LQFP100 | 14 |
| Figure 3. | Compatible board design: LQFP64 | 14 |
| Figure 4. | STM32F21x block diagram | 15 |
| Figure 5. | Multi-AHB matrix | 17 |
| Figure 6. | Startup in regulator bypass/regulator off mode: slow V_{DD} slope - power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization | 22 |
| Figure 7. | Startup in regulator bypass/regulator off mode: slow V_{DD} slope - power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization | 22 |
| Figure 8. | Startup in regulator bypass/regulator off and internal reset off | 22 |
| Figure 9. | STM32F21x LQFP64 pinout | 34 |
| Figure 10. | STM32F21x WLCSP64+2 ballout | 34 |
| Figure 11. | STM32F21x LQFP100 pinout | 35 |
| Figure 12. | STM32F21x LQFP144 pinout | 36 |
| Figure 13. | STM32F21x LQFP176 pinout | 37 |
| Figure 14. | STM32F21xxx UFBGA176 ballout | 38 |
| Figure 15. | Memory map | 54 |
| Figure 16. | Pin loading conditions | 55 |
| Figure 17. | Pin input voltage | 55 |
| Figure 18. | Power supply scheme | 56 |
| Figure 19. | Current consumption measurement scheme | 56 |
| Figure 20. | Number of wait states versus f_{CPU} and V_{DD} range | 60 |
| Figure 21. | High-speed external clock source AC timing diagram | 70 |
| Figure 22. | Low-speed external clock source AC timing diagram | 70 |
| Figure 23. | Typical application with an 8 MHz crystal | 71 |
| Figure 24. | Typical application with a 32.768 kHz crystal | 72 |
| Figure 25. | PLL output clock waveforms in center spread mode | 76 |
| Figure 26. | PLL output clock waveforms in down spread mode | 76 |
| Figure 27. | I/O AC characteristics definition | 84 |
| Figure 28. | Recommended NRST pin protection | 85 |
| Figure 29. | I ² C bus AC waveforms and measurement circuit | 88 |
| Figure 30. | SPI timing diagram - slave mode and CPHA = 0 | 90 |
| Figure 31. | SPI timing diagram - slave mode and CPHA = 1 ⁽¹⁾ | 90 |
| Figure 32. | SPI timing diagram - master mode ⁽¹⁾ | 91 |
| Figure 33. | I ² S slave timing diagram (Philips protocol) ⁽¹⁾ | 93 |
| Figure 34. | I ² S master timing diagram (Philips protocol) ⁽¹⁾ | 93 |
| Figure 35. | USB OTG FS timings: definition of data signal rise and fall time | 95 |
| Figure 36. | ULPI timing diagram | 97 |
| Figure 37. | Ethernet SMI timing diagram | 98 |
| Figure 38. | Ethernet RMII timing diagram | 98 |
| Figure 39. | Ethernet MII timing diagram | 99 |
| Figure 40. | ADC accuracy characteristics | 102 |
| Figure 41. | Typical connection diagram using the ADC | 102 |
| Figure 42. | Power supply and reference decoupling (V_{REF+} not connected to V_{DDA}) | 103 |
| Figure 43. | Power supply and reference decoupling (V_{REF+} connected to V_{DDA}) | 103 |
| Figure 44. | 12-bit buffered /non-buffered DAC | 105 |
| Figure 45. | Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms | 107 |
| Figure 46. | Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms | 108 |

| | | |
|------------|---|-----|
| Figure 47. | Asynchronous multiplexed PSRAM/NOR read waveforms | 109 |
| Figure 48. | Asynchronous multiplexed PSRAM/NOR write waveforms | 111 |
| Figure 49. | Synchronous multiplexed NOR/PSRAM read timings | 112 |
| Figure 50. | Synchronous multiplexed PSRAM write timings | 114 |
| Figure 51. | Synchronous non-multiplexed NOR/PSRAM read timings | 116 |
| Figure 52. | Synchronous non-multiplexed PSRAM write timings | 117 |
| Figure 53. | PC Card/CompactFlash controller waveforms for common memory read access | 118 |
| Figure 54. | PC Card/CompactFlash controller waveforms for common memory write access | 119 |
| Figure 55. | PC Card/CompactFlash controller waveforms for attribute memory read access | 120 |
| Figure 56. | PC Card/CompactFlash controller waveforms for attribute memory write access | 121 |
| Figure 57. | PC Card/CompactFlash controller waveforms for I/O space read access | 121 |
| Figure 58. | PC Card/CompactFlash controller waveforms for I/O space write access | 122 |
| Figure 59. | NAND controller waveforms for read access | 124 |
| Figure 60. | NAND controller waveforms for write access | 124 |
| Figure 61. | NAND controller waveforms for common memory read access | 124 |
| Figure 62. | NAND controller waveforms for common memory write access | 125 |
| Figure 63. | SDIO high-speed mode | 126 |
| Figure 64. | SD default mode | 126 |
| Figure 65. | LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline | 129 |
| Figure 66. | Recommended footprint ⁽¹⁾ | 129 |
| Figure 67. | WLCSP64+2 - 0.400 mm pitch wafer level chip size package outline | 130 |
| Figure 68. | LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline | 131 |
| Figure 69. | Recommended footprint ⁽¹⁾ | 131 |
| Figure 70. | LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline | 132 |
| Figure 71. | Recommended footprint ⁽¹⁾ | 132 |
| Figure 72. | LQFP176 - Low profile quad flat package 24 x 24 x 1.4 mm, package outline | 133 |
| Figure 73. | UFBGA176+25 - ultra thin fine pitch ball grid array 10 x 10 x 0.6 mm, package outline | 134 |
| Figure 74. | Regulator bypass/regulator off | 138 |
| Figure 75. | Regulator bypass/regulator off and internal reset off | 138 |
| Figure 76. | USB OTG FS peripheral-only connection | 139 |
| Figure 77. | USB OTG FS host-only connection | 139 |
| Figure 78. | OTG FS connection dual-role with internal PHY | 140 |
| Figure 79. | USB OTG HS peripheral-only connection | 140 |
| Figure 80. | USB OTG HS host-only connection | 141 |
| Figure 81. | OTG HS connection dual-role with external PHY | 141 |
| Figure 82. | Complete audio player solution 1 | 142 |
| Figure 83. | Complete audio player solution 2 | 142 |
| Figure 84. | Audio player solution using PLL, PLLI2S, USB and 1 crystal | 143 |
| Figure 85. | Audio PLL (PLLI2S) providing accurate I2S clock | 143 |
| Figure 86. | Master clock (MCK) used to drive the external audio DAC | 144 |
| Figure 87. | Master clock (MCK) not used to drive the external audio DAC | 144 |

1 Introduction

This datasheet provides the description of the STM32F215xx and STM32F217xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32™ family, please refer to [Section 2.1: Full compatibility throughout the family](#).

The STM32F215xx and STM32F217xx datasheet should be read in conjunction with the STM32F20x/STM32F21x reference manual.

For information on programming, erasing and protection of the internal Flash memory, please refer to the STM32F20x/STM32F21x Flash programming manual.

The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: <http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/>.

2 Description

The STM32F215xx and STM32F217xx family is based on the high-performance ARM® Cortex™-M3 32-bit RISC core operating at a frequency of up to 120 MHz. The family incorporates high-speed embedded memories (Flash memory up to 1 Mbyte, up to 128 Kbytes of system SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The devices also feature an adaptive real-time memory accelerator (ART Accelerator™) which allows to achieve a performance equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 120 MHz. This performance has been validated using the CoreMark benchmark.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true number random generator (RNG). They also feature standard and advanced communication interfaces. New advanced peripherals include an SDIO, an enhanced flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more), a cryptographic acceleration cell, and a camera interface for CMOS sensors.

- Up to three I²Cs
- Three SPIs, two I²Ss. To achieve audio class accuracy, the I²S peripherals can be clocked via a dedicated internal audio PLL or via an external PLL to allow synchronization.
- 4 USARTs and 2 UARTs
- An USB OTG full-speed and a USB OTG full-speed with high-speed capability (with the ULPI),
- Two CANs
- An SDIO interface
- Ethernet and the camera interface available on STM32F217xx devices only.

The STM32F215xx and STM32F217xx family operates in the –40 to +105 °C temperature range from a 1.8 V to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F215xx and STM32F217xx family offers devices in four packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F215xx and STM32F217xx microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Figure 4 shows the general block diagram of the device family.



Table 2. STM32F215xx and STM32F217xx: features and peripheral counts

| Peripherals | | STM32F215Rx | | STM32F215Vx | | STM32F215Zx | | STM32F217Vx | | STM32F217Zx | | STM32F217Ix | |
|--------------------------|--------------------------|----------------|------|-------------|------|-------------|------|-------------|------|-------------|------|-------------|------|
| | | 512 | 1024 | 512 | 1024 | 512 | 1024 | 512 | 1024 | 512 | 1024 | 512 | 1024 |
| Flash memory in Kbytes | | 512 | 1024 | 512 | 1024 | 512 | 1024 | 512 | 1024 | 512 | 1024 | 512 | 1024 |
| SRAM in Kbytes | System | 128(112+16) | | | | | | | | | | | |
| | Backup | 4 | | 4 | | 4 | | 4 | | 4 | | 4 | |
| FSMC memory controller | | No | | Yes | | | | | | | | | |
| Ethernet | | No | | | | | | Yes | | | | | |
| Timers | General-purpose | 10 | | | | | | | | | | | |
| | Advanced-control | 2 | | | | | | | | | | | |
| | Basic | 2 | | | | | | | | | | | |
| Random number generator | | Yes | | | | | | | | | | | |
| Communication interfaces | SPI / (I ² S) | 3 (2) | | | | | | | | | | | |
| | I ² C | 3 | | | | | | | | | | | |
| | USART | 4 | | | | | | | | | | | |
| | UART | 2 | | | | | | | | | | | |
| | USB OTG FS | Yes | | | | | | | | | | | |
| | USB OTG HS | Yes | | | | | | | | | | | |
| | CAN | 2 | | | | | | | | | | | |
| Camera interface | | No | | | | | | Yes | | | | | |
| Encryption | | Yes | | | | | | | | | | | |
| GPIOs | | 51 | | 82 | | 114 | | 82 | | 114 | | 140 | |
| 12-bit ADC | | 3 | | | | | | | | | | | |
| Number of channels | | 16 | | 16 | | 24 | | 16 | | 24 | | 24 | |
| 12-bit DAC | | Yes | | | | | | | | | | | |
| Number of channels | | 2 | | | | | | | | | | | |
| Maximum CPU frequency | | 120 MHz | | | | | | | | | | | |
| Operating voltage | | 1.8 V to 3.6 V | | | | | | | | | | | |

Table 2. STM32F215xx and STM32F217xx: features and peripheral counts (continued)

| Peripherals | STM32F215Rx | STM32F215Vx | STM32F215Zx | STM32F217Vx | STM32F217Zx | STM32F217Ix |
|------------------------|--|-------------|-------------|-------------|-------------|-----------------------------------|
| Operating temperatures | Ambient temperatures: -40 to +85 °C / -40 to +105 °C | | | | | |
| | Junction temperature: -40 to + 125 °C | | | | | |
| Package | LQFP64 WLCSP64+2 | LQFP100 | LQFP144 | LQFP100 | LQFP144 | LQFP176 ⁽¹⁾ , UFBGA176 |

1. Package not in production and available for development only.

2.1 Full compatibility throughout the family

The STM32F215xx and STM32F217xx constitute the STM32F21x family whose members are fully pin-to-pin, software and feature compatible, allowing the user to try different memory densities and peripherals for a greater degree of freedom during the development cycle.

The STM32F215xx and STM32F217xx devices maintain a close compatibility with the whole STM32F10xxx family. All functional pins are pin-to-pin compatible. The STM32F215xx and STM32F217xx, however, are not drop-in replacements for the STM32F10xxx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xxx to the STM32F21x family remains simple as only a few pins are impacted.

Figure 1 compatible board design between the STM32F21x and the STM32F10xxx family.

Figure 1. Compatible board design: LQFP144

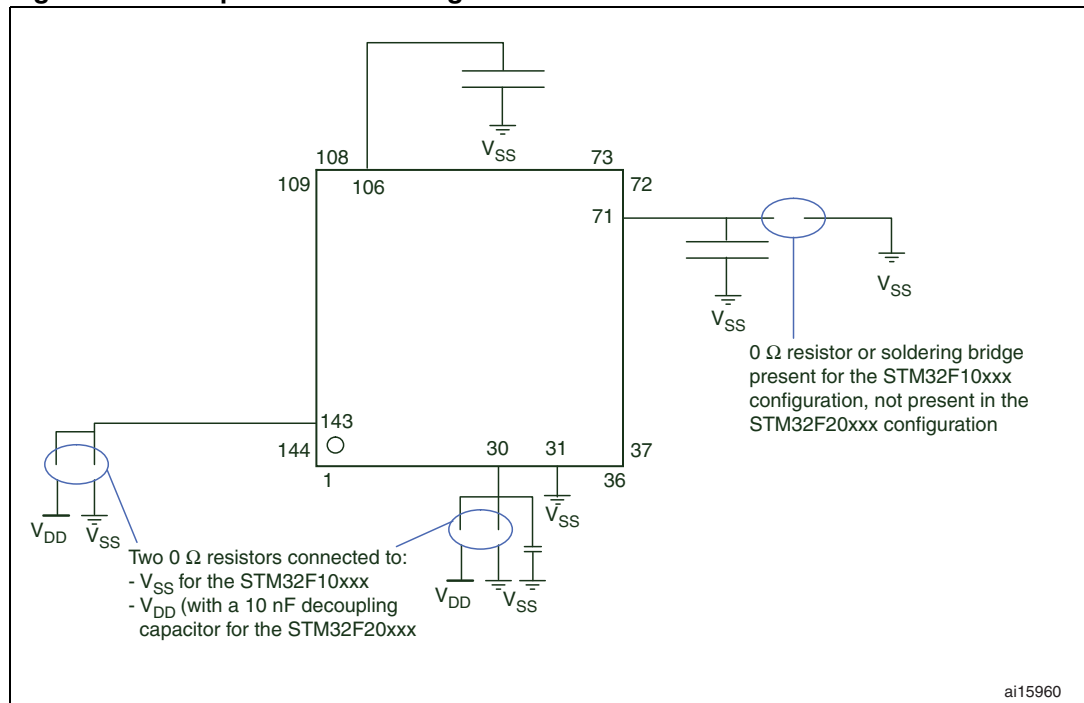


Figure 2. Compatible board design: LQFP100

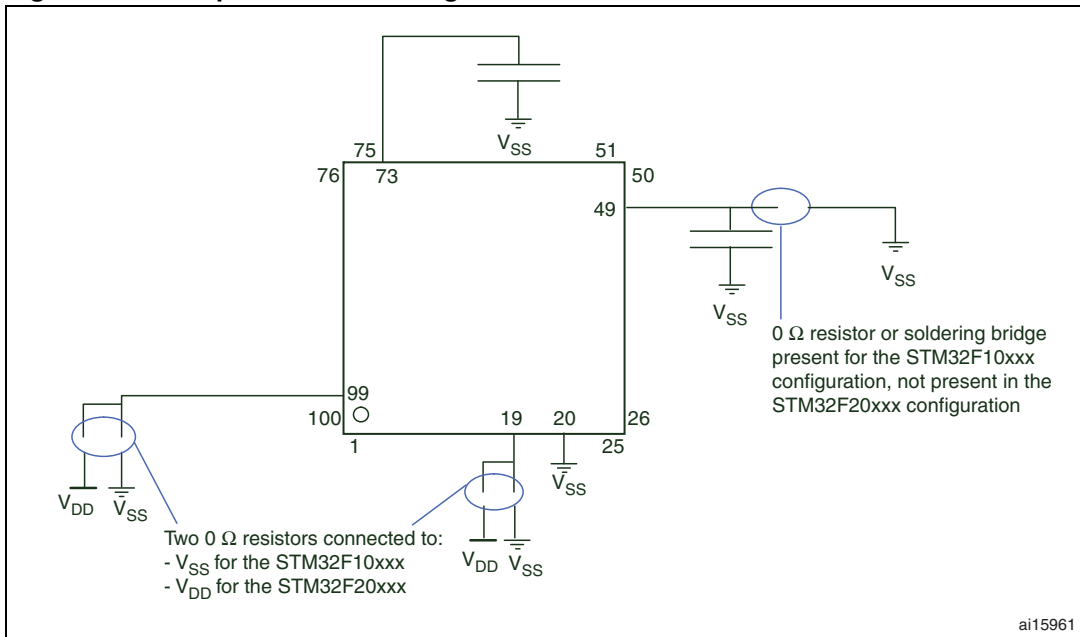
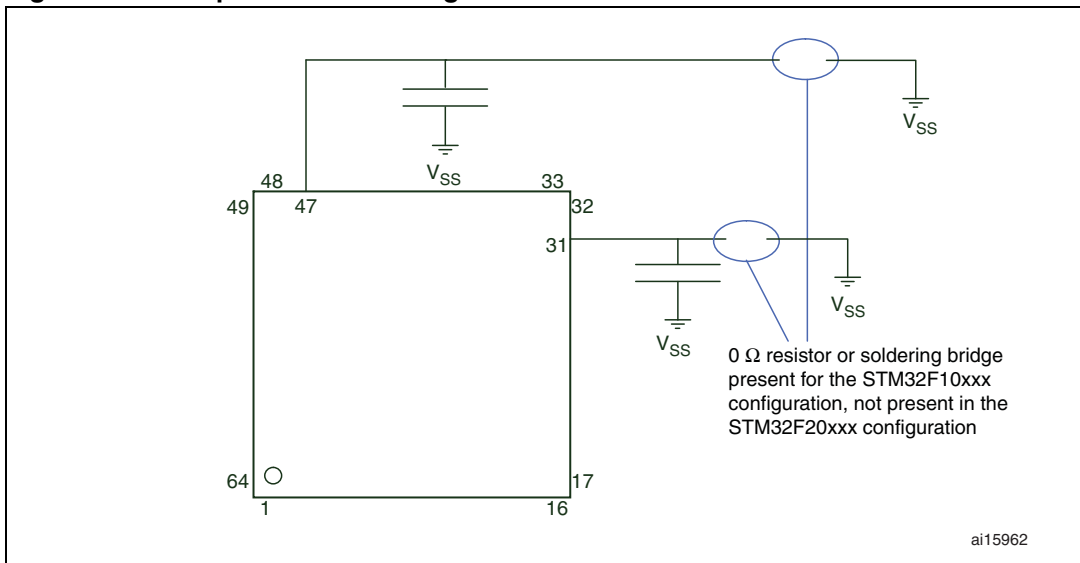
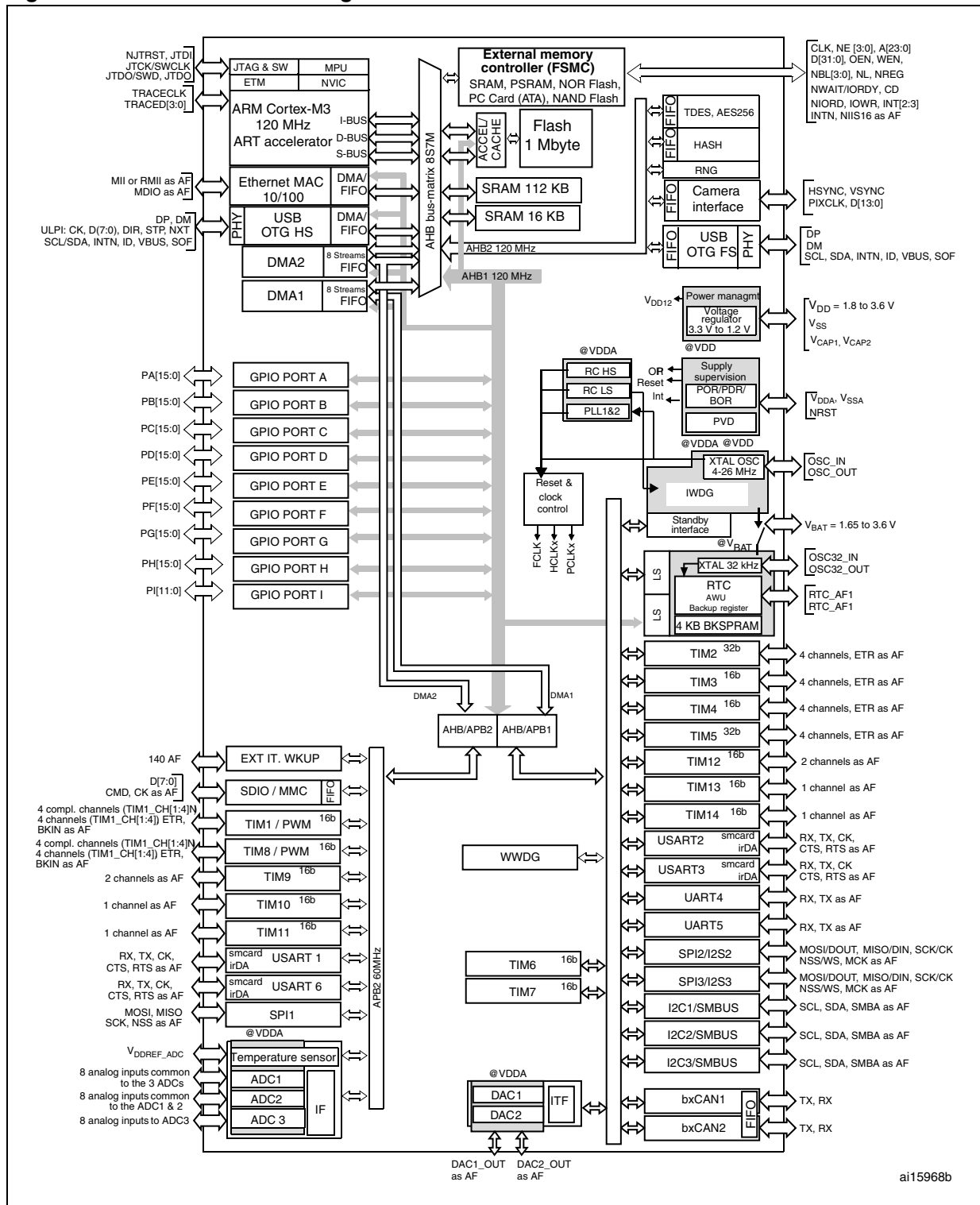


Figure 3. Compatible board design: LQFP64



2.2 Device overview

Figure 4. STM32F21x block diagram



2.2.1 **ARM® Cortex™-M3 core with embedded Flash and SRAM**

The ARM Cortex-M3 processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM core, the STM32F215xx and STM32F217xx family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F21x family.

2.2.2 **Memory protection unit**

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.2.3 **Adaptive real-time memory accelerator (ART Accelerator™)**

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex™-M3 processors. It balances the inherent performance advantage of the ARM Cortex-M3 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher operating frequencies.

To release the processor full 150 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 120 MHz.

2.2.4 **Embedded Flash memory**

The STM32F21x devices embed a 128-bit wide Flash memory of 128 Kbytes, 256 Kbytes, 512 Kbytes, 768 Kbytes or 1 Mbytes available for storing programs and data.

2.2.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.2.6 True random number generator (RNG)

All STM32F2xxx products embed a true RNG that delivers 32-bit random numbers produced by an integrated analog circuit.

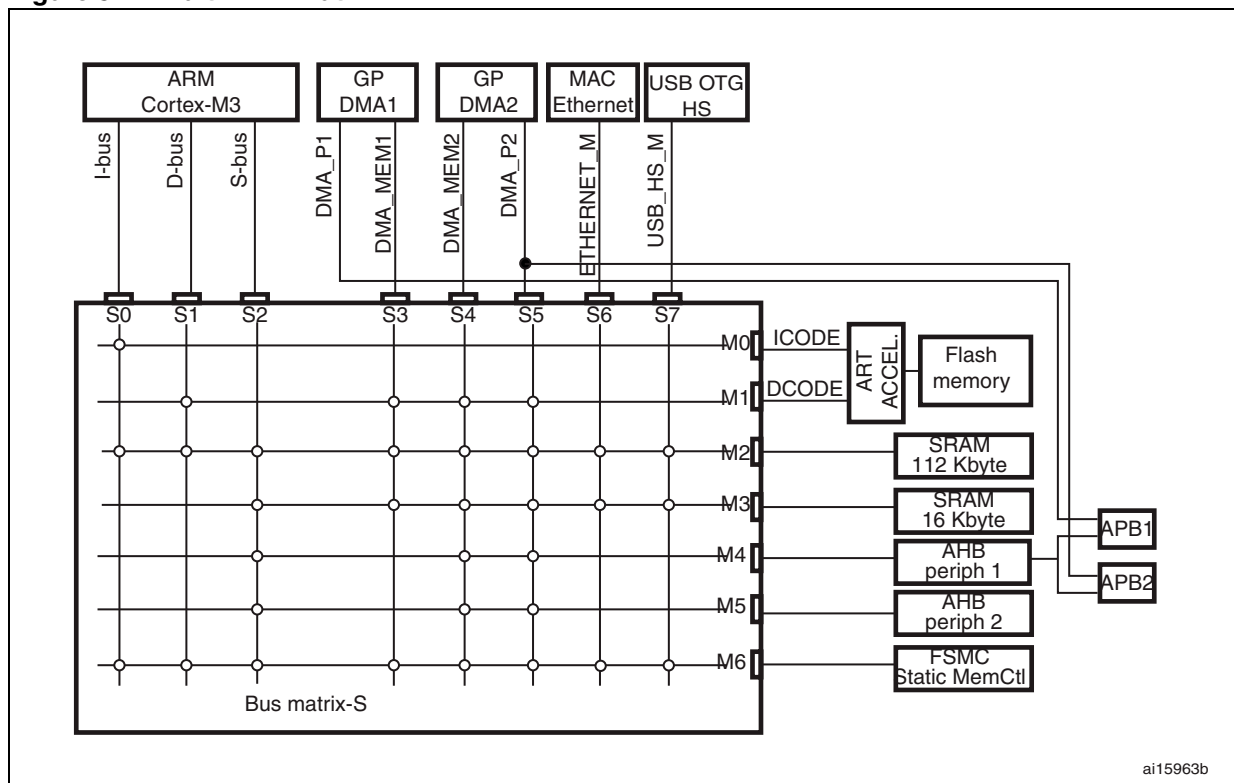
2.2.7 Embedded SRAM

All STM32F21x products embed up to 128 Kbytes of system SRAM accessed (read/write) at CPU clock speed with 0 wait states, plus 4 Kbytes of backup SRAM.

2.2.8 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 5. Multi-AHB matrix



2.2.9 DMA

The flexible 16-stream general-purpose DMAs (8 streams for DMA1 and 8 streams for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They share some centralized FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB) and performance.

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I²S
- I²C
- USART and UART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Cryptographic acceleration
- Camera interface (DCMI)
- ADC.

2.2.10 FSMC (flexible static memory controller)

The FSMC is embedded in the STM32F215xx and STM32F217xx family. It has four Chip Select outputs supporting the following modes: PCCard/Compact Flash, SRAM, PSRAM, NOR Flash and NAND Flash.

Functionality overview:

- Write FIFO
- Code execution from external memory except for NAND Flash and PC Card
- The targeted frequency, f_{CLK} , is equal to $HCLK/2$, so external access is at 60 MHz when HCLK is at 120 MHz and external access is at 30 MHz when HCLK is at 60 MHz

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

2.2.11 Nested vectored interrupt controller (NVIC)

The STM32F215xx and STM32F217xx embed a nested vectored interrupt controller able to handle up to 87 maskable interrupt channels (not including the 16 interrupt lines of the Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

2.2.12 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 140 GPIOs can be connected to the 16 external interrupt lines.

2.2.13 Clocks and startup

System clock selection is performed on startup, however, the 16 MHz internal RC oscillator is selected as the default CPU clock on reset. An external 4-26 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy over the full temperature range.

The advanced clock controller clocks the core and all peripherals using a single crystal or oscillator. In particular, the ethernet and USB OTG FS peripherals can be clocked by the system clock.

Several prescalers and PLLs allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 120 MHz and the maximum frequency the high-speed APB domains is 60 MHz. The maximum allowed frequency of the low-speed APB domain is 30 MHz.

In order to achieve audio class performance, a specific crystal can be used. In this case, the I²S master clock can generate all standard sampling frequencies from 8 kHz to 96 kHz.

2.2.14 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB6), USB OTG FS in Device mode (PA9/PA11/PA12) through DFU (device firmware upgrade).

2.2.15 Power supply schemes

- $V_{DD} = 1.8$ to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins. On WLCSP package, V_{DD} ranges from 1.65 to 3.6 V.
- V_{SSA} , $V_{DDA} = 1.8$ to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

2.2.16 Power supply supervisor

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for an external reset circuit. On devices in WLCSP package, BOR can be inactivated by setting IRROFF to V_{DD} (see [Section 2.2.17: Voltage regulator](#)).

The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.2.17 Voltage regulator

The regulator has five operating modes:

- Regulator on
 - Main regulator mode (MR)
 - Low power regulator (LPR)
 - Power-down
- Regulator off
 - Regulator bypass/regulator off
 - Regulator bypass/regulator off and internal reset off

Regulator on

These modes are activated by default on LQFP packages. On WLCPS66 and UFBGA176, they are activated by setting REGOFF pin to V_{SS} . V_{DD} minimum value is 1.8 V.

There are three regulator on modes:

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes⁷
- Power-down is used in Standby mode:
The regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

Regulator off

- Regulator bypass/regulator off

This mode is activated by setting REGOFF pin to V_{DD} . It is available only on the UFBGA and WLCSP packages.

The regulator bypass/regulator off mode allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins, in addition to V_{DD} .

V_{DD} minimum value is 1.8 V.

The following conditions must be respected in Regulator bypass mode:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is faster than the time for V_{DD} to reach 1.8 V, then PA0 should be connected to the NRST pin (see [Figure 6](#)). Otherwise, PA0 should be asserted low externally until V_{DD} reaches 1.8 V (see [Figure 7](#)).

In regulator bypass only mode, PA0 cannot be used as a GPIO pin.

- Regulator bypass/regulator off and internal reset off

This mode is activated by setting IRROFF pin to V_{DD} . IRROFF cannot be activated in conjunction with REGOFF. This mode is available only on the WLCSP package. It allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins, in addition to V_{DD} .

V_{DD} minimum value is 1.65 V.

The following conditions must be respected in Regulator bypass mode (see [Figure 8](#)):

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- External reset should be used to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach 1.08V and until V_{DD} reaches 1.65 V

PA0 can be used as a standard GPIO pin.

Figure 6. Startup in regulator bypass/regulator off mode: slow V_{DD} slope - power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization

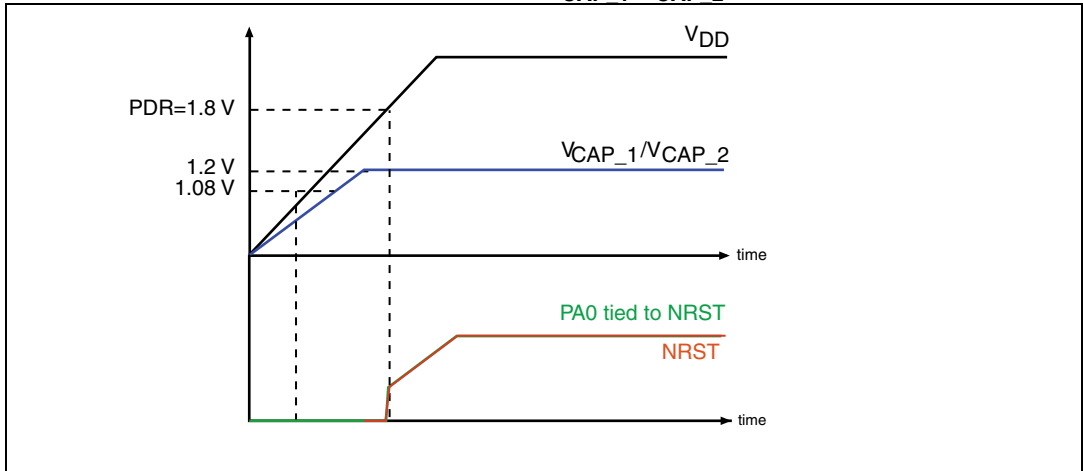


Figure 7. Startup in regulator bypass/regulator off mode: slow V_{DD} slope - power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization

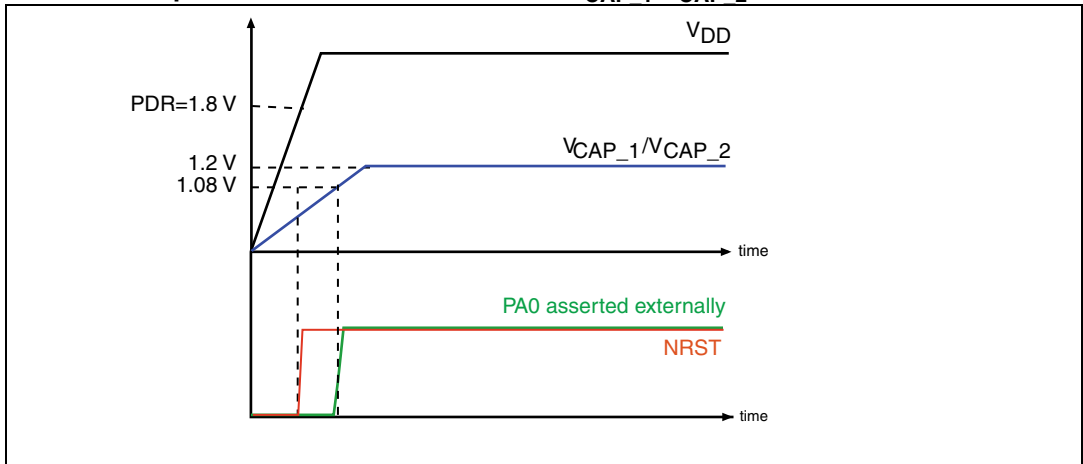
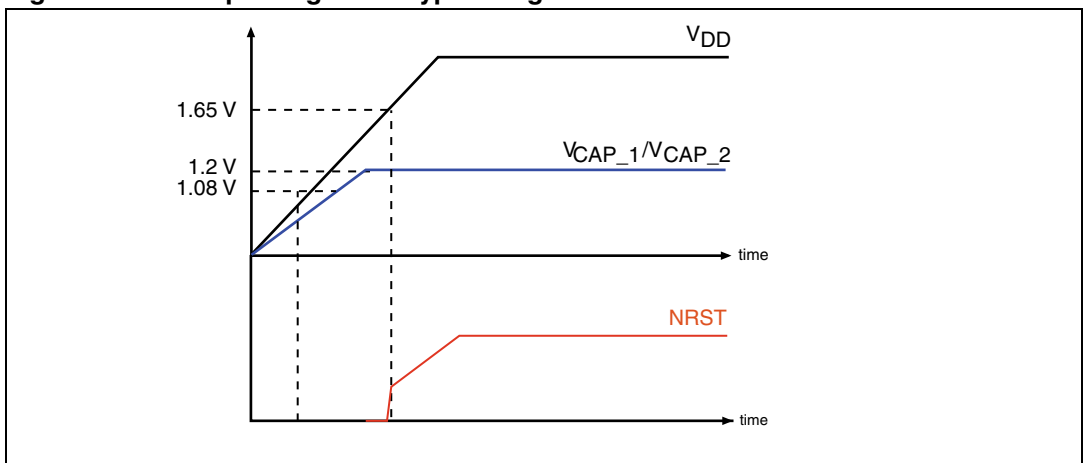


Figure 8. Startup in regulator bypass/regulator off and internal reset off



2.2.18 Real-time clock (RTC), backup SRAM and backup registers

The backup domain of the STM32F215xx and STM32F217xx includes:

- The real-time clock (RTC)
- 4 Kbytes of backup SRAM
- 20 backup registers

The RTC provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

The RTC features calendar registers with seconds, minutes, hours, week day, date, month, year. Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 μ s to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup SRAM size is 4 Kbytes and can be enabled by software. When the backup RAM is enabled the power consumption in Standby or V_{BAT} mode is slightly higher (see [Section 2.2.19: Low-power modes](#)).

The backup registers are 32-bit registers used to store 80 bytes of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see [Section 2.2.19: Low-power modes](#)).

The RTC, backup RAM and backup registers are supplied through a switch that takes power from either the V_{DD} supply when present or the V_{BAT} pin.

2.2.19 Low-power modes

The STM32F215xx and STM32F217xx support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC

and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from the Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

Note: 1 The RTC, the IWDG, and the corresponding clock sources are not stopped when the device enters the Stop or Standby mode.

2.2.20 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery or an external supercapacitor.

V_{BAT} operation is activated when V_{DD} is not present.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

2.2.21 Timers and watchdogs

The STM32F215xx and STM32F217xx devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

[Table 3](#) compares the features of the advanced-control, general-purpose and basic timers.

Table 3. Timer feature comparison

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary output | Max interface clock | Max timer clock |
|------------------|------------|--------------------|-------------------|---------------------------------|------------------------|--------------------------|----------------------|---------------------|-----------------|
| Advanced-control | TIM1, TIM8 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | Yes | 60 MHz | 120 MHz |
| General purpose | TIM2, TIM5 | 32-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 30 MHz | 60 MHz |
| | TIM3, TIM4 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 30 MHz | 60 MHz |
| Basic | TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No | 30 MHz | 60 MHz |

Table 3. Timer feature comparison (continued)

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary output | Max interface clock | Max timer clock |
|-----------------|--------------|--------------------|--------------|---------------------------------|------------------------|--------------------------|----------------------|---------------------|-----------------|
| General purpose | TIM9 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 60 MHz | 120 MHz |
| | TIM10, TIM11 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 60 MHz | 120 MHz |
| | TIM12 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 30 MHz | 60 MHz |
| | TIM13, TIM14 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 30 MHz | 60 MHz |

Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The TIM1 and TIM8 counters can be frozen in debug mode. Many of the advanced-control timer features are shared with those of the standard TIMx timers which have the same architecture. The advanced-control timer can therefore work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F21x devices (see [Table 3](#) for differences).

- **TIM2, TIM3, TIM4, TIM5**

The STM32F21x include 4 full-featured general-purpose timers. TIM2 and TIM5 are 32-bit timers, and TIM3 and TIM4 are 16-bit timers. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 32-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

The counters of TIM2, TIM3, TIM4, TIM5 can be frozen in debug mode. Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM10, TIM11 and TIM9**

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

- **TIM12, TIM13 and TIM14**

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13 and TIM14 feature one independent channel, whereas TIM12 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

They can also be used as simple time bases.

2.2.22 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

2.2.23 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

The counter can be frozen in debug mode.

2.2.24 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.2.25 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.26 I²C bus

Up to three I²C bus interfaces can operate in multimaster and slave modes. They can support the Standard- and Fast-modes. They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.2.27 Universal synchronous/asynchronous receiver transmitters (UARTs/USARTs)

The STM32F215xx and STM32F217xx embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and two universal asynchronous receiver transmitters (UART4 and UART5).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 7.5 Mbit/s. The other available interfaces communicate at up to 3.75 Mbit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 4. USART feature comparison

| USART name | Standard features | Modem (RTS/CTS) | LIN | SPI master | IrDA | Smartcard (ISO 7816) | Max. baud rate in Mbit/s (oversampling by 16) | Max. baud rate in Mbit/s (oversampling by 8) | APB mapping |
|------------|-------------------|-----------------|-----|------------|------|----------------------|---|--|--------------------|
| USART1 | X | X | X | X | X | X | 3.75 | 7.5 | APB2 (max. 60 MHz) |
| USART2 | X | X | X | X | X | X | 1.87 | 3.75 | APB1 (max. 30 MHz) |
| USART3 | X | X | X | X | X | X | 1.87 | 3.75 | APB1 (max. 30 MHz) |

Table 4. USART feature comparison (continued)

| USART name | Standard features | Modem (RTS/CTS) | LIN | SPI master | irDA | Smartcard (ISO 7816) | Max. baud rate in Mbit/s (oversampling by 16) | Max. baud rate in Mbit/s (oversampling by 8) | APB mapping |
|------------|-------------------|-----------------|-----|------------|------|----------------------|---|--|--------------------|
| UART4 | X | - | X | - | X | - | 1.87 | 3.75 | APB1 (max. 30 MHz) |
| UART5 | X | - | XD | - | X | - | 3.75 | 3.75 | APB1 (max. 30 MHz) |
| USART6 | X | X | X | X | X | X | 3.75 | 7.5 | APB2 (max. 60 MHz) |

2.2.28 Serial peripheral interface (SPI)

The STM32F21x feature up to three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 can communicate at up to 30 Mbits/s, SPI2 and SPI3 can communicate at up to 15 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

2.2.29 Inter-integrated sound (I²S)

Two standard I²S interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 96 kHz are supported. When either or both of the I²S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

2.2.30 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

2.2.31 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral available only on the STM32F217xx devices.

The STM32F217xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The STM32F217xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F217xx MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) or 50 MHz (RMII) output from the STM32F217xx.

The STM32F217xx includes the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F20x and STM32F21x reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes, that is 4 Kbytes in total
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

2.2.32 Controller area network (CAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOs with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). The 256 bytes of SRAM which are allocated for each CAN are not shared with any other peripheral.

2.2.33 Universal serial bus on-the-go full-speed (OTG_FS)

The STM32F215xx and STM32F217xx embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller

requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- Internal FS OTG PHY support
- External FS OTG PHY support through an I²C connection

2.2.34 Universal serial bus on-the-go high-speed (OTG_HS)

The STM32F215xx and STM32F217xx devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 1 Kbit × 35 with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External FS OTG PHY support through an I²C connection
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.2.35 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I²S application. It allows to achieve error-free I²S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I²S sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 96 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I2S flow with an external PLL (or Codec output).

2.2.36 Digital camera interface (DCMI)

The camera interface is *not* available in STM32F215xx devices.

STM32F217xx products embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain up to 27 Mbyte/s at 27 MHz or 48 Mbyte/s at 48 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

2.2.37 Cryptographic acceleration

The STM32F215xx and STM32F217xx devices embed a cryptographic accelerator. This cryptographic accelerator provides a set of hardware acceleration for the advanced cryptographic algorithms usually needed to provide confidentiality, authentication, data integrity and non repudiation when exchanging messages with a peer.

- These algorithms consists of :
 - Encryption/Decryption
 - DES/TDES (data encryption standard/triple data encryption standard): ECB (electronic codebook) and CBC (cipher block chaining) chaining algorithms, 64-, 128- or 192-bit key
 - AES (advanced encryption standard): ECB, CBC and CTR (counter mode) chaining algorithms, 128, 192 or 256-bit key
 - Universal hash
 - SHA-1 (secure hash algorithm)
 - MD5
- It also provides a true random number generator that deliver 32-bit random numbers produced by an integrated analog circuit.

2.2.38 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O alternate function configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

To provide fast I/O handling, the GPIOs are on the fast AHB1 bus with a clock up to 120 MHz that leads to a maximum I/O toggling speed of 60 MHz.

2.2.39 ADCs (analog-to-digital converters)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the timers TIM1, TIM2, TIM3, TIM4, TIM5 and TIM8 can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

2.2.40 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

2.2.41 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.8 V and 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

2.2.42 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

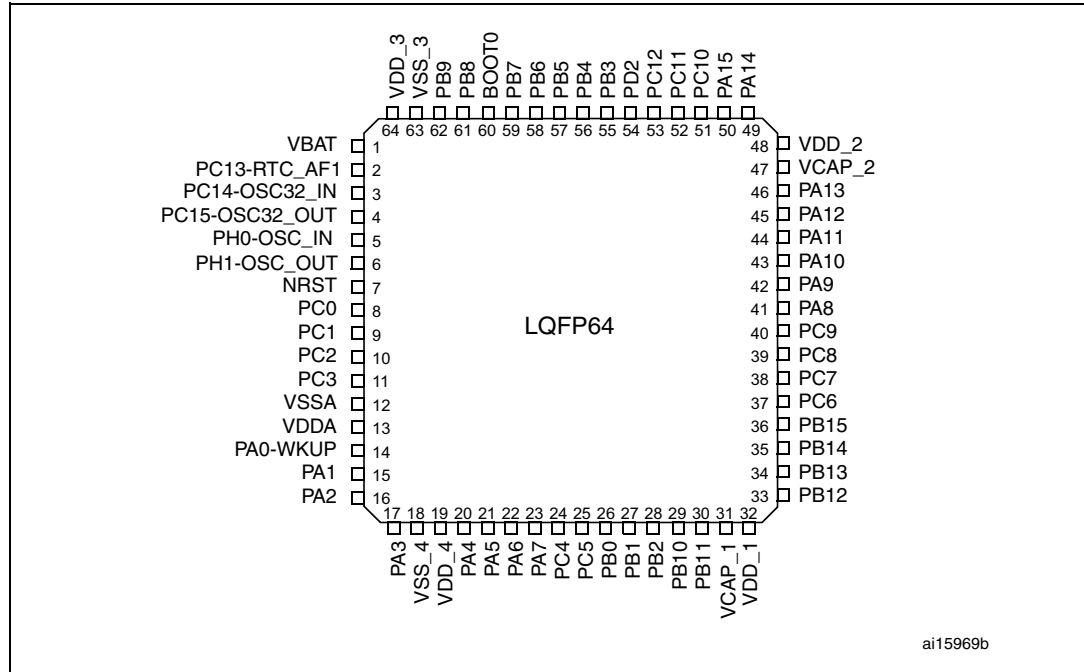
2.2.43 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F21x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

3 Pinouts and pin description

Figure 9. STM32F21x LQFP64 pinout



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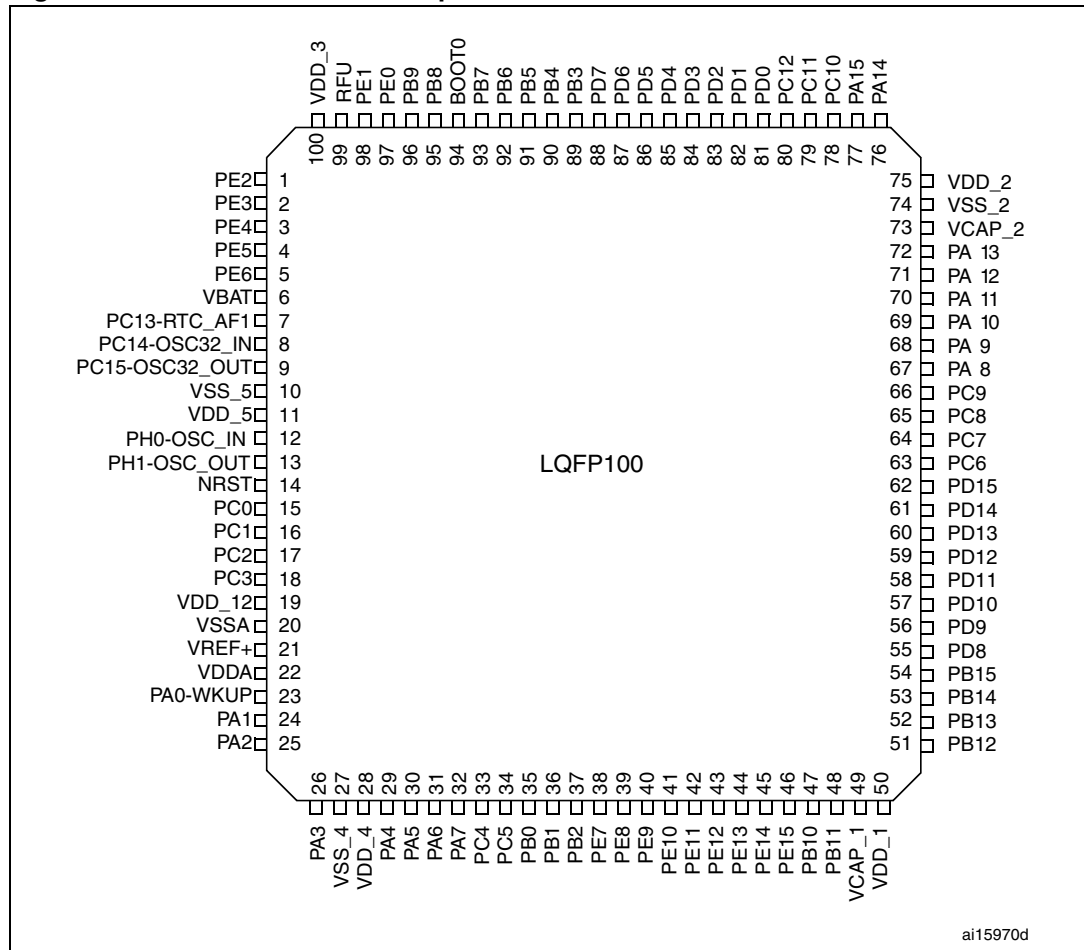
Figure 10. STM32F21x WLCSP64+2 ballout

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|-------|--------|--------|-----|-----|-------|--------|--------|------------------|
| A | PA14 | PA15 | PC12 | PB3 | PB5 | PB7 | PB9 | VDD_2 | V _{BAT} |
| B | VSS_2 | PA13 | PC10 | PB4 | PB6 | BOOT0 | PB8 | PC13 | PC14 |
| C | PA12 | VCAP_2 | PC11 | | | | PD2 | PDROFF | PC15 |
| D | PC9 | PA11 | PA10 | | | | PC2 | VSS_3 | VDD_3 |
| E | VDD_4 | PA8 | PA9 | | | | PA0 | NRST | PH0-OSC_IN |
| F | VSS_4 | PC7 | PC8 | | | | VREF+ | PC1 | PH1-OSC_OUT |
| G | PB15 | PC6 | PC5 | | | | PA3 | PC3 | PC0 |
| H | PB14 | PB13 | PB10 | PC4 | PA6 | PA5 | REGOFF | PA1 | VSS_5 |
| J | PB12 | PB11 | VCAP_1 | PB2 | PB1 | PB0 | PA7 | PA4 | PA2 |

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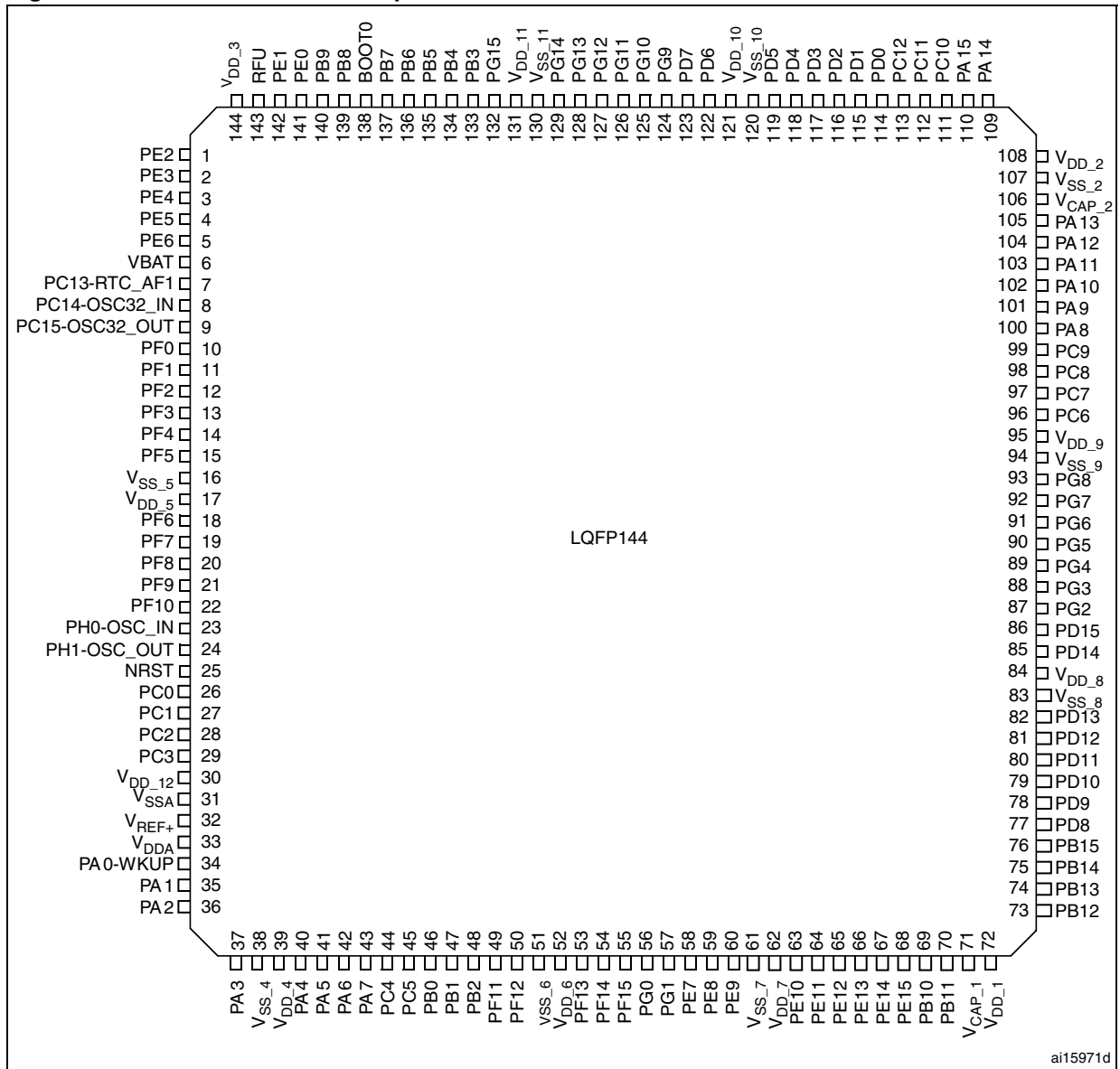
1. Top view.

Figure 11. STM32F21x LQFP100 pinout



1. RFU means "reserved for future use".

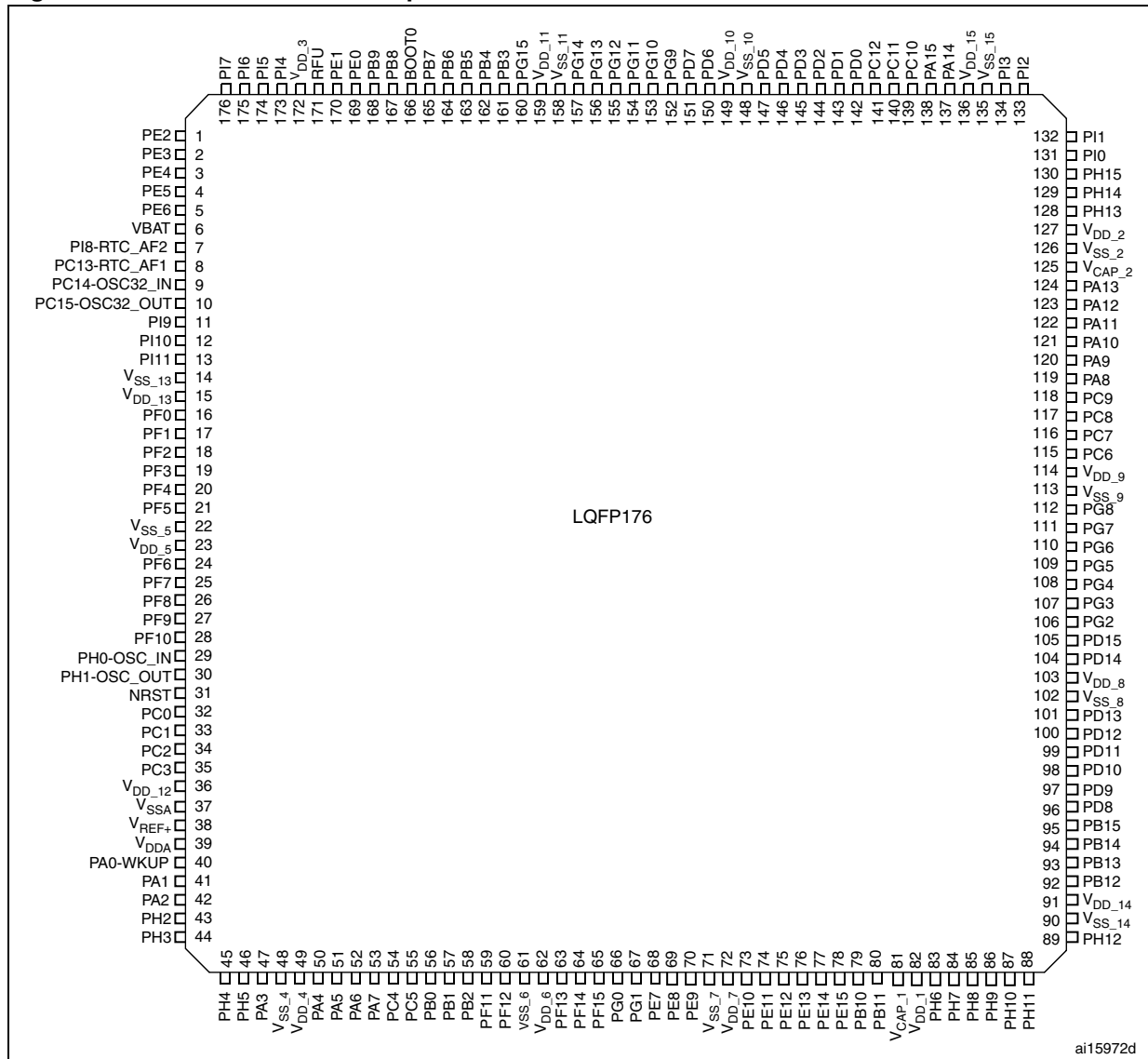
Figure 12. STM32F21x LQFP144 pinout



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1. RFU means "reserved for future use".

Figure 13. STM32F21x LQFP176 pinout



1. Package not in production and available for development only.
2. RFU means "reserved for future use".

Figure 14. STM32F21xxx UFBGA176 ballout

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----|----------------|-----------|----------|--------|---|-------|--------|--------|--------|-------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|------|-----|-----|
| A | PE3 | PE2 | PE1 | PE0 | PB8 | PB5 | PG14 | PG13 | PB4 | PB3 | PD7 | PC12 | PA15 | PA14 | PA13 | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | PE4 | PE5 | PE6 | PB9 | PB7 | PB6 | PG15 | PG12 | PG11 | PG10 | PD6 | PD0 | PC11 | PC10 | PA12 | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | VBAT | PI7 | PI6 | PI5 | VDD_3 | RFU | VDD_11 | VDD_10 | VDD_15 | PG9 | PD5 | PD1 | PI3 | PI2 | PA11 | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | PC13-TAMP1 | PI8-TAMP2 | PI9 | PI4 | VSS | BOOT0 | VSS_11 | VSS_10 | VSS_15 | PD4 | PD3 | PD2 | PH15 | PI1 | PA10 | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | PC14-OSC32_IN | PF0 | PI10 | PI11 | <table border="1" style="margin: auto;"> <tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td></tr> <tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td></tr> <tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td></tr> <tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td></tr> <tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td></tr> </table> | | | | | | | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | PH13 | PH14 | PI0 | PA9 |
| VSS | VSS | VSS | VSS | VSS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VSS | VSS | VSS | VSS | VSS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VSS | VSS | VSS | VSS | VSS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VSS | VSS | VSS | VSS | VSS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VSS | VSS | VSS | VSS | VSS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | PC15-OSC32_OUT | VSS_13 | VDD_13 | PH2 | VSS_2 | VCAP2 | PC9 | PA8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | PH0-OSC_IN | VSS_5 | VDD_5 | PH3 | VSS_9 | VDD_2 | PC8 | PC7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | PH1-OSC_OUT | PF2 | PF1 | PH4 | VSS_14 | VDD_9 | PG8 | PC6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | NRST | PF3 | PF4 | PH5 | VDD_14 | VDD_8 | PG7 | PC6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | PF7 | PF6 | PF5 | VDD_4 | PH12 | PG5 | PG4 | PG3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | PF10 | PF9 | PF8 | REGOFF | PH11 | PH10 | PD15 | PG2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | VSSA | PC0 | PC1 | PC2 | PC3 | PB2 | PG1 | VSS_6 | VSS_7 | VCAP1 | PH6 | PH8 | PH9 | PD14 | PD13 | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | VREF- | PA1 | PA0-WKUP | PA4 | PC4 | PF13 | PG0 | VDD_6 | VDD_7 | VDD_1 | PE13 | PH7 | PD12 | PD11 | PD10 | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | VREF+ | PA2 | PA6 | PA5 | PC5 | PF12 | PF15 | PE8 | PE9 | PE11 | PE14 | PB12 | PB13 | PD9 | PD8 | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | VDDA | PA3 | PA7 | PB1 | PB0 | PF11 | PF14 | PE7 | PE10 | PE12 | PE15 | PB10 | PB11 | PB14 | PB15 | | | | | | | | | | | | | | | | | | | | | | | | | |

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1. RFU means "reserved for future use".
2. Top view.

Table 5. STM32F21x pin and ball definitions

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|---|---------------------|--------------------------|---|---|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| - | - | 1 | 1 | 1 | A2 | PE2 | I/O | FT | PE2 | TRACECLK/ FSMC_A23 / ETH_MII_TXD3 | |
| - | - | 2 | 2 | 2 | A1 | PE3 | I/O | FT | PE3 | TRACED0/FSMC_A19 | |
| - | - | 3 | 3 | 3 | B1 | PE4 | I/O | FT | PE4 | TRACED1/FSMC_A20 / DCMI_D4 | |
| - | - | 4 | 4 | 4 | B2 | PE5 | I/O | FT | PE5 | TRACED2 / FSMC_A21 / TIM9_CH1 / DCMI_D6 | |
| - | - | 5 | 5 | 5 | B3 | PE6 | I/O | FT | PE6 | TRACED3 / FSMC_A22 / TIM9_CH2 / DCMI_D7 | |
| 1 | A9 | 6 | 6 | 6 | C1 | V _{BAT} | S | | V _{BAT} | | |
| - | - | - | - | 7 | D2 | PI8 ⁽⁴⁾ | I/O | FT | PI8 ⁽⁵⁾ | | RTC_AF2 |
| 2 | B8 | 7 | 7 | 8 | D1 | PC13 ⁽⁴⁾ | I/O | FT | PC13 ⁽⁵⁾ | | RTC_AF1 |
| 3 | B9 | 8 | 8 | 9 | E1 | PC14 ⁽⁴⁾ -OSC32_IN ⁽⁶⁾ | I/O | FT | PC14 ⁽⁵⁾ | | OSC32_IN |
| 4 | C9 | 9 | 9 | 10 | F1 | PC15 ⁽⁴⁾ -OSC32_OUT ⁽⁶⁾ | I/O | FT | PC15 ⁽⁵⁾ | | OSC32_OUT |
| - | - | - | - | 11 | D3 | PI9 | I/O | FT | PI9 | CAN1_RX | |
| - | - | - | - | 12 | E3 | PI10 | I/O | FT | PI10 | ETH_MII_RX_ER | |
| - | - | - | - | 13 | E4 | PI11 | I/O | FT | PI11 | OTG_HS_ULPI_DIR | |
| - | - | - | - | 14 | F2 | V _{SS_13} | S | | V _{SS_13} | | |
| - | - | - | - | 15 | F3 | V _{DD_13} | S | | V _{DD_13} | | |
| - | - | - | 10 | 16 | E2 | PF0 | I/O | FT | PF0 | FSMC_A0 / I2C2_SDA | |
| - | - | - | 11 | 17 | H3 | PF1 | I/O | FT | PF1 | FSMC_A1 / I2C2_SCL | |
| - | - | - | 12 | 18 | H2 | PF2 | I/O | FT | PF2 | FSMC_A2 / I2C2_SMBA | |
| - | - | - | 13 | 19 | J2 | PF3 ⁽⁶⁾ | I/O | FT | PF3 | FSMC_A3 | ADC3_IN9 |
| - | - | - | 14 | 20 | J3 | PF4 ⁽⁶⁾ | I/O | FT | PF4 | FSMC_A4 | ADC3_IN14 |
| - | - | - | 15 | 21 | K3 | PF5 ⁽⁶⁾ | I/O | FT | PF5 | FSMC_A5 | ADC3_IN15 |
| - | H9 | 10 | 16 | 22 | G2 | V _{SS_5} | S | | V _{SS_5} | | |
| - | - | 11 | 17 | 23 | G3 | V _{DD_5} | S | | V _{DD_5} | | |
| - | - | - | 18 | 24 | K2 | PF6 ⁽⁶⁾ | I/O | FT | PF6 | TIM10_CH1 / FSMC_NIORD | ADC3_IN4 |
| - | - | - | 19 | 25 | K1 | PF7 ⁽⁶⁾ | I/O | FT | PF7 | TIM11_CH1/FSMC_NREG | ADC3_IN5 |
| - | - | - | 20 | 26 | L3 | PF8 ⁽⁶⁾ | I/O | FT | PF8 | TIM13_CH1 / FSMC_NIOWR | ADC3_IN6 |
| - | - | - | 21 | 27 | L2 | PF9 ⁽⁶⁾ | I/O | FT | PF9 | TIM14_CH1 / FSMC_CD | ADC3_IN7 |

Table 5. STM32F21x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|---|---------------------|--------------------------|---|---|----------------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| - | - | - | 22 | 28 | L1 | PF10 ⁽⁶⁾ | I/O | FT | PF10 | FSMC_INTR | ADC3_IN8 |
| 5 | E9 | 12 | 23 | 29 | G1 | PH0 ⁽⁶⁾ -OSC_IN | I/O | FT | PH0 | | OSC_IN |
| 6 | F9 | 13 | 24 | 30 | H1 | PH1 ⁽⁶⁾ -OSC_OUT | I/O | FT | PH1 | | OSC_OUT |
| 7 | E8 | 14 | 25 | 31 | J1 | NRST | I/O | | NRST | | |
| 8 | G9 | 15 | 26 | 32 | M2 | PC0 ⁽⁶⁾ | I/O | FT | PC0 | OTG_HS_ULPI_STP | ADC123_IN10 |
| 9 | F8 | 16 | 27 | 33 | M3 | PC1 ⁽⁶⁾ | I/O | FT | PC1 | ETH_MDC | ADC123_IN11 |
| 10 | D7 | 17 | 28 | 34 | M4 | PC2 ⁽⁶⁾ | I/O | FT | PC2 | SPI2_MISO / OTG_HS_ULPI_DIR / ETH_MII_TXD2 | ADC123_IN12 |
| 11 | G8 | 18 | 29 | 35 | M5 | PC3 ⁽⁶⁾ | I/O | FT | PC3 | SPI2_MOSI / I2S2_SD / OTG_HS_ULPI_NXT / ETH_MII_TX_CLK | ADC123_IN13 |
| - | - | 19 | 30 | 36 | - | V _{DD_12} | S | | V _{DD_12} | | |
| 12 | - | 20 | 31 | 37 | M1 | V _{SSA} | S | | V _{SSA} | | |
| - | - | - | - | - | N1 | V _{REF-} | S | | V _{REF-} | | |
| - | F7 | 21 | 32 | 38 | P1 | V _{REF+} | S | | V _{REF+} | | |
| 13 | - | 22 | 33 | 39 | R1 | V _{DDA} | S | | V _{DDA} | | |
| 14 | E7 | 23 | 34 | 40 | N3 | PA0 ⁽⁷⁾ -WKUP ⁽⁶⁾ | I/O | FT | PA0-WKUP | USART2_CTS / UART4_TX / ETH_MII_CRD / TIM2_CH1_ETR / TIM5_CH1 / TIM8_ETR | ADC123_CH0 / WKUP |
| 15 | H8 | 24 | 35 | 41 | N2 | PA1 ⁽⁶⁾ | I/O | FT | PA1 | USART2_RTS / UART4_RX / ETH_RMII_REF_CLK / ETH_MII_RX_CLK / TIM5_CH2 / TIM2_CH2 | ADC123_IN1 |
| 16 | J9 | 25 | 36 | 42 | P2 | PA2 ⁽⁶⁾ | I/O | FT | PA2 | USART2_TX / TIM5_CH3 / TIM9_CH1 / TIM2_CH3 / ETH_MDIO | ADC123_IN2 |
| - | - | - | - | 43 | F4 | PH2 | I/O | FT | PH2 | ETH_MII_CRD | |
| - | - | - | - | 44 | G4 | PH3 | I/O | FT | PH3 | ETH_MII_COL | |
| - | - | - | - | 45 | H4 | PH4 | I/O | FT | PH4 | I2C2_SCL / OTG_HS_ULPI_NXT | |
| - | - | - | - | 46 | J4 | PH5 | I/O | FT | PH5 | I2C2_SDA | |

Table 5. STM32F21x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|--------------------|---------------------|--------------------------|---|---|------------------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| 17 | G7 | 26 | 37 | 47 | R2 | PA3 ⁽⁶⁾ | I/O | FT | PA3 | USART2_RX/TIM5_CH4 / TIM9_CH2 / TIM2_CH4 / OTG_HS_ULPI_D0 / ETH_MII_COL | ADC123_IN3 |
| 18 | F1 | 27 | 38 | 48 | - | V _{SS_4} | S | | V _{SS_4} | | |
| | H7 | | | | L4 | REGOFF | I/O | | REGOFF | | |
| 19 | E1 | 28 | 39 | 49 | K4 | V _{DD_4} | S | | V _{DD_4} | | |
| 20 | J8 | 29 | 40 | 50 | N4 | PA4 ⁽⁶⁾ | I/O | | PA4 | SPI1_NSS / SPI3_NSS / USART2_CK / DCMI_HSYNC / OTG_HS_SOF/ I2S3_WS | ADC12_IN4 /DAC1_OUT |
| 21 | H6 | 30 | 41 | 51 | P4 | PA5 ⁽⁶⁾ | I/O | | PA5 | SPI1_SCK/ OTG_HS_ULPI_CK // TIM2_CH1_ETR/ TIM8_CHIN | ADC12_IN5 /DAC2_OUT |
| 22 | H5 | 31 | 42 | 52 | P3 | PA6 ⁽⁶⁾ | I/O | FT | PA6 | SPI1_MISO / TIM8_BKIN/TIM13_CH1 / DCMI_PIXCLK / TIM3_CH1 / TIM1_BKIN | ADC12_IN6 |
| 23 | J7 | 32 | 43 | 53 | R3 | PA7 ⁽⁶⁾ | I/O | FT | PA7 | SPI1_MOSI/ TIM8_CH1N / TIM14_CH1 TIM3_CH2/ ETH_MII_RX_DV / TIM1_CH1N / RMII_CRS_DV | ADC12_IN7 |
| 24 | H4 | 33 | 44 | 54 | N5 | PC4 ⁽⁶⁾ | I/O | FT | PC4 | ETH_RMII_RX_D0 / ETH_MII_RX_D0 | ADC12_IN14 |
| 25 | G3 | 34 | 45 | 55 | P5 | PC5 ⁽⁶⁾ | I/O | FT | PC5 | ETH_RMII_RX_D1 / ETH_MII_RX_D1 | ADC12_IN15 |
| 26 | J6 | 35 | 46 | 56 | R5 | PB0 ⁽⁶⁾ | I/O | FT | PB0 | TIM3_CH3 / TIM8_CH2N/ OTG_HS_ULPI_D1/ ETH_MII_RXD2 / TIM1_CH2N | ADC12_IN8 |
| 27 | J5 | 36 | 47 | 57 | R4 | PB1 ⁽⁶⁾ | I/O | FT | PB1 | TIM3_CH4 / TIM8_CH3N/ OTG_HS_ULPI_D2/ ETH_MII_RXD3 / OTG_HS_INTN / TIM1_CH3N | ADC12_IN9 |
| 28 | J4 | 37 | 48 | 58 | M6 | PB2 | I/O | FT | PB2-BOOT1 | | |
| - | - | - | 49 | 59 | R6 | PF11 | I/O | FT | PF11 | DCMI_12 | |
| - | - | - | 50 | 60 | P6 | PF12 | I/O | FT | PF12 | FSMC_A6 | |

Table 5. STM32F21x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|--------------------|---------------------|--------------------------|---|--|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| - | - | - | 51 | 61 | M8 | V _{SS_6} | S | | V _{SS_6} | | |
| - | - | - | 52 | 62 | N8 | V _{DD_6} | S | | V _{DD_6} | | |
| - | - | - | 53 | 63 | N6 | PF13 | I/O | FT | PF13 | FSMC_A7 | |
| - | - | - | 54 | 64 | R7 | PF14 | I/O | FT | PF14 | FSMC_A8 | |
| - | - | - | 55 | 65 | P7 | PF15 | I/O | FT | PF15 | FSMC_A9 | |
| - | - | - | 56 | 66 | N7 | PG0 | I/O | FT | PG0 | FSMC_A10 | |
| - | - | - | 57 | 67 | M7 | PG1 | I/O | FT | PG1 | FSMC_A11 | |
| - | - | 38 | 58 | 68 | R8 | PE7 | I/O | FT | PE7 | FSMC_D4/TIM1_ETR | |
| - | - | 39 | 59 | 69 | P8 | PE8 | I/O | FT | PE8 | FSMC_D5/TIM1_CH1N | |
| - | - | 40 | 60 | 70 | P9 | PE9 | I/O | FT | PE9 | FSMC_D6/TIM1_CH1 | |
| - | - | - | 61 | 71 | M9 | V _{SS_7} | S | | V _{SS_7} | | |
| - | - | - | 62 | 72 | N9 | V _{DD_7} | S | | V _{DD_7} | | |
| - | - | 41 | 63 | 73 | R9 | PE10 | I/O | FT | PE10 | FSMC_D7/TIM1_CH2N | |
| - | - | 42 | 64 | 74 | P10 | PE11 | I/O | FT | PE11 | FSMC_D8/TIM1_CH2 | |
| - | - | 43 | 65 | 75 | R10 | PE12 | I/O | FT | PE12 | FSMC_D9/TIM1_CH3N | |
| - | - | 44 | 66 | 76 | N11 | PE13 | I/O | FT | PE13 | FSMC_D10/TIM1_CH3 | |
| - | - | 45 | 67 | 77 | P11 | PE14 | I/O | FT | PE14 | FSMC_D11/TIM1_CH4 | |
| - | - | 46 | 68 | 78 | R11 | PE15 | I/O | FT | PE15 | FSMC_D12/TIM1_BKIN | |
| 29 | H3 | 47 | 69 | 79 | R12 | PB10 | I/O | FT | PB10 | SPI2_SCK/ I2S2_CK/ I2C2_SCL / USART3_TX / OTG_HS_ULPI_D3 / ETH_MII_RX_ER / OTG_HS_SCL / TIM2_CH3 | |
| 30 | J2 | 48 | 70 | 80 | R13 | PB11 | I/O | FT | PB11 | I2C2_SDA/USART3_RX/ OTG_HS_ULPI_D4 / ETH_RMII_TX_EN/ ETH_MII_TX_EN / OTG_HS_SDA / TIM2_CH4 | |
| 31 | J3 | 49 | 71 | 81 | M10 | V _{CAP_1} | S | | V _{CAP_1} | | |
| 32 | - | 50 | 72 | 82 | N10 | V _{DD_1} | S | | V _{DD_1} | | |
| - | - | - | - | 83 | M11 | PH6 | I/O | FT | PH6 | I2C2_SMBA / TIM12_CH1 / ETH_MII_RXD2 | |
| - | - | - | - | 84 | N12 | PH7 | I/O | FT | PH7 | I2C3_SCL / ETH_MII_RXD3 | |
| - | - | - | - | 85 | M12 | PH8 | I/O | FT | PH8 | I2C3_SDA / DCMI_HSYNC | |

Table 5. STM32F21x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|--------------------|---------------------|--------------------------|---|--|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| - | - | - | - | 86 | M13 | PH9 | I/O | FT | PH9 | I2C3_SMBA / TIM12_CH2/ DCMI_D0 | |
| - | - | - | - | 87 | L13 | PH10 | I/O | FT | PH10 | TIM5_CH1_ETR / DCMI_D1 | |
| - | - | - | - | 88 | L12 | PH11 | I/O | FT | PH11 | TIM5_CH2 / DCMI_D2 | |
| - | - | - | - | 89 | K12 | PH12 | I/O | FT | PH12 | TIM5_CH3 / DCMI_D3 | |
| - | - | - | - | 90 | H12 | V _{SS_14} | S | | V _{SS_14} | | |
| - | - | - | - | 91 | J12 | V _{DD_14} | S | | V _{DD_14} | | |
| 33 | J1 | 51 | 73 | 92 | P12 | PB12 | I/O | FT | PB12 | SPI2_NSS/I2S2_WS/ I2C2_SMBA/ USART3_CK/ TIM1_BKIN / CAN2_RX / OTG_HS_ULPI_D5/ ETH_RMII_TXD0 / ETH_MII_TXD0/ OTG_HS_ID | |
| 34 | H2 | 52 | 74 | 93 | P13 | PB13 | I/O | FT | PB13 | SPI2_SCK / I2S2_CK / USART3_CTS/ TIM1_CH1N /CAN2_TX / OTG_HS_ULPI_D6 / ETH_RMII_TXD1 / ETH_MII_TXD1 | OTG_HS_VBUS |
| 35 | H1 | 53 | 75 | 94 | R14 | PB14 | I/O | FT | PB14 | SPI2_MISO/ TIM1_CH2N / TIM12_CH1 / OTG_HS_DM USART3_RTS/ TIM8_CH2N | |
| 36 | G1 | 54 | 76 | 95 | R15 | PB15 | I/O | FT | PB15 | SPI2_MOSI / I2S2_SD / TIM1_CH3N / TIM8_CH3N / TIM12_CH2 / OTG_HS_DP | |
| - | - | 55 | 77 | 96 | P15 | PD8 | I/O | FT | PD8 | FSMC_D13 / USART3_TX | |
| - | - | 56 | 78 | 97 | P14 | PD9 | I/O | FT | PD9 | FSMC_D14 / USART3_RX | |
| - | - | 57 | 79 | 98 | N15 | PD10 | I/O | FT | PD10 | FSMC_D15 / USART3_CK | |
| - | - | 58 | 80 | 99 | N14 | PD11 | I/O | FT | PD11 | FSMC_A16/USART3_CTS | |
| - | - | 59 | 81 | 100 | N13 | PD12 | I/O | FT | PD12 | FSMC_A17/TIM4_CH1 / USART3_RTS | |
| - | - | 60 | 82 | 101 | M15 | PD13 | I/O | FT | PD13 | FSMC_A18/TIM4_CH2 | |
| - | - | - | 83 | 102 | - | V _{SS_8} | S | | V _{SS_8} | | |
| - | - | - | 84 | 103 | J13 | V _{DD_8} | S | | V _{DD_8} | | |

Table 5. STM32F21x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|-------------------|---------------------|--------------------------|---|--|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| - | - | 61 | 85 | 104 | M14 | PD14 | I/O | FT | PD14 | FSMC_D0/TIM4_CH3 | |
| - | - | 62 | 86 | 105 | L14 | PD15 | I/O | FT | PD15 | FSMC_D1/TIM4_CH4 | |
| - | - | - | 87 | 106 | L15 | PG2 | I/O | FT | PG2 | FSMC_A12 | |
| - | - | - | 88 | 107 | K15 | PG3 | I/O | FT | PG3 | FSMC_A13 | |
| - | - | - | 89 | 108 | K14 | PG4 | I/O | FT | PG4 | FSMC_A14 | |
| - | - | - | 90 | 109 | K13 | PG5 | I/O | FT | PG5 | FSMC_A15 | |
| - | - | - | 91 | 110 | J15 | PG6 | I/O | FT | PG6 | FSMC_INT2 | |
| - | - | - | 92 | 111 | J14 | PG7 | I/O | FT | PG7 | FSMC_INT3 /USART6_CK | |
| - | - | - | 93 | 112 | H14 | PG8 | I/O | FT | PG8 | USART6_RTS / ETH_PPS_OUT | |
| - | - | - | 94 | 113 | G12 | V _{SS_9} | S | | V _{SS_9} | | |
| - | - | - | 95 | 114 | H13 | V _{DD_9} | S | | V _{DD_9} | | |
| 37 | G2 | 63 | 96 | 115 | H15 | PC6 | I/O | FT | PC6 | SPI2_MCK / TIM8_CH1/SDIO_D6 / USART6_TX / DCMI_D0/TIM3_CH1 | |
| 38 | F2 | 64 | 97 | 116 | G15 | PC7 | I/O | FT | PC7 | SPI3_MCK / TIM8_CH2/SDIO_D7 / USART6_RX / DCMI_D1/TIM3_CH2 | |
| 39 | F3 | 65 | 98 | 117 | G14 | PC8 | I/O | FT | PC8 | TIM8_CH3/SDIO_D0 /TIM3_CH3/USART6_CK / DCMI_D2 | |
| 40 | D1 | 66 | 99 | 118 | F14 | PC9 | I/O | FT | PC9 | I2S2_CKIN/ I2S3_CKIN/ MCO2 / TIM8_CH4/SDIO_D1 / /I2C3_SDA / DCMI_D3 / TIM3_CH4 | |
| 41 | E2 | 67 | 100 | 119 | F15 | PA8 | I/O | FT | PA8 | MCO1 / USART1_CK/ TIM1_CH1/ I2C3_SCL/ OTG_FS_SOF | |
| 42 | E3 | 68 | 101 | 120 | E15 | PA9 | I/O | FT | PA9 | USART1_TX/ TIM1_CH2 / I2C3_SMBA / DCMI_D0 | OTG_FS_ VBUS |
| 43 | D3 | 69 | 102 | 121 | D15 | PA10 | I/O | FT | PA10 | USART1_RX/ TIM1_CH3/ OTG_FS_ID/DCMI_D1 | |
| 44 | D2 | 70 | 103 | 122 | C15 | PA11 | I/O | FT | PA11 | USART1_CTS /CAN1_RX / TIM1_CH4 / OTG_FS_DM | |

Table 5. STM32F21x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|--------------------|---------------------|--------------------------|---|--|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| 45 | C1 | 71 | 104 | 123 | B15 | PA12 | I/O | FT | PA12 | USART1_RTS / CAN1_TX / TIM1_ETR / OTG_FS_DP | |
| 46 | B2 | 72 | 105 | 124 | A15 | PA13 | I/O | FT | JTMS-SWDIO | JTMS-SWDIO | |
| 47 | C2 | 73 | 106 | 125 | F13 | V _{CAP_2} | S | | V _{CAP_2} | | |
| - | B1 | 74 | 107 | 126 | F12 | V _{SS_2} | S | | V _{SS_2} | | |
| 48 | A8 | 75 | 108 | 127 | G13 | V _{DD_2} | S | | V _{DD_2} | | |
| - | - | - | - | 128 | E12 | PH13 | I/O | FT | PH13 | TIM8_CH1N / CAN1_TX | |
| - | - | - | - | 129 | E13 | PH14 | I/O | FT | PH14 | TIM8_CH2N / DCMI_D4 | |
| - | - | - | - | 130 | D13 | PH15 | I/O | FT | PH15 | TIM8_CH3N / DCMI_D11 | |
| - | - | - | - | 131 | E14 | PI0 | I/O | FT | PI0 | TIM5_CH4 / SPI2_NSS / I2S2_WS / DCMI_D13 | |
| - | - | - | - | 132 | D14 | PI1 | I/O | FT | PI1 | SPI2_SCK / I2S2_CK / DCMI_D8 | |
| - | - | - | - | 133 | C14 | PI2 | I/O | FT | PI2 | TIM8_CH4 / SPI2_MISO / DCMI_D9 | |
| - | - | - | - | 134 | C13 | PI3 | I/O | FT | PI3 | TIM8_ETR / SPI2_MOSI / I2S2_SD / DCMI_D10 | |
| - | - | - | - | 135 | D9 | V _{SS_15} | S | | V _{SS_15} | | |
| - | - | - | - | 136 | C9 | V _{DD_15} | S | | V _{DD_15} | | |
| 49 | A1 | 76 | 109 | 137 | A14 | PA14 | I/O | FT | JTCK-SWCLK | JTCK-SWCLK | |
| 50 | A2 | 77 | 110 | 138 | A13 | | I/O | FT | JTDI | JTDI / SPI3_NSS / I2S3_WS / TIM2_CH1_ETR / SPI1_NSS | |
| 51 | B3 | 78 | 111 | 139 | B14 | PC10 | I/O | FT | PC10 | SPI3_SCK / I2S3_CK / UART4_TX / SDIO_D2 / DCMI_D8 / USART3_TX | |
| 52 | C3 | 79 | 112 | 140 | B13 | PC11 | I/O | FT | PC11 | UART4_RX / SPI3_MISO / SDIO_D3 / DCMI_D4 / USART3_RX | |
| 53 | A3 | 80 | 113 | 141 | A12 | PC12 | I/O | FT | PC12 | UART5_TX / SDIO_CK / DCMI_D9 / SPI3_MOSI / I2S3_SD / USART3_CK | |
| - | - | 81 | 114 | 142 | B12 | PD0 | I/O | FT | PD0 | FSMC_D2 / CAN1_RX | |
| - | - | 82 | 115 | 143 | C12 | PD1 | I/O | FT | PD1 | FSMC_D3 / CAN1_TX | |

Table 5. STM32F21x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|--------------------|---------------------|--------------------------|---|--|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| 54 | C7 | 83 | 116 | 144 | D12 | PD2 | I/O | FT | PD2 | TIM3_ETR/UART5_RX SDIO_CMD / DCMI_D11 | |
| - | - | 84 | 117 | 145 | D11 | PD3 | I/O | FT | PD3 | FSMC_CLK/USART2_CTS | |
| - | - | 85 | 118 | 146 | D10 | PD4 | I/O | FT | PD4 | FSMC_NOE/USART2_RTS | |
| - | - | 86 | 119 | 147 | C11 | PD5 | I/O | FT | PD5 | FSMC_NWE/USART2_TX | |
| - | - | - | 120 | 148 | D8 | V _{SS_10} | S | | V _{SS_10} | | |
| - | - | - | 121 | 149 | C8 | V _{DD_10} | S | | V _{DD_10} | | |
| - | - | 87 | 122 | 150 | B11 | PD6 | I/O | FT | PD6 | FSMC_NWAIT/USART2_RX | |
| - | - | 88 | 123 | 151 | A11 | PD7 | I/O | FT | PD7 | USART2_CK/FSMC_NE1/ FSMC_NCE2 | |
| - | - | - | 124 | 152 | C10 | PG9 | I/O | FT | PG9 | USART6_RX / FSMC_NE2/FSMC_NCE3 | |
| - | - | - | 125 | 153 | B10 | PG10 | I/O | FT | PG10 | FSMC_NCE4_1/ FSMC_NE3 | |
| - | - | - | 126 | 154 | B9 | PG11 | I/O | FT | PG11 | FSMC_NCE4_2 / ETH_MII_TX_EN | |
| - | - | - | 127 | 155 | B8 | PG12 | I/O | FT | PG12 | FSMC_NE4 / USART6_RTS | |
| - | - | - | 128 | 156 | A8 | PG13 | I/O | FT | PG13 | FSMC_A24 / USART6_CTS /ETH_MII_TXD0/ETH_RMII _TXD0 | |
| - | - | - | 129 | 157 | A7 | PG14 | I/O | FT | PG14 | FSMC_A25 / USART6_TX /ETH_MII_TXD1/ETH_RMII _TXD1 | |
| - | - | - | 130 | 158 | D7 | V _{SS_11} | S | | V _{SS_11} | | |
| - | - | - | 131 | 159 | C7 | V _{DD_11} | S | | V _{DD_11} | | |
| - | - | - | 132 | 160 | B7 | PG15 | I/O | FT | PG15 | USART6_CTS / DCMI_D13 | |
| 55 | A4 | 89 | 133 | 161 | A10 | PB3 | I/O | FT | JTDO/ TRACESWO | JTDO/ TRACESWO/ SPI3_SCK / I2S3_CK / TIM2_CH2 / SPI1_SCK | |
| 56 | B4 | 90 | 134 | 162 | A9 | PB4 | I/O | FT | NJTRST | NJTRST/ SPI3_MISO / TIM3_CH1 / SPI1_MISO | |

Table 5. STM32F21x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|--------------------|---------------------|--------------------------|---|--|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| 57 | A5 | 91 | 135 | 163 | A6 | PB5 | I/O | FT | PB5 | I2C1_SMBA/ CAN2_RX / OTG_HS_ULPI_D7 / ETH_PPS_OUT/TIM3_CH2 / SPI1_MOSI/ SPI3_MOSI / DCMI_D10 / I2S3_SD | |
| 58 | B5 | 92 | 136 | 164 | B6 | PB6 | I/O | FT | PB6 | I2C1_SCL/ TIM4_CH1 / CAN2_TX /OTG_FS_INTN / DCMI_D5/USART1_TX | |
| 59 | A6 | 93 | 137 | 165 | B5 | PB7 | I/O | FT | PB7 | I2C1_SDA / FSMC_NL ⁽⁸⁾ / DCMI_VSYNC / USART1_RX/ TIM4_CH2 | |
| 60 | B6 | 94 | 138 | 166 | D6 | BOOT0 | I | | BOOT0 | | V _{PP} |
| 61 | B7 | 95 | 139 | 167 | A5 | PB8 | I/O | FT | PB8 | TIM4_CH3/SDIO_D4/ TIM10_CH1 / DCMI_D6 / OTG_FS_SCL/ ETH_MII_TXD3 / I2C1_SCL/ CAN1_RX | |
| 62 | A7 | 96 | 140 | 168 | B4 | PB9 | I/O | FT | PB9 | SPI2_NSS/ I2S2_WS/ TIM4_CH4/ TIM11_CH1/ OTG_FS_SDA/ SDIO_D5 / DCMI_D7 / I2C1_SDA / CAN1_TX | |
| - | - | 97 | 141 | 169 | A4 | PE0 | I/O | FT | PE0 | TIM4_ETR / FSMC_NBL0 / DCMI_D2 | |
| - | - | 98 | 142 | 170 | A3 | PE1 | I/O | FT | PE1 | FSMC_NBL1 / DCMI_D3 | |
| | | | | | D5 | V _{SS} | S | | V _{SS} | | |
| 63 | D8 | - | - | - | - | V _{SS_3} | S | | V _{SS_3} | | |
| - | - | 99 | 143 | 171 | C6 | RFU ⁽⁹⁾ | | | | | |
| 64 | D9 | 100 | 144 | 172 | C5 | V _{DD_3} | S | | V _{DD_3} | | |
| - | - | - | - | 173 | D4 | PI4 | I/O | FT | PI4 | TIM8_BKIN / DCMI_D5 | |
| - | - | - | - | 174 | C4 | PI5 | I/O | FT | PI5 | TIM8_CH1 / DCMI_VSYNC | |
| - | - | - | - | 175 | C3 | PI6 | I/O | FT | PI6 | TIM8_CH2 / DCMI_D6 | |
| - | - | - | - | 176 | C2 | PI7 | I/O | FT | PI7 | TIM8_CH3 / DCMI_D7 | |
| - | C8 | - | - | - | - | IRROFF | I/O | | IRROFF | | |

1. I = input, O = output, S = supply, HiZ = high impedance.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.

4. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
5. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F20x and STM32F21x reference manual, available from the STMicroelectronics website: www.st.com.
6. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
7. If the device is delivered in an UFBGA176 package and if the REGOFF pin is set to V_{DD} (Regulator in bypass mode), then PA0 is used as an internal Reset (active low).
8. FSMC_NL pin is also named FSMC_NADV on memory devices.
9. RFU = reserved for future use.



Table 6. Alternate function mapping

| Port | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF014 | AF15 |
|----------|-------------------|----------------------|----------|--------------|----------------|---------------------|----------------------|------------|--------------------|---------------------------|----------------|------------------------------------|----------------------|------------|-------|----------|
| | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/I2C2/I2C3 | SPI1/SPI2/I2S2 | SPI3/I2S3 | USART1/2/3 | UART4/5/ USART6 | CAN1/CAN2/ TIM12/13/14 | OTG_FS/ OTG_HS | ETH | FSMC/SDIO/ OTG_FS | DCMI | | |
| PA0-WKUP | | TIM2_CH1 TIM2_ETR | TIM5_CH1 | TIM8_ETR | | | | USART2_CTS | UART4_TX | | | ETH_MII_CRS | | | | EVENTOUT |
| PA1 | | TIM2_CH2 | TIM5_CH2 | | | | | USART2_RTS | UART4_RX | | | ETH_MII_RX_CLK ETH_RMII_REF_CLK | | | | EVENTOUT |
| PA2 | | TIM2_CH3 | TIM5_CH3 | TIM9_CH1 | | | | USART2_TX | | | | ETH_MDIO | | | | EVENTOUT |
| PA3 | | TIM2_CH4 | TIM5_CH4 | TIM9_CH2 | | | | USART2_RX | | | OTG_HS_ULPI_D0 | ETH_MII_COL | | | | EVENTOUT |
| PA4 | | | | | | SPI1_NSS | SPI3_NSS I2S3_WS | USART2_CK | | | | | OTG_HS_SOF | DCMI_HSYNC | | EVENTOUT |
| PA5 | | TIM2_CH1 TIM2_ETR | | TIM8_CH1N | | SPI1_SCK | | | | | OTG_HS_ULPI_CK | | | | | EVENTOUT |
| PA6 | | TIM1_BKIN | TIM3_CH1 | TIM8_BKIN | | SPI1_MISO | | | | TIM13_CH1 | | | | DCMI_PIXCK | | EVENTOUT |
| PA7 | | TIM1_CH1N | TIM3_CH2 | TIM8_CH1N | | SPI1_MOSI | | | | TIM14_CH1 | | ETH_MII_RX_DV ETH_RMII_CRS_DV | | | | EVENTOUT |
| PA8 | MCO1 | TIM1_CH1 | | | I2C3_SCL | | | USART1_CK | | | OTG_FS_SOF | | | | | EVENTOUT |
| PA9 | | TIM1_CH2 | | | I2C3_SMBA | | | USART1_TX | | | | | | DCMI_D0 | | EVENTOUT |
| PA10 | | TIM1_CH3 | | | | | | USART1_RX | | | OTG_FS_ID | | | DCMI_D1 | | EVENTOUT |
| PA11 | | TIM1_CH4 | | | | | | USART1_CTS | | CAN1_RX | OTG_FS_DM | | | | | EVENTOUT |
| PA12 | | TIM1_ETR | | | | | | USART1_RTS | | CAN1_TX | OTG_FS_DP | | | | | EVENTOUT |
| PA13 | JTMS-SWDIO | | | | | | | | | | | | | | | EVENTOUT |
| PA14 | JTCK-SWCLK | | | | | | | | | | | | | | | EVENTOUT |
| PA15 | JTDI | TIM2_CH1 TIM2_ETR | | | | SPI1_NSS | SPI3_NSS I2S3_WS | | | | | | | | | EVENTOUT |
| PB0 | | TIM1_CH2N | TIM3_CH3 | TIM8_CH2N | | | | | | | OTG_HS_ULPI_D1 | ETH_MII_RXD2 | | | | EVENTOUT |
| PB1 | | TIM1_CH3N | TIM3_CH4 | TIM8_CH3N | | | | | | | OTG_HS_ULPI_D2 | ETH_MII_RXD3 | OTG_HS_INTN | | | EVENTOUT |
| PB2 | | | | | | | | | | | | | | | | EVENTOUT |
| PB3 | JTDO/ TRACESWO | TIM2_CH2 | | | | SPI1_SCK | SPI3_SCK I2S3_CK | | | | | | | | | EVENTOUT |
| PB4 | JTRST | | TIM3_CH1 | | | SPI1_MISO | SPI3_MISO | | | | | | | | | EVENTOUT |
| PB5 | | | TIM3_CH2 | | I2C1_SMBA | SPI1_MOSI | SPI3_MOSI I2S3_SD | | | CAN2_RX | OTG_HS_ULPI_D7 | ETH_PPS_OUT | | DCMI_D10 | | EVENTOUT |
| PB6 | | | TIM4_CH1 | | I2C1_SCL | | | USART1_TX | | CAN2_TX | OTG_FS_INTN | | | DCMI_D5 | | EVENTOUT |
| PB7 | | | TIM4_CH2 | | I2C1_SDA | | | USART1_RX | | | | | FSMC_NL | DCMI_VSYNC | | EVENTOUT |
| PB8 | | | TIM4_CH3 | TIM10_CH1 | I2C1_SCL | | | | | CAN1_RX | OTG_FS_SCL | ETH_MII_TXD3 | SDIO_D4 | DCMI_D6 | | EVENTOUT |
| PB9 | | | TIM4_CH4 | TIM11_CH1 | I2C1_SDA | SPI2_NSS I2S2_WS | | | | CAN1_TX | OTG_FS_SDA | | SDIO_D5 | DCMI_D7 | | EVENTOUT |
| PB10 | | TIM2_CH3 | | | I2C2_SCL | SPI2_SCK I2S2_CK | | USART3_TX | | | OTG_HS_ULPI_D3 | ETH_MII_RX_ER | OTG_HS_SCL | | | EVENTOUT |
| PB11 | | TIM2_CH4 | | | I2C2_SDA | | | USART3_RX | | | OTG_HS_ULPI_D4 | ETH_MII_TX_EN ETH_RMII_TX_EN | OTG_HS_SDA | | | EVENTOUT |
| PB12 | | TIM1_BKIN | | | I2C2_SMBA | SPI2_NSS I2S2_WS | | USART3_CK | | CAN2_RX | OTG_HS_ULPI_D5 | ETH_MII_TXD0 ETH_RMII_TXD0 | OTG_HS_ID | | | EVENTOUT |
| PB13 | | TIM1_CH1N | | | | SPI2_SCK I2S2_CK | | USART3_CTS | | CAN2_TX | OTG_HS_ULPI_D6 | ETH_MII_TXD1 ETH_RMII_TXD1 | | | | EVENTOUT |
| PB14 | | TIM1_CH2N | | TIM8_CH2N | | SPI2_MISO | | USART3_RTS | | TIM12_CH1 | | | OTG_HS_DM | | | EVENTOUT |


Table 6. Alternate function mapping (continued)

| Port | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF014 | AF15 |
|----------------|----------|-----------|----------|--------------|----------------|----------------------|----------------------|------------|--------------------|---------------------------|-----------------|-----------------------------------|----------------------|----------|-------|----------|
| | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/I2C2/I2C3 | SPI1/SPI2/I2S2 | SPI3/I2S3 | USART1/2/3 | UART4/5/ USART6 | CAN1/CAN2/ TIM12/13/14 | OTG_FS/ OTG_HS | ETH | FSMC/SDIO/ OTG_FS | DCMI | | |
| PB15 | RTC_50Hz | TIM1_CH3N | | TIM8_CH3N | | SPI2_MOSI I2S2_SD | | | | TIM12_CH2 | | | OTG_HS_DP | | | EVENTOUT |
| PC0 | | | | | | | | | | | OTG_HS_ULPI_STP | | | | | EVENTOUT |
| PC1 | | | | | | | | | | | | ETH_MDC | | | | EVENTOUT |
| PC2 | | | | | | SPI2_MISO | | | | | OTG_HS_ULPI_DIR | ETH_MII_TXD2 | | | | EVENTOUT |
| PC3 | | | | | | SPI2_MOSI | | | | | OTG_HS_ULPI_NXT | ETH_MII_TX_CLK ETH_RMII_TX_CLK | | | | EVENTOUT |
| PC4 | | | | | | | | | | | | ETH_MII_RXD0 ETH_RMII_RXD0 | | | | EVENTOUT |
| PC5 | | | | | | | | | | | | ETH_MII_RXD1 ETH_RMII_RXD1 | | | | EVENTOUT |
| PC6 | | | TIM3_CH1 | TIM8_CH1 | | I2S2_MCK | | | USART6_TX | | | | SDIO_D6 | DCMI_D0 | | EVENTOUT |
| PC7 | | | TIM3_CH2 | TIM8_CH2 | | | I2S3_SCK | | USART6_RX | | | | SDIO_D7 | DCMI_D1 | | EVENTOUT |
| PC8 | | | TIM3_CH3 | TIM8_CH3 | | | | | USART6_CK | | | | SDIO_D0 | DCMI_D2 | | EVENTOUT |
| PC9 | MCO2 | | TIM3_CH4 | TIM8_CH4 | I2C3_SDA | I2S2_CKIN | I2S3_CKIN | | | | | | SDIO_D1 | DCMI_D3 | | EVENTOUT |
| PC10 | | | | | | | SPI3_SCK I2S3_CK | USART3_TX | UART4_TX | | | | SDIO_D2 | DCMI_D8 | | EVENTOUT |
| PC11 | | | | | | | SPI3_MISO | USART3_RX | UART4_RX | | | | SDIO_D3 | DCMI_D4 | | EVENTOUT |
| PC12 | | | | | | | SPI3_MOSI I2S3_SD | USART3_CK | UART5_TX | | | | SDIO_CK | DCMI_D9 | | EVENTOUT |
| PC13 | | | | | | | | | | | | | | | | |
| PC14-OSC32_IN | | | | | | | | | | | | | | | | |
| PC15-OSC32_OUT | | | | | | | | | | | | | | | | |
| PD0 | | | | | | | | | | CAN1_RX | | | FSMC_D2 | | | EVENTOUT |
| PD1 | | | | | | | | | | CAN1_TX | | | FSMC_D3 | | | EVENTOUT |
| PD2 | | | TIM3_ETR | | | | | | UART5_RX | | | | SDIO_CMD | DCMI_D11 | | EVENTOUT |
| PD3 | | | | | | | | USART2_CTS | | | | | FSMC_CLK | | | EVENTOUT |
| PD4 | | | | | | | | USART2_RTS | | | | | FSMC_NOE | | | EVENTOUT |
| PD5 | | | | | | | | USART2_TX | | | | | FSMC_NWE | | | EVENTOUT |
| PD6 | | | | | | | | USART2_RX | | | | | FSMC_NWAIT | | | EVENTOUT |
| PD7 | | | | | | | | USART2_CK | | | | | FSMC_NE1 | | | EVENTOUT |
| PD8 | | | | | | | | USART3_TX | | | | | FSMC_D13 | | | EVENTOUT |
| PD9 | | | | | | | | USART3_RX | | | | | FSMC_D14 | | | EVENTOUT |
| PD10 | | | | | | | | USART3_CK | | | | | FSMC_D15 | | | EVENTOUT |
| PD11 | | | | | | | | USART3_CTS | | | | | FSMC_A16 | | | EVENTOUT |
| PD12 | | | TIM4_CH1 | | | | | USART3_RTS | | | | | FSMC_A17 | | | EVENTOUT |
| PD13 | | | TIM4_CH2 | | | | | | | | | | FSMC_A18 | | | EVENTOUT |
| PD14 | | | TIM4_CH3 | | | | | | | | | | FSMC_D0 | | | EVENTOUT |



Table 6. Alternate function mapping (continued)

| Port | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF014 | AF15 |
|------|----------|-----------|----------|--------------|----------------|----------------|-----------|------------|--------------------|---------------------------|----------------|--------------|----------------------|----------|-------|----------|
| | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/I2C2/I2C3 | SPI1/SPI2/I2S2 | SPI3/I2S3 | USART1/2/3 | UART4/5/ USART6 | CAN1/CAN2/ TIM12/13/14 | OTG_FS/ OTG_HS | ETH | FSMC/SDIO/ OTG_FS | DCMI | | |
| PD15 | | | TIM4_CH4 | | | | | | | | | | FSMC_D1 | | | EVENTOUT |
| PE0 | | | TIM4_ETR | | | | | | | | | | FSMC_NBL0 | DCMI_D2 | | EVENTOUT |
| PE1 | | | | | | | | | | | | | FSMC_BLN1 | DCMI_D3 | | EVENTOUT |
| PE2 | TRACECLK | | | | | | | | | | | ETH_MII_TXD3 | FSMC_A23 | | | EVENTOUT |
| PE3 | TRACED0 | | | | | | | | | | | | FSMC_A19 | | | EVENTOUT |
| PE4 | TRACED1 | | | | | | | | | | | | FSMC_A20 | DCMI_D4 | | EVENTOUT |
| PE5 | TRACED2 | | | TIM9_CH1 | | | | | | | | | FSMC_A21 | DCMI_D6 | | EVENTOUT |
| PE6 | TRACED3 | | | TIM9_CH2 | | | | | | | | | FSMC_A22 | DCMI_D7 | | EVENTOUT |
| PE7 | | TIM1_ETR | | | | | | | | | | | FSMC_D4 | | | EVENTOUT |
| PE8 | | TIM1_CH1N | | | | | | | | | | | FSMC_D5 | | | EVENTOUT |
| PE9 | | TIM1_CH1 | | | | | | | | | | | FSMC_D6 | | | EVENTOUT |
| PE10 | | TIM1_CH2N | | | | | | | | | | | FSMC_D7 | | | EVENTOUT |
| PE11 | | TIM1_CH2 | | | | | | | | | | | FSMC_D8 | | | EVENTOUT |
| PE12 | | TIM1_CH3N | | | | | | | | | | | FSMC_D9 | | | EVENTOUT |
| PE13 | | TIM1_CH3 | | | | | | | | | | | FSMC_D10 | | | EVENTOUT |
| PE14 | | TIM1_CH4 | | | | | | | | | | | FSMC_D11 | | | EVENTOUT |
| PE15 | | TIM1_BKIN | | | | | | | | | | | FSMC_D12 | | | EVENTOUT |
| PF0 | | | | | I2C2_SDA | | | | | | | | FSMC_A0 | | | EVENTOUT |
| PF1 | | | | | I2C2_SCL | | | | | | | | FSMC_A1 | | | EVENTOUT |
| PF2 | | | | | I2C2_SMBA | | | | | | | | FSMC_A2 | | | EVENTOUT |
| PF3 | | | | | | | | | | | | | FSMC_A3 | | | EVENTOUT |
| PF4 | | | | | | | | | | | | | FSMC_A4 | | | EVENTOUT |
| PF5 | | | | | | | | | | | | | FSMC_A5 | | | EVENTOUT |
| PF6 | | | | TIM10_CH1 | | | | | | | | | FSMC_NIORD | | | EVENTOUT |
| PF7 | | | | TIM11_CH1 | | | | | | | | | FSMC_NREG | | | EVENTOUT |
| PF8 | | | | | | | | | | TIM13_CH1 | | | FSMC_NIOWR | | | EVENTOUT |
| PF9 | | | | | | | | | | TIM14_CH1 | | | FSMC_CD | | | EVENTOUT |
| PF10 | | | | | | | | | | | | | FSMC_INTR | | | EVENTOUT |
| PF11 | | | | | | | | | | | | | | DCMI_D12 | | EVENTOUT |
| PF12 | | | | | | | | | | | | | FSMC_A6 | | | EVENTOUT |
| PF13 | | | | | | | | | | | | | FSMC_A7 | | | EVENTOUT |
| PF14 | | | | | | | | | | | | | FSMC_A8 | | | EVENTOUT |
| PF15 | | | | | | | | | | | | | FSMC_A9 | | | EVENTOUT |



Table 6. Alternate function mapping (continued)

| Port | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF014 | AF15 |
|---------------|-----|--------|------------------|--------------|----------------|----------------|-----------|------------|--------------------|---------------------------|-----------------|---------------------------------|----------------------|------------|-------|----------|
| | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/I2C2/I2C3 | SPI1/SPI2/I2S2 | SPI3/I2S3 | USART1/2/3 | UART4/5/ USART6 | CAN1/CAN2/ TIM12/13/14 | OTG_FS/ OTG_HS | ETH | FSMC/SDIO/ OTG_FS | DCMI | | |
| PG0 | | | | | | | | | | | | | FSMC_A10 | | | EVENTOUT |
| PG1 | | | | | | | | | | | | | FSMC_A11 | | | EVENTOUT |
| PG2 | | | | | | | | | | | | | FSMC_A12 | | | EVENTOUT |
| PG3 | | | | | | | | | | | | | FSMC_A13 | | | EVENTOUT |
| PG4 | | | | | | | | | | | | | FSMC_A14 | | | EVENTOUT |
| PG5 | | | | | | | | | | | | | FSMC_A15 | | | EVENTOUT |
| PG6 | | | | | | | | | | | | | FSMC_INT2 | | | EVENTOUT |
| PG7 | | | | | | | | | USART6_CK | | | | FSMC_INT3 | | | EVENTOUT |
| PG8 | | | | | | | | | USART6_RTS | | | ETH_PPS_OUT | | | | EVENTOUT |
| PG9 | | | | | | | | | USART6_RX | | | | FSMC_NE2 | | | EVENTOUT |
| PG10 | | | | | | | | | | | | | FSMC_NCE4_1 | | | EVENTOUT |
| PG11 | | | | | | | | | | | | ETH_MII_TX_EN ETH_RMII_TX_EN | FSMC_NCE4_2 | | | EVENTOUT |
| PG12 | | | | | | | | | USART6_RTS | | | | FSMC_NE4 | | | EVENTOUT |
| PG13 | | | | | | | | | UART6_CTS | | | ETH_MII_TXD0 ETH_RMII_TXD0 | FSMC_A24 | | | EVENTOUT |
| PG14 | | | | | | | | | USART6_TX | | | ETH_MII_TXD1 ETH_RMII_TXD1 | FSMC_A25 | | | EVENTOUT |
| PG15 | | | | | | | | | USART6_CTS | | | | | DCMI_D13 | | EVENTOUT |
| PH0 - OSC_IN | | | | | | | | | | | | | | | | |
| PH1 - OSC_OUT | | | | | | | | | | | | | | | | |
| PH2 | | | | | | | | | | | | ETH_MII_CRS | | | | EVENTOUT |
| PH3 | | | | | | | | | | | | ETH_MII_COL | | | | EVENTOUT |
| PH4 | | | | | I2C2_SCL | | | | | | OTG_HS_ULPI_NXT | | | | | EVENTOUT |
| PH5 | | | | | I2C2_SDA | | | | | | | | | | | EVENTOUT |
| PH6 | | | | | I2C2_SMBA | | | | | TIM12_CH1 | | ETH_MII_RXD2 | | | | EVENTOUT |
| PH7 | | | | | I2C3_SCL | | | | | | | ETH_MII_RXD3 | | | | EVENTOUT |
| PH8 | | | | | I2C3_SDA | | | | | | | | | DCMI_HSYNC | | EVENTOUT |
| PH9 | | | | | I2C3_SMBA | | | | | TIM12_CH2 | | | | DCMI_D0 | | EVENTOUT |
| PH10 | | | TIM5_CH1TIM5_ETR | | | | | | | | | | | DCMI_D1 | | EVENTOUT |
| PH11 | | | TIM5_CH2 | | | | | | | | | | | DCMI_D2 | | EVENTOUT |
| PH12 | | | TIM5_CH3 | | | | | | | | | | | DCMI_D3 | | EVENTOUT |
| PH13 | | | | TIM8_CH1N | | | | | | CAN1_TX | | | | | | EVENTOUT |
| PH14 | | | | TIM8_CH2N | | | | | | | | | | DCMI_D4 | | EVENTOUT |
| PH15 | | | | TIM8_CH3N | | | | | | | | | | DCMI_D11 | | EVENTOUT |



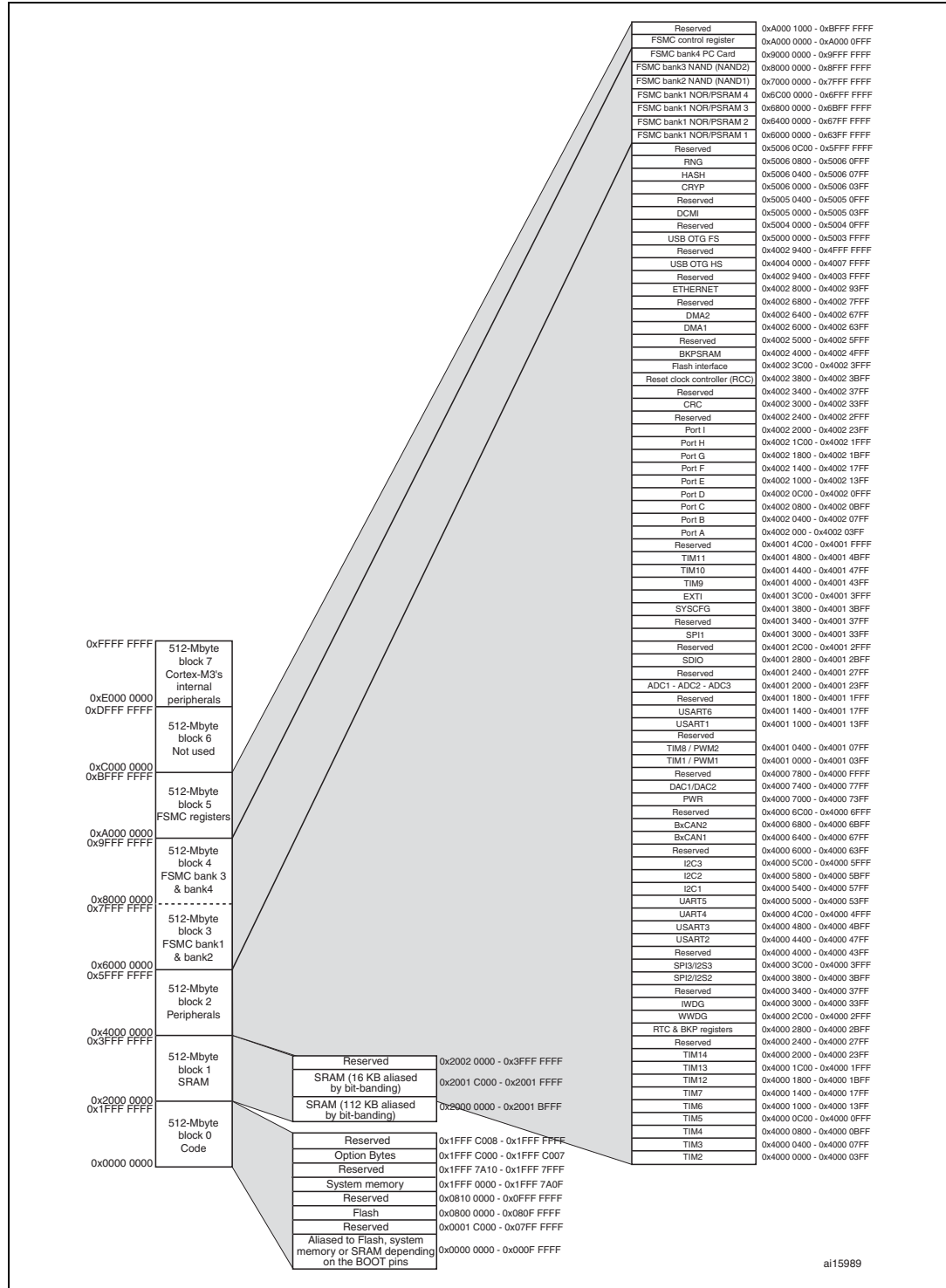
Table 6. Alternate function mapping (continued)

| Port | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF014 | AF15 |
|------|-----|--------|----------|--------------|----------------|----------------------|-----------|------------|--------------------|---------------------------|-----------------|---------------|----------------------|------------|-------|----------|
| | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/I2C2/I2C3 | SPI1/SPI2/I2S2 | SPI3/I2S3 | USART1/2/3 | UART4/5/ USART6 | CAN1/CAN2/ TIM12/13/14 | OTG_FS/ OTG_HS | ETH | FSMC/SDIO/ OTG_FS | DCMI | | |
| PI0 | | | TIM5_CH4 | | | SPI2_NSS I2S2_WS | | | | | | | | DCMI_D13 | | EVENTOUT |
| PI1 | | | | | | SPI2_SCK I2S2_CK | | | | | | | | DCMI_D8 | | EVENTOUT |
| PI2 | | | | TIM8_CH4 | | SPI2_MISO | | | | | | | | DCMI_D9 | | EVENTOUT |
| PI3 | | | | TIM8_ETR | | SPI2_MOSI I2S2_SD | | | | | | | | DCMI_D10 | | EVENTOUT |
| PI4 | | | | TIM8_BKIN | | | | | | | | | | DCMI_D5 | | EVENTOUT |
| PI5 | | | | TIM8_CH1 | | | | | | | | | | DCMI_VSYNC | | EVENTOUT |
| PI6 | | | | TIM8_CH2 | | | | | | | | | | DCMI_D6 | | EVENTOUT |
| PI7 | | | | TIM8_CH3 | | | | | | | | | | DCMI_D7 | | EVENTOUT |
| PI8 | | | | | | | | | | | | | | | | |
| PI9 | | | | | | | | | | CAN1_RX | | | | | | EVENTOUT |
| PI10 | | | | | | | | | | | | ETH_MII_RX_ER | | | | EVENTOUT |
| PI11 | | | | | | | | | | | OTG_HS_ULPI_DIR | | | | | EVENTOUT |

4 Memory mapping

The memory map is shown in [Figure 15](#).

Figure 15. Memory map



5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ °C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean} \pm 3\sigma$).

5.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ °C}$, $V_{DD} = 3.3\text{ V}$ (for the $1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ($\text{mean} \pm 2\sigma$).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 16](#).

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 17](#).

Figure 16. Pin loading conditions

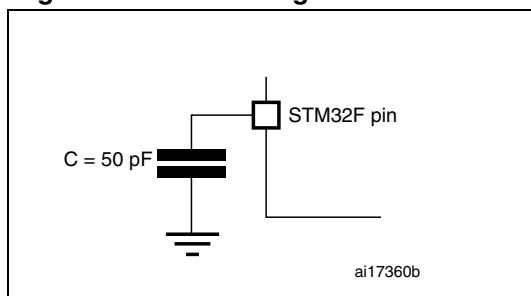
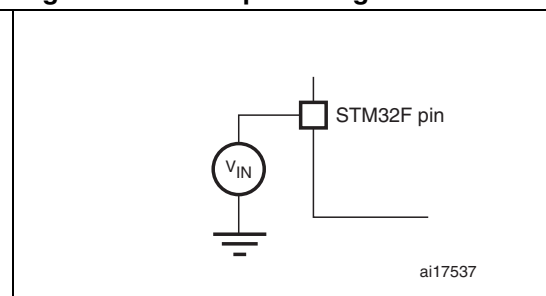
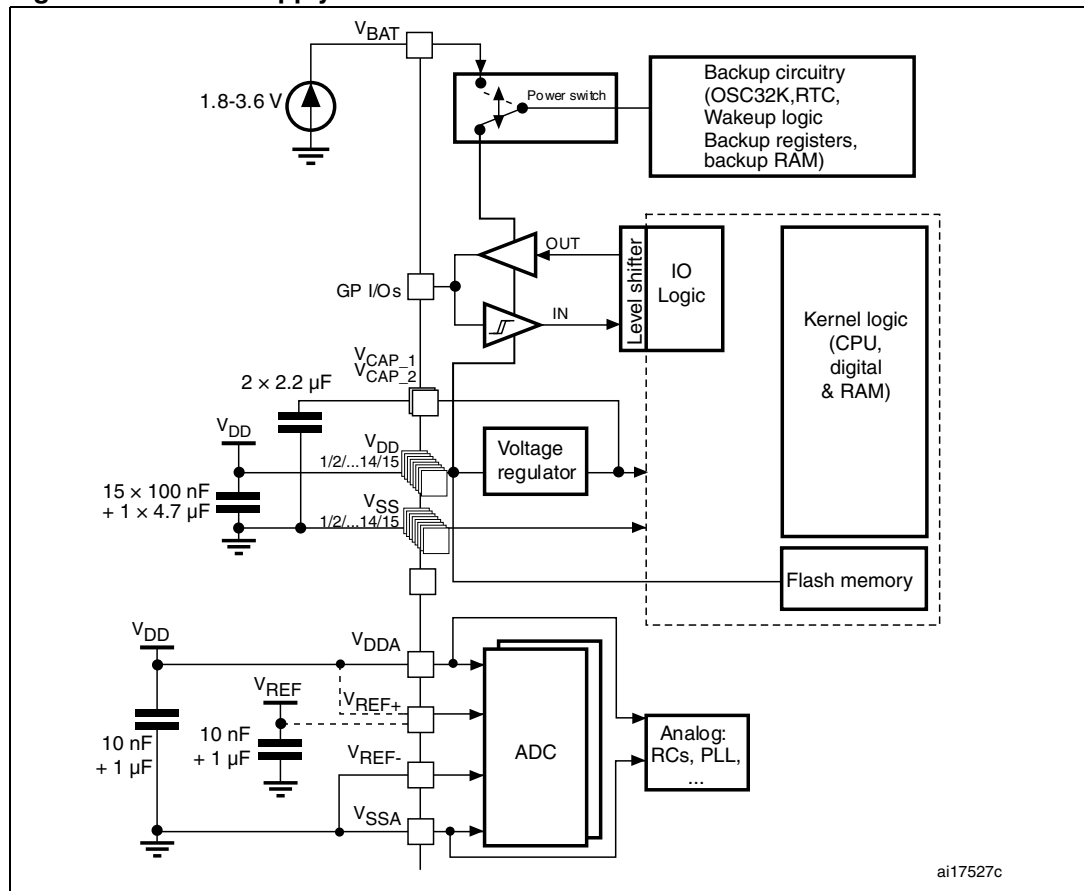


Figure 17. Pin input voltage



5.1.6 Power supply scheme

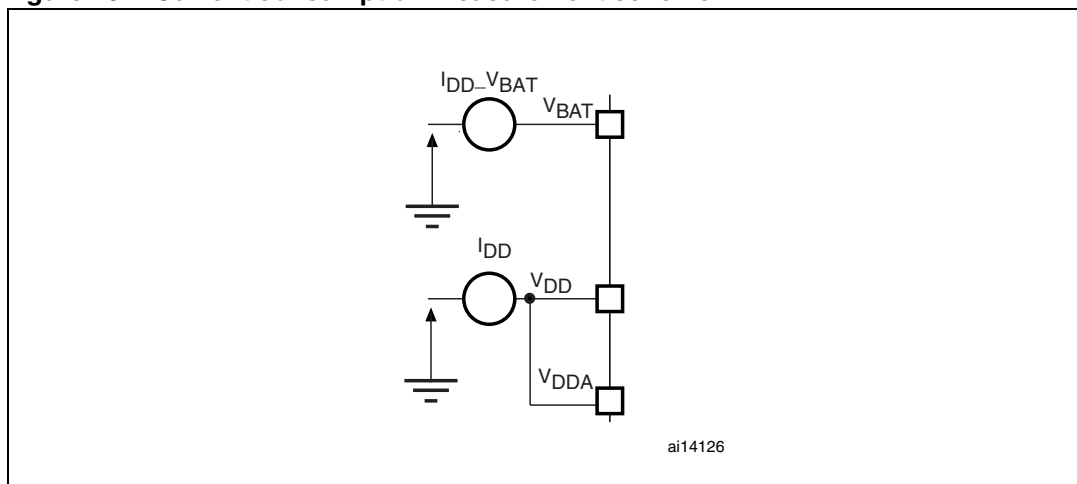
Figure 18. Power supply scheme



- 1. 4.7μF capacitor must be connected to one of the V_{DD} pin.

5.1.7 Current consumption measurement

Figure 19. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 7: Voltage characteristics](#), [Table 8: Current characteristics](#), and [Table 9: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Voltage characteristics

| Symbol | Ratings | Min | Max | Unit |
|----------------------|---|---|--------------|------|
| $V_{DD}-V_{SS}$ | External main supply voltage (including V_{DDA} , V_{DD}) ⁽¹⁾ | TBD | TBD | V |
| V_{IN} | Input voltage on five-volt tolerant pin ⁽²⁾ | $V_{SS}-0.3$ | $V_{DD}+4.0$ | |
| | Input voltage on any other pin ⁽³⁾ | $V_{SS}-0.3$ | 4.0 | |
| $ \Delta V_{DDx} $ | Variations between different V_{DD} power pins | | TBD | mV |
| $ V_{SSx} - V_{SS} $ | Variations between all the different ground pins | | TBD | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see Section 5.3.13: Absolute maximum ratings (electrical sensitivity) | | |

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded (see [Table 8: Current characteristics](#)). This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{INmax}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
3. Positive current injection is not possible on these I/Os. V_{IN} maximum must be respected. Negative current injection is possible and must not exceed $I_{INJ(PIN)}$.

Table 8. Current characteristics

| Symbol | Ratings | Max. | Unit |
|--------------------------------------|---|-------|------|
| I_{VDD} | Total current into V_{DD}/V_{DDA} power lines (source) ⁽¹⁾ | TBD | mA |
| I_{VSS} | Total current out of V_{SS} ground lines (sink) ⁽¹⁾ | TBD | |
| I_{IO} | Output current sunk by any I/O and control pin | TBD | |
| | Output current source by any I/Os and control pin | TBD | |
| $I_{INJ(PIN)}$ ⁽²⁾ | Injected current on five-volt tolerant I/O ⁽³⁾ | -5/+0 | |
| | Injected current on any other pin ⁽⁴⁾ | ±5 | |
| $\Sigma I_{INJ(PIN)}$ ⁽⁴⁾ | Total injected current (sum of all I/O and control pins) ⁽⁵⁾ | TBD | |

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in [Section 5.3.18: 12-bit ADC characteristics](#).
3. Positive injection is not possible on these I/Os. V_{IN} maximum must always be respected. $I_{INJ(PIN)}$ must never be exceeded. A negative injection is induced by $V_{IN} < V_{SS}$.
4. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.

- When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 9. Thermal characteristics

| Symbol | Ratings | Value | Unit |
|------------------|------------------------------|-------------|------|
| T _{STG} | Storage temperature range | -40 to +125 | °C |
| T _J | Maximum junction temperature | 125 | °C |

5.3 Operating conditions

5.3.1 General operating conditions

Table 10. General operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------------------|---|--|--------------------|-----|------|
| f _{HCLK} | Internal AHB clock frequency | | 0 | 120 | MHz |
| f _{PCLK1} | Internal APB1 clock frequency | | 0 | 30 | |
| f _{PCLK2} | Internal APB2 clock frequency | | 0 | 60 | |
| V _{DD} | Standard operating voltage | | 1.8 ⁽¹⁾ | 3.6 | V |
| V _{DDA} ⁽²⁾ | Analog operating voltage (ADC limited to 1 M samples) | Must be the same potential as V _{DD} ⁽³⁾ | 1.8 ⁽¹⁾ | 3.6 | V |
| | Analog operating voltage (ADC limited to 2 M samples) | | 2.4 | 3.6 | |
| V _{BAT} | Backup operating voltage | | 1.65 | 3.6 | V |
| P _D | Power dissipation at T _A = 85 °C for suffix 6 or T _A = 105 °C for suffix 7 ⁽⁴⁾ | LQFP64 | | 444 | mW |
| | | WLCSP66 | | 392 | |
| | | LQFP100 | | 434 | |
| | | LQFP144 | | 500 | |
| | | LQFP176 | | 526 | |
| | | UFBGA176 | | 513 | |
| T _A | Ambient temperature for 6 suffix version | Maximum power dissipation | -40 | 85 | °C |
| | | Low power dissipation ⁽⁵⁾ | -40 | 105 | |
| | Ambient temperature for 7 suffix version | Maximum power dissipation | -40 | 105 | °C |
| | | Low power dissipation ⁽⁵⁾ | -40 | 125 | |
| T _J | Junction temperature range | 6 suffix version | -40 | 105 | °C |
| | | 7 suffix version | -40 | 125 | |

- This value is reduced to 1.65 V for STM32F21x in WLCSP package assuming IRROFF is set to V_{DD}.
- When the ADC is used, refer to [Table 59: ADC characteristics](#).
- It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.

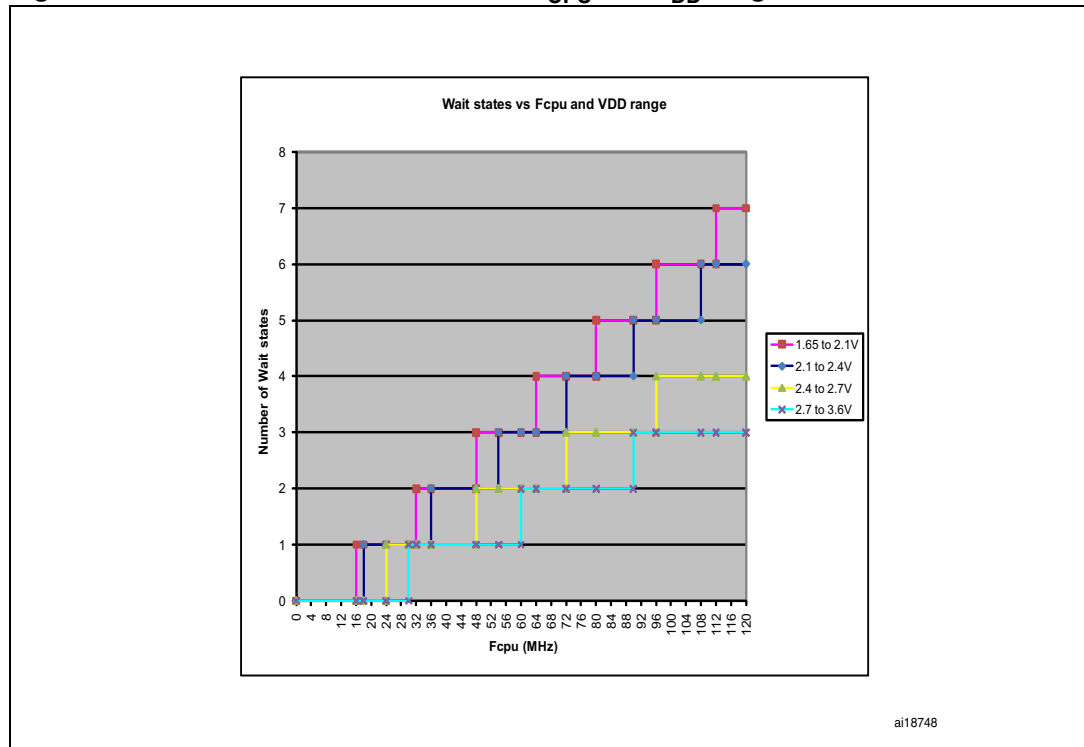
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} .
5. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} .

Table 11. Limitations depending on the operating power supply range

| Operating power supply range | ADC operation | Maximum Flash memory access frequency ($f_{Flashmax}$) | Number of wait states at maximum CPU frequency ($f_{CPUmax}=120\text{ MHz}$) ⁽¹⁾ | I/O operation | FSMC controller operation | Possible Flash memory operations |
|--|------------------------------|--|---|--|--|---|
| $V_{DD} = 1.8\text{ to }2.1\text{ V}$ ⁽²⁾ | Conversion time up to 1 Msps | 16 MHz with no Flash memory wait state | 7 ⁽³⁾ | – Degraded speed performance – No I/O compensation | up to 30 MHz | 8-bit erase and program operations only |
| $V_{DD} = 2.1\text{ to }2.4\text{ V}$ | Conversion time up to 1 Msps | 18 MHz with no Flash memory wait state | 6 ⁽³⁾ | – Degraded speed performance – No I/O compensation | up to 30 MHz | 16-bit erase and program operations |
| $V_{DD} = 2.4\text{ to }2.7\text{ V}$ | Conversion time up to 2 Msps | 24 MHz with no Flash memory wait state | 4 ⁽³⁾ | – Degraded speed performance – I/O compensation works | up to 48 MHz | 16-bit erase and program operations |
| $V_{DD} = 2.7\text{ to }3.6\text{ V}$ ⁽⁴⁾ | Conversion time up to 2 Msps | 30 MHz with no Flash memory wait state | 3 ⁽³⁾ | – Full-speed operation – I/O compensation works | – up to 60 MHz when $V_{DD} = 3.0\text{ to }3.6\text{ V}$ – up to 48 MHz when $V_{DD} = 2.7\text{ to }3.0\text{ V}$ | 32-bit erase and program operations |

1. The number of wait states can be reduced by reducing the CPU frequency (see [Figure 20](#)).
2. This voltage range is reduced to 1.65 to 2.1 V for devices in WLCSP package assuming IRROFF is set to V_{DD} .
3. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
4. The voltage range for ULPI USB high-speed, Ethernet MII and Ethernet RMII is 3.0 to 3.6 V.

Figure 20. Number of wait states versus f_{CPU} and V_{DD} range



5.3.2 Operating conditions at power-up / power-down (regulator not bypassed)

Subject to general operating conditions for T_A .

Table 12. Operating conditions at power-up / power-down (regulator not bypassed)

| Symbol | Parameter | Min | Max | Unit |
|-----------|-------------------------|-----|----------|-----------|
| t_{VDD} | V_{DD} rise time rate | TBD | ∞ | $\mu s/V$ |
| | V_{DD} fall time rate | TBD | ∞ | |

5.3.3 Operating conditions at power-up / power-down in regulator bypass mode

Subject to general operating conditions for T_A .

Table 13. Operating conditions at power-up / power-down in regulator bypass mode

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------|--|------------|-----|----------|-----------------|
| t_{VDD} | V_{DD} rise time rate | Power-up | TBD | ∞ | $\mu\text{s/V}$ |
| | V_{DD} fall time rate | Power-down | TBD | ∞ | |
| t_{VCAP} | V_{CAP_1} and V_{CAP_2} rise time rate | Power-up | TBD | ∞ | |
| | V_{CAP_1} and V_{CAP_2} fall time rate | Power-down | TBD | ∞ | |

5.3.4 Embedded reset and power control block characteristics

The parameters given in [Table 14](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 10](#).

Table 14. Embedded reset and power control block characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------|---|-----------------------------|-----|------|-----|------|
| V_{PVD} | Programmable voltage detector level selection | PLS[2:0]=000 (rising edge) | TBD | TBD | TBD | V |
| | | PLS[2:0]=000 (falling edge) | TBD | 2.00 | TBD | V |
| | | PLS[2:0]=001 (rising edge) | TBD | TBD | TBD | V |
| | | PLS[2:0]=001 (falling edge) | TBD | 2.20 | TBD | V |
| | | PLS[2:0]=010 (rising edge) | TBD | TBD | TBD | V |
| | | PLS[2:0]=010 (falling edge) | TBD | 2.30 | TBD | V |
| | | PLS[2:0]=011 (rising edge) | TBD | TBD | TBD | V |
| | | PLS[2:0]=011 (falling edge) | TBD | 2.50 | TBD | V |
| | | PLS[2:0]=100 (rising edge) | TBD | TBD | TBD | V |
| | | PLS[2:0]=100 (falling edge) | TBD | 2.70 | TBD | V |
| | | PLS[2:0]=101 (rising edge) | TBD | TBD | TBD | V |
| | | PLS[2:0]=101 (falling edge) | TBD | 2.80 | TBD | V |
| | | PLS[2:0]=110 (rising edge) | TBD | TBD | TBD | V |
| | | PLS[2:0]=110 (falling edge) | TBD | 2.90 | TBD | V |
| | | PLS[2:0]=111 (rising edge) | TBD | TBD | TBD | V |
| PLS[2:0]=111 (falling edge) | TBD | 3.00 | TBD | V | | |
| $V_{PVDhyst}^{(2)}$ | PVD hysteresis | | | 100 | | mV |

Table 14. Embedded reset and power control block characteristics (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|--|--------------|--------------------|------|-----|------|
| $V_{POR/PDR}$ | Power-on/power-down reset threshold | Falling edge | TBD ⁽¹⁾ | 1.70 | TBD | V |
| | | Rising edge | TBD | 1.74 | TBD | V |
| V_{BOR1} | Brownout level 1 threshold | Falling edge | TBD | 2.20 | TBD | V |
| | | Rising edge | TBD | TBD | TBD | V |
| V_{BOR2} | Brownout level 2 threshold | Falling edge | TBD | 2.50 | TBD | V |
| | | Rising edge | TBD | TBD | TBD | V |
| V_{BOR3} | Brownout level 3 threshold | Falling edge | TBD | 2.80 | TBD | V |
| $V_{PDRhyst}^{(2)}$ | PDR hysteresis | | | 40 | | mV |
| $T_{RSTTEMPO}^{(2)}$ | Reset temporization | | TBD | TBD | TBD | ms |
| I_{RUSH} | InRush current on voltage regulator power-on | | - | - | 200 | mA |

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 19: Current consumption measurement scheme](#).

All run mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 30 MHz, 1 wait state from 30 to 60 MHz, 2 wait states from 60 to 90 MHz and 3 wait states from 90 to 120 MHz).
- Prefetch and Cache ON (Reminder: this bit must be set before clock setting and bus prescaling).
- When the peripherals are enabled f_{PCLK1} = f_{HCLK}/4, f_{PCLK2} = f_{HCLK}/2, f_{ADCCLK} = f_{PCLK2}/4
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A = 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Table 15. Typical and maximum current consumption in Run mode, code with data processing running from Flash

| Symbol | Parameter | Conditions | f _{HCLK} | Typical | Max ⁽¹⁾ | | Unit |
|-----------------|----------------------------|--|-------------------|------------------------|------------------------|-------------------------|------|
| | | | | T _A = 25 °C | T _A = 85 °C | T _A = 105 °C | |
| I _{DD} | Supply current in Run mode | External clock ⁽²⁾ , all peripherals enabled | 120 MHz | TBD | TBD | TBD | mA |
| | | | 90 MHz | TBD | TBD | TBD | |
| | | | 60 MHz | TBD | TBD | TBD | |
| | | | 30 MHz | TBD | TBD | TBD | |
| | | | 26 MHz | TBD | TBD | TBD | |
| | | | 16 MHz | TBD | TBD | TBD | |
| | | External clock ⁽²⁾ , all peripherals disabled | 120 MHz | TBD | TBD | TBD | |
| | | | 90 MHz | TBD | TBD | TBD | |
| | | | 60 MHz | TBD | TBD | TBD | |
| | | | 30 MHz | TBD | TBD | TBD | |
| | | | 26 MHz | TBD | TBD | TBD | |
| | | | 16 MHz | TBD | TBD | TBD | |

1. Based on characterization, not tested in production.
 2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 16. Typical and maximum current consumption in Run mode, code with data processing running from RAM

| Symbol | Parameter | Conditions | f _{HCLK} | Typ | Max ⁽¹⁾ | | Unit |
|-----------------|----------------------------|--|-------------------|------------------------|------------------------|-------------------------|------|
| | | | | T _A = 25 °C | T _A = 85 °C | T _A = 105 °C | |
| I _{DD} | Supply current in Run mode | External clock ⁽²⁾ , all peripherals enabled ⁽³⁾ | 120 MHz | 49.5 | TBD | TBD | mA |
| | | | 90 MHz | 38 | TBD | TBD | |
| | | | 60 MHz | 26 | TBD | TBD | |
| | | | 30 MHz | 14.5 | TBD | TBD | |
| | | | 26 MHz | TBD | TBD | TBD | |
| | | | 16 MHz | TBD | TBD | TBD | |
| | | External clock ⁽²⁾ , all peripherals disabled | 120 MHz | 22 | TBD | TBD | |
| | | | 90 MHz | 17 | TBD | TBD | |
| | | | 60 MHz | 12.5 | TBD | TBD | |
| | | | 30 MHz | 7 | TBD | TBD | |
| | | | 26 MHz | TBD | TBD | TBD | |
| | | | 16 MHz | TBD | TBD | TBD | |

1. Based on characterization, tested in production at V_{DD} max, f_{HCLK} max.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.
3. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

Table 17. Typical and maximum current consumption in Sleep mode

| Symbol | Parameter | Conditions | f _{HCLK} | Typ | Max ⁽¹⁾ | | Unit |
|-----------------|------------------------------|--|-------------------|------------------------|------------------------|-------------------------|------|
| | | | | T _A = 25 °C | T _A = 85 °C | T _A = 105 °C | |
| I _{DD} | Supply current in Sleep mode | External clock ⁽²⁾ , all peripherals enabled ⁽³⁾ | 120 MHz | 37.5 | TBD | TBD | mA |
| | | | 90 MHz | 29.5 | TBD | TBD | |
| | | | 60 MHz | 20.5 | TBD | TBD | |
| | | | 30 MHz | 14.5 | TBD | TBD | |
| | | | 26 MHz | TBD | TBD | TBD | |
| | | | 16 MHz | TBD | TBD | TBD | |
| | | External clock ⁽²⁾ , all peripherals disabled | 120 MHz | 8.0 | TBD | TBD | |
| | | | 90 MHz | 6.5 | TBD | TBD | |
| | | | 60 MHz | 5.0 | TBD | TBD | |
| | | | 30 MHz | 3.5 | TBD | TBD | |
| | | | 26 MHz | TBD | TBD | TBD | |
| | | | 16 MHz | TBD | TBD | TBD | |

1. Based on characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

3. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

Table 18. Typical and maximum current consumptions in Stop mode

| Symbol | Parameter | Conditions | Typ ⁽¹⁾ | | | Max | | Unit |
|----------------------|---|---|---|---|---|------------------------|-------------------------|------|
| | | | V _{DD} /V _{BAT} = 1.8 V | V _{DD} /V _{BAT} = 2.4 V | V _{DD} /V _{BAT} = 3.3 V | T _A = 85 °C | T _A = 105 °C | |
| I _{DD_STOP} | Supply current in Stop mode with main regulator in Run mode | Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 350 | | | TBD | TBD | µA |
| | | Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 300 | | | TBD | TBD | |
| | Supply current in Stop mode with main regulator in Low Power mode | Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 200 | | | | | |
| | | Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 150 | | | | | |

1. Typical values are measured at T_A = 25 °C.

Table 19. Typical and maximum current consumptions in Standby mode

| Symbol | Parameter | Conditions | Typ ⁽¹⁾ | | | Max | | Unit |
|----------------------|--------------------------------|--------------------------|---|---|---|------------------------|-------------------------|------|
| | | | V _{DD} /V _{BAT} = 1.8 V | V _{DD} /V _{BAT} = 2.4 V | V _{DD} /V _{BAT} = 3.3 V | T _A = 85 °C | T _A = 105 °C | |
| I _{DD_STBY} | Supply current in Standby mode | Backup SRAM ON, RTC ON | 4 | | | TBD ⁽²⁾ | TBD ⁽²⁾ | µA |
| | | Backup SRAM OFF, RTC ON | 3.3 | | | TBD ⁽²⁾ | TBD ⁽²⁾ | |
| | | Backup SRAM ON, RTC OFF | 3.2 | | | TBD ⁽²⁾ | TBD ⁽²⁾ | |
| | | Backup SRAM OFF, RTC OFF | 2.5 | | | TBD ⁽²⁾ | TBD ⁽²⁾ | |

1. Typical values are measured at T_A = 25 °C.

2. Based on characterization, not tested in production.

Table 20. Typical and maximum current consumptions in VBAT mode

| Symbol | Parameter | Conditions | Typ ⁽¹⁾ | | | Max | | Unit |
|----------------------|------------------------------|--|--|--|--|---------------------------|----------------------------|------|
| | | | V _{DD} /V _{BAT} = 1.8 V | V _{DD} /V _{BAT} = 2.4 V | V _{DD} /V _{BAT} = 3.3 V | T _A = 85 °C | T _A = 105 °C | |
| I _{DD_VBAT} | Backup domain supply current | Backup SRAM OFF, low-speed oscillator and RTC ON | 0.8 | | | TBD ⁽²⁾ | TBD ⁽²⁾ | µA |
| | | Backup SRAM ON, RTC ON | 1.5 | | | TBD ⁽²⁾ | TBD ⁽²⁾ | |
| | | Backup SRAM OFF, RTC OFF | 0 | | | TBD ⁽²⁾ | TBD ⁽²⁾ | |
| | | Backup SRAM ON, RTC OFF | 0.7 | | | TBD ⁽²⁾ | TBD ⁽²⁾ | |

1. Typical values are measured at T_A = 25 °C.
2. Based on characterization, not tested in production.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in [Table 21](#). The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with one peripheral clocked on (with only the clock applied)
- ambient operating temperature and V_{DD} supply voltage conditions summarized in [Table 7](#).

Table 21. Peripheral current consumption

| Peripheral ⁽¹⁾ | | Typical consumption at 25 °C | Unit |
|---------------------------|---------|------------------------------|------|
| AHB1 | GPIO A | TBD | mA |
| | GPIO B | TBD | |
| | GPIO C | TBD | |
| | GPIO D | TBD | |
| | GPIO E | TBD | |
| | GPIO F | TBD | |
| | GPIO G | TBD | |
| | GPIO H | TBD | |
| | GPIO I | TBD | |
| | OTG_HS | TBD | |
| | ETH_MAC | TBD | |
| AHB2 | OTG_FS | TBD | mA |
| | DCMI | TBD | |
| | RNG | TBD | |
| AHB2 | CRYPTO | TBD | mA |
| | HASH | TBD | |

Table 21. Peripheral current consumption (continued)

| Peripheral ⁽¹⁾ | | Typical consumption at 25 °C | Unit |
|---------------------------|---------------------|------------------------------|------|
| APB1 | TIM2 | TBD | mA |
| | TIM3 | TBD | |
| | TIM4 | TBD | |
| | TIM5 | TBD | |
| | TIM6 | TBD | |
| | TIM7 | TBD | |
| | TIM12 | TBD | |
| | TIM13 | TBD | |
| | TIM14 | TBD | |
| | USART2 | TBD | |
| | USART3 | TBD | |
| | UART4 | TBD | |
| | UART5 | TBD | |
| | I2C1 | TBD | |
| | I2C2 | TBD | |
| | I2C3 | TBD | |
| | SPI2 | TBD | |
| | SPI3 | TBD | |
| | CAN1 | TBD | |
| CAN2 | TBD | | |
| DAC | TBD | | |
| APB2 | SDIO | TBD | mA |
| | TIM1 | TBD | |
| | TIM8 | TBD | |
| | TIM9 | TBD | |
| | TIM10 | TBD | |
| | TIM11 | TBD | |
| | ADC1 ⁽²⁾ | TBD | |
| | ADC2 ⁽²⁾ | TBD | |
| | ADC3 | TBD | |
| | SPI1 | TBD | |
| | USART1 | TBD | |
| | USART6 | TBD | |

1. $f_{HCLK} = 120\text{ MHz}$, $f_{APB1} = f_{HCLK}/4$, $f_{APB2} = f_{HCLK}/2$, default prescaler value for each peripheral.
2. Specific conditions for ADC: $f_{HCLK} = 120\text{ MHz}$, $f_{APB1} = f_{HCLK}/4$, $f_{APB2} = f_{HCLK}/2$, $f_{ADCLK} = f_{APB2}/2$, ADON bit in the ADC_CR2 register is set to 1.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in [Table 22](#) result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 10](#).

Table 22. High-speed external user clock characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|---|----------------------------------|-------------|-----|-------------|---------|
| f_{HSE_ext} | External user clock source frequency ⁽¹⁾ | | 1 | 8 | 50 | MHz |
| V_{HSEH} | OSC_IN input pin high level voltage | | $0.7V_{DD}$ | | V_{DD} | V |
| V_{HSEL} | OSC_IN input pin low level voltage | | V_{SS} | | $0.3V_{DD}$ | |
| $t_{w(HSE)}$ $t_{w(HSE)}$ | OSC_IN high or low time ⁽¹⁾ | | 16 | | | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time ⁽¹⁾ | | | | 20 | |
| $C_{in(HSE)}$ | OSC_IN input capacitance ⁽¹⁾ | | | 5 | | pF |
| $DuCy_{(HSE)}$ | Duty cycle | | 45 | | 55 | % |
| I_L | OSC_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | | | ± 1 | μA |

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

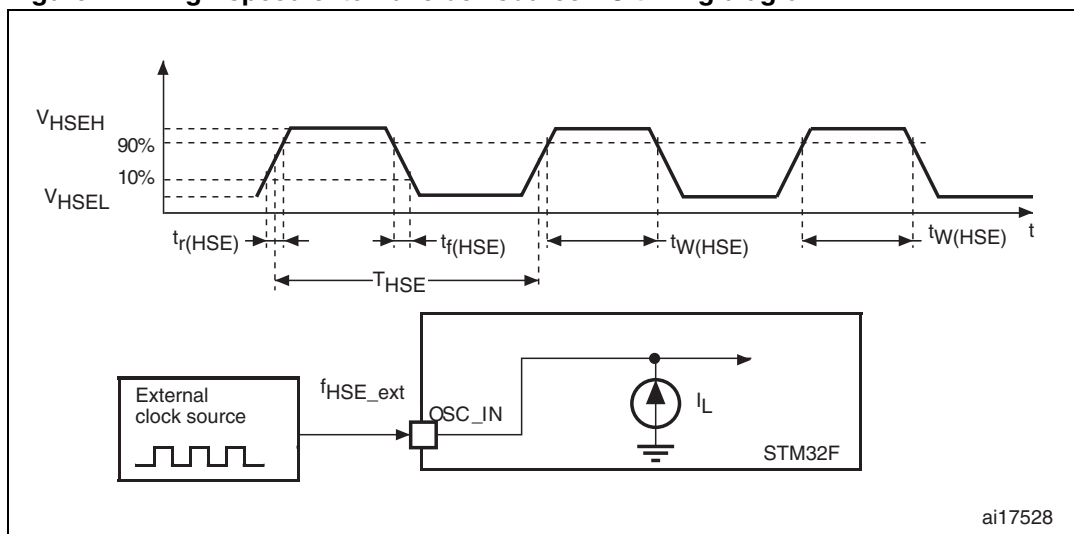
The characteristics given in [Table 23](#) result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 10](#).

Table 23. Low-speed external user clock characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|---|----------------------------------|-------------|--------|-------------|---------|
| f_{LSE_ext} | User External clock source frequency ⁽¹⁾ | | | 32.768 | 1000 | kHz |
| V_{LSEH} | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | | V_{DD} | V |
| V_{LSEL} | OSC32_IN input pin low level voltage | | V_{SS} | | $0.3V_{DD}$ | |
| $t_{w(LSE)}$ $t_{w(LSE)}$ | OSC32_IN high or low time ⁽¹⁾ | | 450 | | | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time ⁽¹⁾ | | | | 50 | |
| $C_{in(LSE)}$ | OSC32_IN input capacitance ⁽¹⁾ | | | 5 | | pF |
| $DuCy_{(LSE)}$ | Duty cycle | | 30 | | 70 | % |
| I_L | OSC32_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | | | ± 1 | μA |

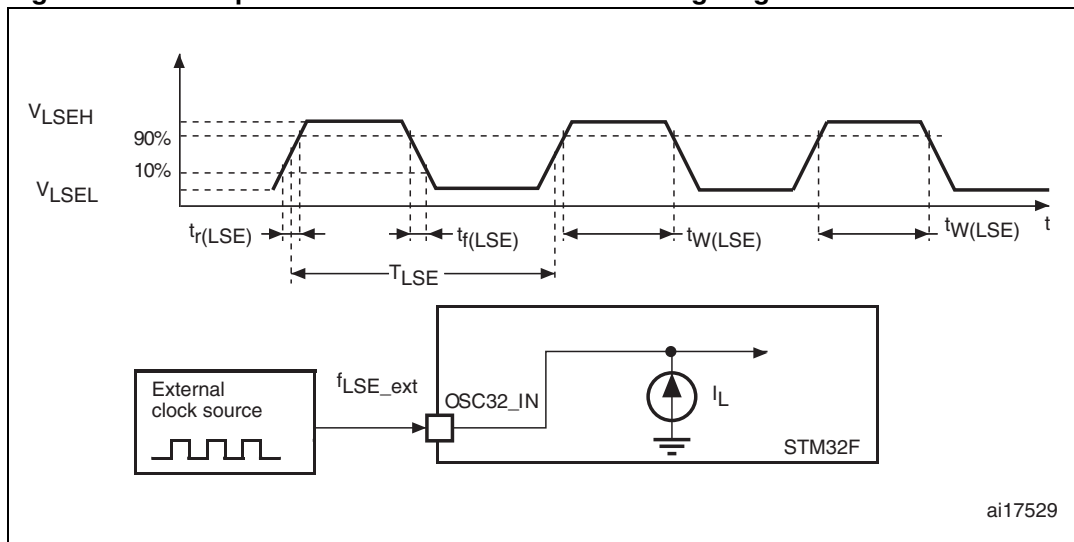
1. Guaranteed by design, not tested in production.

Figure 21. High-speed external clock source AC timing diagram



ai17528

Figure 22. Low-speed external clock source AC timing diagram



ai17529

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 24](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

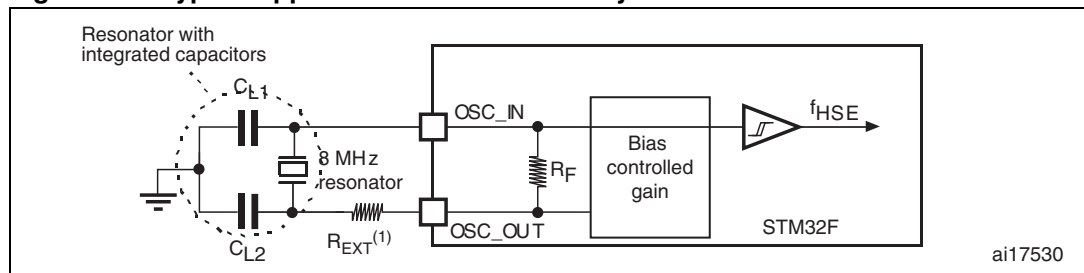
Table 24. HSE 4-26 MHz oscillator characteristics^{(1) (2)}

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|--|---|-----|-----|-----|------------|
| f_{OSC_IN} | Oscillator frequency | | 4 | | 26 | MHz |
| R_F | Feedback resistor | | | 200 | | k Ω |
| C | Recommended load capacitance versus equivalent serial resistance of the crystal (R_S) ⁽³⁾ | $R_S = 30 \Omega$ | | 30 | | pF |
| i_2 | HSE driving current | $V_{DD} = 3.3 V, V_{IN} = V_{SS}$ with 30 pF load | | | 1 | mA |
| g_m | Oscillator transconductance | Startup | 25 | | | mA/V |
| $t_{SU(HSE)}$ ⁽⁴⁾ | Startup time | V_{DD} is stabilized | | 2 | | ms |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 23](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} . Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 23. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 25](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 25. LSE oscillator characteristics ($f_{LSE} = 32.768 \text{ kHz}$) ⁽¹⁾

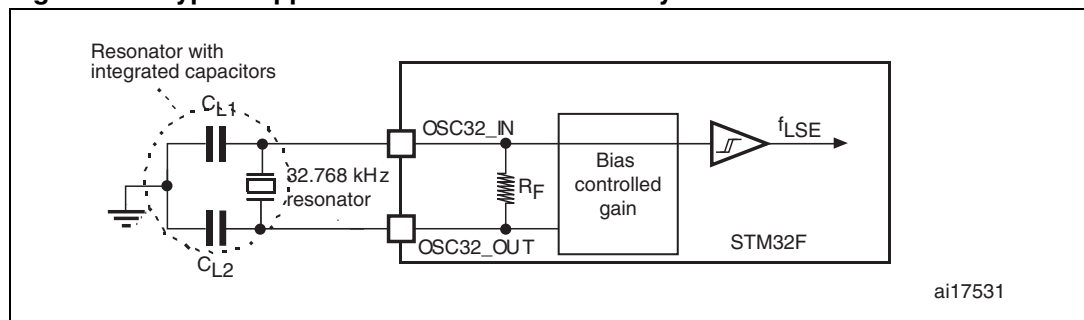
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|--|---|-----|-----|-----|-----------------|
| R_F | Feedback resistor | | | 5 | | $M\Omega$ |
| $C^{(2)}$ | Recommended load capacitance versus equivalent serial resistance of the crystal (R_S) ⁽³⁾ | $R_S = 30 \text{ k}\Omega$ | | | 15 | μF |
| I_2 | LSE driving current | $V_{DD} = 3.3 \text{ V}, V_{IN} = V_{SS}$ | | | 1.4 | μA |
| g_m | Oscillator Transconductance | | 5 | | | $\mu\text{A/V}$ |
| $t_{SU(LSE)}^{(4)}$ | startup time | V_{DD} is stabilized | | 3 | | s |

1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Note: For C_{L1} and C_{L2} it is recommended to use high-quality external ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 24). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7 \text{ pF}$. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of $C_L = 6 \text{ pF}$, and $C_{stray} = 2 \text{ pF}$, then $C_{L1} = C_{L2} = 8 \text{ pF}$.

Figure 24. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in [Table 26](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 10](#).

High-speed internal (HSI) RC oscillator

Table 26. HSI oscillator characteristics ⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|---------------|----------------------------------|--|-------------------------|-----|-----|------|---|
| f_{HSI} | Frequency | | | 16 | | MHz | |
| ACC_{HSI} | Accuracy of the HSI oscillator | User-trimmed with the RCC_CR register ⁽²⁾ | | | TBD | % | |
| | | Factory-calibrated | $T_A = -40$ to 105 °C | TBD | | TBD | % |
| | | | $T_A = -10$ to 85 °C | TBD | | TBD | % |
| | | | $T_A = 0$ to 70 °C | TBD | | TBD | % |
| | $T_A = 25$ °C | TBD | | TBD | % | | |
| $t_{su(HSI)}$ | HSI oscillator startup time | | TBD | | TBD | µs | |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | | 80 | TBD | µA | |

- $V_{DD} = 3.3$ V, $T_A = -40$ to 105 °C unless otherwise specified.
- Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website www.st.com.

Low-speed internal (LSI) RC oscillator

Table 27. LSI oscillator characteristics ⁽¹⁾

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------------|----------------------------------|-----|------|-----|------|
| $f_{LSI}^{(2)}$ | Frequency | 30 | 32 | 60 | kHz |
| $t_{su(LSI)}^{(3)}$ | LSI oscillator startup time | | 85 | TBD | µs |
| $I_{DD(LSI)}^{(3)}$ | LSI oscillator power consumption | | 0.65 | TBD | µA |

- $V_{DD} = 3$ V, $T_A = -40$ to 105 °C unless otherwise specified.
- Based on characterization, not tested in production.
- Guaranteed by design, not tested in production.

5.3.8 Wakeup time from low-power mode

The wakeup times given in [Table 28](#) is measured on a wakeup phase with a 16 MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 10](#).

Table 28. Low-power mode wakeup timings

| Symbol | Parameter | Typ | Unit |
|---------------------|--|-----|---------|
| $t_{WUSLEEP}^{(1)}$ | Wakeup from Sleep mode | 1 | μs |
| $t_{WUSTOP}^{(1)}$ | Wakeup from Stop mode (regulator in run mode) | 9 | μs |
| | Wakeup from Stop mode (regulator in low power mode) | 15 | |
| | Wakeup from Stop mode (regulator in low power mode and Flash memory in Deep power down mode) | 110 | |
| $t_{WUSTDBY}^{(1)}$ | Wakeup from Standby mode | 200 | μs |

1. The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

5.3.9 PLL characteristics

The parameters given in [Table 29](#) and [Table 30](#) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in [Table 10](#).

Table 29. Main PLL characteristics

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ ⁽¹⁾ | Max ⁽¹⁾ | Unit |
|------------------|------------------------------------|--|--------------------|--------------------|--------------------|---------|
| f_{PLL_IN} | PLL input clock ⁽²⁾ | | 0.95 | 1 | 2.00 | MHz |
| f_{PLL_OUT} | PLL multiplier output clock | | 24 | | 120 | MHz |
| f_{PLL48_OUT} | 48 MHz PLL multiplier output clock | | | | 48 | MHz |
| f_{VCO_OUT} | PLL VCO output | | 192 | | 432 | MHz |
| t_{LOCK} | PLL lock time | | | | 350 | μs |
| Jitter | Cycle-to-cycle jitter | System clock 120 MHz | | | 300 | ps |
| $I_{DD(PLL)}$ | PLL power consumption on VDD | VCO freq = 192 MHz VCO freq = 432 MHz | TBC | | TBC | mA |
| $I_{DDA(PLL)}$ | PLL power consumption on VDDA | VCO freq = 192 MHz VCO freq = 432 MHz | TBC | | TBC | mA |

1. Based on characterization, not tested in production.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.

Table 30. PLLI2S (audio PLL) characteristics

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ ⁽¹⁾ | Max ⁽¹⁾ | Unit |
|-------------------|-----------------------------------|----------------------|--------------------|--------------------|--------------------|---------|
| f_{PLLI2S_IN} | PLLI2S input clock ⁽²⁾ | | 0.95 | 1 | 1.05 | MHz |
| f_{PLLI2S_OUT} | PLLI2S multiplier output clock | | | | 216 | MHz |
| f_{VCO_OUT} | PLLI2S VCO output | | 192 | | 432 | MHz |
| t_{LOCK} | PLLI2S lock time | | | | 350 | μs |
| Jitter | Cycle-to-cycle jitter | System clock 120 MHz | | | 300 | ps |



Table 30. PLLI2S (audio PLL) characteristics (continued)

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ ⁽¹⁾ | Max ⁽¹⁾ | Unit |
|--------------------------|--|--|--------------------|--------------------|--------------------|------|
| Jitter | Master I2S clock jitter | Cycle to cycle at 12,343 KHz on 48KHz period N=432, P=4, R=5 | TBC | | TBC | ps |
| Jitter | Master I2S clock jitter | Average frequency of 12,343 KHz N=432, P=4, R=5 on 256 samples | TBC | | TBC | ps |
| Jitter | WS I2S clock jitter | Cycle to cycle at 48 KHz on 1000 samples | TBC | | TBC | ps |
| Jitter | Main Clock Output for Ethernet | Cycle to cycle at 50 MHz on 1000 samples | TBC | | TBC | ps |
| Jitter | Bit Time CAN Jitter | Cycle to cycle at 1 MHz on 1000 samples | TBC | | TBC | ps |
| I _{DD(PLLI2S)} | PLLI2S power consumption on V _{DD} | VCO freq = 192 MHz VCO freq = 432 MHz | TBC | | TBC | mA |
| I _{DDA(PLLI2S)} | PLLI2S power consumption on V _{DDA} | VCO freq = 192 MHz VCO freq = 432 MHz | TBC | | TBC | mA |

1. Based on characterization, not tested in production.
2. Take care of using the appropriate division factor M to have the specified PLL input clock values.

5.3.10 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature is only available on the main PLL.

Table 31. SSCG parameters constraint

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------|-----------------------|-----|-----|--------------------|------|
| f _{Mod} | Modulation frequency | | | 10 | KHz |
| md | Peak modulation depth | 0.5 | | 2 | dec |
| MODEPER * INCSTEP | | | | 2 ¹⁵ -1 | dec |

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$\text{MODEPER} = \text{round}[f_{\text{PLL_IN}} / (4 \times f_{\text{Mod}})]$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$\text{INCSTEP} = \text{round}[\frac{(2^{15} - 1) \times \text{md} \times f_{\text{VCO_OUT}}}{(100 \times 5 \times \text{MODEPER})}]$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODEPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$\text{md}_{\text{quantized}}\% = \frac{(\text{MODEPER} \times \text{INCSTEP} \times 100 \times 5)}{((2^{15} - 1) \times f_{\text{VCO_OUT}})}$$

Figure 25 and Figure 26 show the main PLL output clock waveforms in center spread and down spread modes, where:

- F0 is $f_{\text{PLL_OUT}}$ nominal.
- T_{mode} is the modulation period.
- md is the modulation depth.

Figure 25. PLL output clock waveforms in center spread mode

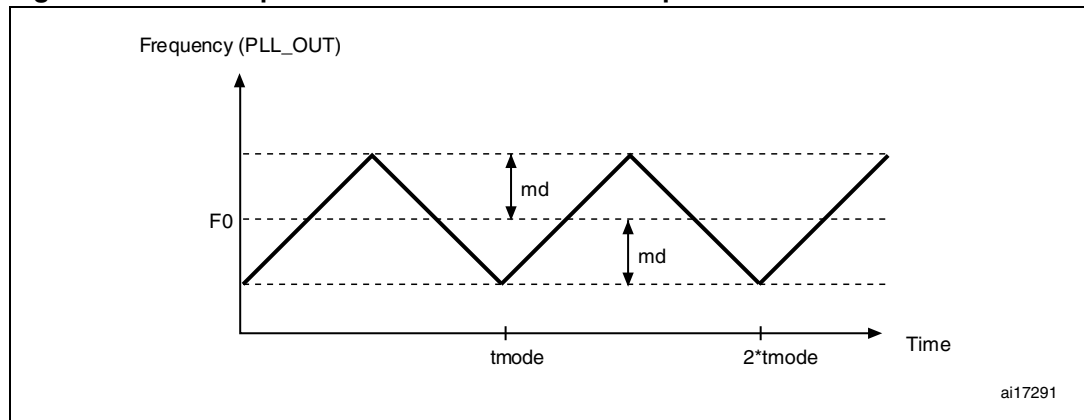
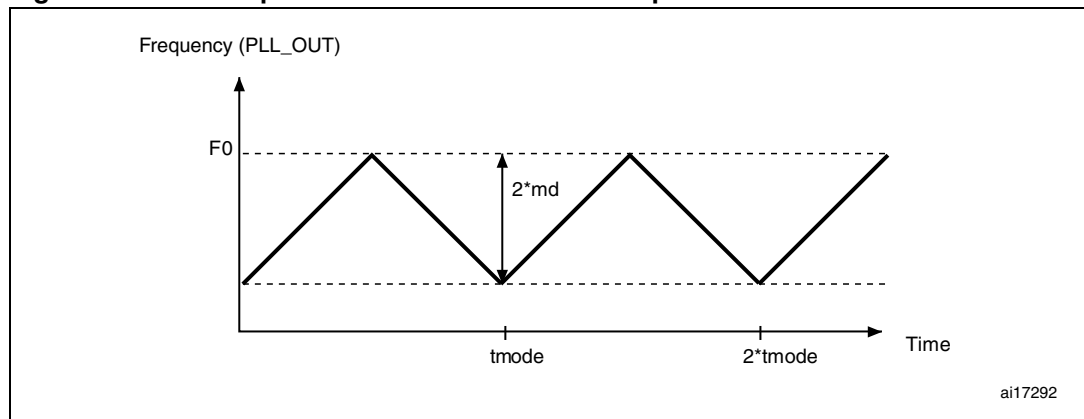


Figure 26. PLL output clock waveforms in down spread mode



5.3.11 Memory characteristics

Flash memory

The characteristics are given at $T_A = -40$ to 105 °C unless otherwise specified.

Table 32. Flash memory characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------|----------------|---|-----|-----|---------|
| I_{DD} | Supply current | Read mode $f_{HCLK} = 120$ MHz with 3 wait states, $V_{DD} = 3.3$ V | | TBD | mA |
| | | Write / Erase modes $f_{HCLK} = 120$ MHz, $V_{DD} = 3.3$ V | | TBD | mA |
| | | Power-down mode / Halt, $V_{DD} = 3.0$ to 3.6 V | | TBD | μ A |

Table 33. Flash memory programming

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ | Max ⁽¹⁾ | Unit |
|------------------|----------------------------|--------------------------|--------------------|-----|--------------------|---------|
| t_{prog} | Word programming time | $T_A = -40$ to $+105$ °C | | 12 | 100 | μ s |
| $t_{ERASE16KB}$ | Sector (16 KB) erase time | | | 400 | | ms |
| $t_{ERASE64KB}$ | Sector (64 KB) erase time | | | 700 | | ms |
| $t_{ERASE128KB}$ | Sector (128 KB) erase time | | | 1 | | s |
| t_{ME} | Mass erase time | | TBD | | TBD | ms |
| V_{prog} | Programming voltage | 32-bit program operation | 2.7 | | 3.6 | V |
| | | 16-bit program operation | 2.1 | | 3.6 | V |
| | | 8-bit program operation | 1.8 | | 3.6 | V |

1. Guaranteed by design, not tested in production.

Table 34. Flash memory programming with V_{PP}

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ | Max ⁽¹⁾ | Unit | |
|------------------|--|-----------------------|--------------------|-----|--------------------|---------|------|
| t_{prog} | Double word programming | $T_A = 0$ to $+40$ °C | | 7 | 60 | μ s | |
| $t_{ERASE16KB}$ | Sector (16 KB) erase time | | | TBD | | | |
| $t_{ERASE64KB}$ | Sector (64 KB) erase time | | | TBD | | | |
| $t_{ERASE128KB}$ | Sector (128 KB) erase time | | | TBD | | | |
| t_{ME} | Mass erase time | | | TBD | | | |
| V_{prog} | Programming voltage | | | 2.7 | | 3.6 | V |
| V_{PP} | V_{PP} voltage range | | | 7 | | 9 | V |
| I_{PP} | Minimum current sunk on the V_{PP} pin | | | 10 | | | mA |
| $t_{VPP}^{(2)}$ | Cumulative time during which V_{PP} is applied | | | | | 1 | hour |

1. Guaranteed by design, not tested in production.
2. V_{PP} should only be connected during programming/erasing.

Table 35. Flash memory endurance and data retention

| Symbol | Parameter | Conditions | Value | | | Unit |
|-----------|----------------|---|--------------------|-----|-----|---------|
| | | | Min ⁽¹⁾ | Typ | Max | |
| N_{END} | Endurance | $T_A = -40$ to $+85$ °C (6 suffix versions) $T_A = -40$ to $+105$ °C (7 suffix versions) | 10 | | | kcycles |
| t_{RET} | Data retention | 1 kcycle ⁽²⁾ at $T_A = 85$ °C | 30 | | | Years |
| | | 1 kcycle ⁽²⁾ at $T_A = 105$ °C | 10 | | | |
| | | 10 kcycles ⁽²⁾ at $T_A = 55$ °C | 20 | | | |

1. Based on characterization, not tested in production.
2. Cycling performed over the whole temperature range.

5.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 36](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 36. EMS characteristics

| Symbol | Parameter | Conditions | Level/Class |
|------------|---|---|-------------|
| V_{FESD} | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD} = 3.3$ V, LQFP100, $T_A = +25$ °C, $f_{HCLK} = 75$ MHz, conforms to IEC 61000-4-2 | 2B |
| V_{EFTB} | Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance | $V_{DD} = 3.3$ V, LQFP100, $T_A = +25$ °C, $f_{HCLK} = 75$ MHz, conforms to IEC 61000-4-2 | 4A |

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 37. EMI characteristics

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [f _{HSE} /f _{HCLK}] | | Unit |
|------------------|------------|--|--------------------------|--|----------|------|
| | | | | 8/48 MHz | 8/72 MHz | |
| S _{EMI} | Peak level | V _{DD} = 3.3 V, T _A = 25 °C, LQFP100 package compliant with IEC61967-2 | 0.1 to 30 MHz | 9 | 9 | dBμV |
| | | | 30 to 130 MHz | 26 | 13 | |
| | | | 130 MHz to 1GHz | 25 | 31 | |
| | | | SAE EMI Level | 4 | 4 | - |

5.3.13 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 38. ESD absolute maximum ratings

| Symbol | Ratings | Conditions | Class | Maximum value ⁽¹⁾ | Unit |
|----------------|---|---|-------|------------------------------|------|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A = +25\text{ °C}$ conforming to JESD22-A114 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A = +25\text{ °C}$ conforming to JESD22-C101 | II | 500 | |

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 39. Electrical sensitivities

| Symbol | Parameter | Conditions | Class |
|--------|-----------------------|--|------------|
| LU | Static latch-up class | $T_A = +105\text{ °C}$ conforming to JESD78A | II level A |

5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 40](#) are derived from tests performed under the conditions summarized in [Table 10](#). All I/Os are CMOS and TTL compliant.

Table 40. I/O static characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|-----------|---|---|-----------------------------|-----|----------------|------|----------------|
| V_{IL} | Input low level voltage | TTL ports $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | $V_{SS} - 0.3$ | | 0.8 | V | |
| V_{IH} | Standard I/O input high level voltage | | 2 | | $V_{DD} + 0.3$ | | |
| | FT ⁽¹⁾ I/O input high level voltage | | 2 | | 5.5V | | |
| V_{IL} | Input low level voltage | CMOS ports $1.65\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | -0.3 | | $0.3 V_{DD}$ | | |
| V_{IH} | Standard I/O high level voltage | | 0.7 V_{DD} | | | | $V_{DD} + 0.3$ |
| | FT ⁽¹⁾ I/O input high level voltage | | | | | | 5.25 |
| | | CMOS ports $2.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | | | 5.5 | | |
| V_{hys} | Standard IO Schmitt trigger voltage hysteresis ⁽²⁾ | | 200 | | | mV | |
| | IO FT Schmitt trigger voltage hysteresis ⁽²⁾ | | $5\% V_{DD}$ ⁽³⁾ | | | mV | |

Table 40. I/O static characteristics (continued)

| Symbol | Parameter | | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---|-----------------------------------|---|-----|-----|-----|------|
| I _{Ikg} | Standard I/O input leakage current ⁽⁴⁾ | | V _{SS} ≤ V _{IN} ≤ V _{DD} | | | ±1 | μA |
| | FT I/O input leakage ⁽⁴⁾ | | V _{IN} = 5 V | | | 3 | |
| R _{PU} | Weak pull-up equivalent resistor ⁽⁵⁾ | All pins except for PA10 and PB12 | V _{IN} = V _{SS} | 30 | 40 | 50 | kΩ |
| | | PA10 and PB12 | | 8 | 11 | 15 | |
| R _{PD} | Weak pull-down equivalent resistor ⁽⁵⁾ | All pins except for PA10 and PB12 | V _{IN} = V _{DD} | 30 | 40 | 50 | kΩ |
| | | PA10 and PB12 | | 8 | 11 | 15 | |
| C _{IO} ⁽⁶⁾ | I/O pin capacitance | | | | 5 | | pF |

1. FT = Five-volt tolerant.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).
6. Guaranteed by design, not tested in production.

All I/Os are CMOS and TTL compliant (no software configuration required), their characteristics consider the most strict CMOS-technology or TTL parameters:

- For V_{IH}:
 - if V_{DD} is in the [2.00 V - 3.08 V] range: CMOS characteristics but TTL included
 - if V_{DD} is in the [3.08 V - 3.60 V] range: TTL characteristics but CMOS included
- For V_{IL}:
 - if V_{DD} is in the [2.00 V - 2.28 V] range: TTL characteristics but CMOS included
 - if V_{DD} is in the [2.28 V - 3.60 V] range: CMOS characteristics but TTL included

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink +20 mA (with a relaxed V_{OL}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 5.2](#):

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see [Table 8](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see [Table 8](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 41](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 10](#). All I/Os are CMOS and TTL compliant.

Table 41. Output voltage characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------------|---|---|--------------|-----|------|
| $V_{OL}^{(2)}$ | Output low level voltage for an I/O pin when 8 pins are sunk at same time | TTL port $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$ | | 0.4 | V |
| $V_{OH}^{(3)}$ | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}-0.4$ | | |
| $V_{OL}^{(2)}$ | Output low level voltage for an I/O pin when 8 pins are sunk at same time | CMOS port $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$ | | 0.4 | V |
| $V_{OH}^{(3)}$ | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | 2.4 | | |
| $V_{OL}^{(2)(4)}$ | Output low level voltage for an I/O pin when 8 pins are sunk at same time | $I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$ | | 1.3 | V |
| $V_{OH}^{(3)(4)}$ | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}-1.3$ | | |
| $V_{OL}^{(2)(4)}$ | Output low level voltage for an I/O pin when 8 pins are sunk at same time | $I_{IO} = +6 \text{ mA}$ $2 \text{ V} < V_{DD} < 2.7 \text{ V}$ | | 0.4 | V |
| $V_{OH}^{(3)(4)}$ | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}-0.4$ | | |

- PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
- The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 8](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
- The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 8](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
- Based on characterization data, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 27](#) and [Table 42](#), respectively.

Unless otherwise specified, the parameters given in [Table 42](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 10](#).

Table 42. I/O AC characteristics⁽¹⁾

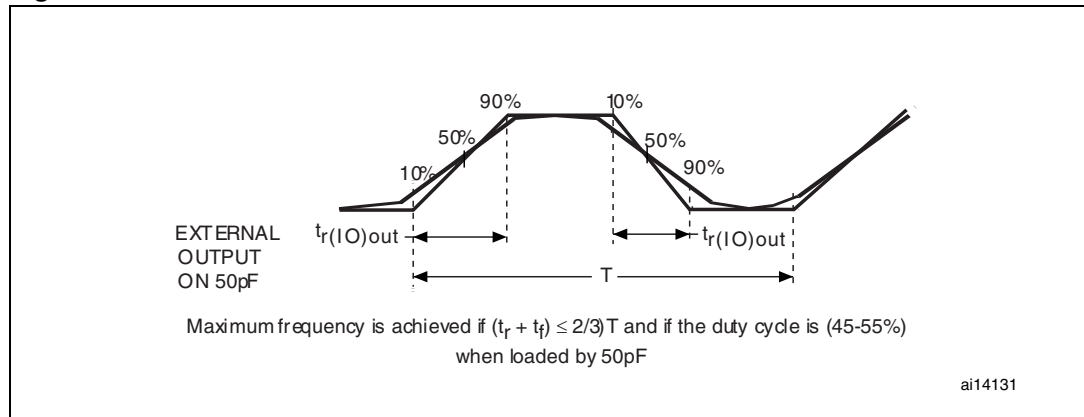
| OSPEEDRy [1:0] bit value ⁽¹⁾ | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|--------------------|------------------------------------|---|-----|-----|--------------------|------|
| 00 | $f_{\max(I/O)out}$ | Maximum frequency ⁽²⁾ | $C_L = 50 \text{ pF}$, $V_{DD} = 1.8 \text{ V}$ to 3.6 V | | | 2 | MHz |
| | $t_{f(I/O)out}$ | Output high to low level fall time | $C_L = 50 \text{ pF}$, $V_{DD} = 1.8 \text{ V}$ to 3.6 V | | | TBD ⁽³⁾ | ns |
| | $t_{r(I/O)out}$ | Output low to high level rise time | | | | TBD ⁽³⁾ | |

Table 42. I/O AC characteristics⁽¹⁾ (continued)

| OSPEEDRy [1:0] bit value ⁽¹⁾ | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---------------------------------|---|---|--------------------|-----|--------------------|------|
| 01 | $f_{\max(\text{IO})\text{out}}$ | Maximum frequency ⁽²⁾ | $C_L = 50 \text{ pF}, V_{DD} < 2.7 \text{ V}$ | 25 | | TBD | MHz |
| | | | $C_L = 10 \text{ pF}, V_{DD} > 2.7 \text{ V}$ | 25 | | 50 ⁽⁴⁾ | MHz |
| | $t_{f(\text{IO})\text{out}}$ | Output high to low level fall time | $C_L = 50 \text{ pF}, V_{DD} < 2.7 \text{ V}$ | | | TBD ⁽³⁾ | ns |
| | | | $C_L = 10 \text{ pF}, V_{DD} > 2.7 \text{ V}$ | | | TBD ⁽³⁾ | |
| | $t_{r(\text{IO})\text{out}}$ | Output low to high level rise time | $C_L = 50 \text{ pF}, V_{DD} < 2.7 \text{ V}$ | | | TBD ⁽³⁾ | |
| | | | $C_L = 10 \text{ pF}, V_{DD} > 2.7 \text{ V}$ | | | TBD ⁽³⁾ | |
| 10 | $f_{\max(\text{IO})\text{out}}$ | Maximum frequency ⁽²⁾ | $C_L = 50 \text{ pF}, 2.4 < V_{DD} < 2.7 \text{ V}$ | 50 ⁽⁴⁾ | | TBD | MHz |
| | | | $C_L = 10 \text{ pF}, V_{DD} > 2.7 \text{ V}$ | 50 ⁽⁴⁾ | | 100 ⁽⁴⁾ | MHz |
| | $t_{f(\text{IO})\text{out}}$ | Output high to low level fall time | $C_L = 50 \text{ pF}, 2.4 < V_{DD} < 2.7 \text{ V}$ | | | TBD ⁽³⁾ | ns |
| | | | $C_L = 10 \text{ pF}, V_{DD} > 2.7 \text{ V}$ | | | TBD ⁽³⁾ | |
| | $t_{r(\text{IO})\text{out}}$ | Output low to high level rise time | $C_L = 50 \text{ pF}, 2.4 < V_{DD} < 2.7 \text{ V}$ | | | TBD ⁽³⁾ | |
| | | | $C_L = 10 \text{ pF}, V_{DD} > 2.7 \text{ V}$ | | | TBD ⁽³⁾ | |
| 11 | $F_{\max(\text{IO})\text{out}}$ | Maximum frequency ⁽²⁾ | $C_L = 20 \text{ pF}, 2.4 < V_{DD} < 2.7 \text{ V}$ | 100 ⁽⁴⁾ | | TBD | MHz |
| | | | $C_L = 10 \text{ pF}, V_{DD} > 2.7 \text{ V}$ | 100 ⁽⁴⁾ | | 200 ⁽⁴⁾ | MHz |
| | $t_{f(\text{IO})\text{out}}$ | Output high to low level fall time | $C_L = 20 \text{ pF}, 2.4 < V_{DD} < 2.7 \text{ V}$ | | | TBD ⁽³⁾ | ns |
| | | | $C_L = 10 \text{ pF}, V_{DD} > 2.7 \text{ V}$ | | | TBD ⁽³⁾ | |
| | $t_{r(\text{IO})\text{out}}$ | Output low to high level rise time | $C_L = 20 \text{ pF}, 2.4 < V_{DD} < 2.7 \text{ V}$ | | | TBD ⁽³⁾ | |
| | | | $C_L = 10 \text{ pF}, V_{DD} > 2.7 \text{ V}$ | | | TBD ⁽³⁾ | |
| - | $t_{\text{EXTI}pw}$ | Pulse width of external signals detected by the EXTI controller | | 10 | | | ns |

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F20/21xxx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
2. The maximum frequency is defined in [Figure 27](#).
3. Guaranteed by design, not tested in production.
4. For maximum frequencies above 50 MHz, it is required to use the compensation cell.

Figure 27. I/O AC characteristics definition



5.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 40](#)).

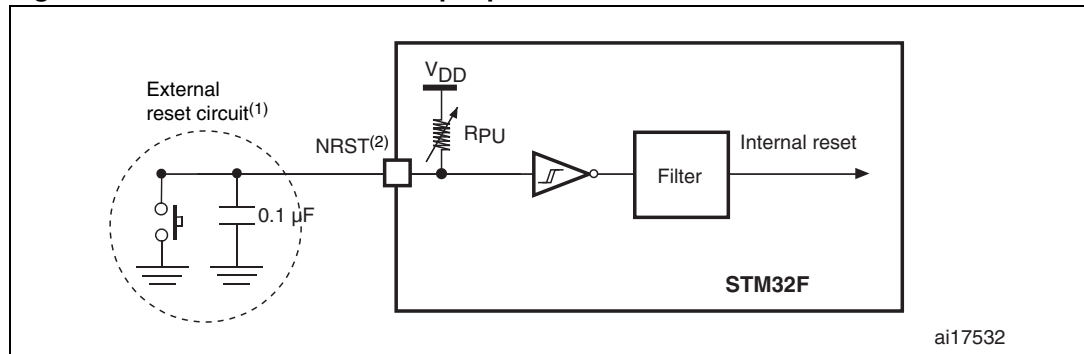
Unless otherwise specified, the parameters given in [Table 43](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 10](#).

Table 43. NRST pin characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|---|-----------------------|------|-----|--------------|------------|
| $V_{IL(NRST)}^{(1)}$ | NRST Input low level voltage | | -0.5 | | 0.8 | V |
| $V_{IH(NRST)}^{(1)}$ | NRST Input high level voltage | | 2 | | $V_{DD}+0.5$ | |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | | | 200 | | mV |
| R_{PU} | Weak pull-up equivalent resistor ⁽²⁾ | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | k Ω |
| $V_{F(NRST)}^{(1)}$ | NRST Input filtered pulse | | | | 100 | ns |
| $V_{NF(NRST)}^{(1)}$ | NRST Input not filtered pulse | $V_{DD} > 2.7 V$ | 300 | | | ns |
| T_{NRST_OUT} | Generated reset pulse duration | Internal Reset source | 20 | | | μs |

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 28. Recommended NRST pin protection



- 2. The reset network protects the device against parasitic resets.
- 3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 43. Otherwise the reset is not taken into account by the device.

5.3.16 TIM timer characteristics

The parameters given in Table 44 and Table 45 are guaranteed by design.

Refer to Section 5.3.14: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 44. Characteristics of TIMx connected to the APB1 domain⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|------------------|---|---|--------|-----------------|----------------------|---------------|
| $t_{res(TIM)}$ | Timer resolution time | $f_{TIMxCLK} = 60\text{ MHz}$ $APB1 = 30\text{ MHz}$ | 1 | | $t_{TIMxCLK}$ | |
| | | | 16.7 | | ns | |
| f_{EXT} | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}/2$ | MHz | |
| | | | 0 | 36 | MHz | |
| Res_{TIM} | Timer resolution | | | | 16 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected | | 1 | 65536 | $t_{TIMxCLK}$ | |
| | | | 0.0167 | 1092 | μs | |
| | 32-bit counter clock period when internal clock is selected | | 1 | | $t_{TIMxCLK}$ | |
| | | | 0.0167 | 71582788 | μs | |
| t_{MAX_COUNT} | Maximum possible count | | | | 65536×65536 | $t_{TIMxCLK}$ |
| | | | | 71.6 | s | |

1. TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, and TIM12 timers.

Table 45. Characteristics of TIMx connected to the APB2 domain⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------------|---|---|--------|-------------------------|----------------------|
| t _{res(TIM)} | Timer resolution time | f _{TIMxCLK} = 120 MHz APB2 = 60 MHz | 1 | | t _{TIMxCLK} |
| | | | 8.3 | | ns |
| f _{EXT} | Timer external clock frequency on CH1 to CH4 | | 0 | f _{TIMxCLK} /2 | MHz |
| | | | 0 | 30 | MHz |
| Res _{TIM} | Timer resolution | | | 16 | bit |
| t _{COUNTER} | 16-bit counter clock period when internal clock is selected | | 1 | 65536 | t _{TIMxCLK} |
| | | | 0.0083 | 546 | µs |
| t _{MAX_COUNT} | Maximum possible count | | | 65536 × 65536 | t _{TIMxCLK} |
| | | | 35.79 | s | |

1. TIMx is used as a general term to refer to the TIM1, TIM8, TIM9, TIM10, and TIM11 timers.

5.3.17 Communications interfaces

I²C interface characteristics

Unless otherwise specified, the parameters given in [Table 46](#) are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in [Table 10](#).

The STM32F21x and STM32F215xx I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

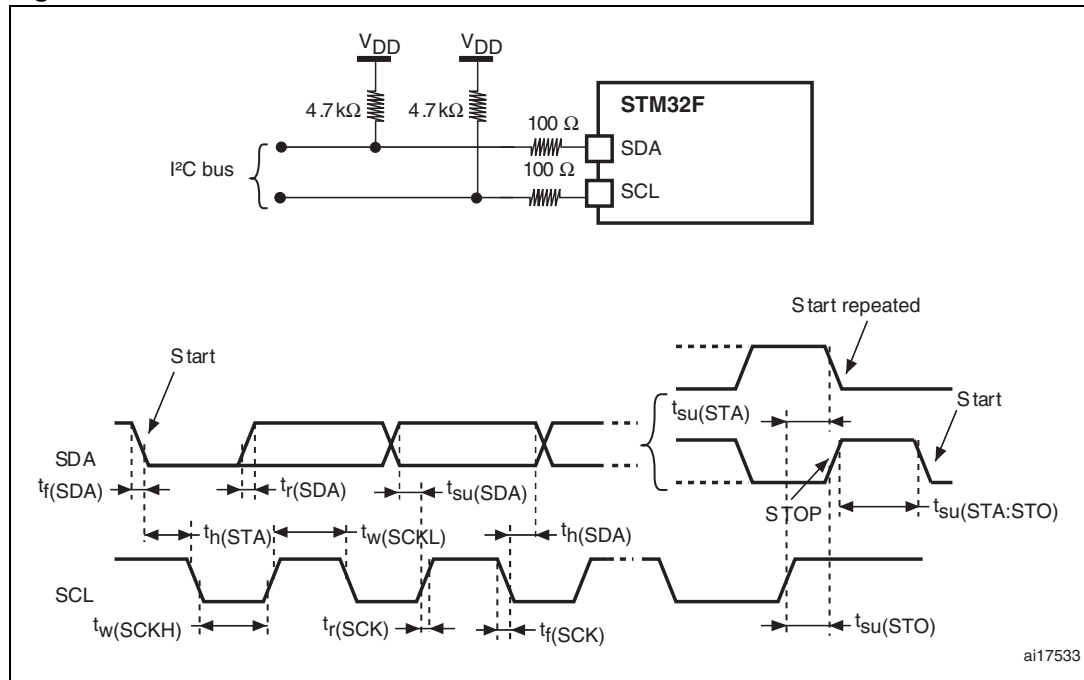
The I²C characteristics are described in [Table 46](#). Refer also to [Section 5.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

Table 46. I²C characteristics

| Symbol | Parameter | Standard mode I ² C ⁽¹⁾ | | Fast mode I ² C ⁽¹⁾⁽²⁾ | | Unit |
|------------------------------|---|---|------|--|--------------------|---------|
| | | Min | Max | Min | Max | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.3 | | μ s |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | |
| $t_{su(SDA)}$ | SDA setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 ⁽³⁾ | | 0 ⁽⁴⁾ | 900 ⁽³⁾ | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | $20 + 0.1C_b$ | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | | 300 | | 300 | |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | | 0.6 | | μ s |
| $t_{su(STA)}$ | Repeated Start condition setup time | 4.7 | | 0.6 | | |
| $t_{su(STO)}$ | Stop condition setup time | 4.0 | | 0.6 | | μ s |
| $t_{w(STO:STA)}$ | Stop to Start condition time (bus free) | 4.7 | | 1.3 | | μ s |
| C_b | Capacitive load for each bus line | | 400 | | 400 | pF |

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 4 MHz to achieve the maximum fast mode I²C frequency.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 29. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 47. SCL frequency ($f_{PCLK1} = 30 \text{ MHz}, V_{DD} = 3.3 \text{ V}$)⁽¹⁾⁽²⁾

| f _{SCL} (kHz) | I2C_CCR value |
|------------------------|-------------------------|
| | R _p = 4.7 kΩ |
| 400 | 0x8019 |
| 300 | 0x8021 |
| 200 | 0x8032 |
| 100 | 0x0096 |
| 50 | 0x012C |
| 20 | 0x02EE |

1. R_p = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

I²S - SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 48](#) for SPI or in [Table 49](#) for I²S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 10](#).

Refer to [Section 5.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 48. SPI characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--|----------------------------------|--|---------------------|---------------------|------|
| f _{SCK} 1/t _{c(SCK)} | SPI clock frequency | Master mode | | 30 | MHz |
| | | Slave mode | | 30 | |
| t _{r(SCK)} t _{f(SCK)} | SPI clock rise and fall time | Capacitive load: C = 30 pF | | 8 | ns |
| DuCy(SCK) | SPI slave input clock duty cycle | Slave mode | 30 | 70 | % |
| t _{su(NSS)} ⁽²⁾ | NSS setup time | Slave mode | 4 t _{PCLK} | | ns |
| t _{h(NSS)} ⁽²⁾ | NSS hold time | Slave mode | 2 t _{PCLK} | | |
| t _{w(SCKH)} ⁽²⁾ t _{w(SCKL)} ⁽²⁾ | SCK high and low time | Master mode, f _{PCLK} = 36 MHz, presc = 4 | 50 | 60 | |
| t _{su(MI)} ⁽²⁾ t _{su(SI)} ⁽²⁾ | Data input setup time | Master mode | 5 | | |
| | | Slave mode | 5 | | |
| t _{h(MI)} ⁽²⁾ t _{h(SI)} ⁽²⁾ | Data input hold time | Master mode | 5 | | |
| | | Slave mode | 4 | | |
| t _{a(SO)} ⁽²⁾⁽³⁾ | Data output access time | Slave mode, f _{PCLK} = 20 MHz | 0 | 3 t _{PCLK} | |
| t _{dis(SO)} ⁽²⁾⁽⁴⁾ | Data output disable time | Slave mode | 2 | 10 | |
| t _{v(SO)} ⁽²⁾⁽¹⁾ | Data output valid time | Slave mode (after enable edge) | | 25 | |
| t _{v(MO)} ⁽²⁾⁽¹⁾ | Data output valid time | Master mode (after enable edge) | | 5 | |
| t _{h(SO)} ⁽²⁾ t _{h(MO)} ⁽²⁾ | Data output hold time | Slave mode (after enable edge) | 15 | | |
| | | Master mode (after enable edge) | 2 | | |

1. Remapped SPI1 characteristics to be determined.
2. Based on characterization, not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 30. SPI timing diagram - slave mode and CPHA = 0

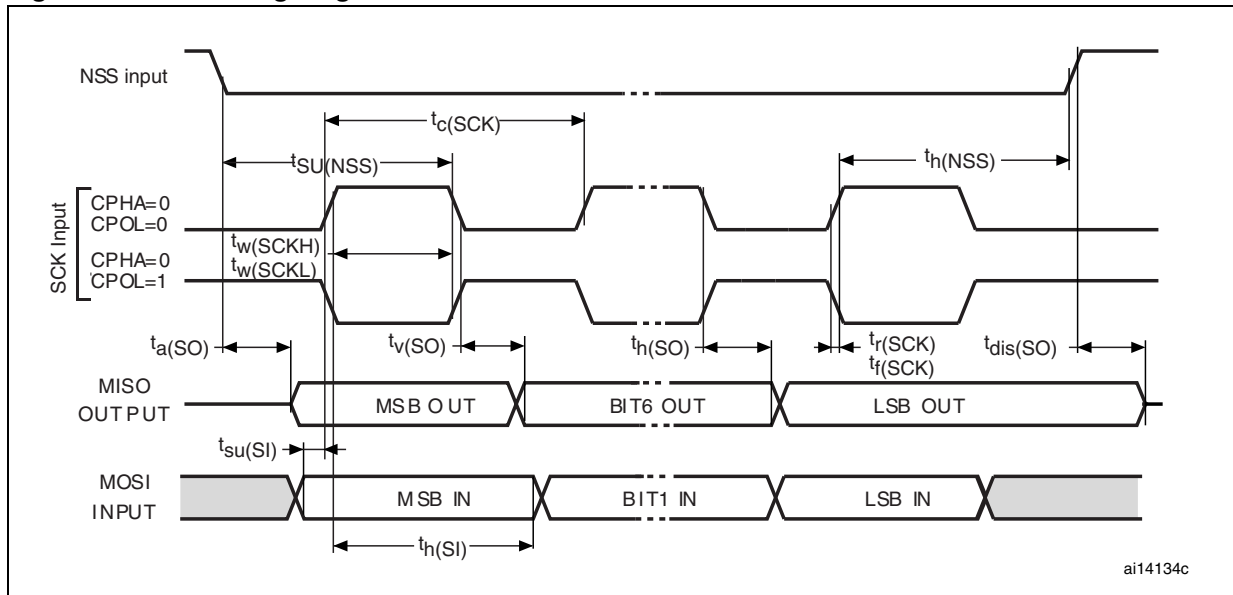
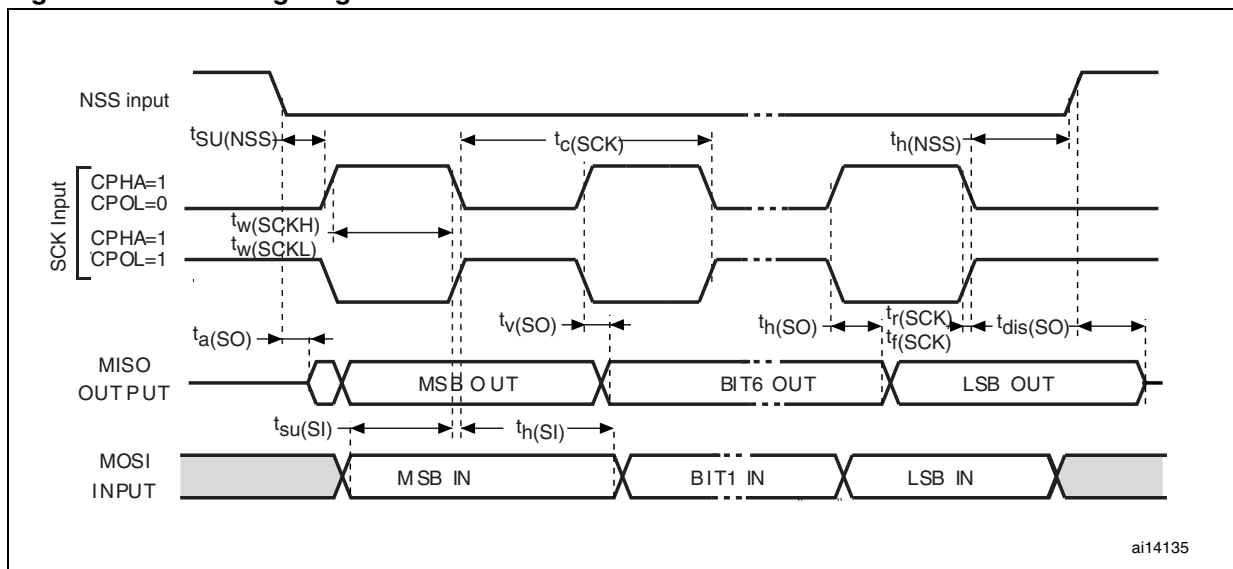
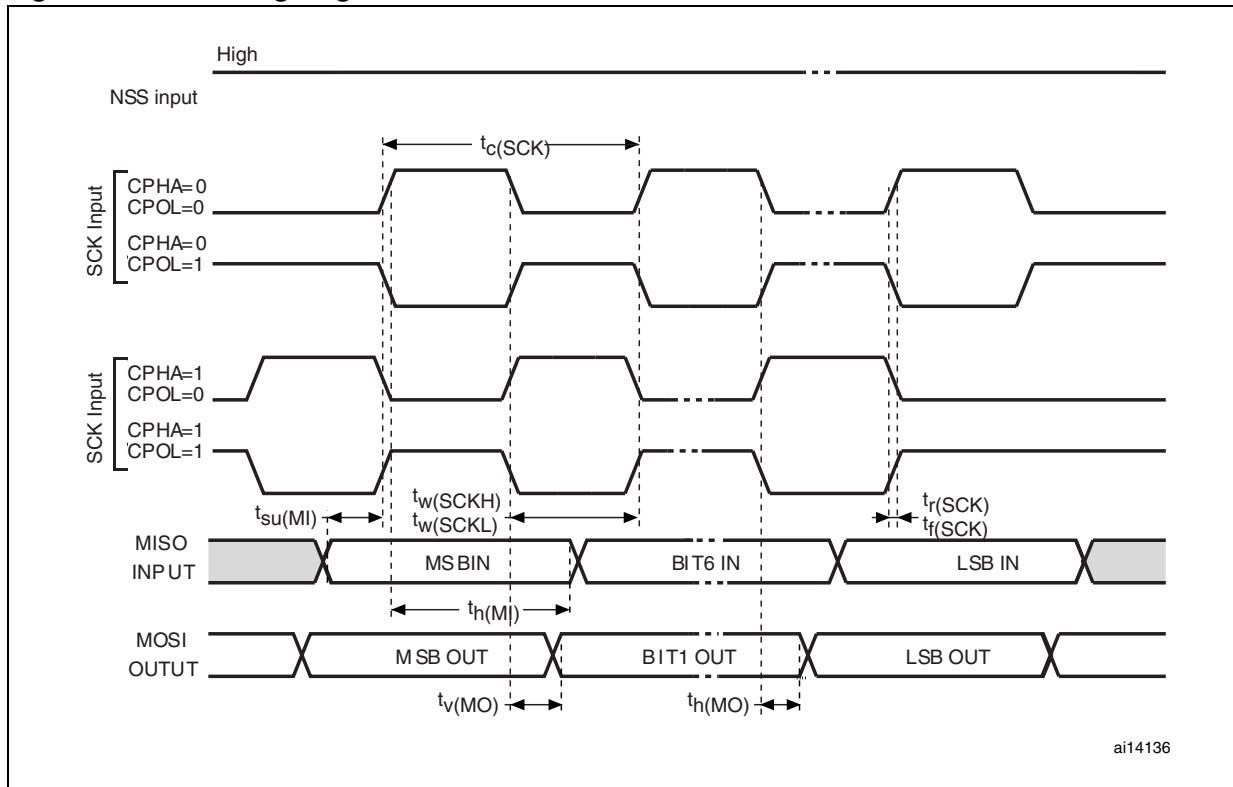


Figure 31. SPI timing diagram - slave mode and CPHA = 1⁽¹⁾



1. Measurement points are done at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.

Figure 32. SPI timing diagram - master mode⁽¹⁾



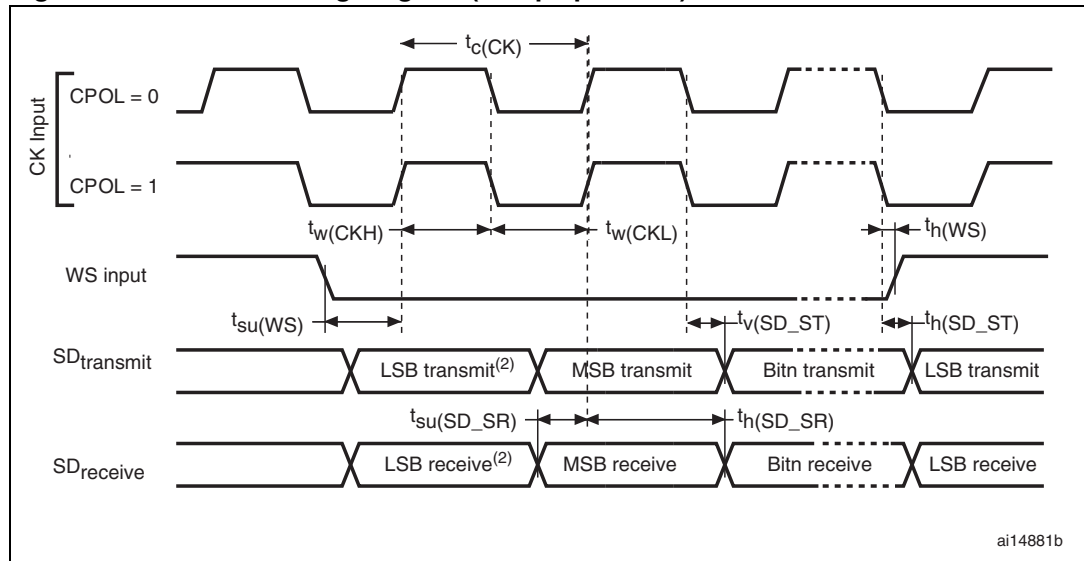
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 49. I²S characteristics (1)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--|---|---|------------|-----|------|
| f _{CK} 1/t _{c(CK)} | I ² S clock frequency | Master | TBD | TBD | MHz |
| | | Slave | 0 | TBD | |
| t _{r(CK)} t _{f(CK)} | I ² S clock rise and fall time | capacitive load C _L = 50 pF | | TBD | ns |
| t _{v(WS)} ⁽²⁾ | WS valid time | Master | TBD | | |
| t _{h(WS)} ⁽²⁾ | WS hold time | Master | TBD | | |
| t _{su(WS)} ⁽²⁾ | WS setup time | Slave | TBD | | |
| t _{h(WS)} ⁽²⁾ | WS hold time | Slave | TBD | | |
| t _{w(CKH)} ⁽²⁾ t _{w(CKL)} ⁽²⁾ | CK high and low time | Master f _{PCLK} = TBD, presc = TBD | TBD | | |
| t _{su(SD_MR)} ⁽²⁾ t _{su(SD_SR)} ⁽²⁾ | Data input setup time | Master receiver Slave receiver | TBD TBD | | |
| t _{h(SD_MR)} ⁽²⁾⁽³⁾ t _{h(SD_SR)} ⁽²⁾⁽³⁾ | Data input hold time | Master receiver Slave receiver | TBD TBD | | |
| t _{h(SD_MR)} ⁽²⁾ t _{h(SD_SR)} ⁽²⁾ | Data input hold time | Master f _{PCLK} = TBD Slave f _{PCLK} = TBD | TBD TBD | | |
| t _{v(SD_ST)} ⁽²⁾⁽³⁾ | Data output valid time | Slave transmitter (after enable edge) | | TBD | |
| | | f _{PCLK} = TBD | | TBD | |
| t _{h(SD_ST)} ⁽²⁾ | Data output hold time | Slave transmitter (after enable edge) | TBD | | |
| t _{v(SD_MT)} ⁽²⁾⁽³⁾ | Data output valid time | Master transmitter (after enable edge) | | TBD | |
| | | f _{PCLK} = TBD | TBD | TBD | |
| t _{h(SD_MT)} ⁽²⁾ | Data output hold time | Master transmitter (after enable edge) | TBD | | |

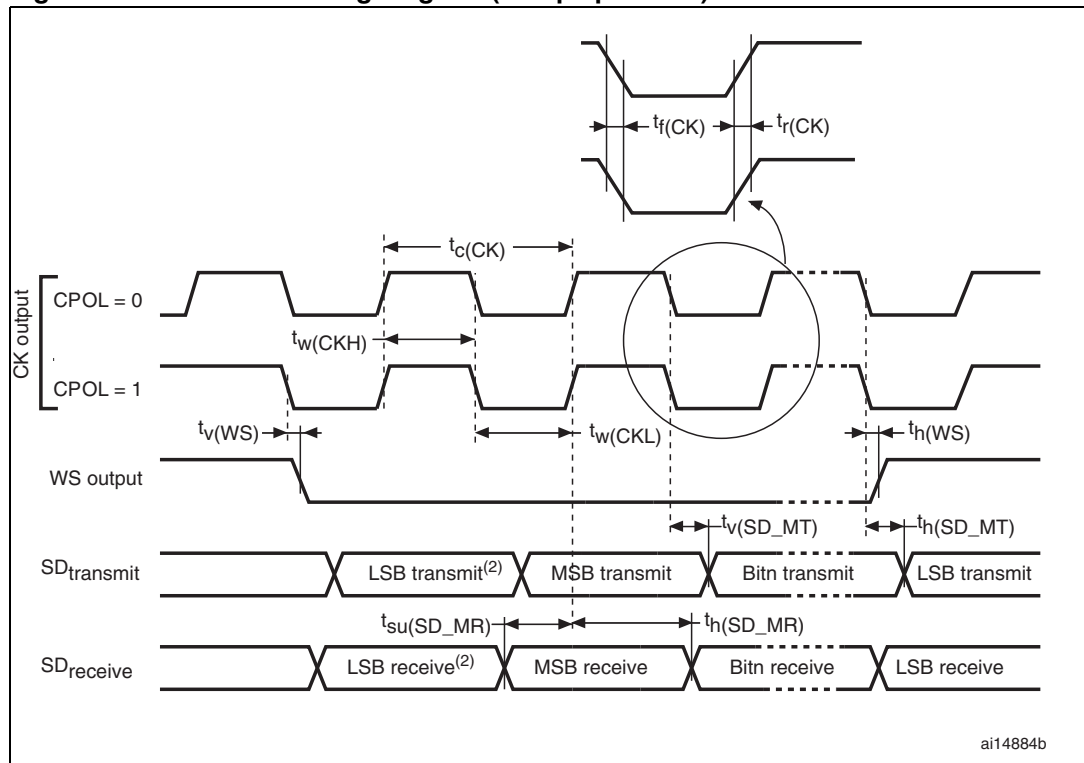
1. TBD = to be determined.
2. Based on design simulation and/or characterization results, not tested in production.
3. Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = 1/f_{PCLK} =125 ns.

Figure 33. I²S slave timing diagram (Philips protocol)⁽¹⁾



1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 34. I²S master timing diagram (Philips protocol)⁽¹⁾



1. Based on characterization, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USB OTG FS characteristics

The USB OTG interface is USB-IF certified (Full-Speed). This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 50. USB OTG FS startup time

| Symbol | Parameter | Max | Unit |
|----------------------------|-------------------------------------|-----|---------------|
| $t_{\text{STARTUP}}^{(1)}$ | USB OTG FS transceiver startup time | 1 | μs |

1. Guaranteed by design, not tested in production.

Table 51. USB OTG FS DC electrical characteristics

| Symbol | Parameter | Conditions | Min. ⁽¹⁾ | Typ. | Max. ⁽¹⁾ | Unit |
|----------------------|---|---------------------------------|--|------|---------------------|------------|
| Input levels | V_{DD} | USB OTG FS operating voltage | 3.0 ⁽²⁾ | | 3.6 | V |
| | $V_{\text{DI}}^{(3)}$ | Differential input sensitivity | I(USB_FS_DP/DM, USB_HS_DP/DM) | 0.2 | | V |
| | $V_{\text{CM}}^{(3)}$ | Differential common mode range | Includes V_{DI} range | 0.8 | 2.5 | |
| | $V_{\text{SE}}^{(3)}$ | Single ended receiver threshold | | 1.3 | 2.0 | |
| Output levels | V_{OL} | Static output level low | R_{L} of 1.5 k Ω to 3.6 V ⁽⁴⁾ | | 0.3 | V |
| | V_{OH} | Static output level high | R_{L} of 15 k Ω to $V_{\text{SS}}^{(4)}$ | 2.8 | 3.6 | |
| R_{PD} | PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM) | $V_{\text{IN}} = V_{\text{DD}}$ | 17 | 21 | 24 | k Ω |
| | PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS) | | 0.65 | 1.1 | 2.0 | |
| R_{PU} | PA12, PB15 (USB_FS_DP, USB_HS_DP) | $V_{\text{IN}} = V_{\text{SS}}$ | 1.5 | 1.8 | 2.1 | |
| | PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS) | $V_{\text{IN}} = V_{\text{SS}}$ | 0.25 | 0.37 | 0.55 | |

1. All the voltages are measured from the local ground potential.
2. The STM32F21x and STM32F215xx USB OTG FS functionality is ensured down to 2.7 V but not the full USB OTG FS electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design, not tested in production.
4. R_{L} is the load connected on the USB OTG FS drivers

Figure 35. USB OTG FS timings: definition of data signal rise and fall time

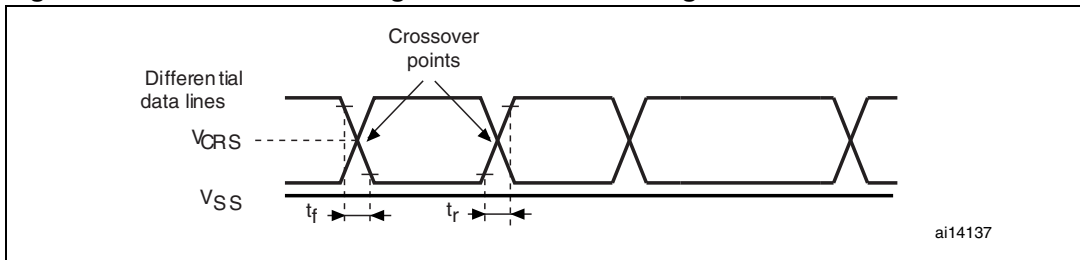


Table 52. USB OTG FS electrical characteristics⁽¹⁾

| Driver characteristics | | | | | |
|------------------------|---------------------------------|-----------------------|-----|-----|------|
| Symbol | Parameter | Conditions | Min | Max | Unit |
| t_r | Rise time ⁽²⁾ | $C_L = 50 \text{ pF}$ | 4 | 20 | ns |
| t_f | Fall time ⁽²⁾ | $C_L = 50 \text{ pF}$ | 4 | 20 | ns |
| t_{rfm} | Rise/ fall time matching | t_r/t_f | 90 | 110 | % |
| V_{CRS} | Output signal crossover voltage | | 1.3 | 2.0 | V |

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

USB HS characteristics

Table 53. Clock timing parameters

| Parameter ⁽¹⁾ | | Symbol | Min | Nominal | Max | Unit |
|--|------------------|-------------------|--------|---------|--------|---------------|
| Frequency (first transition) | 8-bit $\pm 10\%$ | F_{START_8BIT} | 54 | 60 | 66 | MHz |
| Frequency (steady state) $\pm 500 \text{ ppm}$ | | F_{STEADY} | 59.97 | 60 | 60.03 | MHz |
| Duty cycle (first transition) | 8-bit $\pm 10\%$ | D_{START_8BIT} | 40 | 50 | 60 | % |
| Duty cycle (steady state) $\pm 500 \text{ ppm}$ | | D_{STEADY} | 49.975 | 50 | 50.025 | % |
| Time to reach the steady state frequency and duty cycle after the first transition | | T_{STEADY} | | | 1.4 | ms |
| Clock startup time after the de-assertion of SuspendM | Peripheral | T_{START_DEV} | | | 5.6 | ms |
| | Host | T_{START_HOST} | | | | |
| PHY preparation time after the first transition of the input clock | | T_{PREP} | | | | μs |
| Jitter | | T_{JITTER} | | | | ps |
| Rise time | | T_{RISE} | | | | ns |
| Fall time | | T_{FALL} | | | | |

1. Guaranteed by design, not tested in production.

Figure 36. ULPI timing diagram

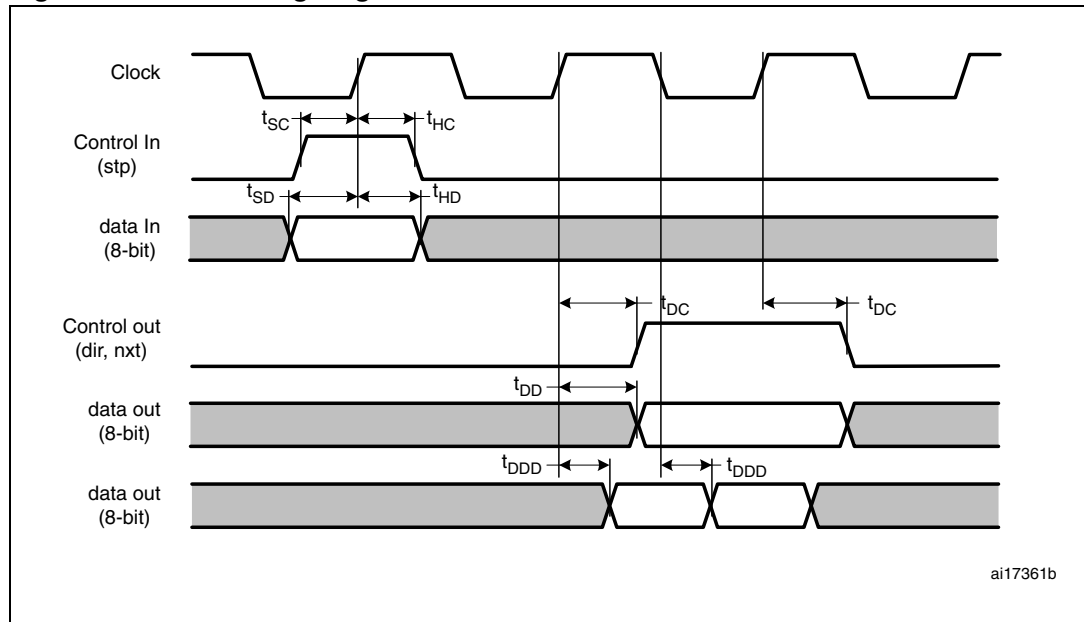


Table 54. ULPI timing

| Parameter | | Symbol | Value ⁽¹⁾ | | Unit |
|------------------------|----------------------------|------------------|----------------------|------|------|
| | | | Min. | Max. | |
| Output clock | Setup time (control in) | t_{SC}, t_{SD} | | 6.0 | ns |
| | Hold time (control in) | t_{HC}, t_{HD} | 0.0 | | ns |
| | Output delay (control out) | t_{DC}, t_{DD} | | 9.0 | ns |
| Input clock (optional) | Setup time (control in) | t_{SC}, t_{SD} | | 3.0 | ns |
| | Hold time (control in) | t_{HC}, t_{HD} | 1.5 | | ns |
| | Output delay (control out) | t_{DC}, t_{DD} | | 6.0 | ns |

1. $V_{DD} = 3\text{ V to }3.6\text{ V}$ and $T_A = -40\text{ to }85\text{ }^\circ\text{C}$.

Ethernet characteristics

Table 55 shows the Ethernet operating voltage.

Table 55. Ethernet DC electrical characteristics

| Symbol | | Parameter | Min. ⁽¹⁾ | Max. ⁽¹⁾ | Unit |
|-------------|----------|----------------------------|---------------------|---------------------|------|
| Input level | V_{DD} | Ethernet operating voltage | 3.0 | 3.6 | V |

1. All the voltages are measured from the local ground potential.

Table 56 gives the list of Ethernet MAC signals for the SMI (station management interface) and Figure 37 shows the corresponding timing diagram.

Figure 37. Ethernet SMI timing diagram

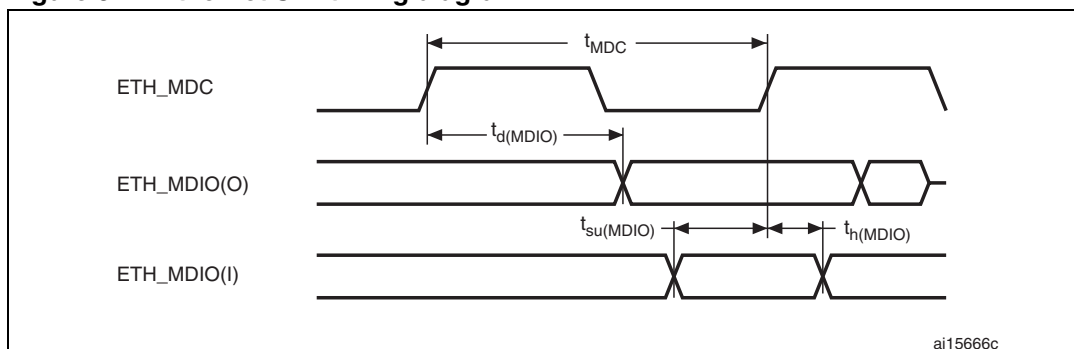


Table 56. Dynamics characteristics: Ethernet MAC signals for SMI⁽¹⁾

| Symbol | Rating | Min | Typ | Max | Unit |
|----------------|---|-----|-----|-----|------|
| t_{MDC} | MDC cycle time (1.71 MHz, AHB = 72 MHz) | TBD | TBD | TBD | ns |
| $t_{d(MDIO)}$ | MDIO write data valid time | TBD | TBD | TBD | ns |
| $t_{su(MDIO)}$ | Read data setup time | TBD | TBD | TBD | ns |
| $t_{h(MDIO)}$ | Read data hold time | TBD | TBD | TBD | ns |

1. TBD stands for to be determined.

Table 57 gives the list of Ethernet MAC signals for the RMII and Figure 38 shows the corresponding timing diagram.

Figure 38. Ethernet RMII timing diagram

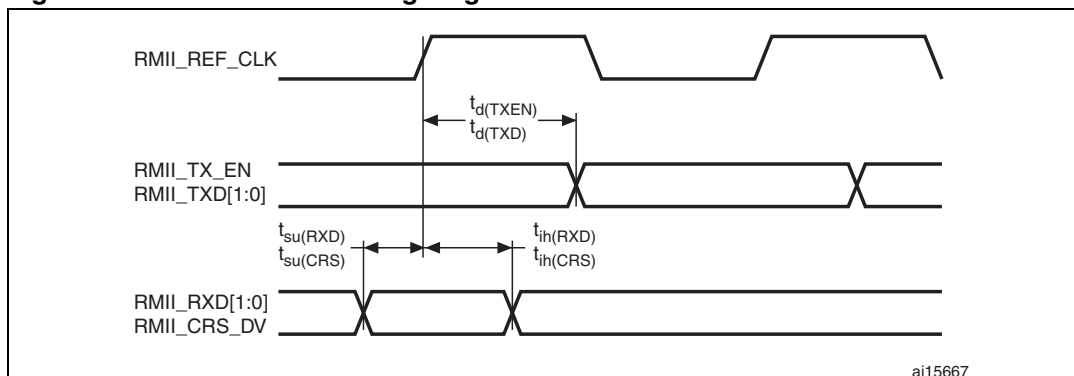


Table 57. Dynamics characteristics: Ethernet MAC signals for RMII⁽¹⁾

| Symbol | Rating | Min | Typ | Max | Unit |
|---------------|----------------------------------|-----|-----|------|------|
| $t_{su(RXD)}$ | Receive data setup time | TBD | TBD | TBD | ns |
| $t_{h(RXD)}$ | Receive data hold time | TBD | TBD | TBD | ns |
| $t_{su(CRS)}$ | Carrier sense set-up time | TBD | TBD | TBD | ns |
| $t_{h(CRS)}$ | Carrier sense hold time | TBD | TBD | TBD | ns |
| $t_{d(TXEN)}$ | Transmit enable valid delay time | 0 | 9.6 | 21.9 | ns |
| $t_{d(TXD)}$ | Transmit data valid delay time | 0 | 9.9 | 21 | ns |

1. TBD stands for to be determined.

Table 58 gives the list of Ethernet MAC signals for MII and Figure 38 shows the corresponding timing diagram.

Figure 39. Ethernet MII timing diagram

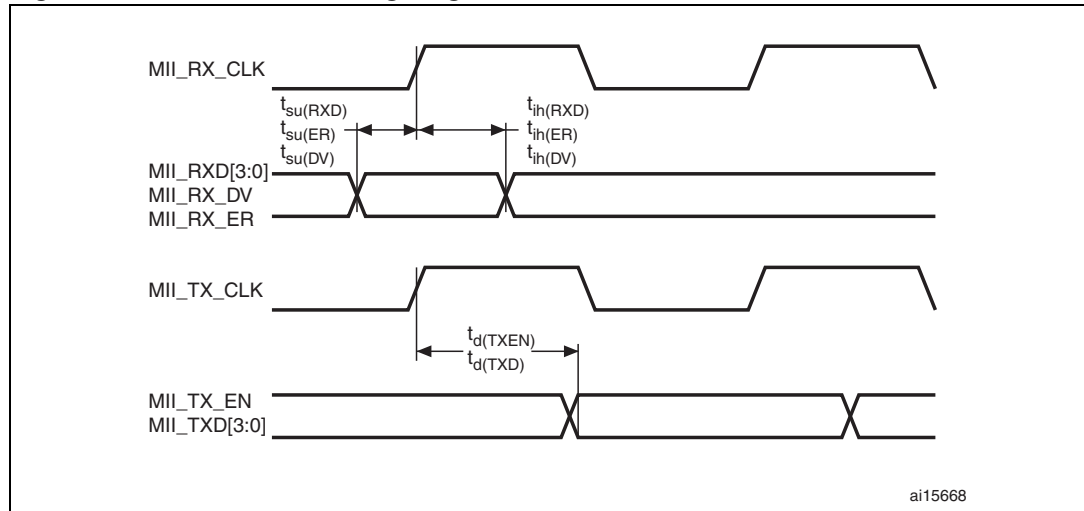


Table 58. Dynamics characteristics: Ethernet MAC signals for MII⁽¹⁾

| Symbol | Rating | Min | Typ | Max | Unit |
|---------------|----------------------------------|------|------|------|------|
| $t_{su}(RXD)$ | Receive data setup time | TBD | TBD | TBD | ns |
| $t_{oh}(RXD)$ | Receive data hold time | TBD | TBD | TBD | ns |
| $t_{su}(DV)$ | Data valid setup time | TBD | TBD | TBD | ns |
| $t_{oh}(DV)$ | Data valid hold time | TBD | TBD | TBD | ns |
| $t_{su}(ER)$ | Error setup time | TBD | TBD | TBD | ns |
| $t_{oh}(ER)$ | Error hold time | TBD | TBD | TBD | ns |
| $t_d(TXEN)$ | Transmit enable valid delay time | 13.4 | 15.5 | 17.7 | ns |
| $t_d(TXD)$ | Transmit data valid delay time | 12.9 | 16.1 | 19.4 | ns |

1. TBD stands for to be determined.

CAN (controller area network) interface

Refer to Section 5.3.14: I/O port characteristics for more details on the input/output alternate function characteristics (CANTX and CANRX).

5.3.18 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 59](#) are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in [Table 10](#).

Table 59. ADC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---|---|---|--------------------|--------------------|-------------|
| V_{DDA} | Power supply | | 1.8 | | 3.6 | V |
| V_{REF+} | Positive reference voltage | | 1.65 | | V_{DDA} | V |
| I_{VREF} | Current on the V_{REF} input pin | | | 160 ⁽¹⁾ | 220 ⁽¹⁾ | μ A |
| f_{ADC} | ADC clock frequency | $V_{DDA} = 1.8$ to 2.4 V | 0.6 | | 15 | MHz |
| | | $V_{DDA} = 2.4$ to 3.6 V | 0.6 | | 30 | MHz |
| $f_{TRIG}^{(1)}$ | External trigger frequency | $f_{ADC} = 30$ MHz | | | 823 | kHz |
| | | | | | 17 | $1/f_{ADC}$ |
| V_{AIN} | Conversion voltage range ⁽²⁾ | | 0 (V_{SSA} or V_{REF-} tied to ground) | | V_{REF+} | V |
| $R_{AIN}^{(1)}$ | External input impedance | See Equation 1 for details | | | 50 | k Ω |
| $R_{ADC}^{(1)}$ | Sampling switch resistance | | | | 1 | k Ω |
| $C_{ADC}^{(1)}$ | Internal sample and hold capacitor | | | | 8 | pF |
| $t_{lat}^{(1)}$ | Injection trigger conversion latency | $f_{ADC} = 30$ MHz | | | 0.100 | μ s |
| | | | | | 3 ⁽³⁾ | $1/f_{ADC}$ |
| $t_{latr}^{(1)}$ | Regular trigger conversion latency | $f_{ADC} = 30$ MHz | | | 0.067 | μ s |
| | | | | | 2 ⁽³⁾ | $1/f_{ADC}$ |
| $t_S^{(1)}$ | Sampling time | $f_{ADC} = 30$ MHz | 0.100 | | 16 | μ s |
| | | | 3 | | 480 | $1/f_{ADC}$ |
| $t_{STAB}^{(1)}$ | Power-up time | | 0 | 0 | 1 | μ s |
| $t_{CONV}^{(1)}$ | Total conversion time (including sampling time) | $f_{ADC} = 30$ MHz 12-bit resolution | 0.5 | | 16.40 | μ s |
| | | $f_{ADC} = 30$ MHz 10-bit resolution | 0.43 | | 16.34 | μ s |
| | | $f_{ADC} = 30$ MHz 8-bit resolution | 0.37 | | 16.27 | μ s |
| | | $f_{ADC} = 30$ MHz 6-bit resolution | 0.3 | | 16.20 | μ s |
| | | 9 to 492 (t_S for sampling +n-bit resolution for successive approximation) | | | | |

Table 59. ADC characteristics (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|--|---|-----|-----|-----|---------------|
| $f_S^{(1)}$ | Sampling rate ($f_{ADC} = 30\text{ MHz}$) | 12-bit resolution Single ADC | | | 2 | Msp/s |
| | | 12-bit resolution Interleave Dual ADC mode | | | 4 | Msp/s |
| | | 12-bit resolution Interleave Triple ADC mode | | | 6 | Msp/s |
| I_{VREF+} | ADC V_{REF+} DC current consumption in conversion mode | $f_{ADC} = 30\text{ MHz}$ 3 sampling time 12-bit resolution | | | TBD | μA |
| | | $f_{ADC} = 30\text{ MHz}$ 480 sampling time 12-bit resolution | | | TBD | μA |
| I_{DDA} | ADC V_{DDA} DC current consumption in conversion mode | $f_{ADC} = 30\text{ MHz}$ 3 sampling time 12-bit resolution | | | TBD | μA |
| | | $f_{ADC} = 30\text{ MHz}$ 480 sampling time 12-bit resolution | | | TBD | μA |

1. Based on characterization, not tested in production.
2. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA} .
3. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in [Table 59](#).

Equation 1: R_{AIN} max formula

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here $N = 12$ (from 12-bit resolution).

Table 60. ADC accuracy ⁽¹⁾

| Symbol | Parameter | Test conditions | Typ | Max ⁽²⁾ | Unit |
|--------|------------------------------|--|-----------|--------------------|------|
| ET | Total unadjusted error | $f_{PCLK2} = 60\text{ MHz}$, $f_{ADC} = 30\text{ MHz}$, $R_{AIN} < 10\text{ k}\Omega$, $V_{DDA} = 1.8\text{ V to }3.6\text{ V}$ | ± 2 | ± 5 | LSB |
| EO | Offset error | | ± 1.5 | ± 2.5 | |
| EG | Gain error | | ± 1.5 | ± 3 | |
| ED | Differential linearity error | | ± 1 | ± 2 | |
| EL | Integral linearity error | | ± 1.5 | ± 3 | |

1. Better performance could be achieved in restricted V_{DD} , frequency and temperature ranges.
2. Based on characterization, not tested in production.

Note: ADC accuracy vs. negative injection current: Injecting a negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to

add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 5.3.14](#) does not affect the ADC accuracy.

Figure 40. ADC accuracy characteristics

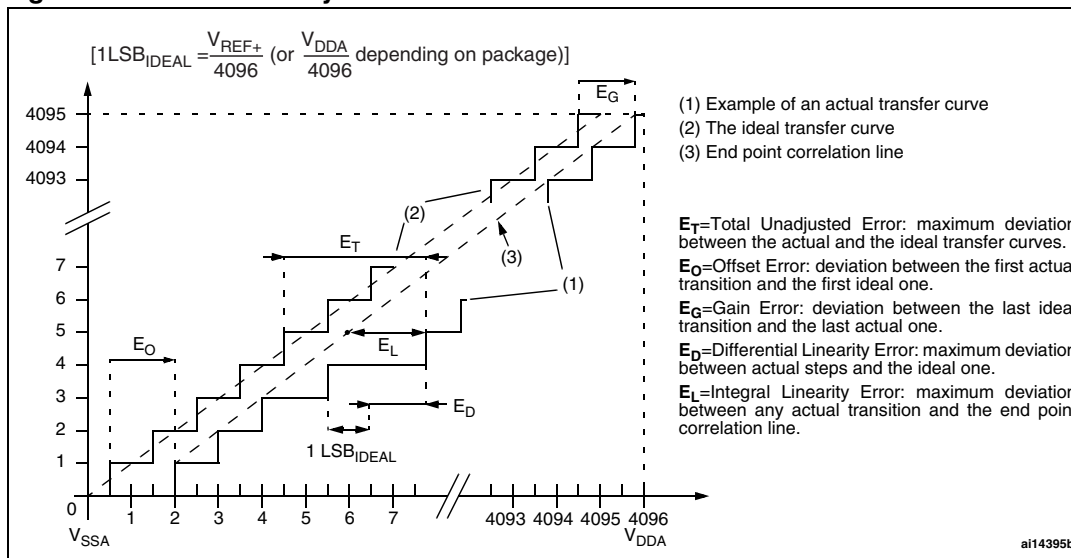
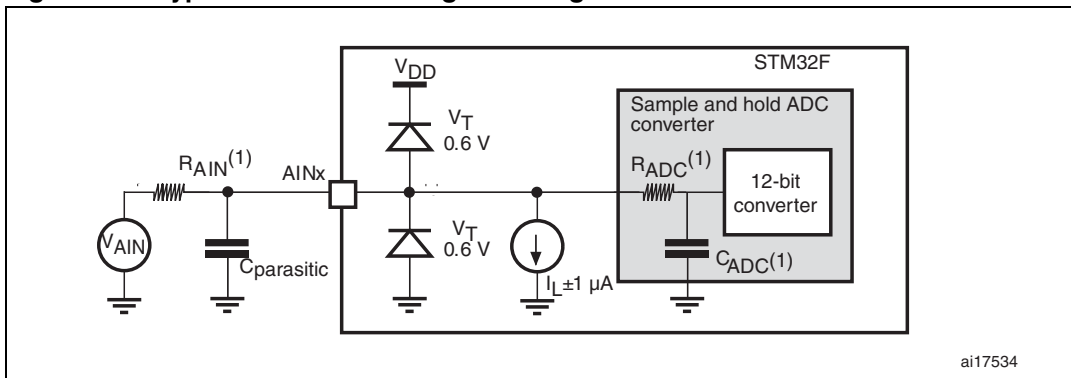


Figure 41. Typical connection diagram using the ADC

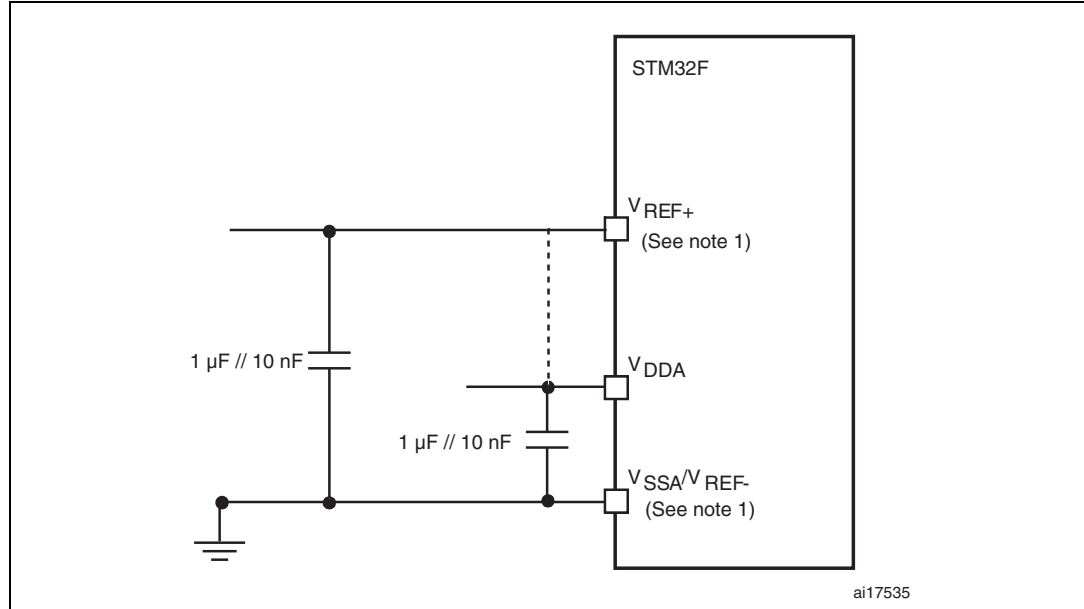


1. Refer to [Table 59](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

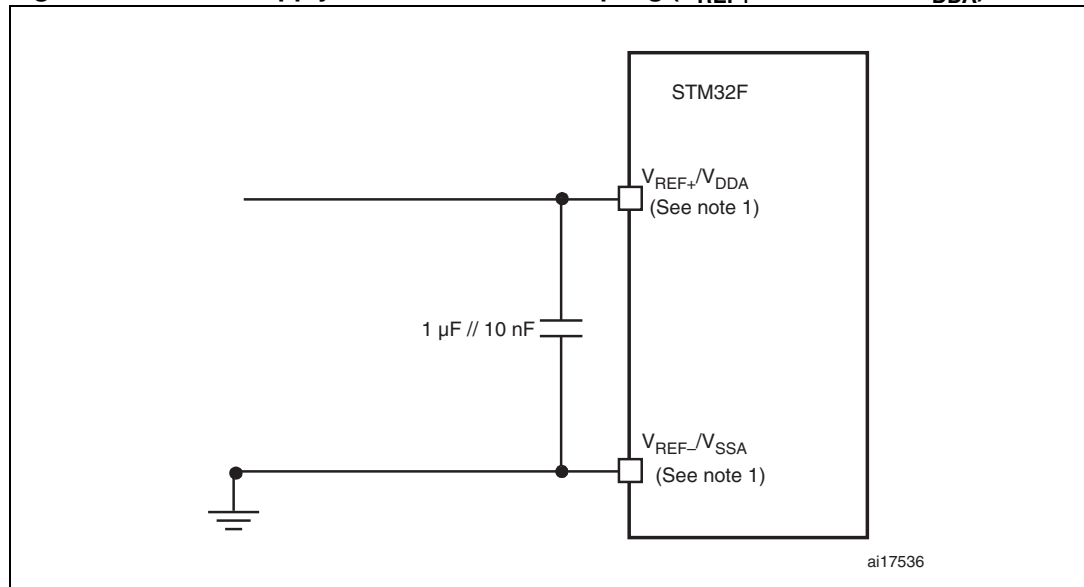
Power supply decoupling should be performed as shown in [Figure 42](#) or [Figure 43](#), depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 42. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Figure 43. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.19 DAC electrical specifications

Table 61. DAC characteristics

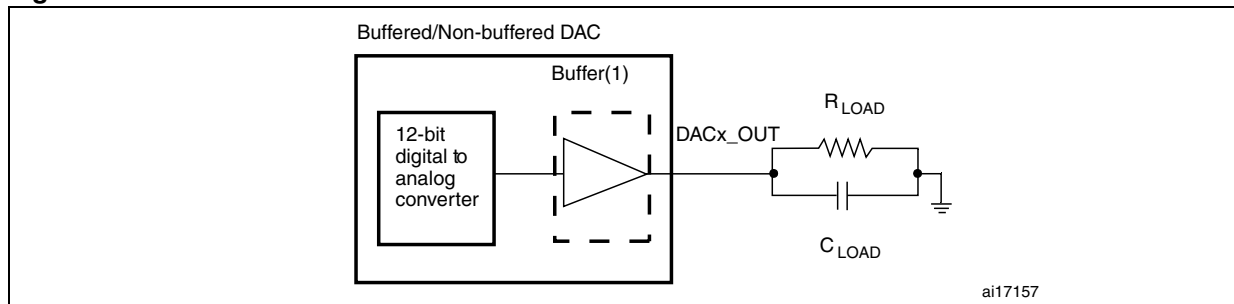
| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|------------------------|---|-----|-----|-------------------|------------|--|
| V_{DDA} | Analog supply voltage | 1.8 | | 3.6 | V | |
| V_{REF+} | Reference supply voltage | 1.8 | | 3.6 | V | $V_{REF+} \leq V_{DDA}$ |
| V_{SSA} | Ground | 0 | | 0 | V | |
| $R_{LOAD}^{(1)}$ | Resistive load with buffer ON | 5 | | | k Ω | |
| $R_O^{(1)}$ | Impedance output with buffer OFF | | | 15 | k Ω | When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 M Ω |
| $C_{LOAD}^{(1)}$ | Capacitive load | | | 50 | pF | Maximum capacitive load at DAC_OUT pin (when the buffer is ON). |
| $DAC_OUT_{min}^{(1)}$ | Lower DAC_OUT voltage with buffer ON | 0.2 | | | V | It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{REF+} = 3.6$ V and (0x1C7) to (0xE38) at $V_{REF+} = 1.8$ V |
| $DAC_OUT_{max}^{(1)}$ | Higher DAC_OUT voltage with buffer ON | | | $V_{DDA} - 0.2$ | V | |
| $DAC_OUT_{min}^{(1)}$ | Lower DAC_OUT voltage with buffer OFF | | 0.5 | | mV | It gives the maximum output excursion of the DAC. |
| $DAC_OUT_{max}^{(1)}$ | Higher DAC_OUT voltage with buffer OFF | | | $V_{REF+} - 1LSB$ | V | |
| I_{VREF+} | DAC DC V_{REF} current consumption in quiescent mode (Standby mode) | | | 220 | μ A | With no load, worst code (0xF1C) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs |
| I_{DDA} | DAC DC V_{DDA} current consumption in quiescent mode (Standby mode) | | | 380 | μ A | With no load, middle code (0x800) on the inputs |
| | | | | 480 | μ A | With no load, worst code (0xF1C) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs |
| $DNL^{(2)}$ | Differential non linearity Difference between two consecutive code-1LSB) | | | ± 0.5 | LSB | Given for the DAC in 10-bit configuration. |
| | | | | ± 2 | LSB | Given for the DAC in 12-bit configuration. |
| $INL^{(2)}$ | Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023) | | | ± 1 | LSB | Given for the DAC in 10-bit configuration. |
| | | | | ± 4 | LSB | Given for the DAC in 12-bit configuration. |

Table 61. DAC characteristics (continued)

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|-------------------------------|--|-----|-----|------|------|---|
| Offset ⁽²⁾ | Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$) | | | ±10 | mV | Given for the DAC in 12-bit configuration |
| | | | | ±3 | LSB | Given for the DAC in 10-bit at $V_{REF+} = 3.6\text{ V}$ |
| | | | | ±12 | LSB | Given for the DAC in 12-bit at $V_{REF+} = 3.6\text{ V}$ |
| Gain error ⁽²⁾ | Gain error | | | ±0.5 | % | Given for the DAC in 12bit configuration |
| $t_{SETTLING}$ ⁽²⁾ | Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±4LSB) | | 3 | 4 | µs | $C_{LOAD} \leq 50\text{ pF}$, $R_{LOAD} \geq 5\text{ k}\Omega$ |
| THD ⁽²⁾ | Total Harmonic Distortion Buffer ON | | | | dB | $C_{LOAD} \leq 50\text{ pF}$, $R_{LOAD} \geq 5\text{ k}\Omega$ |
| Update rate ⁽¹⁾ | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | | | 1 | MS/s | $C_{LOAD} \leq 50\text{ pF}$, $R_{LOAD} \geq 5\text{ k}\Omega$ |
| t_{WAKEUP} ⁽²⁾ | Wakeup time from off state (Setting the ENx bit in the DAC Control register) | | 6.5 | 10 | µs | $C_{LOAD} \leq 50\text{ pF}$, $R_{LOAD} \geq 5\text{ k}\Omega$ input code between lowest and highest possible ones. |
| PSRR+ ⁽¹⁾ | Power supply rejection ratio (to V_{DDA}) (static DC measurement) | | -67 | -40 | dB | No R_{LOAD} , $C_{LOAD} = 50\text{ pF}$ |

1. Guaranteed by design, not tested in production.
2. Guaranteed by characterization, not tested in production.

Figure 44. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.20 Temperature sensor characteristics

Table 62. TS characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------------|---|-----|---------|---------|------------------------|
| $T_L^{(1)}$ | V_{SENSE} linearity with temperature | | ± 1 | ± 2 | $^{\circ}\text{C}$ |
| Avg_Slope ⁽¹⁾ | Average slope | | 2.5 | | mV/ $^{\circ}\text{C}$ |
| $V_{25}^{(1)}$ | Voltage at 25 $^{\circ}\text{C}$ | | 0.76 | | V |
| $t_{START}^{(2)}$ | Startup time | 4 | | 10 | μs |
| $T_{S_temp}^{(3)(2)}$ | ADC sampling time when reading the temperature 1 $^{\circ}\text{C}$ accuracy | 16 | | | μs |

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

5.3.21 V_{BAT} monitoring characteristics

Table 63. V_{BAT} monitoring characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------------|--|-----|-----|-----|---------------|
| $R^{(1)}$ | Resistor bridge for V_{BAT} | | TBD | | K Ω m |
| $Q^{(1)}$ | Ratio on V_{BAT} measurement | | 2 | | |
| $E_r^{(1)}$ | Error on Q | -1 | | +1 | % |
| $T_{S_vbat}^{(2)(2)}$ | ADC sampling time when reading the V_{BAT} 1mV accuracy | TBD | | | μs |

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

5.3.22 Embedded reference voltage

The parameters given in [Table 64](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 10](#).

Table 64. Embedded internal reference voltage

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|---|--|------|------|--------------------|---------------|
| V_{REFINT} | Internal reference voltage | $-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$ | 1.16 | 1.20 | 1.26 | V |
| | | $-40\text{ }^{\circ}\text{C} < T_A < +85\text{ }^{\circ}\text{C}$ | 1.16 | 1.20 | 1.24 | V |
| $T_{S_vrefint}^{(1)}$ | ADC sampling time when reading the internal reference voltage | | | 5.1 | TBD ⁽²⁾ | μs |

Table 64. Embedded internal reference voltage

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|--|---|-----|-----|-----|--------|
| $V_{\text{RERINT}}^{(2)}$ | Internal reference voltage spread over the temperature range | $V_{\text{DD}} = 3 \text{ V} \pm 10 \text{ mV}$ | | | 10 | mV |
| $T_{\text{Coeff}}^{(2)}$ | Temperature coefficient | | | | 100 | ppm/°C |

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

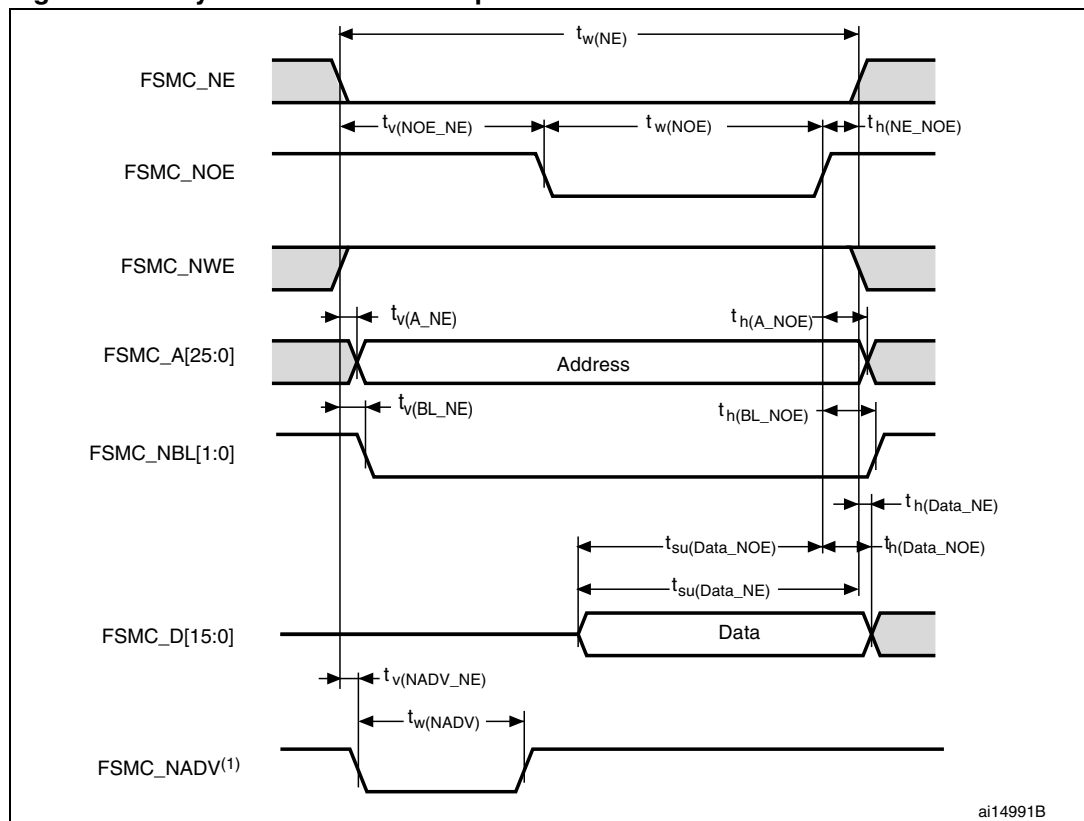
5.3.23 FSMC characteristics

Asynchronous waveforms and timings

Figure 45 through Figure 48 represent asynchronous waveforms and Table 65 through Table 68 provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0
- AddressHoldTime = 1
- DataSetupTime = 1

Figure 45. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



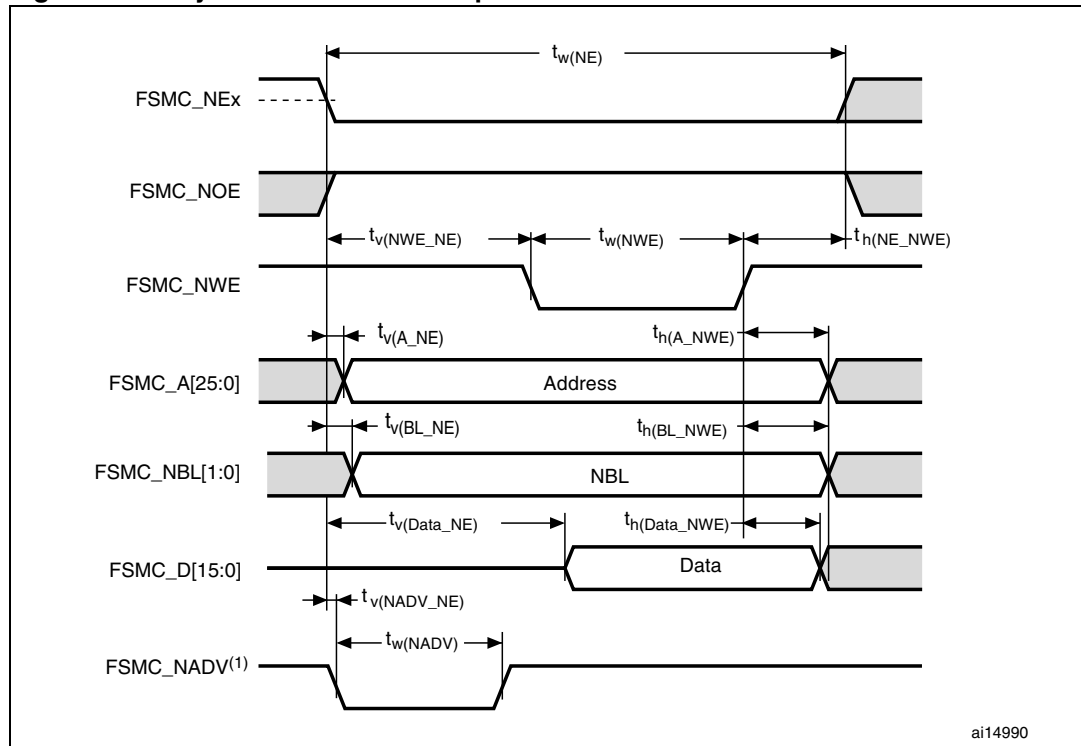
1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 65. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings^{(1) (2)}

| Symbol | Parameter | Min | Max | Unit |
|---------------------|---|-------------------|-------------------|------|
| $t_{w(NE)}$ | FSMC_NE low time | $5T_{HCLK} - 1.5$ | $5T_{HCLK} + 2$ | ns |
| $t_{v(NOE_NE)}$ | FSMC_NEx low to FSMC_NOE low | 0.5 | 1.5 | ns |
| $t_{w(NOE)}$ | FSMC_NOE low time | $5T_{HCLK} - 1.5$ | $5T_{HCLK} + 1.5$ | ns |
| $t_{h(NE_NOE)}$ | FSMC_NOE high to FSMC_NE high hold time | -1.5 | | ns |
| $t_{v(A_NE)}$ | FSMC_NEx low to FSMC_A valid | | 7 | ns |
| $t_{h(A_NOE)}$ | Address hold time after FSMC_NOE high | 0.1 | | ns |
| $t_{v(BL_NE)}$ | FSMC_NEx low to FSMC_BL valid | | 0 | ns |
| $t_{h(BL_NOE)}$ | FSMC_BL hold time after FSMC_NOE high | 0 | | ns |
| $t_{su(Data_NE)}$ | Data to FSMC_NEx high setup time | $2T_{HCLK} + 25$ | | ns |
| $t_{su(Data_NOE)}$ | Data to FSMC_NOEx high setup time | $2T_{HCLK} + 25$ | | ns |
| $t_{h(Data_NOE)}$ | Data hold time after FSMC_NOE high | 0 | | ns |
| $t_{h(Data_NE)}$ | Data hold time after FSMC_NEx high | 0 | | ns |
| $t_{v(NADV_NE)}$ | FSMC_NEx low to FSMC_NADV low | | 5 | ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | | $T_{HCLK} + 1.5$ | ns |

1. $C_L = 15$ pF.
2. Based on characterization, not tested in production.

Figure 46. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 66. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|--------------------|---|------------------|------------------|------|
| $t_{w(NE)}$ | FSMC_NE low time | $3T_{HCLK} - 1$ | $3T_{HCLK} + 2$ | ns |
| $t_{v(NWE_NE)}$ | FSMC_NEx low to FSMC_NWE low | $T_{HCLK} - 0.5$ | $T_{HCLK} + 1.5$ | ns |
| $t_{w(NWE)}$ | FSMC_NWE low time | $T_{HCLK} - 0.5$ | $T_{HCLK} + 1.5$ | ns |
| $t_{h(NE_NWE)}$ | FSMC_NWE high to FSMC_NE high hold time | T_{HCLK} | | ns |
| $t_{v(A_NE)}$ | FSMC_NEx low to FSMC_A valid | | 7.5 | ns |
| $t_{h(A_NWE)}$ | Address hold time after FSMC_NWE high | T_{HCLK} | | ns |
| $t_{v(BL_NE)}$ | FSMC_NEx low to FSMC_BL valid | | 1.5 | ns |
| $t_{h(BL_NWE)}$ | FSMC_BL hold time after FSMC_NWE high | $T_{HCLK} - 0.5$ | | ns |
| $t_{v(Data_NE)}$ | FSMC_NEx low to Data valid | | $T_{HCLK} + 7$ | ns |
| $t_{h(Data_NWE)}$ | Data hold time after FSMC_NWE high | T_{HCLK} | | ns |
| $t_{v(NADV_NE)}$ | FSMC_NEx low to FSMC_NADV low | | 5.5 | ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | | $T_{HCLK} + 1.5$ | ns |

1. $C_L = 15$ pF.
2. Based on characterization, not tested in production.

Figure 47. Asynchronous multiplexed PSRAM/NOR read waveforms

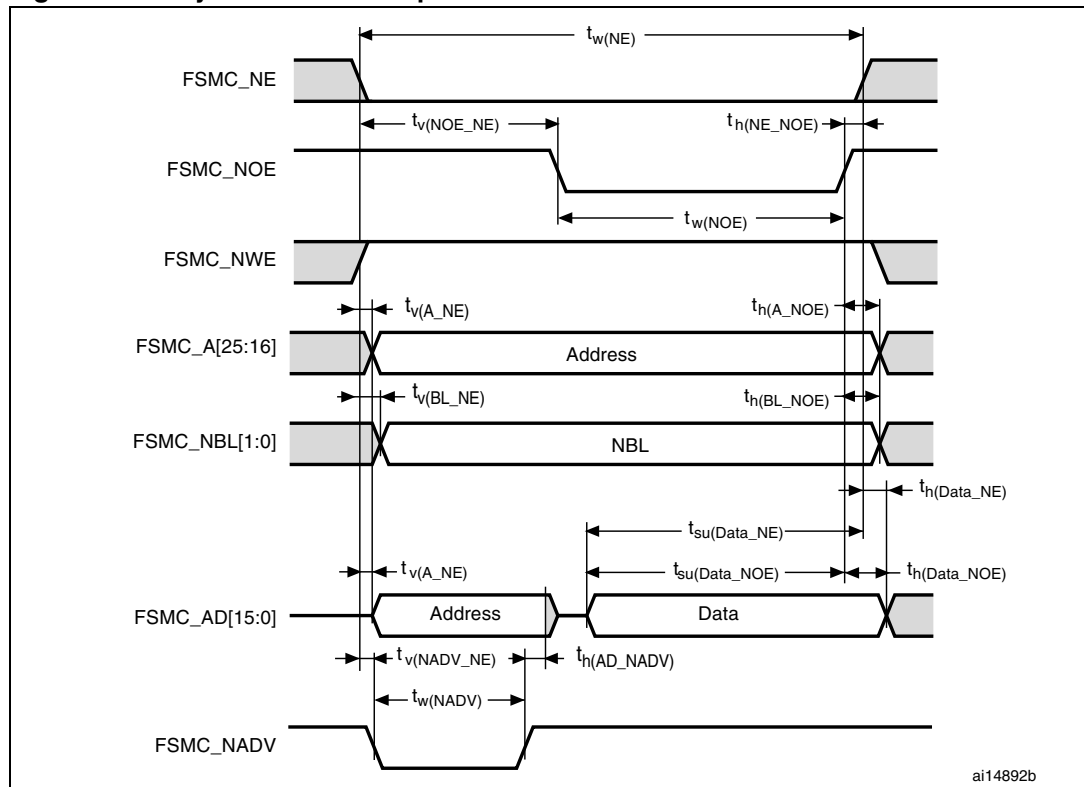


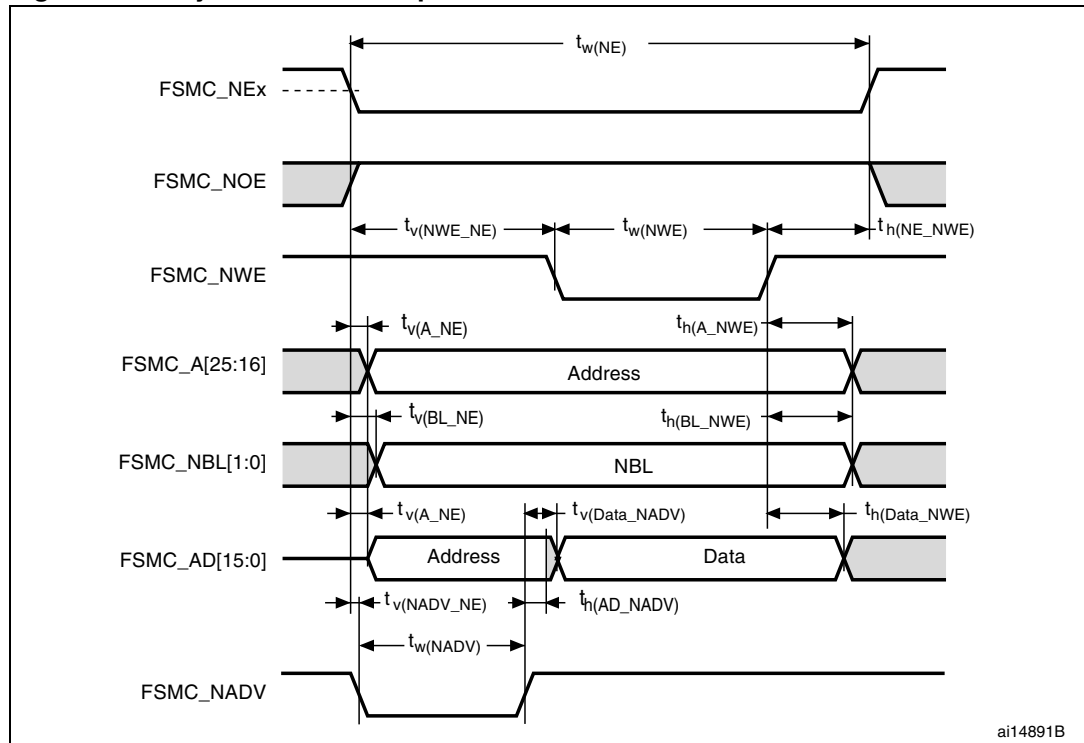
Table 67. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|-----------------------|--|-------------------|-------------------|------|
| $t_{w(NE)}$ | FSMC_NE low time | $7T_{HCLK} - 2$ | $7T_{HCLK} + 2$ | ns |
| $t_{v(NOENOE)}$ | FSMC_NEx low to FSMC_NOE low | $3T_{HCLK} - 0.5$ | $3T_{HCLK} + 1.5$ | ns |
| $t_{w(NOENOE)}$ | FSMC_NOE low time | $4T_{HCLK} - 1$ | $4T_{HCLK} + 2$ | ns |
| $t_{h(NEENOE)}$ | FSMC_NOE high to FSMC_NE high hold time | -1 | | ns |
| $t_{v(AENOE)}$ | FSMC_NEx low to FSMC_A valid | | 0 | ns |
| $t_{v(NADVNOENOE)}$ | FSMC_NEx low to FSMC_NADV low | 3 | 5 | ns |
| $t_{w(NADVNOENOE)}$ | FSMC_NADV low time | $T_{HCLK} - 1.5$ | $T_{HCLK} + 1.5$ | ns |
| $t_{h(ADNADVNOENOE)}$ | FSMC_AD (address) valid hold time after FSMC_NADV high | T_{HCLK} | | ns |
| $t_{h(AENOE)}$ | Address hold time after FSMC_NOE high | T_{HCLK} | | ns |
| $t_{h(BLNOENOE)}$ | FSMC_BL hold time after FSMC_NOE high | 0 | | ns |
| $t_{v(BLNOENOE)}$ | FSMC_NEx low to FSMC_BL valid | | 0 | ns |
| $t_{su(DataENOE)}$ | Data to FSMC_NEx high setup time | $2T_{HCLK} + 24$ | | ns |
| $t_{su(DataNOENOE)}$ | Data to FSMC_NOE high setup time | $2T_{HCLK} + 25$ | | ns |
| $t_{h(DataENOE)}$ | Data hold time after FSMC_NEx high | 0 | | ns |
| $t_{h(DataNOENOE)}$ | Data hold time after FSMC_NOE high | 0 | | ns |

1. $C_L = 15$ pF.

2. Based on characterization, not tested in production.

Figure 48. Asynchronous multiplexed PSRAM/NOR write waveforms



ai14891B

Table 68. Asynchronous multiplexed PSRAM/NOR write timings⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|---------------------|--|------------------|------------------|------|
| $t_{w(NE)}$ | FSMC_NE low time | $5T_{HCLK} - 1$ | $5T_{HCLK} + 2$ | ns |
| $t_{v(NWE_NE)}$ | FSMC_NEx low to FSMC_NWE low | $2T_{HCLK}$ | $2T_{HCLK} + 1$ | ns |
| $t_{w(NWE)}$ | FSMC_NWE low time | $2T_{HCLK} - 1$ | $2T_{HCLK} + 2$ | ns |
| $t_{h(NE_NWE)}$ | FSMC_NWE high to FSMC_NE high hold time | $T_{HCLK} - 1$ | | ns |
| $t_{v(A_NE)}$ | FSMC_NEx low to FSMC_A valid | | 7 | ns |
| $t_{v(NADV_NE)}$ | FSMC_NEx low to FSMC_NADV low | 3 | 5 | ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | $T_{HCLK} - 1$ | $T_{HCLK} + 1$ | ns |
| $t_{h(AD_NADV)}$ | FSMC_AD (address) valid hold time after FSMC_NADV high | $T_{HCLK} - 3$ | | ns |
| $t_{h(A_NWE)}$ | Address hold time after FSMC_NWE high | $4T_{HCLK}$ | | ns |
| $t_{v(BL_NE)}$ | FSMC_NEx low to FSMC_BL valid | | 1.6 | ns |
| $t_{h(BL_NWE)}$ | FSMC_BL hold time after FSMC_NWE high | $T_{HCLK} - 1.5$ | | ns |
| $t_{v(Data_NADV)}$ | FSMC_NADV high to Data valid | | $T_{HCLK} + 1.5$ | ns |
| $t_{h(Data_NWE)}$ | Data hold time after FSMC_NWE high | $T_{HCLK} - 5$ | | ns |

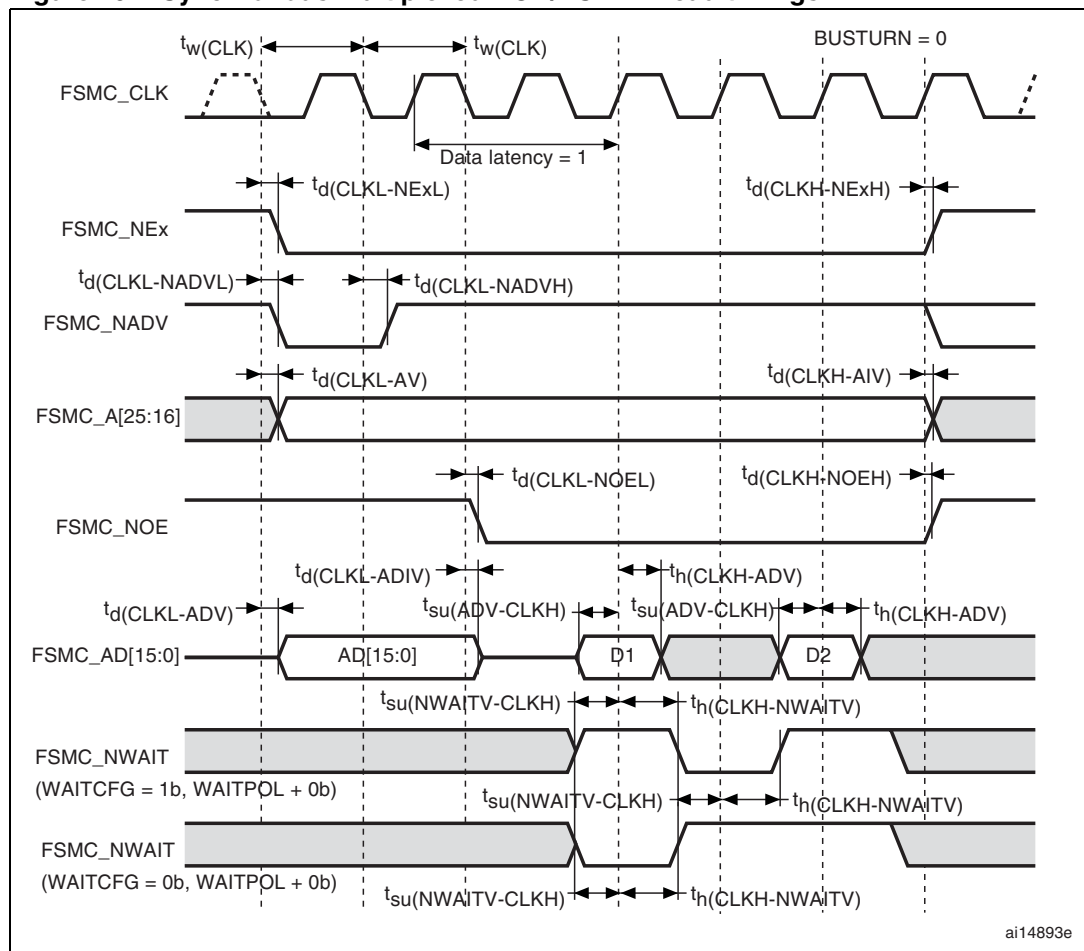
1. $C_L = 15$ pF.
2. Based on characterization, not tested in production.

Synchronous waveforms and timings

Figure 49 through Figure 52 represent synchronous waveforms and Table 70 through Table 72 provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F20xxx/21xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Figure 49. Synchronous multiplexed NOR/PSRAM read timings



ai14893e

Table 69. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|------------------------------|--|-------------------------|-----------------------|------|
| $t_{w(\text{CLK})}$ | FSMC_CLK period | 27.7 | | ns |
| $t_{d(\text{CLKL-NExL})}$ | FSMC_CLK low to FSMC_NEx low (x = 0...2) | | 1.5 | ns |
| $t_{d(\text{CLKH-NExH})}$ | FSMC_CLK high to FSMC_NEx high (x = 0...2) | $T_{\text{HCLK}} + 2$ | | ns |
| $t_{d(\text{CLKL-NADV})}$ | FSMC_CLK low to FSMC_NADV low | | 4 | ns |
| $t_{d(\text{CLKL-NADVH})}$ | FSMC_CLK low to FSMC_NADV high | 5 | | ns |
| $t_{d(\text{CLKL-AV})}$ | FSMC_CLK low to FSMC_Ax valid (x = 16...25) | | 0 | ns |
| $t_{d(\text{CLKH-AIV})}$ | FSMC_CLK high to FSMC_Ax invalid (x = 16...25) | $T_{\text{HCLK}} + 2$ | | ns |
| $t_{d(\text{CLKL-NOEL})}$ | FSMC_CLK low to FSMC_NOE low | | $T_{\text{HCLK}} + 1$ | ns |
| $t_{d(\text{CLKH-NOEH})}$ | FSMC_CLK high to FSMC_NOE high | $T_{\text{HCLK}} + 0.5$ | | ns |
| $t_{d(\text{CLKL-ADV})}$ | FSMC_CLK low to FSMC_AD[15:0] valid | | 12 | ns |
| $t_{d(\text{CLKL-ADIV})}$ | FSMC_CLK low to FSMC_AD[15:0] invalid | 0 | | ns |
| $t_{su(\text{ADV-CLKH})}$ | FSMC_A/D[15:0] valid data before FSMC_CLK high | 6 | | ns |
| $t_h(\text{CLKH-ADV})$ | FSMC_A/D[15:0] valid data after FSMC_CLK high | $T_{\text{HCLK}} - 10$ | | ns |
| $t_{su(\text{NWAITV-CLKH})}$ | FSMC_NWAIT valid before FSMC_CLK high | 8 | | ns |
| $t_h(\text{CLKH-NWAITV})$ | FSMC_NWAIT valid after FSMC_CLK high | 2 | | ns |

1. $C_L = 15$ pF.

2. Based on characterization, not tested in production.

Figure 50. Synchronous multiplexed PSRAM write timings

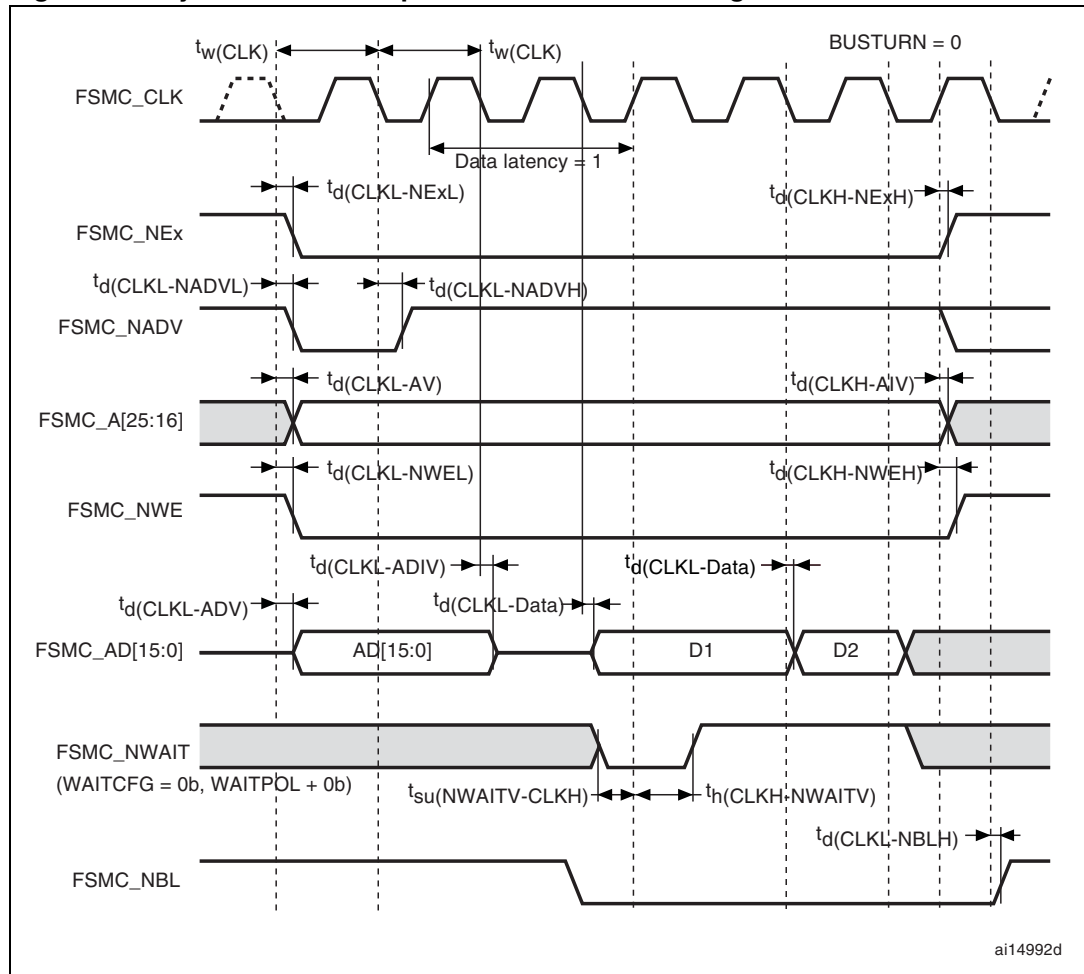


Table 70. Synchronous multiplexed PSRAM write timings⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|------------------------------|--|-----------------------|-----|------|
| $t_{w(\text{CLK})}$ | FSMC_CLK period | 27.7 | | ns |
| $t_{d(\text{CLKL-NExL})}$ | FSMC_CLK low to FSMC_Nex low (x = 0...2) | | 2 | ns |
| $t_{d(\text{CLKH-NExH})}$ | FSMC_CLK high to FSMC_NEx high (x = 0...2) | $T_{\text{HCLK}} + 2$ | | ns |
| $t_{d(\text{CLKL-NADV})}$ | FSMC_CLK low to FSMC_NADV low | | 4 | ns |
| $t_{d(\text{CLKL-NADVH})}$ | FSMC_CLK low to FSMC_NADV high | 5 | | ns |
| $t_{d(\text{CLKL-AV})}$ | FSMC_CLK low to FSMC_Ax valid (x = 16...25) | | 0 | ns |
| $t_{d(\text{CLKH-AIV})}$ | FSMC_CLK high to FSMC_Ax invalid (x = 16...25) | $T_{\text{CK}} + 2$ | | ns |
| $t_{d(\text{CLKL-NWEL})}$ | FSMC_CLK low to FSMC_NWE low | | 1 | ns |
| $t_{d(\text{CLKH-NWEH})}$ | FSMC_CLK high to FSMC_NWE high | $T_{\text{HCLK}} + 1$ | | ns |
| $t_{d(\text{CLKL-ADV})}$ | FSMC_CLK low to FSMC_AD[15:0] valid | | 12 | ns |
| $t_{d(\text{CLKL-ADIV})}$ | FSMC_CLK low to FSMC_AD[15:0] invalid | 3 | | ns |
| $t_{d(\text{CLKL-Data})}$ | FSMC_A/D[15:0] valid after FSMC_CLK low | | 6 | ns |
| $t_{su(\text{NWAITV-CLKH})}$ | FSMC_NWAIT valid before FSMC_CLK high | 7 | | ns |
| $t_h(\text{CLKH-NWAITV})$ | FSMC_NWAIT valid after FSMC_CLK high | 2 | | ns |
| $t_{d(\text{CLKL-NBLH})}$ | FSMC_CLK low to FSMC_NBL high | 1 | | ns |

1. $C_L = 15$ pF.

2. Based on characterization, not tested in production.

Figure 51. Synchronous non-multiplexed NOR/PSRAM read timings

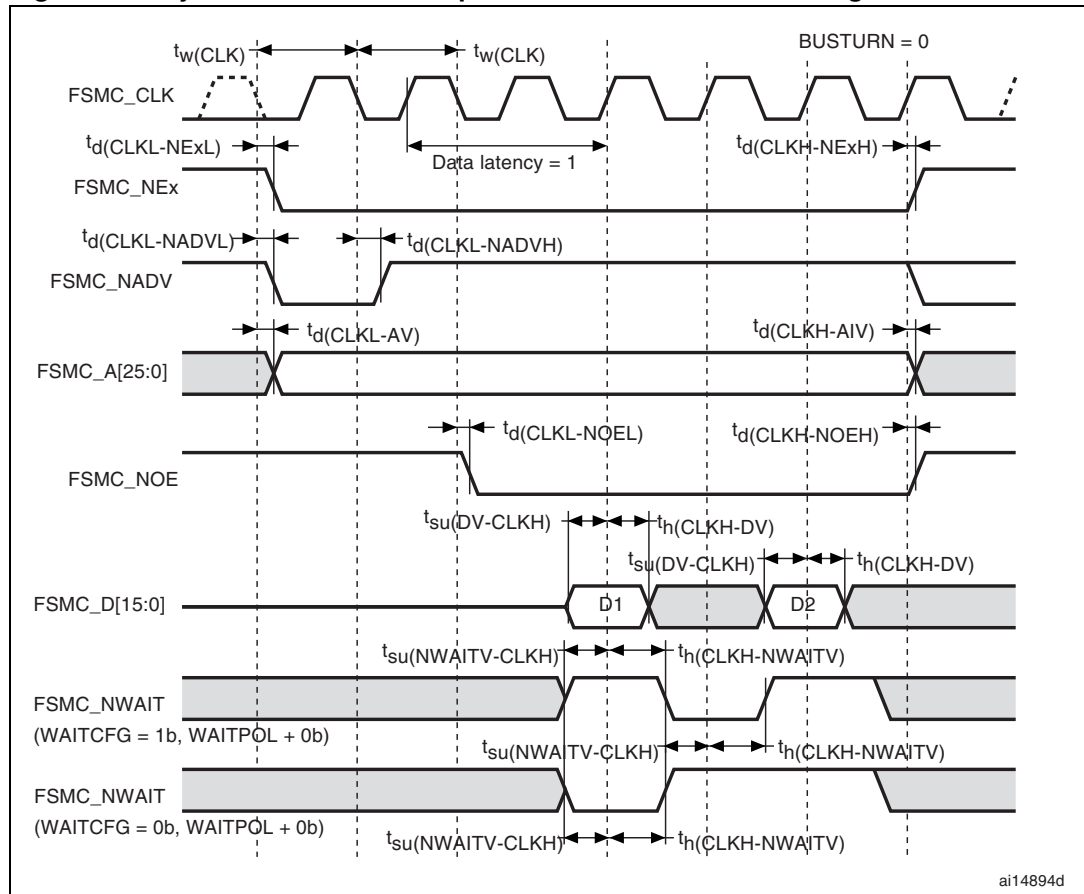


Table 71. Synchronous non-multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|------------------------------|---|-------------------------|-------------------------|------|
| $t_w(\text{CLK})$ | FSMC_CLK period | 27.7 | | ns |
| $t_d(\text{CLKL-NExL})$ | FSMC_CLK low to FSMC_NEx low (x = 0...2) | | 1.5 | ns |
| $t_d(\text{CLKH-NExH})$ | FSMC_CLK high to FSMC_NEx high (x = 0...2) | $T_{\text{HCLK}} + 2$ | | ns |
| $t_d(\text{CLKL-NADV})$ | FSMC_CLK low to FSMC_NADV low | | 4 | ns |
| $t_d(\text{CLKL-NADVH})$ | FSMC_CLK low to FSMC_NADV high | 5 | | ns |
| $t_d(\text{CLKL-AV})$ | FSMC_CLK low to FSMC_Ax valid (x = 0...25) | | 0 | ns |
| $t_d(\text{CLKH-AIV})$ | FSMC_CLK high to FSMC_Ax invalid (x = 0...25) | $T_{\text{HCLK}} + 4$ | | ns |
| $t_d(\text{CLKL-NOEL})$ | FSMC_CLK low to FSMC_NOE low | | $T_{\text{HCLK}} + 1.5$ | ns |
| $t_d(\text{CLKH-NOEH})$ | FSMC_CLK high to FSMC_NOE high | $T_{\text{HCLK}} + 1.5$ | | ns |
| $t_{su}(\text{DV-CLKH})$ | FSMC_D[15:0] valid data before FSMC_CLK high | 6.5 | | ns |
| $t_h(\text{CLKH-DV})$ | FSMC_D[15:0] valid data after FSMC_CLK high | 7 | | ns |
| $t_{su}(\text{NWAITV-CLKH})$ | FSMC_NWAIT valid before FSMC_SMCLK high | 7 | | ns |
| $t_h(\text{CLKH-NWAITV})$ | FSMC_NWAIT valid after FSMC_CLK high | 2 | | ns |

1. $C_L = 15 \text{ pF}$.
2. Based on characterization, not tested in production.

Figure 52. Synchronous non-multiplexed PSRAM write timings

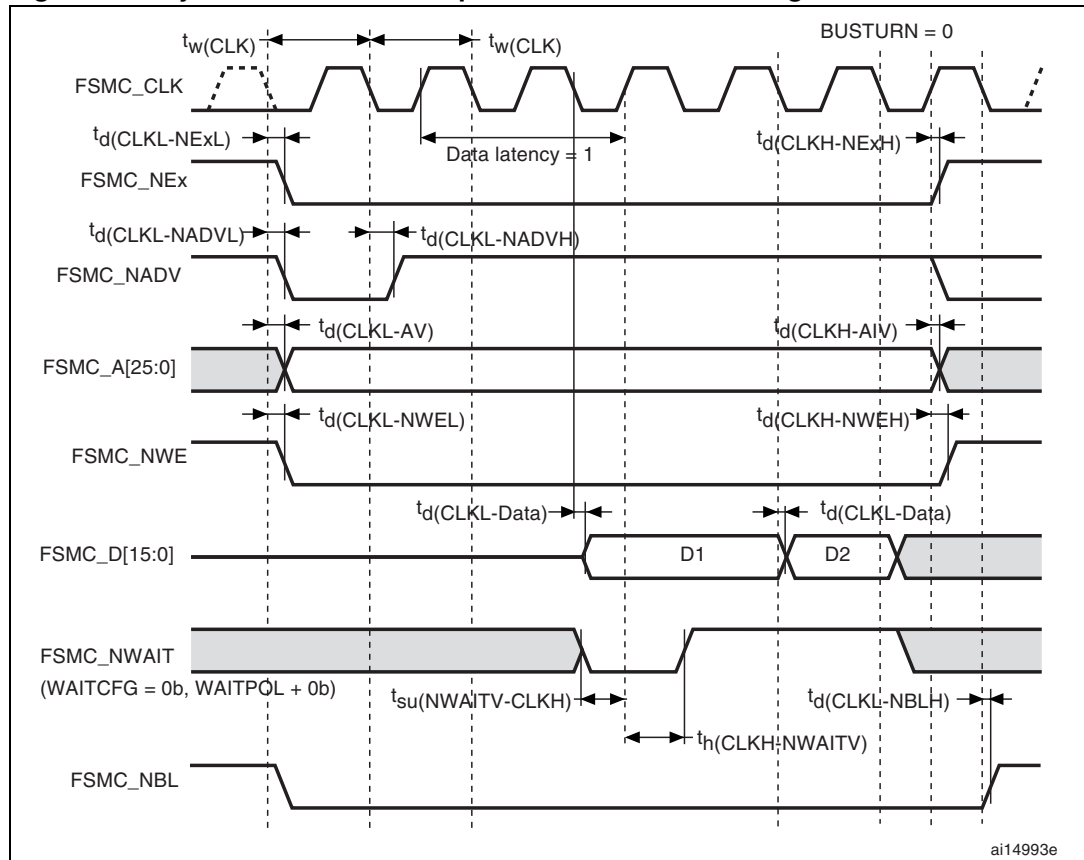


Table 72. Synchronous non-multiplexed PSRAM write timings⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|-------------------------------------|---|-----------------------|-----|------|
| $t_w(\text{CLK})$ | FSMC_CLK period | 27.7 | | ns |
| $t_d(\text{CLKL-NExL})$ | FSMC_CLK low to FSMC_NEx low (x = 0..2) | | 2 | ns |
| $t_d(\text{CLKH-NExH})$ | FSMC_CLK high to FSMC_NEx high (x = 0..2) | $T_{\text{HCLK}} + 2$ | | ns |
| $t_d(\text{CLKL-NADV})$ | FSMC_CLK low to FSMC_NADV low | | 4 | ns |
| $t_d(\text{CLKL-NADVH})$ | FSMC_CLK low to FSMC_NADV high | 5 | | ns |
| $t_d(\text{CLKL-AV})$ | FSMC_CLK low to FSMC_Ax valid (x = 16..25) | | 0 | ns |
| $t_d(\text{CLKH-AIV})$ | FSMC_CLK high to FSMC_Ax invalid (x = 16..25) | $T_{\text{CK}} + 2$ | | ns |
| $t_d(\text{CLKL-NWEL})$ | FSMC_CLK low to FSMC_NWE low | | 1 | ns |
| $t_d(\text{CLKH-NWEH})$ | FSMC_CLK high to FSMC_NWE high | $T_{\text{HCLK}} + 1$ | | ns |
| $t_d(\text{CLKL-Data})$ | FSMC_D[15:0] valid data after FSMC_CLK low | | 6 | ns |
| $t_{\text{su}}(\text{NWAITV-CLKH})$ | FSMC_NWAIT valid before FSMC_CLK high | 7 | | ns |
| $t_{\text{h}}(\text{CLKH-NWAITV})$ | FSMC_NWAIT valid after FSMC_CLK high | 2 | | ns |
| $t_d(\text{CLKL-NBLH})$ | FSMC_CLK low to FSMC_NBL high | 1 | | ns |

1. $C_L = 15 \text{ pF}$.

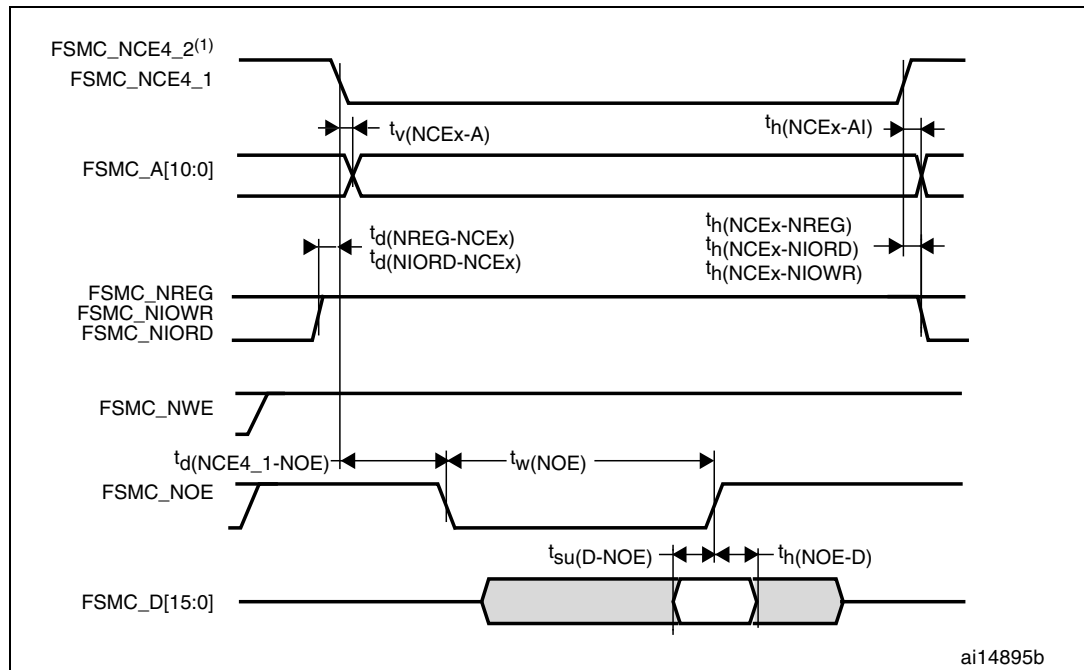
2. Based on characterization, not tested in production.

PC Card/CompactFlash controller waveforms and timings

Figure 53 through Figure 58 represent synchronous waveforms and Table 73 provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x04;
- COM.FSMC_WaitSetupTime = 0x07;
- COM.FSMC_HoldSetupTime = 0x04;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x04;
- ATT.FSMC_WaitSetupTime = 0x07;
- ATT.FSMC_HoldSetupTime = 0x04;
- ATT.FSMC_HiZSetupTime = 0x00;
- IO.FSMC_SetupTime = 0x04;
- IO.FSMC_WaitSetupTime = 0x07;
- IO.FSMC_HoldSetupTime = 0x04;
- IO.FSMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 53. PC Card/CompactFlash controller waveforms for common memory read access



1. FSMC_NCE4_2 remains high (inactive during 8-bit access).

Figure 54. PC Card/CompactFlash controller waveforms for common memory write access

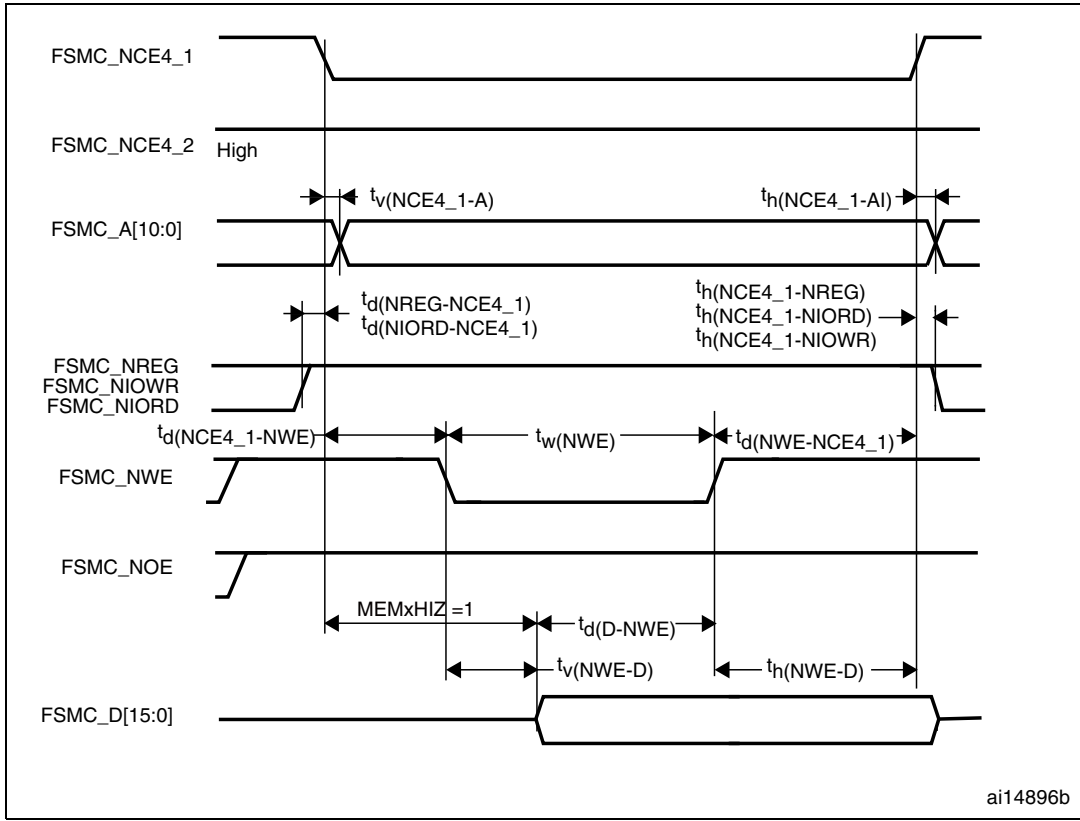
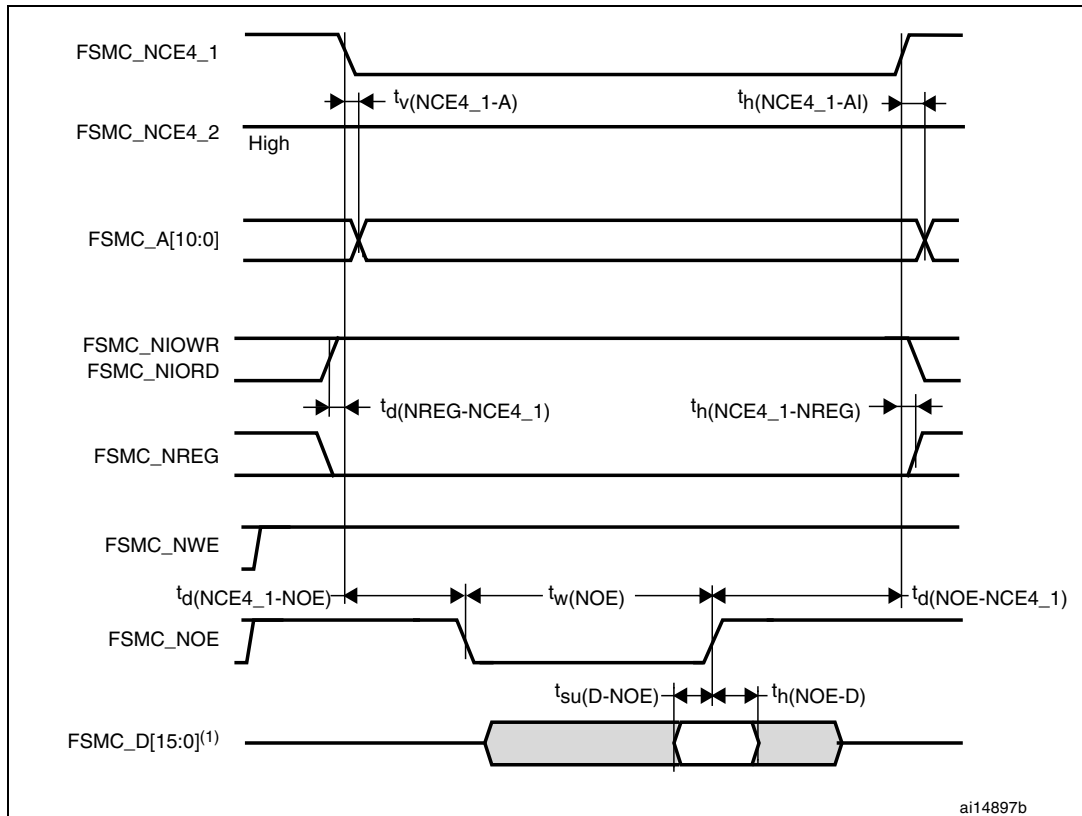
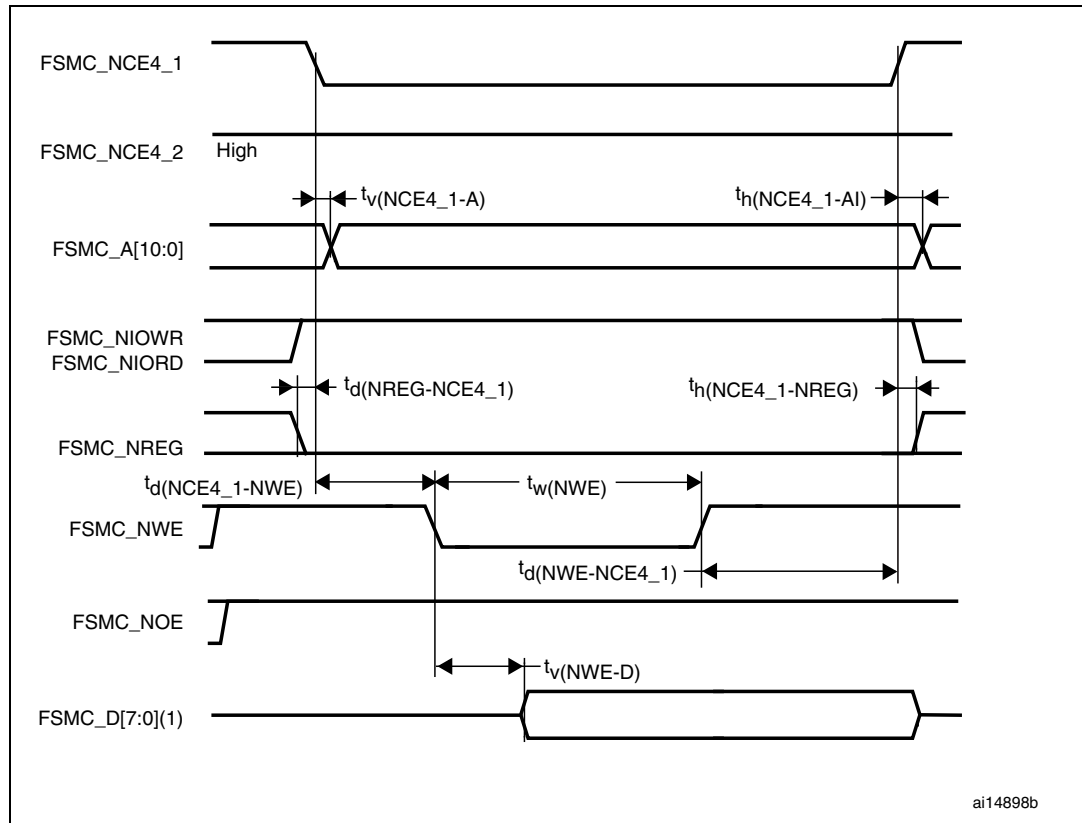


Figure 55. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

Figure 56. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains Hi-Z).

Figure 57. PC Card/CompactFlash controller waveforms for I/O space read access

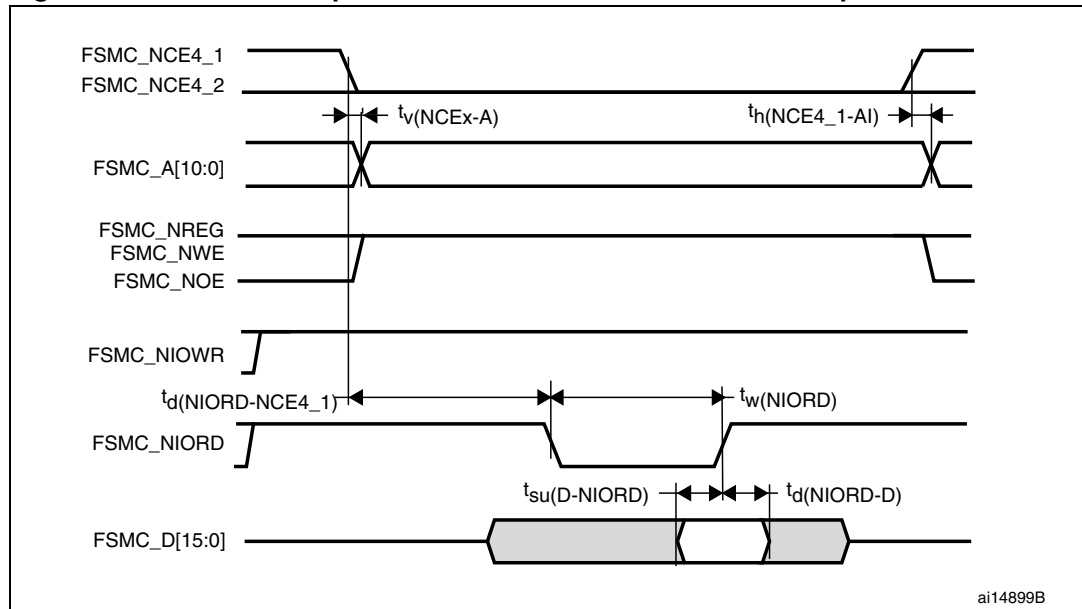
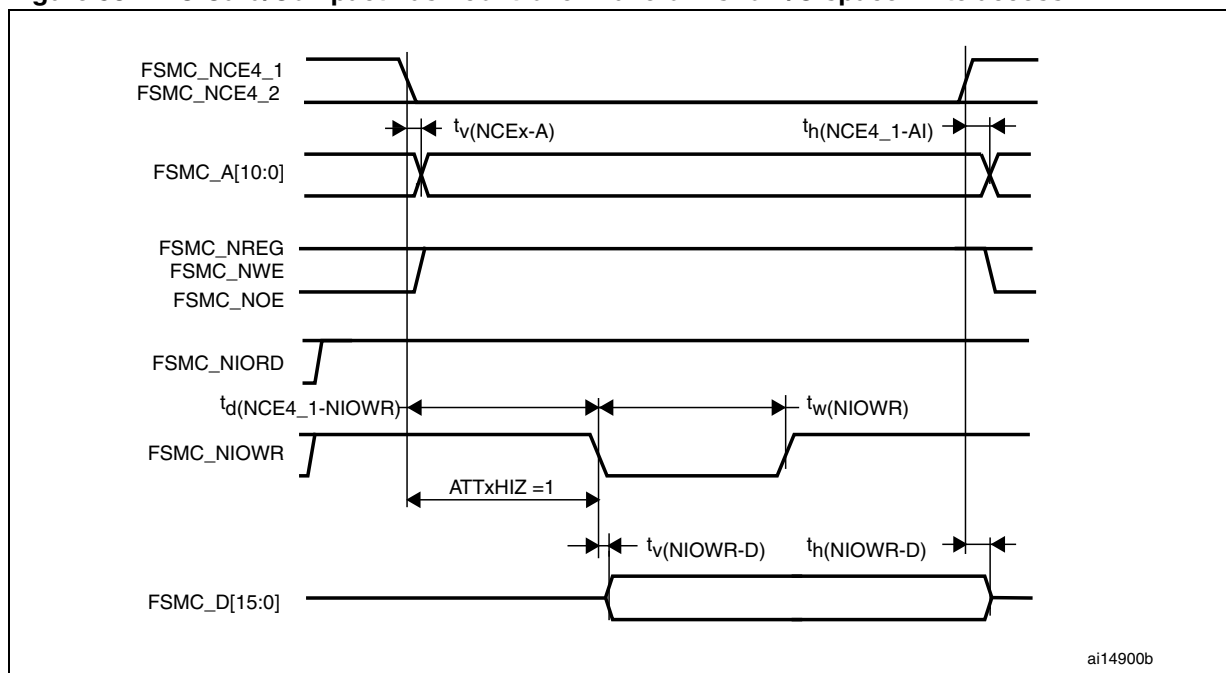


Figure 58. PC Card/CompactFlash controller waveforms for I/O space write access



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Table 73. Switching characteristics for PC Card/CF read and write cycles⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|--|---|-------------------|-------------------|------|
| $t_{v(NCEx-A)}$ $t_{v(NCE4_1-A)}$ | FSMC_NCEx low (x = 4_1/4_2) to FSMC_Ay valid (y = 0...10) FSMC_NCE4_1 low (x = 4_1/4_2) to FSMC_Ay valid (y = 0...10) | | 0 | ns |
| $t_{h(NCEx-AI)}$ $t_{h(NCE4_1-AI)}$ | FSMC_NCEx high (x = 4_1/4_2) to FSMC_Ax invalid (x = 0...10) FSMC_NCE4_1 high (x = 4_1/4_2) to FSMC_Ax invalid (x = 0...10) | 2.5 | | ns |
| $t_{d(NREG-NCEx)}$ $t_{d(NREG-NCE4_1)}$ | FSMC_NCEx low to FSMC_NREG valid FSMC_NCE4_1 low to FSMC_NREG valid | | 5 | ns |
| $t_{h(NCEx-NREG)}$ $t_{h(NCE4_1-NREG)}$ | FSMC_NCEx high to FSMC_NREG invalid FSMC_NCE4_1 high to FSMC_NREG invalid | $T_{HCLK} + 3$ | | ns |
| $t_{d(NCE4_1-NOE)}$ | FSMC_NCE4_1 low to FSMC_NOE low | | $5T_{HCLK} + 2$ | ns |
| $t_{w(NOE)}$ | FSMC_NOE low width | $8T_{HCLK} - 1.5$ | $8T_{HCLK} + 1$ | ns |
| $t_{d(NOE-NCE4_1)}$ | FSMC_NOE high to FSMC_NCE4_1 high | $5T_{HCLK} + 2$ | | ns |
| $t_{su(D-NOE)}$ | FSMC_D[15:0] valid data before FSMC_NOE high | 25 | | ns |
| $t_{h(NOE-D)}$ | FSMC_D[15:0] valid data after FSMC_NOE high | 15 | | ns |
| $t_{w(NWE)}$ | FSMC_NWE low width | $8T_{HCLK} - 1$ | $8T_{HCLK} + 2$ | ns |
| $t_{d(NWE-NCE4_1)}$ | FSMC_NWE high to FSMC_NCE4_1 high | $5T_{HCLK} + 2$ | | ns |
| $t_{d(NCE4_1-NWE)}$ | FSMC_NCE4_1 low to FSMC_NWE low | | $5T_{HCLK} + 1.5$ | ns |
| $t_{v(NWE-D)}$ | FSMC_NWE low to FSMC_D[15:0] valid | | 0 | ns |
| $t_{h(NWE-D)}$ | FSMC_NWE high to FSMC_D[15:0] invalid | $11T_{HCLK}$ | | ns |
| $t_{d(D-NWE)}$ | FSMC_D[15:0] valid before FSMC_NWE high | $13T_{HCLK}$ | | ns |

Table 73. Switching characteristics for PC Card/CF read and write cycles⁽¹⁾⁽²⁾ (continued)

| Symbol | Parameter | Min | Max | Unit |
|---|--|-----------------|-------------------|------|
| $t_{w(NIOWR)}$ | FSMC_NIOWR low width | $8T_{HCLK} + 3$ | | ns |
| $t_{v(NIOWR-D)}$ | FSMC_NIOWR low to FSMC_D[15:0] valid | | $5T_{HCLK} + 1$ | ns |
| $t_{h(NIOWR-D)}$ | FSMC_NIOWR high to FSMC_D[15:0] invalid | $11T_{HCLK}$ | | ns |
| $t_{d(NCE4_1-NIOWR)}$ | FSMC_NCE4_1 low to FSMC_NIOWR valid | | $5T_{HCLK} + 3ns$ | ns |
| $t_{h(NCEx-NIOWR)}$ $t_{h(NCE4_1-NIOWR)}$ | FSMC_NCEx high to FSMC_NIOWR invalid FSMC_NCE4_1 high to FSMC_NIOWR invalid | $5T_{HCLK} - 5$ | | ns |
| $t_{d(NIORD-NCEx)}$ $t_{d(NIORD-NCE4_1)}$ | FSMC_NCEx low to FSMC_NIORD valid FSMC_NCE4_1 low to FSMC_NIORD valid | | $5T_{HCLK} + 2.5$ | ns |
| $t_{h(NCEx-NIORD)}$ $t_{h(NCE4_1-NIORD)}$ | FSMC_NCEx high to FSMC_NIORD invalid FSMC_NCE4_1 high to FSMC_NIORD invalid | $5T_{HCLK} - 5$ | | ns |
| $t_{su(D-NIORD)}$ | FSMC_D[15:0] valid before FSMC_NIORD high | 4.5 | | ns |
| $t_{d(NIORD-D)}$ | FSMC_D[15:0] valid after FSMC_NIORD high | 9 | | ns |
| $t_{w(NIORD)}$ | FSMC_NIORD low width | $8T_{HCLK} + 2$ | | ns |

1. $C_L = 15$ pF.

2. Based on characterization, not tested in production.

NAND controller waveforms and timings

Figure 59 through Figure 62 represent synchronous waveforms and Table 74 provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 59. NAND controller waveforms for read access

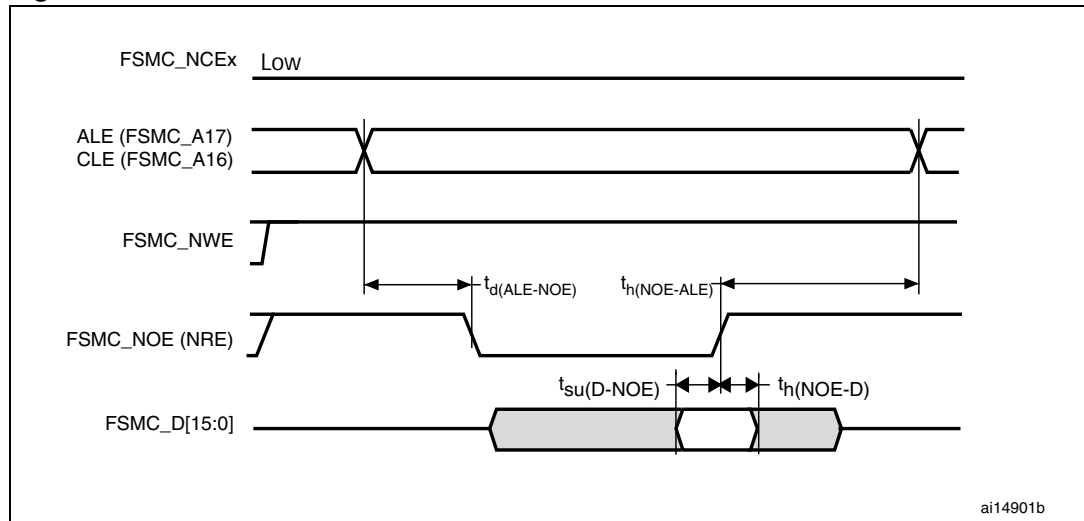


Figure 60. NAND controller waveforms for write access

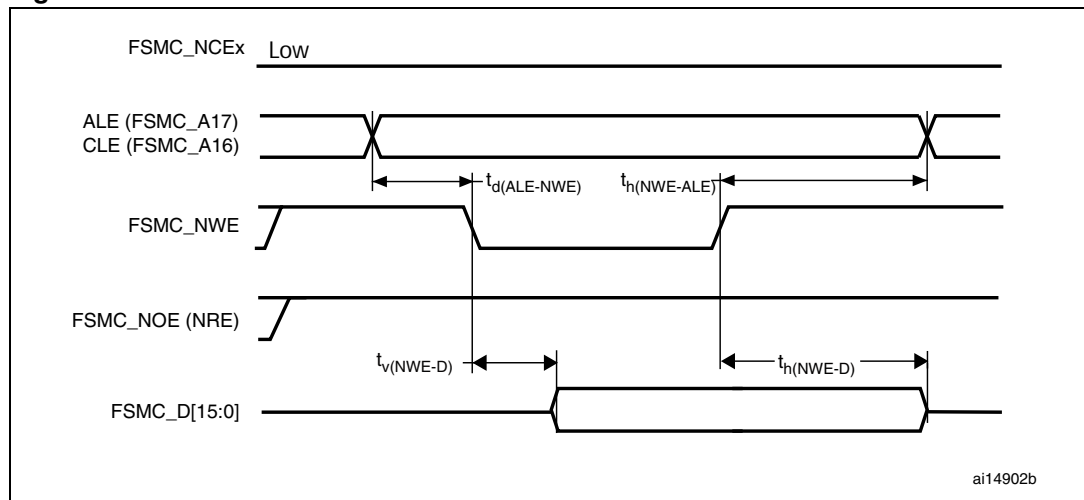


Figure 61. NAND controller waveforms for common memory read access

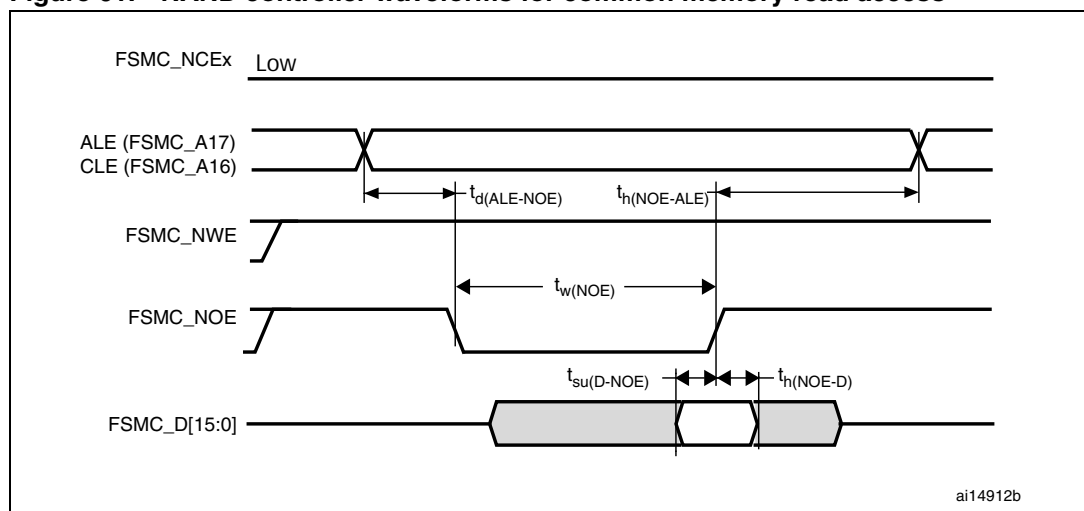


Figure 62. NAND controller waveforms for common memory write access

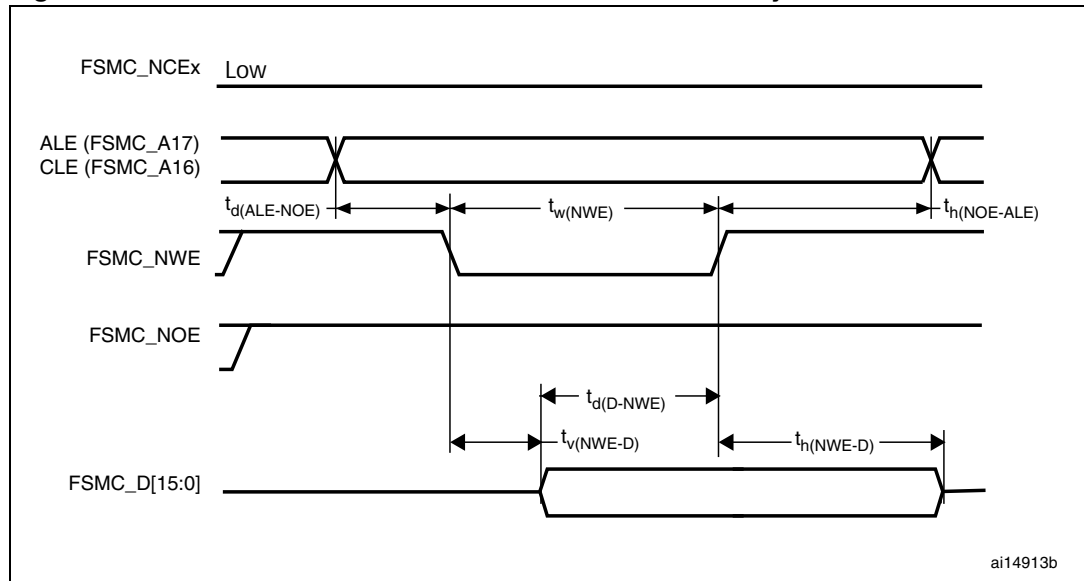


Table 74. Switching characteristics for NAND Flash read and write cycles⁽¹⁾

| Symbol | Parameter | Min | Max | Unit |
|------------------------|--|-------------------|-------------------|------|
| $t_{d(D-NWE)}^{(2)}$ | FSMC_D[15:0] valid before FSMC_NWE high | $6T_{HCLK} + 12$ | | ns |
| $t_{w(NOE)}^{(2)}$ | FSMC_NOE low width | $4T_{HCLK} - 1.5$ | $4T_{HCLK} + 1.5$ | ns |
| $t_{su(D-NOE)}^{(2)}$ | FSMC_D[15:0] valid data before FSMC_NOE high | 25 | | ns |
| $t_{h(NOE-D)}^{(2)}$ | FSMC_D[15:0] valid data after FSMC_NOE high | 7 | | ns |
| $t_{w(NWE)}^{(2)}$ | FSMC_NWE low width | $4T_{HCLK} - 1$ | $4T_{HCLK} + 2.5$ | ns |
| $t_{v(NWE-D)}^{(2)}$ | FSMC_NWE low to FSMC_D[15:0] valid | | 0 | ns |
| $t_{h(NWE-D)}^{(2)}$ | FSMC_NWE high to FSMC_D[15:0] invalid | $10T_{HCLK} + 4$ | | ns |
| $t_{d(ALE-NWE)}^{(3)}$ | FSMC_ALE valid before FSMC_NWE low | | $3T_{HCLK} + 1.5$ | ns |
| $t_{h(NWE-ALE)}^{(3)}$ | FSMC_NWE high to FSMC_ALE invalid | $3T_{HCLK} + 4.5$ | | ns |
| $t_{d(ALE-NOE)}^{(3)}$ | FSMC_ALE valid before FSMC_NOE low | | $3T_{HCLK} + 2$ | ns |
| $t_{h(NOE-ALE)}^{(3)}$ | FSMC_NWE high to FSMC_ALE invalid | $3T_{HCLK} + 4.5$ | | ns |

1. $C_L = 15$ pF.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

5.3.24 Camera interface (DCMI) timing specifications

Table 75. DCMI characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|--|-------------------------|-----|-----|------|
| | Frequency ratio $DCMI_PIXCLK/f_{HCLK}$ | $DCMI_PIXCLK = 48$ MHz | | 2.5 | |

5.3.25 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in [Table 76](#) are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 10](#).

Refer to [Section 5.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

Figure 63. SDIO high-speed mode

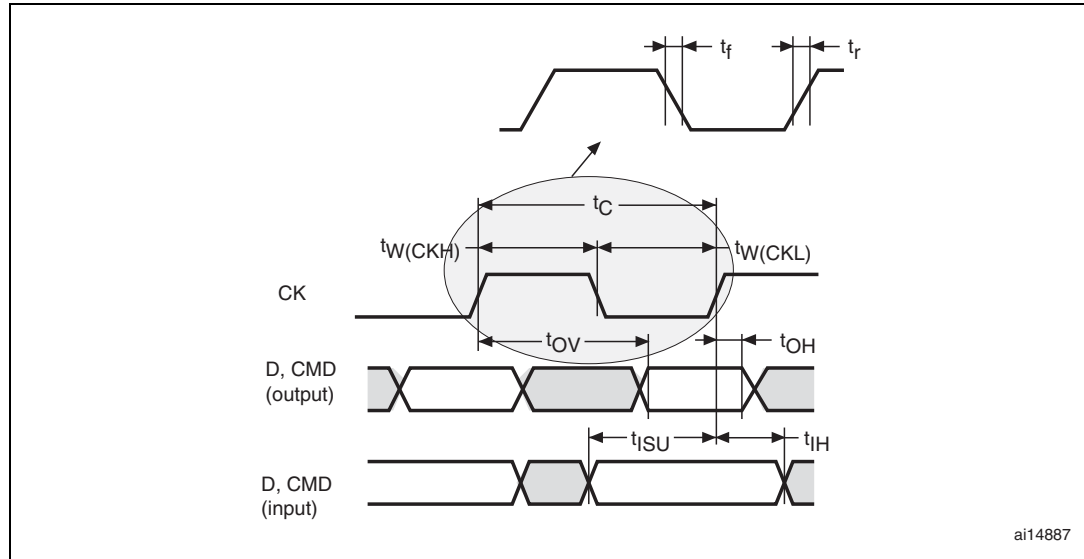


Figure 64. SD default mode

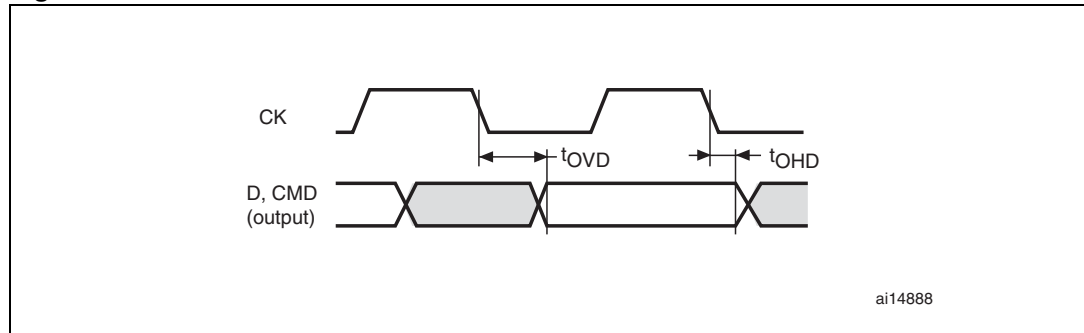


Table 76. SD / MMC characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------|---------------------------------------|------------------|-----|-----|------|
| f_{PP} | Clock frequency in data transfer mode | $C_L \leq 30$ pF | 0 | 48 | MHz |
| - | SDIO_CK/ f_{PCLK2} frequency ratio | - | - | 8/3 | - |

Table 76. SD / MMC characteristics (continued)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|------------------------------------|------------------|-----|-----|------|
| $t_{W(CKL)}$ | Clock low time, $f_{PP} = 16$ MHz | $C_L \leq 30$ pF | 32 | | ns |
| $t_{W(CKH)}$ | Clock high time, $f_{PP} = 16$ MHz | $C_L \leq 30$ pF | 31 | | |
| t_r | Clock rise time | $C_L \leq 30$ pF | | 3.5 | |
| t_f | Clock fall time | $C_L \leq 30$ pF | | 5 | |
| CMD, D inputs (referenced to CK) | | | | | |
| t_{SU} | Input setup time | $C_L \leq 30$ pF | 2 | | ns |
| t_{IH} | Input hold time | $C_L \leq 30$ pF | 0 | | |
| CMD, D outputs (referenced to CK) in MMC and SD HS mode | | | | | |
| t_{OV} | Output valid time | $C_L \leq 30$ pF | | 6 | ns |
| t_{OH} | Output hold time | $C_L \leq 30$ pF | 0.3 | | |
| CMD, D outputs (referenced to CK) in SD default mode⁽¹⁾ | | | | | |
| t_{OVD} | Output valid default time | $C_L \leq 30$ pF | | 7 | ns |
| t_{OHD} | Output hold default time | $C_L \leq 30$ pF | 0.5 | | |

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

5.3.26 RTC characteristics

Table 77. RTC characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|------------------------------------|--|-----|-----|------|
| - | $f_{PCLK1}/RTCCLK$ frequency ratio | Any read/write operation from/to an RTC register | 4 | - | - |

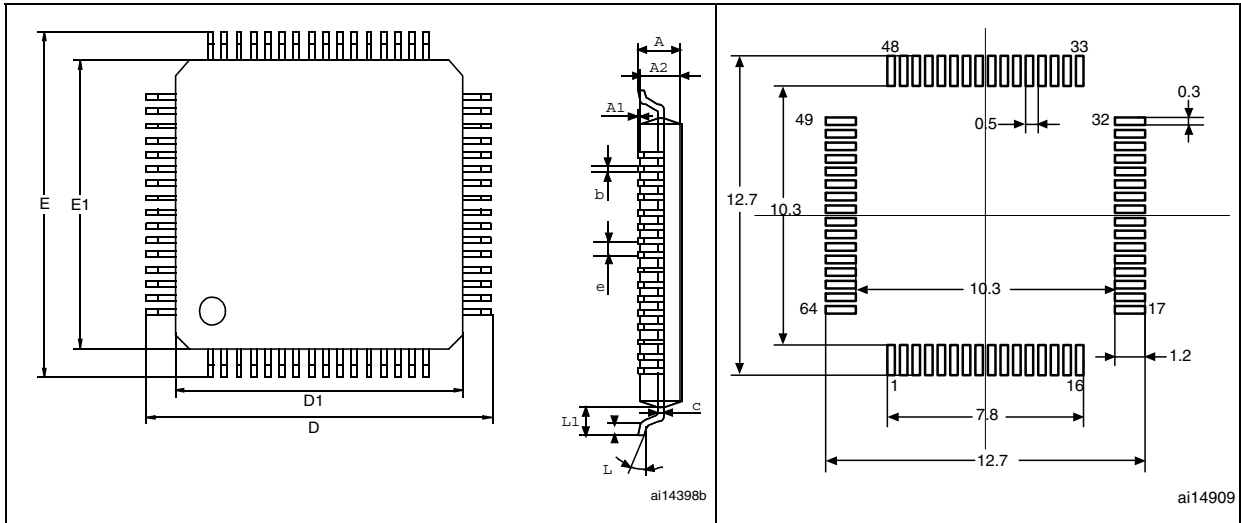
6 Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 65. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline⁽¹⁾

Figure 66. Recommended footprint⁽¹⁾⁽²⁾



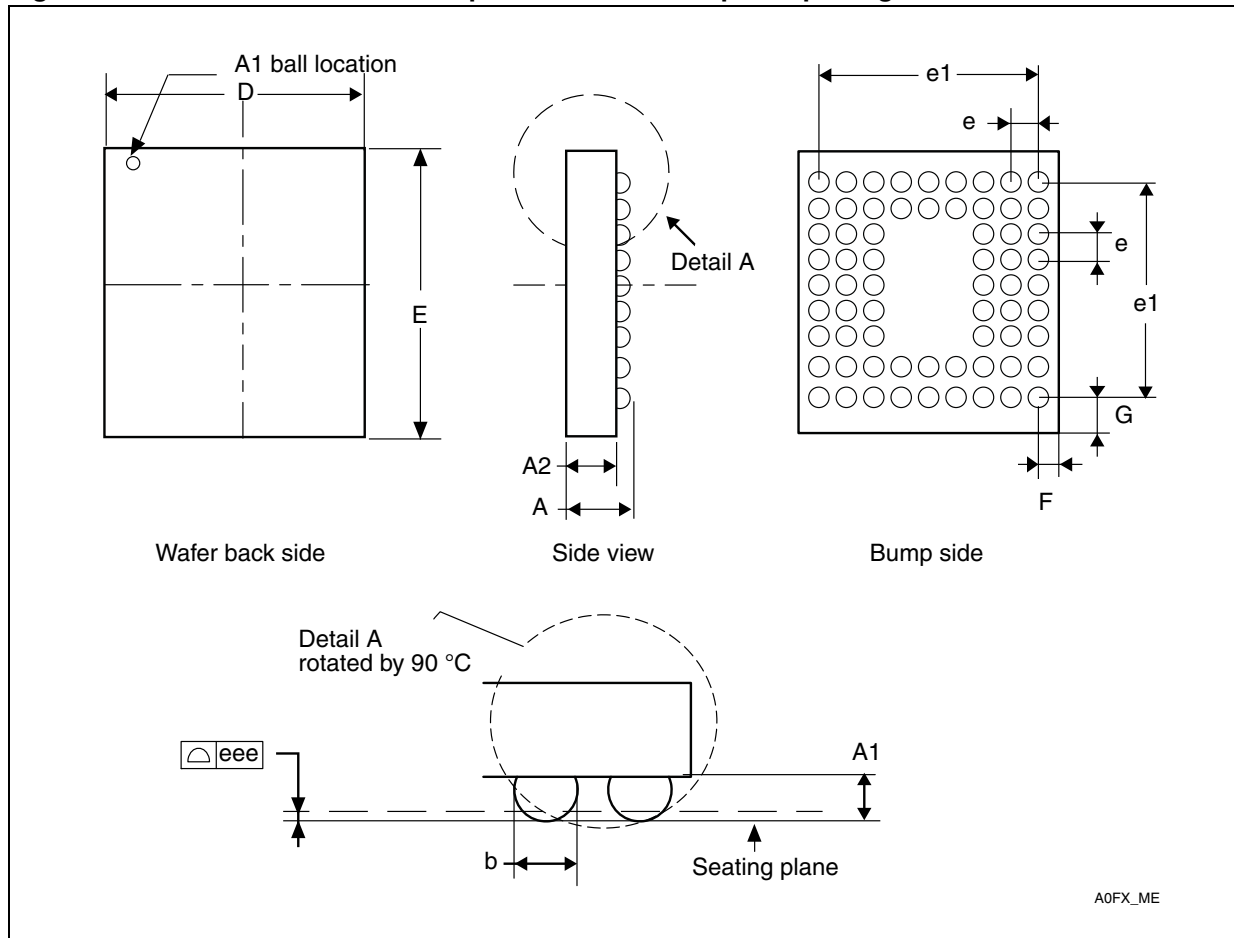
1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 78. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-----------------------|--------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | | 12.000 | | | 0.4724 | |
| D1 | | 10.000 | | | 0.3937 | |
| E | | 12.000 | | | 0.4724 | |
| E1 | | 10.000 | | | 0.3937 | |
| e | | 0.500 | | | 0.0197 | |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| N | Number of pins | | | | | |
| | 64 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 67. WLCSP64+2 - 0.400 mm pitch wafer level chip size package outline



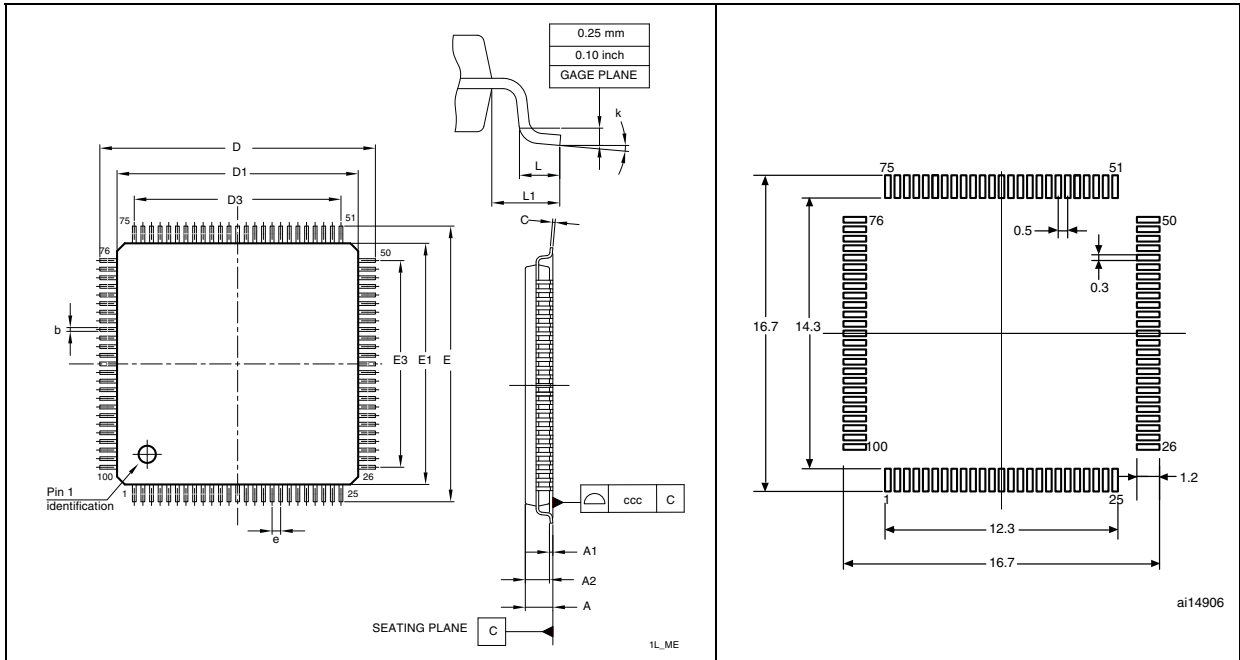
1. Drawing is not to scale.

Table 79. WLCSP64+2 - 0.400 mm pitch wafer level chip size package mechanical data

| Symbol | millimeters | | | inches | | |
|--------|-------------|-------|-------|--------|--------|--------|
| | Typ | Min | Max | Typ | Min | Max |
| A | 0.570 | 0.520 | 0.620 | 0.0224 | 0.0205 | 0.0244 |
| A1 | 0.190 | 0.170 | 0.210 | 0.0075 | 0.0067 | 0.0083 |
| A2 | 0.380 | 0.350 | 0.410 | 0.0150 | 0.0138 | 0.0161 |
| b | 0.270 | 0.240 | 0.300 | 0.0106 | 0.0094 | 0.0118 |
| D | 3.674 | 3.654 | 3.694 | 0.1446 | 0.1439 | 0.1454 |
| E | 4.006 | 3.986 | 4.026 | 0.1577 | 0.1569 | 0.1585 |
| e | 0.400 | | | 0.0157 | | |
| e1 | 3.200 | | | 0.1260 | | |
| F | 0.237 | | | 0.0093 | | |
| G | 0.403 | | | 0.0159 | | |
| eee | | 0.050 | | | 0.0020 | |

Figure 68. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline⁽¹⁾

Figure 69. Recommended footprint⁽¹⁾⁽²⁾



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 80. LQFP100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|--------|--------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| D1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| D3 | | 12.000 | | | 0.4724 | |
| E | 15.80v | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| E1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| E3 | | 12.000 | | | 0.4724 | |
| e | | 0.500 | | | 0.0197 | |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | 0.080 | | | 0.0031 | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 70. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline⁽¹⁾

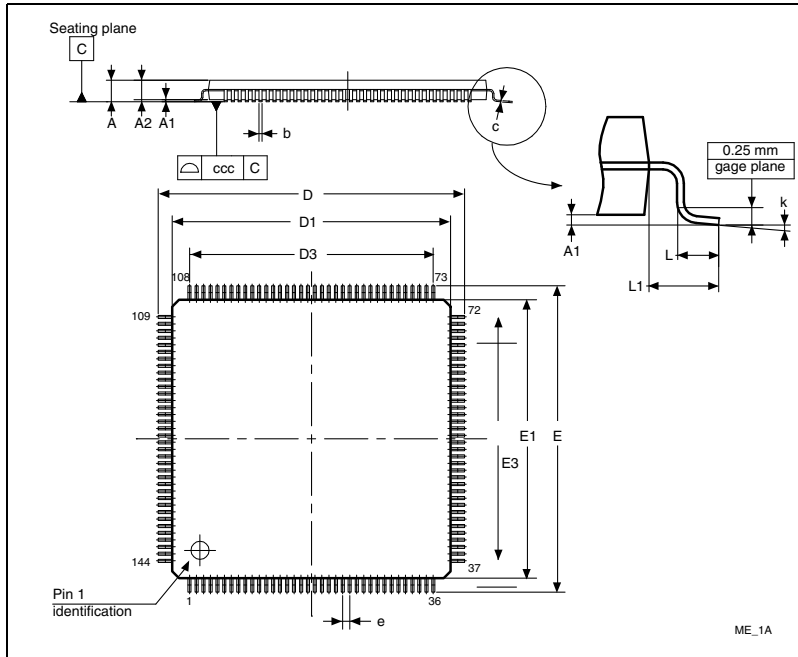
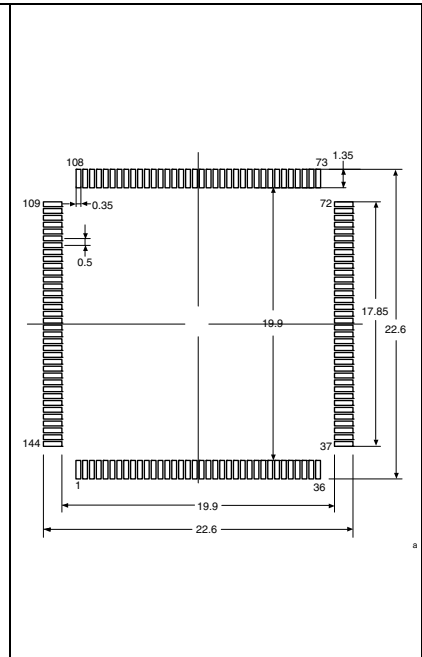


Figure 71. Recommended footprint⁽¹⁾⁽²⁾



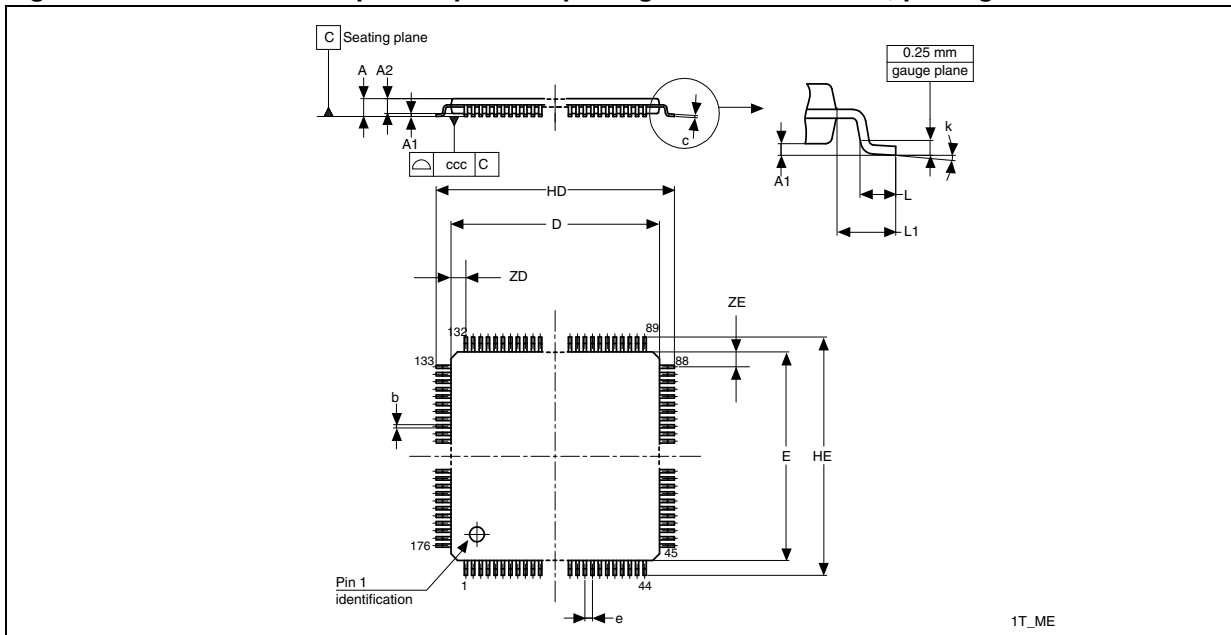
1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 81. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|--------|--------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.874 |
| D1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| D3 | | 17.500 | | | 0.689 | |
| E | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| E1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| E3 | | 17.500 | | | 0.6890 | |
| e | | 0.500 | | | 0.0197 | |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | | 0.080 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 72. LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm, package outline



1. Drawing is not to scale.

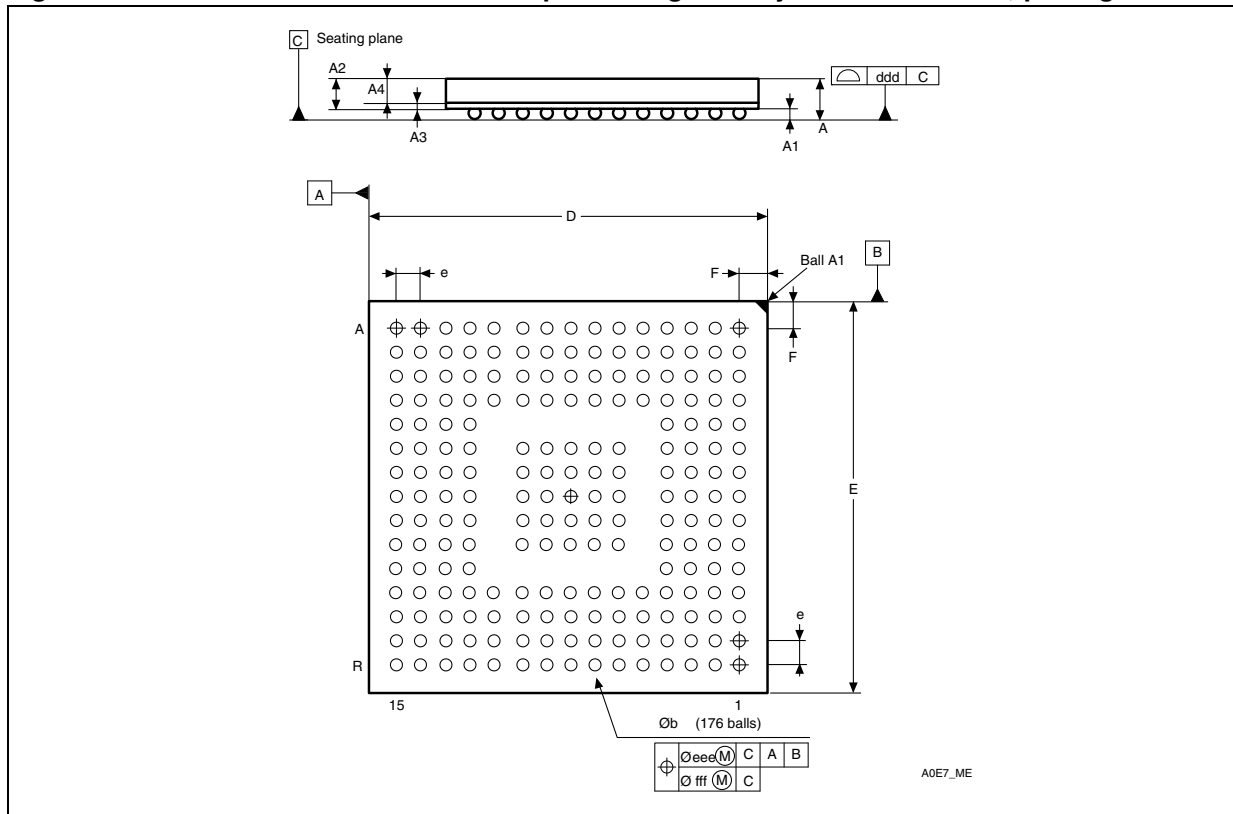
Table 82. LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|------------------|-------------|-------|--------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | | 1.450 | 0.0531 | | 0.0571 |
| b | 0.170 | | 0.270 | 0.0067 | | 0.0106 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | 23.900 | | 24.100 | 0.9409 | | 0.9488 |
| E | 23.900 | | 24.100 | 0.9409 | | 0.9488 |
| e | | 0.500 | | | 0.0197 | |
| HD | 25.900 | | 26.100 | 1.0197 | | 1.0276 |
| HE | 25.900 | | 26.100 | 1.0197 | | 1.0276 |
| L ⁽²⁾ | 0.450 | | 0.750 | 0.0177 | | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| ZD | | 1.250 | | | 0.0492 | |
| ZE | | 1.250 | | | 0.0492 | |
| k | 0° | | 7° | 0° | | 7° |
| ccc | 0.080 | | | 0.0031 | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. L dimension is measured at gauge plane at 0.25 mm above the seating plane.

Figure 73. UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline



1. Drawing is not to scale.

Table 83. UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|--------|--------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.460 | 0.530 | 0.610 | 0.0181 | 0.0209 | 0.0240 |
| A1 | 0.050 | 0.080 | 0.110 | 0.002 | 0.0031 | 0.0043 |
| A2 | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| A3 | 0.130 | | | 0.0051 | | |
| A4 | 0.270 | 0.320 | 0.370 | 0.0106 | 0.0126 | 0.0146 |
| b | 0.300 | 0.350 | 0.400 | 0.0118 | 0.0138 | 0.0157 |
| D | 9.950 | 10.000 | 10.050 | 0.3740 | 0.3937 | 0.3957 |
| E | 9.950 | 10.000 | 10.050 | 0.3740 | 0.3937 | 0.3957 |
| e | 0.600 | 0.650 | 0.700 | 0.0236 | 0.0256 | 0.0276 |
| F | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| ddd | 0.120 | | | 0.0047 | | |
| eee | 0.150 | | | 0.0059 | | |
| fff | 0.080 | | | 0.0031 | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.2 Thermal characteristics

The maximum chip-junction temperature, $T_J \text{ max}$, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A \text{ max}$ is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D \text{ max}$ is the sum of $P_{INT} \text{ max}$ and $P_{I/O} \text{ max}$ ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- $P_{INT} \text{ max}$ is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O} \text{ max}$ represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 84. Package thermal characteristics

| Symbol | Parameter | Value | Unit |
|---------------|---|-------|------|
| Θ_{JA} | Thermal resistance junction-ambient LQFP 64 - 10 × 10 mm / 0.5 mm pitch | 45 | °C/W |
| | Thermal resistance junction-ambient WLCSP64+2 - 0.400 mm pitch | 51 | |
| | Thermal resistance junction-ambient LQFP 100 - 14 × 14 mm / 0.5 mm pitch | 46 | |
| | Thermal resistance junction-ambient LQFP 144 - 20 × 20 mm / 0.5 mm pitch | 40 | |
| | Thermal resistance junction-ambient LQFP 176 - 24 × 24 mm / 0.5 mm pitch | 38 | |
| | Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.5 mm pitch | 39 | |

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

7 Part numbering

Table 85. Ordering information scheme

| | | | | | | | | |
|---|-------|---|-----|---|---|---|---|-----|
| Example: | STM32 | F | 215 | R | E | T | 6 | xxx |
| Device family STM32 = ARM-based 32-bit microcontroller | | | | | | | | |
| Product type F = general-purpose | | | | | | | | |
| Device subfamily 215 = STM32F21x, connectivity, USB OTG FS/HS, camera interface, cryptographic acceleration 217 = STM32F21x, connectivity, USB OTG FS/HS, camera interface, cryptographic acceleration, Ethernet | | | | | | | | |
| Pin count R = 64 pins or 66 pins ⁽¹⁾ V = 100 pins Z = 144 pins I = 176 pins ⁽²⁾ | | | | | | | | |
| Flash memory size E = 512 Kbytes of Flash memory G = 1024 Kbytes of Flash memory | | | | | | | | |
| Package T = LQFP H = UFBGA Y = WLCSP | | | | | | | | |
| Temperature range 6 = Industrial temperature range, -40 to 85 °C. 7 = Industrial temperature range, -40 to 105 °C. | | | | | | | | |
| Options xxx = programmed parts TR = tape and reel | | | | | | | | |

1. The 66 pins is available on WLCSP package only.
2. The LQFP176 package is not in production. It is available only for development.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Appendix A Application block diagrams

A.1 Main applications versus package

Table 86 gives examples of configurations for each package.

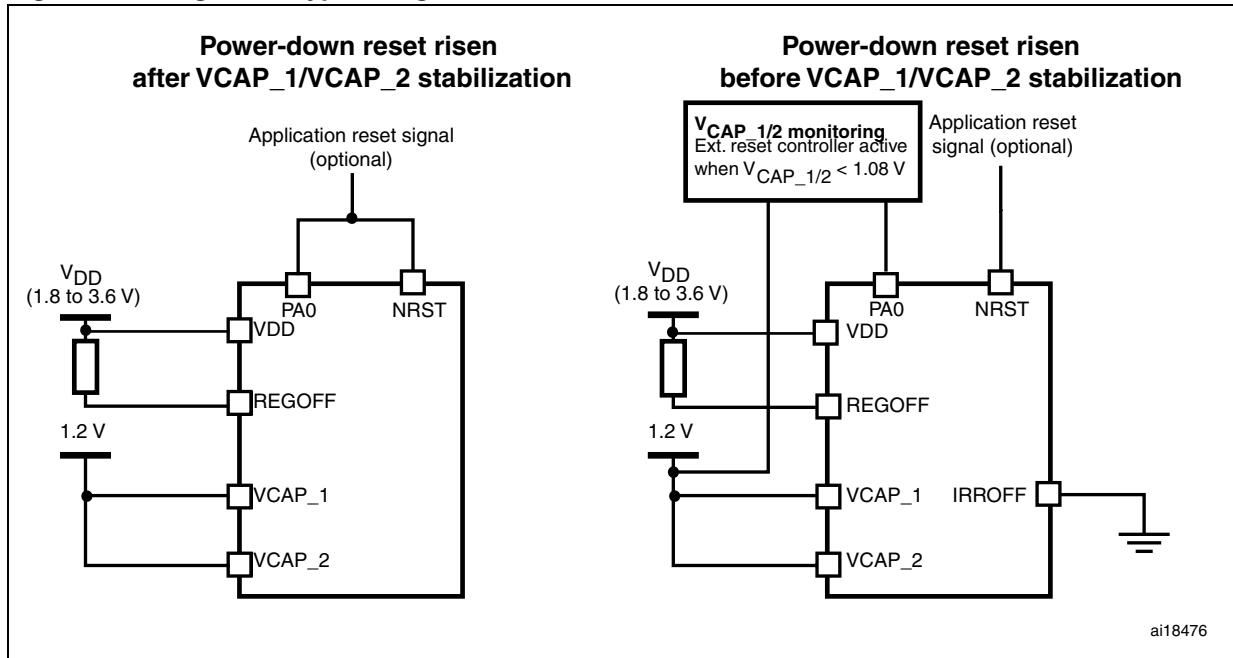
Table 86. Main applications versus package for STM32F217xx microcontrollers⁽¹⁾

| | | 64 pins | | | 100 pins | | | | 144 pins | | | | 176 pins | |
|----------------------|---------------|--------------|--------------|----------|--------------|--------------|------------------|------------------|--------------|------------------|------------------|------------------|------------------|------------------|
| | | Config 1 | Config 2 | Config 3 | Config 1 | Config 2 | Config 3 | Config 4 | Config 1 | Config 2 | Config 3 | Config 4 | Config 1 | Config 2 |
| USB 1 | OTG FS | X | X | X | X | X | X | - | X | | X | | X | |
| | FS | X | X | X | X | X | X | X | X | X | X | X | X | |
| USB 2 | HS ULPI | - | - | - | X | - | - | - | X | X | | | X | X |
| | OTGFS | - | - | - | X | | | | X | X | | | X | X |
| | FS | - | - | - | X | X | X | X | X | X | X | X | X | X |
| Ethernet | MII | - | - | - | - | - | X | X | | | X | X | X | X |
| | RMI | - | - | - | - | X | X | X | X | X | X | X | X | X |
| SPI/I2S2 SPI/I2S3 | | - | X | - | - | X | X | X | X | X | X | X | X | X |
| SDIO | SDIO | | | - | | | | X | | X | | X | X | X |
| DCMI | 8bits Data | SDIO or DCMI | SDIO or DCMI | - | SDIO or DCMI | SDIO or DCMI | SDIO or DCMI | X | SDIO or DCMI | SDIO or DCMI | SDIO or DCMI | X | SDIO or DCMI | X |
| | 10bits Data | | | - | | | | X | | | | X | | |
| | 12bits Data | | | - | | | | X | | | | X | | |
| | 14bits Data | - | - | - | - | - | - | - | X | | X | X | X | |
| FSMC | NOR/RAM Muxed | - | - | - | X | X | X | X | X | X | X | X | X | X |
| | NOR/RAM | - | - | - | | | | | X | X | X | X | X | X |
| | NAND | - | - | - | X | X | X ^{*22} | X ^{*19} | X | X ^{*19} | X ^{*22} | X ^{*19} | X ^{*22} | X ^{*22} |
| | CF | - | - | - | - | - | - | - | X | X | X | X | X | X |
| CAN | | - | X | X | - | X | X | X | - | - | X | X | - | X |

1. X^{*y}: FSMC address limited to “y”.

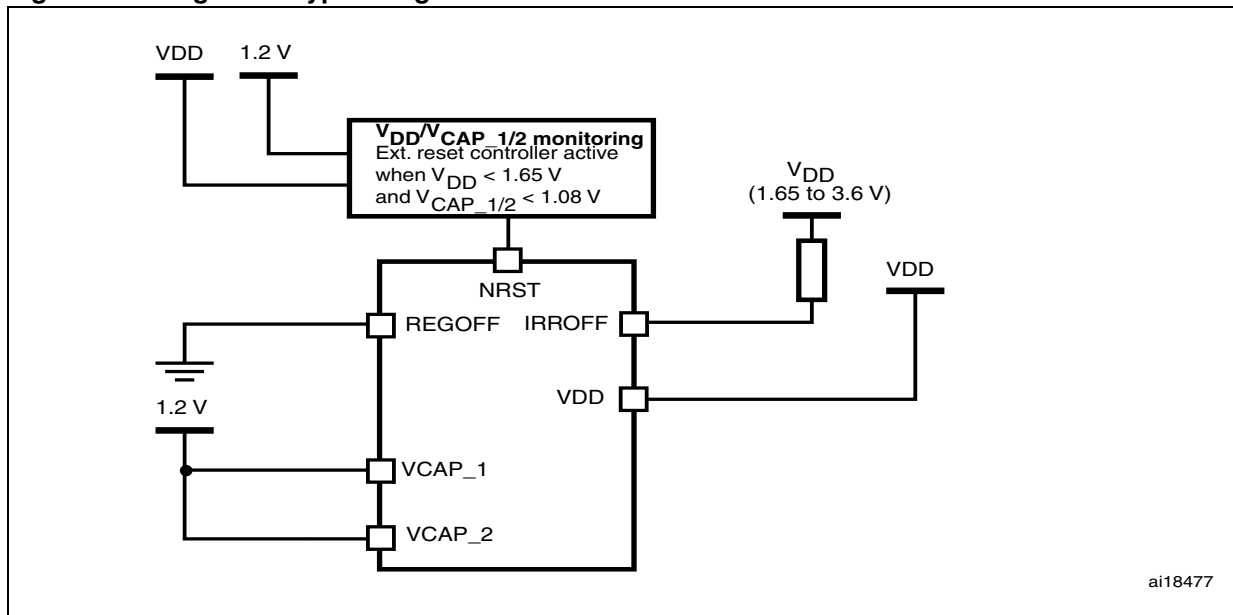
A.2 Application example with regulator off

Figure 74. Regulator bypass/regulator off



1. This mode is available only on UFBGA176 and WLCS64+2 packages.

Figure 75. Regulator bypass/regulator off and internal reset off



1. This mode is available only on WLCS64+2 package.

A.3 USB OTG full speed (FS) interface solutions

Figure 76. USB OTG FS peripheral-only connection

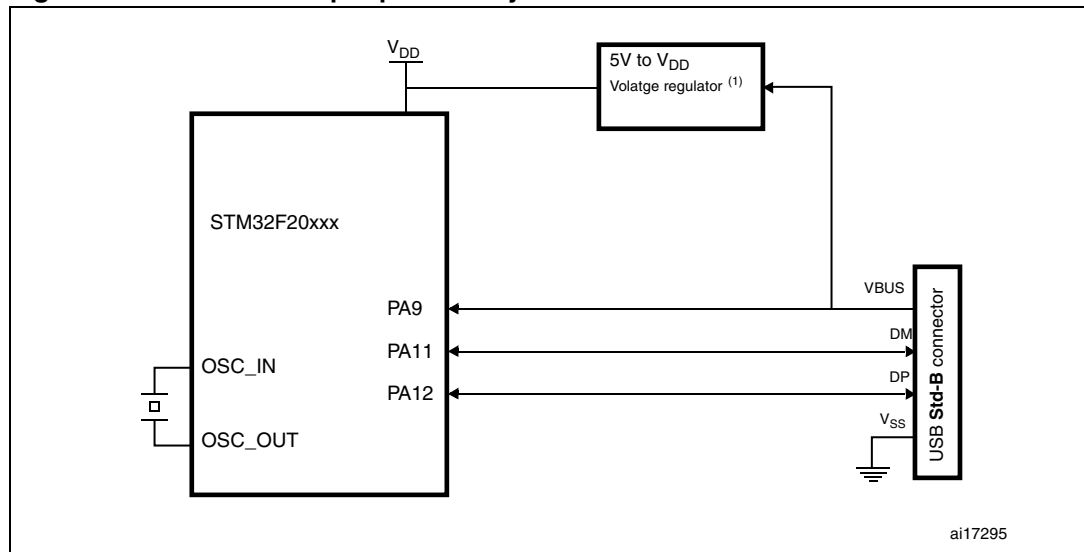
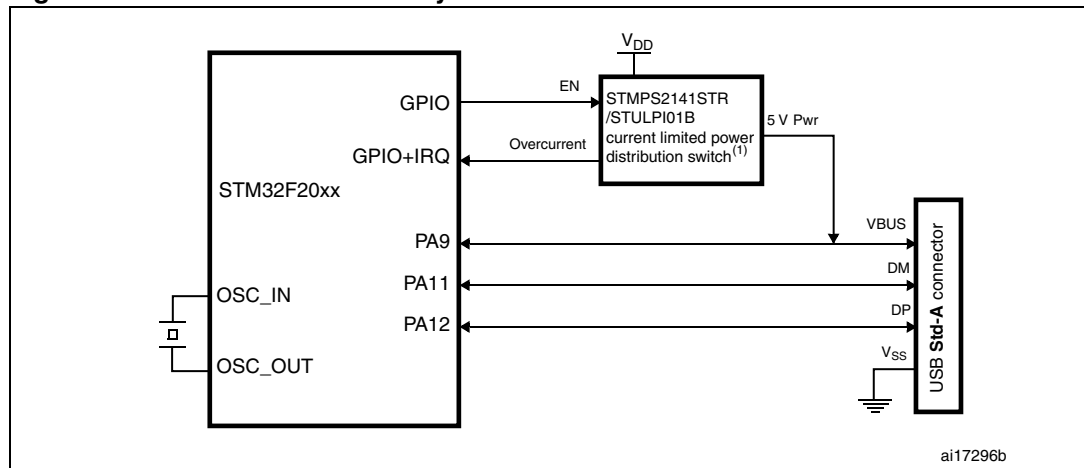
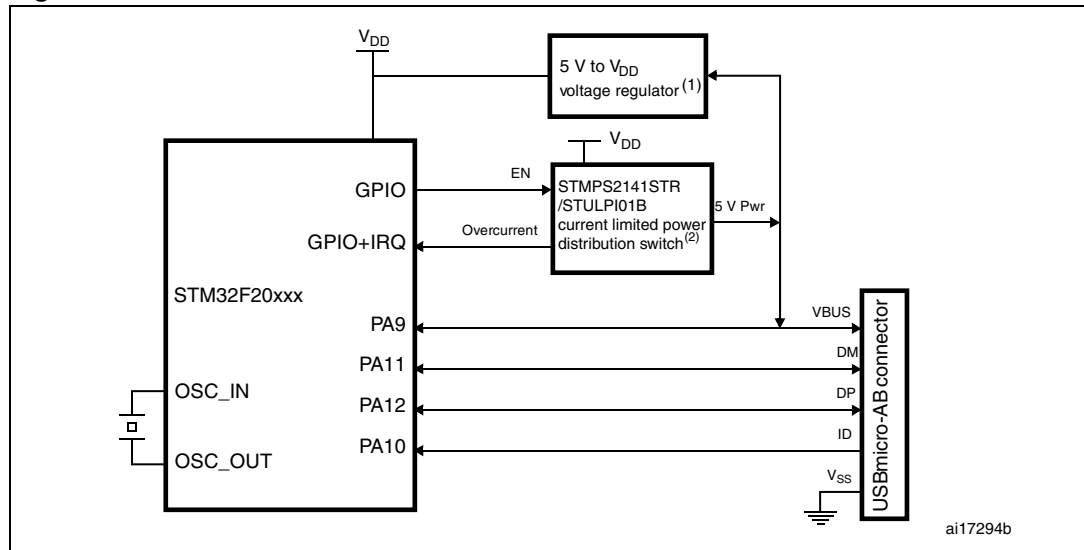


Figure 77. USB OTG FS host-only connection



1. STMP2141STR/STULPI01B needed only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.

Figure 78. OTG FS connection dual-role with internal PHY



1. External voltage regulator only needed when building a V_{BUS} powered device.
2. STMP2141STR/STULPI01B needed only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
3. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

A.4 USB OTG high speed (HS) interface solutions

Figure 79. USB OTG HS peripheral-only connection

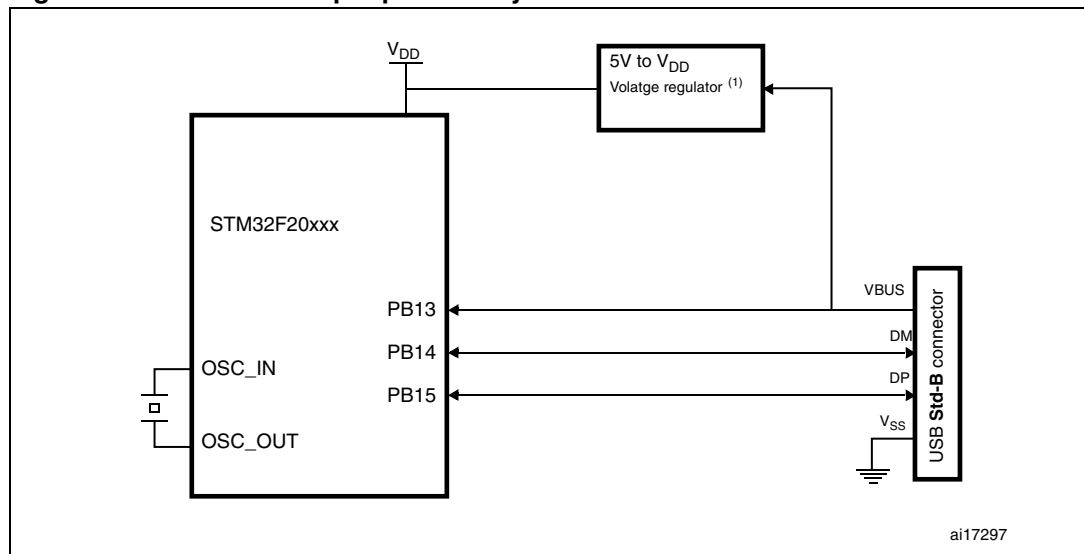
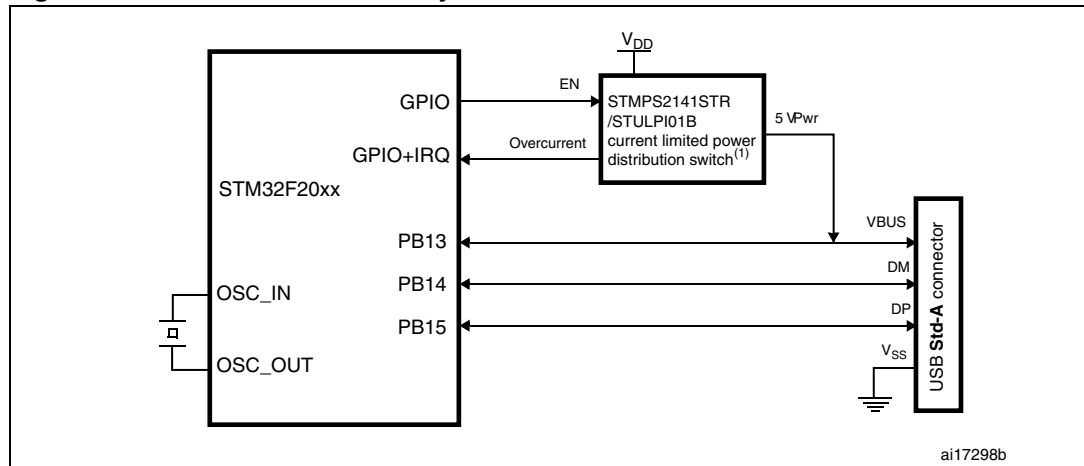
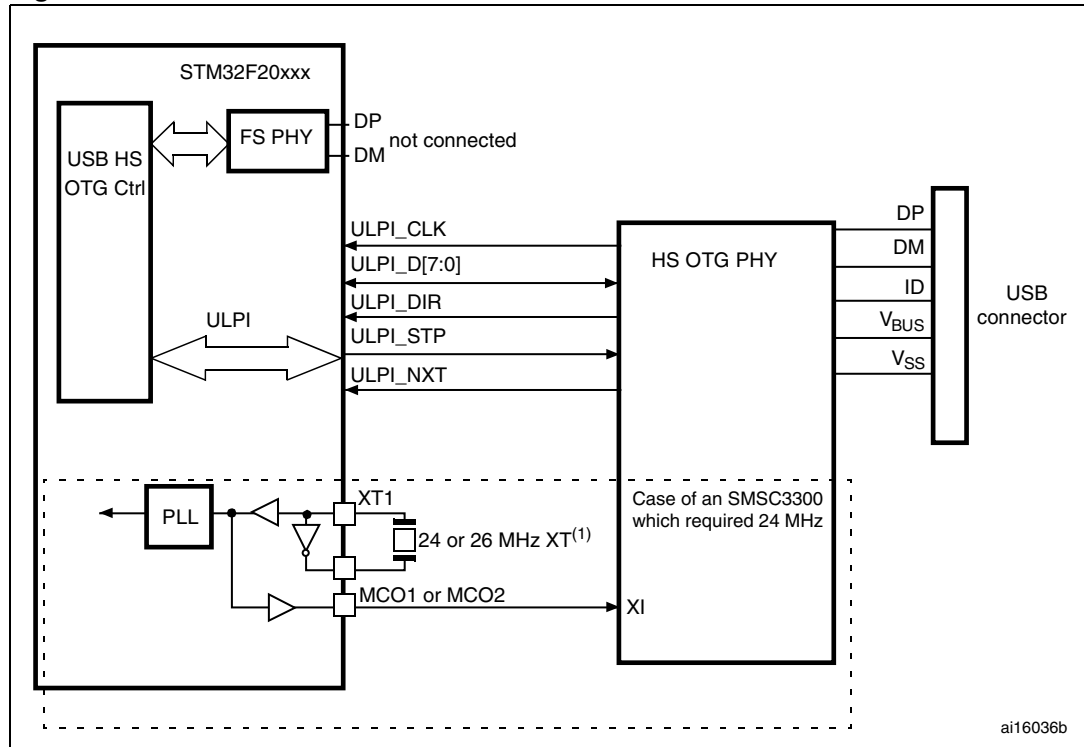


Figure 80. USB OTG HS host-only connection



1. STMP2141STR/STULPI01B needed only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.

Figure 81. OTG HS connection dual-role with external PHY



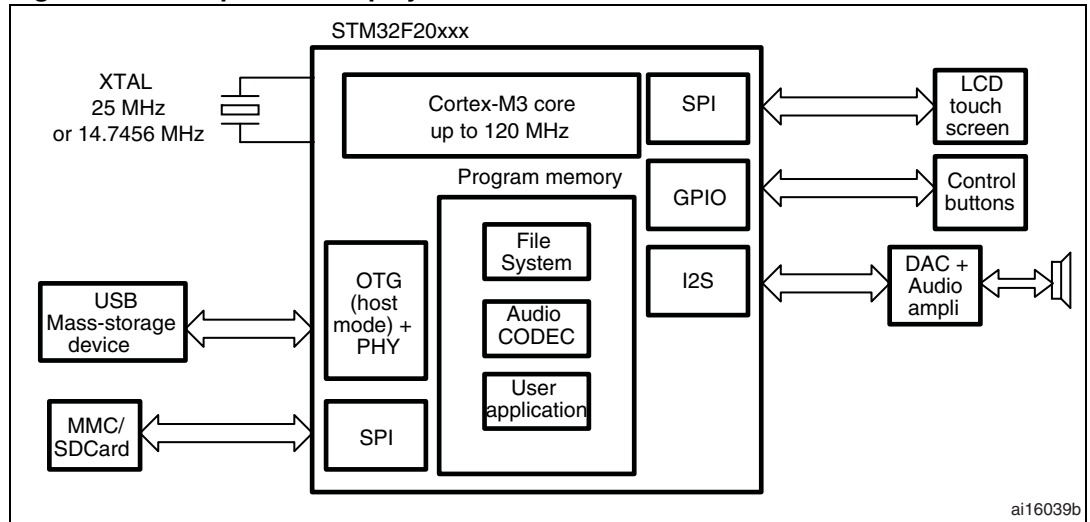
1. It is possible to use MCO1 or MCO2 to save a crystal. It is however not mandatory to clock the STM32F21x with a 24 or 26 MHz crystal when using USB HS. The above figure only shows an example of a possible connection.

A.5 Complete audio player solutions

Two solutions are offered, illustrated in [Figure 82](#) and [Figure 83](#).

[Figure 82](#) shows storage media to audio DAC/amplifier streaming using a software Codec. This solution implements an audio crystal to provide audio class I²S accuracy on the master clock (0.5% error maximum, see the Serial peripheral interface section in the reference manual for details).

Figure 82. Complete audio player solution 1



[Figure 83](#) shows storage media to audio Codec/amplifier streaming with SOF synchronization of input/output audio streaming using a hardware Codec.

Figure 83. Complete audio player solution 2

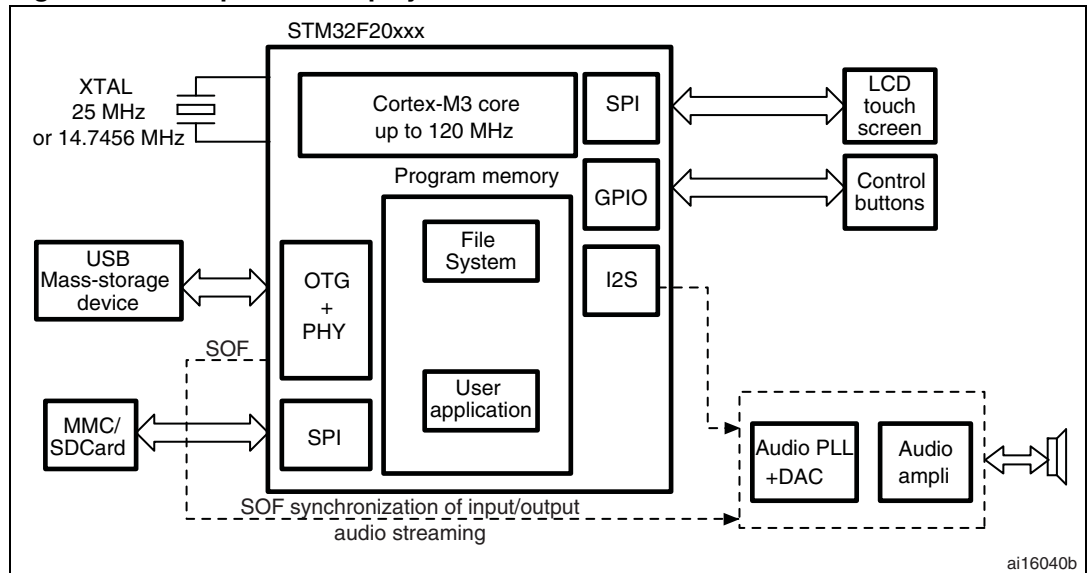


Figure 84. Audio player solution using PLL, PLLI2S, USB and 1 crystal

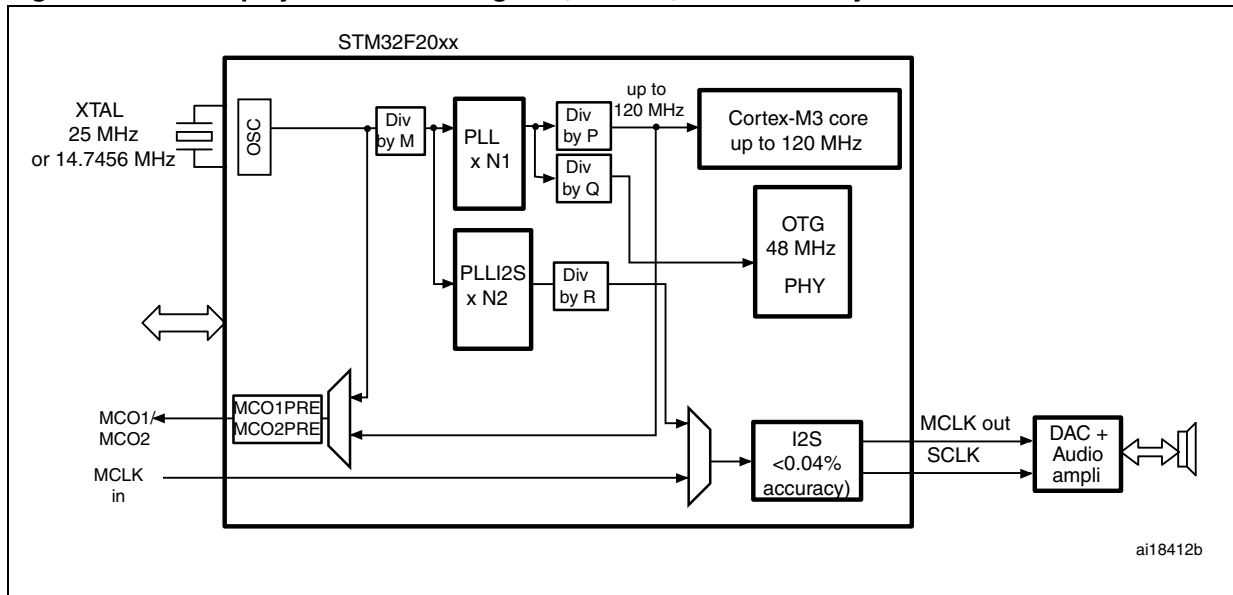


Figure 85. Audio PLL (PLLI2S) providing accurate I2S clock

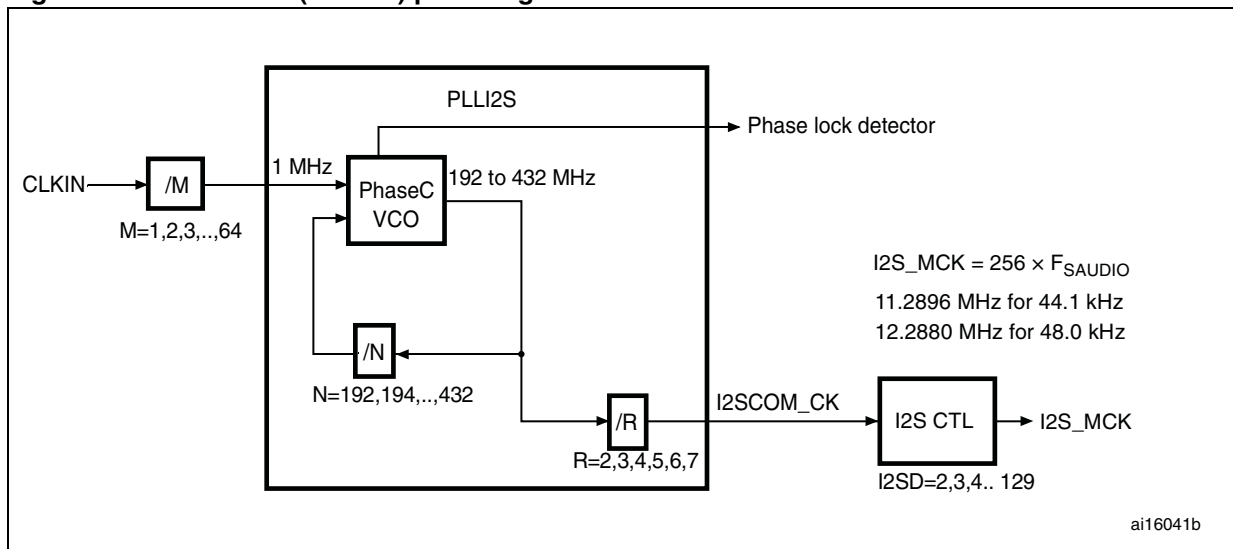
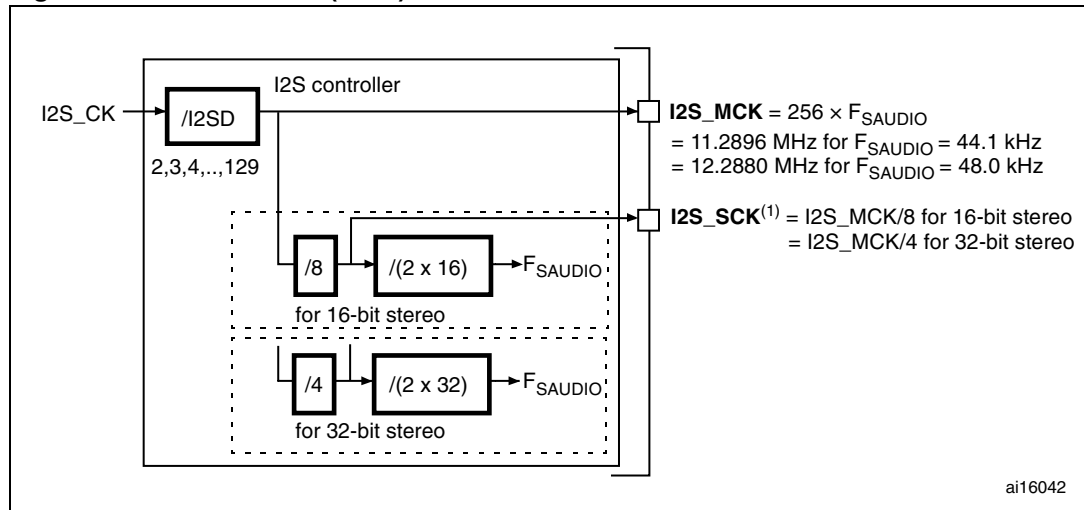
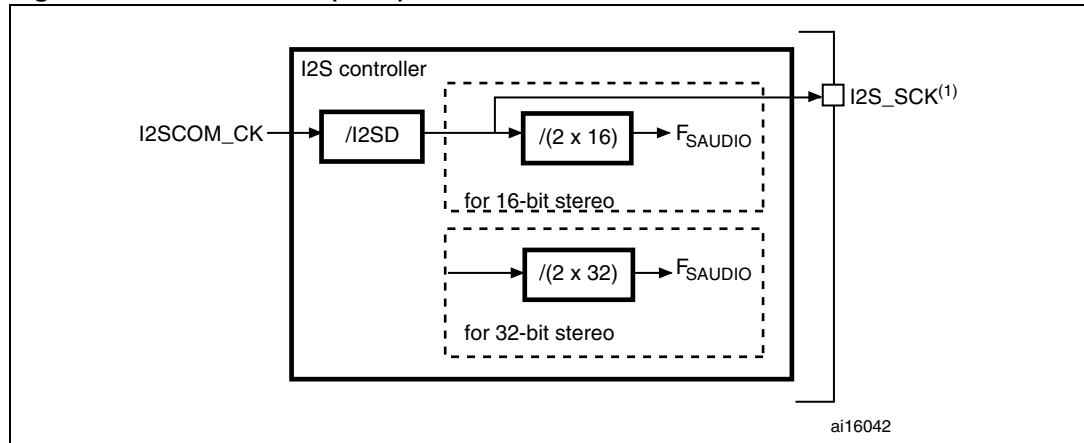


Figure 86. Master clock (MCK) used to drive the external audio DAC



1. $I2S_SCK$ is the I2S serial clock to the external audio DAC (not to be confused with $I2S_CK$).

Figure 87. Master clock (MCK) not used to drive the external audio DAC



1. $I2S_SCK$ is the I2S serial clock to the external audio DAC (not to be confused with $I2S_CK$).

Revision history

Table 87. Document revision history

| Date | Revision | Changes |
|-------------|----------|------------------|
| 02-Feb-2010 | 1 | Initial release. |

Table 87. Document revision history (continued)

| Date | Revision | Changes |
|-------------|----------|---|
| 13-Jul-2010 | 2 | <p>Updated datasheet status to PRELIMINARY DATA. Renamed high-speed SRAM, system SRAM. Added UFBGA176 package, and note 1 related to LQFP176 package in Table 2, Figure 13, and Table 85. Added information on ART accelerator and audio PLL (PLLI2S). Added Table 4: USART feature comparison. Several updates on Table 5: STM32F21x pin and ball definitions and Table 6: Alternate function mapping. ADC, DAC, oscillator, RTC_AF, WKUP and VBUS signals removed from alternate functions and moved to the “other functions” column in Table 5: STM32F21x pin and ball definitions. TRACESWO added in Figure 4: STM32F21x block diagram, Table 5: STM32F21x pin and ball definitions, and Table 6: Alternate function mapping. XTAL oscillator frequency updated on cover page, in Figure 4: STM32F21x block diagram and in Section 2.2.12: External interrupt/event controller (EXTI). Updated list of peripherals used for boot mode in Section 2.2.14: Boot modes. Added Regulator bypass mode in Section 2.2.17: Voltage regulator, and Section 5.3.3: Operating conditions at power-up / power-down in regulator bypass mode. Updated Section 2.2.18: Real-time clock (RTC), backup SRAM and backup registers. Added Note Note in Section 2.2.19: Low-power modes. Added SPI TI protocol in Section 2.2.28: Serial peripheral interface (SPI). Updated Section 2.2.33: Universal serial bus on-the-go full-speed (OTG_FS), and Section 2.2.34: Universal serial bus on-the-go high-speed (OTG_HS). Added Section 5: Electrical characteristics, and Section 6.2: Thermal characteristics. Updated Table 82: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm package mechanical data and Figure 72: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm, package outline. Added Table 86: Main applications versus package for STM32F217xx microcontrollers in A.1: Main applications versus package. Updated figures in Appendix A.3: USB OTG full speed (FS) interface solutions and A.4: USB OTG high speed (HS) interface solutions. Updated Figure 84: Audio player solution using PLL, PLLI2S, USB and 1 crystal and Figure 85: Audio PLL (PLLI2S) providing accurate I2S clock.</p> |

Table 87. Document revision history (continued)

| Date | Revision | Changes |
|-------------|----------|---|
| 25-Nov-2010 | 3 | <p>Added random number generation feature. Added trademark for ART accelerator and updated Section 2.2.3: Adaptive real-time memory accelerator (ART Accelerator™).</p> <p>Added WLCSP66 (64+2) package. Added note 1 related to LQFP176 on cover page.</p> <p>Update I/Os in Section : Features.</p> <p>Updated Table 5: Multi-AHB matrix.</p> <p>Added case of BOR inactivation using IRROFF on WLCSP devices in Section 2.2.16: Power supply supervisor.</p> <p>Reworked Section 2.2.17: Voltage regulator to clarify regulator off modes. Added Section 2.2.20: V_{BAT} operation.</p> <p>Modified V_{DD_3} pin in Table 5: STM32F21x pin and ball definitions, and added note related to the FSMC_NL pin.</p> <p>Renamed BYPASS-REG REGOFF, and add IRROFF pin.</p> <p>Changed V_{SS_SA} to V_{SS}, and V_{DD_SA} pin reserved for future use.</p> <p>Updated maximum HSE crystal frequency to 26 MHz.</p> <p>USART4/5 renamed UART4/5. USART4 pins remained UART4 in Table 5: STM32F21x pin and ball definitions. Updated LIN and IrDA features for UART4/5 in Table 4: USART feature comparison.</p> <p>Section 5.2: Absolute maximum ratings: Updated V_{IN} minimum and maximum values and note for non-five-volt tolerant pins in Table 7: Voltage characteristics. Updated I_{INJ(PIN)} maximum values and related notes in Table 8: Current characteristics.</p> <p>Updated V_{DDA} minimum value in Table 10: General operating conditions.</p> <p>Added Note 2 and updated Maximum CPU frequency in Table 11: Limitations depending on the operating power supply range; and added Figure 20: Number of wait states versus f_{CPU} and V_{DD} range.</p> <p>Renamed Brownout Low, medium and High reset thresholds, Renamed V_{BORL}/V_{BORM}/V_{BORH}, V_{BOR1}/V_{BOR2}/V_{BOR3} in Table 14: Embedded reset and power control block characteristics.</p> <p>Changed f_{LSI} typical value in Table 27: LSI oscillator characteristics.</p> <p>Changed f_{OSC_IN} maximum value in Table 24: HSE 4-26 MHz oscillator characteristics.</p> <p>Changed f_{PLL_IN} maximum value in Table 29: Main PLL characteristics, and updated jitter parameters in Table 30: PLLI2S (audio PLL) characteristics.</p> <p>Section 5.3.14: I/O port characteristics: updated V_{IH} and V_{IL} in Table 40: I/O static characteristics.</p> <p>Added Note 1 below Table 41: Output voltage characteristics.</p> <p>Updated R_{PD} and R_{PU} parameter description in Table 51: USB OTG FS DC electrical characteristics.</p> <p>Updated V_{REF+} minimum value in Table 59: ADC characteristics.</p> <p>Updated Table 64: Embedded internal reference voltage.</p> <p>Removed Ethernet and USB2 for 64-pin devices in Table 86: Main applications versus package for STM32F217xx microcontrollers.</p> <p>Added A.2: Application example with regulator off, removed “OTG FS connection with external PHY” figure, updated Figure 77, Figure 78, and Figure 80 to add STULPI01B.</p> |

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