Opus Card
Reference Manual

Reference Manual (v1.00) December 2010

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1 Summary of Features

- Onboard Xilinx Virtex-5 FPGA
  - Model: FX30T
    - PowerPC and MicroBlaze cores
    - Hard Ethernet MAC
- Programmable Clock Generator Chip
  - Model: IDT 5V9885
    - 8 outputs with available frequencies from 0.0049 – 550 MHz
    - Output types: LVPECL, LVTTL, and LVDS
    - 12-bit Multiplier
    - 8-bit pre and 12-bit post Divider
- Onboard Xilinx Platform Flash
  - XCF132P 32 Mb PROM
- Memory Banks
  - 2 × 128 MB DDR2 Banks
- Ethernet
  - Ethernet port with 10/100 Ethernet PHY
- Secure Digital File System
  - Includes a 2 GB SD card configured with Linux image that runs on the PowerPC core
- External Connectors
  - JTAG port
  - Dual RS232 ports
  - 4 dual Pmod headers
  - 2×20 general purpose I/O header
  - Secure Digital file system
  - 8-lane PCI express edge connector
  - Reset button
- Standard Power Supply
  - Powered by a single 6-pin PCIe power connector
- Standard Dimensions
  - Card measures 4.3” × 6.9”

Figure 1-1: Opus Card

2 Overview

The Opus card is a complete development system driven by the Xilinx Virtex 5 FPGA. The card was designed with the end-purpose of running as a standalone Linux system that plugs into a host PC and is a node in a network of Opus systems. In addition to the node functionality, the Opus card also has all the necessary components to be an independent development platform.

The Virtex 5 FPGA has powerful PowerPC 440 and MicroBlaze cores, and combined with 256 MB of DDR-2 RAM, the Opus card can host a variety of applications, from peripheral management to full Linux kernels. Applications can be loaded to the card using a JTAG port, or from the available Xilinx XCF32P Flash memory. The Opus card has four peripheral module (Pmod) connectors that can host a variety of Pmod devices, such as LCD and seven segment displays, LEDs, hardware adapters (PS/2, RS-232), and many others. A 2x20 GPIO header adds additional input/output pins. The included Secure Digital port allows reading and writing to an SD filesystem, and the 10/100 Ethernet port provides the ability for the card to act as a network device.

Figure 2-1 is a block diagram that represents the Opus card interfaced with a host system. The black arrows indicate bi-directional communication, while the grey arrows are single direction.

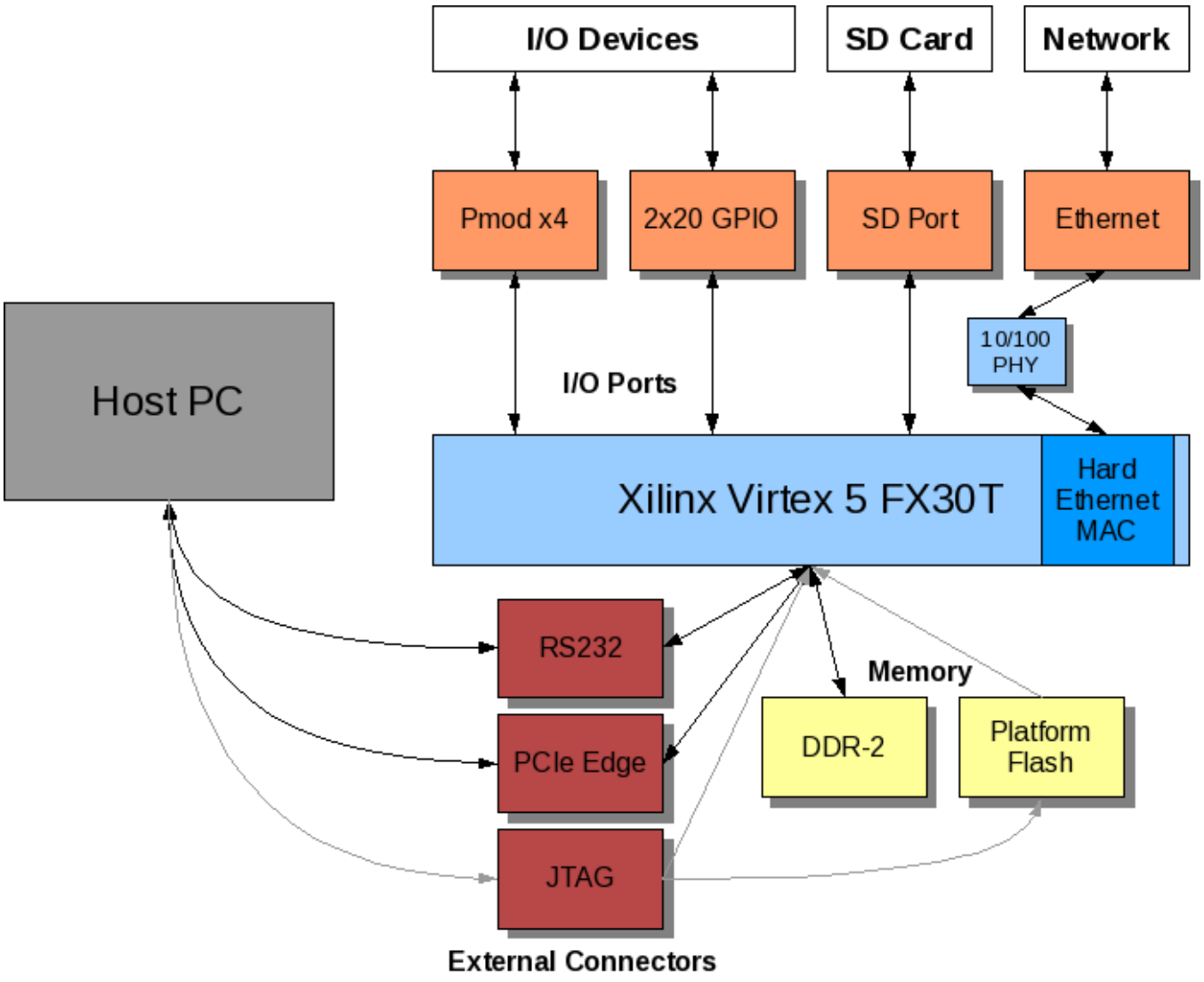
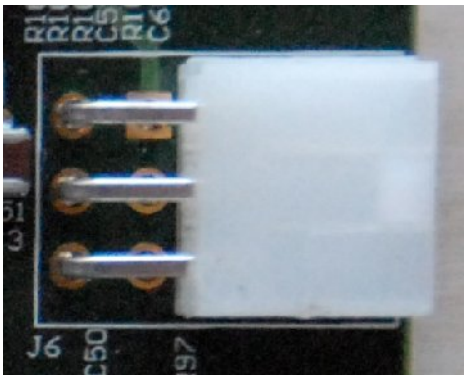


Figure 2-1: Opus Card System Block Diagram

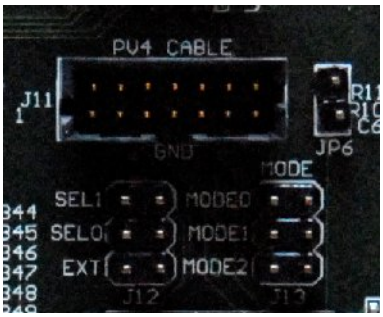


3 Power Supply

The Opus card requires a 12V 6-pin PCIe expansion card power source, available on most modern power supply units. The socket on the card is white in color and located in the upper right corner of the card, labeled as J6. The power supply should be switched off while plugging in the Opus card.

4 FPGA and Platform Flash Configuration

The Opus card must be configured before use. Configuration files, called bit files, can be generated from hardware configurations and software applications built using the Xilinx EDK. The bit files can be loaded to the FPGA in two ways: directly from a host PC through the JTAG port, or from the preloaded onboard Xilinx XCF16P platform flash memory.

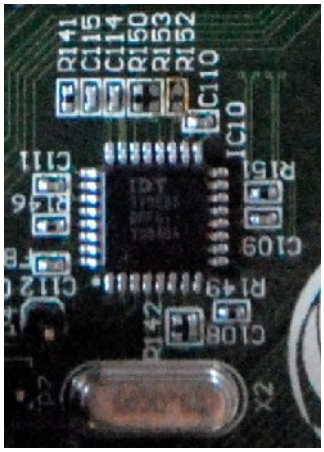


The location to load is selected by a mode jumper located at J13, directly below the JTAG port. To configure the FPGA from JTAG, the mode jumpers must remain open. In JTAG mode, the card will not perform any action when turned on or reset, but waits for a configuration file to be loaded using the Xilinx iMPACT tool. To configure the FPGA from platform flash, jumper blocks must be placed across pins 1 and 2 (MODE 0) and 3 and 4 (MODE 1) of the mode jumper J13. When the jumpers are in place to use the platform flash, the card will configure the FPGA from the bit file stored in the platform flash when powered on or reset.

Please note: The Opus card platform flash is packaged with a configuration file already loaded. This configuration file contains the manufacturing level hardware tests and Linux bootloader, and acts as a fail-safe configuration when developing with the Opus card. If the platform flash is overwritten, the original bit file can be found at the CML web site. Also note, when in JTAG mode, the FPGA will retain the configuration file until a power cycle occurs or the reset button is pressed at which point it will clear; alternately, the bit file remains in the platform flash unless it is reprogrammed, and is unaffected by power cycles.

5 Clocks

The Opus card uses a programmable clock generator chip with eight outputs and available frequency ranges of 0.0049 – 550 MHz. The chip outputs three signal types: LVPECL, LVTTL, and LVDS. The chip has a 12-bit frequency multiplier, and 8-bit pre and 12-bit post dividers.



The clock chip is programmed to the following frequencies during manufacturing:

- Pin 6: 25.00 MHz
- Pin 13: 25.00 MHz
- Pin 29: 14.30 MHz
- Pin 8: 12.00 MHz
- Differential pair pins 10 and 11: 33.00 MHz
- Differential pair pins 15 and 16: 100.00 MHz

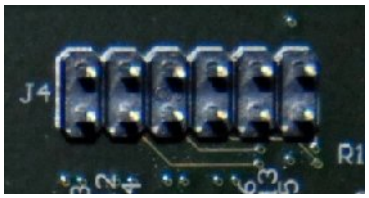
Additionally, the 50 MHz oscillator frequency can be verified by measuring the frequency at pin 3.

6 Memory

The Opus has a total of 256 MB of DDR-2 RAM, divided into two banks of 128 MB. Each bank is organized into 32 bit words, which can be written and read in bursts by enabling burst mode. In big endian format, writing a 1 to the 31st bit of the configuration register enables burst mode. The configuration register for each bank is located at the base address of the registers.

The Opus card also has 32 Mb of platform flash, which can store hardware bitstreams between power cycles. The platform flash can be programmed with the Xilinx iMPACT tool, by selecting the XCF32P in the device chain. The card can be configured to automatically load from the platform flash at power on or reset by using jumper blocks on the MODE 0 and MODE 1 pin pairs on the Mode jumper, located at J13.

7 Input/Output Ports



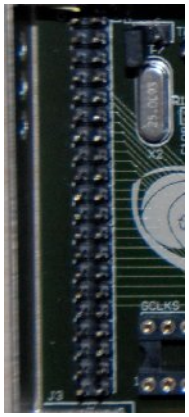
The Opus card has two serial RS232 Pmods, located at J11. Using Digilent's Pmod to RS232 adapter, which uses one of the RS232 Pmods, the pins can be used to connect to a host PC and communicate with a terminal emulator. This communication point presents a wide variety of uses, such as debugging designs, software application I/O, and more. For the included Linux system, ensure the RS-232 Pmod cable connects from pin 1 on J4 to pin 1 on the RS232 Pmod to provide the Linux system console. The port configuration should be set to 115,200 baud, 8-bits, no parity, one stop bit, and software flow control.

The Opus card also has a 2x20 general purpose I/O port, with pins that can be configured as input or output based on hardware configuration settings. The GPIO pin-out is listed in Table 7-1:

Table 7-1: 2x20 GPIO Pin-out to FPGA Pins

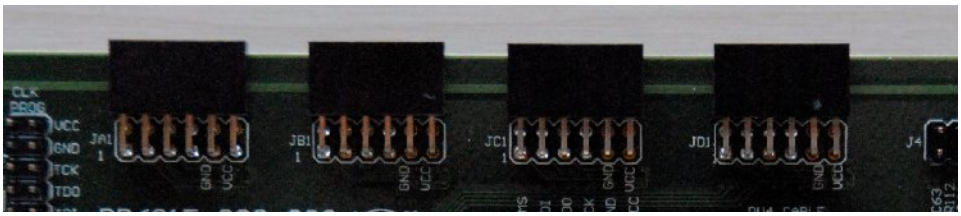
Pin 1: GND	Pin 2: VU12V0
Pin 3: VCC3V3	Pin 4: C12
Pin 5: C11	Pin 6: D11
Pin 7: D10	Pin 8: C9
Pin 9: D9	Pin 10: G9
Pin 11: F8	Pin 12: F9
Pin 13: E8	Pin 14: F7
Pin 15: C7	Pin 16: G7
Pin 17: A12	Pin 18: B12
Pin 19: B11	Pin 20: A10
Pin 21: B10	Pin 22: A9
Pin 23: B9	Pin 24: A8
Pin 25: A7	Pin 26: B7
Pin 27: B6	Pin 28: A5
Pin 29: B5	Pin 30: A4
Pin 31: B4	Pin 32: A3
Pin 33: C8	Pin 34: D8
Pin 35: E7	Pin 36: C6
Pin 37: D6	Pin 38: E6
Pin 39: E5	Pin 40: D5

The GPIO pins have an I/O level of 3.3V. They are controlled using the General Purpose I/O IP included with the Xilinx EDK. Adding the IP to a project gives access to two sets of two 32-bit software accessible registers at the base address of the GPIO IP, each set consisting of a data register and a tri-state register. Each bit in the data and tri-state register can be connected to a pin on the GPIO header. Writing a 1 to the bit in the tri-state register configures the pin as input, while writing a 0 sets it to output. Therefore, if the value of an input pin changes, its value in the data register changes; conversely, writing a value to a data register bit will change the value of the pin when configured as output.



8 Peripheral Connectors

The Opus card has four two-row Pmod headers located along its top edge at positions JA1, JB1, JC1, and JD1. These headers allow up to eight Pmods, such as those sold by Digilent, to be connected to the card at one time. These headers greatly increase the usability of the card in a variety of applications by increasing the amount of user I/O devices available.



Similar to the GPIO header, the Pmod headers have an I/O level of 3.3V, and are controlled by software-accessible registers located at a base address generated by EDK during synthesis. The first 32 bits at the base address are the data register for the Pmods, and the second 32 bits are the tri-state register. A reference design on using the Pmod headers and software accessible registers can be found at the CML web site. The pin-out for the Pmod connectors is shown in Table 8-1.

Table 8-1: Pmod Header Pin-out to FPGA Pins

Pmod 1: JA		Pmod 2: JB		Pmod 3: JC		Pmod 4: JD	
JA1: C13	JA7: G12	JB1: C18	JB7: H19	JC1: C23	JC7: C24	JD1: B26	JD7: C26
JA2: C14	JA8: G14	JB2: C19	JB8: D19	JC2: D24	JC8: H11	JD2: D25	JD8: D26
JA3: G11	JA9: C16	JB3: D20	JB9: D21	JC3: F13	JC9: F14	JD3: G17	JD9: F18
JA4: H18	JA10: C17	JB4: C22	JB10: D23	JC4: F15	JC10: F17	JD4: G19	JD10: C21