

SAM3U-EK Development Board

User Guide





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Section 1

Introduction

1.1 SAM3U Evaluation Kit

The SAM3U Evaluation Kit (SAM3U-EK) allows the evaluation of the SAM3U series devices. It has enough features to demonstrate most of the product's capabilities to the users. The SAM3U-EK also features extension connectors to allow the users to add new interfaces in case they are not on-board.

1.2 User Guide

This guide gives details on how the SAM3U-EK has been designed. It is made up of 6 sections:

- Section 1 includes references, applicable documents
- Section 2 describes the kit contents, its main features
- Section 3 provides instructions to power up the SAM3U-EK and describes how to use it.
- Section 4 describes the hardware resources, and includes default jumper and switch settings, and the schematics.
- Section 5 provides all the board schematics
- Section 6 give troubleshooting recommendations

1.3 References and Applicable Documents

Table 1-1. References and Applicable Documents

Title	Comment
SAM3U Datasheet	http://www.atmel.com/dyn/products/product_card.asp?part_id=4562

2.1 Deliverables

The Atmel® SAM3U-EK toolkit contains the following items:

- a SAM3U-EK board
- power supply
- universal input AC/DC power supply with US, Europe and UK plug adapters
- one 3V Lithium Battery type CR1225
- one USB cable
- one serial RS232 cable
- A Welcome Letter

Figure 2-1. Unpacked SAM3U-EK



Unpack and inspect the kit carefully. Contact your local Atmel distributor, should you have issues concerning the contents of the kit.

2.2 Electrostatic Warning

The SAM3U-EK board is shipped in a protective anti-static package. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the components or any other metallic element of the board.



3.1 Power up the Board

Unpack the board taking care to avoid electrostatic discharge. Unpack the power supply, select the right power plug adapter corresponding to that of your country, and insert it in the power supply.

Connect the power supply DC connector to the board and plug the power supply to an AC power plug.

The board LCD should light up and display a welcome page. Then, click or touch icons displayed on the screen and enjoy the demo.

3.2 Battery

The SAM3U-EK ships with a 3V coin battery.

This battery is not required for the board to start up.

The coin battery is provided for user convenience in case the user would like to exercise the date and time backup function of the SAM3U series devices when the board is switched off.

3.3 DevStart

The on-board NAND Flash contains “SAM3U-EK DevStart”.

It is stored in the “SAM3U-EK DevStart” folder on the USB Flash disk available when the SAM3U-EK is connected to a host computer and you click on the Flash Disk icon of the on-board demo.

Click the file “welcome.html” in this folder to launch SAM3U-EK DevStart.

SAM3U-EK DevStart guides you through installation processes of IAR™ EWARM, Keil MDK and GNU toolkits. Then, it gives you step-by-step instructions on how to rebuild a single example project and how to program it into the SAM3U-EK. Optionally, if you have a SAM-ICE™, instructions are also given about how to debug the code.

We recommend that you backup the “SAM3U-EK DevStart” folder on your computer before launching it.

3.4 Recovery Procedure

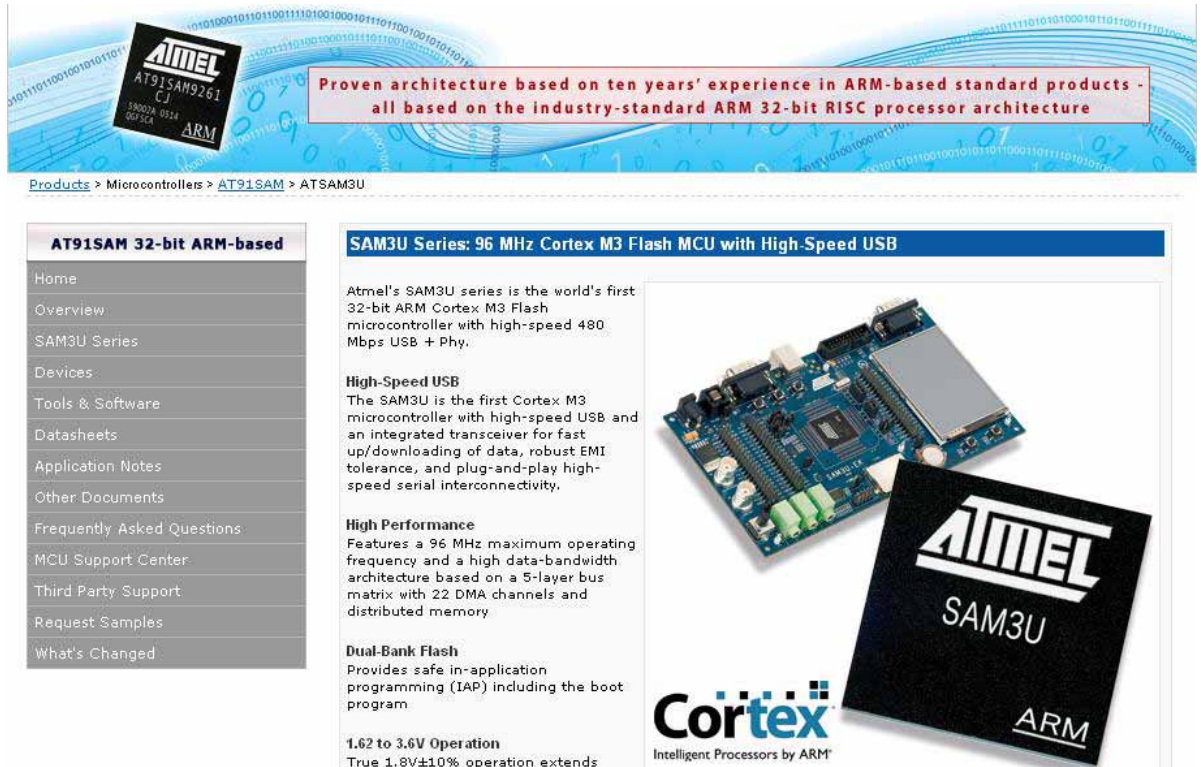
The DevStart ends by giving step-by-step instructions on how to recover the SAM3U-EK to the state as it was when shipped by Atmel.

Follow the instructions if you deleted the contents of the embedded Flash or the NAND Flash and want to recover from this situation.

3.5 Sample Code and Technical Support

After boot up, you can run some sample code or your own application on the development kit. You can download sample code and get technical support from Atmel website http://www.atmel.com/products/at91/sam3landing.asp?family_id=605

Figure 3-1. Atmel Website for SAM3U Series



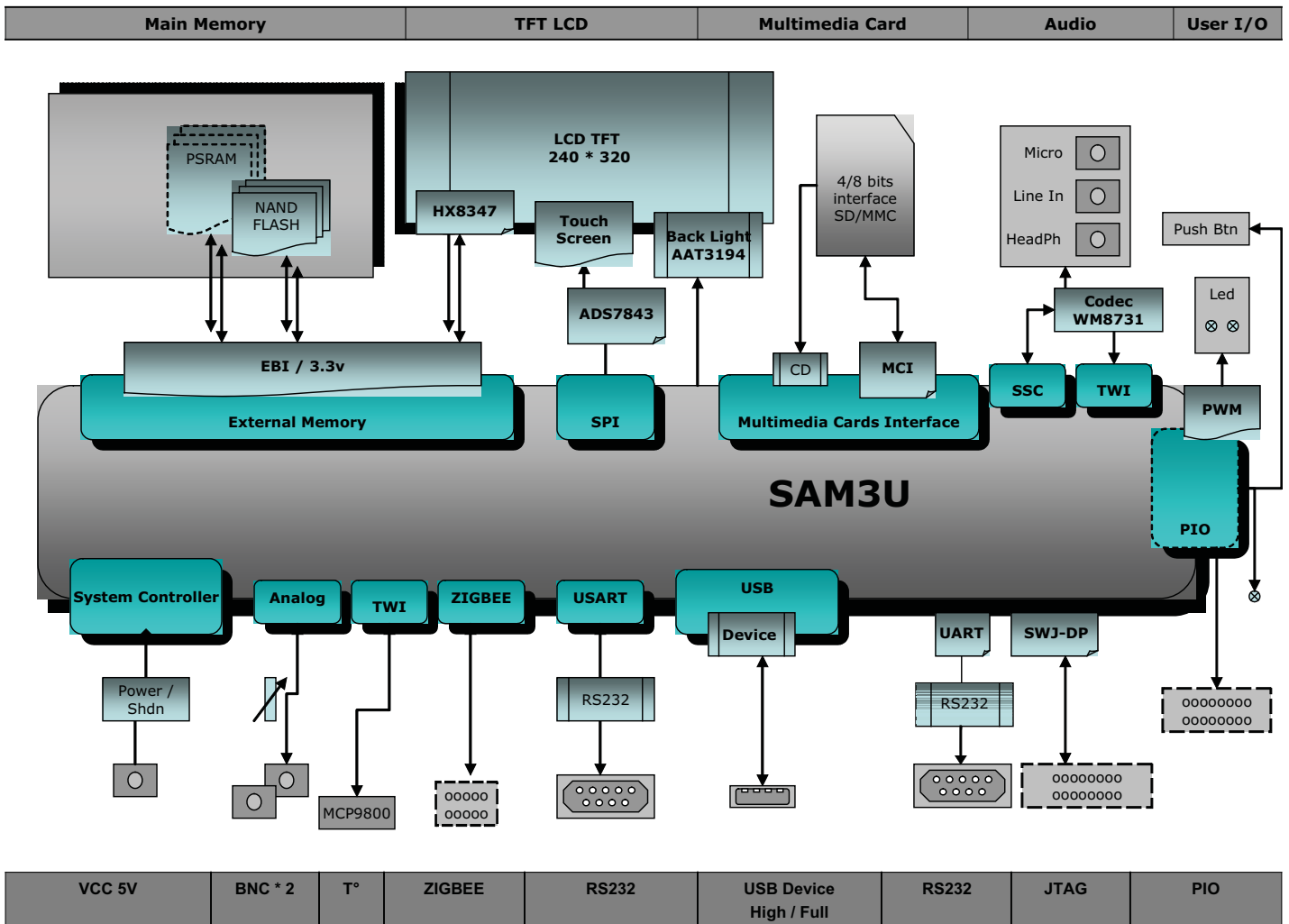
Evaluation Kit Hardware

4.1 Board Overview

This section introduces the Atmel SAM3U Evaluation Kit design. It introduces system-level concepts, such as power distribution, memory, and interface assignments.

The SAM3U-EK board is based on the integration of an ARM® Cortex®-M3 processor with on-board fast PSRAM (pseudo-static RAM), NAND-Flash and a set of popular peripherals. It is designed to provide a high performance processor evaluation solution with high flexibility for various kinds of applications.

Figure 4-1. SAM3U-EK Block Diagram



4.2 Features List

Here is the list of the main board components and interfaces:

- SAM3U4E QFP chip with optional socket footprint
- 12 MHz crystal
- 32.768 KHz crystal
- Optional SMB connector, for external system clock input
- PSRAM
- NAND-Flash
- Backup Battery
- 2.8 inch TFT color LCD display with touch-panel and backlight
- UART port with level shifter IC
- USART port with level shifter IC
- Audio codec with input and output jacks: stereo headphone out, stereo line in, mono microphone in
- SD/MMC interface
- 3-D accelerometer sensor
- Temperature sensor
- Reset and Wake-Up buttons: NRST, NRSTB, FWUP
- User buttons: Left and Right
- High Speed USB device port
- JTAG port
- On-board power regulation with shutdown control (by the SAM3 chip)
- Two user LEDs
- Power LED
- BNC connectors for ADC input
- User potentiometer connected to the ADC input
- ZigBee® connector
- 3x32 bit PIO connection interfaces (PIOA, PIOB, PIOC)

4.3 Function Blocks

4.3.1 Processor

The SAM3U-EK is equipped with a SAM3U4E in LQFP144 package.

4.3.2 Memory

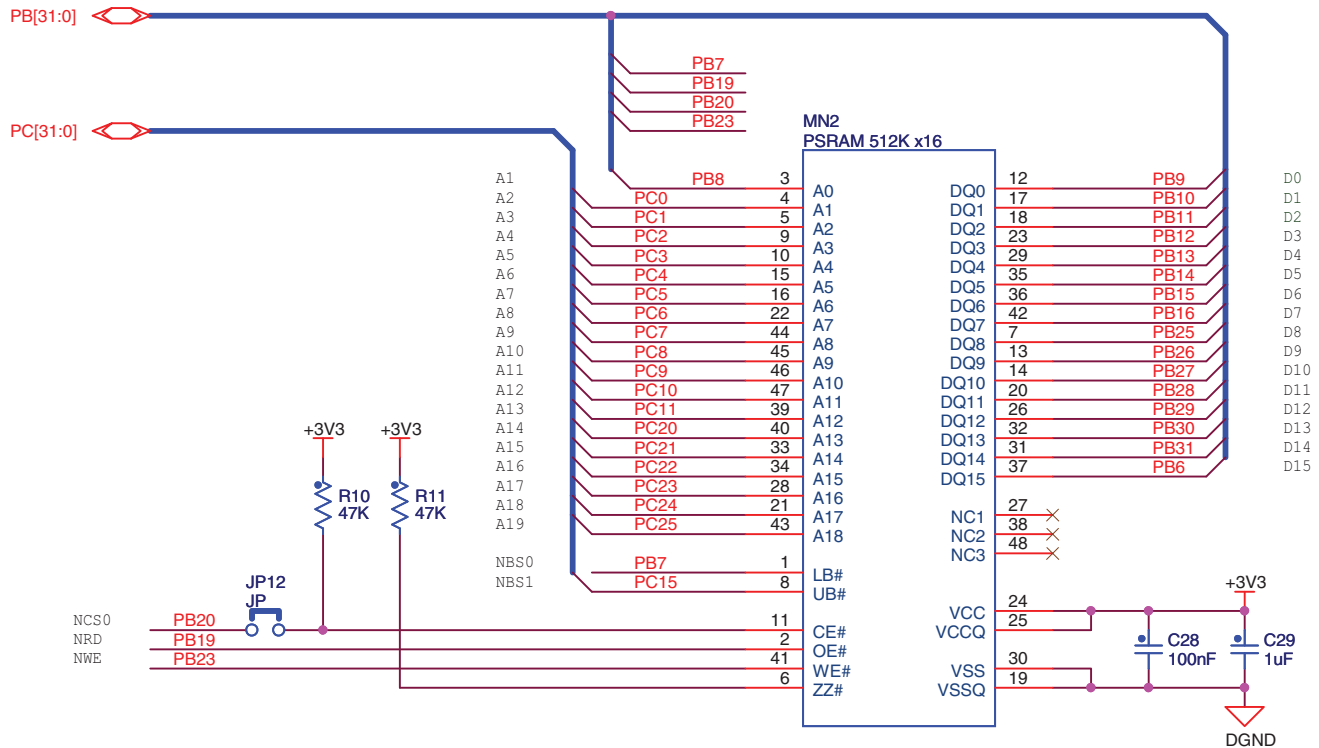
The SAM3U4E chip embeds:

- 256 Kbytes of embedded Flash
- 48 Kbytes of embedded SRAM with dual bank
- 16 Kbytes of ROM with embedded bootloader routines (UART, USB) and IAP (In-Application Programming functions) routines.

The SAM3U4E features an External Bus Interface (EBI) that permits interfacing to a broad range of external memories and virtually to any parallel peripheral. The SAM3U-EK board is equipped with two kinds of memory devices connected to the SAM3U4E EBI:

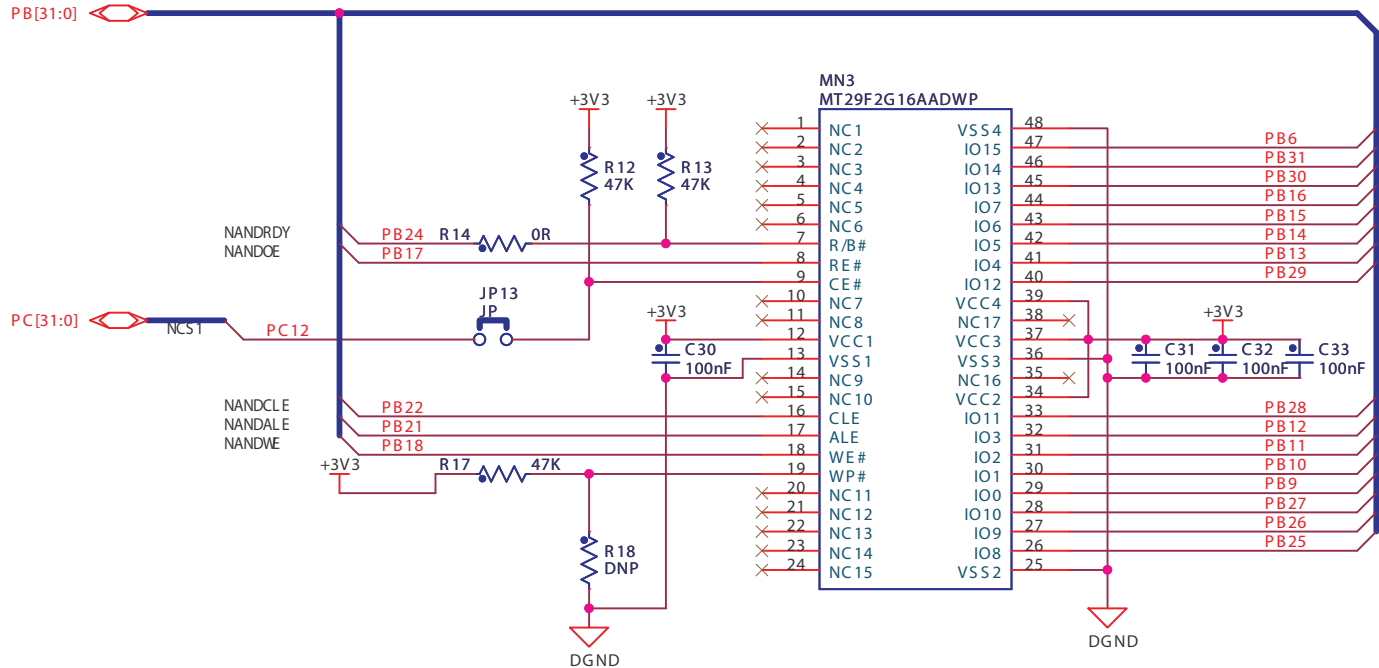
- One 512K x16 PSRAM device⁽¹⁾
- One NAND-Flash MT29F2G16ABD.

Figure 4-2. PSRAM



Note: 1. Brand and reference may vary. Check the bill of material (BOM) corresponding to your kit version to get precise information regarding that matter.

Figure 4-3. NAND-Flash



The chip select signals NCS0 and NCS1 are used for PSRAM and NAND-Flash chips selection, respectively. Furthermore, a dedicated jumper can disconnect these from the memories, to let NCS0 and NCS1 be used for other custom purpose.

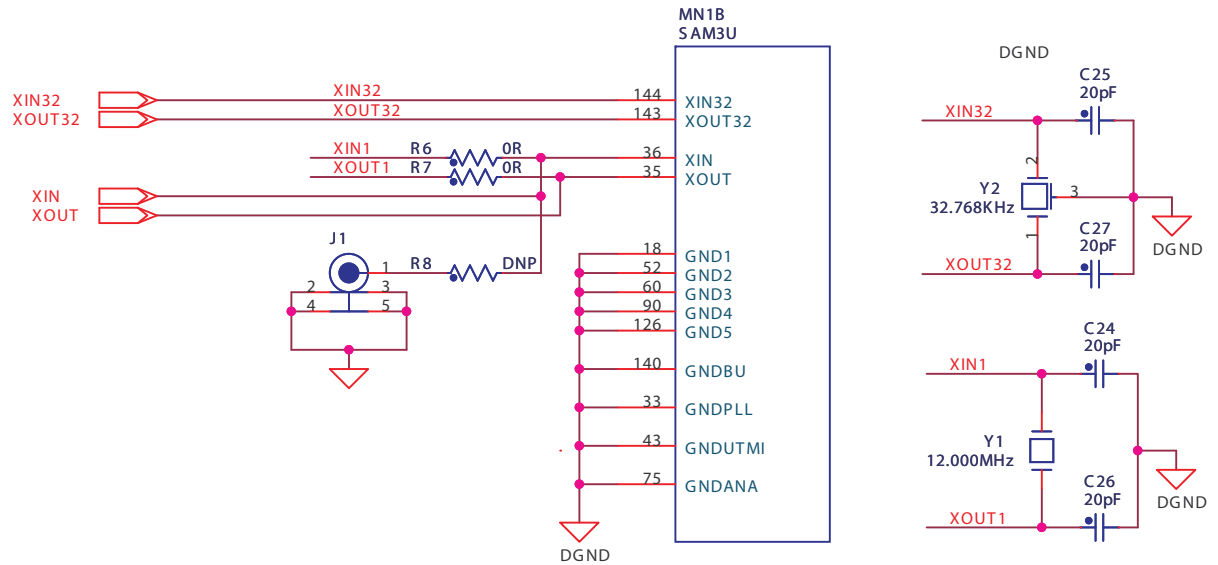
4.3.3 Clock Circuitry

The clock generator of a SAM3U4E microcontroller is made up of:

- A Low Power 32,768 Hz Slow Clock Oscillator with bypass mode
- A 3 to 20 MHz Crystal Oscillator, which can be bypassed (12 MHz needed in case of USB)
- A factory programmed fast internal RC Oscillator. 3 output frequencies can be selected: 4, 8 or 12 MHz (default value is 4 MHz).
- A 480 MHz UTMI PLL providing a clock for the USB High Speed Device Controller
- A 96 to 192 MHz programmable PLL (input from 8 to 16 MHz), capable of providing the clock MCK to the processor and to the peripherals.

The SAM3U-EK board is equipped with one 12 MHz crystal, one 32,768 Hz crystal and an external clock input connector (optional, not populated by default).

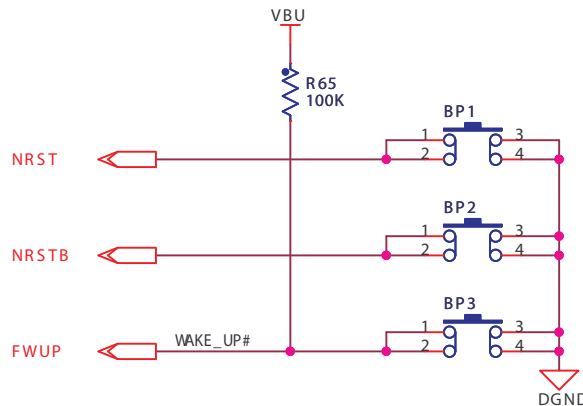
Figure 4-4. External Clock Source



4.3.4 Reset and Wake-Up Circuitry

The on-board NRST button BP1 and NRSTB button BP2 provide the SAM3U4E with external reset control. The on-board WAKE-UP button BP3 can be used to wake up the chip from low power modes.

Figure 4-5. System Buttons



The NRST pin is bidirectional. It is handled by the on-chip reset controller. It can be driven low to provide a reset signal out to the external components. Conversely, it can be asserted low from the outside to reset the microcontroller, its core and peripherals, Backup region (RTC, RTT and Supply Controller) excepted. The NRST pin integrates a permanent pull-up resistor of about 100 kOhm to VDDIO.

On the SAM3U-EK board, the NRST signal is connected to the LCD module and JTAG port.

The NRSTB pin is an input-only signal that enables the asynchronous reset of the SAM3U4E series when asserted low. The NRSTB pin integrates a permanent pull-up resistor of about 15 kOhm. This allows the connection of a simple push button for implementing a system-user reset. Whatever the mode, this pin will reset the chip including the Backup region (RTC, RTT and Supply Controller). It makes the chip behave as for a Power-on reset. An external capacitor (10 nF) is connected between NRSTB and VDDIO to enforce the signal stability on this pin.

The FWUP pin is Force Wake-Up active low input. It is enabled as a wake-up source with external pull-up. If the FWUP pin is asserted for a time longer than the debouncing period (configurable for 100 μ s, 1 ms, 16 ms, 128 ms or 1 second), a core power supply wake-up is initiated.

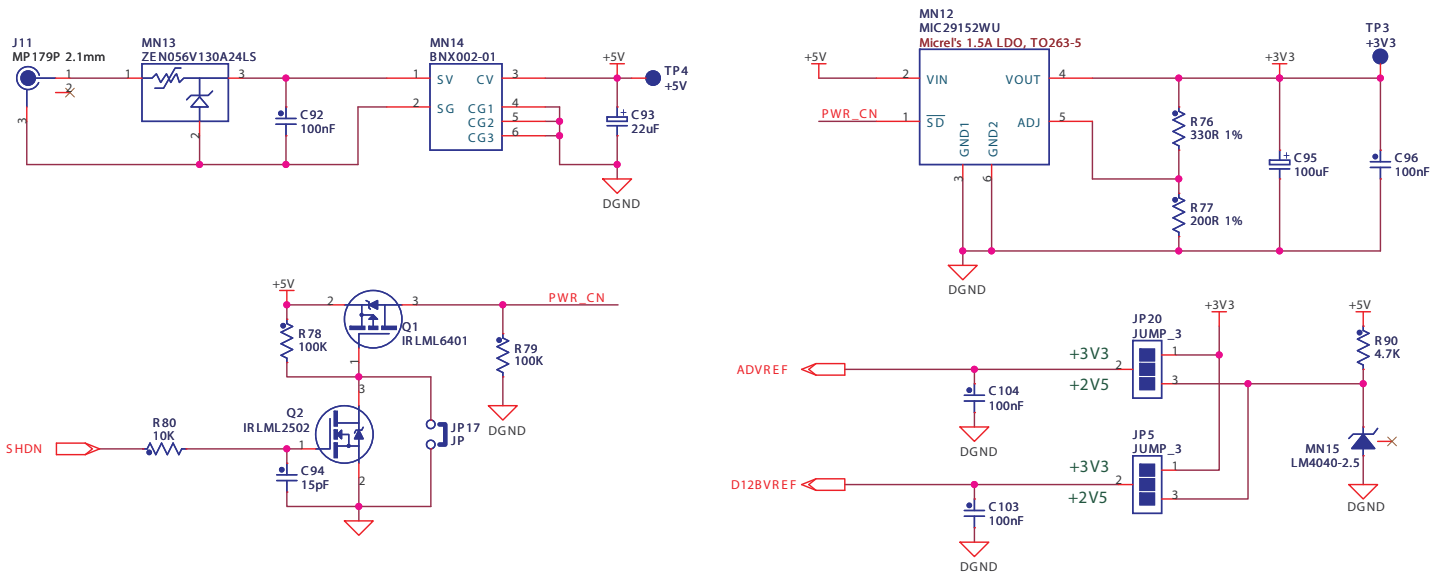
4.3.5 Power Supply and Management

The SAM3U-EK board is supplied with an external 5V DC block through input J11. Protection circuitry is obtained by a PolyZen diode MN13 and an LC combinatory filter MN14.

The adjustable LDO regulator MN12 is employed for the main supply of the 3.3V rail. It powers all the 3.3V board components. The shut down control of this LDO is made by MOSFETs Q1, Q2 piloted by the SAM3U4E SHDN pin. When SAM3U4E is in backup mode, SHDN pin outputs a low level signal, which shuts down the LDO. When the device is running (not in backup mode), SHDN pin output a high level signal, which enables the LDO.

By closing the “FORCE POWER ON” jumper JP17, the P-channel MOSFET Q1 will be forced on, no matter the level present on the SHDN pin, and the LDO 3.3V output will thereby be forced active.

Figure 4-6. Power Block



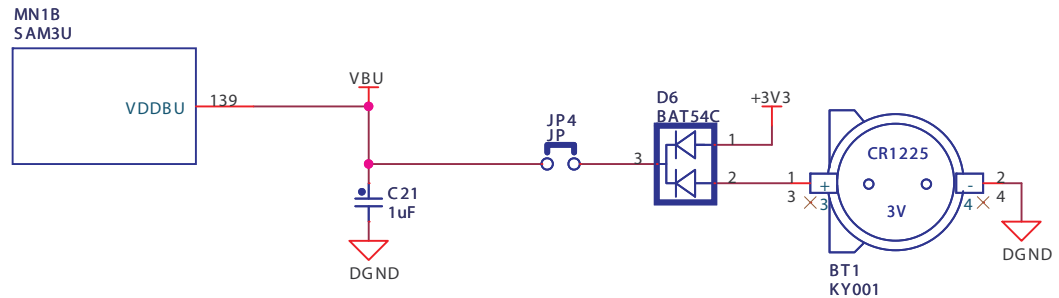
The SAM3U-EK board uses the 3.3V LDO output as its main supply source. VDDUTMI, VDDANA, VDDIO, VDDIN are powered directly from that source.

The internal 1.8V regulator output feeds VDDCORE and VDDPLL.

VDDCORE and VDDPLL can also be powered by an external supply. (Refer to the SAM3U datasheet for more details).

VDDBU pin is powered from the 3.3V rail and a backup battery BT1 via a dual Schottky diode D6.

Figure 4-7. Backup Battery

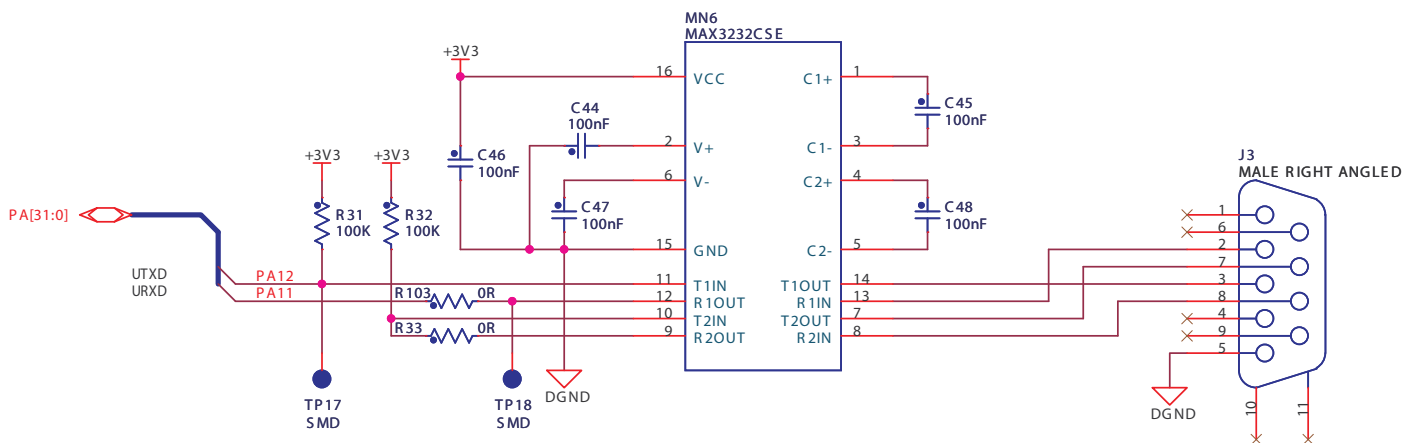


4.3.6 UART

The Universal Asynchronous Receiver Transmitter features a two-pin UART that can be used for communication and trace purposes. It offers an ideal channel for in-situ programming solutions. This UART is associated with two PDC channels to reduce the processor time on packet handling.

This two-pin UART (TXD and RXD only) is buffered through an RS232 Transceiver MN6 and brought to the DB9 male connector J3.

Figure 4-8. UART

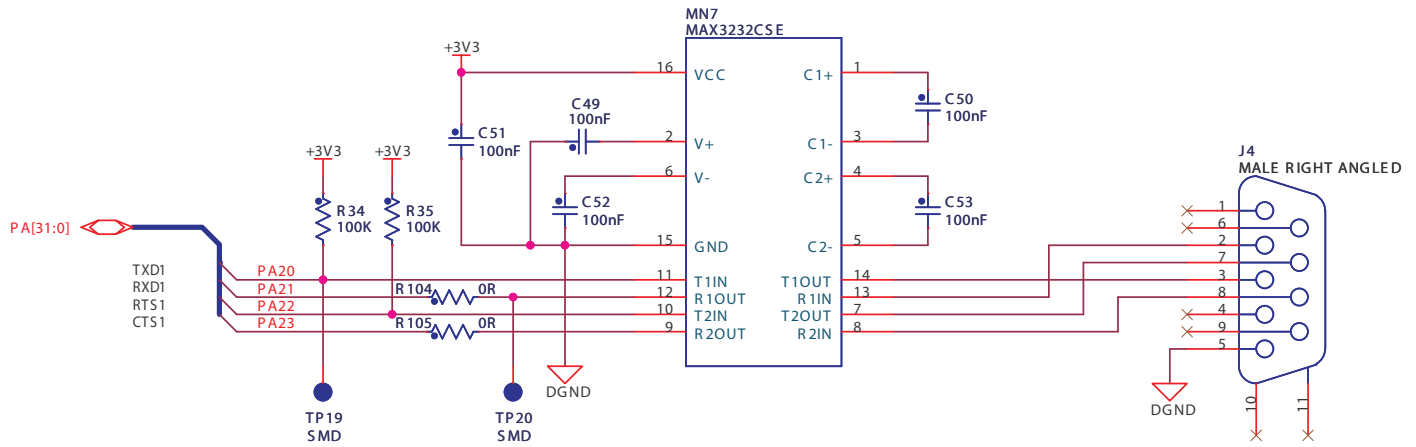


4.3.7 USART

The Universal Synchronous/Asynchronous Receiver Transmitter (USART) provides one full duplex universal synchronous/asynchronous serial link. The data frame format is extensively configurable (data length, parity, number of stop bits) to support a broad range of serial communication standards. The USART is also associated with PDC channels for TX/RX data access.

There are 3 USARTs on the SAM3U4E device, SAM3U-EK connects the USART1 bus (including TXD, RXD, RTS, CTS handshake signals control) to the DB9 male connector J4 through the RS232 Transceiver MN7.

Figure 4-9. USART

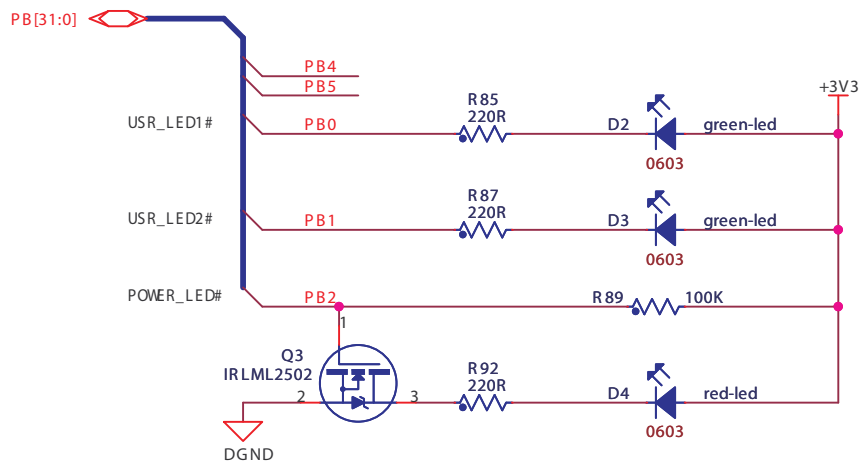


4.3.8 LEDs

There are three LEDs on the SAM3U-EK board:

- D2 and D3 green LEDs are user defined and controlled by the GPIO.
- D4 red LED is a power LED indicating that the 3.3V rail is enabled. It can also be controlled by the GPIO (by default, the GPIO is disabled and an on-board pull-up to 3.3V lights the LED).

Figure 4-10. LEDs



4.3.9 LCD, Backlight Control and Touch Panel

SAM3U-EK carries one TFT/Transmissive LCD module with touch screen, FTM280C12D, with integrated driver IC HX8347. The LCD display size is 2.8 inches, with a native resolution of 240 x 320 pixels.

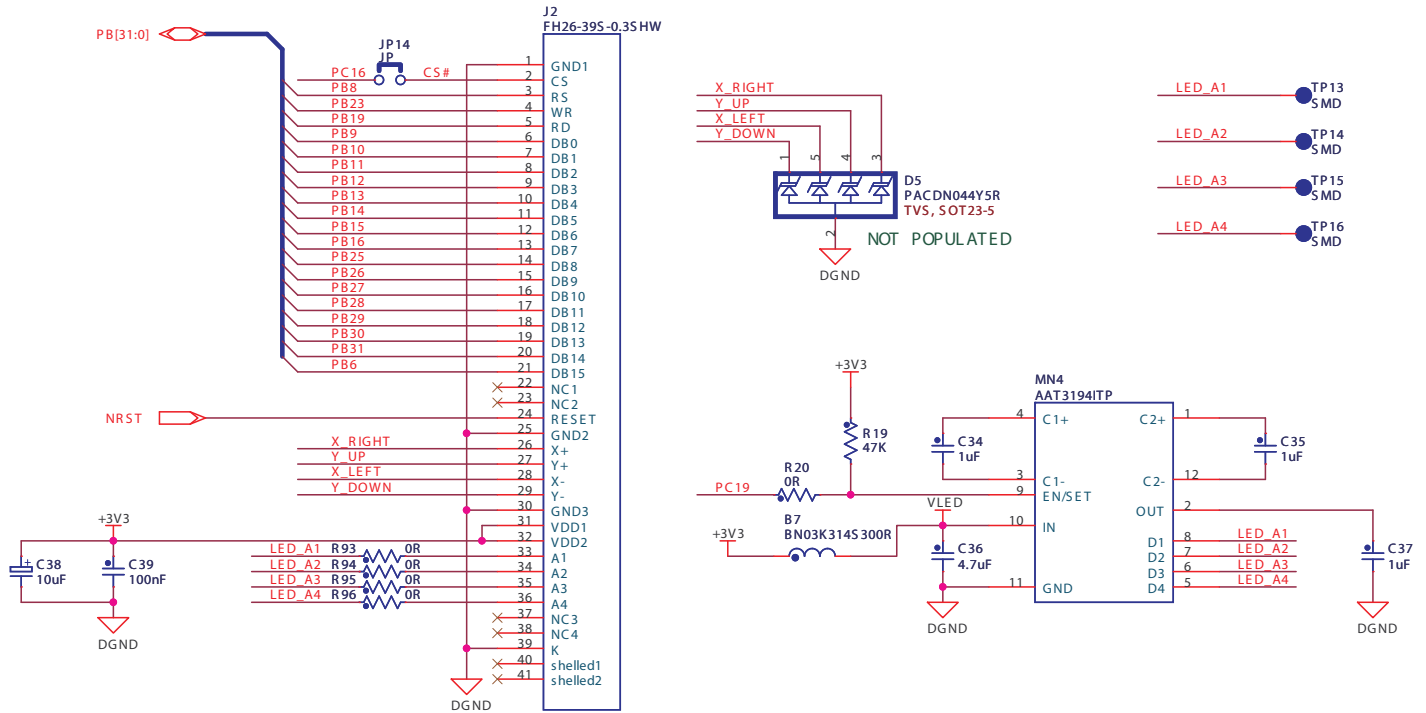
Table 4-1. LCD Module Pin Out

Pin	Symbol	Function
1	GND	Ground
2	CS	Chip Select
3	RS	Register select signal
4	WR	Write operation signal
5	RD	Read operation signal
6~21	DB0~DB15	Data bus
22~23	NC	No connection
24	RESET	Reset signal
25	GND	Ground
26	X+	Touch panel X_RIGHT
27	Y+	Touch panel Y_UP
28	X-	Touch panel X_LEFT
29	Y-	Touch panel Y_DOWN
30	GND	Ground
31	VDD1	Power supply for digital IO Pad
32	VDD2	Power supply for analog circuit
33~36	A1~A4	Power supply for backlight
37~38	NC	No connection
39	K	Backlight ground

The LCD module gets its reset from NRST. As explained previously, this NRST is shared with the JTAG port and the push button BP1. The LCD chip select signal is connected to NCS2 (a dedicated jumper can disable it, making NCS2 available for other custom usage).

The SAM3U4E communicates with the LCD through PIOB where a 16-bit parallel “8080-like” protocol data bus has to be implemented by software.

Figure 4-11. LCD Block

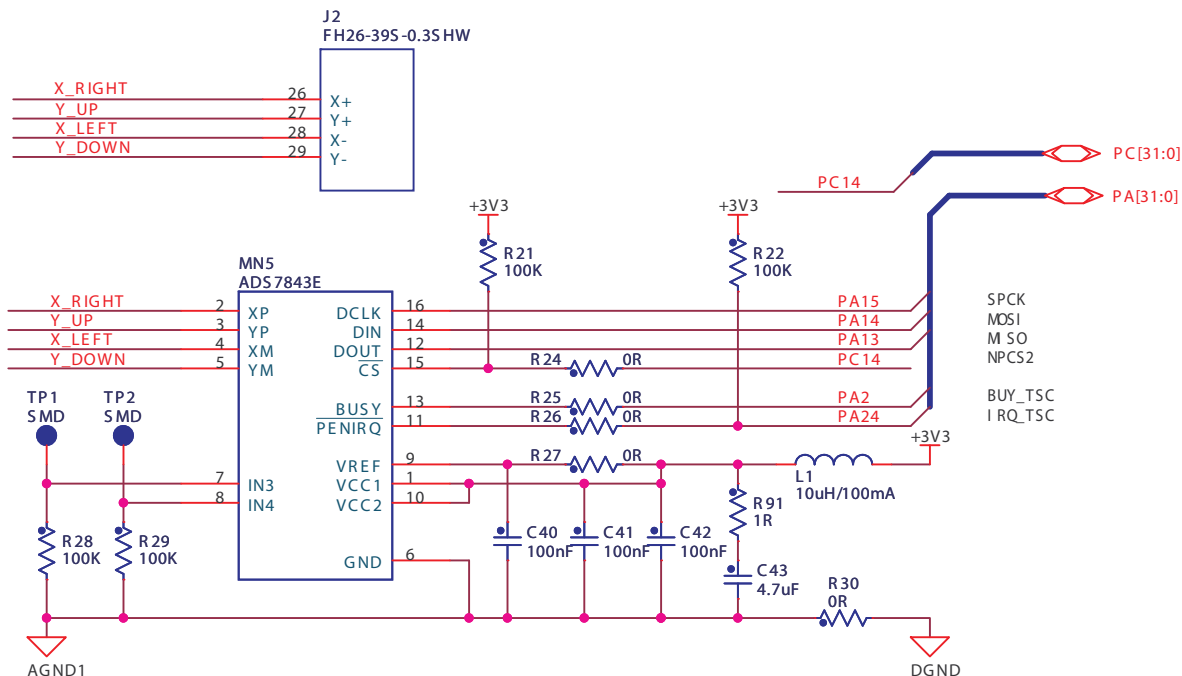


LCD backlight is made of 4 white chip LEDs in parallel, driven by an AAT3194 charge pump, MN4. The AAT3194 is controlled by the SAM3U4E through a single line Simple Serial Control (S2Cwire) interface, which permits to enable, disable, and set the LED drive current (LED brightness control) from a 32-level logarithmic scale. Four 0-Ohm resistors R93/R94/R95/R96 are implemented for optional current limitation (replace 0 Ohm with the required resistor value).

The LCD module integrates a 4-wire touch screen panel controlled by MN5, ADS7843, which is a slave device on the SAM3U4E SPI bus.

The ADS7843 touch ADC auxiliary inputs IN3/IN4 are connected to test points for optional function extension.

Figure 4-12. Touch Screen Controller

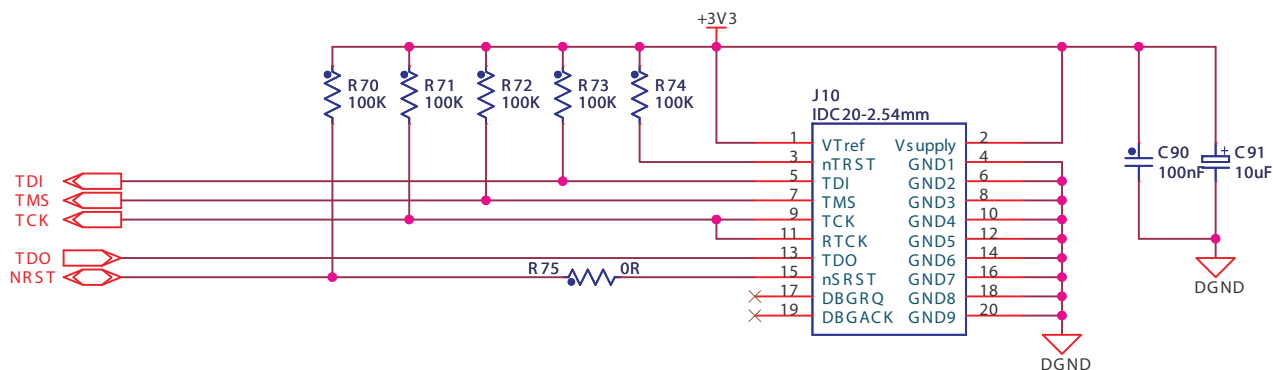


4.3.10 JTAG

A standard 20-pin JTAG connector is implemented on the SAM3U-EK for any ARM JTAG emulator connection, such as SAM-ICE.

Note that the NRST net is connected to the system button BP1, and is also used to reset the LCD module. 0-Ohm resistor R75 may be removed in order to isolate the JTAG port from the system reset signal.

Figure 4-13. JTAG Connector



4.3.11 Audio Codec

The SAM3U-EK includes a WOLFSON codec WM8731 for digital sound input and output. This interface includes audio jacks for:

- microphone input,
- line audio input, and
- headphone output.



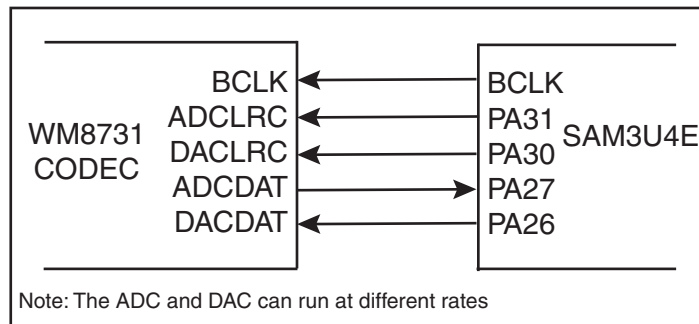
The SAM3U4E programmable clock output is used to generate the WM8731 master clock (MCLK). The SAM3U4E ODT (On-Die Termination) feature guarantees a signal integrity on this clock line without the need for external discrete components.

WM8731 pin 21 MODE is pulled down by default; this configures the device as a TWI device for internal register access.

Pin15 CSB is pulled up, which sets its TWI address as 33 [0x0011011].

The WM8731 digital interface works in slave mode on the SAM3U4E Synchronous Serial Controller (SSC) interface, which means that Codec digital audio bit clock and ADC/DAC left/right control clock are to be generated by the SAM3U4E.

Figure 4-14. Codec Slave Mode

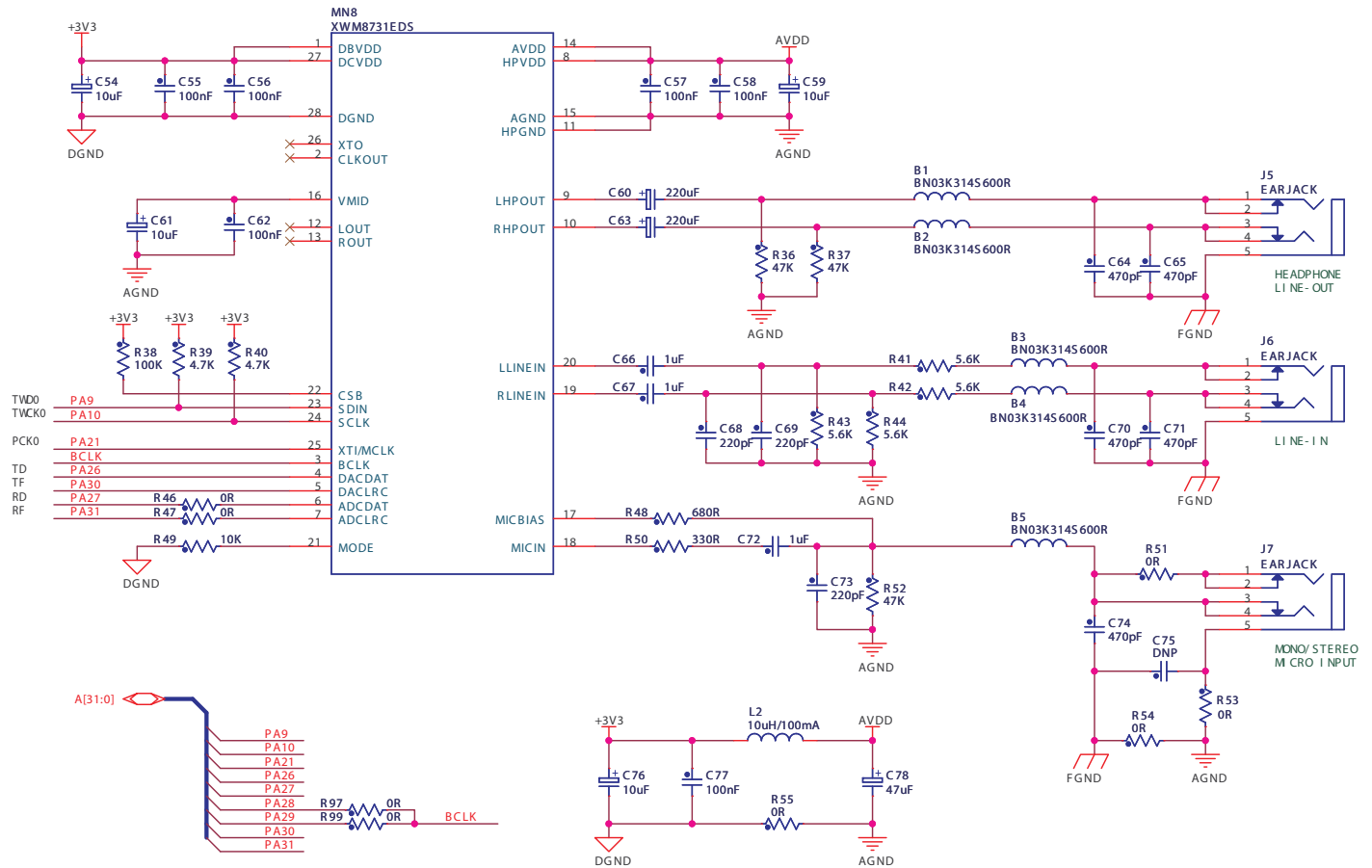


The WM8731 ADC and DAC have separated left/right control clocks to run at different rates.

The bit clock is shared; it can be the SSC transmitter clock (TK) or the receiver clock (RK). The default setting on SAM3U-EK is TK and RK shorted together through R97/R99. Please note that trying different ADC/DAC rates would mean different RK/TK rates; this default setting can be modified.

The 0-Ohm resistors R46/R47/R97/R99 have been implemented to offer a disconnection possibility (freeing these dedicated PIO lines for other custom usage).

Figure 4-15. Codec Block



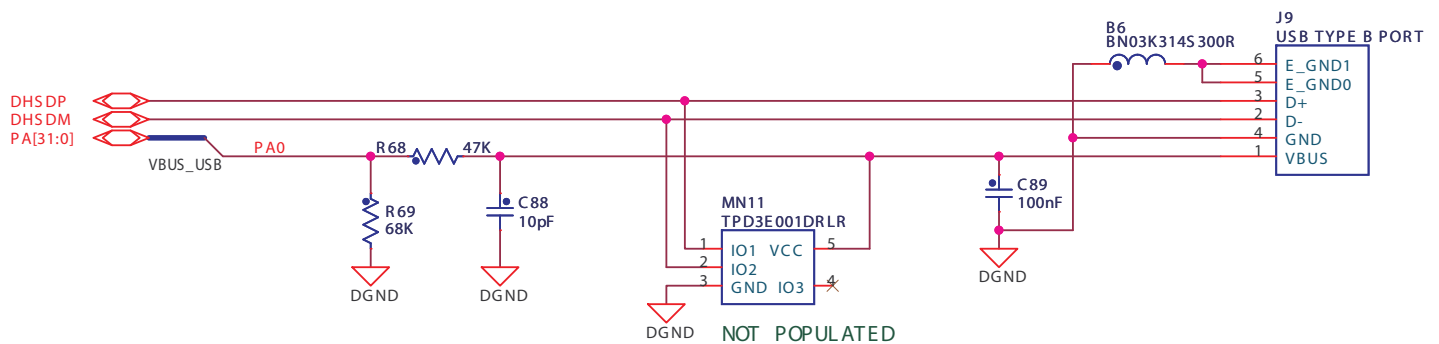
4.3.12 USB

The SAM3U4E UDPHS port is compliant with the Universal Serial Bus (USB) rev 2.0 High Speed device specification. J9 is a B-type receptacle for USB device.

Both R2 and R3 39-Ohm resistors build up a 90-Ohm differential impedance together with the 5-Ohm output impedance of the Hi-speed channel drivers.

R68 and R69 build up a divider bridge from VBUS +5V to implement plug-in detection (5V level gets lowered to a PIO compatible 3.3V level) through PA0. Note that PA0 is also shared with ZigBee signal IRQ0.

Figure 4-16. USB Slave Block



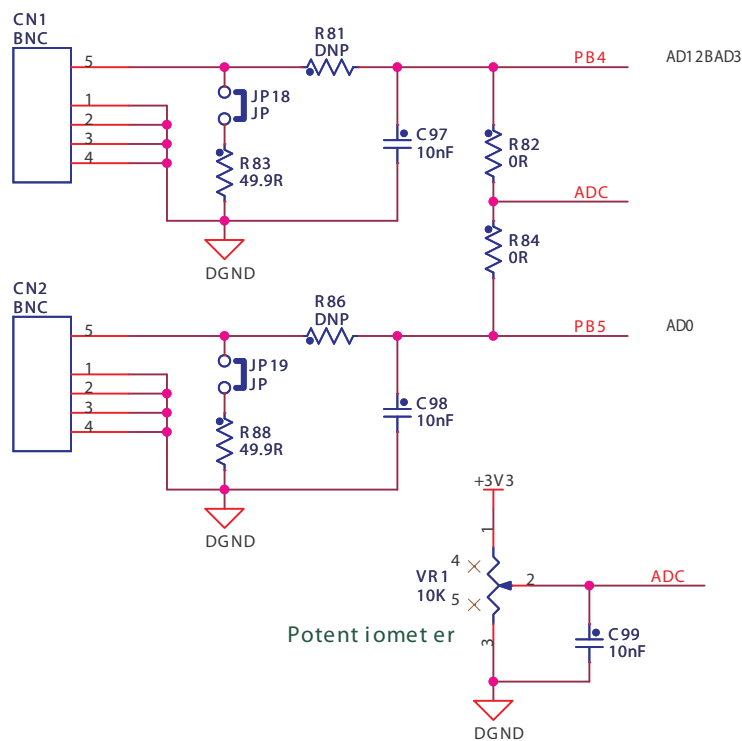
4.3.13 ADC Input

There are 8 multiplexed analog channel inputs on the 12-bit ADC, and 8 multiplexed analog channel inputs on the 10-bit ADC. SAM3U-EK optionally connects the two ADC channels to BNC header (check for your actual components implementation, schematics and BOM, on <http://www.atmel.com/products/>). One is 12-bit ADC channel 3, shared with PIO pin PB4. The other one is 10-bit ADC channel 0, shared with PIO PB5.

A potentiometer is also connected to these two channels to implement an easy access to ADC programming and debugging (or implement an analog user control such as display brightness, volume, etc.). Please note that SAM3U-EK default setting connects both AD12BAD3 and AD0 to the potentiometer so that AD12BAD3 and AD0 are actually shorted. If these two ports need to work separately, R82 and/or R84 should be removed.

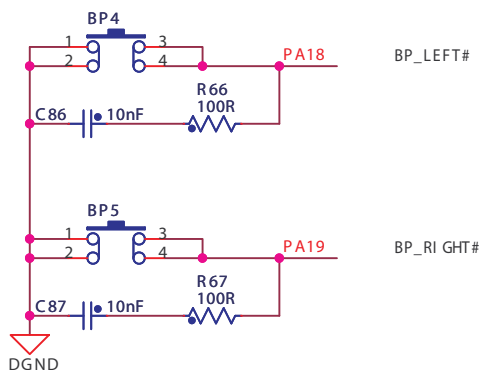
There is another ADC application capability on SAM3U-EK (See “G-Sensor” on page 4-15.)

Figure 4-17. ADC Input



4.3.14 User Buttons

2 user buttons on the SAM3U-EK are connected to PIO lines, and are defined as left and right buttons by default.

Figure 4-18. User Buttons

4.3.15 G-Sensor

The SAM3U-EK board is equipped with a three axis accelerometer MMA7341. Basically, it is an acceleration to analog voltage converter. Converted data on corresponding directions are read by 3 SAM3U4E 12-bit ADC channels.

Table 4-2. Direction

Direction	PIO usage	ADC channel
XOUT	PB3	AD2
YOUT	PC17	AD6
ZOUT	PC18	AD7

PC13 controls the device sleep mode. A low level on PC13 will place the MMA7341 into sleep mode to reduce the current; conversely, a high PC13 level will wake it up from sleep mode.

Jumper JP15 controls the device g-select function, which allows the selection between two sensitivity levels. Depending on the logic input placed on pin 10, the device internal gain will be changed, operating within a 3g or 11g range with different sensitivities.

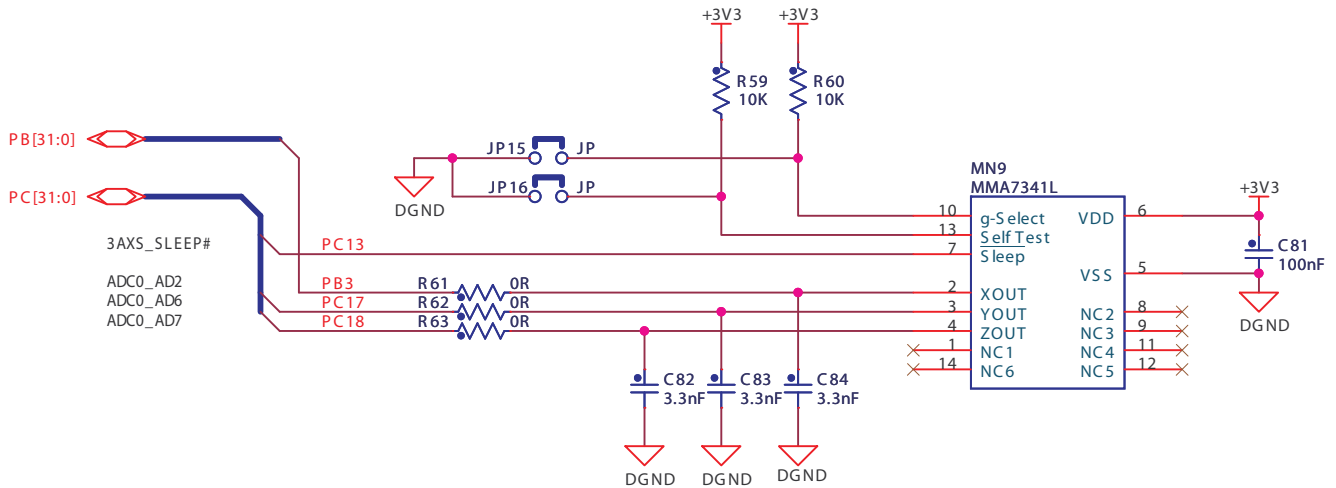
Table 4-3. g-Select

g-select	g-range	Sensitivity
0	3g	440mV/g
1	11g	117.5mV/g

Jumper JP16 provides control of the device self-test function. When the self-test function is initiated, an electrostatic force is applied to each axis to cause it to deflect. The x- and y-axis are deflected slightly while the z-axis is trimmed to deflect 1g. This procedure assures that both mechanical (g-cell) and electronic sections of the accelerometer are functioning.

Note that the 0-Ohm resistors R61/R62/R63 have been implemented to offer a disconnection possibility (freeing these dedicated PIO lines for other custom usage).

Figure 4-19. G-Sensor

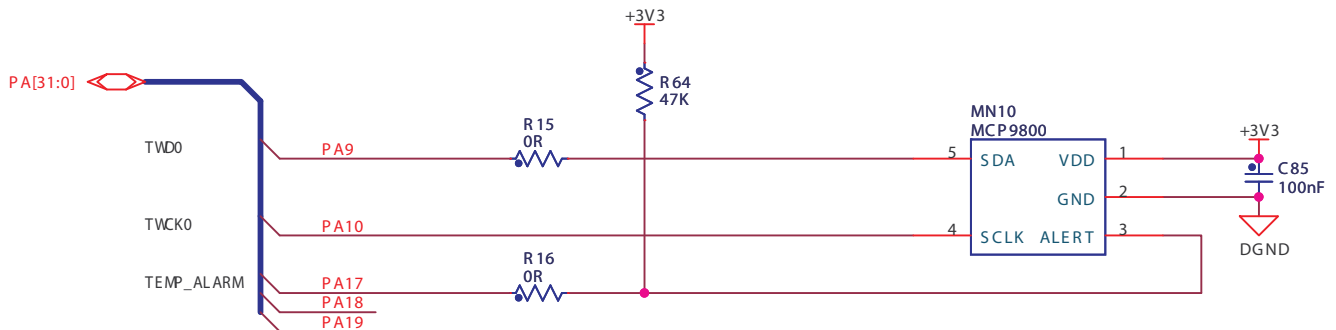


4.3.16 Temperature Sensor

A temperature sensor MCP9800 is connected to the SAM3U4E TWI bus. This device also features an open-drain output ALERT pin. The device outputs an alert signal when the ambient temperature goes beyond the user-programmed temperature limit.

Note that the 0-Ohm resistors R15 and R16 have been implemented to offer a disconnection possibility (freeing these dedicated PIO lines for other custom usage).

Figure 4-20. Temperature Sensor



4.3.17 SD Card

The SAM3U-EK has an MMC/MMCPlus high-speed 8-bit multimedia interface. This interface is used as a 4/8-bit interface, connected to an 8-bit SD/MMC card slot with card detection.

Figure 4-21. SD Card Socket

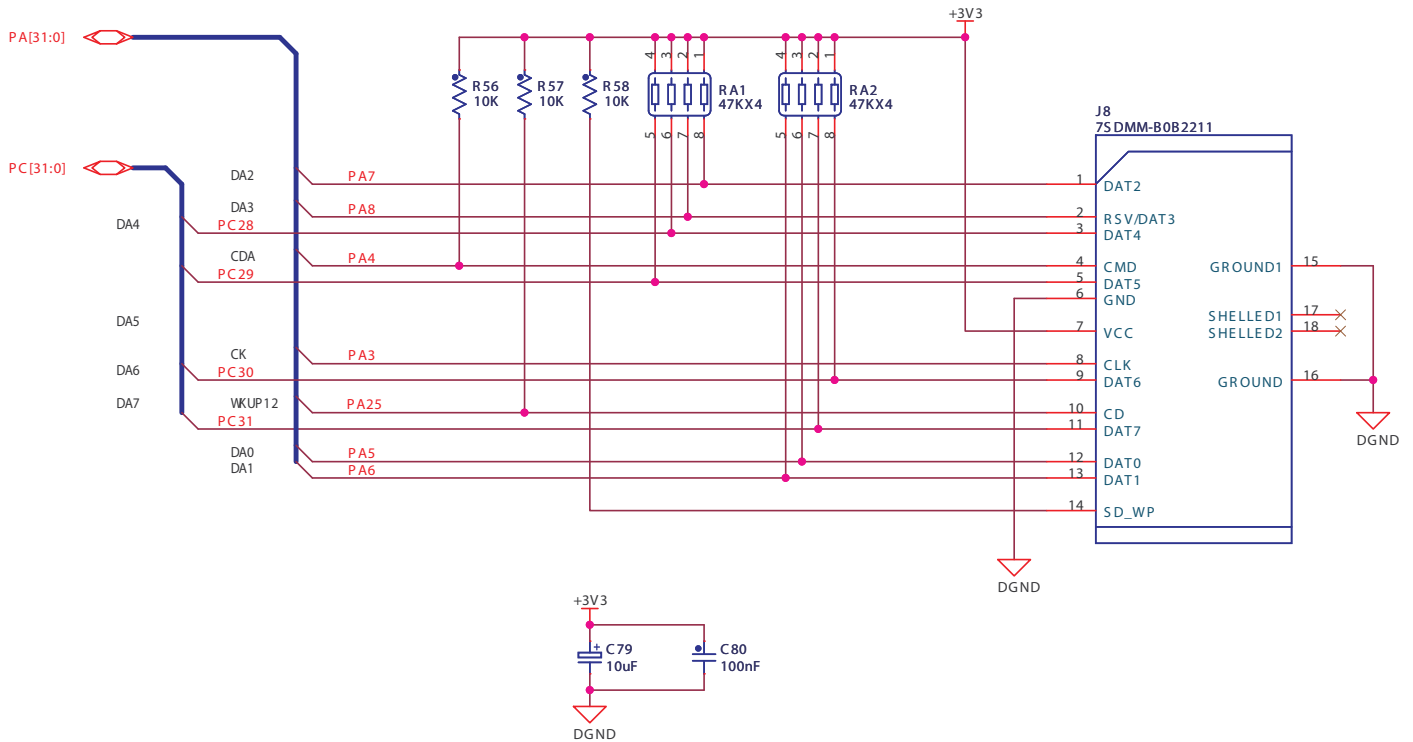


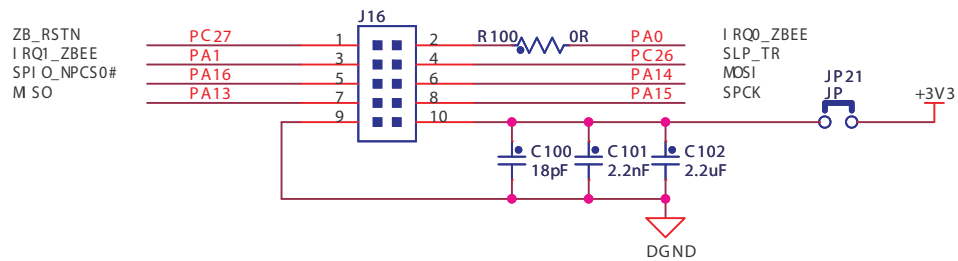
Table 4-4. Pin Card Detection Scheme

Status	Detection
WITHOUT CARD	SD_WP: OPEN CD: OPEN
SD Card inserted with write protection lock	SD_WP: OPEN CD: GND
SD Card inserted with write protection unlock, or other card inserted	SD_WP: GND CD: GND

4.3.18 ZigBee

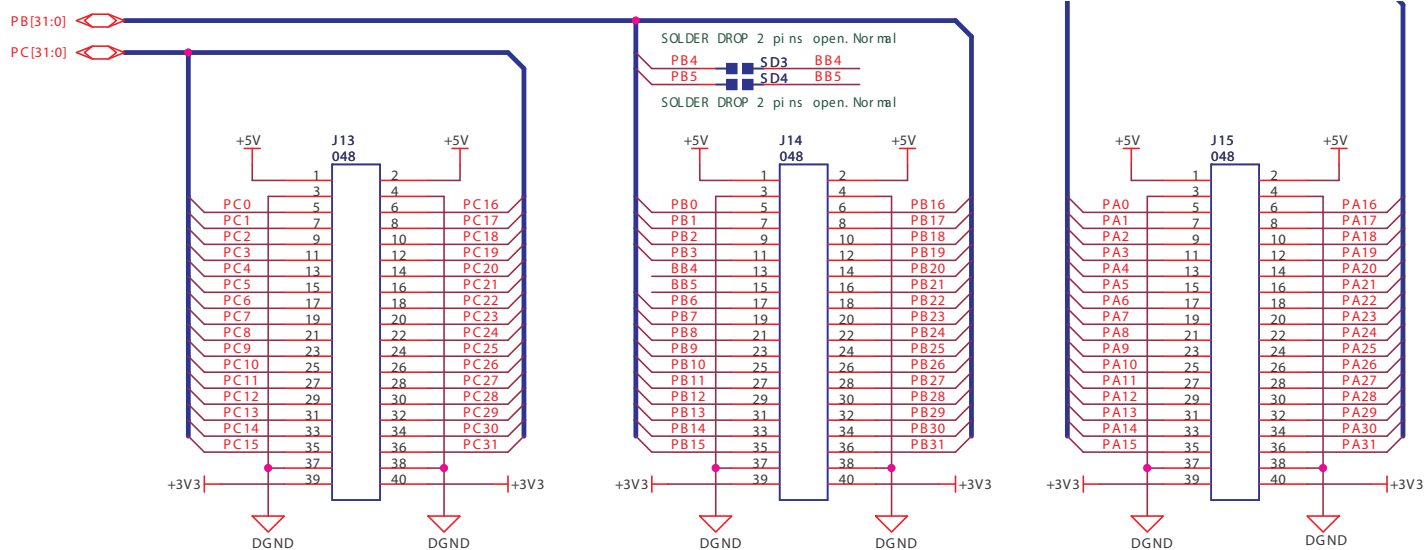
SAM3U4E has a 10-pin male connector for the RZ600 ZigBee module.

Figure 4-22. ZigBee



4.3.19 PIO Expansion

Figure 4-23. PIO Expansion Ports



The SAM3U4E product features 3 PIO controllers, PIOA, PIOB and PIOC, which multiplex the I/O lines of the peripheral set. Each PIO controller controls up to 32 lines. Expansion ports J13, J14, J15 provide a way for customers to define any PIO channels.

All the expansion port pins are directly connected to the SAM3U4E chip, except PB4 and PB5, which are assigned as AD12BAD3 and AD0 by default on the board. Solder drops have been implemented on the board to avoid signal conflicts from traces routing to expansion ports. If PB4 and PB5 need to be connected to the J14 connector, solder drops SD3 and SD4 should be shorted.

Figure 4-24. SD3 Location

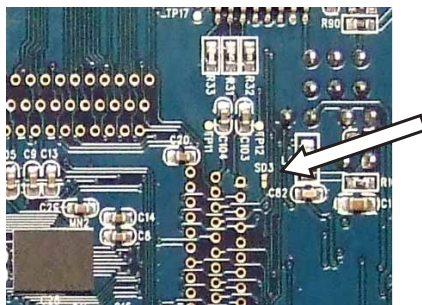
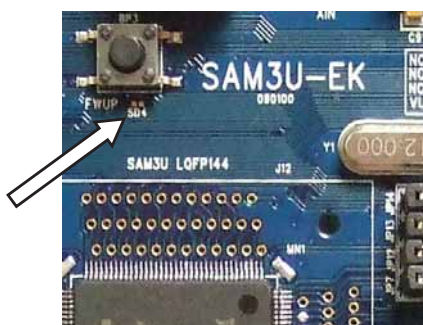


Figure 4-25. SD4 Location



4.4 Configuration

This section describes the PIO usage, the jumpers, the test points and the solder drops of a SAM3U-EK board.

4.4.1 PIO Usage

Table 4-5. PIO Port A Assignment

I/O Line	Peripheral A	Peripheral B	Extra Function	EK Usage	Device
PA0	TIOB0	NPCS1	WKUP0	IRQ0_ZBEE/	
VBUS_USB	ZigBee,				
USB					
PA1	TIOA0	NPCS2	WKUP1	IRQ0_ZBEE	ZigBee
PA2	TCLK0	AD12BTRG	WKUP2	BUSY_TSC	Touch Screen
PA3	MCKK	PCK1		MCKK	SD/MMC
PA4	MCCDA	PWMH0		MCCDA	SD/MMC
PA5	MCDA0	PWMH1		MCDA0	SD/MMC
PA6	MCDA1	PWMH2		MCDA1	SD/MMC
PA7	MCDA2	PWML0		MCDA2	SD/MMC
PA8	MCDA3	PWML1		MCDA3	SD/MMC
PA9	TWD0	PWML2	WKUP3	TWD0	Codec, Temp sensor
PA10	TWCK0	PWML3	WKUP4	TWCK0	Codec, Temp sensor
PA11	URXD	PWMF10		URXD	UART
PA12	UTXD	PWMF11		URXD	UART
PA13	MISO			MISO	Touch panel, ZigBee
PA14	MOSI			MOSI	Touch panel, ZigBee
PA15	SPCK	PWMH2		SPCK	Touch panel, ZigBee
PA16	NPCS0	NCS1	WKUP5	SPIO_NPCS0#	ZigBee
PA17	SCK0	ADTRG	WKUP6	TEMP_ALARM	Temp sensor
PA18	TXD0	PWMF12	WKUP7	BP_LEFT#	User Button
PA19	RXD0	NPCS3	WKUP8	BP_RIGHT#	User Button
PA20	TXD1	PWMH3	WKUP9	TXD1	USART
PA21	RXD1	PCK0	WKUP10	RXD1	USART
PA22	TXD2	RTS1	AD12B0	RTS1	USART
PA23	RXD2	CTS1		CTS1	USART
PA24	TWD1	SCK1	WKUP11	IRQ_TSC	Touch Screen
PA25	TWCK1	SCK2	WKUP12	MCI_CD	SD/MMC
PA26	TD	TCLK2		TD	Audio codec
PA27	RD	PCK0		RD	Audio codec
PA28	TK	PWMH0		TK	Audio codec



Table 4-5. PIO Port A Assignment

I/O Line	Peripheral A	Peripheral B	Extra Function	EK Usage	Device
PA29	RK	PWMH1		RK	Audio codec
PA30	TF	TIOA2	AD12B1	TF	Audio codec
PA31	RF	TIOB2		RF	Audio codec

Table 4-6. PIO Port B Assignment

I/O Line	Peripheral A	Peripheral B	Extra Function	EK Usage	Device
PB0	PWMH0	A2	WKUP13	USR_LED1#	USER_LED
PB1	PWMH1	A3	WKUP14	USR_LED2#	USER_LED
PB2	PWMH2	A4	WKUP15	POWER_LED	POWER_LED
PB3	PWMH3	A5	AD12BAD2	3AXS_XOUT	Accelerometer
PB4	TCLK1	A6	AD12BAD3	BNC1	Analog input
PB5	TIOA1	A7	AD0	BNC2	Analog input
PB6	TIOB1	D15	AD1	D15	PSRAM, NAND-Flash, LCD
PB7	RTS0	A0/NBS0	AD2	NBS0	PSRAM,
PB8	CTS0	A1	AD3	A1/RS	PSRAM, LCD
PB9	D0	DTR0		D0	PSRAM, NAND-Flash, LCD
PB10	D1	DSR0		D1	PSRAM, NAND-Flash, LCD
PB11	D2	DCD0		D2	PSRAM, NAND-Flash, LCD
PB12	D3	RI0		D3	PSRAM, NAND-Flash, LCD
PB13	D4	PWMH0		D4	PSRAM, NAND-Flash, LCD
PB14	D5	PWMH1		D5	PSRAM, NAND-Flash, LCD
PB15	D6	PWMH2		D6	PSRAM, NAND-Flash, LCD
PB16	D7	PWMH3		D7	PSRAM, NAND-Flash, LCD
PB17	NANDOE	PWML0		NANDOE	NAND-Flash
PB18	NANDWE	PWML1		NANDWE	NAND-Flash
PB19	NRD	PWML2		NRD	PSRAM, LCD
PB20	NCS0	PWML3		NCS0	PSRAM
PB21	A21/NANDALE	RTS2		NANDALE	NAND-Flash
PB22	A22/NANDCLE	CTS2		NANDCLE	NAND-Flash
PB23	NWR0/NEW	PCK2		NWE	PSRAM, LCD
PB24	NANDRDY	PCK1		NANDRDY	NAND-Flash
PB25	D8	PWML0		D8	PSRAM, NAND-Flash, LCD
PB26	D9	PWML1		D9	PSRAM, NAND-Flash, LCD
PB27	D10	PWML2		D10	PSRAM, NAND-Flash, LCD
PB28	D11	PWML3		D11	PSRAM, NAND-Flash, LCD

Table 4-6. PIO Port B Assignment

I/O Line	Peripheral A	Peripheral B	Extra Function	EK Usage	Device
PB29	D12			D12	PSRAM, NAND-Flash, LCD
PB30	D13			D13	PSRAM, NAND-Flash, LCD
PB31	D14			D14	PSRAM, NAND-Flash, LCD

Table 4-7. PIO Port C Assignment

I/O Line	Peripheral A	Peripheral B	Extra Function	EK Usage	Device
PC0	A2			A2	PSRAM
PC1	A3			A3	PSRAM
PC2	A4			A4	PSRAM
PC3	A5	NPCS1		A5	PSRAM
PC4	A6	NPCS2		A6	PSRAM
PC5	A7	NPCS3		A7	PSRAM
PC6	A8	PWML0		A8	PSRAM
PC7	A8	PWML1		A8	PSRAM
PC8	A10	PWML2		A10	PSRAM
PC9	A11	PWML3		A11	PSRAM
PC10	A12	CTS3		A12	PSRAM
PC11	A13	RTS3		A13	PSRAM
PC12	NCS1	TXD3		NCS1	NAND-Flash
PC13	A2	RSD3		3AXS_SLEEP#	Accelerometer
PC14	A3	NPCS2		NPCS2	Touch Screen
PC15	NWR1/NBS1		AD12BAD4	NBS1	NAND-Flash
PC16	NCS2	PWML3	AD12BAD5	NCS2	LCD
PC17	NCS3		AD12BAD6	3AXS_YOUT	Accelerometer
PC18	NWAIT		AD12BAD7	3AXS_ZOUT	Accelerometer
PC19	SCK3	NPCS1		BL_EN	Back Light
PC20	A14			A14	PSRAM
PC21	A15			A15	PSRAM
PC22	A16			A16	PSRAM
PC23	A17			A17	PSRAM
PC24	A18			A18	PSRAM
PC25	A19	PWMH1		A19	PSRAM
PC26	A20	PWMH2		SLP_TR	ZigBee
PC27	A23	PWMH3		ZB_RSTN	ZigBee
PC28		MCDA4	AD4	MCDA4	SD/MMC

Table 4-7. PIO Port C Assignment

I/O Line	Peripheral A	Peripheral B	Extra Function	EK Usage	Device
PC29	PWML0	MCDA5	AD5	MCDA5	SD/MMC
PC30	PWML1	MCDA6	AD6	MCDA6	SD/MMC
PC31	PWML2	MCDA7	AD7	MCDA7	SD/MMC

4.4.2 Jumpers

The SAM3U-EK board jumpers are used for many purposes such as internal Flash Memory reinitialization, power current measurement and other configurations.

Table 4-8. Jumpers Setting

Designation	Label	Default Setting	Feature
JP1	ERASE	Open	Close it to reinitialize the Flash content and some of its NVM bits. This jumper must be closed for more than 220 ms at power-up to perform the re-initialization.
JP2 (DNP)	TEST	Not populated (open)	reserved
JP3	VIN	Close	Measure current feed into VDDIN pin
JP5	AD12BVREF	Pin1 Pin2 close, Switch to +3V3	Select the reference voltage of the 12-bit ADC to be either 3.3V (close 1-2) or 2.5V (close 2-3)
JP6	VIO	Close	Measure current feed into VDDIO pins
JP7	VUTMI	Close	Measure current feed into VDDUTMI pin
JP8	VANA	Close	Measure current feed into VDDANA pin
JP9	VCORE	Close	Measure current feed into VDDCORE pins
JP10	VPLL	Close	Measure current feed into VDDPLL pin
JP11	VOUT	Close	Measure current out of VDDOUT pin
JP12	NCS0	Close	Disconnection possibility on NCS0
JP13	NCS1	Close	Disconnection possibility on NCS1
JP14	NCS2	Close	Disconnection possibility on NCS2
JP15	3AXS	Close	G-select feature, sensitivity level switch. Close as 440mv/g, open as 117.5mV/g
JP16	3AXS	Close	Open to cause a slight deflect on each axis output, which is device self test
JP17	FORCE POWER ON	Close	Force +3V3 LDO output valid
JP18 (DNP)	-	Not populated (open)	Close to enable 50-Ohm terminal resistor for AD12BAD3 BNC port
JP19 (DNP)	-	Not populated (open)	Close to enable 50-Ohm terminal resistor for AD0 BNC port
JP20	ADVREF	Pin1 Pin2 close, Switch to +3V3	Select the reference voltage of the 10-bit ADC to be either 3.3V (close 1-2) or 2.5V (close 2-3)
JP21	-	Open	Measure current feed into ZigBee module

4.4.3 Test Points

Some test points have been placed on the SAM3U-EK board for the verification of important signals.

Table 4-9. Test Points

Designation	Part	Description
TP1	Pad	Aux ADC input IN3 for touch screen control
TP2	Pad	Aux ADC input IN4 for touch screen control
TP3	Ring Hook	+3V3
TP4	Ring Hook	+5V
TP5	Ring Hook	GND
TP6	Ring Hook	GND
TP7	Ring Hook	GND
TP8	Ring Hook	GND
TP9	Pad	FWUP
TP10	Pad	SHDN
TP11	Pad	ADVREF
TP12	Pad	AD12BVREF
TP13	Pad	LED_A1
TP14	Pad	LED_A2
TP15	Pad	LED_A3
TP16	Pad	LED_A4
TP17	Pad	UTXD
TP18	Pad	URXD
TP19	Pad	TXD1
TP20	Pad	RXD1

4.4.4 Solder Drops

Two solder drops have been designed on the SAM3U-EK for isolation purposes.

Table 4-10. Solder Drops

Designation	Default Setting	Feature
SD3	Open	Isolation of AD12BAD3 input from PIO expansion socket
SD4	Open	Isolation of AD0 input from PIO expansion socket

4.4.5 Assigned PIO Lines, Disconnection Possibility

As pointed out in previous interface descriptions, 0-Ohm resistors have been inserted on the PIO lines receiver path of the SAM3U-EK. Some PIO lines are connected to an external driver on the board. The 0-Ohm resistors allow disconnecting each of these for custom usage (through PIO expansion connec-

tors, for example). This feature gives the user an added level of versatility for prototyping a system of his own. See the table below.

Table 4-11. Disconnecting Possibility

Designation	Default Assignment	PIO
R14	NANDRDY	PB24
R15	NANDOE	PB17
R16	NANDWE	PB18
R20	BL_EN	PC19
R24	NPCS2	PC14
R25	BUY_TSC	PA2
R26	IRQ_TSC	PA24
R46	RD	PA27
R47	RF	PA31
R61	AD12BAD2	PB3
R62	AD12BAD6	PC17
R63	AD12BAD7	PC18
R97	TK	PA28
R99	RK	PA29
R100	IRQ0_ZBEE	PA0
R103	URXD	PA11
R104	RXD1	PA21
R105	CTS1	PA23



Section 5

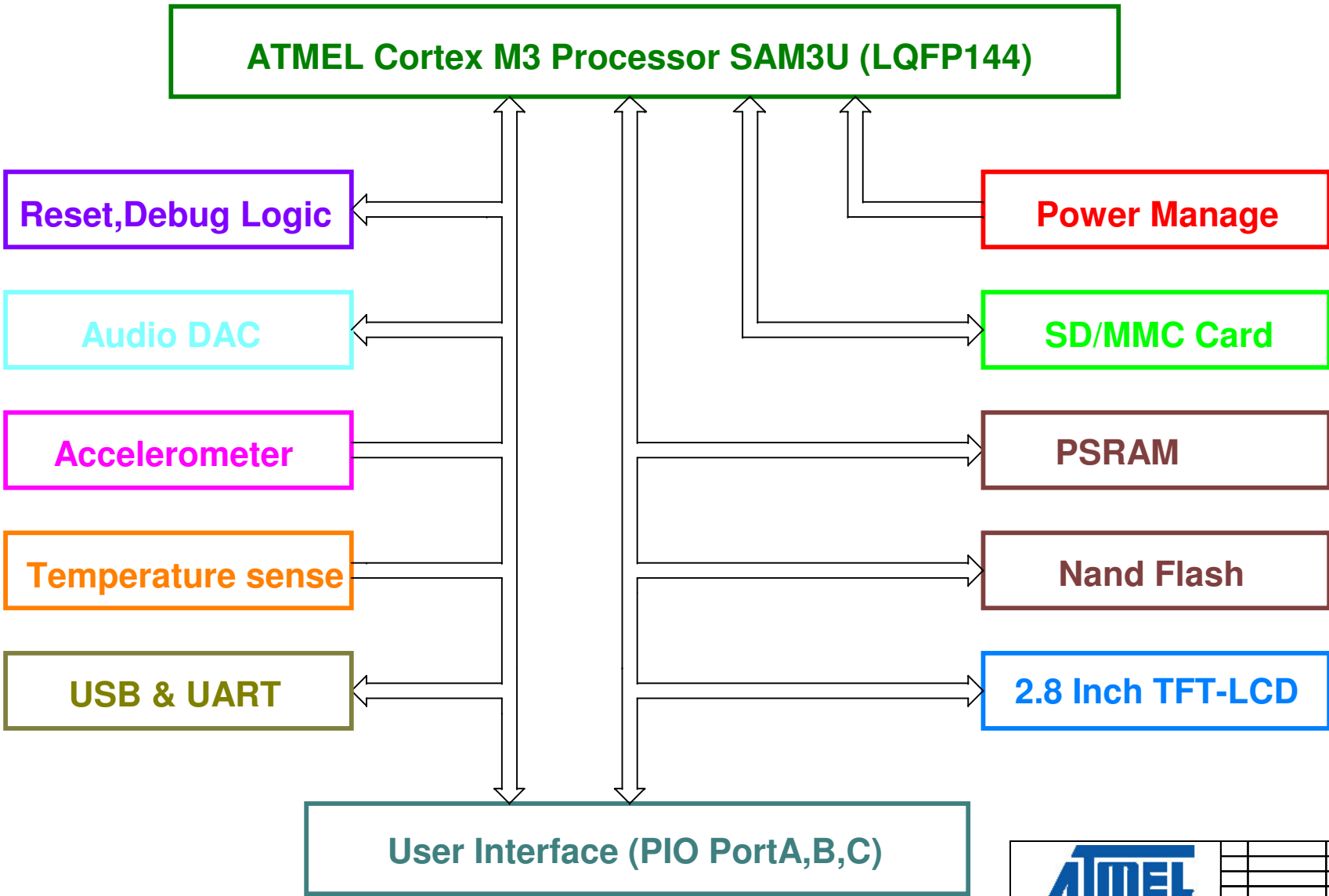
Schematics


5.1 Schematics

This section contains the following schematics:

- Block Diagram
- Design Notes
- SAM3U PIO
- SAM3U CPU
- EBI Memory 1MB PSRAM
- EBI Memory II 2GB NAND-Flash
- TFT LCD and TSC
- UART and COM1 RS232
- Audio DAC
- SD/MMC Interface
- Accelerometer, Temp, Buttons
- USB and JTAG
- Power Supply, ADC and LED
- SAM3U Socket
- User Interface and ZigBee

SAM3U-EK RevB Block Diagram



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SAM3U-EK RevB Block Diagram		SCALE	1/1			REV.	SHEET
						B	1/15

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1. SAM3U-EK Revision HISTORY

Rev: A

SCH: SAM3U-EK RevA Data: 2008/12

Note: Original Released

Rev: B


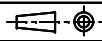
SCH: SAM3U-EK RevB Data: 2009/04

Note: Final Released

2. Explain of Schematics

(1) Resistance Unit: "K" is
"K|,"

(2) "DNP" means the component is not populated by default

					
SAM3U-EK RevB		SCALE	1/1	REV.	B
Design notes				SHEET	2/15
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PB[31:0] {5,6,7,11,13,14,15}

MN1A
SAM3U

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PA1	111
PA2	113
PA3	115
PA4	117
PA5	119
PA6	121
PA7	123
PA8	128
PA9	130
PA10	132
PA11	133
PA12	134
PA13	87
PA14	88
PA15	91
PA16	93
PA17	95
PA18	99
PA19	100
PA20	101
PA21	102
PA22	77
PA23	103
PA24	105
PA25	106
PA26	107
PA27	64
PA28	45
PA29	46
PA30	78
PA31	48

PA0/WKUP0
PA1/WKUP1
PA2/WKUP2
PA3/CK
PA4/CDA
PA5/DA0
PA6/DA1
PA7/DA2
PA8/DA3
PA9/TWD0
PA10/TWCK0
PA11/URXD
PA12/UTXD
PA13/MISO
PA14/MOSI
PA15/SPCK
PA16/NPCS0
PA17/WKUP7
PA18/WKUP8
PA19/WKUP9
PA20/TXD1
PA21/RXD1
PA22/RTS1
PA23/CTS2
PA24/WKUP11
PA25/WKUP12
PA26/TD
PA27/PCK0
PA28/TK
PA29/PWMH1
PA30/TF
PA31/RF

PB0/PWMH0
PB1/PWMH1
PB2/PWMH2
PB3/AD12BAD2
PB4/AD12BAD3
PB5/AD1
PB6/D15
PB7/A0/NBS0
PB8/A1
PB9/D0
PB10/D1
PB11/D2
PB12/D3
PB13/D4
PB14/D5
PB15/D6
PB16/D7
PB17/NANDOE
PB18/NANDWE
PB19/NRD
PB20/NCS0
PB21/A21/NANDALE
PB22/A22/NANDCLE
PB23/NWR0/NWE
PB24/NANDRYD
PB25/D8
PB26/D9
PB27/D10
PB28/D11
PB29/D12
PB30/D13
PB31/D14

53	PB0
55	PB1
57	PB2
79	PB3
80	PB4
65	PB5
66	PB6
67	PB7
68	PB8
31	PB9
30	PB10
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8	PB29
6	PB30
5	PB31

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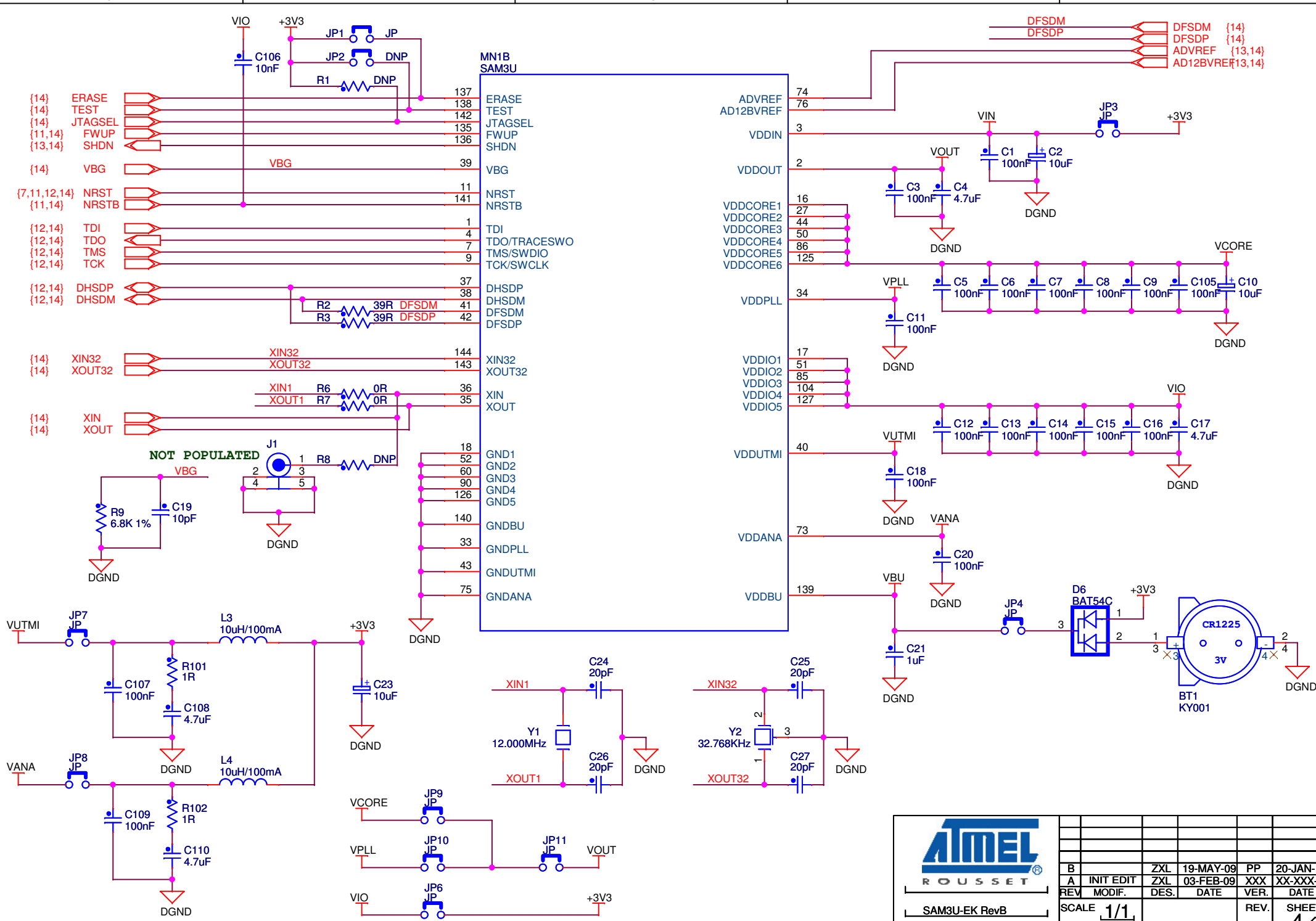
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PC15/NWR1/NBS1

PC16/NCS2
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PC27/A23
PC28/DA4
PC29/DA5
PC30/DA6
PC31/DA7

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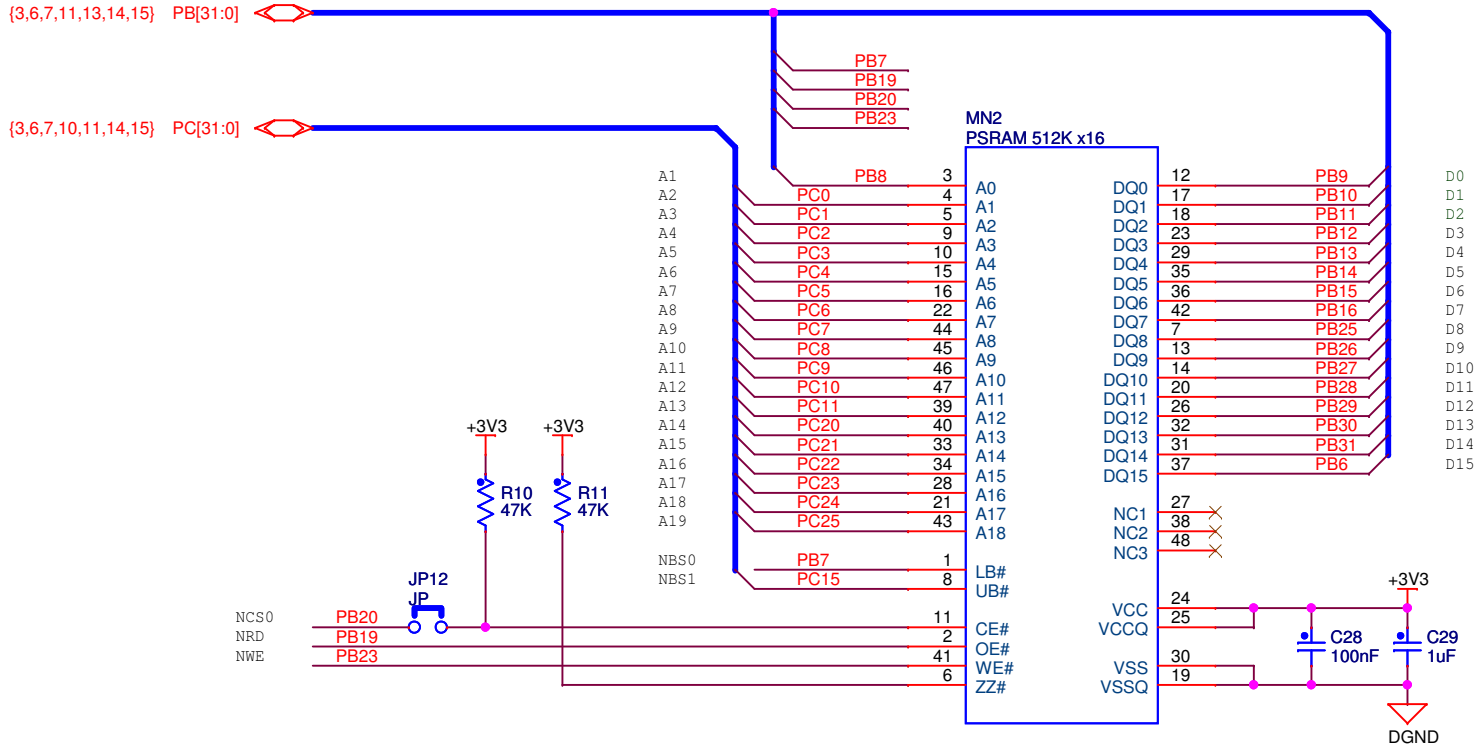
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SAM3U-EK RevB					
SAM3U PIO					

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SHEET 4/15				

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SCALE 1/1				REV. B	SHEET 5/15
SAM3U-EK RevB					
EBI Memory 1MB PSRAM					

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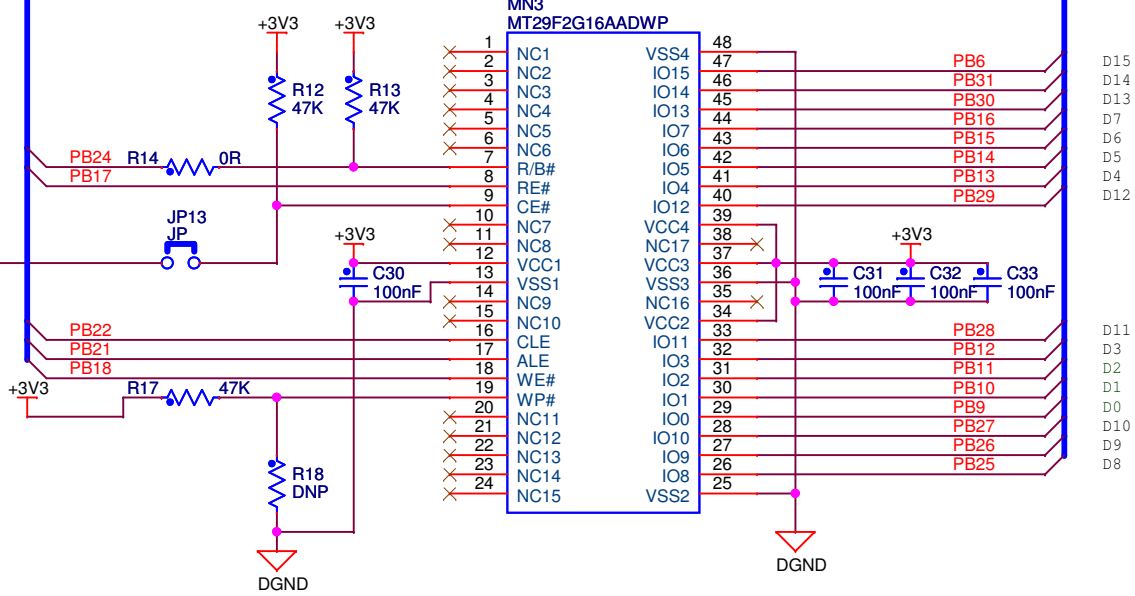
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NANDALE
NANDWE

NCS1 PC12

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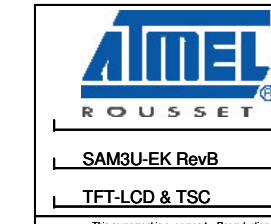
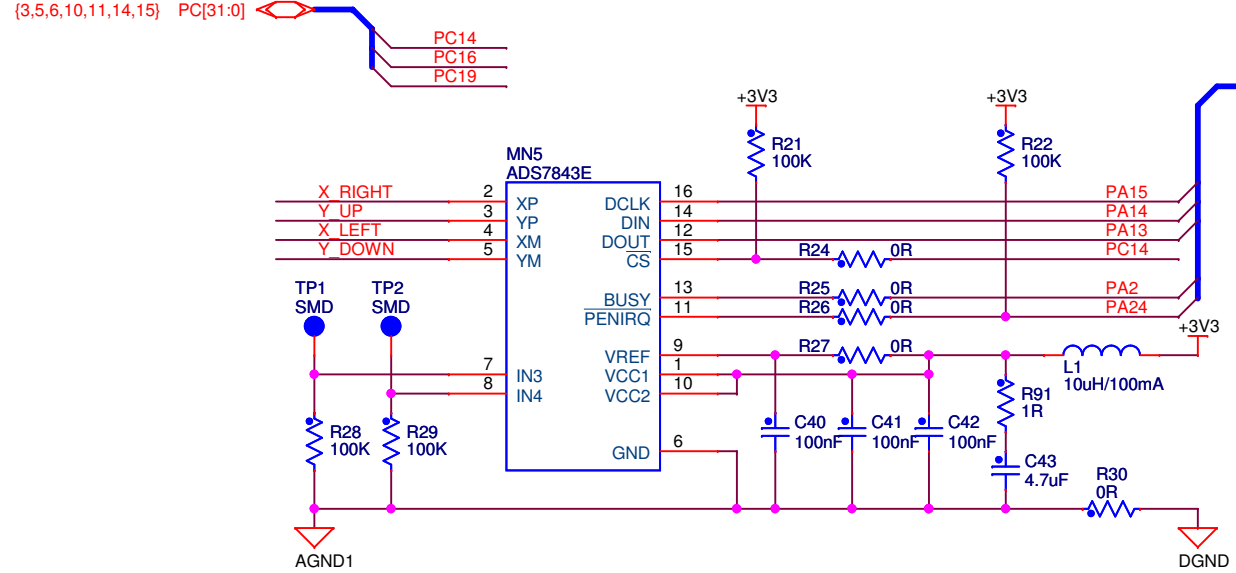
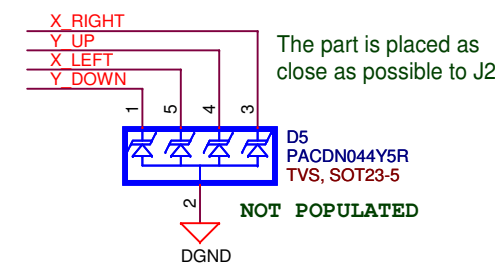
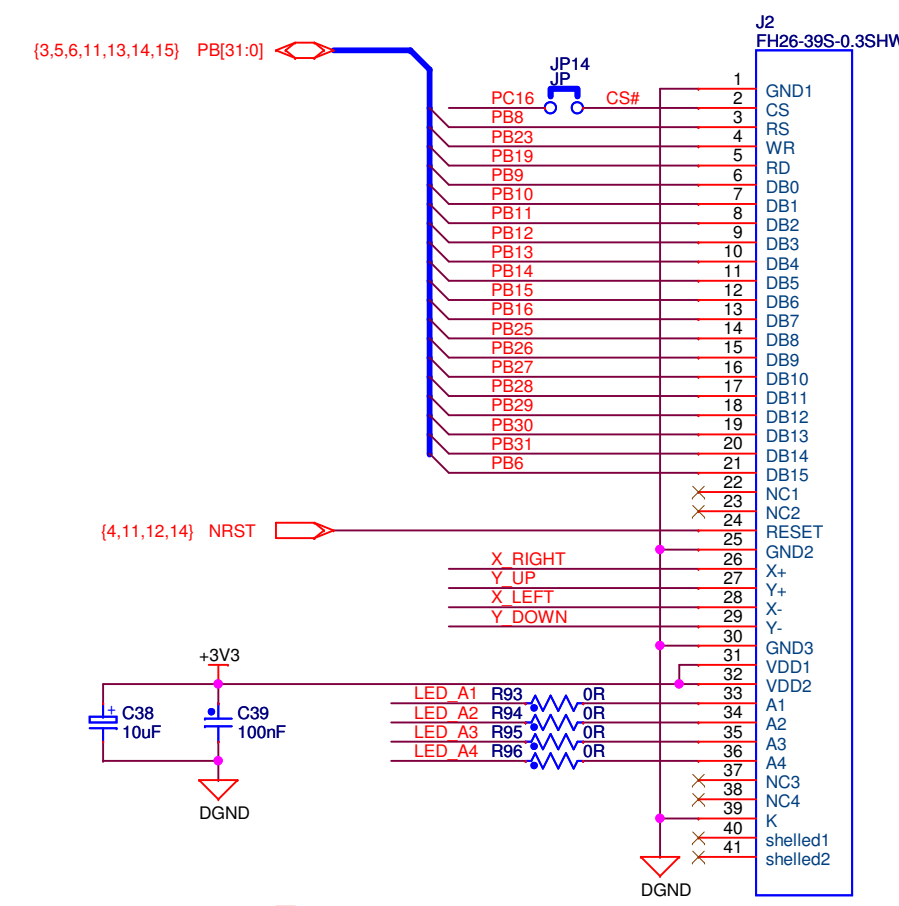


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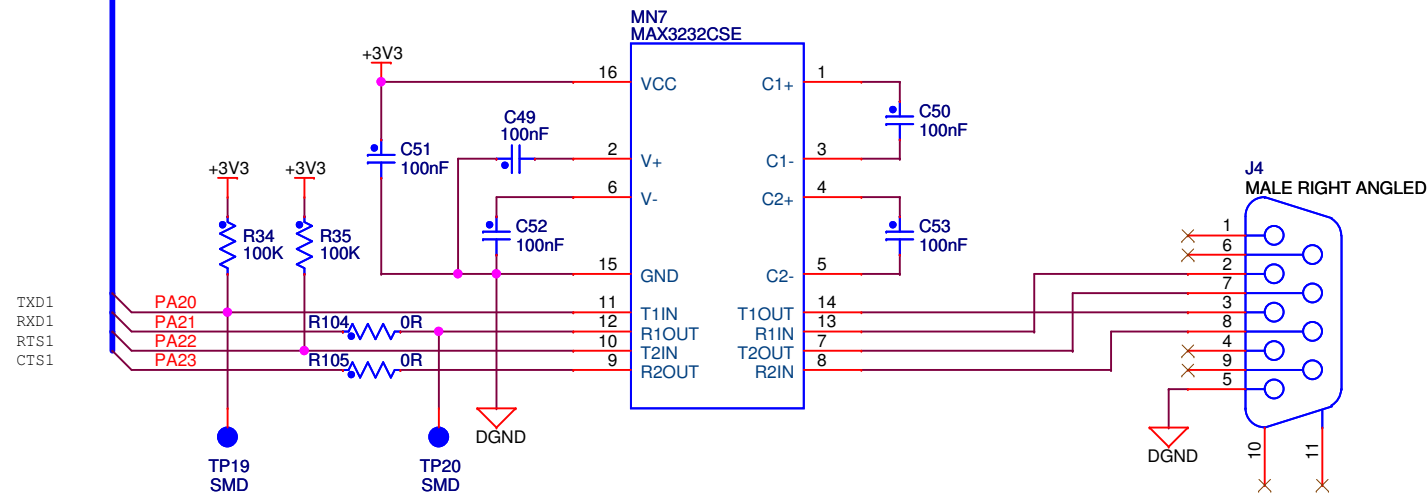
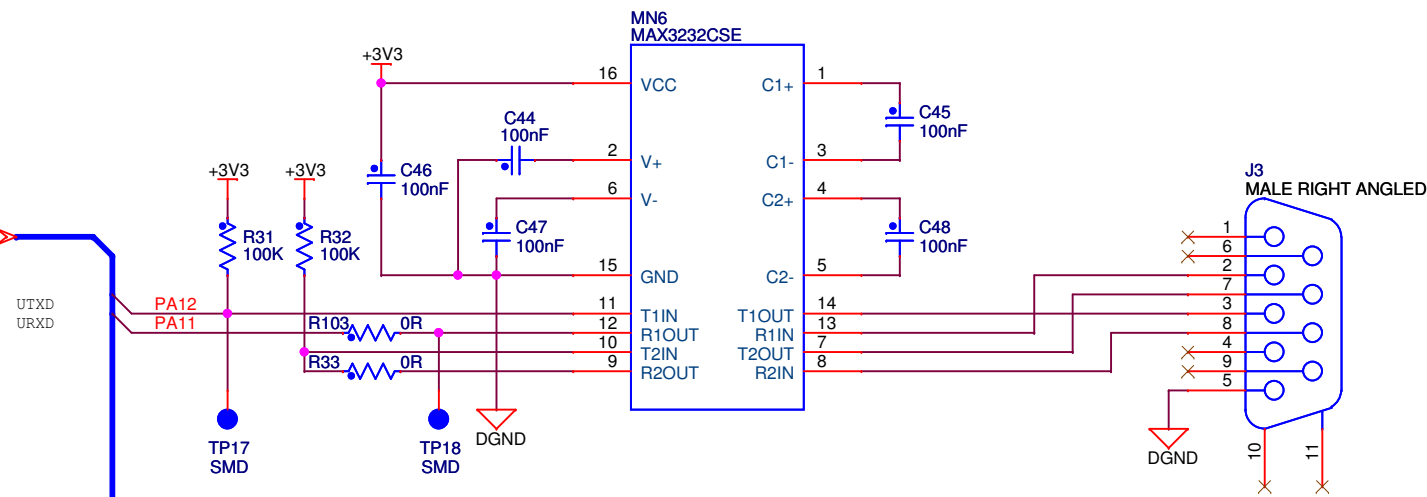
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SAM3U-EK RevB					
EBI Memory II NAND FLASH					

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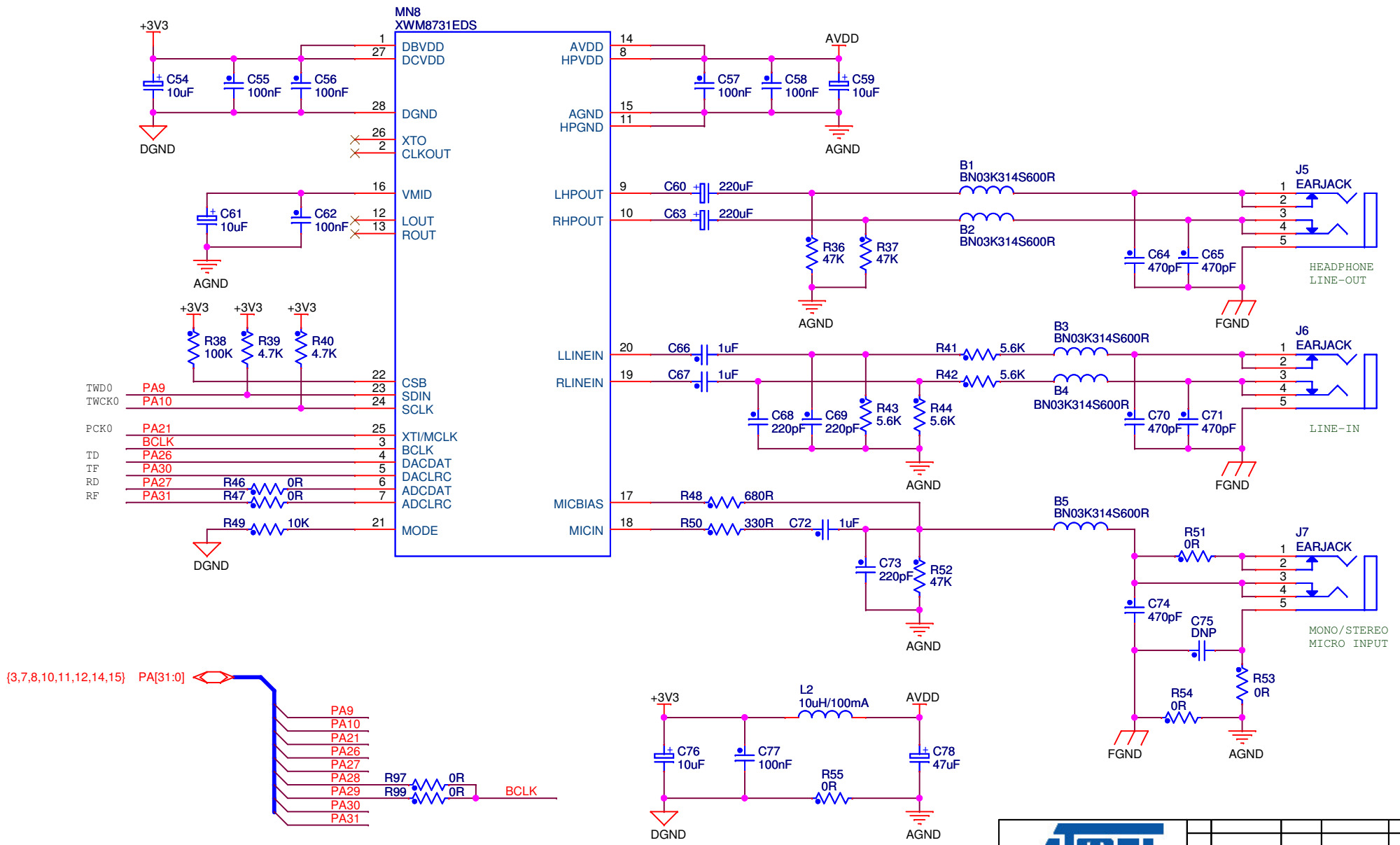


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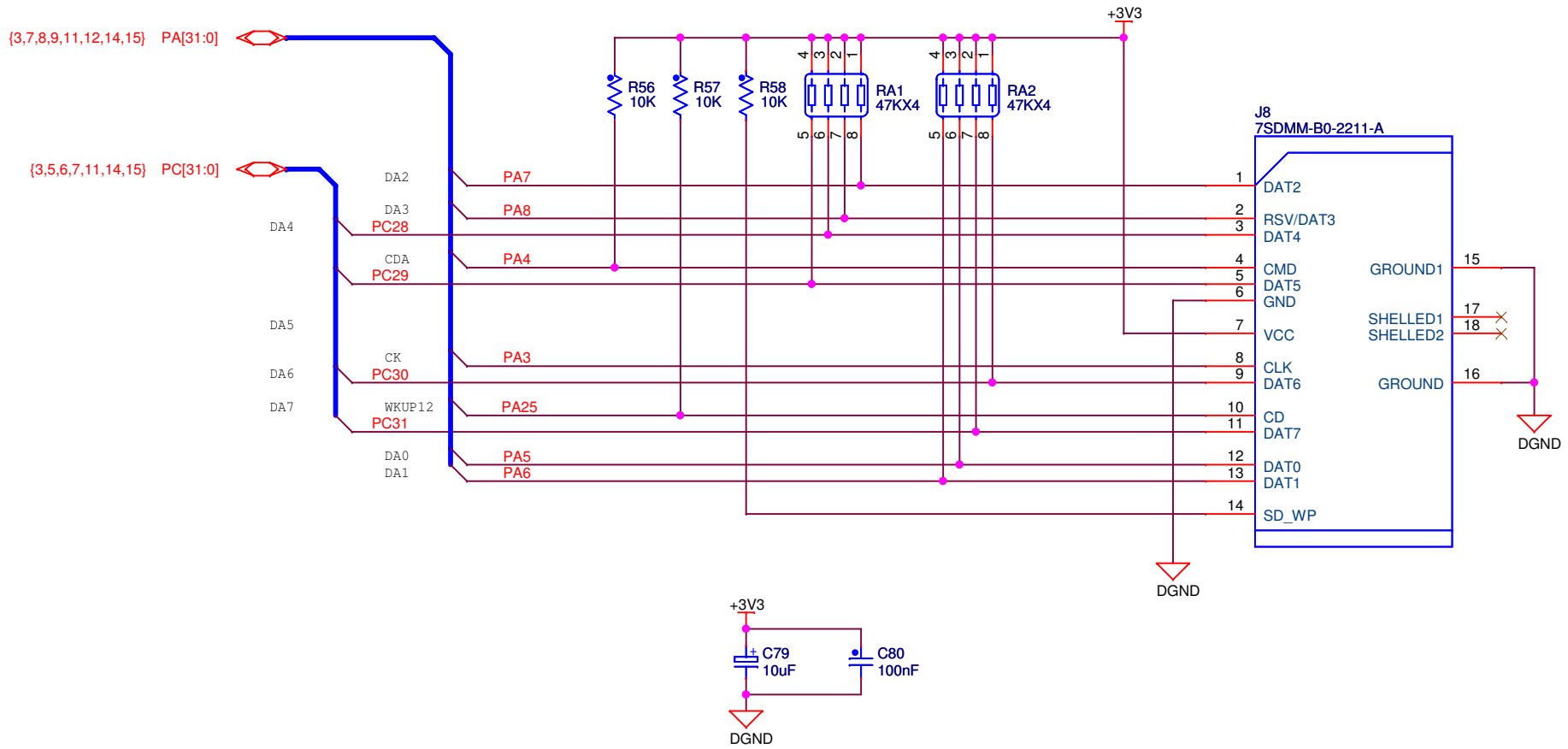


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UART & COM1 RS232					
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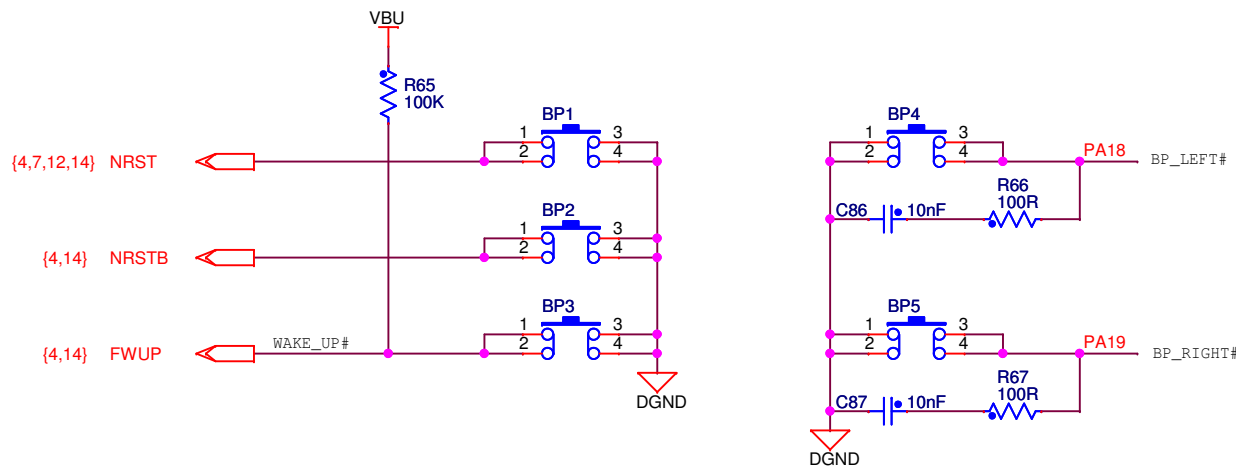
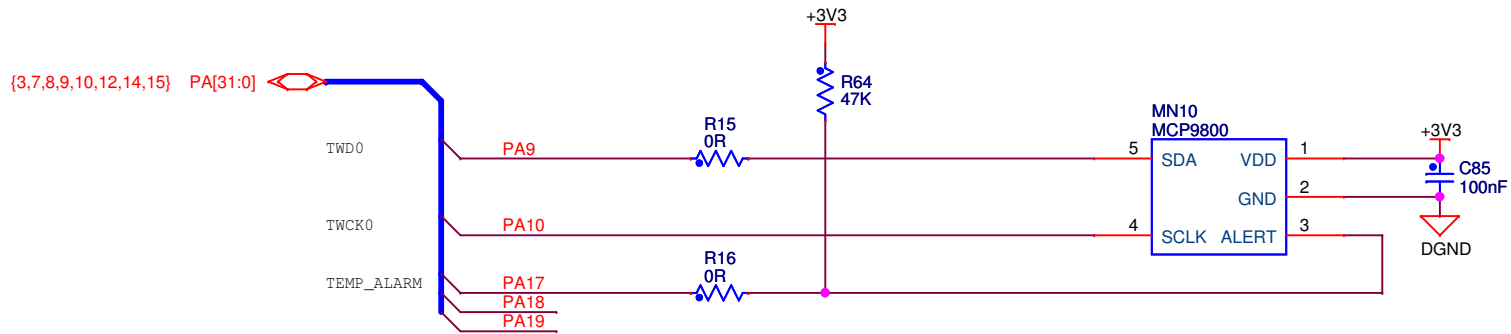
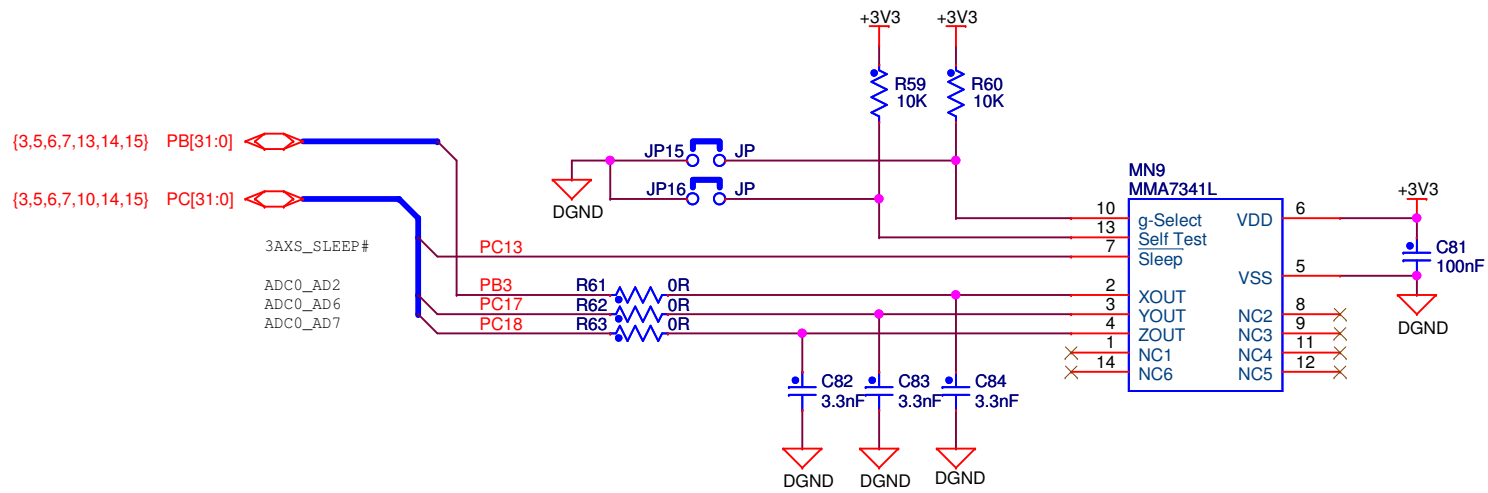


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A	INIT EDIT	ZXL	03-FEB-09	XXX	XX-XX-XX
REV	MODIF.	DES.	DATE	VER.	DATE
SAM3U-EK RevB		SCALE 1/1		REV. B	SHEET 9/15
Audio DAC					

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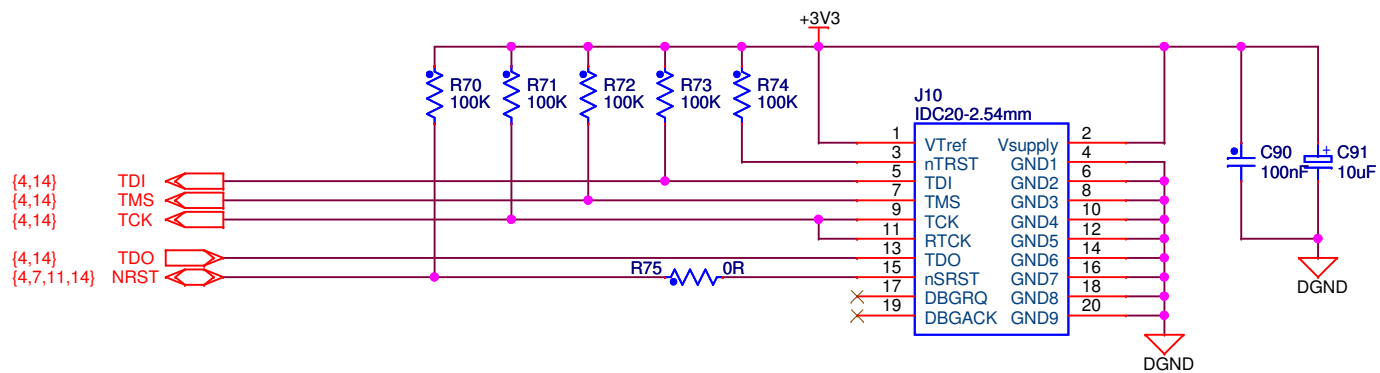
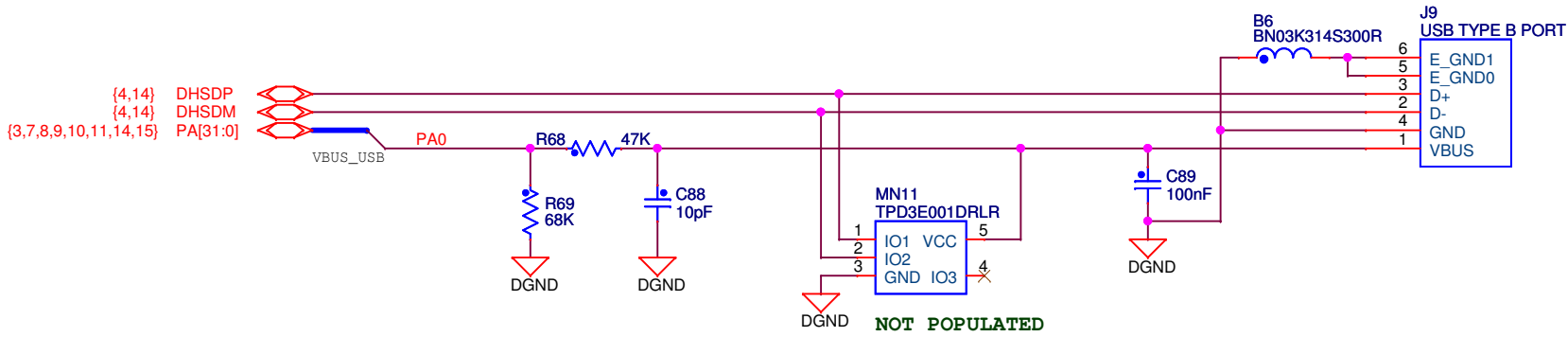


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A	INIT EDIT	ZXL	03-FEB-09	XXX	XX-XXX-XX	
REV	MODIF.	DES.	DATE	VER.	DATE	
SAM3U-EK RevB		SCALE 1/1		REV. B	SHEET 10/15	
SD/MMC interface						
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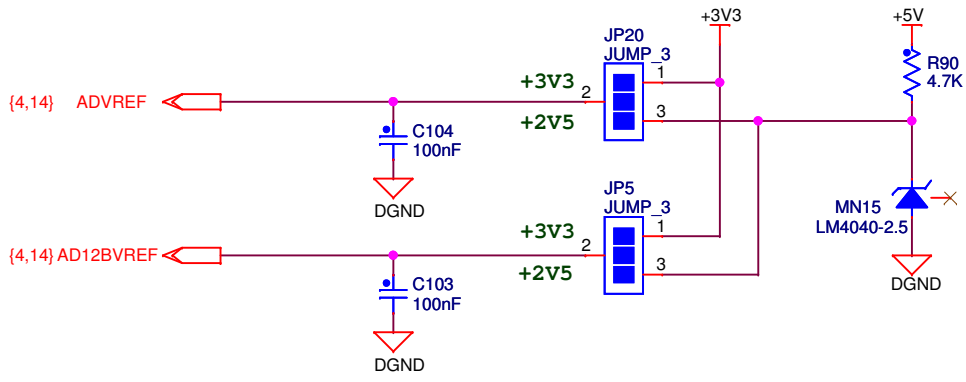
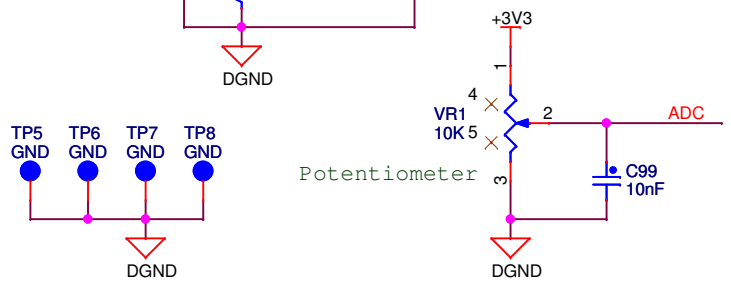
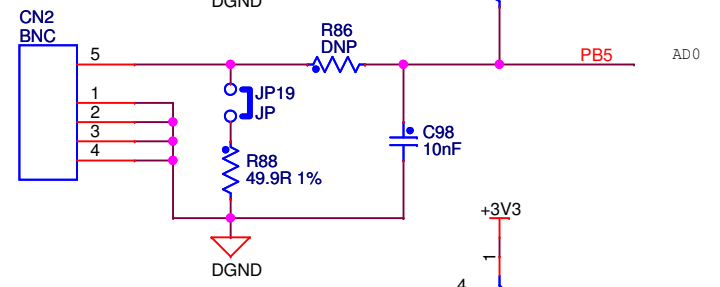
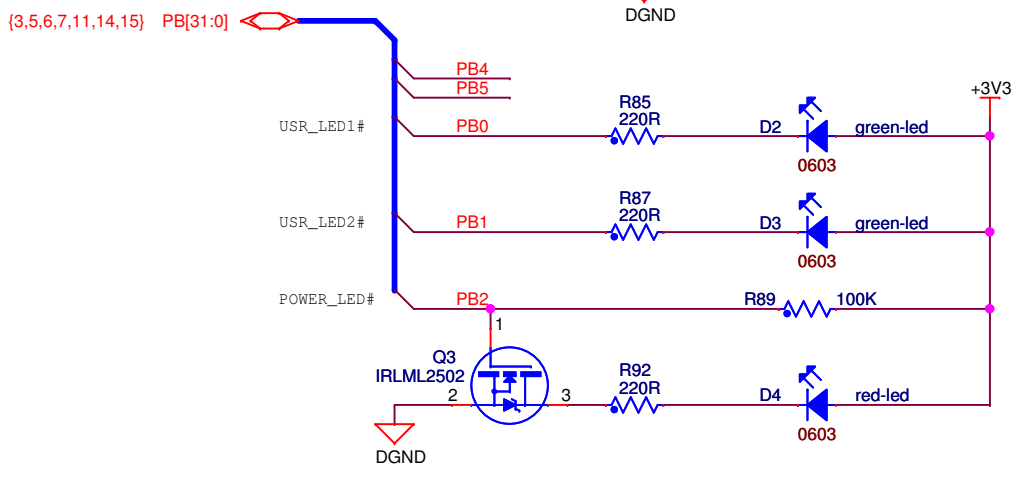
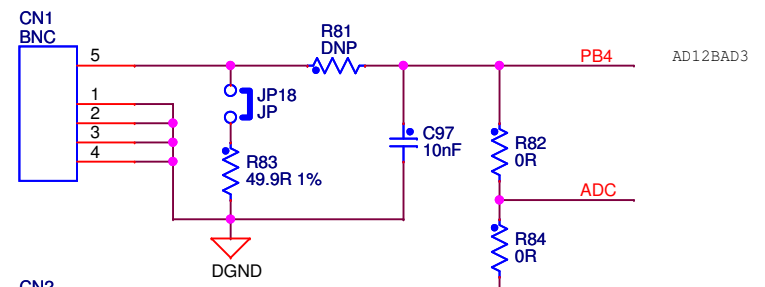
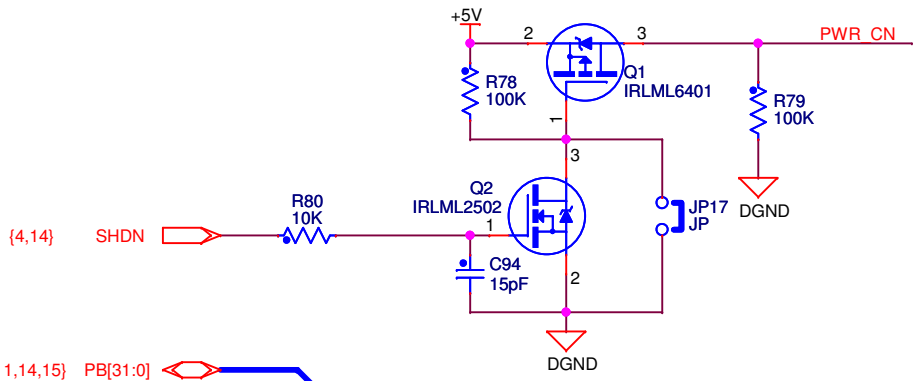
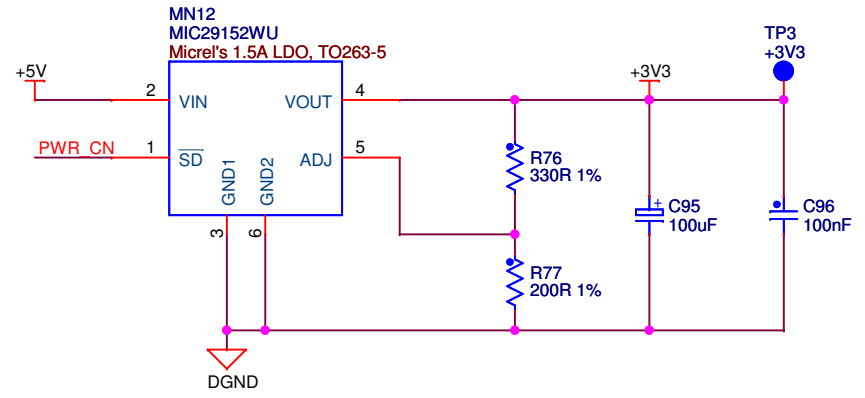
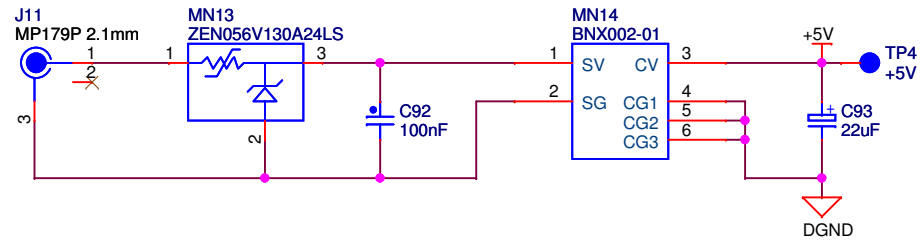


		REV	MODIF.	DES.	DATE	VER.	DATE
		B	INIT EDIT	ZXL	19-MAY-09	PP	20-JAN-10
SAM3U-EK RevB Accelerometer,Temp.Buttons		SCALE	1/1		REV.	SHEET	
				B	11/15		

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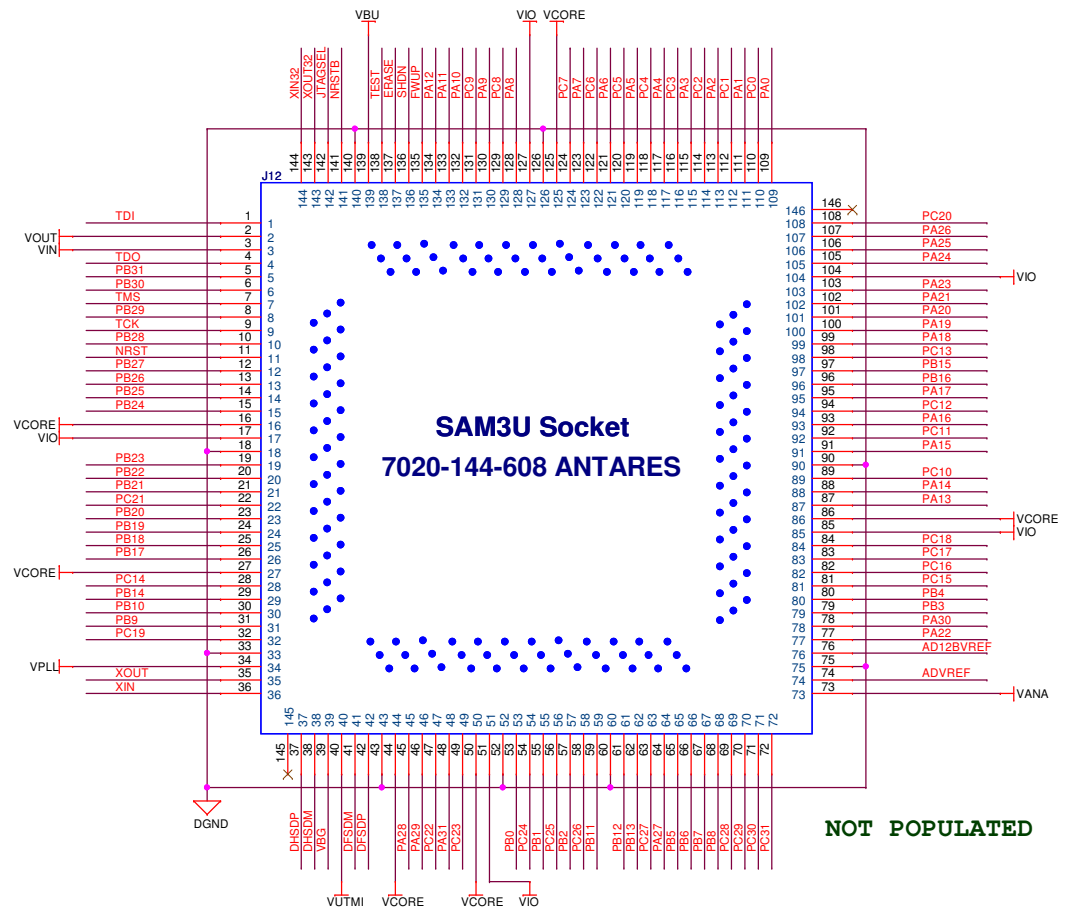
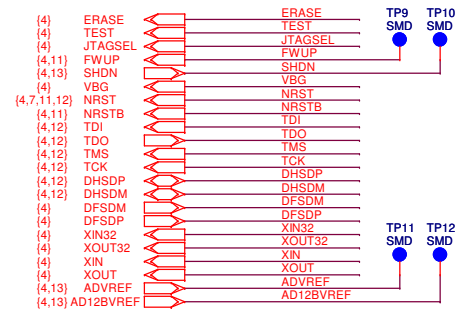
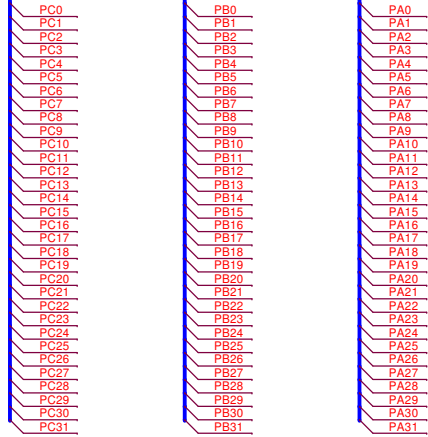


		REV	MODIF.	DES.	DATE	VER.	DATE
		SCALE 1/1				REV. B	SHEET 12/15
SAM3U-EK RevB USB & JTAG							



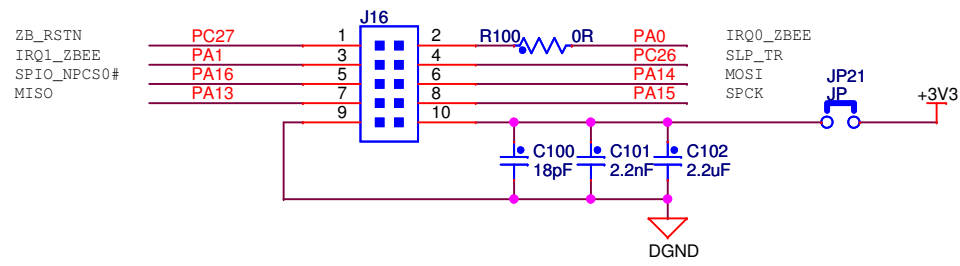
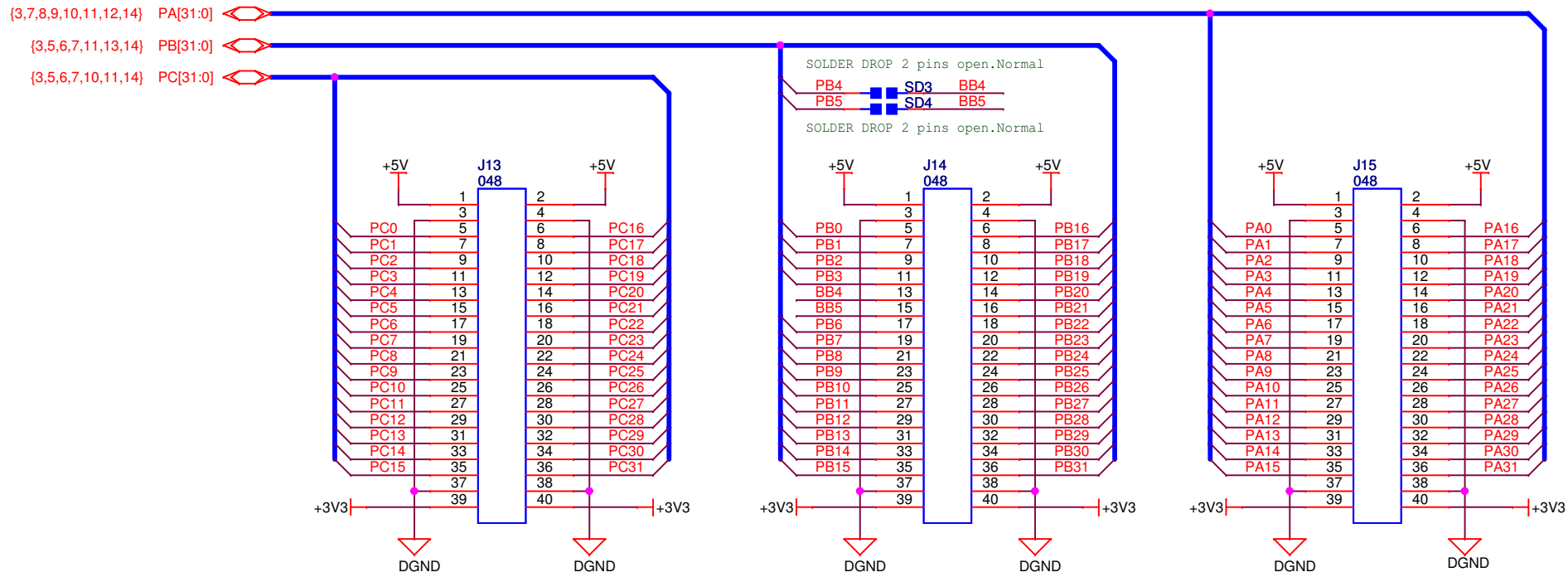
		B	ZXL	19-MAY-09	PP	20-JAN-10	
SAM3U-EK RevB		A	INIT EDIT	ZXL	03-FEB-09	XXX	XX-XX-XX
Power Supply, ADC & Led		REV	MODIF.	DES.	DATE	VER.	DATE
SCALE 1/1						REV.	SHEET
						B	13/15
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(3,7,8,9,10,11,12,15) PA[31:0]
 (3,5,6,7,11,13,15) PB[31:0]
 (3,5,6,7,10,11,15) PC[31:0]



NOT POPULATED

		B	INIT EDIT	ZXL	19-MAY-09
A	MODIF	ZXL	03-FEB-09	XXX	XX-XXX-XX
SAM3U-EK RevB SAM3U socket		SCALE 1/1 	REV. B SHEET 14/15		



ATMEL					
ROUSSET					
B	INIT EDIT	ZXL	19-MAY-09	PP	20-JAN-10
A	MODIF.	ZXL	03-FEB-09	XXX	XX-XXX-XX
REV	SCALE	DES.	DATE	VER.	SHEET
	1/1			B	15/15
User interface & ZigBee					

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Section 6

Troubleshooting

6.1 Self-Test

A test package software is available to implement a functional test for each section of the board. Refer to the SAM3U-EK page on www.atmel.com.

6.2 Board Recovery

The SAM3U-EK is delivered with an on-board recovery procedure allowing to reprogram the board as it was when shipped. This procedure is accessible from the Flash disk mounted on a PC when the board is connected to this PC through the USB as described in [Section 3](#).



Revision History

7.1 Revision History

Table 7-1.

Document	Comments	Change Request Ref.
6478C	Vendor name and reference removed from PSRAM in Section 4.3.2, "Memory" and Figure 4-2, "PSRAM"	6975
6478B	Table 4-8 , JP15 and JP16 Default Settings changed from 'Open' to 'Close'; JP16 Feature edited.	6445
	Table 4-8 , JP17 Default Setting changed from 'Open' to 'Close'; JP17 Feature edited.	6727
6478A	First issue.	



Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com
www.atmel.com/AT91SAM

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