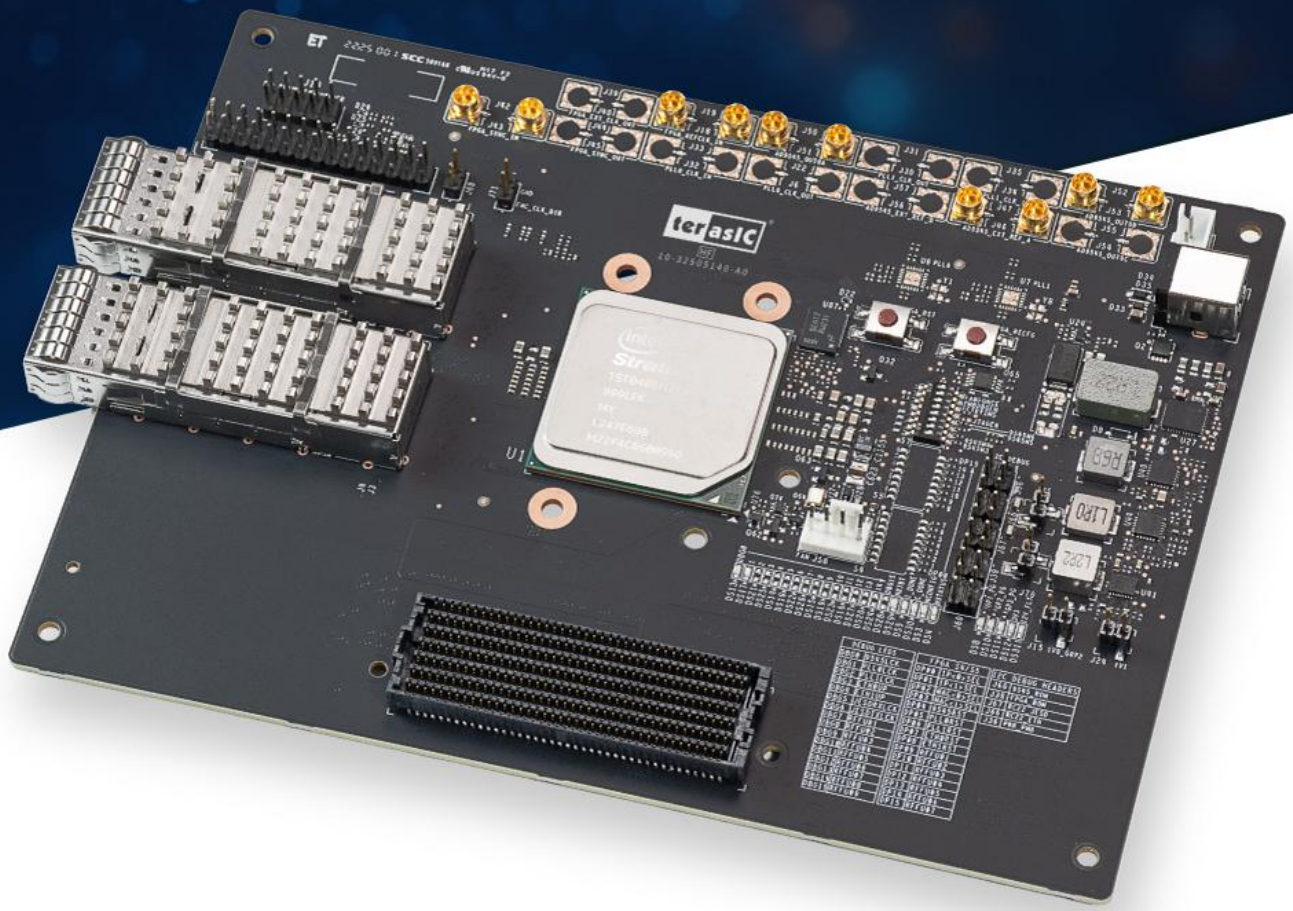
Stratix 10 Sensor Processing Kit



User Manual

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Chapter 1

Introduction

1.1 Overview

The Stratix 10 Sensor Processing Kit is designed to enable quick adoption of the NVIDIA sensor processing capabilities provided within the NVIDIA Holoscan infrastructure. The Stratix 10 Sensor Processing Kit functionality is comprised of a vendor-agnostic FPGA IP and the software that interfaces to that IP to facilitate the processing of sensor data on GPU-enabled NVIDIA host machines.

The Stratix 10 Sensor Processing Kit is based on an Altera Stratix 10 1ST040EH2F35E2VG F PGAand includes a VITATM 57.4 FMC+ connector for interfacing to commercially available vendor sensor boards. The Kit also includes multiple clocking options to facilitate evaluation of a wide range of sensors and sensor topologies. The board also has various user-definable components such as DIP switches, GPIO header pins, LED's, etc.

1.2 Block Diagram

The below diagram shows the components on the Kit and connectivity to the FPGA:

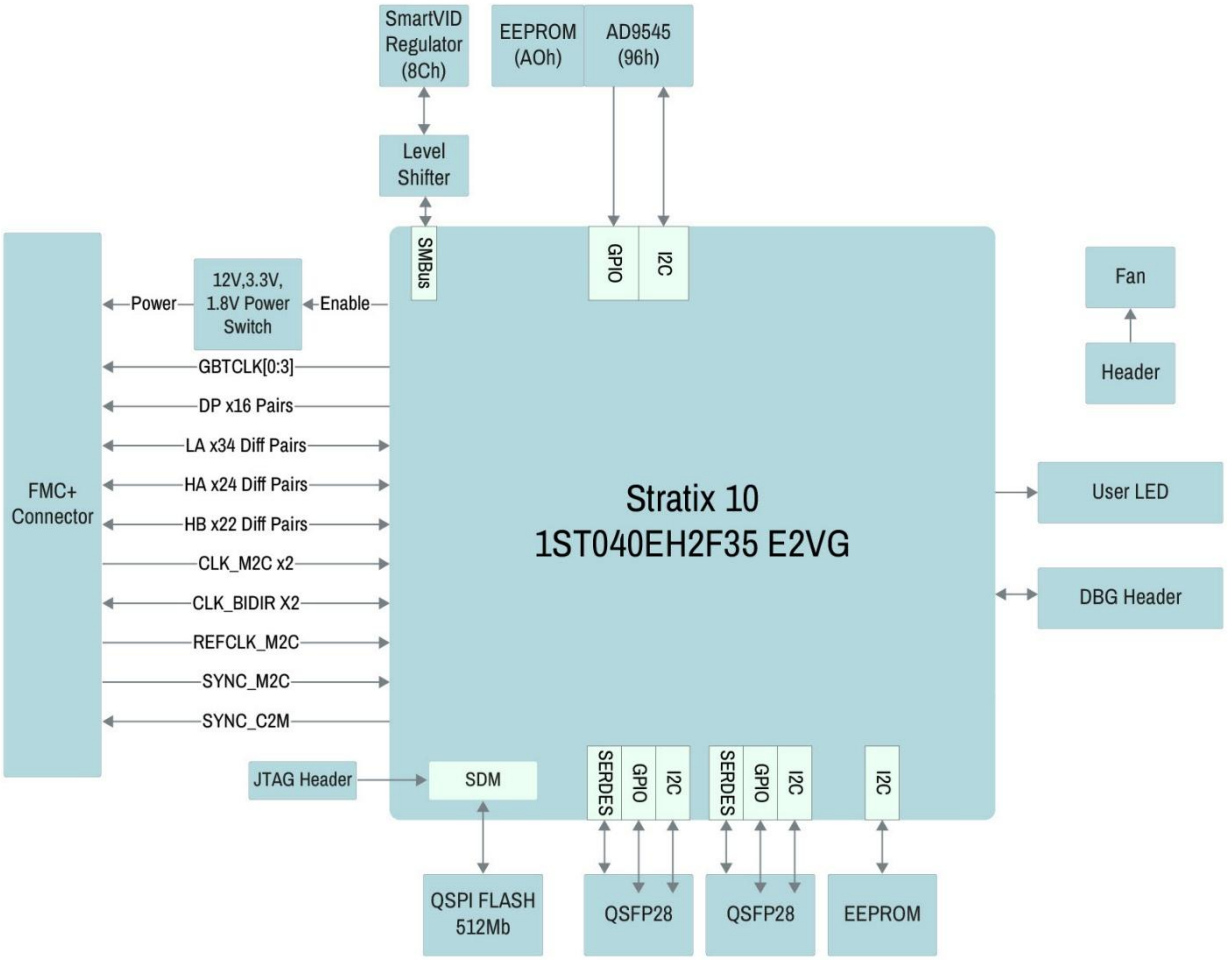


Figure 1-1 Block Diagram

1.3 Board Features

- Stratix 10 1ST040EH2F35E2VG FPGA
- Configuration:
  - JTAG
  - QSPI Flash
- 2kb EEPROM for configuration storage (Ethernet MAC addresses for ex)
- Clocks:
  - 100MHz General Purpose FPGA clock oscillator
  - 156.25MHz E-tile REFCLK1 oscillator for Ethernet
  - AD9545 clock IC
  - Multiple external input/output connection for clocking devices

- Vita 57.4 FMC+ connector
  - 16 High Speed SERDES lanes
  - 4 High Speed Clock lanes

    - 34 Differential pairs via LA bank
    - 24 Differential pairs via HA bank
    - 22 Differential pairs via HB bank
    - Miscellaneous clocks and status
- I2C Debug headers for attached devices
- 2 User LEDs
- 16-pin debug header
- 2x QSFP Ethernet Interfaces supporting up to 100Gbps each

Chapter 2

Board Setup and Configuration

2.1 Layout and Components

Figure 2-1 shows the front side of the board with numbered components of interest:

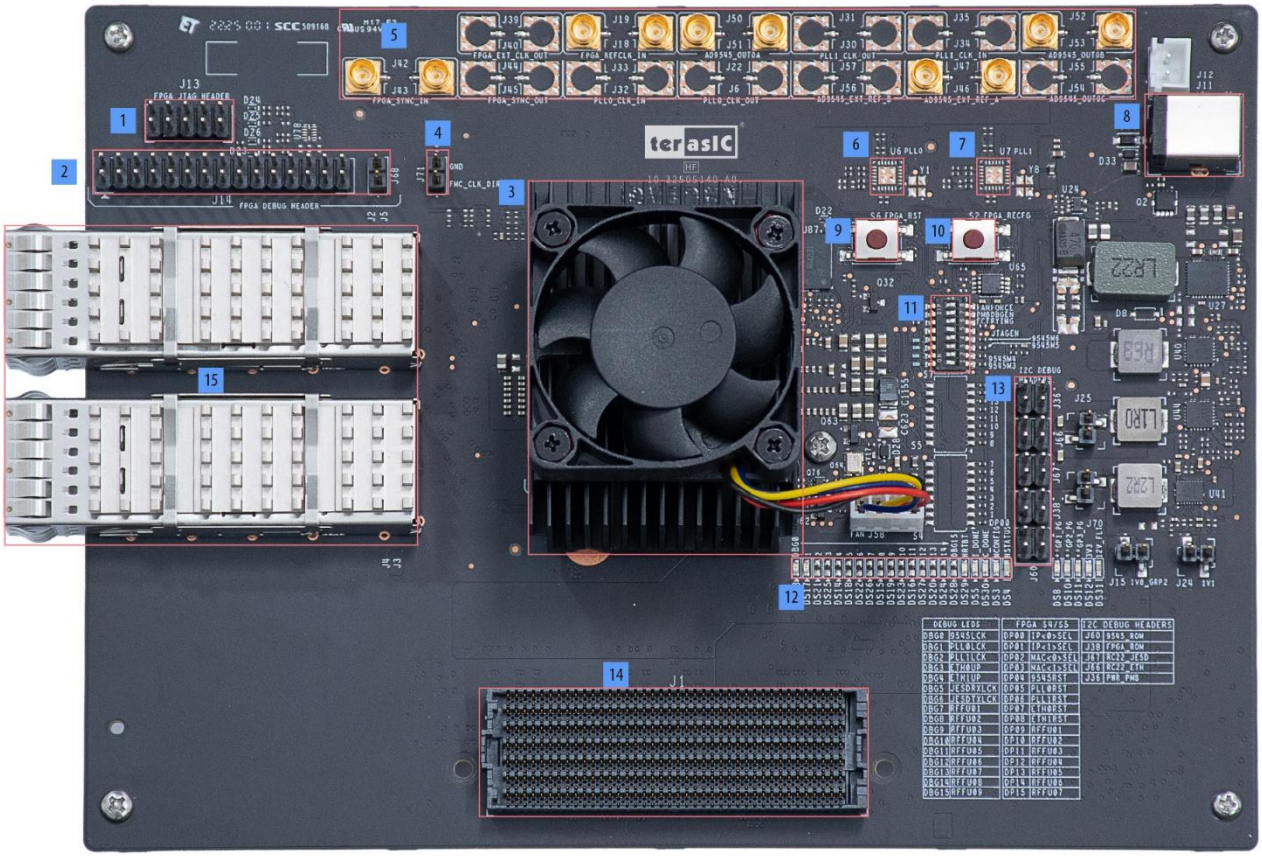


Figure 2-1 Components on Front Side of Board

Table 2-1 Front Side Board Components

Callout	*Component*	*Silkscreen*	*Notes*
1	5x2 JTAG header	J13	JTAG programming header. Compatible with Altera USB-Blaster II.
2	8x2 Pin Header	J14+J78	General Purpose FPGA GPIO Header.
3	Stratix 10 ST040EH2F35E2VG FPGA and Fan	U1	FPGA and cooling solution.
4	2-pin header	J71	Used to force FMC_CLK_DIR if desired.
5	SMP connectors	See board	Internal and external clocking connections.
6	Renesas RC32504 Jitter Attenuator or Clock Generator	U6	One of two Renesas RC32504 clocking ICs.
7	Renesas RC32504 Jitter Attenuator or Clock Generator	U7	One of two Renesas RC32504 clocking ICs.
8	DC Power barrel jack	J11	Main power connector for DC power. 12V @ 5A recommended.
9	FPGA Reset Push Button	S6	General purpose push button input to the FPGA. Recommended to be used for a reset.
10	FPGA Reconfigure Push Button	S2	Push button to force FPGA reconfiguration via QSPI Flash.
11	8 Switch Configuration DIP Bank	S7	DIP switches used for specific board configuration and/or component configuration.
12	Status and User LEDs	See board	General purpose used LEDs.
13	I2C Debug Headers	J60,J38,J67,J66,J36	Debug headers to connect external I2C tools for device debugging and/or configuration.
14	Vita 57.4 FMC+ Connector	J1	Standard FMC+ connector for interfacing to other FMC+ based boards.
15	QSFP Interfaces	J3/J4	QSFP cages for Ethernet connectivity.

The following figure shows the back side of the board with numbered components of interest:

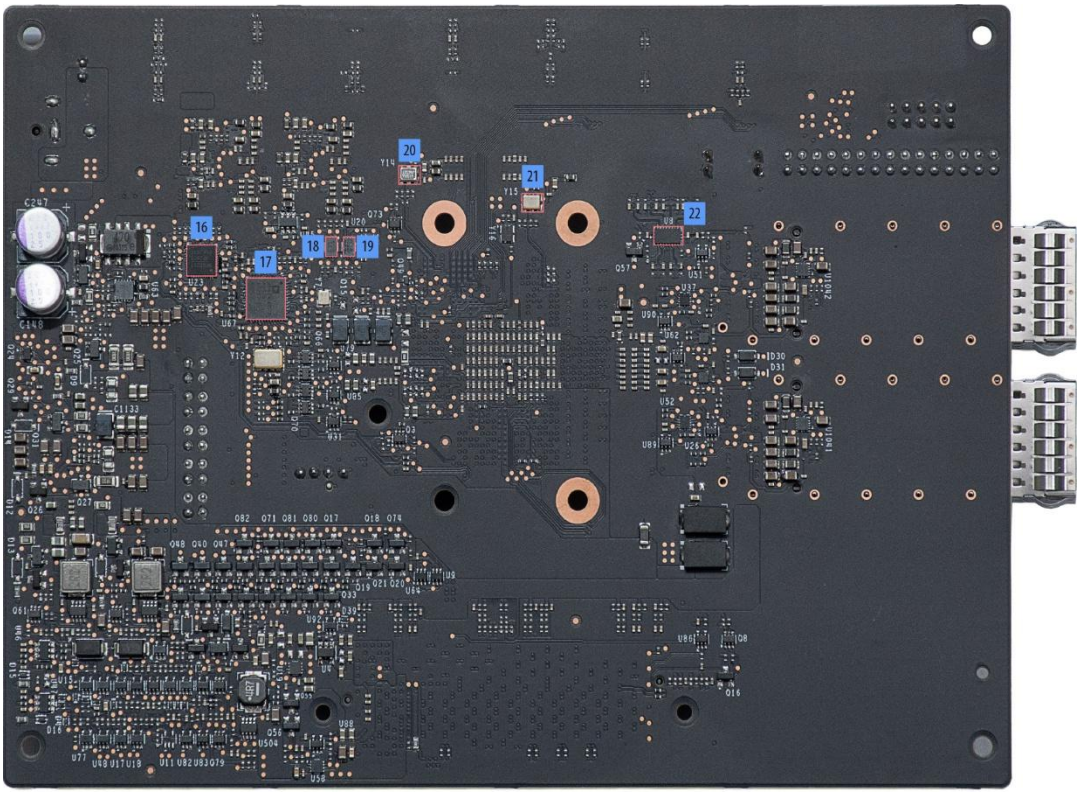


Figure 2-2 Components on Back Side of Board

Table 2-2 Back Side Board Components

Callout	*Component*	*Silkscreen*	*Notes*
16	MPS multiphase power controller	U23	MP2975GU PMBus power controller for FPGA core voltage.
17	AD9545 4-input, 10-output Dual PLL	U67	Analog Devices clocking IC
18	24AA16T EEPROM	U21	16Kb EEPROM used for storage of AD9545 configurations.
19	AT24C02D EEPROM	U20	1Kb EEPROM used for storage of parameters for FPGA use.
20	NX33A00007 Clock Oscillator	Y14	100MHz clock oscillator for general purpose FPGA use.
21	DHA5600003 Clock Oscillator	Y15	156.25MHz clock oscillator used for Ethernet transceivers.
22	PI3DBS12212 Bidirectional Mux	U8	Bidirectional mux used in circuit with the FMC-specified bidirectional clock signals.

2.2 Board Power

The kit receives power via the barrel jack using typical DC power supplies. The recommended operating requirements of the power supply are 12V @ 5A. Example: 12V Power Supply.

Simply plugging in an appropriate supply will power the board. Removing power will power down the board. There is no switch or push button on the board to turn power on or off.

2.3 Default Switch Configuration

The following table shows the default switch positions for the "Configuration DIP Bank" (#11 in above Table 2-1):

Table 2-3 Configuration DIP Bank Defaults

Switch Number	*Switch Label*	*Switch Position*
1	9545M3	ON
2	9545M4	OFF
3	9545M5	OFF
4	9545M6	OFF
5	JTAGEN	ON
6	FCTRYIMG	OFF
7	PMBDBGEN	OFF
8	FANFORCE	OFF

2.4 Stratix 10 FPGA Device Configuration

■ JTAG

The Stratix 10 FPGA can be programmed directly via the JTAG header and an applicable JTAG programming device (Altera USB-Blaster II for example). The FPGA can be programmed with an applicable sof file using the Quartus software. The MT25QU512 QSPI Flash device can also be programmed via the Quartus software using an applicable flash image.

■ Quad SPI

Once the Quad SPI is programmed with an applicable image, the FPGA can be loaded directly by power cycling the board or by pressing the "FPGA Reconfigure" push button (#10).

Chapter 3

Board and Component Descriptions

This chapter provides an instruction to use the board and describes the peripherals.

3.1 Board Power

The below picture shows the power tree of the Board.

Figure 3-1 Power Tree

3.2 Clocking

The following diagram shows the clock connectivity on the Kit. Note that small circles on signals in the diagram indicate an external SMP connection (#5 in Table 2-1, also shown in Figure 3-3)

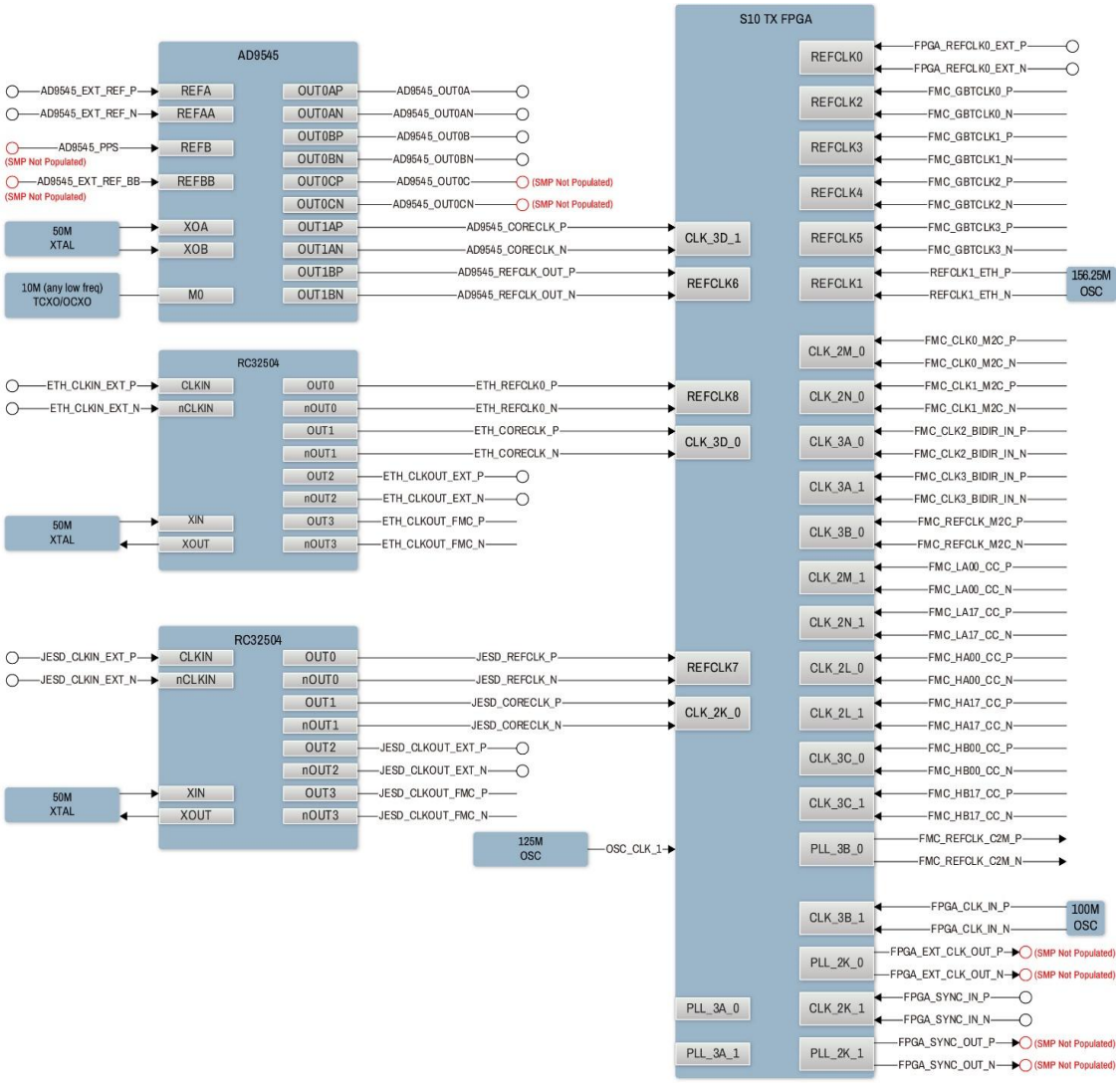


Figure 3-2 Clock Connectivity

The following picture shows the SMP connectors with a numbered label. These will be referenced in the descriptions below.

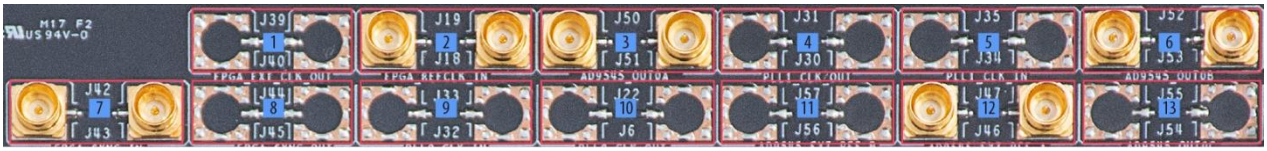


Figure 3-3 SMP Connectors

3.2.1 E-Tile Transceiver Reference Clocks

The Stratix 10 E-tile transceivers allow up to nine reference clocks to be connected to the FPGA. All E-tile reference clocks are connected to a clock resource as shown above in **Figure 3-2**. Of importance, REFCLK1 is connected to a fixed 156.25MHz oscillator. This facilitates two requirements in usage of the E-tile:

1. REFCLK1 must be bonded out for any reference clock switching scenarios and
2. The E-tile transceivers must be sourced with a stable reference clock prior to FPGA configuration else the device will not configure correctly.

The following table lists the E-tile reference clocks and their respective sources:

Table 3-1 E-tile reference clocks and their respective sources

Clock Name	*Source*	*Description*
REFCLK0	SMP Pair (#2 in Figure 3-3)	A pair of SMP connectors is provided such that an external clock can drive the E-tile reference clock.
REFCLK1	Fixed 156.25MHz oscillator	This is the reference clock for the Ethernet transceivers and can be used as the default reference clock for the FMC transceivers.
REFCLK2	FMC_GBTCLK_0	High speed clock pair from the FMC+ connector.
REFCLK3	FMC_GBTCLK_1	High speed clock pair from the FMC+ connector.
REFCLK4	FMC_GBTCLK_2	High speed clock pair from the FMC+ connector.
REFCLK5	FMC_GBTCLK_3	High speed clock pair from the FMC+ connector.
REFCLK6	Differential output from AD9545	OUT1B from the AD9545 clock IC.

3.2.2 AD9545 IC

The Analog Device 9545 clocking IC is a quad input, 10-output dual DPLL chip. More information on the device can be found here: [AD9545 Datasheet and Product Info | Analog Devices]

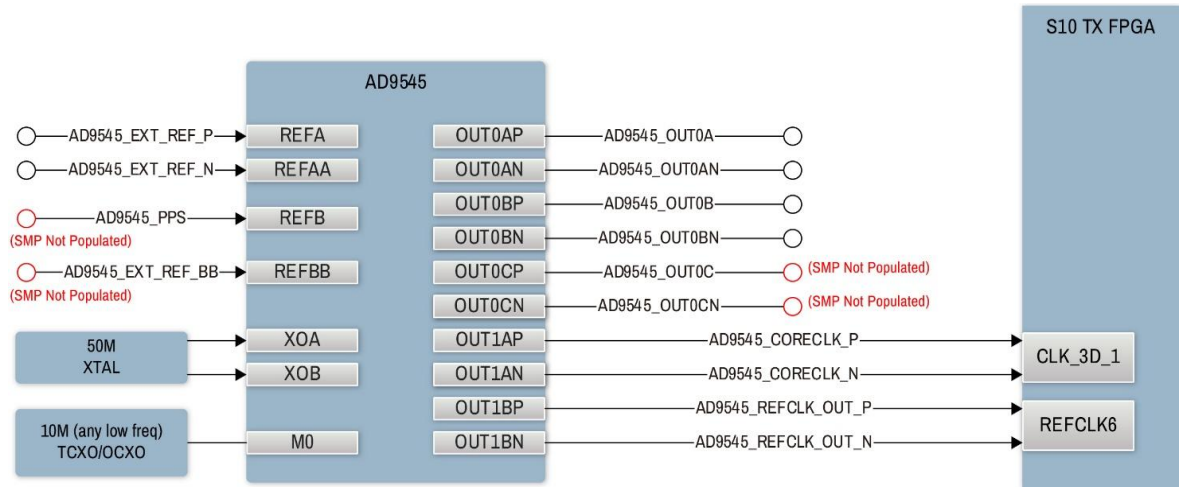


Figure 3-4 AD9545 IC

The below table lists the clock connectivity of the AD9545:

Table 3-2 AD9545 Clock Connectivity

AD9545 Pin	*Direction (relative to AD9545)*	*Connectivity*	*Notes*
REFA	Input	With REFA, differential input from SMP connectors. See #12 in Figure 3-3.	
REFAA	Input	With REFAA, differential input from SMP connectors. See #12 in Figure 3-3.	
REFB	Input	Single ended input from SMP connector. This SMP connector is not populated, see #11 in Figure 3-3.	
REFBB	Input	Single ended input from SMP connector. This SMP connector is not populated, see #11 in Figure 3-3.	
X0A	Input	With X0B, connected to a 50MHz XTAL	Used as reference clock for the AD9545 system clock PLL.
X0B	Output	With X0A, connected to a 50MHz XTAL	Used as reference clock for the AD9545 system clock PLL.
OUT0AP	Output	With OUT0AN, differential connection to SMPs. See #3 in Figure 3-3.	
OUT0AN	Output	With OUT0AP, differential connection to SMPs. See #3 in Figure 3-3.	
OUT0BP	Output	With OUT0BN, differential connection to SMPs. See #6 in Figure 3-3.	
OUT0BN	Output	With OUT0BP, differential connection to SMPs. See #6 in Figure 3-3.	

OUT0CP	Output	With OUT0CN, differential connection to SMPs. This SMP connector is not populated, see #13 in Figure 3-3.	
OUT0CN	Output	With OUT0CP, differential connection to SMPs. This SMP connector is not populated, see #13 in Figure 3-3..	
OUT1AP	Output	With OUT1AN, differential connection to the clock capable input 1 in bank 3D of the FPGA.	FPGA pin CLK_3D_1_P
OUT1AN	Output	With OUT1AP, differential connection to the clock capable input 1 in bank 3D of the FPGA.	FPGA pin CLK_3D_1_N
OUT1BP	Output	With OUT1BN, differential connection to the FPGA E-tile reference clock 6.	FPGA pin REFCLK_GXEL8A_CH6_P
OUT1BN	Output	With OUT1BP, differential connection to the FPGA E-tile reference clock 6.	FPGA pin REFCLK_GXEL8A_CH6_N

■ AD9545 EEPROM

There is an EEPROM attached to the AD9545 that can be used to store the chip's configurations. This allows for the AD9545 to provide clocks right after board power up. This could be important for an FPGA design that utilizes the AD9545 to source the reference clock to any FPGA transceiver.

The simplified connectivity of the EEPROM to the AD9545 via an I2C interface is shown below:

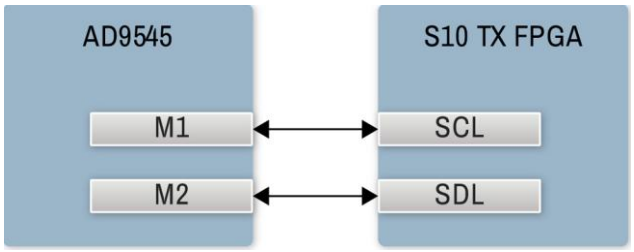


Figure 3-5 AD9545 EEPROM Connectivity

The EEPROM is connected to the AD9545's M1 and M2 mode pins. More details on the operation of the AD9545's configuration storage capabilities can be found in documentation located at this link: AD9545 Documentation. Not shown above, there is also connectivity to the I2C signals via a debug header on the board. The debug headers are discussed in section FIXME.

■ I2C Interface

The AD9545 also has its own I2C interface. The I2C signals are directly connected to the FPGA.

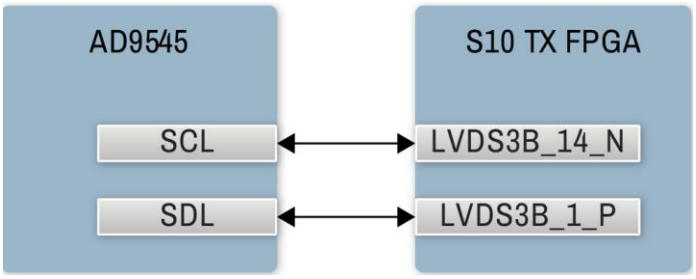


Figure 3-6 AD9545 I2C Interface Connectivity

■ Miscellaneous Signals

The below table lists other pin connectivity on the AD9545.

Table 3-3 AD9545 Miscellaneous Pin Connectivity

AD9545 Pin	*Direction (relative to AD9545)*	*Connection(s)*	*Notes*
M0	Input/Output	Connected to the output of a 40MHz TCXO. Also routed to FPGA pin LVDS3B_3_N.	See the AD9545 documentation for details on using this feature.
M1	Input/Output	Connected to the SCL pin of the AD9545 EEPROM and to I2C debug header. Also routed to FPGA pin LVDS3B_3_P.	See the AD9545 documentation for details on how the mode pins operate in EEPROM configuration mode.
M2	Input/Output	Connected to the SDA pin of the AD9545 EEPROM and to I2C debug header. Also routed to FPGA pin LVDS3B_5_N.	See the AD9545 documentation for details on how the mode pins operate in EEPROM configuration mode.
M3	Input/Output	Connected to switch 1 on DIP bank #11 in Figure 2-1. Also connected to FPGA pin LVDS3B_7_P.	If set to a 1, the AD9545 will load its configuration from EEPROM. See the AD9545 documentation for more details.
M4	Input/Output	Connected to switch 2 on DIP bank #11 in Figure 2-1. Also connected to FPGA pin LVDS3B_9_N.	See the AD9545 documentation for more details.
M5	Input/Output	Connected to switch 3 on DIP bank #11 in Figure 2-1. Also connected to FPGA pin LVDS3B_11_N.	See the AD9545 documentation for more details.
M6	Input/Output	Connected to switch 3 on DIP bank #11 in Figure 2-1. Also connected to FPGA pin LVDS3B_9_P.	See the AD9545 documentation for more details.
RESETB_N	Input	Connected to FPGA pin LVDS3B_1_N.	Active low reset to the AD9545. Can be driven via the FPGA (active low

			assertion). There is a 100k pullup resistor in the AD9545.

3.2.3 FMC Bidirectional Clocks

There are two differential bidirectional clocks specified in the VITA 57.4 FMC+ standard. The directionality of these clocks is defined by another FMC+ signal, CLK_DIR signal, also defined as part of the VITA 57.4 standard. When CLK_DIR is tied to or driven to GND, the two bidirectional clocks are outputs from the FMC-connected device to the carrier card (kit) and ultimately the FPGA. When CLK_DIR is pulled or driven high, then the bidirectional clocks are sourced from the carrier card (kit) to the FMC connected device.

On the Board there is a circuit that utilizes a bidirectional multiplexer to route these bidirectional clocks to either the FPGA (when CLK_DIR = 0) or from the RC32504 devices towards the FMC-connected device (when CLK_DIR = 1).

The below diagram shows the clock connectivity when CLK_DIR = 0:

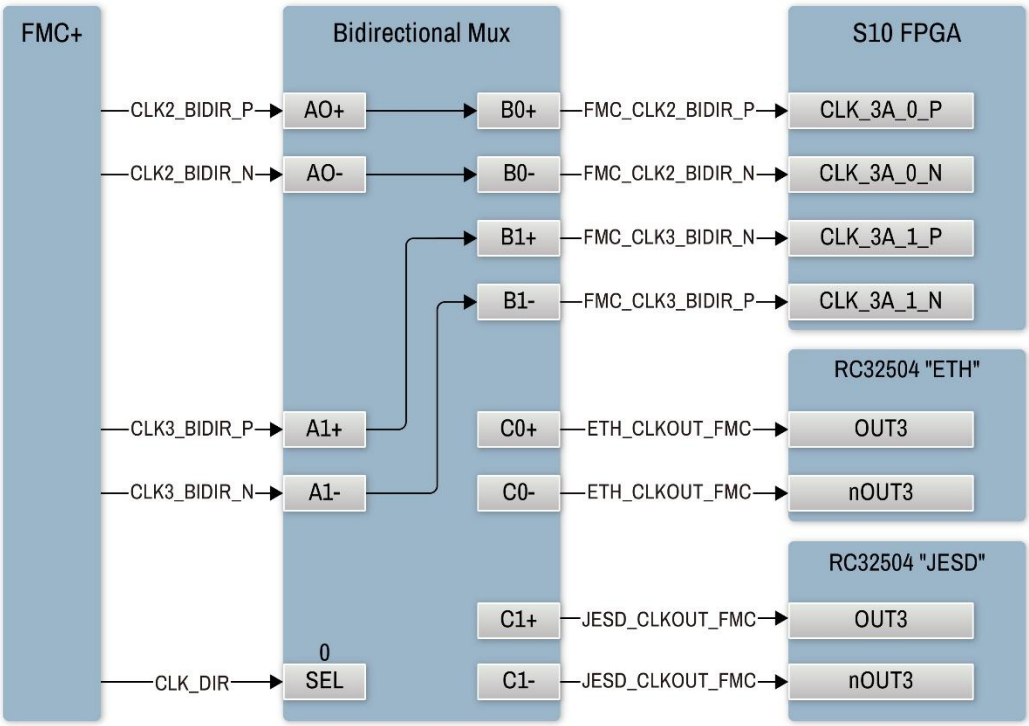


Figure 3-7 FMC Bidirectional Clocks When CLK_DIR=0

When CLK_DIR = 0, the two clocks are driven from the FMC. These clocks are muxed onto the clock pairs that are connected to the FPGA as shown.

The below diagram shows the clock connectivity when CLK_DIR = 1:

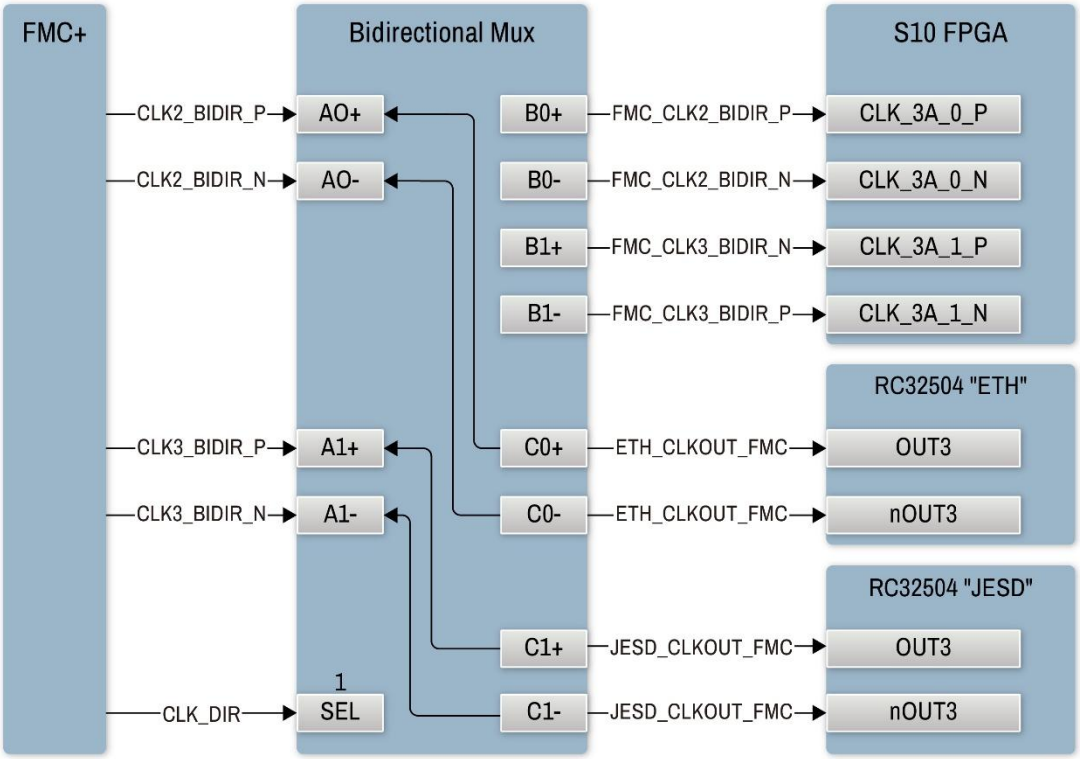


Figure 3-8 FMC Bidirectional Clocks When CLK_DIR=1

When CLK_DIR = 1, both of the RC32504 devices source clocks via their OUT3 interfaces. These clocks are muxed onto the clock pairs going over to the FMC connector.

■ FMC_CLK_DIR Header:

There is a 2-pin header on the board. See #4 in Table 2-1. This header can be used to force the CLK_DIR to GND if desired. Placing a jumper across the header pins will for CLK_DIR to GND.

3.2.4 Other FPGA Clock Connectivity

The following table lists the other clocks that are provisioned to/from the FPGA. Most of these clocks are connected to the FMC+ interface. The FMC+ standard defines several clock capable pairs of signals within each IO bank. The usage of these signals is dependent on the FMC board attached to the kit. Other than the OSC_CLK_1, most of the below could be provisioned as FPGA inputs or outputs depending on use cases and FMC-connected boards.

Table 3-4 Other FPGA Clock Connectivity

FPGA Pin	*Direction (Relative to FPGA)*	*Connectivity*	*Notes*
OSC_CLK_1	Input	125MHz oscillator.	This clock is required by the FPGA for proper configuration.
CLK_2K_1_P	Input	FPGA_SYNC_IN_P routed to SMP connector. See #7 in Figure 3-3.	This external connection can be used for a general purpose clock or synchronization signal to the FPGA.
CLK_2K_1_N	Input	FPGA_SYNC_IN_N routed to SMP connector. See #7 in Figure 3-3.	This external connection can be used for a general purpose clock or synchronization signal to the FPGA.
CLK_2L_0_P	Input	FMC_HA00_CC_P	Vita 54.7-defined clock capable IO in the HA bank of the FMC+ connector.
CLK_2L_0_N	Input	FMC_HA00_CC_N	Vita 54.7-defined clock capable IO in the HA bank of the FMC+ connector.
CLK_2L_1_P	Input	FMC_HA17_CC_P	Vita 54.7-defined clock capable IO in the HA bank of the FMC+ connector.
CLK_2L_1_N	Input	FMC_HA17_CC_N	Vita 54.7-defined clock capable IO in the HA bank of the FMC+ connector.
CLK_2M_0_P	Input	FMC_CLK0_M2C_P	Vita 54.7-defined differential clock sourced from FMC to FPGA.

CLK_2M_0_N	Input	FMC_CLK0_M2C_N	Vita 54.7-defined differential clock sourced from FMC to FPGA.
CLK_2M_1_P	Input	FMC_LA00_CC_P	Vita 54.7-defined clock capable IO in the LA bank of the FMC+ connector.
CLK_2M_1_N	Input	FMC_LA00_CC_N	Vita 54.7-defined clock capable IO in the LA bank of the FMC+ connector.
CLK_2N_0_P	Input	FMC_CLK1_M2C_P	Vita 54.7-defined differential clock sourced from FMC to FPGA.
CLK_2N_0_N	Input	FMC_CLK1_M2C_N	Vita 54.7-defined differential clock sourced from FMC to FPGA.
CLK_2N_1_P	Input	FMC_LA17_CC_P	Vita 54.7-defined clock capable IO in the LA bank of the FMC+ connector.
CLK_2N_1_N	Input	FMC_LA17_CC_N	Vita 54.7-defined clock capable IO in the LA bank of the FMC+ connector.
CLK_3A_0_P	Input	FMC_CLK2_BIDIR_P	Vita 54.7-defined differential bidirectional clock. See FMC Bidirectional Clocks for details.
CLK_3A_0_N	Input	FMC_CLK2_BIDIR_N	Vita 54.7-defined differential bidirectional clock. See FMC Bidirectional Clocks for details.
CLK_3A_1_P	Input	FMC_CLK3_BIDIR_P	Vita 54.7-defined differential bidirectional clock. See FMC Bidirectional Clocks for details.
CLK_3A_1_N	Input	FMC_CLK3_BIDIR_N	Vita 54.7-defined differential bidirectional clock. See FMC Bidirectional Clocks for details.

CLK_3B_0_P	Input	FMC_REFCLK_M2C_P	Vita 54.7-defined differential reference clock sourced from FMC to FPGA.
CLK_3B_0_N	Input	FMC_REFCLK_M2C_N	Vita 54.7-defined differential reference clock sourced from FMC to FPGA.
CLK_3B_1_P	Input	FPGA_CLK_IN_P	Differential 100MHz oscillator used for general purpose FPGA clocking.
CLK_3B_1_N	Input	FPGA_CLK_IN_N	Differential 100MHz oscillator used for general purpose FPGA clocking.
CLK_3C_0_P	Input	FMC_HB00_CC_P	Vita 54.7-defined clock capable IO in the HB bank of the FMC+ connector.
CLK_3C_0_N	Input	FMC_HB00_CC_N	Vita 54.7-defined clock capable IO in the HB bank of the FMC+ connector.
CLK_3C_1_P	Input	FMC_HB17_CC_P	Vita 54.7-defined clock capable IO in the HB bank of the FMC+ connector.
CLK_3C_1_N	Input	FMC_HB17_CC_N	Vita 54.7-defined clock capable IO in the HB bank of the FMC+ connector.
PLL_2K_0_P	Output	FPGA_EXT_CLK_OUT_P	An FPGA clock or general purpose signal can be sourced to SMP connector. This SMP connector is not populated, see #1 in Figure 3-3.
PLL_2K_0_N	Output	FPGA_EXT_CLK_OUT_N	An FPGA clock or general purpose signal can be sourced to SMP connector. This SMP connector is not populated, see #1 in Figure 3-3.
PLL_2K_1_P	Output	FPGA_SYNC_OUT_P	An FPGA synchronization signal, clock, or general purpose signal can be sourced to SMP connector. This SMP connector is not populated, see #8 in Figure 3-3.

PLL_2K_1_N	Output	FPGA_SYNC_OUT_N	An FPGA synchronization signal, clock, or general purpose signal can be sourced to SMP connector. This SMP connector is not populated, see #8 in Figure 3-3.
PLL_3B_0_P	Output	FMC_REFCLK_C2M_P	Vita 54.7-defined differential clock sourced to FMC connector.
PLL_3B_0_N	Output	FMC_REFCLK_C2M_N	Vita 54.7-defined differential clock sourced to FMC connector.

3.3 QSFP Interfaces

The kit has two QSFP interfaces that are used for connections to external Host machines using standard Ethernet protocols. See #15 in Table 2-1. Each interface is comprised of four high-speed SERDES lanes that connect to four transceivers in the FPGA E-tile, GPIO, and an I2C interface. IP available from Altera can be used to implement the Ethernet functionality in the FPGA.

The below tables describe the signals associated with the QSPF interfaces.

Table 3-5 QSFP0 Signals

Signal	*Direction (Relative to FPGA)*	*FPGA Connectivity*	*Description*
QSFP0_RX_P[3:0]	Input	E-tile transceiver channels.	Differential high speed RX SERDES lanes.
QSFP0_RX_N[3:0]	Input	E-tile transceiver channels.	Differential high speed RX SERDES lanes.
QSFP0_TX_P[3:0]	Output	E-tile transceiver channels.	Differential high speed TX SERDES lanes.
QSFP0_TX_N[3:0]	Output	E-tile transceiver channels.	Differential high speed TX SERDES lanes.
QSFP0_PWR_GOOD	Input	DIFF_3A_14_N	Indicates that the power for the QSFP interface is good.
QSFP0_LPMODE	Output	DIFF_3A_1_N	Module low power mode. Drive 0 by default.

QSPF0_RESET_L	Output	DIFF_3A_1_P	Module active low reset. Drive high by default.
QSFP0_MODSEL_L	Output	DIFF_3A_3_P	Module mode select. Vendor specific. Drive high by default.
QSFP0_MODPRS_L	Input	DIFF_3A_4_P	Module present indication. Active low.
QSFP0_PWR_EN	Output	DIFF_3A_5_N	Power enable for QSFP0. Drive high for active modules.
QSFP0_INT_L	Input	DIFF_3A_3_N	Module interrupt input.
QSFP0_SDA	Inout	DIFF_3A_2_N	Module I2C data line.
QSFP0_SCL	Inout	DIFF_3A_2_P	Module I2C clock line.

Table 3-6 QSFP1 Signals

Signal	***Direction (Relative to FPGA)***	***FPGA Connectivity***	***Description***
QSFP1_RX_P[3:0]	Input	E-tile transceiver channels.	Differential high speed RX SERDES lanes.
QSFP1_RX_N[3:0]	Input	E-tile transceiver channels.	Differential high speed RX SERDES lanes.
QSFP1_TX_P[3:0]	Output	E-tile transceiver channels.	Differential high speed TX SERDES lanes.
QSFP1_TX_N[3:0]	Output	E-tile transceiver channels.	Differential high speed TX SERDES lanes.
QSFP1_PWR_GOOD	Input	DIFF_3A_14_P	Indicates that the power for the QSFP interface is good.
QSFP1_LPMODE	Output	DIFF_3A_7_N	Module low power mode. Drive 0 by default.
QSPF1_RESET_L	Output	DIFF_3A_8_P	Module active low reset. Drive high by default.
QSFP1_MODSEL_L	Output	DIFF_3A_5_P	Module mode select. Vendor specific. Drive high by default.
QSFP1_MODPRS_L	Input	DIFF_3A_6_N	Module present indication. Active low.
QSFP1_PWR_EN	Output	DIFF_3A_7_P	Power enable for QSFP0. Drive high for active modules.
QSFP1_INT_L	Input	DIFF_3A_8_N	Module interrupt input.
QSFP1_SDA	Inout	DIFF_3A_4_N	Module I2C data line.
QSFP1_SCL	Inout	DIFF_3A_6_P	Module I2C clock line.

3.4 FPGA SDM, QSPI, JTAG and Associated

The below diagram shows the simplified connectivity specific to the configuration of the FPGA:

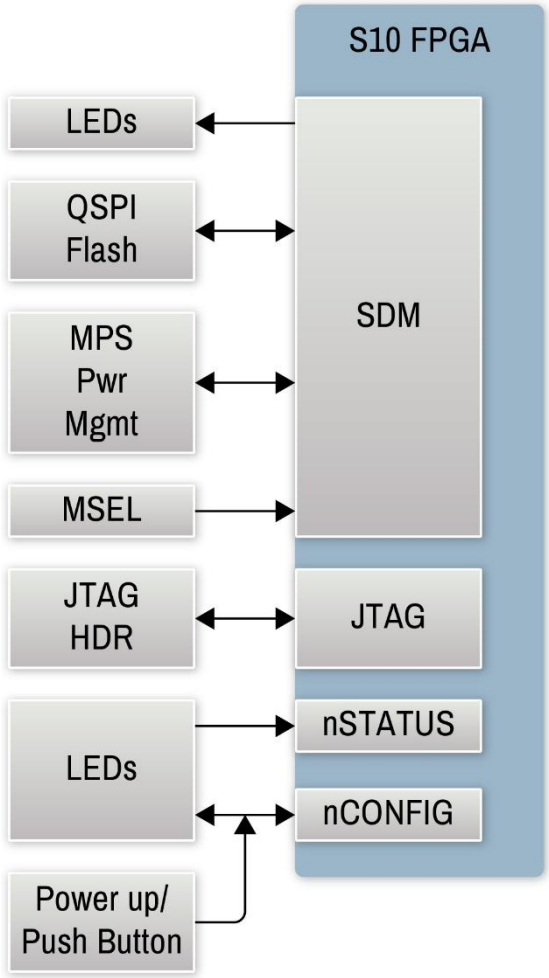


Figure 3-9 FPGA Configuration Connectivity

3.4.1 SDM

The Stratix 10 FPGA has a built-in secure device manager (SDM) that is used to configure the FPGA as well as perform other management services for the FPGA. This SDM connects to the QSPI Flash used to store FPGA configuration images as well as other devices on the board. More details on the SDM can be found at this link: Stratix 10 Configuration User Guide. The SDM pins on the FPGA can be configured in different ways depending on board connectivity and desired options. The kit SDM connections will be described. Also the other configuration pins on the FPGA will be detailed.

The below table lists the FPGA SDM pins, their functionality, and how they are provisioned on the board:

Table 3-7 FPGA SDM Connectivity

SDM Pin	*Functionality*	*Connectivity*	*Description*
SDM_IO0	FPGA_INIT_DONE	Status LED	This signal asserts when the FPGA has entered user mode after a successful configuration. The LED illuminates when FPGA_INIT_DONE asserts.
SDM_IO1	CFG_SPI_SDIO1	DQ1 on QSPI Flash	Data pin 1 on FPGA configuration QSPI flash device.
SDM_IO2	CFG_SPI_SCK	SCK on QSPI Flash	Clock pin on the FPGA configuration QSPI flash device.
SDM_IO3	CFG_SPI_SDIO2	DQ2 on QSPI Flash	Data pin 2 on the FPGA configuration QSPI flash device.
SDM_IO4	CFG_SPI_SDIO0	DQ0 on QSPI Flash	Data pin 0 on the FPGA configuration QSPI flash device.
SDM_IO5	CFG_SPI_CS0N_MSEL0	CS* on QSPI Flash/MSEL0 Pullup resistor.	Chip select pin on the FPGA configuration QSPI flash device. Also used for mode select 0. The FPGA samples the mode pins at power up to determine configuration mode. Default board settings are for AS Normal Mode.
SDM_IO6	CFG_SPI_SDIO3	DQ3 on QSPI Flash	Data pin 3 on the FPGA configuration QSPI flash device.
SDM_IO7	FPGA_MSEL1	MSEL1 Pullup resistor.	Mode select 1. The FPGA samples the mode pins at power up to determine configuration mode. Default board settings are for AS Normal Mode.
SDM_IO8	N/C	No Connection	
SDM_IO9	FPGA_MSEL2	MSEL2 Pulldown resistor.	Mode select 2. The FPGA samples the mode pins at power up to determine configuration mode. Default board settings are for AS Normal Mode.
SDM_IO10	N/C	No Connection	
SDM_IO11	PWRMGT_SDA	PMBus data line on MPS power management device.	Connects to the MPS power management device that controls the core voltage of the FPGA via the Smart VID power functionality.

SDM_IO12	PWRMGT_ALERT_L	Alert Signal on MPS power management device.	Alert pin sourced from the MPS power management device that controls the core voltage of the FPGA via the Smart VID power functionality.
SDM_IO13	N/C	No Connection	
SDM_IO14	PWRMGT_SCL	PMBus clock line on MPS power management device.	Connects to the MPS power management device that controls the core voltage of the FPGA via the Smart VID power functionality.
SDM_IO15	N/C	No Connection	
SDM_IO16	FPGA_CONFIG_DONE	Status LED	This signal asserts to indicate the FPGA received the bitstream successfully.
nCONFIG	FPGA_NCONFIG_L	Connected to power sequencing logic as well as a status LED.	This signal is used to initiate an FPGA configuration. It is connected to power sequencing logic such that the FPGA is powered up before a configuration request is asserted. The
nSTATUS	FPGA_NSTATUS_L	LED	signal is also connected to an LED for status purposes. This signal indicates status associated with FPGA configuration. See the linked Altera documentation for more details.

3.4.2 QSPI

There is a 512Mb QSPI flash device (MT25QU512) that is used to store FPGA configuration images. The below diagram shows the connectivity of the flash device:

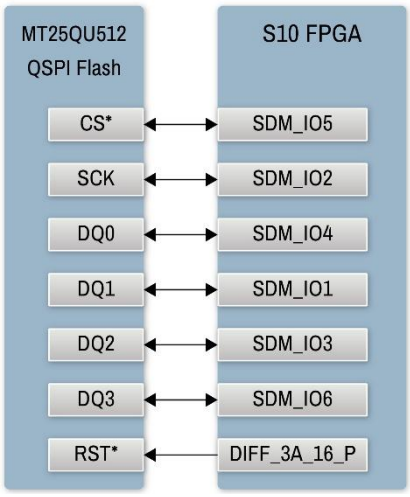


Figure 3-10 QSPI Flash Connectivity

The FPGA's Secure Device Manager is the main interface between the FPGA and the QSPI flash. It handles all of the communication needed to write images to the flash as well as configure the FPGA from the flash. There is a reset signal that is routed to the FPGA in case there is a need to hold the flash in reset by the FPGA.

3.4.3 JTAG

There is a 10-pin JTAG header on the board. This header provides a JTAG interface to the FPGA and can be used for direct programming of it and/or the attached QSPI flash using the Altera Quartus programming tool. See #1 in **Figure 2-1**.

This header is provisioned as such:

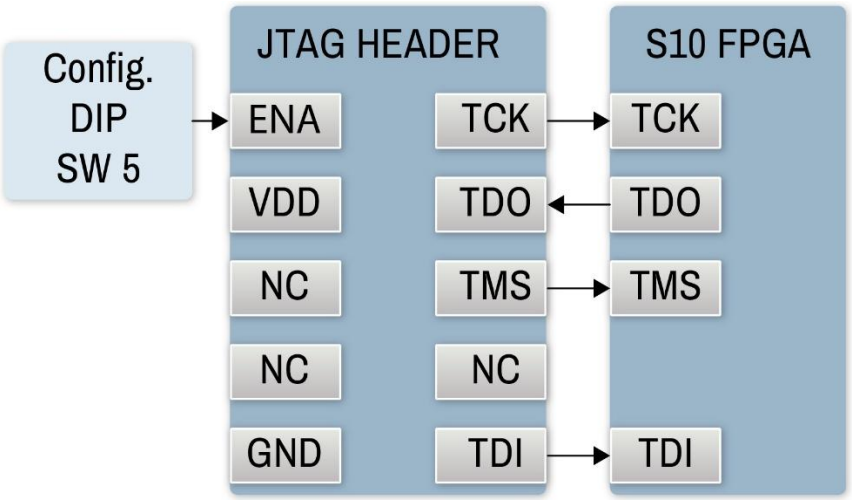


Figure 3-11 JTAG Header Connectivity

See Table 2-1 for the default setting for the ENA pin.

3.4.4 MSEL

The mode select pins on the FPGA SDM determine the configuration mode that is used when the FPGA power ups. These pins are sampled at the power up of the FPGA. On the Board, these MSEL pins are connected to pullup/pulldown resistors to implement MSEL mode: 011, AS normal mode. See Stratix 10 Configuration User Guide for more information on these signals. There is no need to change these settings for normal operation.

3.5 FPGA EEPROM

There is an EEPROM connected to the FPGA. This EEPROM can be used to store non-volatile information that the FPGA might need. As an example, Ethernet MAC addresses can be stored on the EEPROM, read in as part of the FPGA bringup, and then used in Ethernet packet forming.

The connectivity of the EEPROM is shown below:

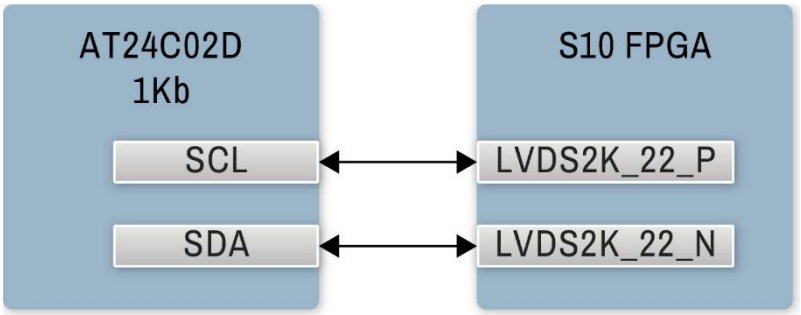


Figure 3-12 FPGA EEPROM Connectivity

3.6 User LEDs

There are 2 LEDs connected to the FPGA for use as general purpose signaling. There is also an LED labeled HRTBT that is intended to be used as a "heartbeat" status, or an indication that the FPGA is functioning. See #12 in Figure 2-1.

The connectivity of the user LEDs is shown in the table below:

Table 3-8 User DIP Switch Connectivity

LED Name	*FPGA Connectivity*	*Description*
DBG0	DIFF_3D_11_N	General purpose status LED.
DBG1	DIFF_3D_6_P	General purpose status LED.
HRTBT	DIFF_3A_17_P	Heartbeat LED. Or can be used as general purpose LED.

3.7 User Header

There is a 2x15 pin header on the board that has direct connectivity to the FPGA. There is also another 2 pin header adjacent to the 2x15 pin header that adds an additional debug pin for a total of 16 user

connections. See #2 in Table 2-1. The top row pins are connected to the FPGA and the bottom row are connected to GND.

The following table describes the connectivity to the FPGA. For reference, pin number 1 is the upper left-most pin.

Table 3-9 User Header Connectivity

Connector	*Header Pin*	*FPGA Connectivity*	*Description*
J14	2	LVDS2K_2_N	General Purpose debug header pin.
J14	4	LVDS2K_2_P	General Purpose debug header pin.
J14	6	LVDS2K_4_N	General Purpose debug header pin.
J14	8	LVDS2K_4_P	General Purpose debug header pin.
J14	10	LVDS2K_1_N	General Purpose debug header pin.
J14	12	LVDS2K_1_P	General Purpose debug header pin.
J14	14	LVDS2K_3_N	General Purpose debug header pin.
J14	16	LVDS2K_6_N	General Purpose debug header pin.
J14	18	LVDS2K_6_P	General Purpose debug header pin.
J14	20	LVDS2K_5_N	General Purpose debug header pin.
J14	22	LVDS2K_5_P	General Purpose debug header pin.
J14	24	LVDS2K_3_P	General Purpose debug header pin.
J14	26	LVDS2K_8_N	General Purpose debug header pin.
J14	28	LVDS2K_8_P	General Purpose debug header pin.
J14	30	LVDS2K_16_P	General Purpose debug header pin.
J68	2	LVDS2K_16_N	General Purpose debug header pin.

■ I2C Connectivity

The following figure shows the I2C connectivity to devices on the board. For the most part, devices that communicate over I2C, have a dedicated set of signals connected to the FPGA. Also, most the I2C connected devices have an associated debug header that can be used with an Aardvark or similar 3rd party I2C communication device. Except for the SDM-connected MPS power management IC, each I2C debug header has a voltage translator inline to change the 3.3V debug header voltage to the 1.8V

needed to communicate to the device. The MPS power management device has a native 3.3V PMBus interface so the voltage translator is in between the FPGA and the IC.
The voltage translator circuits all have enable signals. Most of the enable signals are driven by the FPGA. The MPS power management device's voltage translation enable signal is driven by a DIP SW. See #11 in **Figure 2-1**.

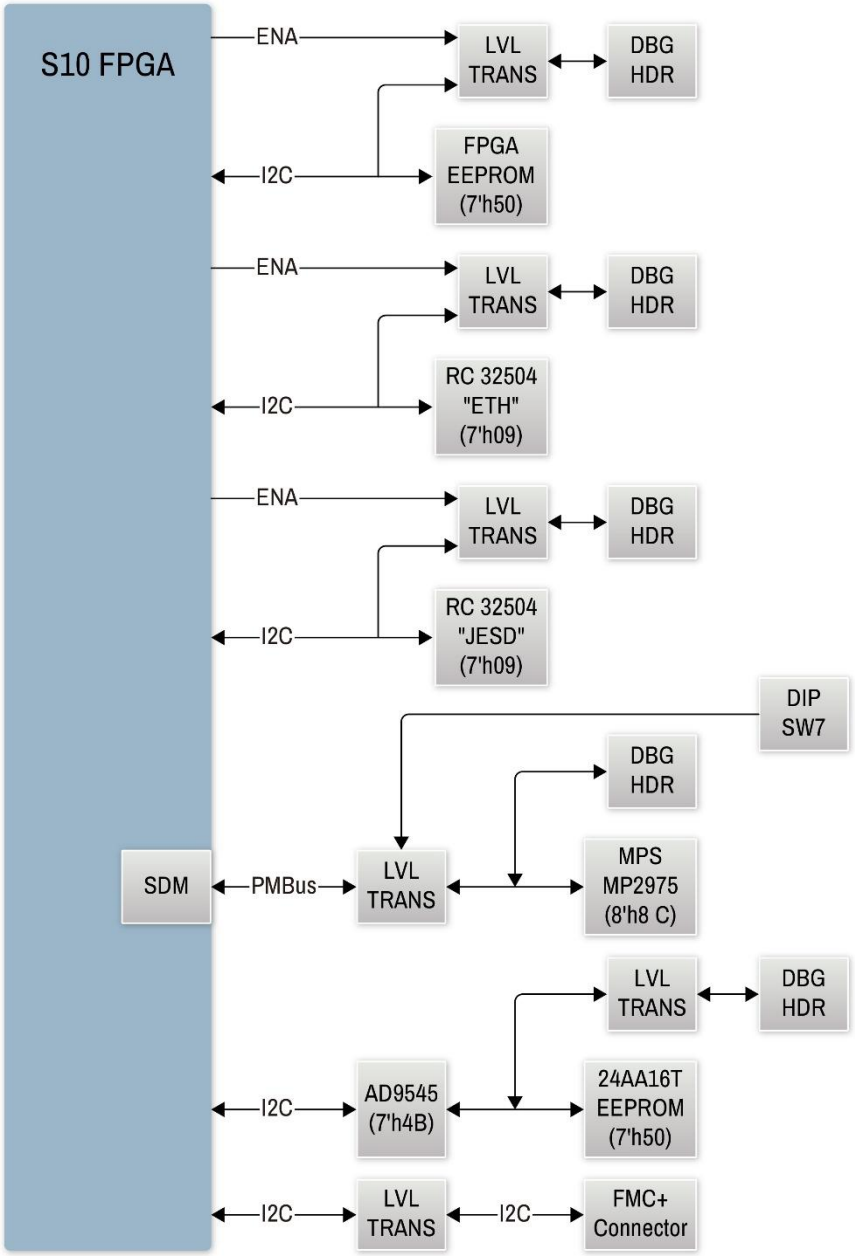


Figure 3-13 I2C Connectivity

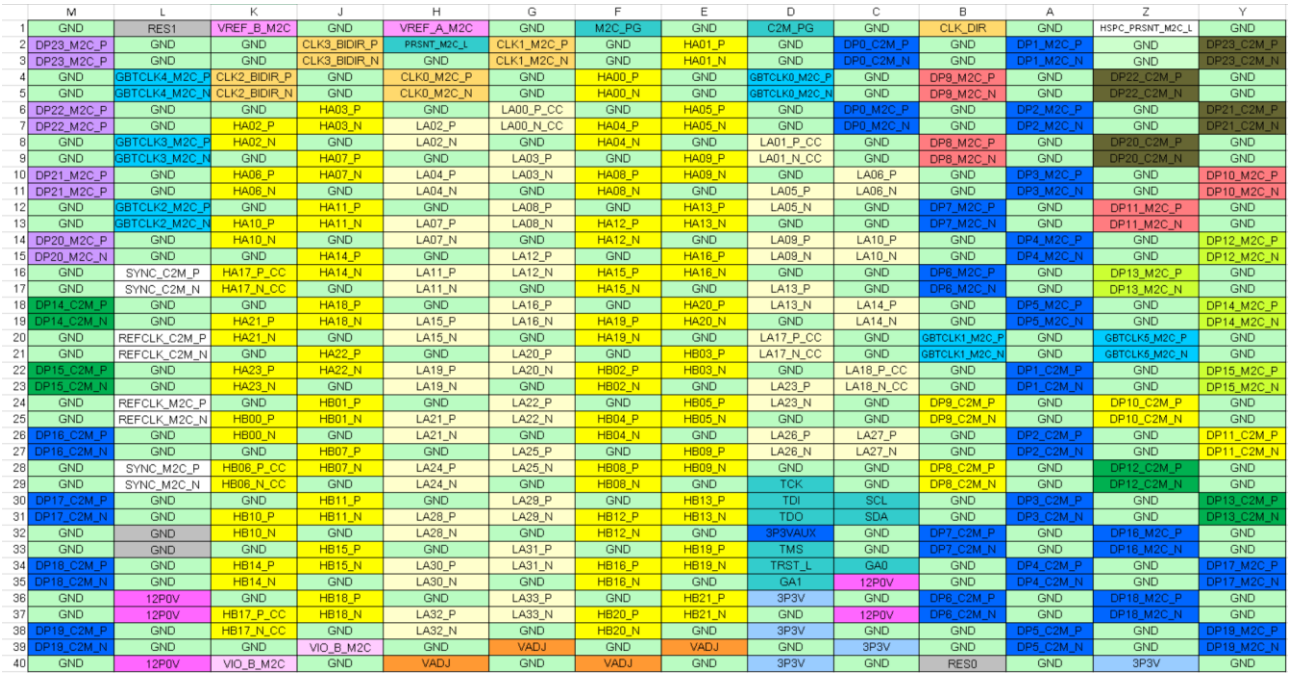
Table 3-10 User Header Connectivity

FPGA Signal	*FPGA Pin*	*Description*

FPGA_EEPROM_I2C_LVL_EN	DIFF_3A_20_P	Enable signal for the FPGA EEPROM debug I2C voltage translator. Set to a 1 to enable the ability to use the debug header for this I2C interface.
FPGA_EEPROM_SDA	LVDS2K_22_N	I2C data line for the FPGA EEPROM.
FPGA_EEPROM_SCL	LVDS2K_22_P	I2C clock line for the FPGA EEPROM.
ETH_RC32504_I2C_LVL_EN	DIFF_3A_21_P	Enable signal for the “ETH” RC32504 debug I2C voltage translator. Set to a 1 to enable the ability to use the debug header for this I2C interface.
RC32504_ETH_SDA	LVDS3B_8_N	I2C data line for the “ETH” RC32504.
RC32504_ETH_SCL	LVDS3B_6_N	I2C clock line for the “ETH” RC32504.
JESD_RC32504_I2C_LVL_EN	DIFF_3A_22_N	Enable signal for the “JESD” RC32504 debug I2C voltage translator. Set to a 1 to enable the ability to use the debug header for this I2C interface.
RC32504_JESD_SDA	LVDS3B_4_P	I2C data line for the “JESD” RC32504.
RC32504_JESD_SCL	LVDS3B_2_P	I2C clock line for the “JESD” RC32504.
AD9545 SCK	LVDS3B_14_N	I2C clock line for the AD9545 IC.
AD9545_SDA	LVDS3B_1_P	I2C data line for the AD9545 IC.
PWRMGT_SCL	SDM_IO14	PMBus clock line for the MPS power management device.
PWRMGT_SDA	SDM_IO11	PMBus data line for the MPS power management device.
FMC_I2C_SDA	LVDS2N_16_N	FMC+ connector’s I2C data line.
FMC_I2C_SCL	LVDS2N_16_P	FMC+ connector’s I2C clock line.
FMC_I2C_LVL_EN	DIFF_3A_22_P	Enable signal for the voltage translator that changes the FPGA I2C 1.8V to the 3.3V FMC standard. Must be driven high to use the FMC+ I2C interface.

3.8 FMC+ Connectivity

The FMC+ interface is an industry-defined high pin count connector that is used to bridge communication between FPGAs and devices on FMC-attached boards. On the Board, the FMC+ interface is intended to allow connection to sensor evaluation boards as well as other 3rd party platforms that need communication to an FPGA device (ie QSFP ethernet plug in cards).
The signals defined on the FMC+ connector are shown below:



	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	M2C_PG	GND	C2M_PG	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_P	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_P	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_P	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP8_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP8_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00_P	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	GND	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP18_M2C_P	GND
33	GND	GND	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP18_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND

Figure 3-14 FMC+ Connector Signals

- Consult the specification for details about the signals, but in general there are:
-

- High Speed Serial lanes designed to interface to FPGA SERDES/transceivers.
- High Speed Serial clock lanes designed to carry reference clocks for SERDES interfaces/transceivers.
- Groups of signal pairs intended to interface to FPGA either single-ended or differentially.
- Reference clocks pairs.
- Status and miscellaneous signals.
- Power and related signals.

-

3.8.1 User Defined Signals

■ Bank A Low Pin Count Signals (LA)

The following table describes the connectivity of the LA signals on the FMC+ connector. There are 34 pairs of signals defined, and all are routed to the FPGA, specifically banks 2M and 2N:

Table 3-11 LA Signal Connectivity

FMC Signal	*FPGA Connectivity*	*Description*
LA00_CC_P	LVDS2M_12_P/CLK_2M_1_P	General purpose IO. Also clock capable input on FPGA.
LA00_CC_N	LVDS2M_12_N/CLK_2M_1_N	General purpose IO. Also clock capable input on FPGA.

LA01_CC_P	LVDS2M_21_P	General purpose IO.
LA01_CC_N	LVDS2M_21_N	General purpose IO.
LA02_P	LVDS2M_22_P	General purpose IO.
LA02_N	LVDS2M_22_N	General purpose IO.
LA03_P	LVDS2M_10_P	General purpose IO.
LA03_N	LVDS2M_10_N	General purpose IO.
LA04_P	LVDS2M_19_P	General purpose IO.
LA04_N	LVDS2M_19_N	General purpose IO.
LA05_P	LVDS2M_8_P	General purpose IO.
LA05_N	LVDS2M_8_N	General purpose IO.
LA06_P	LVDS2M_18_P	General purpose IO.
LA06_N	LVDS2M_18_N	General purpose IO.
LA07_P	LVDS2M_15_P	General purpose IO.
LA07_N	LVDS2M_15_N	General purpose IO.
LA08_P	LVDS2M_9_P	General purpose IO.
LA08_N	LVDS2M_9_N	General purpose IO.
LA09_P	LVDS2M_5_P	General purpose IO.
LA09_N	LVDS2M_5_N	General purpose IO.
LA10_P	LVDS2M_16_P	General purpose IO.
LA10_N	LVDS2M_16_N	General purpose IO.
LA11_P	LVDS2M_14_P	General purpose IO.
LA11_N	LVDS2M_14_N	General purpose IO.
LA12_P	LVDS2M_7_P	General purpose IO.
LA12_N	LVDS2M_7_N	General purpose IO.
LA13_P	LVDS2M_3_P	General purpose IO.
LA13_N	LVDS2M_3_N	General purpose IO.
LA14_P	LVDS2M_6_P	General purpose IO.
LA14_N	LVDS2M_6_N	General purpose IO.
LA15_P	LVDS2M_1_P	General purpose IO.
LA15_N	LVDS2M_1_N	General purpose IO.
LA16_P	LVDS2M_17_P	General purpose IO.
LA16_N	LVDS2M_17_N	General purpose IO.
LA17_CC_P	LVDS2N_12_P/CLK_2N_1_P	General purpose IO. Also clock capable input on FPGA.
LA17_CC_N	LVDS2N_12_N/CLK_2N_1_N	General purpose IO. Also clock capable input on FPGA.
LA18_CC_P	LVDS2N_4_P	General purpose IO.
LA18_CC_N	LVDS2N_4_N	General purpose IO.
LA19_P	LVDS2N_6_P	General purpose IO.
LA19_N	LVDS2N_6_N	General purpose IO.
LA20_P	LVDS2N_2_P	General purpose IO.
LA20_N	LVDS2N_2_N	General purpose IO.
LA21_P	LVDS2N_3_P	General purpose IO.
LA21_N	LVDS2N_3_N	General purpose IO.
LA22_P	LVDS2N_24_P	General purpose IO.
LA22_N	LVDS2N_24_N	General purpose IO.

LA23_P	LVDS2N_1_P	General purpose IO.
LA23_N	LVDS2N_1_N	General purpose IO.
LA24_P	LVDS2N_9_P	General purpose IO.
LA24_N	LVDS2N_9_N	General purpose IO.
LA25_P	LVDS2N_20_P	General purpose IO.
LA25_N	LVDS2N_20_N	General purpose IO.
LA26_P	LVDS2N_5_P	General purpose IO.
LA26_N	LVDS2N_5_N	General purpose IO.
LA27_P	LVDS2N_10_P	General purpose IO.
LA27_N	LVDS2N_10_N	General purpose IO.
LA28_P	LVDS2N_14_P	General purpose IO.
LA28_N	LVDS2N_14_N	General purpose IO.
LA29_P	LVDS2N_8_P	General purpose IO.
LA29_N	LVDS2N_8_N	General purpose IO.
LA30_P	LVDS2N_22_P	General purpose IO.
LA30_N	LVDS2N_22_N	General purpose IO.
LA31_P	LVDS2N_19_P	General purpose IO.
LA31_N	LVDS2N_19_N	General purpose IO.
LA32_P	LVDS2N_15_P	General purpose IO.
LA32_N	LVDS2N_15_N	General purpose IO.
LA33_P	LVDS2N_21_P	General purpose IO.
LA33_N	LVDS2N_21_N	General purpose IO.

■ Bank A High Pin Count Signals (HA)

The following table describes the connectivity of the HA signals on the FMC+ connector. There are 24 pairs of signals defined, and all are routed to the FPGA, specifically bank 2L. One pair of signals, HA23_P/N is routed to bank 2M due to IO limitations on the FPGA 2L bank:

Table 3-12 HA Signal Connectivity

FMC Signal	*FPGA Connectivity*	*Description*
HA00_CC_P	LVDS2L_13_P/CLK_2L_1_P	General purpose IO. Also clock capable input on FPGA.
HA00_CC_N	LVDS2L_13_N/CLK_2L_1_N	General purpose IO. Also clock capable input on FPGA.
HA01_CC_P	LVDS2L_22_P	General purpose IO.
HA01_CC_N	LVDS2L_22_N	General purpose IO.
HA02_P	LVDS2L_15_P	General purpose IO.
HA02_N	LVDS2L_15_N	General purpose IO.
HA03_P	LVDS2L_17_P	General purpose IO.
HA03_N	LVDS2L_17_N	General purpose IO.
HA04_P	LVDS2L_18_P	General purpose IO.
HA04_N	LVDS2L_18_N	General purpose IO.
HA05_P	LVDS2L_19_P	General purpose IO.

HA05_N	LVDS2L_19_N	General purpose IO.
HA06_P	LVDS2L_16_P	General purpose IO.
HA06_N	LVDS2L_16_N	General purpose IO.
HA07_P	LVDS2L_21_P	General purpose IO.
HA07_N	LVDS2L_21_N	General purpose IO.
HA08_P	LVDS2L_20_P	General purpose IO.
HA08_N	LVDS2L_20_N	General purpose IO.
HA09_P	LVDS2L_24_P	General purpose IO.
HA09_N	LVDS2L_24_N	General purpose IO.
HA10_P	LVDS2L_9_P	General purpose IO.
HA10_N	LVDS2L_9_N	General purpose IO.
HA11_P	LVDS2L_23_P	General purpose IO.
HA11_N	LVDS2L_23_N	General purpose IO.
HA12_P	LVDS2L_10_P	General purpose IO.
HA12_N	LVDS2L_10_N	General purpose IO.
HA13_P	LVDS2L_14_P	General purpose IO.
HA13_N	LVDS2L_14_N	General purpose IO.
HA14_P	LVDS2L_8_P	General purpose IO.
HA14_N	LVDS2L_8_N	General purpose IO.
HA15_P	LVDS2L_4_P	General purpose IO.
HA15_N	LVDS2L_4_N	General purpose IO.
HA16_P	LVDS2L_7_P	General purpose IO.
HA16_N	LVDS2L_7_N	General purpose IO.
HA17_CC_P	LVDS2L_12_P/CLK_2L_1_P	General purpose IO. Also clock capable input on FPGA.
HA17_CC_N	LVDS2L_12_N/CLK_2L_1_N	General purpose IO. Also clock capable input on FPGA.
HA18_P	LVDS2L_3_P	General purpose IO.
HA18_N	LVDS2L_3_N	General purpose IO.
HA19_P	LVDS2L_6_P	General purpose IO.
HA19_N	LVDS2L_6_N	General purpose IO.
HA20_P	LVDS2L_2_P	General purpose IO.
HA20_N	LVDS2L_2_N	General purpose IO.
HA21_P	LVDS2L_5_P	General purpose IO.
HA21_N	LVDS2L_5_N	General purpose IO.
HA22_P	LVDS2L_1_P	General purpose IO.
HA22_N	LVDS2L_1_N	General purpose IO.
HA23_P	LVDS2M_2_P	General purpose IO.
HA23_N	LVDS2M_2_N	General purpose IO.

■ Bank B High Pin Count Signals (HB)

The following table describes the connectivity of the HA signals on the FMC+ connector. There are 22 pairs of signals defined, and all are routed to the FPGA, specifically bank 3C.

Table 3-13 HA Signal Connectivity

FMC Signal	*FPGA Connectivity*	*Description*
HB00_CC_P	LVDS3C_13_P/CLK_3C_0_P	General purpose IO. Also clock capable input on FPGA.
HB00_CC_N	LVDS3C_13_N/CLK_3C_0_N	General purpose IO. Also clock capable input on FPGA.
HB01_P	LVDS3C_6_P	General purpose IO.
HB01_N	LVDS3C_6_N	General purpose IO.
HB02_P	LVDS3C_5_P	General purpose IO.
HB02_N	LVDS3C_5_N	General purpose IO.
HB03_P	LVDS3C_3_P	General purpose IO.
HB03_N	LVDS3C_3_N	General purpose IO.
HB04_P	LVDS3C_1_P	General purpose IO.
HB04_N	LVDS3C_1_N	General purpose IO.
HB05_P	LVDS3C_4_P	General purpose IO.
HB05_N	LVDS3C_4_N	General purpose IO.
HB06_CC_P	LVDS3C_2_P	General purpose IO.
HB06_CC_N	LVDS3C_2_N	General purpose IO.
HB07_P	LVDS3C_7_P	General purpose IO.
HB07_N	LVDS3C_7_N	General purpose IO.
HB08_P	LVDS3C_9_P	General purpose IO.
HB08_N	LVDS3C_9_N	General purpose IO.
HB09_P	LVDS3C_17_P	General purpose IO.
HB09_N	LVDS3C_17_N	General purpose IO.
HB10_P	LVDS3C_10_P	General purpose IO.
HB10_N	LVDS3C_10_N	General purpose IO.
HB11_P	LVDS3C_8_P	General purpose IO.
HB11_N	LVDS3C_8_N	General purpose IO.
HB12_P	LVDS3C_18_P	General purpose IO.
HB12_N	LVDS3C_18_N	General purpose IO.
HB13_P	LVDS3C_15_P	General purpose IO.
HB13_N	LVDS3C_15_N	General purpose IO.
HB14_P	LVDS3C_14_P	General purpose IO.
HB14_N	LVDS3C_14_N	General purpose IO.
HB15_P	LVDS3C_23_P	General purpose IO.
HB15_N	LVDS3C_23_N	General purpose IO.
HB16_P	LVDS3C_19_P	General purpose IO.
HB16_N	LVDS3C_19_N	General purpose IO.
HB17_CC_P	LVDS3C_12_P/CLK_3C_1_P	General purpose IO. Also clock capable input on FPGA.
HB17_CC_N	LVDS3C_12_N/CLK_3C_1_N	General purpose IO. Also clock capable input on FPGA.
HB18_P	LVDS3C_16_P	General purpose IO.
HB18_N	LVDS3C_16_N	General purpose IO.

HB19_P	LVDS3C_21_P	General purpose IO.
HB19_N	LVDS3C_21_N	General purpose IO.
HB20_P	LVDS3C_20_P	General purpose IO.
HB20_N	LVDS3C_20_N	General purpose IO.
HB21_P	LVDS3C_22_P	General purpose IO.
HB21_N	LVDS3C_22_N	General purpose IO.

■ Gigabit Interface Signals

The following table describes the connectivity of the gigabit signal pairs and the associated clocks. There are 16 out 32 high-speed lanes routed to the FPGA:

Table 3-14 Gigabit Signal Connectivity

FMC Signal	*FPGA Connectivity*	*Description*
DP0_M2C_P	GXEL8A_CH6_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP0_M2C_N	GXEL8A_CH6_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP1_M2C_P	GXEL8A_CH7_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP1_M2C_N	GXEL8A_CH7_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP2_M2C_P	GXEL8A_CH8_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP2_M2C_N	GXEL8A_CH8_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP3_M2C_P	GXEL8A_CH9_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP3_M2C_N	GXEL8A_CH9_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.

DP4_M2C_P	GXEL8A_CH10_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP4_M2C_N	GXEL8A_CH10_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP5_M2C_P	GXEL8A_CH11_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP5_M2C_N	GXEL8A_CH11_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP6_M2C_P	GXEL8A_CH12_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP6_M2C_N	GXEL8A_CH12_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP7_M2C_P	GXEL8A_CH13_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP7_M2C_N	GXEL8A_CH13_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP8_M2C_P	GXEL8A_CH14_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP8_M2C_N	GXEL8A_CH14_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP9_M2C_P	GXEL8A_CH15_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP9_M2C_N	GXEL8A_CH15_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output

		from the FMC to the FPGA.
DP10_M2C_P	GXEL8A_CH16_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes “Meazzanine to Carrier” so this signal is an output from the FMC to the FPGA.
DP10_M2C_N	GXEL8A_CH16_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes “Meazzanine to Carrier” so this signal is an output from the FMC to the FPGA.
DP11_M2C_P	GXEL8A_CH17_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes “Meazzanine to Carrier” so this signal is an output from the FMC to the FPGA.
DP11_M2C_N	GXEL8A_CH17_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes “Meazzanine to Carrier” so this signal is an output from the FMC to the FPGA.
DP12_M2C_P	GXEL8A_CH4_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes “Meazzanine to Carrier” so this signal is an output from the FMC to the FPGA.
DP12_M2C_N	GXEL8A_CH4_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes “Meazzanine to Carrier” so this signal is an output from the FMC to the FPGA.
DP13_M2C_P	GXEL8A_CH5_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes “Meazzanine to Carrier” so this signal is an output from the FMC to the FPGA.
DP13_M2C_N	GXEL8A_CH5_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes “Meazzanine to Carrier” so this signal is an output from the FMC to the FPGA.
DP14_M2C_P	GXEL8A_CH18_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes “Meazzanine to Carrier” so this signal is an output from the FMC to the FPGA.
DP14_M2C_N	GXEL8A_CH18_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes “Meazzanine to Carrier” so this signal is an output from the FMC to the FPGA.
DP15_M2C_P	GXEL8A_CH19_RXP	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes “Meazzanine to Carrier” so this signal is an output from the FMC to the FPGA.

DP15_M2C_N	GXEL8A_CH19_RXN	Differential gigabit receive lane. Connects to E-tile transceiver channel. M2C in the name denotes "Meazzanine to Carrier" so this signal is an output from the FMC to the FPGA.
DP0_C2M_P	GXEL8A_CH6_TXP	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes "Carrier to Mezzanine" so this signal is an output from the FPGA to the FMC.
DP0_C2M_N	GXEL8A_CH6_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes "Carrier to Mezzanine" so this signal is an output from the FPGA to the FMC.
DP1_C2M_P	GXEL8A_CH7_TXP	Differential gigabit transmit lane. Connects to E-tile transceiver channel. C2M in the name denotes "Carrier to Mezzanine" so this signal is an output from the FPGA to the FMC.
DP1_C2M_N	GXEL8A_CH7_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes "Carrier to Mezzanine" so this signal is an output from the FPGA to the FMC.
DP2_C2M_P	GXEL8A_CH8_TXP	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes "Carrier to Mezzanine" so this signal is an output from the FPGA to the FMC.
DP2_C2M_N	GXEL8A_CH8_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes "Carrier to Mezzanine" so this signal is an output from the FPGA to the FMC.
DP3_C2M_P	GXEL8A_CH9_TXP	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes "Carrier to Mezzanine" so this signal is an output from the FPGA to the FMC.
DP3_C2M_N	GXEL8A_CH9_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes "Carrier to Mezzanine" so this signal is an output from the FPGA to the FMC.
DP4_C2M_P	GXEL8A_CH10_TXP	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes "Carrier to Mezzanine" so this signal is an output from the FPGA to the FMC.
DP4_C2M_N	GXEL8A_CH10_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes "Carrier to Mezzanine" so this signal is an output from the FPGA to the FMC.
DP5_C2M_P	GXEL8A_CH11_TXP	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes "Carrier to Mezzanine" so this signal is an output

		from the FPGA to the FMC.
DP5_C2M_N	GXEL8A_CH11_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP6_C2M_P	GXEL8A_CH12_TXP	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP6_C2M_N	GXEL8A_CH12_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP7_C2M_P	GXEL8A_CH13_TXP	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP7_C2M_N	GXEL8A_CH13_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP8_C2M_P	GXEL8A_CH14_TXP	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP8_C2M_N	GXEL8A_CH14_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP9_C2M_P	GXEL8A_CH15_TXP	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP9_C2M_N	GXEL8A_CH15_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP10_C2M_P	GXEL8A_CH16_TXP	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP10_C2M_N	GXEL8A_CH16_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.

DP11_C2M_P	GXEL8A_CH17_TXP	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP11_C2M_N	GXEL8A_CH17_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP12_C2M_P	GXEL8A_CH4_TXP	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP12_C2M_N	GXEL8A_CH4_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP13_C2M_P	GXEL8A_CH5_TXP	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP13_C2M_N	GXEL8A_CH5_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP14_C2M_P	GXEL8A_CH18_TXP	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP14_C2M_N	GXEL8A_CH18_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP15_C2M_P	GXEL8A_CH19_TXP	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
DP15_C2M_N	GXEL8A_CH19_TXN	Differential gigabit transmit lane. Connects to E- tile transceiver channel. C2M in the name denotes “Carrier to Mezzanine” so this signal is an output from the FPGA to the FMC.
GBTCLK0_M2C_P	REFCLK_GXEL8A_CH2_P	Differential reference clock for the E-tile transceivers.
GBTCLK0_M2C_N	REFCLK_GXEL8A_CH2_N	Differential reference clock for the E-tile transceivers.
GBTCLK1_M2C_P	REFCLK_GXEL8A_CH3_P	Differential reference clock for the E-tile transceivers.

GBTCLK1_M2C_N	REFCLK_GXEL8A_CH3_P	Differential reference clock for the E-tile transceivers.
GBTCLK2_M2C_P	REFCLK_GXEL8A_CH4_P	Differential reference clock for the E-tile transceivers.
GBTCLK2_M2C_N	REFCLK_GXEL8A_CH4_P	Differential reference clock for the E-tile transceivers.
GBTCLK3_M2C_P	REFCLK_GXEL8A_CH5_P	Differential reference clock for the E-tile transceivers.
GBTCLK3_M2C_N	REFCLK_GXEL8A_CH5_P	Differential reference clock for the E-tile transceivers.

3.8.2 Other FMC Signals

The following table describes other signals that are part of the FMC+ interface:

Table 3-15 Other FMC Signal Connectivity

FMC Signal	*FPGA Connectivity*	*Description*
CLK0_M2C_P	LVDS2M_13_P/CLK_2M_0_P	Differential pairs defined as clock signals, driven from the FMC to the FPGA.
CLK0_M2C_N	LVDS2M_13_N/CLK_2M_0_N	Differential pairs defined as clock signals, driven from the FMC to the FPGA.
CLK1_M2C_P	LVDS2N_13_P/CLK_2N_0_P	Differential pairs defined as clock signals, driven from the FPGA to the FMC.
CLK1_M2C_N	LVDS2N_13_N/CLK_2N_0_N	Differential pairs defined as clock signals, driven from the FPGA to the FMC.
CLK2_BIDIR_P	See FMC Bidirectional Clocks	
CLK2_BIDIR_N	See FMC Bidirectional Clocks	
CLK3_BIDIR_P	See FMC Bidirectional Clocks	
CLK3_BIDIR_N	See FMC Bidirectional Clocks	
REFCLK_C2M_P	LVDS3B_15_P	LVDS reference clock used for synchronization. Driven from the FPGA to the FMC.
REFCLK_C2M_N	LVDS3B_15_N	LVDS reference clock used for synchronization. Driven from the FPGA to the FMC.
REFCLK_M2C_P	LVDS3B_13_P	LVDS reference clock used for synchronization. Driven from the FMC to the FPGA.
REFCLK_M2C_N	LVDS3B_13_N	LVDS reference clock used for synchronization. Driven from the FMC to the FPGA.

SYNC_C2M_P	LVDS2M_4_P	LVDS trigger signal. Driven from the FPGA to the FMC.
SYNC_C2M_N	LVDS2M_4_N	LVDS trigger signal. Driven from the FPGA to the FMC.
SYNC_M2C_P	LVDS2N_18_P	LVDS trigger signal. Driven from the FMC to the FPGA.
SYNC_M2C_N	LVDS2N_18_N	LVDS trigger signal. Driven from the FMC to the FPGA.
CLK_DIR	See FMC Bidirectional Clocks	
GA0	LVDS2N_23_P	Used for I2C addressing on the FMC board. These signals are driven by the FPGA. The usage of these signals is FMC board dependent.
GA1	LVDS2N_23_N	Used for I2C addressing on the FMC board. These signals are driven by the FPGA. The usage of these signals is FMC board dependent.
SDA	LVDS2N_16_N	FMC I2C data line.
SCL	LVDS2N_16_P	FMC I2C clock line.
PG_C2M	LVDS2M_11_N	Power good indicator from the FPGA board to the FMC board. Asserts from the carrier card when power supplies VADJ, 12P0V, 3P3V are within tolerance.
PG_M2C	LVDS2M_20_N	This signal asserts high by the mezzanine module when power supplies VIO_B_M2C, VREF_A_M2C, VREF_B_M2C are within tolerance.
PRSNT_M2C_L	LVDS2M_23_P	Signal used by the FPGA to detect the presence of an FMC board. Driven low by the FMC board.
HSPC_PRSNT_M2C_L	LVDS2M_24_P	Signal used by the FPGA to detect the presence of an FMC+ board. Driven low by the FMC+ board.
TRST_L	N/C	FMC JTAG interface reset. Not connected.
TCK	N/C	FMC JTAG interface TCK. Not connected.
TMS	N/C	FMC JTAG interface TMS. Not connected.
TDI	N/C	FMC JTAG interface TDI. Not

		connected.
TDO	N/C	FMC JTAG interface TDO. Not connected.

3.8.3 FMC Power Connectivity

The below diagram shows the power connectivity to the FMC+ connector:

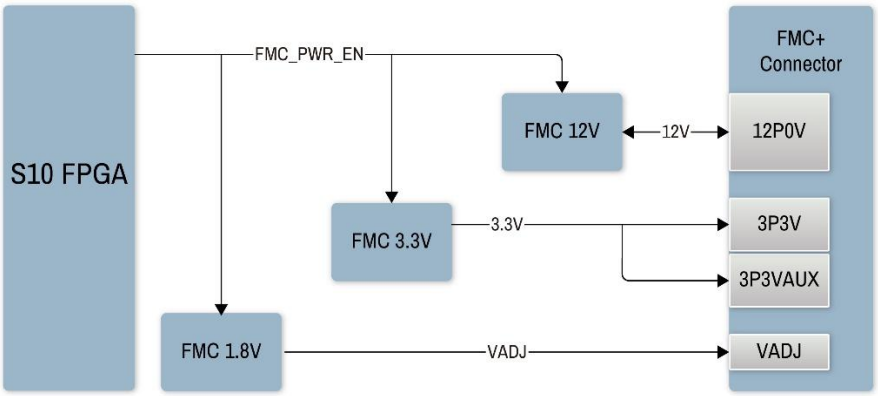


Figure 3-15 FMC+ Power Connectivity

There are three main FMC+ power supplies on the kit: 12V, 3.3V, and 1.8V. Each power supply circuit is enabled by driving the FMC_PWR_EN signal high (DIFF_3A_17_N on the FPGA). In the FMC standard, VADJ has a voltage range of 0 to 3.3V. The P3844 supports 1.8V VADJ, which is a typical voltage that FMC cards support.

Chapter 4

Appendix

4.1 Revision History

Version	*Change Log*
V1.0	**Initial Version**
V1.0.1	**Modify by Team review**

4.2 Copyright Statement