Motor control Discovery kit with STM32G473QE MCU

Introduction

The B-G473E-ZEST1S Discovery kit is a part of the motor-control development platform supporting ZeST and HSO algorithms. B-G473E-ZEST1S is a control board with STM32G473QET6 microcontroller in ZeST Discovery pack and works together with a Power board such as STEVAL-LVLP01, an optional adaptor board such as B-ZEST-ADAPT1, and an accessories package such as B-MOTOR-PMSMA1.

The B-G473E-ZEST1S control board is connected to the power board or adaptor board through an embedded MC connector V2. B-G473E-ZEST1S can also support motor driver expansion boards X-NUCLEO-IHM08M1, X-NUCLEO-IHM09M1, and X-NUCLEO-IHM16M1 via the Morpho MC connector. STLINK-V3EC is integrated into the board, as an embedded in-circuit debugger and programmer for the STM32 MCU and the USB Virtual COM port bridge.

Figure 1. B-G473E-ZEST1S top view

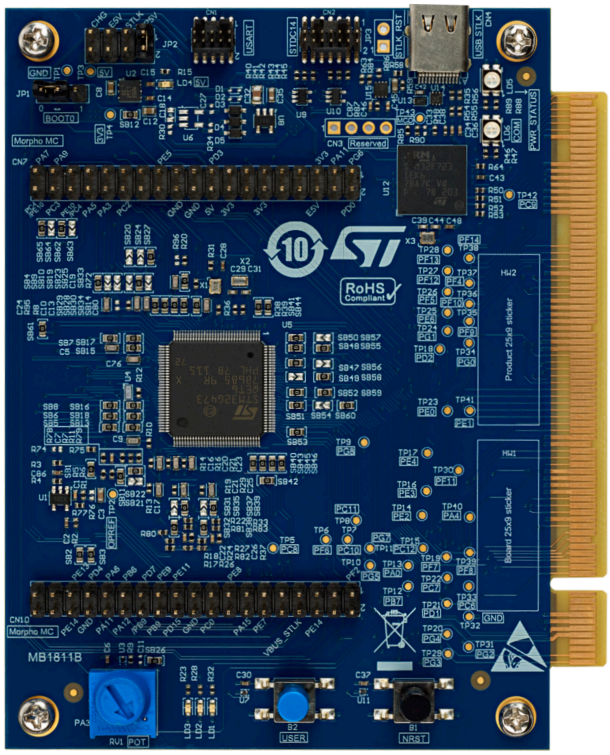
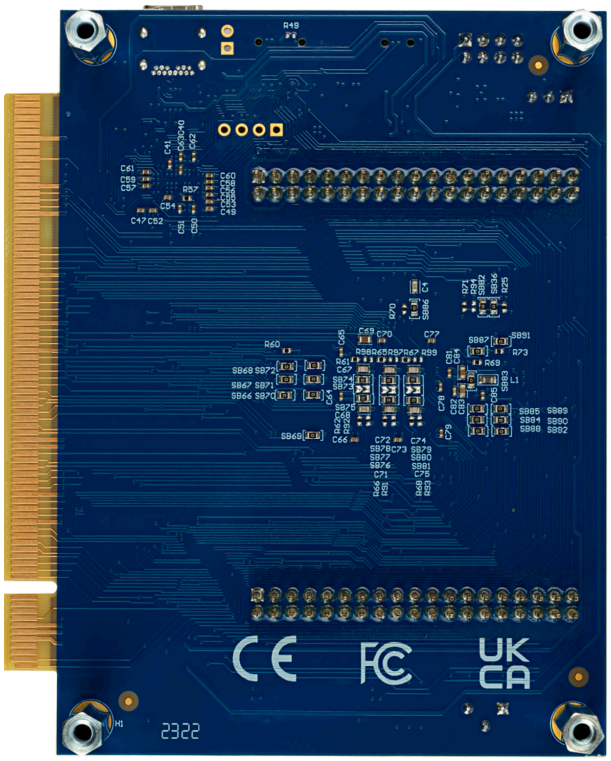


Figure 2. B-G473E-ZEST1S bottom view



Pictures are not contractual.

1 Features

- STM32G473QET6 microcontroller based on the Arm® Cortex®-M4 core, featuring 512 Kbytes of flash memory and 128 Kbytes of SRAM in an LQFP128 package
- Three user LEDs
- User/tamper and reset push-buttons
- Potentiometer for ADC
- Board connectors:
  - MC connector V2
  - Morpho MC
  - STDC14 and USART debug ports
- Flexible power-supply options: 5V from Power board, ST-LINK USB V_{BUS}, or 5V external sources from Morpho MC connector
- On-board STLINK-V3EC debugger/programmer with USB re-enumeration capability: two Virtual COM ports, and debug port
- Comprehensive free software libraries and examples available with the STM32CubeG4 MCU Package
- Support of a wide choice of Integrated Development Environments (IDEs) including IAR Embedded Workbench®, MDK-ARM, and STM32CubeIDE
- Part of STM32 motor control ecosystem with X-CUBE-MCSDK motor project configuration tool

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Ordering information

To order the B-G473E-ZEST1S Discovery kit, refer to Table 1. Additional information is available from the datasheet and reference manual of the target microcontroller.

Table 1. List of available products

Order code	Board reference	Target STM32
B-G473E-ZEST1S	MB1811(1)	STM32G473QET6

1. *Subsequently called main board in the rest of the documentation.*

2.1 Codification

The meaning of the codification is explained in Table 2.

Table 2. Codification explanation

B-XXYYZ-ZEST1S	Description	Example: B-G473E-ZEST1S
B	Discovery kit	Discovery kit
XX	MCU series in STM32 32-bit Arm Cortex MCUs	STM32G4 series
YY	MCU product line in the series	STM32G4x3 product line
Z	STM32 flash memory size: • E for 512 Kbytes	512 Kbytes
-ZEST	Dedicated to application	Control board for ZEST application

3 Development environment

3.1 System requirements

- Multi-OS support: Windows® 10, Linux® 64-bit, or macOS®
- USB Type-A or USB Type-C® to USB Type-C® cable

Note: macOS® is a trademark of Apple Inc., registered in the U.S. and other countries and regions.
Linux® is a registered trademark of Linus Torvalds.
Windows is a trademark of the Microsoft group of companies.

3.2 Development toolchains

- IAR Systems® - IAR Embedded Workbench®(1)
- Keil® - MDK-ARM(1)
- STMicroelectronics - STM32CubeIDE

1. *On Windows® only.*

3.3 Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board microcontroller, is preloaded in the STM32 flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from *www.st.com*.

4 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

Table 3. ON/OFF convention

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Jumper JPx [1-2]	Jumper fitted between Pin 1 and Pin 2
Solder bridge SBx ON	SBx connections closed by 0 Ω resistor
Solder bridge SBx OFF	SBx connections left open
Resistor Rx ON	Resistor soldered
Resistor Rx OFF	Resistor not soldered
Capacitor Cx ON	Capacitor soldered
Capacitor Cx OFF	Capacitor not soldered

5 Quick start

Follow the sequence below to configure the B-G473E-ZEST1S Discovery board and launch the demonstration application (refer to Figure 4 for component location):

1. Check the jumper position on the board (refer to Table 4).
2. For the correct identification of the device interfaces from the host PC and before connecting the board, install the STLINK-V3EC USB driver available on the *www.st.com* website.
3. Connect the B-G473E-ZEST1S Discovery board to a PC with a USB cable (USB Type-A or USB Type-C® to USB Type-C®) through the STLINK-V3EC USB connector (CN4) to power the board.
4. Then, the 5V_PWR green LED (LD4) lights up and the COM LED (LD6) blinks.
5. Download the demonstration software and several software examples that help to use the B-G473E-ZEST1S Discovery board features. These are available on the *www.st.com* website.
6. Develop your application using the available examples.

6 Hardware layout and configuration

6.1 Hardware block diagram

The B-G473E-ZEST1S Discovery board is designed with the STM32G473QET6 target microcontroller. Figure 3 illustrates STM32G473QET6 connections with peripheral components. Figure 4 helps to locate these features on the B-G473E-ZEST1S Discovery board.

Figure 3. Hardware block diagram

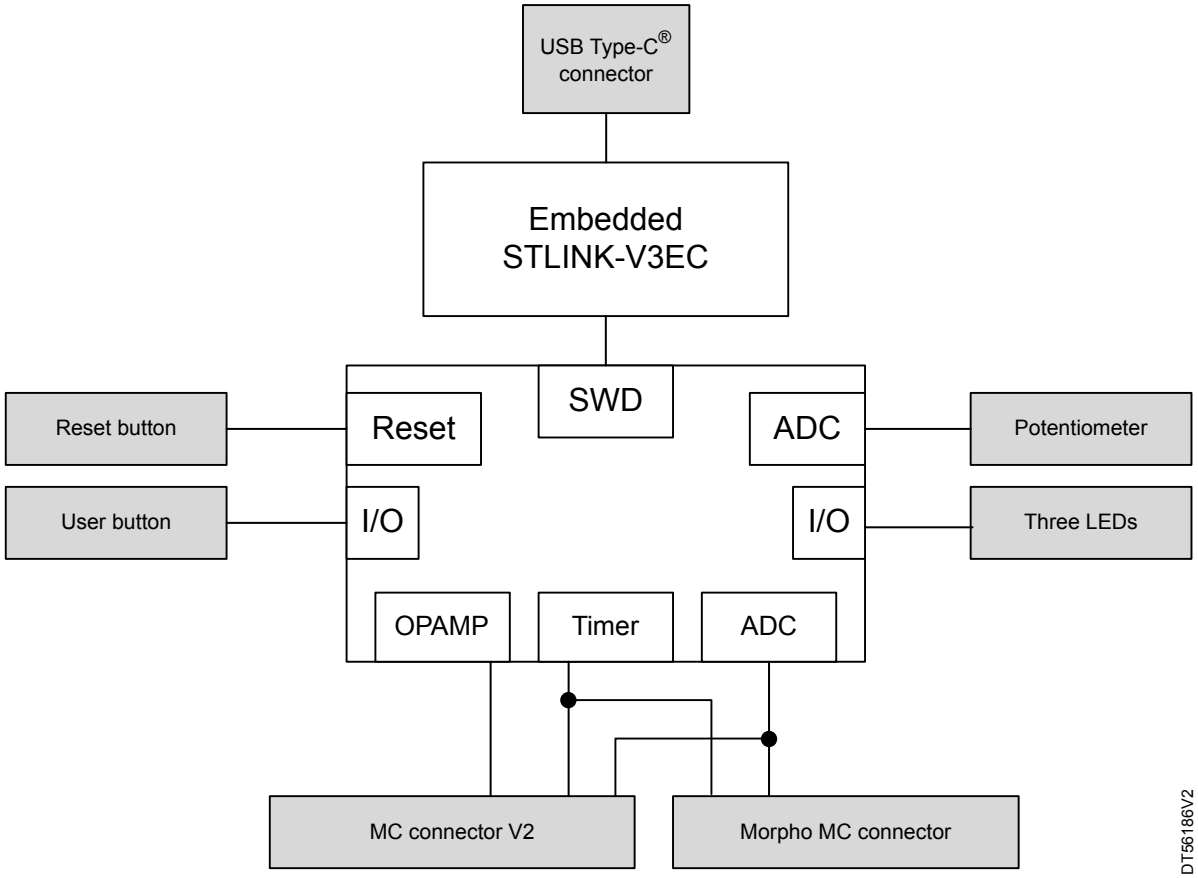
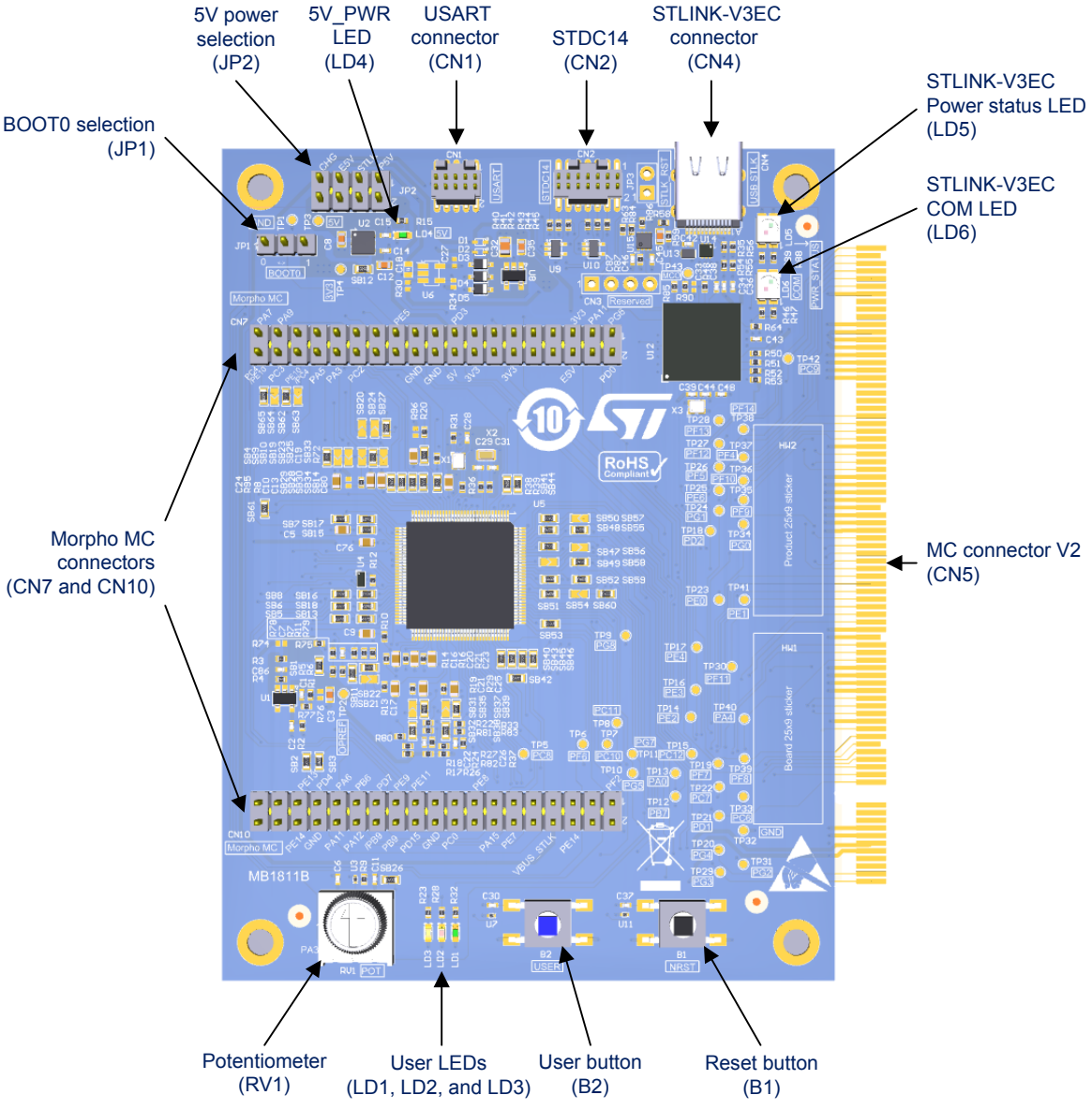


Figure 4. **B-G473E-ZEST1S PCB layout (top view)**



6.2 Default board configuration

Table 4 describes the default jumper setting.

Table 4. **Default jumper setting**

Jumper	Function	Setting	Comment
JP1	BOOT0	**[1-2]**	BOOT0 set to 0
JP2	5V power source selection	**[1-2]**	5V connected to P5V, 5V from power board

6.3 Embedded STLINK-V3EC

6.3.1 Description

There are two different ways to program and debug the on-board STM32 MCU:

1. Using the embedded STLINK-V3EC
2. Using an external debug tool connected to the STDC14/MIPI10 connector (CN2) and USART connector (CN1) for the second USART VCP

The STLINK-V3EC facility for debugging and flashing is integrated into the B-G473E-ZEST1S Discovery board. The embedded STLINK-V3EC supports only SWD and VCP for STM32 devices. Features supported in STLINK-V3EC;

- 5 V power supplied by the USB Type-C® connector (CN4)
- USB 2.0 high-speed-compatible interface
- Serial Wire Debug (SWD) interface
- STDC14, MIPI10-compatible connector (CN2)
- Second USART connector (CN1) for external debugger
- COM status tricolor LED (LD6) which blinks during communication with the PC
- Power status tricolor LED (LD5) which provides information about STLINK-V3EC target power status
- 5 V power green LED (LD4)

Table 5 describes the USB Type-C® connector (CN4) pinout.

Table 5. USB Type-C® connector (CN4) pinout

Pin number	Pin name	Signal name	STLINK-V3EC STM32 pin	Function
A4, A9, B4, and B9	VBUS	5V_USB_CHGR	-	VBUS power
A7 and B7	DM	USB_DEV_HS_CN_N	PB14	DM
A6 and B6	DP	USB_DEV_HS_CN_P	PB15	DP
A5	CC1	-	-	5.1 kΩ pull-down
B5	CC2	-	-	5.1 kΩ pull-down
A1, A12, B1, and B12	GND	GND	GND	GND

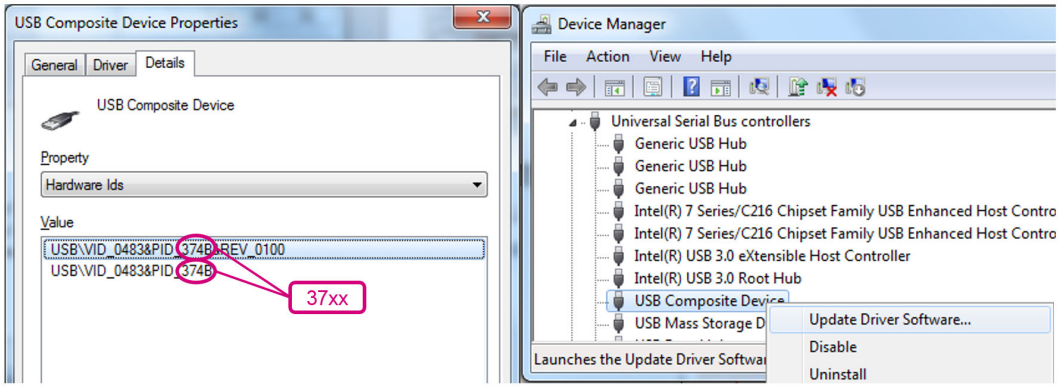
6.3.2 Drivers

Before connecting the B-G473E-ZEST1S Discovery board to a Windows PC via USB, the user must install a driver for the STLINK-V3EC (not required for Windows 10). It is available on the *www.st.com* website.

In case the B-G473E-ZEST1S Discovery board is connected to the PC before the driver is installed, some B-G473E-ZEST1S Discovery board interfaces might be declared as *Unknown* in the PC device manager. In this case, the user must install the dedicated driver files, and update the driver of the connected device from the device manager as shown in Figure 5.

Note: Prefer using the USB Composite Device to handle a full recovery.

Figure 5. USB composite device



Note: 37xx:

- *374E for STLINK-V3EC without bridge functions*
- *374F for STLINK-V3EC with bridge functions*

6.3.3 Firmware upgrade

STLINK-V3EC embeds a firmware upgrade mechanism for in-place upgrades through the USB port. As the firmware might evolve during the lifetime of the STLINK-V3EC product (for example new functionalities, bug fixes, support for new microcontroller families), it is recommended to visit the *www.st.com* website before starting to use the B-G473E-ZEST1S Discovery board and periodically, to stay up-to-date with the latest firmware version.

6.3.4 Use of an external debugging tool to program and debug the on-board STM32

There are two basic ways to support an external debugging tool:

1. Keep the embedded STLINK-V3EC running. Power on the STLINK-V3EC at first until the COM LED lights red. Then connect the external debugging tool through the STDC14/MIPI10 debug connector (CN2).
2. Connect the USART connector on the external debugging tool (for example, STLINK-V3SET) to the USART connector (CN1) for the second VCP (optional).

6.4 STDC14/MIPI10 and USART connectors

6.4.1 Description

The 7x2-pin header 1.27 mm pitch connector (CN2), can output the SWD signals used for debugging compatible with STDC14.

Figure 6 shows the CN2 STDC14 connector pinout.

Figure 6. STDC14 connector pinout (CN2)

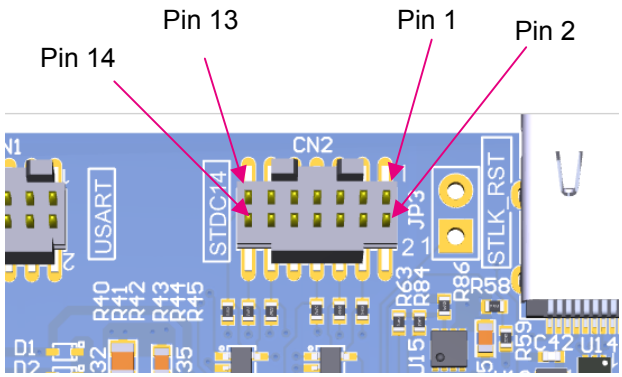


Table 6 describes the STDC14/MIPI10 connector pinout compatible with both interfaces: STDC14 and MIPI10.

Table 6. STDC14/MIPI10 debug connector pinout

MIPI10 pin number	STDC14 pin number	STM32 pin	Board function
-	1	-	Reserved
-	2	-	Reserved
1	3	VDD	Target VDD
2	4	PA13	JTMS_SWDIO: Target SWDIO using the SWD protocol.
3	5	GND	Ground
4	6	PA14	JTCK_SWCLK: Target SWCLK using the SWD protocol.
5	7	GND	Ground
6	8	PB3	JTDO_SWO: Target SWO using the SWD protocol.
7	9	-	NC
8	10	-	NC
9	11	-	GNDDetect: GND detection for plug indicator
10	12	NRST	NRST: Target NRST using the SWD protocol
-	13	PA10	T_VCP1_RX: Target RX used for VCP and connected to STLK_VCP_TX
-	14	PA9 (bootloader)/ PG9 (no bootloader)	T_VCP1_TX: Target TX used for VCP and connected to STLK_VCP_RX

Table 7 describes the hardware configuration for the STDC14 function.

Table 7. Hardware I/O configuration for the STDC14 connector (CN2)

IO	Bridge	Setting(1)	Comment
PA9	SB54	ON	PA9 is used as USART1_TX, it is connected to T_VCP1_TX (bootloader support).
		OFF	**PA9 is NOT connected to T_VCP1_TX.** **PA9 can be used as an ADC on Morpho MC.**
PG9	SB51	**ON**	**PA9 is used as USART1_TX, it is connected to T_VCP1_TX (no bootloader support).**
PA10	-	-	PA10 is used as USART1_RX, it is connected to T_VCP1_RX.
PA13	-	-	PA13 is connected to SWD SWDIO.
PA14	-	-	PA14 is connected to SWD SWCLK.
PB3	-	-	PB3 is connected to SWD SWO.
NRST	-	-	NRST is used to reset the target.

1. *The default configuration is in bold.*

The 5x2-pin header 1.27 mm pitch connector (CN1) can output USART2 signals used for the second VCP port.

Figure 7 shows the USART connector (CN1) pinout.

Figure 7. USART connector (CN1) pinout

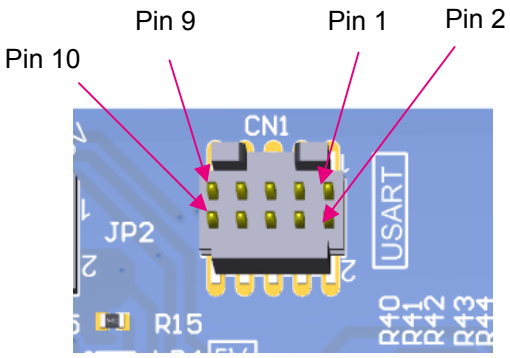


Table 8 describes the USART connector pinout.

Table 8. USART debug connector pinout

Connector pin number	STM32 pin	Board function
1	-	NC
2	-	NC
3	PD6	T_VCP2_RX: Target RX used for VCP2 and connected to Bridge_USART_TX
4	-	NC
5	PD5	T_VCP2_TX: Target TX used for VCP2 and connected to Bridge_USART_RX
6	-	NC
7	-	NC
8	-	NC
9	GND	Ground
10	-	NC

Table 9 describes the hardware configuration for the USART connector.

Table 9. Hardware I/O configuration for the USART connector (CN1)

IO	Bridge	Setting[1]	Comment
PD5	SB58	**ON**	**PD5 is used as USART2_TX, it is connected to T_VCP2_TX.**
		OFF	PD5 is NOT connected to T_VCP2_TX. PD5 can be used as LED3.
PD6	SB49	ON	PD6 is used as USART2_RX, it is connected to T_VCP2_RX.
		OFF	**PD6 is NOT connected to T_VCP2_RX.** **PD6 can be used as LED2.**

1. *The default configuration is in bold.*

6.4.2 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32G473QET6 by multiple peripherals, the following limitations apply in using the STDC14 and USART2 features:

- By default, VCP1_TX is connected to PG9 without bootloader support. VCP1_TX can be connected to PA9 with the bootloader by setting SB51 and SB60 OFF and SB54 ON (removing SB60 disconnects Morpho MC (CN7) pin35). If PA9 is used as VCP1_TX, Morpho MC (CN7) pin35 cannot be used.
- By default, VCP2_RX is not connected. VCP2_RX can be connected to PD6 by setting SB49 ON (sharing with LED2).

6.5 Power supply

6.5.1 5 V power supply general view

The B-G473E-ZEST1S Discovery board is designed to be powered from the 5 V DC power source. One of the following five 5 V DC power inputs can be used, upon an appropriate board configuration:

- P5V from CN5 MC connector V2 (CN5) for power board (default)
- 5V_USB_STLK from the USB Type-C® receptacle (CN4) of STLINK-V3EC
- E5V from Morpho MC connector (CN7) for custom daughterboard
- 5V_USB_CHGR from the USB Type-C® receptacle (CN4) of STLINK-V3EC, in the case of a wall charger (no enumeration)

The green LED (LD4) turns on when the voltage on the power line marked as 5V is present. All supply lines required for the operation of the components on B-G473E-ZEST1S are derived from that 5V line.

Table 10 describes the 5V power supply capabilities.

Table 10. Power source capability

Input power name	Connector pins	Voltage range	Max current	Limitation
P5V	CN5 pin A05 and B05 JP2[1-2]	4.75 to 5.25 V	1500 mA	• The maximum current depends on the power board
5V_USB_STLK	CN4 pin A4/A9/B4/B9 JP2[3-4]		500/1500/3000 mA	STLINK-V3EC manages the maximum current.
E5V	CN7 pin 6 JP2[5-6]		-	The maximum current depends on the daughter boards
5V_CHG	CN4 pin A4/A9/B4/B9 JP2[7-8]		-	The maximum current depends on the USB wall charger used to power the board (no enumeration, no current protection).

6.5.2 P5V power source

P5V is the DC power coming from the power board through MC connector V2 (CN5). In this case, the JP2 jumper must be on pin [1-2] to select the P5V power source on the JP2 silkscreen. This is the default setting.

6.5.3 5V STLINK-V3EC source: 5V_USB_STLK

5V_STLK is a DC power with limitations from the STLINK-V3EC USB Type-C® connector. In this case, the JP2 jumper must be on pin [3-4] to select the STLK power source on the JP2 silkscreen. If the USB enumeration succeeds, the 5V_STLK power is enabled, by asserting the T_PWR_EN signal, coming from the STLINK-V3EC MCU (U12). This pin is connected to a USB power switch (U15), which powers the board. This power switch features also a 500 mA current limitation, to protect the PC in case of an on-board short-circuit.

The B-G473E-ZEST1S board, with its shield on it, can be powered from the STLINK-V3EC USB connector (CN4), but only the STLINK-V3EC circuit has the power before USB enumeration, as the host PC only provides 100 mA to the board at that time. During the USB enumeration, the B-G473E-ZEST1S board asks for 500 mA power to the host PC.

If the host can provide the required power, the enumeration finishes with a *SetConfiguration* command, and then, the power switch is switched ON, the 5V green LED (LD4) turns ON, thus the B-G473E-ZEST1S board and its shield on it can consume 500 mA current, but no more.

If the host is not able to provide the requested current, the enumeration fails. Therefore, the power switch remains OFF and the MCU power domain, including the extension board, is not powered. As a consequence, the 5V green LED (LD4) remains turned OFF. In this case, it is mandatory to use an external power supply.

6.5.4 E5V power source

E5V is the DC power coming from the Morpho MC connector (CN7). In this case, the JP2 jumper must be set on pin [5-6] to select the E5V power source on the JP2 silkscreen.

6.5.5 5V_CHG power source

VBUS_STLK is the DC power charger connected to STLINK-V3EC USB (CN4). To select the CHG power source on the JP2 silkscreen, the jumper of JP2 must be set on pins [7-8].

Note: If the B-G473E-ZEST1S board is powered by an external USB charger, then the debug is not available. If a computer is connected instead of the charger, the current limitation is no longer effective. Never use this configuration with a computer connected instead of the charger, because the USB_PWR_protection is bypassed, and if the board consumption is more than 500 mA, this can damage the computer. To avoid this risk, it is recommended to select 5V_STLK mode.

6.5.6 Programing/debugging when the power supply is not from STLINK-V3EC (5V_STLK)

P5V or E5V can be used as an external power supply in case the current consumption of the B-G473E-ZEST1S with expansion boards exceeds the allowed current on USB. In such a condition, it is still possible to use USB for communication for programming or debugging only.

In this case, it is mandatory to power the board first using P5V or E5V then connect the B-G473E-ZEST1S USB cable to the PC. Proceeding this way, the enumeration succeeds thanks to the external power source.

The following power sequence procedure must be respected:

1. Connect the JP2 jumper according to the external 5V power source selected.
2. Connect the external power source selected.
3. Power on the external power supply source.
4. Check that the 5V green LED (LD4) is turned ON.
5. Connect the PC to the B-G473E-ZEST1S USB connector (CN4).

If this sequence is not respected, V_{BUS} from STLINK-V3EC might power the board first, and the following risks might be encountered:

- If the board needs more than 500 mA, it might damage the PC or the PC limits the current. Therefore, the board is not powered correctly.
- A 500 mA current is requested at enumeration. If the PC does not provide such a current, the request might be rejected, and enumeration does not succeed. Consequently, the board is not powered, and the green LED (LD4) remains OFF.

6.6 Clock sources

Two clock references are available on B-G473E-ZEST1S for the STM32G473QET6 target microcontroller.

- 32.768 kHz crystal X2 for embedded RTC (LSE)
- 24 MHz oscillator X1 for HSE clock

6.7 Reset sources

The reset signal of the STM32G473QET6 on the B-G473E-ZEST1S Discovery board is active LOW.

Sources of reset are:

- B1 reset button (black button)
- CN2 STDC14 connector (CN2), reset from debug tools
- Embedded STLINK-V3EC MCU (U12)

6.8 RSS/bootloader

6.8.1 Description

The bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the flash memory via USART, I^2C, SPI, CAN FD, or USB FS in device mode through the DFU (device firmware upgrade). The bootloader is available on all devices. Refer to the application note *STM32 microcontroller system memory boot mode* (AN2606) for more details.

The Root Secure Services (RSS) are embedded in a flash memory area named the secure information block, programmed during ST production. For example, it enables Secure Firmware Installation (SFI), thanks to the RSS extension firmware (RSSe SFI). This feature allows customers to protect the confidentiality of the firmware to be provisioned into the STM32 when production is subcontracted to an untrusted third-party. The Root Secure Services are available on all devices, after enabling the TrustZone® through the TZEN option bit.

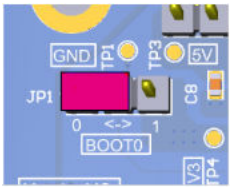
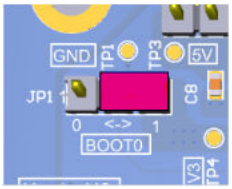
The bootloader version can be identified by reading the bootloader ID at the address `0x0BF99EFE`.

6.8.2 Boot from RSS

The BOOT0 value might come from the PB8_BOOT0 pin, connected to the BOOT jumper JP1, or from an option bit depending on the value of a user option bit.

Table 11 describes the hardware configuration of the switch SW1 for the Boot mode.

Table 11. BOOT selection switch

I/O	Jumper	Setting(1)	Description
PB8-BOOT0	JP1	**BOOT0 = 0 (JP1 [1-2])** 	The BOOT0 line is tied low. STM32G473QET6 boot address defined by user option bytes NSBOOTADD0 or SECBOOTADD0 according to TrustZone® setting.
		BOOT0 = 1 (JP1 [2-3]) 	The BOOT0 line is tied high. STM32G473QET6 boot address defined by user option bytes NSBOOTADD1 or RSS according to TrustZone® setting.

1. *The default configuration is in bold.*

Caution: PB8_BOOT0 is also used as a Hall sensor signal of Motor2, the pull-up resistor on the Hall sensor signal (M2_Hall_3) might impact the function of BOOT0, thus MCU does not boot from flash memory. When using M2_Hall_3, the BOOT0 feature must be bypassed by setting the nSWBOOT0 option byte to LOW, and nBOOT0 and mBOOT1 bytes to HIGH.

6.9 MC connector V2

6.9.1 Description

MC connector V2 is a new generation interface between the control board and the power board (or adaptor board). It is a PCI Express format connector. On B-G473E-ZEST1S, this connector is a PCI-E 16x edge-finger.

Three motors, PFC, SPI, and ADCs signals are implemented on MC connector V2. The signals of the second motor (Motor 2) signals are shared with the Morpho MC signals.

6.9.2 Pinout

Table 12 describes the pinout of the CN5 MC connector V2.

Table 12. MC connector V2

Pin number	Category	Pin name	STM32 signal	Function of B-G473E-ZEST1S	Comment
A side					
1	SPI	SPI_nSS	PG5	M_SPI_1_NSS	-
2		SPI_SCK	PG2	M_SPI_1_SCK	-
3		SPI_nSS	-	-	-
4		SPI_SCK	-	-	-
5		5V_to_CTRLB	-	P5V	-
6		3.3V_to_PWRB	-	3V3	-
7		DGND	-	GND	-
8		ID_Enable	PF15	GPIO	-
9	ADC	ADC	-	-	-
10		ADC	-	-	-
11		ADC	-	-	-
12	Motor1	Emergency(BKIN)	PB7	M1_EmergencySTOP_TIM_8_BKIN	-
13		INH/PWM	PC6	M1_PWM_UH_TIM_8_CH1	-
14		INH/PWM	PC7	M1_PWM_VH_TIM_8_CH2	-
15		INH/PWM	PC8	M1_PWM_WH_TIM_8_CH3	-
16		Master_EN	PG7	M1_Master_EN(GPIO)	-
17		Timer_ETR	PA0	M1_TIM_8_ETR	-
18		Hall_sensors_H1	PE2	M1_Hall_1_TIM_3_CH1	-
19		Hall_sensors_H2	PE3	M1_Hall_2_TIM_3_CH2	-
20	-	DGND	-	GND	-
21	Motor1	Shunt+	PB0	M1_SHUNT1_OPAMP_3_VINP	Refer to Table 19 for SB setting
		ADC input	PD11	M1_CURR_U_ADC_345_IN8	
22		Shunt+	PB11	M1_SHUNT2_OPAMP_4_VINP	
		ADC input	PD12	M1_CURR_V_ADC_345_IN9	
23		Shunt+	PB14	M1_SHUNT3_OPAMP_5_VINP	
		ADC input	PD14	M1_CURR_W_ADC_345_IN11	
24	-	AGND	-	GND	-
25	Motor1	Ph_Voltage+/BEMF_zc	PD10	M1_VOL+_U_ADC_345_IN7	-
26		Ph_Voltage+/BEMF_zc	PE12	M1_VOL+_V_ADC_345_IN16	-

Pin number	Category	Pin name	STM32 signal	Function of B-G473E-ZEST1S	Comment
27	Motor1	Ph_Voltage+/BEMF_zc	PD13	M1_VOL+_W_ADC_345_IN10	-
28		Temperature/Board ID	PE15	M1_TEMP_ADC_4_IN2	-
29		VBUS	PB13	M1_VBUS_ADC_3_IN5	-
30		Dissipative_brake	PG8	M1_DissipativeBrake(GPIO)	-
31	-	DGND	-	GND	-
32	-	AGND	-	GND	-
33	PFC	AC_voltage	PF1	M_AC voltage_ADC_2_IN10	-
34		PFC_Current1	PD8	M_PFC current 1_ADC_4_IN12/5_IN12	-
35		PFC_BKIN_OC	PB5	M_PFC_BKIN_OC_TIM_16_BKIN	-
36		PFC_PWM1	PE0	M_PFC_PWM1_TIM_16_CH1	-
37	Motor2	Emergency(BKIN)	PA15	M2_EmergencySTOP_TIM_1_BKIN	-
38		INH/PWM	PE9	M2_PWM_UH_TIM_1_CH1	-
39		INH/PWM	PE11	M2_PWM_VH_TIM_1_CH2	-
40		INH/PWM	PE13	M2_PWM_WH_TIM_1_CH3	-
41		Master_EN	PG6	M2_Master_EN(GPIO)	-
42		Timer_ETR	PE7	M2_TIM_1_ETR	-
43		Hall_sensors_H1	PB6	M2_Hall_1_TIM_4_CH1	-
44		Hall_sensors_H2	PA12	M2_Hall_2_TIM_4_CH2	-
45	-	DGND	-	-	-
46	Motor2	Shunt+	PA7	M2_SHUNT1_ADC_2_IN4	-
47		Shunt+	PC2	M2_SHUNT2_ADC_12_IN8	-
48		Shunt+	PC3	M2_SHUNT3_ADC_12_IN9	-
49	-	AGND	-	GND	-
50	Motor2	Ph_Voltage+/BEMF_zc	-	-	For test only
51		Ph_Voltage+/BEMF_zc	-	-	For test only
52		Ph_Voltage+/BEMF_zc	-	-	For test only
53		Temperature/Board ID	PC4	M2_TEMP_ADC_2_IN5	-
54		VBUS	PC0	M2_VBUS_ADC_12_IN6	-
55		Dissipative_brake	PD0	M2_DissipativeBrake(GPIO)	-
56	-	DGND	-	GND	-
57	Motor3	Emergency(BKIN)	PF9	M3_EmergencySTOP_TIM_20_BKIN	-
58		INH/PWM	PF12	M3_PWM_UH_TIM_20_CH1	-
59		INH/PWM	PF13	M3_PWM_VH_TIM_20_CH2	-
60		INH/PWM	PF14	M3_PWM_WH_TIM_20_CH3	-
61		Master_EN	-	-	-
62		Timer_ETR	-	-	-
63		Hall_sensors_H1	-	-	-
64		Hall_sensors_H2	-	-	-
65	-	DGND	-	GND	-

Pin number	Category	Pin name	STM32 signal	Function of B-G473E-ZEST1S	Comment
66	Motor3	Shunt+	PA1	M1_Resolver_Sin/ M3_SHUNT1_ADC_12_IN2	Shared with pin B-29(1)
67		Shunt+	PC1	M1_Resolver_Cos/ M3_SHUNT2_ADC_12_IN7	Shared with pin B-55(1)
68		Shunt+	PA2	M2_Resolver_Cos/ M3_SHUNT3_ADC_1_IN3	Shared with pin B-30(1)
69	-	AGND	-	GND	-
70	Motor3	Ph_Voltage+/BEMF_zc	-	-	-
71		Ph_Voltage+/BEMF_zc	-	-	-
72		Ph_Voltage+/BEMF_zc	-	-	-
73		Temperature/Board ID	PA6	M3_BoardID_ADC2_IN3	-
74		VBUS	-	-	-
75		Dissipative_brake	-	-	-
76	-	DGND	-	GND	-
77	Motor1	SD_CLKO/SPI_nSS	-	-	-
78		SD_DIN/Enable	-	-	-
79	Motor2	SD_CLKO/SPI_nSS	-	-	-
80		SD_DIN/Enable	-	-	-
81	Motor3	SD_CLKO/SPI_nSS	-	-	-
82		SD_DIN/Enable	-	-	-
B side					
1	SPI	SPI_MISO	PG3	M_SPI_1_MISO	-
2		SPI_MOSI	PG4	M_SPI_1_MOSI	-
3		SPI_MISO	-	-	-
4		SPI_MOSI	-	-	-
5	-	5V_to_CTRLB	-	P5V	-
6	-	VREF+	-	3V3	-
7	-	DGND	-		-
8	-	AGND	-		-
9	ADC	ADC	-	-	-
10		ADC	-	-	-
11		ADC	-	-	-
12	Motor1	Emergency(BKIN2)	PD1	M1_EmergencySTOP_TIM_8_BKIN2	-
13		INL/EN	PC10	M1_PWM_UL_TIM_8_CH1N	-
14		INL/EN	PC11	M1_PWM_VL_TIM_8_CH2N	-
15		INL/EN	PC12	M1_PWM_WL_TIM_8_CH3N	-
16		Encoder_A	PF6	M1_Encoder_A_TIM_5_CH1	-
17		Encoder_B	PF7	M1_Encoder_B_TIM_5_CH2	-
18		Encoder_Z	PF8	M1_Encoder_Z_TIM_5_CH3	-
19		Hall_sensors_H3	PE4	M1_Hall_3_TIM_3_CH3	-
20	-	DGND	-	GND	-
21	Motor1	Shunt-	PB2	M1_SHUNT1_OPAMP_3_VINM	-

Pin number	Category	Pin name	STM32 signal	Function of B-G473E-ZEST1S	Comment
22	Motor1	Shunt-	PB10	M1_SHUNT2_OPAMP_4_VINM	-
23		Shunt-	PB15	M1_SHUNT3_OPAMP_5_VINM	-
24	-	AGND	-	GND	-
25	Motor1	Ph_Voltage-/BEMF_ref	-	GND	-
26		Ph_Voltage-/BEMF_ref	-	GND	-
27		Ph_Voltage-/BEMF_ref	-	GND	-
28		Res.Ex/Curr.REF	PA4	M1_DAC_1_OUT1	-
29		Resolver_Sin/GPIO_BEMF	PA1	M1_Resolver_Sin/ M3_SHUNT1_ADC_12_IN2	Shared with pin A-66(1)
30		Resolver_Cos	PA2	M1_Resolver_Cos/ M3_SHUNT2_ADC_1_IN3	Shared with pin A-68(1)
31	-	DGND	-	GND	-
32	-	AGND	-	GND	-
33	PFC	AC_zero_crossing	PC5	M_AC zero crossing_ADC_2_IN11	-
34		PFC_Current2	PD9	M_PFC current 2_ADC_4_IN13/5_IN13	-
35		Inrush_lim.	PF11	Inrush lim(GPIO)	-
36		PFC_PWM2	PE1	M_PFC_PWM2_TIM_17_CH1	-
37	Motor2	Emergency(BKIN2)	PA11	M2_EmergencySTOP_TIM_1_BKIN2	-
38		INL/EN	PE8	M2_PWM_UL_TIM_1_CH1N	-
39		INL/EN	PE10	M2_PWM_VL_TIM_1_CH2N	-
40		INL/EN	PB9	M2_PWM_WL_TIM_1_CH3N	-
41		Encoder_A	PD3	M2_Encoder_A_TIM_2_CH1/2_ETR	-
42		Encoder_B	PD4	M2_Encoder_B_TIM_2_CH2	-
43		Encoder_Z	PD7	M2_Encoder_Z_TIM_2_CH3	-
44		Hall_sensors_H3	PB8-BOOT0	M2_Hall_3_TIM_4_CH3/BOOT0	Shared with BOOT0 function on the board(2)
45	-	DGND	-	GND	-
46	Motor2	Shunt-	-	GND	-
47		Shunt-	-	GND	-
48		Shunt-	-	GND	-
49	-	AGND	-	GND	-
50	Motor2	Ph_Voltage-/BEMF_ref	-	GND	-
51		Ph_Voltage-/BEMF_ref	-	GND	-
52		Ph_Voltage-/BEMF_ref	-	GND	-
53		Res.Ex/Curr.REF	PA5	M2_DAC_1_OUT2	-
54		Resolver_Sin/GPIO_BEMF	PA3	M2_Resolver_Sin/ Potentiometer_ADC_1_IN4	Shared with POT(3)
55		Resolver_Cos	PC1	M2_Resolver_Cos/ M3_SHUNT3_ADC_12_IN7	Shared with A-67(1)
56	-	AGND	-	GND	-

Pin number	Category	Pin name	STM32 signal	Function of B-G473E-ZEST1S	Comment
57	Motor3	Emergency(BKIN2)	PF10	M3_EmergencySTOP_TIM_20_BKIN2	-
58		INL/EN	PG0	M3_PWM_UL_TIM_20_CH1N	-
59		INL/EN	PG1	M3_PWM_VL_TIM_20_CH2N	-
60		INL/EN	PE6	M3_PWM_WL_TIM_20_CH3N	-
61		Encoder_A	-	-	-
62		Encoder_B	-	-	-
63		Encoder_Z	-	-	-
64		Hall_sensor_H3	-	-	-
65	-	DGND	-	GND	-
66	Motor3	Shunt-	-	GND	-
67		Shunt-	-	GND	-
68		Shunt-	-	GND	-
69	-	AGND	-	GND	-
70	Motor3	Ph_Voltage-/BEMF_ref	-	GND	-
71		Ph_Voltage-/BEMF_ref	-	GND	-
72		Ph_Voltage-/BEMF_ref	-	GND	-
73		Res.Ex/Curr.REF	-	-	-
74		Resolver_Sin/GPIO_BEMF	-	-	-
75		Resolver_Cos	-	-	-
76	-	AGND	-	GND	-
77	Motor1	SD_DIN/Enable	PF4	M1_ENABLE1(GPIO)	-
78		SD_DIN/Enable	PF5	M1_ENABLE2(GPIO)	-
79	Motor2	SD_DIN/Enable	PE5	M2_ENABLE1(GPIO)	-
80		SD_DIN/Enable	PF2	M2_ENABLE2(GPIO)	-
81	Motor3	SD_DIN/Enable	PC9	M3_ENABLE1(GPIO)	-
82		SD_DIN/Enable	PD2	M3_ENABLE2(GPIO)	-

1. *Refer to Section 6.9.3 for details.*
2. *Refer to Section 6.8.2 for details.*
3. *Refer to Section 6.14.2 for details.*

6.9.3 Hardware configuration for MC connector V2

Table 13 describes the pinout of the CN5 MC connector V2.

Table 13. Hardware I/O configuration for MC connector V2

I/O	Hardware	Setting[1]	Configuration
PA1	SB4, SB9	**SB4 ON, SB9 OFF**	**PA1 is used as the Motor1 Resolver_Sin signal**
		SB4 OFF, SB9 ON	PA1 is used as the Motor3 current input 1
PA2	SB23, SB19	**SB23 ON, SB19 OFF**	**PA2 is used as the Motor1 Resolver_Cos signal**
		SB23 OFF, SB19 ON	PA2 is used as the Motor3 current input 3
PC1	SB27, SB20	**SB27 ON, SB20 OFF**	**PC1 is used as the Motor2 Resolver_Cos signal**
		SB27 OFF, SB20 ON	PC1 is used as the Motor3 current input 2

1. *The default configuration is in bold.*

6.9.4 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32G473QET6 by multiple peripherals, the following limitations apply in using the MC connector V2:

- The M2_Resolver sin (PA3) cannot be operated simultaneously with the potentiometer.
- The Motor2 cannot be operated simultaneously with the Morpho MC connectors.

6.10 Morpho MC connectors

6.10.1 Description

The Morpho MC connectors (CN7 and CN10) are implemented on B-G473E-ZEST1S to be compatible with the X-NUCLEO-IHM08M1, X-NUCLEO-IHM09M1, and X-NUCLEO-IHM16M1 motor-driver expansion boards.

6.10.2 Pinout

Figure 8 shows the position of the Morpho MC connectors on B-G473E-ZEST1S.

Figure 8. CN7 and CN10 connector pinout

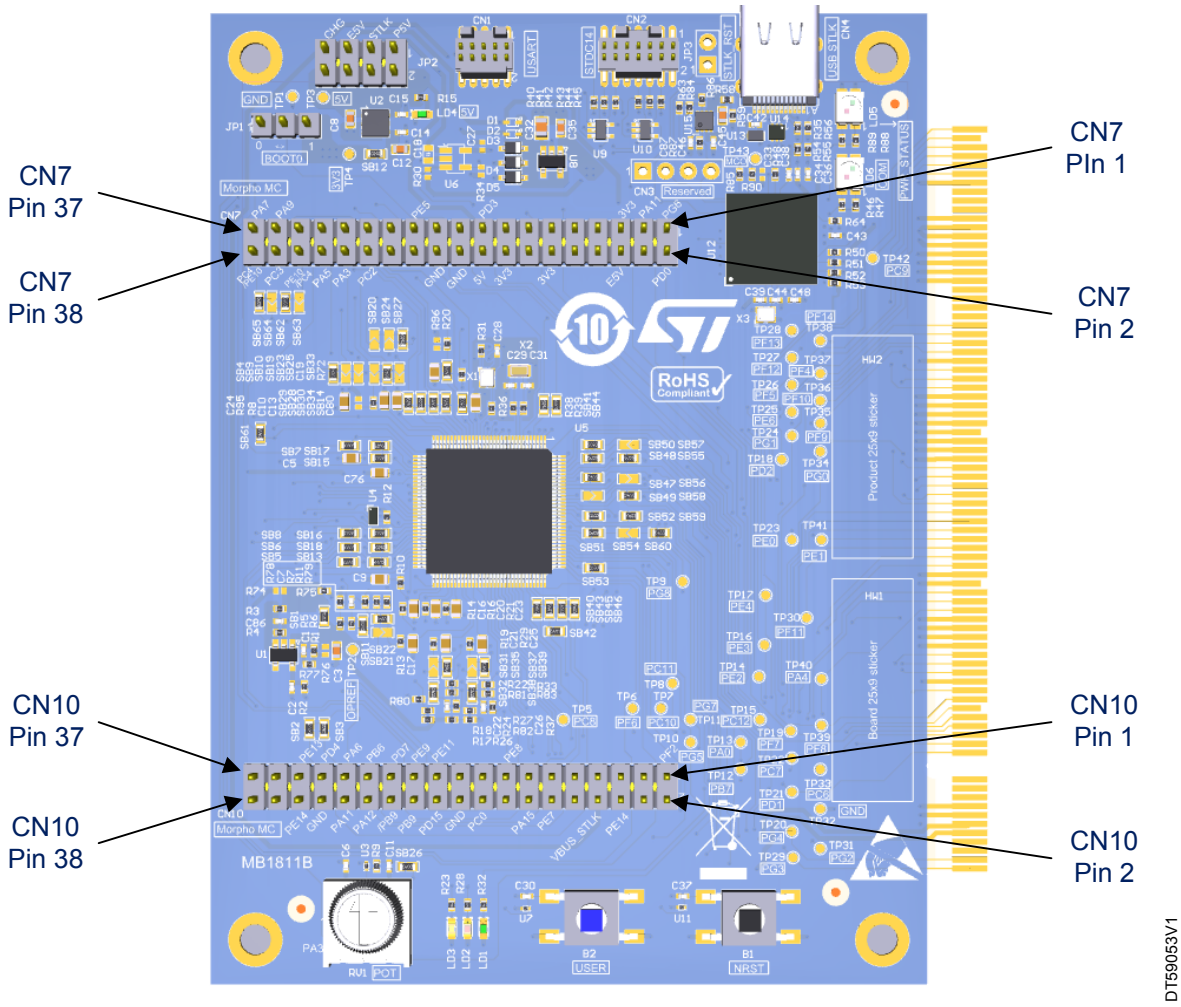


Table 14 and Table 15 describe the pinout of the Morpho MC connectors.

Table 14. Morpho MC connector (CN7)

Pin number	Category	Pin name	STM32 signal	Function of X-NUCLEO-IHM08M1	Function of X-NUCLEO-IHM09M1	Function of X-NUCLEO-IHM16M1
1	GPIO	NTC_bypass_GPIO	PG6	-	NTC bypass	-
2	GPIO	DissipativeBrake_GPIO	PD0	-	Dissipative brake/OCP disable	-
3	-	-	-	-	-	-
4	-	-	-	-	-	-
5	-	-	-	-	-	-
6	E5V	-	-	E5V	E5V	-
7	-	-	-	-	-	-

Pin number	Category	Pin name	STM32 signal	Function of X-NUCLEO-IHM08M1	Function of X-NUCLEO-IHM09M1	Function of X-NUCLEO-IHM16M1
8	-	-	-	-	-	-
9	-	-	-	-	-	-
10	-	-	-	-	-	-
11	-	-	-	-	-	-
12	VDD	-	-	VDD	VDD	VDD
13	-	-	-	-	-	-
14	-	-	-	-	-	-
15	-	-	-	-	-	-
16	-	-	-	-	-	-
17	TIMy_CH1	TIM_2_CH1/ 2_ETR	PD3	Encoder A/Hall H1	Encoder A/Hall H1	Encoder A/Hall H1
18	+5V	-	-	+5V	+5V	+5V
19	-	-	-	-	-	-
20	GND	-	-	GND	GND	GND
21	-	-	-	-	-	-
22	GND	-	-	GND	GND	GND
23	GPIO	Button_GPIO	PE5	Button	-	-
24	-	-	-	-	-	-
25	-	-	-	-	-	-
26	-	-	-	-	-	-
27	-	-	-	-	-	-
28	ADC	ADC_12_IN8	PC2	Current_A	Current_A	VBUS
29	-	-	-	-	-	-
30	ADC	ADC_1_IN4	PA3(1)	VBUS	VBUS	Current_A
31	-	-	-	-	-	-
32	DAC	DAC_1_OUT2	PA5	DAC	DAC	DAC
33	-	-	-	-	-	-
34	TIMx_CH2N	TIM_1_CH2N	PE10(2)	VL	VL	-
	ADC	ADC_2_IN5	PC4(2)	-	-	Current_C
35	ADC	ADC_5_IN2 (shared with bootloader TX)	PA9(3)	Temp	Temp	Speed
36	ADC	ADC_12_IN9	PC3	Current_B	Current_B	BEMF3
37	ADC	ADC_2_IN4	PA7	BEMF1	BEMF1	BEMF2
38	ADC	ADC_2_IN5	PC4(2)	Current_C	Current_C	-
	ADC	ADC345_IN14	PE10(2)	-	-	BEMF1

1. *SB26 to be OFF when PA3 is used on Morpho MC, refer to Table 20 for details.*
2. *PC4 and PE10 are needed to swap for IHM16M1. Refer to Table 16 for details.*
3. *PA9 might be used as VCP1_TX with bootloader support, refer to Table 6 and Table 7 for details.*

Table 15. **Morpho MC connector (CN10)**

Pin number	Category	Pin name	STM32 signal	Function of X-NUCLEO-IHM08M1	Function of X-NUCLEO-IHM09M1	Function of X-NUCLEO-IHM16M1
1	GPIO	BEMF_GPIO	PF2	GPIO_BEMF	-	GPIO_BEMF
2	-	-	-	-	-	-
3	-	-	-	-	-	-
4	-	-	-	-	-	-
5	-	-	-	-	-	-
6	ADC	ADC_4_IN1	PE14(1)	BEMF3	-	-
7	-	-	-	-	-	-
8	U5V	-	-	-	-	-
9	-	-	-	-	-	-
10	-	-	-	-	-	-
11	-	-	-	-	-	-
12	TIMx_ETR	TIM_1_ETR	PE7	CPOUT (TIMx_ETR)	-	-
13	-	-	-	-	-	-
14	TIMx_BKIN	TIM_1_BKIN	PA15	BKIN	BKIN2	BKIN
15	TIMx_CH1N	TIM_1_CH1N	PE8	UL	UL	UL(2)
16	-	-	-	-	-	-
17	-	-	-	-	-	-
18	ADC	ADC_12_IN6	PC0	BEMF2	-	Current_B
19	-	-	-	-	-	-
20	-	-	-	-	-	-
21	TIMx_CH2	TIM_1_CH2	PE11	VH	VH	VH
22	GPIO	LED_RED_GPIO	PD15	LED_RED	LED_RED	-
23	TIMx_CH1	TIM_1_CH1	PE9	UH	UH	UH
24	TIMx_CH3N	TIM_1_CH3N	PB9(3)	WL	WL	-
25	TIMy_CH3	TIM_2_CH3	PD7	Encoder Z/Hall H3	Encoder Z/Hall H3	Encoder Z/Hall H3
26	TIMx_CH3N	TIM_1_CH3N	PB9(3)	-	-	WL
27	TIMz	TIM_4_CH1	PB6	PWM	PWM	PWM
28	TIMx_CH2N(2)	TIM_1_CH2N	PA12	-	-	VL
29	DAC	DAC_2_OUT1	PA6	DAC	DAC	-
30	TIMx_CH1N(2)	TIM_1_CH1N	PA11	-	-	UL
31	TIMy_CH2	TIM_2_CH2	PD4	Encoder B/Hall H2	Encoder B/Hall H2	Encoder B/Hall H2
32	-	-	-	-	-	-
33	TIMx_CH3	TIM_1_CH3	PE13	WH	WH	WH
34	ADC	ADC_4_IN1	PE14(1)	-	-	NTC
35	-	-	-	-	-	-
36	-	-	-	-	-	-

Pin number	Category	Pin name	STM32 signal	Function of X-NUCLEO-IHM08M1	Function of X-NUCLEO-IHM09M1	Function of X-NUCLEO-IHM16M1
37	-	-	-	-	-	-
38	-	-	-	-	-	-

1. *PE14 is shared on CN10 pins 6 and 34, refer to Table 16 for details.*
2. *R74 to be ON on the X-NUCLEO-IHM16M1*
3. *PB9 is shared on CN10 pins 24 and 26, refer to Table 16 for details.*

6.10.3 Hardware configuration for Morpho MC

The hardware configuration for the Morpho MC is shown in Table 16.

Table 16. Hardware I/O configuration for the Morpho MC

I/O	Hardware	Setting(1)	Configuration
PE10 and PC4	SB62 SB64 SB63 SB65	**ON** **OFF** **OFF** **ON**	**PE10 is connected to Morpho MC CN7 pin 34 and PC4 is connected to Morpho MC CN7 pin 36 for IHM08M1 and IHM09M1.**
		OFF ON ON OFF	PE10 is connected to Morpho MC CN7 pin 36 and PC4 is connected to Morpho MC CN7 pin 34 for IHM16M1.
PE14	SB3	**ON**	**PE14 is connected to Morpho MC CN10 pin6.**
		OFF	PE14 is NOT connected to Morpho MC CN10 pin 6
	SB2	**ON**	**PE14 is connected to Morpho MC CN10 pin 34.**
		OFF	PE14 is NOT connected to Morpho MC CN10 pin34.
PB9	SB50	**ON**	**PB9 is connected to Morpho MC CN10 pin24**
		OFF	PB9 is NOT connected to Morpho MC CN10 pin24
	SB57	**OFF**	**PB9 is NOT connected to Morpho MC CN10 pin26**
		ON	PB9 is connected to Morpho MC CN10 pin26

1. *The default configuration is in bold.*

6.10.4 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32G473QET6 by multiple peripherals, the following limitations apply in using the Morpho MC connectors:

1. The PA3 (CN7 pin 30) cannot be operated simultaneously with the potentiometer. When using PA3 on Morpho MC, SB26 must be OFF. Refer to Table 20 for further details.
2. The Morpho MC connectors cannot be operated simultaneously with Motor2 on MC connector V2.
3. If PA9 is used as VCP1_TX, Morpho MC CN7 pin 35 cannot be used

6.11 User LEDs

6.11.1 Description

Three general-purpose color LEDs (LD1, LD2, and LD3) are available as light indicators. Each LED is on when a low level is applied to the corresponding I/O ports.

Green LED LD1 (PF3) is connected to the STM32G473QET6 by default.

The two other user LEDs, the red LED LD2 (PD6) and the yellow LED LD3 (PD5) are shared with VCP2 USART of STLINK-V3EC but the default setting is LED.

6.11.2 LED interface

Table 17 describes the hardware IO configuration for the LED interface.

Table 17. Hardware I/O configuration for the LED interface

I/O	Hardware	Setting[1]	Configuration
PF3	-	**-**	**PF3 is connected to the green LED LD1. Active Low**
PD6	SB49	**OFF**	**PD6 is connected to the red LED LD2. Active Low**
		ON	PD6 is sharing with VCP2_RX
PD5	-	-	**PD5 is connected to yellow LED LD3. Active Low** Sharing with VCP2_TX by default because LED and RX are both output signals.

1. *The default configuration is in bold.*

6.11.3 I/O restriction to other features

Caution: LD2 and LD3 are not showing correctly when PD5 and PD6 are used as VCP2 signals.

6.12 Physical input devices: buttons

6.12.1 Description

The B-G473E-ZEST1S Discovery board provides two buttons for physical human control. These are:

- A reset button (B1)
- A tamper/user button (B2)

6.12.2 Physical input I/O interface

Table 18 describes the hardware IO configuration for the physical user interface.

Table 18. Hardware I/O configuration for the physical user interface

I/O	Hardware	Configuration
PC13	B2	**PC13 connected to the user button B2 (active HIGH)**
PG10-NRST	B1	**Button RESET source (active LOW)**

6.13 Operational amplifier

6.13.1 Description

The B-G473E-ZEST1S Discovery board offers the possibility to test the internal operational amplifier for Motor1 shunt signals. Shunt signals can pass through the internal operational amplifier or enter the ADC input of STM32G473QET6 directly by setting solder bridges.

6.13.2 Operational amplifier interface

Table 19 describes the hardware I/O configuration for the OPAMP interface.

Table 19. Hardware I/O configuration for the OPAMP interface

Amplifier	Hardware	Setting[1]	Configuration
OPAMP3	SB11, SB22, and SB21	**SB11 and SB22 ON** **SB21 OFF**	**Shunt1 through OPAMP3** **INP is PB0, INM is PB2. OUT is PB1**
		SB11 and SB22 OFF SB21 ON	Shunt1 does not pass through OPAMP3 and enter ADC input ADC_345_IN8 (PD11) directly.
OPAMP4	SB32, SB35, and SB31	**SB32 and SB35 ON** **SB31 OFF**	**Shunt2 passes through OPAMP4** **INP is PB11, INM is PB10. OUT is PB12**
		SB32 and SB35 OFF SB31 ON	Shunt2 does not pass through OPAMP4 and enter ADC input ADC_345_IN9 (PD12) directly.
OPAMP5	SB38, SB39, and SB37	**SB38 and SB39 ON** **SB37 OFF**	**Shunt3 through OPAMP5** **INP is PB14, INM is PB15. OUT is PA8**
		SB38 and SB39 OFF SB37 ON	Shunt2 does not pass OPAMP4 and enter ADC input ADC_345_IN11 (PD14) directly.

1. *The default configuration is in bold.*

6.14 Analog input, potentiometer

6.14.1 Description

The B-G473E-ZEST1S Discovery board provides an onboard analog-to-digital converter ADC. The on-board potentiometer is connected to PA3 ADC_1_IN4.

6.14.2 Potentiometer

Table 20 describes the hardware I/O configuration for the potentiometer.

Table 20. Hardware I/O configuration for the potentiometer

I/O	Hardware	Setting[1]	Configuration
PA3	SB26, SB36, and SB82	SB26 ON SB36 and SB82 OFF	PA3 is used as a potentiometer input (ADC_1_IN4)
		SB26 OFF **SB36 and SB82 ON**	**PA3 is used for motor2 Resolver_Sin or ADC signal on Morpho MC CN7 pin 30**

1. *The default configuration is in bold.*

6.14.3 I/O restriction to other features

Caution: The potentiometer cannot be used if PA3 is used for the Motor2 Resolver_Sin or ADC signal on Morpho MC CN7 pin 30.

7 B-G473E-ZEST1S product information

7.1 Product marking

The stickers located on the top or bottom side of all PCBs provide product information:

- First sticker: product order code and product identification, generally placed on the main board featuring the target device.
  Example:

  Product order code
  Product identification

- Second sticker: board reference with revision and serial number, available on each PCB.
  Example:

  MBxxxx-Variant-yzz
  syywwxxxxx

On the first sticker, the first line provides the product order code, and the second line the product identification.

On the second sticker, the first line has the following format: *"MBxxxx-Variant-yzz"*, where *"MBxxxx"* is the board reference, *"Variant"* (optional) identifies the mounting variant when several exist, *"y"* is the PCB revision, and *"zz"* is the assembly revision, for example B01. The second line shows the board serial number used for traceability.

Parts marked as *"ES"* or *"E"* are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

"ES" or *"E"* marking examples of location:

- On the targeted STM32 that is soldered on the board (for an illustration of STM32 marking, refer to the STM32 datasheet *Package information* paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck, or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a *"U"* marking option at the end of the standard part number and is not available for sales.

To use the same commercial stack in their applications, the developers might need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

7.2 B-G473E-ZEST1S product history

Table 21. Product history

Order code	Product identification	Product details	Product change description	Product limitations
B-G473E-ZEST1S	BG473EZEST$AT1	MCU: • STM32G473QET6 silicon revision "X"	Initial revision	No limitation
		MCU errata sheet: • *STM32G471xx/473xx/474xx/483xx/484xx device errata* (ES0430)		
		Board: • MB1811-G473QE-B01 (main board)		
	BG473EZEST$AT2	MCU: • STM32G473QET6 silicon revision "X"	Board version updated	No limitation
		MCU errata sheet: • *STM32G471xx/473xx/474xx/483xx/484xx device errata* (ES0430)		
		Board: • MB1811-G473QE-B02 (main board)		

7.3 Board revision history

Table 22. Board revision history

Board reference	Board variant and revision	Board change description	Board limitations
MB1811 (main board)	MB1811-G473QE-B01	Initial revision	No limitation
	MB1811-G473QE-B02	C68, C71, and C75 (filtering on voltage measurement) are updated from 2.2 nF to 100 pF to reduce the delay added by the filters.	No limitation

8 Federal Communications Commission (FCC) and ISED Canada Compliance Statements

8.1 FCC Compliance Statement

Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

Part 15.105

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Responsible party (in the USA)

Terry Blanchard
Americas Region Legal | Group Vice President and Regional Legal Counsel, The Americas
STMicroelectronics, Inc.
750 Canyon Drive | Suite 300 | Coppell, Texas 75019
USA
Telephone: +1 972-466-7845

8.2 ISED Compliance Statement

ISED Canada ICES-003 Compliance Label: *CAN ICES-3 (A) / NMB-3 (A)*.
Étiquette de conformité à la NMB-003 d'ISDE Canada: *CAN ICES-3 (A) / NMB-3 (A)*.

9 CE conformity

9.1 Warning

EN 55032 / CISPR32 (2012) Class A product

Warning: this device is compliant with Class A of EN55032 / CISPR32. In a residential environment, this equipment may cause radio interference.

Avertissement : cet équipement est conforme à la Classe A de la EN55032 / CISPR 32. Dans un environnement résidentiel, cet équipement peut créer des interférences radio.

10 Certification information

B-G473E-ZEST1S was tested and certified with STEVAL-LVLP01 and B-MOTOR-PMSMA1. It is recommended to use STEVAL-LVLP01 and B-MOTOR-PMSMA1 with B-G473E-ZEST1S.

Revision history

Table 23. **Document revision history**

Date	Revision	Changes
14-Mar-2023	1	Initial release.
25-Apr-2023	2	Updated *Table 14* with swapped pins 20 and 21 Added BG473EZEST$AT2 product identification with MB1811-G473QE-B02 board in *Table 21* and *Table 22*
09-Nov-2023	3	Added: • B-MOTOR-PMSMA1 accessories package to Introduction • Section 10 Certification information on the product certification environment

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