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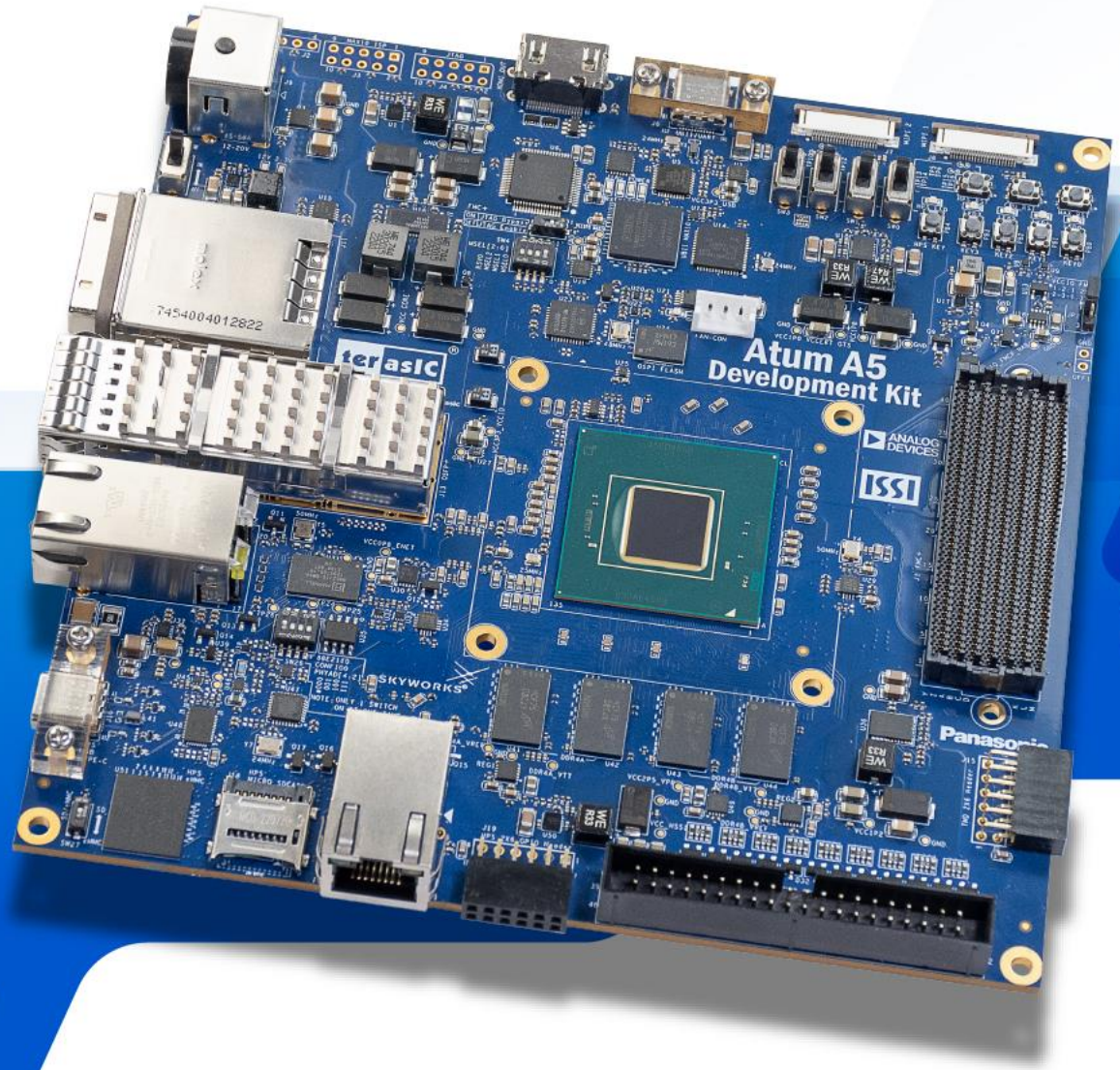
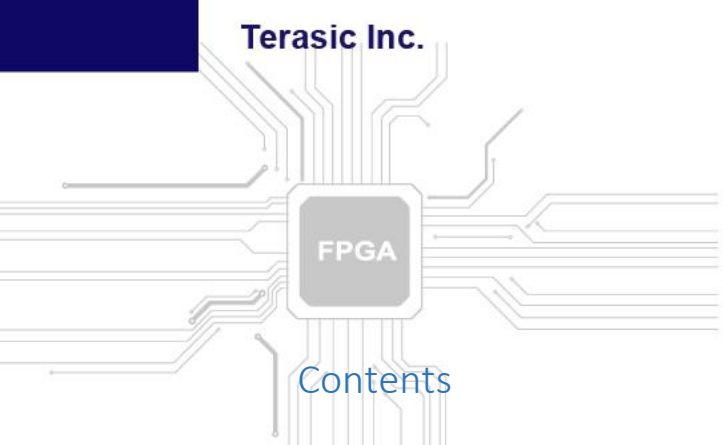
ATUM A5 Board

User manual





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Chapter 1

Overview

This chapter provides an overview of the Atum A5 Development Kit and installation guide.

1.1 General Description

The Atum A5 Development Kit is Terasic's first development kit in the Intel® Agilex™ 5 FPGA portfolio. Powered by the largest Agilex® 5 SoC FPGA with 656K LEs, the Atum A5 Development Kit is an out-of-the-box platform for advanced AI and vision application development.

With a rich set of interfaces ranging from 2.5G Ethernet, high-speed DDR4, QSFP+, PCIe Gen 3x4, FMC+ connectors, to MIPI connector and HDMI, the Atum A5 excels in a wide range of applications, including industrial networking, AI, embedded vision, medical and healthcare, video applications, and various other I/O expansion and high-speed applications!

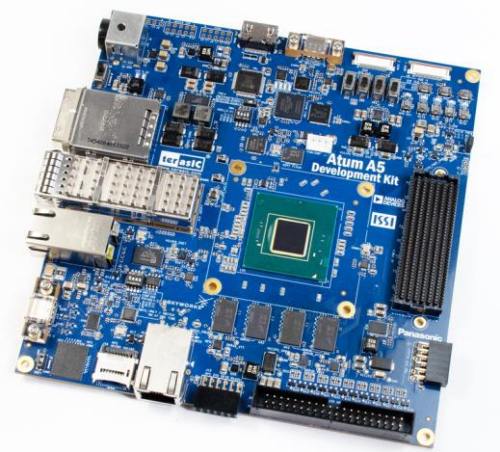


Figure 1-1 Atum A5 board

1.2 Board Layout

The figures below depict the layout of the board and indicate the location of the connectors and key components.

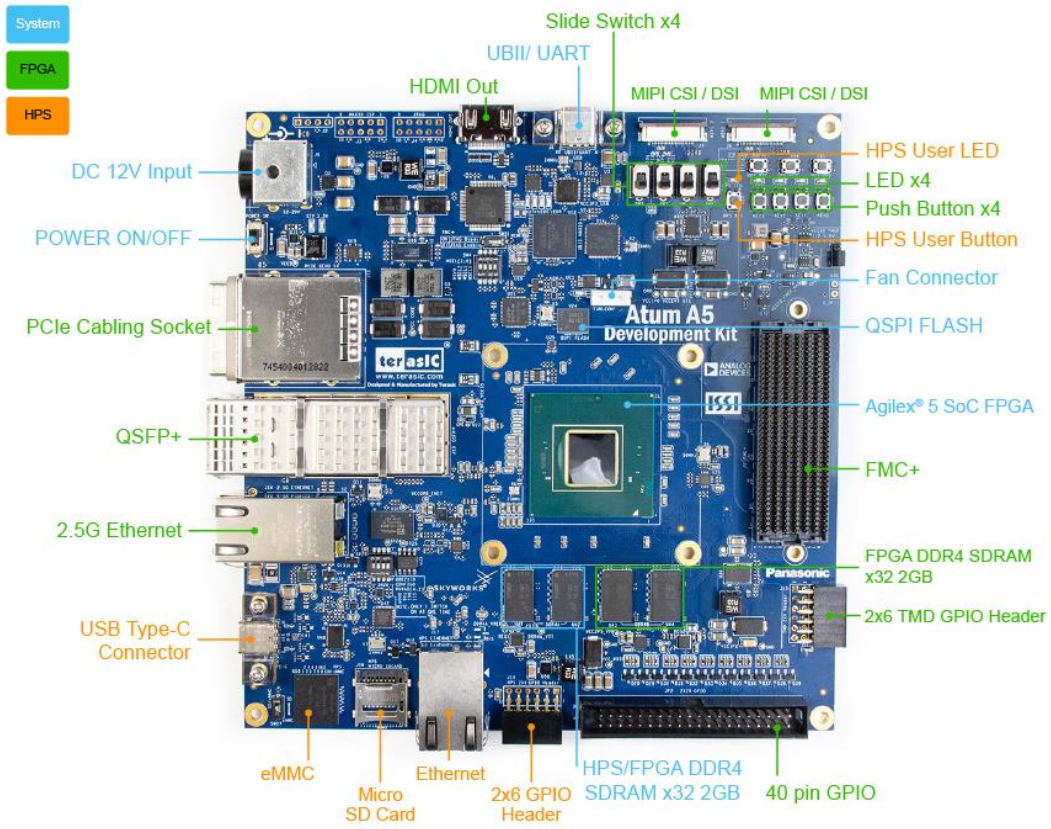


Figure 1-2 Atum A5 board top

1.3 Key Features

The following hardware is implemented on the Atum A5 board:

■ FPGA Device

- Intel® Agilex™ 5 SoC FPGA : A5ED065BB32AE4SR0
  - 650K logic elements (LEs)
  - 31.46 Mbits embedded memory(M20K)
  - 24 transceivers (up to 17.16Gbps)
  - 11,520 18-bit x 19-bit multipliers
  - 1692 DSP blocks

- MIPI D-PHY v2.5

FPGA Configuration

- On-Board USB Blaster II (UB2) for FPGA programming and Debug
- Support ASx4 Configure Mode with 512Mbits QSPI Flash

FPGA Fabric

- HDMI Output Port (Support 1080P)
- DDR4-A: 4GB DDR4 with 32-bit data bus (no ECC). Shared with HPS
- DDR4-B: 4GB DDR4 with 32-bit data bus (no ECC)
- One FMC+ connector with 12 transceivers
- One QSFP+ Port for 40 GbE network interface
- One 2.5G Ethernet Port
- Two 2-lanes MIPI Connector for Camera/Display
- One PCIe Calbing Gen3 x4 Socket
- One 3.3V 2x20 DE-GPIO Header
- One 3.3V 2x6 TMD Header
- User LED x4, Button x4, DIP Switch x4

HPS(Hard Processor System) Fabric

- MicroSD Socket and 8GB eMMC
- DDR4-A: 4GB DDR4 with 32-bit data bus (no ECC). Shared with FPGA
- Gigabit Ethernet PHY + RJ45
- USB 3.1 Gen1 (5Gbps; use 1 transceiver) with USB Type-C connector
- UART to USB Port
- LED x1, Button x1, Cold Reset Button
- One 3.3V 2x6 GPIO Header. Including One I2C Bus

Dashboard System

- Power Monitor
- Temperature Monitor
- Auto Fan Control

1.3. Block Diagram

Figure 1-3 shows the block diagram of the Atum A5 board. To provide maximum flexibility for the users, all key components are connected to the Agilex® SoC FPGA device. Thus, users can configure the FPGA to implement any system design.

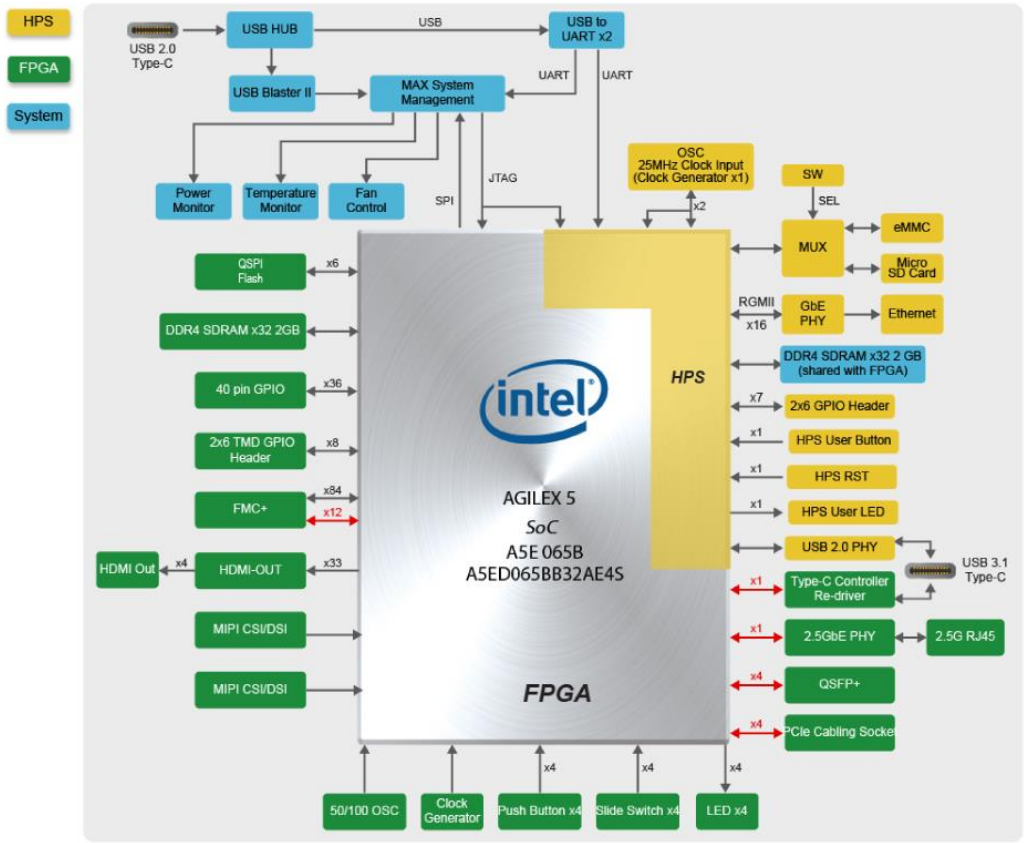


Figure 1-3 Block diagram of the Atum A5 board

1.4. Mechanical Specifications

Figure 1-4 shows the Mechanical Layout of Atum A5 board. The unit of the Mechanical Layout is millimeter (mm).

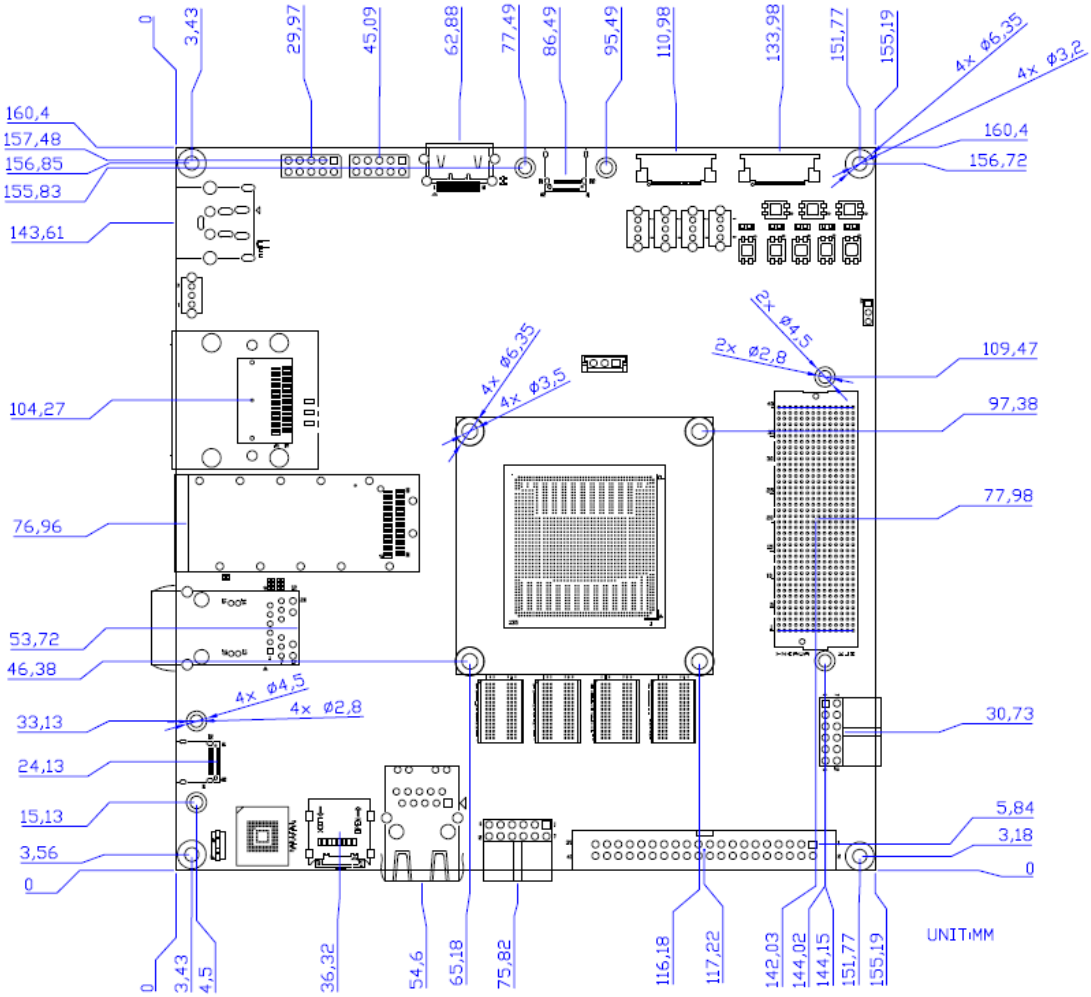


Figure 1-4 Mechanical layout

Chapter 2

Board Component

This chapter introduces all the important components on the Atum A5.

2.1 Configuration Interface

This section describes the configuration mode for Agilex SoC FPGA available on the Atum A5. The peripheral circuits and usage scenarios for each mode will be listed.

As shown in **Figure 2-1**, the mode select pin of the FPGA on the Atum A5 board has been set to **Active Serial (AS) Fast mode** using **FPGA Configure Setup Switch (SW4),** For detailed about SW4, please refer to section 2.2 : *FPGA Configure Setup Switch* part. Thus, the Atum A5 board supports the following configuration modes:

- JTAG Mode (Configure the FPGA using the on-board USB Blaster II).
- Active Serial (AS) Fas mode

Users can use these modes to configure the FPGA or HPS (Hardware Process System) fabric in the Agilex SoC FPGA and make the FPGA to run the user's logic or boot the HPS to run the OS.

Below we will introduce more detailed information of AS mode, as well as other configuration information.

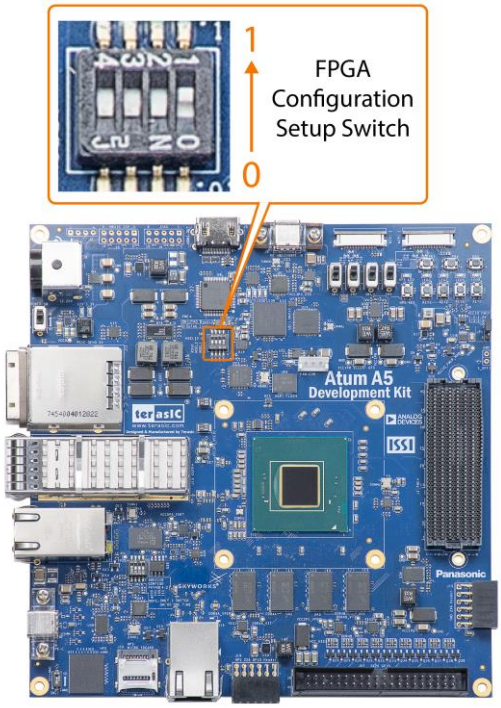


Figure 2-1 The MSEL pin setting

■ Active Serial (Fast) mode

In AS mode, the FPGA's configuration file is stored in the QSPI flash. The Secure Device Manager (SDM) in Agilex SoC FPGA is responsible for the entire AS mode process and interface. The SDM will load the initial configuration firmware from the QSPI flash to configure the FPGA including FPGA I / O and core configuration. HPS part of the boot can also be completed in this mode. **Figure 2-2** shows the architecture of the AS mode of the Atum A5 board.

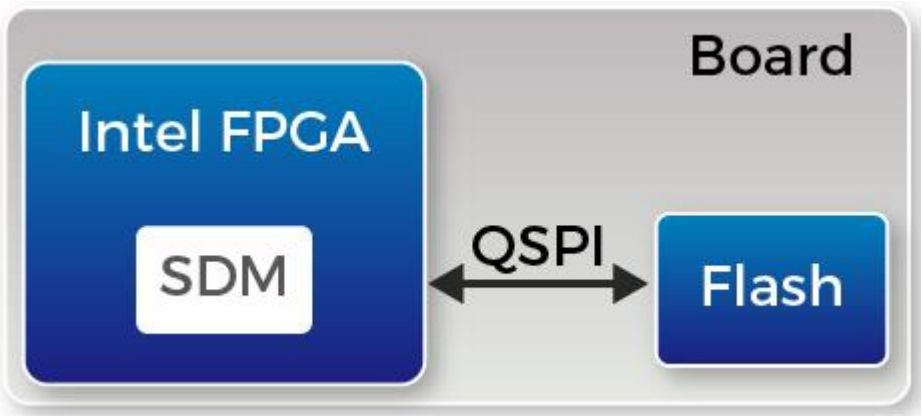


Figure 2-2 AS mode for the Atum A5 board

For more information on the configuration of Agilex SoC FPGAs, please refer to the file: Device Configuration User Guide: Agilex™ 5 FPGAs and SoCs

■ SoC FPGA boot

The boot process for Agilex SoC FPGA can be divided into two different methods:

- FPGA Configuration First Mode
- HPS Boot First Mode

The difference between the two methods is the initial difference between HPS and FPGA fabric after powering on. More details can be found in the user documentation: Hard Processor System Booting User Guide: Agilex 5 SoCs.

The factory setting of the SoC boot of the Atum A5 board is the **FPGA Configuration First Mode**. The architecture is shown in the **Figure 2-3**. Two storage mediums are used. The system needs QSPI flash on Atum A5 as SDM flash for booting.

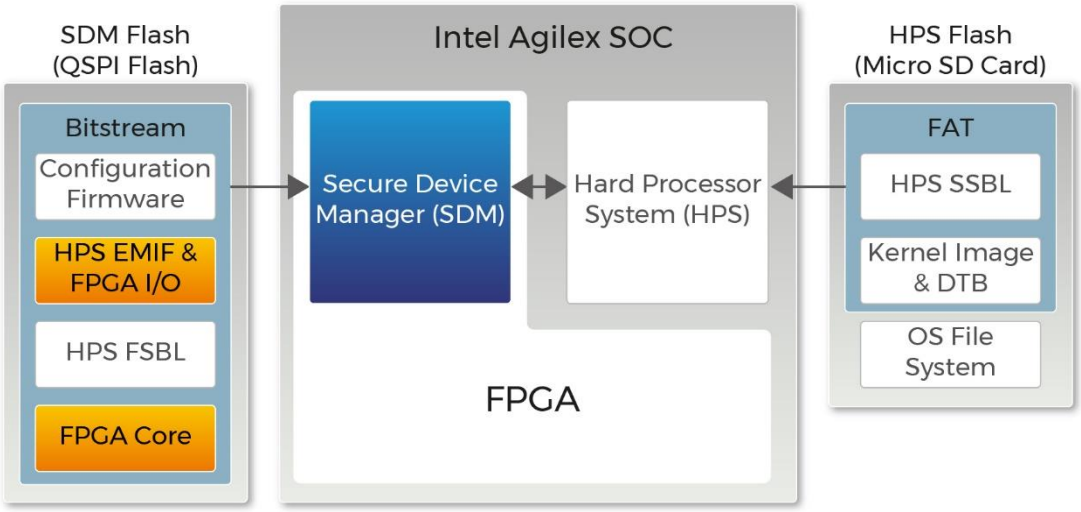


Figure 2-3 FPGA Configuration First Dual SDM and HPS Flash

The QSPI flash memory has the following boot data for the first part of the SoC FPGA configuration:

- Configuration firmware for the SDM
- FPGA I/O and HPS external memory interface (EMIF) I/O configuration data
- FPGA core configuration data
- HPS First-Stage Boot Loader(FSBL) code and FSBL hardware handoff binary data

Meanwhile, Terasic provides the micro SD card with built-in image data as HPS flash, which is used for HPS boot in the later part. The micro SD card stores the following data:

- Second-Stage Boot Loader(SSBL)
- Kernel Image and Device Tree Blob(DTB)
- Operating System

The factory SoC boot process of Atum A5 is summarized as follows:

When the Atum A5 board is powered on, the SDM will read the configuration firmware and complete SDM initial form the QSPI flash according to the MSEL pin setting. Then, the SDM will configure the FPGA I/O and core (full configuration).

After the FPGA is first configured, SDM continues to load the FSBL(First-Stage Boot Loader) from the QSPI flash and transfer it to the HPS on-chip RAM, and releases the HPS reset to let the HPS start using the FSBL hardware handoff file to setup the clocks, HPS dedicated I/Os, and peripherals.

The FSBL then loads the SSBL(Second-Stage Boot Loader) from the Micro SD Card into HPS SDRAM and passes the control to the SSBL. The SSBL enables more advanced peripherals and loads OS into SDRAM.

Finally, the OS boots and applications are scheduled for runtime launch.

■ JTAG Programming

The JTAG interface of the Atum A5 is mainly implemented by the USB Blaster II circuit on the board. For programming by on-board USB Blaster II, the following procedures show how to download a configuration bit stream into the Agilex SoC FPGA:

- Make sure that power is provided to the FPGA board
- Connect your PC to the FPGA board using a micro-USB cable and make sure the USB Blaster II driver is installed on the PC.
- Launch Quartus Prime programmer and make sure the USB Blaster II is detected.
- In Quartus Prime Programmer, add the configuration bit stream file (.sof), check the associated “Program/Configure” item, and click “Start” to start

FPGA programming.

2.2 Setup and Status Components

This section will introduce the use of the switch for setup on the Atum A5 board, as well as a description of the various status LEDs.

■ Status LED

The FPGA development board includes board-specific status LEDs to indicate board status. Please refer to **Table 2-1** for the description of the LED indicators. **Figure 2-4** shows the location of all these status LED.

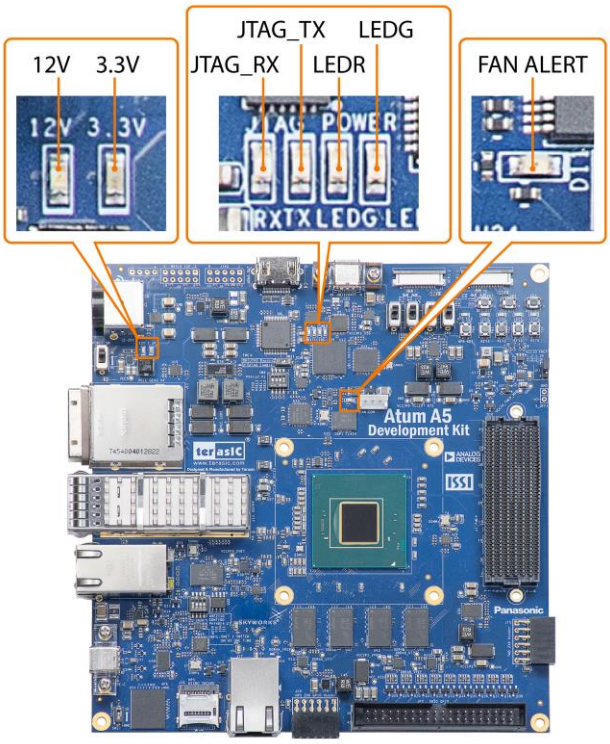


Figure 2-4 Position of the status LED

Table 2-1 Status LED

Board Reference	LED Name	Description
D11	FAN(FAN_ALERT)	Illuminates when the fan is abnormal, such as when the fan speed is different from expected
D9	12V(12-V Power)	Illuminates when 12-V power is active.

D10	3.3V(3.3-V Power)	Illuminates when 3.3-V power is active.
D6	JTAG_TX	Illuminates when the USB Blaster II circuit is transmitting data
D5	JTAG_RX	Illuminates when the USB Blaster II circuit is receiving data
D8	POWER_LEDG	Illuminates when the 3.3V power good and power sequence process finished.
D7	POWER_LEDR	1. Illuminates when the 3.3V power abnormal or power sequence process failed. 2. LED will blink when the following situations occur: (i) the FPGA temperature on the board temperature exceeds 95 degrees. (ii) the power consumption exceeds 160W. (iii) when the current of VCC_CORE exceeds 100A. Also, all the power of the FPGA will be cut off when this LED is blinking.

■ FPGA Configure Setup Switch

The **SW4** switche (see **Figure 2-6**) are used to specify the configuration mode of the FPGA. As currently only AS Fast and JTAG mode are supported. If SW4 is set to AS fast mode. When the board power up, the Secure Device Manager (SDM) in the FPGA will boot from the Quad SPI flash.

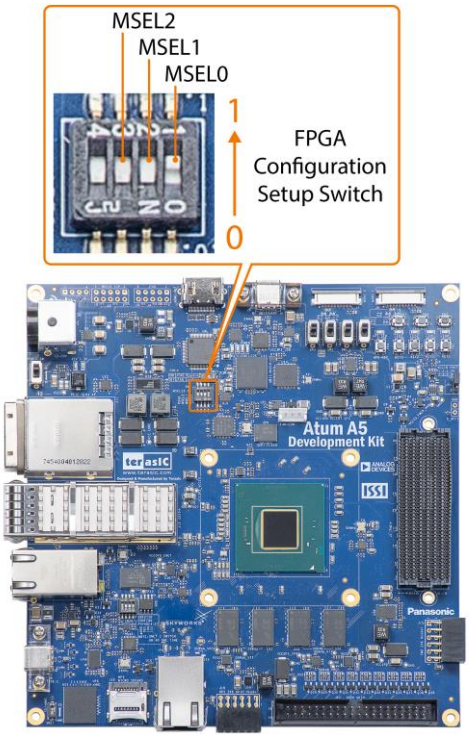


Figure 2-5 Position of slide switch SW4 for FPGA Configuration Mode

Table 2-2 MSEL Settings for supported configuration Scheme of the board

FPGA Configuration Mode	MSEL2	MSEL1	MSEL0
AS Fast (Default)	0	0	1
JTAG	1	1	1

■ FMC+ and HPS JTAG Interface Switch

The JTAG interface switch **SW31** is to set whether the JTAG interface of the FMC + connector is connected to the JTAG chain in the Atum A5 board. The FMC+ connector will **not** be included in the JTAG chain if the switche is set to **ON** position (See **Figure 2-6**).**Table 2-3** lists the setting of the SW31. Note, if the user turns the position on SW31 to the OFF position, but does not connect the JTAG device on the FMC+ connector. The JTAG chain on the Atum A5 board will not be able to form a closed loop and Quartus will not be able to detect the FPGA device.

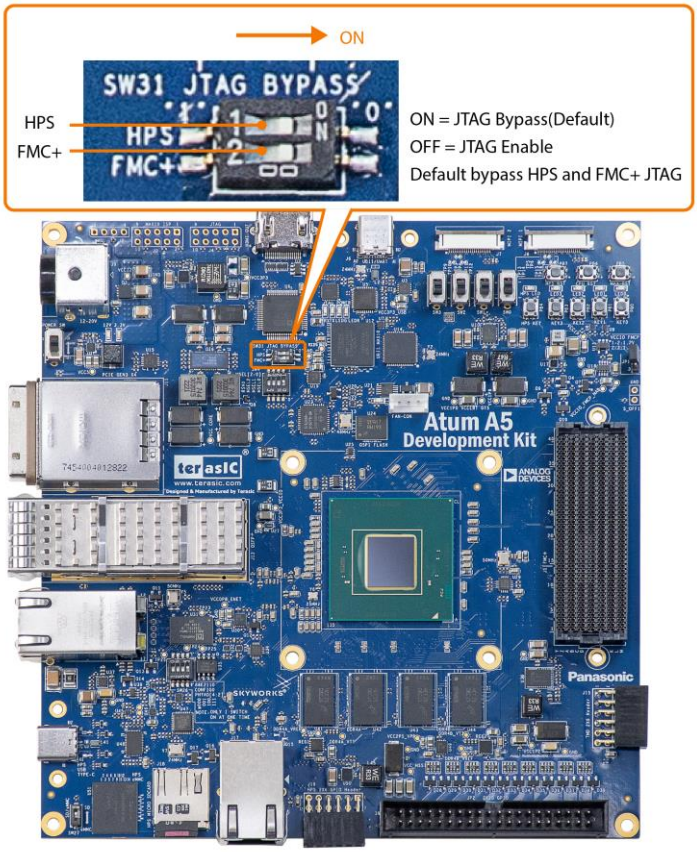


Figure 2-6 Position of slide switches SW31

Table 2-3 SW31 setting

Board Reference	Signal Name	Description	Default
SW31.1	HPS_JTAG_BYPASS_n	**ON** : **Bypass** the JTAG interface of the **HPS** connector into the JTAG chain **OFF**: **Enable** the JTAG interface of the **HPS** connector into the JTAG chain	ON
SW31.2	FMCP_JTAG_BYPASS_n	**ON** : **Bypass** the JTAG interface of the **FMC+** connector into the JTAG chain **OFF**: **Enable** the JTAG interface of the **FMC+** connector into the JTAG chain	ON

■ SDMMC Bus Device Select Switch

The board provides Micro SD Card and on-board eMMC interface for HPS fabric in the FPGA. Users can choose one of them for HPS boot/data/system storage. The switch **SW27** on the board can help the user select which device (Micro SD Card or eMMC) will be used for HPS fabric. **Figure 2-7** shows the position of the SW27. **Table 2-4** list the setting for the JP1

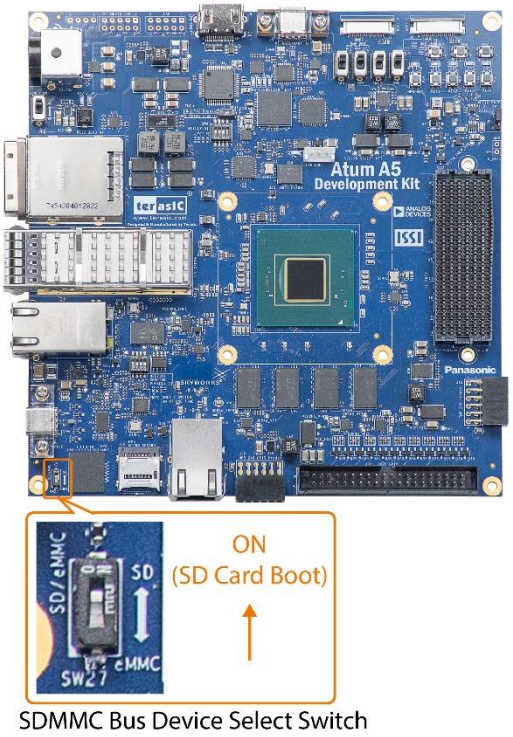


Figure 2-7 Position of slide switches SW27

Table 2-4 SW27 setting

Board Reference	Signal Name	Description	Default
SW27	EMMC_SEL	**ON** : Select SD Card as the storage device for HPS fabric. **OFF**: Select eMMC as the storage device for HPS fabric	ON

■ Ethernet PHY_ADR Setting Switch

The **SW26** switches are used to set bit4~2 of the PHY address(**PHYAD[4:2]**) for the 2.5G Ethernet PHY (Marvell 88E2110). SW26 has a total of four switches, each switch represents a group of PHYAD [4:2] setting value. **Note that only one switch can be set to the on position at a time**. **Figure 2-8** shows the position of this switch on the board. **Table 2-5** list the setting for each switch.

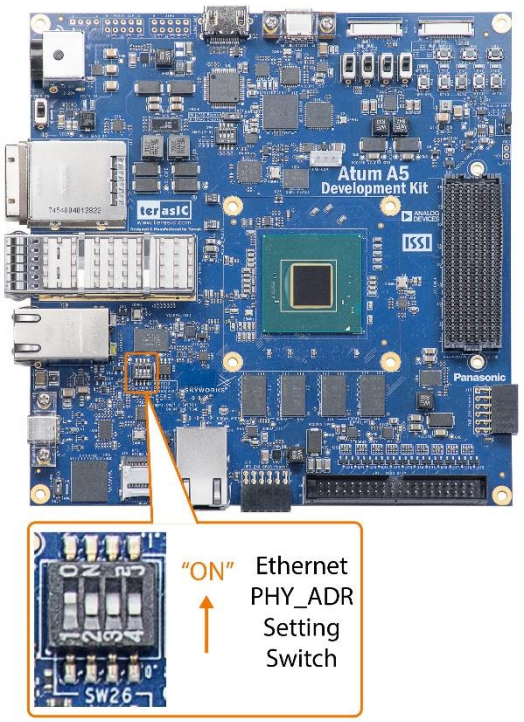


Figure 2-8 Position of slide switches SW26

Table 2-5 SW26 setting

Board Reference	Description	Default
SW26.1	**ON** : Selects 000 for PHYAD[4:2] **OFF**: Deselect 000 for PHYAD[4:2]	ON
SW26.2	**ON** : Selects 001 for PHYAD[4:2] **OFF**: Deselect 001 for PHYAD[4:2]	OFF
SW26.3	**ON** : Selects 010 for PHYAD[4:2] **OFF**: Deselect 010 for PHYAD[4:2]	OFF
SW26.4	**ON** : Selects 111 for PHYAD[4:2] **OFF**: Deselect 111 for PHYAD[4:2]	OFF

■ FMC+ HAB VCCIO Select Header

Some of the FPGA pin's I/O standard connected with the HPC (High Pin Count) part of the **FMC+ connector** can be set to voltages: 1.2V or 1.3V (See **Figure 2-9** and **Table 2-6**). This function can be achieved because the VCCIO power pin of the FPGA bank where these FPGA I/Os are located can adjust the input voltage through the 3 pin header (**JP1**). **Figure 2-10** shows the position of the JP1. **Table 2-7** list the setting for the JP1, user can short 2 pins of the header to modify the voltage level of the VCCIO_FMCP_HAB.

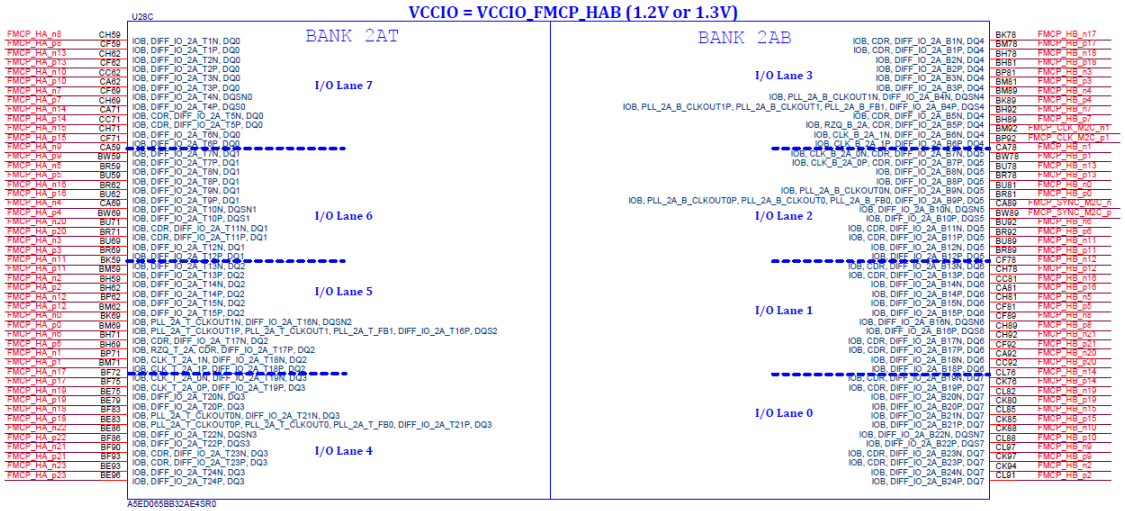


Figure 2-9 HPC FMC+ pin of the FPGA Bank 2AT/2AB

Table 2-6 FPGA I/Os on the FMC+ connector which can be changed I/O standard to 1.2 or 1.3V

FMC Pins which can modify I/O stadnard
FMCP_HA_p[23..0]
FMCP_HA_n[23..0]
FMCP_HB_p[21..0]
FMCP_HB_p[21..0]
FMCP_CLK_M2C_p[1..0]
FMCP_CLK_M2C_n[1..0]
FMCP_SYNC_M2C_p

FMCP_SYNC_M2C_n

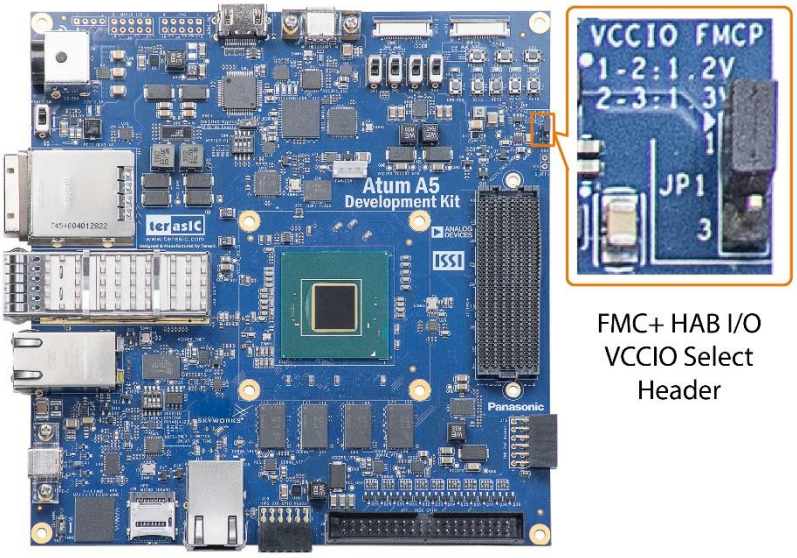


Figure 2-10 FMC+ HAB I/O standard setting headers

Table 2-7 JP1 Setting for FMC+ I/O standard

JP3 Setting	FMC I/O Standard
	1.2V (Default)
	1.3V

2.3 Reset Devices

The board provides 3 reset buttons for different system reset situations (see **Figure 2-11**). These buttons can reset FPGA, System MAX, HPS and FPGA respectively. Please refer to the following **Table 2-8** for details.

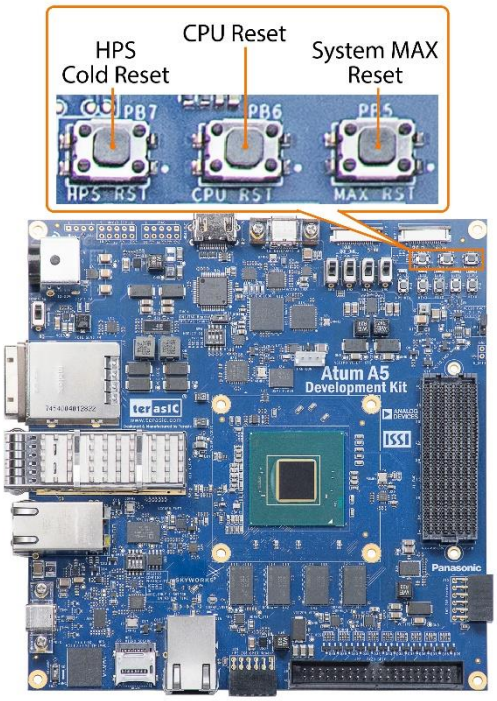


Figure 2-11 Rest devices of the board

Table 2-8 Reset Devices Pin Assignments, Schematic Signal Names, and Functions

Part Number	Schematic Signal Name	I/O Standard	FPGA Pin Number	Application
PB6	CPU_RESET_n	3.3-V LVCMOS	PIN_ BF104	This button can be used for rest FPGA (Need user setting or logic)
PB5	MAX_RESET_n	--	--	For resetting System MAX10
PB7	HPS_COLD_RESET_N	--	--	For resetting System HPS Fabric

2.4 Clock Circuit

The development board includes a 50 MHz TCXO, a 125 MHz OSC, a 150Mhz OSC and two programmable clock generators. **Figure 2-12** shows the default frequencies of on-board all external clocks going to the Agilex SoC FPGA.

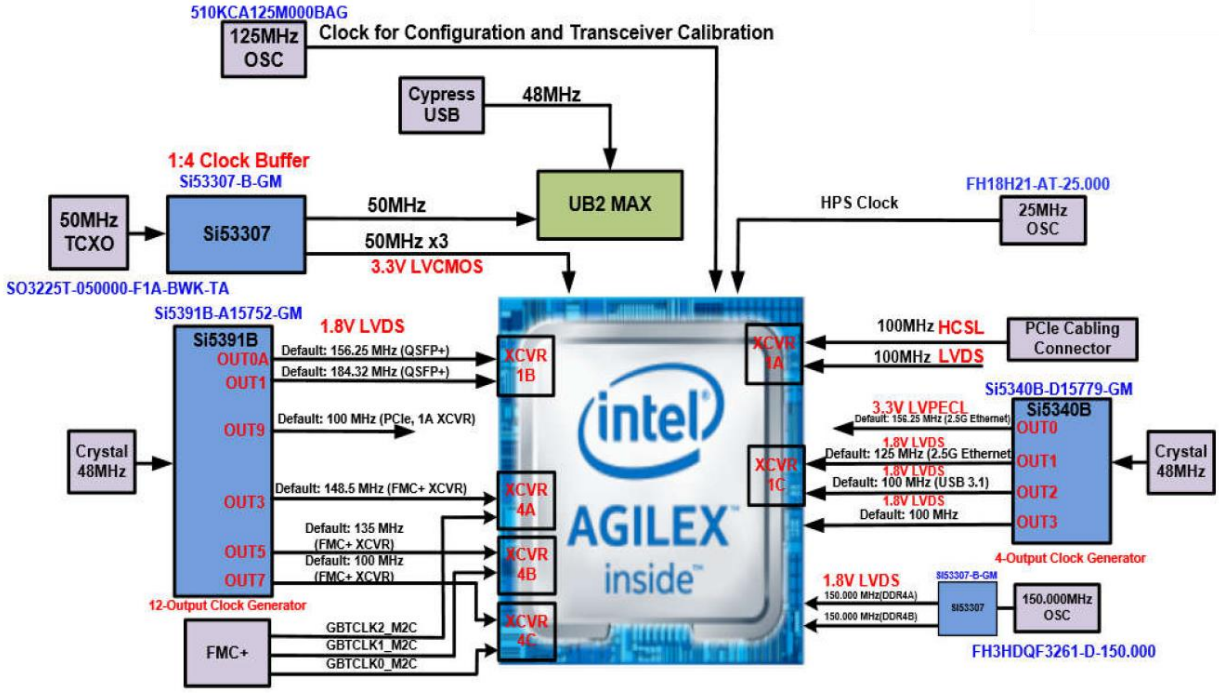


Figure 2-12 Clock circuit of the FPGA Board

A clock buffer is used to duplicate the 50 MHz TCXO output clock, so there are three 50MHz clocks fed into different FPGA banks.

One of the programming clock generator (Si5391B) with ultra low-jitter clock outputs are used to provide special and high-quality clock signals for high-speed transceivers. Through I2C serial interface, the clock generator controllers in the Agilex SoC FPGA can be used to program the Si5391B to generate FMC+ connector, QSFP+ and PCIe reference clocks.

The other programming clock generator (Si5340B) is used to provide a high-speed differential clock source for the Ethernet and USB3.1 interfaces on the board. Users can also modify the output frequency through the I2C interface.

For memory interface, the board provides a 150Mhz clock and fan out it to two

different clocks to the Agilex FPGA via clock buffer (Si53307). The two clocks are used for the reference clock of the two group of the on-board DDR4 SDRAM.

One oscillator provides a 125 MHz clock used as configuration or used as the clock for transceiver calibration. Besides, there is one 25 MHz clock source to use as the HPS input clock.

Table 2-9 Clock source and clock pin to the FPGA

Source	Schematic Signal Name	Default Frequency	I/O Standard	FPGA Pin Number	Application
U29 Si53307	CLK_50_B5A	50.0 MHz	3.3V	PIN_CH128	User application
	CLK_50_B6A		3.3V	PIN_BP22	User application
	CLK_50_B6C		3.3V	PIN_D8	User application
Y8 OSC	OSC_CLK_1	125 MHz	1.8V	PIN_BR102	Clock for configuration and transceiver calibration
Y10 OSC and U34 Clock Buffer	DDR4A_REFCLK_p	150 Mhz	True Differential Signaling	PIN_AB117	DDR4A reference clock
	DDR4B_REFCLK_p	150 Mhz	True Differential Signaling	PIN_AC68	DDR4B reference clock
U23 Si5340B	ENET_88E2110_REFCLK_125M_p	125MHz	High Speed Differential I/O	PIN_AT120	2.5G Ethernet Interface
	HPS_USB3_REFCLK_100M_p	100Mhz	CML	PIN_AP120	HPS USB3.1 Interface
	CLK_100_B2B_p	100 Mhz	True Differential Signaling	PIN_BF68	User application

U57 Si5391B	FMCP_REFCLK0_p	148.5 MHz	Differential	PIN_AT16	FMC+ connector reference clock 0
	FMCP_REFCLK1_p	135 MHz	Differential	PIN_AY16	FMC+ connector reference clock 1
	FMCP_REFCLK2_p	100 MHz	Differential	PIN_BC29	FMC+ connector reference clock 2
	QSFP_REFCLK_p	156.25 MHz	Differential	PIN_AV120	QSFP port reference clock
	CIPRI_REFCLK_p	184.32 MHz	Differential	PIN_AY120	CIPRI clock
	PCIE_OB_REFCLK_p	100 MHz	Differential	PIN_BC111	PCIe on-board reference clock

2.5 General User I/O

This section describes the user I/O interface of the FPGA and HPS fabric. Please note that the HPS and FPGA portions of the device each have their own pins. Pins are not freely shared between the HPS and the FPGA fabric. **Figure 2-13** shows the position of all these components and interface.

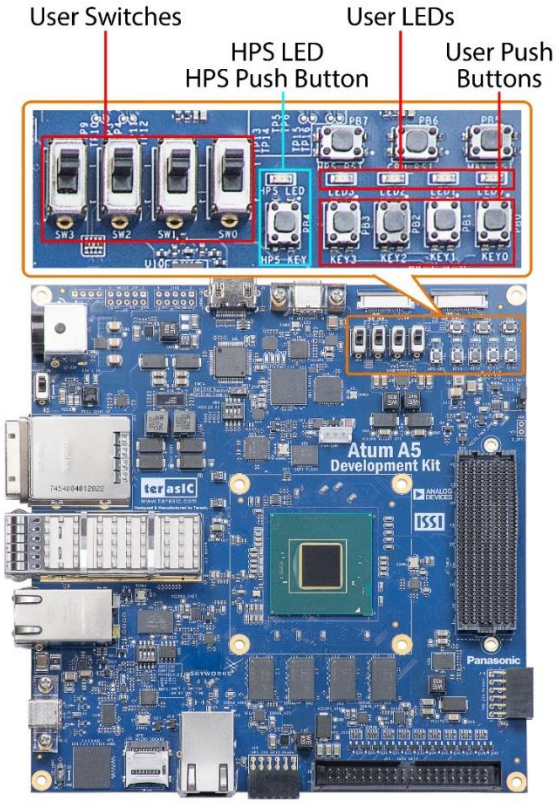


Figure 2-13 Position of all the general user components

■ User Defined Push-buttons

The FPGA board includes four FPGA and one HPS fabric user defined push-buttons that allow users to interact with the Agilex SoC device. Each push-button provides a high logic level or a low logic level when it is not pressed or pressed, respectively. **Table 2-10** lists the board references, signal names and their corresponding Agilex SoC device pin numbers for the push-buttons of the FPGA. **Table 2-11** list the information of the push-button for the HPS fabric.

Table 2-10 Push-button (FPGA) Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
PB0	BUTTON0	High Logic Level when the button is not pressed	3.3 V	PIN_H8
PB1	BUTTON1		3.3 V	PIN_C2
PB2	BUTTON2		3.3 V	PIN_D4
PB3	BUTTON3		3.3 V	PIN_F4

Table 2-11 Push-button (HPS fabric) Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
PB3	HPS_KEY	High Logic Level when the button is not pressed	1.8 V	PIN_ PIN_B134

■ User-Defined Dip Switch

There are four positions slide switches on the FPGA fabric to provide additional FPGA input control. When a position of dip switch is in the DOWN position or the UPPER position, it provides a low logic level or a high logic level to the Agilex SoC FPGA, respectively.

Table 2-12 lists the signal names and their corresponding Agilex SoC device pin numbers.

Table 2-12 Dip Switch Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
SW0	SW0	High logic level when SW in the UPPER position.	3.3 V	PIN_CK4
SW1	SW1		3.3 V	PIN_CH4
SW2	SW2		3.3 V	PIN_K8
SW3	SW3		3.3 V	PIN_F8

■ User-Defined LEDs

The FPGA board consists of 2 FPGA fabric and 1 HPS fabric user-controllable LEDs to allow status and debugging signals to be driven to the LEDs from the designs loaded into the Agilex SoC FPGA. Each LED is driven directly by the FPGA. The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin names on the FPGA that are connected to the LEDs is given in **Table 2-13**. **Table 2-14** list the information of the LED for the HPS fabric.

Table 2-13 User LEDs (FPGA fabric) Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
LED0	LED0	Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	3.3 V	PIN_BF120
LED1	LED1		3.3 V	PIN_B39
LED2	LED2		3.3 V	PIN_B4
LED3	LED3		3.3 V	PIN_A11

Table 2-14 User LEDs (HPS fabric) Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
HPS_LED	HPS_LED	Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	1.8-V	PIN_W135

2.6 2x20 GPIO Expansion Header

The board has one 40-pin expansion headers. The header has 36 user pins connected directly to the Agilex 5 SoC FPGA. It also comes with DC +5V (VCC5), DC +3.3V (VCC3P3), and two GND pins. The maximum power consumption allowed for a daughter card connected to one GPIO ports is shown in **Table 2-15**.

Table 2-15 Voltage and Max. Current Limit of Expansion Header(s)

Supplied Voltage	Max. Current Limit
5V	1A
3.3V	1.5A

Each pin on the expansion headers is connected to two diodes and a resistor for protection against high or low voltage level. Figure 2-14 shows the protection circuitry applied to all 36 data pins. **Table 2-16** shows the pin assignment of the GPIO header.

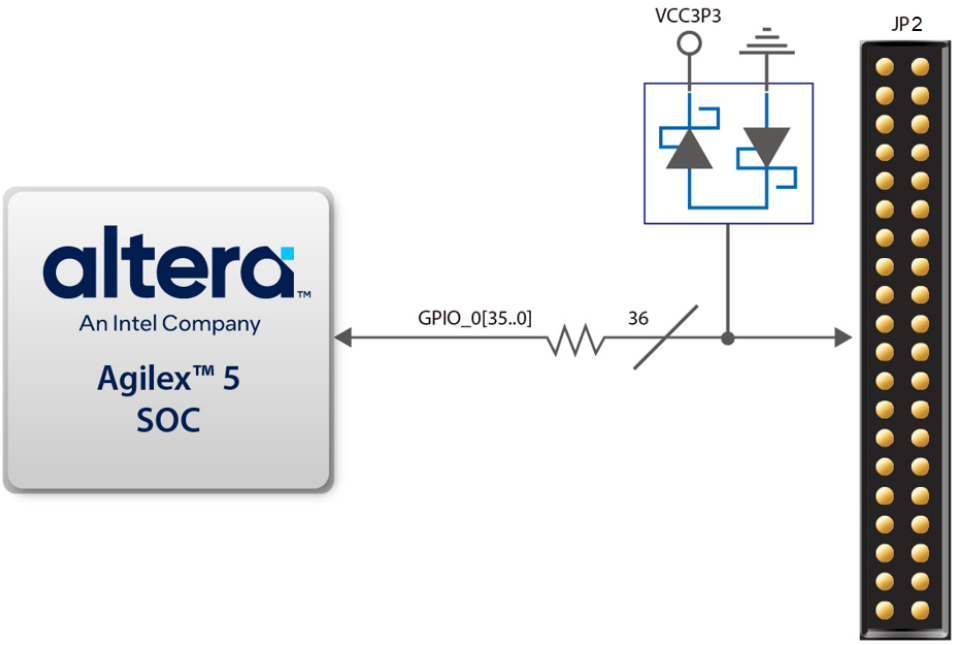


Figure 2-14 Connections between the GPIO header and Agilex 5 SoC FPGA

Table 2-16 Pin Assignment of Expansion Headers

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
GPIO[0]	GPIO Connection[0]	3.3-V	PIN_BK31
GPIO[1]	GPIO Connection[1]	3.3-V	PIN_BU31
GPIO[2]	GPIO Connection[2]	3.3-V	PIN_BF25
GPIO[3]	GPIO Connection[3]	3.3-V	PIN_BU28
GPIO[4]	GPIO Connection[4]	3.3-V	PIN_BR31
GPIO[5]	GPIO Connection[5]	3.3-V	PIN_BU19
GPIO[6]	GPIO Connection[6]	3.3-V	PIN_BR19
GPIO[7]	GPIO Connection[7]	3.3-V	PIN_CJ2
GPIO[8]	GPIO Connection[8]	3.3-V	PIN_BW28
GPIO[9]	GPIO Connection[9]	3.3-V	PIN_BW19
GPIO[10]	GPIO Connection[10]	3.3-V	PIN_BU22
GPIO[11]	GPIO Connection[11]	3.3-V	PIN_BR22
GPIO[12]	GPIO Connection[12]	3.3-V	PIN_BM19
GPIO[13]	GPIO Connection[13]	3.3-V	PIN_BM22
GPIO[14]	GPIO Connection[14]	3.3-V	PIN_BK19
GPIO[15]	GPIO Connection[15]	3.3-V	PIN_BK22
GPIO[16]	GPIO Connection[16]	3.3-V	PIN_BH19

GPIO[17]	GPIO Connection[17]	3.3-V	PIN_BR28
GPIO[18]	GPIO Connection[18]	3.3-V	PIN_BM28
GPIO[19]	GPIO Connection[19]	3.3-V	PIN_BM31
GPIO[20]	GPIO Connection[20]	3.3-V	PIN_BK28
GPIO[21]	GPIO Connection[21]	3.3-V	PIN_BH28
GPIO[22]	GPIO Connection[22]	3.3-V	PIN_BF36
GPIO[23]	GPIO Connection[23]	3.3-V	PIN_BF40
GPIO[24]	GPIO Connection[24]	3.3-V	PIN_BE43
GPIO[25]	GPIO Connection[25]	3.3-V	PIN_BP31
GPIO[26]	GPIO Connection[26]	3.3-V	PIN_CK2
GPIO[27]	GPIO Connection[27]	3.3-V	PIN_CF9
GPIO[28]	GPIO Connection[28]	3.3-V	PIN_CH12
GPIO[29]	GPIO Connection[29]	3.3-V	PIN_CF12
GPIO[30]	GPIO Connection[30]	3.3-V	PIN_BF21
GPIO[31]	GPIO Connection[31]	3.3-V	PIN_BF16
GPIO[32]	GPIO Connection[32]	3.3-V	PIN_BE21
GPIO[33]	GPIO Connection[33]	3.3-V	PIN_BE25
GPIO[34]	GPIO Connection[34]	3.3-V	PIN_BF29
GPIO[35]	GPIO Connection[35]	3.3-V	PIN_BE29

2.7 Micro SD Card and eMMC

The board provides Micro SD Card and on-board eMMC device (SanDisk 8GB :SDINBDG4-8G) for HPS fabric in the FPGA (See Figure 2-15). Users can choose one of them for HPS boot/data/system storage. The switch SW27(See Figure 2-16) on the board can help the user select which device (Micro SD Card or eMMC) will be used for HPS fabric. The Micro SD card socket can provide flexible capacity expansion while eMMC device can support stable and fixed storage solutions. **Table 2-17** lists the pin assignment of Micro SD card socket and eMMC device to the HPS.

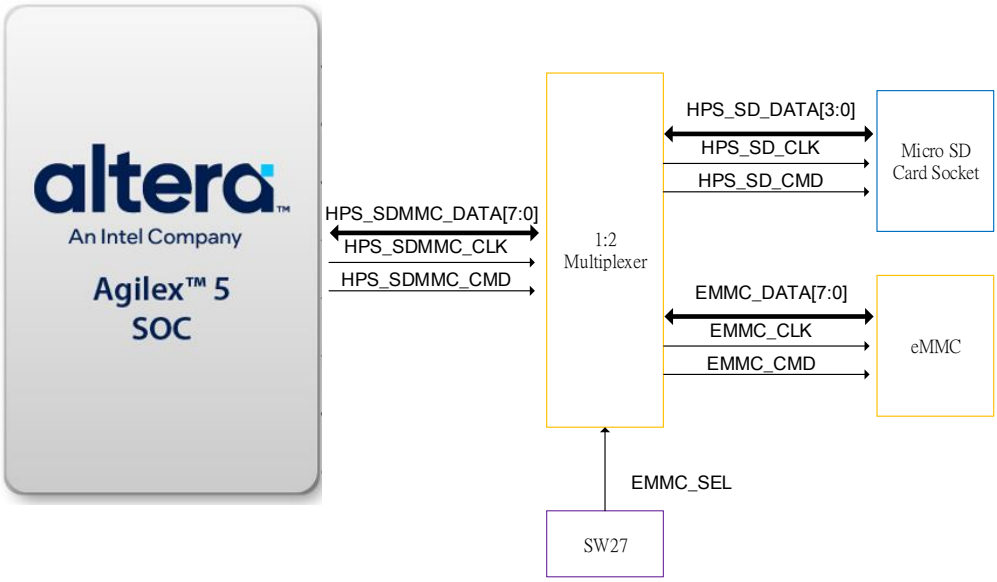
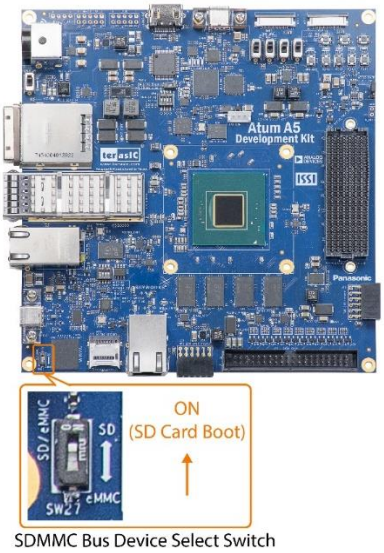


Figure 2-15 Connections between Micro SD card socket, eMMC and Agilex 5 SoC FPGA



SDMMC Bus Device Select Switch

Figure 2-16 SDMMC Bus Device Select Switch

Table 2-17 Micro SD Card Socket Header Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
HPS_SDMMC_CLK	HPS SD/eMMC Clock	1.8-V	PIN_D132
HPS_SDMMC_CMD	HPS SD/eMMC Command Line	1.8-V	PIN_AB132
HPS_SDMMC_DATA[0]	HPS SD/eMMC Data[0]	1.8-V	PIN_E135

HPS_SDMMC_DATA[1]	HPS SD/eMMC Data[1]	1.8-V	PIN_F132
HPS_SDMMC_DATA[2]	HPS SD/eMMC Data[2]	1.8-V	PIN_AA135
HPS_SDMMC_DATA[3]	HPS SD/eMMC Data[3]	1.8-V	PIN_V127

2.8 FMC+ Connector

The board equipped with a FPGA Mezzanine Card Plus(FMC+) connector to provide a mechanism to extend the peripheral-set of an FPGA host board by means of add-on daughter cards, which can address today's high-speed signaling requirements as well as low-speed device interface support. The FMC+ interfaces support JTAG, clock outputs and inputs, high-speed serial I/O (transceivers), and single-ended or differential signaling.

There FMC+ connector on the Atum A5 board is a **High Pin Count (HPC)** size of connector, The HPC connector on Atum A5 board can provides 169 user-define, single-ended signals (80 pair differential I/O) and 12 serial transceiver pairs. **Figure 2-17** is the FPGA I/O connected to the FMC+ connector on the Atum A5 board.

Below we will introduce according to the individual functions of FMC+ connector.

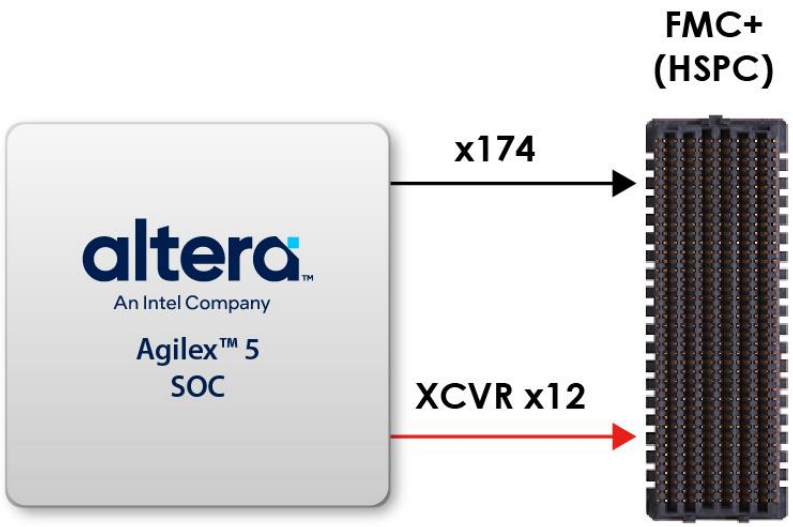


Figure 2-17 FMC+ connector on Atum A5 board

■ Clock Interface

Table 2-18 shows the FPGA clock interface pin placement on the FMC+ connector.

Table 2-18 FMC+ clock input interface distribution

Signal Name	FMC Clock input pin name	FPGA Clock Input Pin Placement	FPGA Pin Assignment
FMCP_CLK_M2C_p0	CLK0_M2C_P	CLK_B_2B_0P	PIN_CH38
FMCP_CLK_M2C_n0	CLK0_M2C_N	CLK_B_2B_0N	PIN_CF38
FMCP_CLK_M2C_p1	CLK1_M2C_P	CLK_B_2A_1P	PIN_BP92
FMCP_CLK_M2C_n1	CLK1_M2C_N	CLK_B_2A_1N	PIN_BM92
FMCP_HA_p1	HA01_P_CC	CLK_T_2A_1P	PIN_BM71
FMCP_HA_n1	HA01_N_CC	CLK_T_2A_1N	PIN_BP71
FMCP_HA_p17	HA17_P	CLK_T_2A_0P	PIN_BP71
FMCP_HA_n17	HA17_N	CLK_T_2A_0N	PIN_BF72
FMCP_HB_p1	HB01_P	CLK_B_2A_0P	PIN_BW78
FMCP_HB_n1	HB01_N	CLK_B_2A_0N	PIN_CA78
FMCP_LA_p0	LA00_P_CC	CLK_T_2B_0P	PIN_BK38
FMCP_LA_n0	LA00_N_CC	CLK_T_2B_0N	PIN_BM38
FMCP_LA_p17	LA17_P_CC	CLK_B_2B_1P	PIN_BR49
FMCP_LA_n17	LA17_N_CC	CLK_B_2B_1N	PIN_BU49

■ Power Supply

The Atum A5 board provides 12V, 3.3V and 1.2V(VADJ) power through FMC+ ports. **Table 2-19** indicates the maximum power consumption for the FMC+ connector.

CAUTION: Before powering on the Atum A5 board with a daughter card, please check to see if there is a short circuit between the power pins and FMC+ FPGA I/O.

Table 2-19 Power Supply of the FMC+

Supplied Voltage	Max. Current Limit
12V	1A
3.3V	3A
1.2V(VADJ)	4A

■ JTAG Chain on FMC+

The JTAG chain on the Atum A5 board supports JTAG interface extension to the FMC+ connector so that the JTAG device on the user's FMC+ daughter card can be joined with JTAG chain on the Atum A5 board. Users can enable this feature through the switch (**SW31**) on the Atum A5 board. In the board's default setting, the JTAG interface of the FMC+ connector is bypassed to keep the Atum A5 board JTAG chain to maintain close loop. For detailed setting, please refer to ***Section 2.2: FMC+ and HPS JTAG Interface Switch***.

■ Adjustable I/O Standards

Some of the FPGA pin's I/O standard connected with the HPC (High Pin Count) part of the FMC+ connector can be set to voltages: 1.2V and 1.3V. This function can be achieved because the VCCIO power pin of the FPGA bank where these FPGA I/Os are located can adjust the input voltage through the 3 pin header (**JP1**). For detailed setting, please refer to Section 2.2: ***FMC+ HAB VCCIO Select Header***.

■ Transceiver Channels Speed

There are 12 E-series GTS transceivers connected to the Agilex SoC FPGA on the FMC+ connector and the maximum transmission speed is **16 G bps**.

■ Component Information of the FMC+ Connector

Table 2-20 shows the manufacture and part numbers of the FMC connector.

Table 2-20 FMC+ Connector Part Number on the Atum A5 board

Connector	Manufacturer and Part Number
FMC+ on the Atum A5 board	Samtec : ASP-184329-01
Mating Connector	Samtec : ASP-184330-01

■ Refernce clock for FMC+ transceivers

There are three clocks are feed to the FPGA for the FMC+ transceivers as the reference clock. These clocks are provides by the programmable clock generator(SI5391B). User can modify the clock frequencies via I2C interface for differential applications.

Table 2-21 FMC+ Reference clock

Source	Schematic Signal Name	Default Frequency	I/O Standard	Agilex Pin Number
U57.OUT3	FMCP_REFCLK0_p	148.5 MHz	LVDS	PIN_AT16
U57.OUT4	FMCP_REFCLK1_p	135 MHz	LVDS	PIN_AY16
U57.OUT5	FMCP_REFCLK2_p	100MHz	LVDS	PIN_BC29

■ FPGA Pin Assignments for FMC+ Connector

Figure 2-18 shows the pin out table of the FMC+ connector on the Atum A5 and **Table 2-22** lists the FMC+ connector pin assignments, signal names and functions.

	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	NC	FMC_VREFB	GND	FMC_VREFA	GND	M2C_FG	GND	C2M_FG	GND	GND	GND	FMCP_PRSNT_M2C_L	GND
2	NC	GND	GND	CLK3_BIDIR_P	FMCP_PRSNT_M2C_L	CLK_M2C_P1	GND	HA_P1	GND	DP_C2M_P0	GND	DP_M2C_P1	GND	NC
3	NC	GND	GND	CLK3_BIDIR_N	GND	CLK_M2C_N1	GND	HA_N1	GND	DP_C2M_N0	GND	DP_M2C_N1	GND	NC
4	GND	NC	CLK2_BIDIR_P	GND	CLK_M2C_P0	GND	HA_P0	GND	GBTCLK_M2C_P0	GND	DP_M2C_P9	GND	NC	GND
5	GND	NC	CLK2_BIDIR_N	GND	CLK_M2C_N0	GND	HA_N0	GND	GBTCLK_M2C_N0	GND	DP_M2C_N9	GND	NC	GND
6	NC	GND	GND	HA_P3	GND	LA_P0	GND	HA_P5	GND	DP_M2C_P0	GND	DP_M2C_P2	GND	NC
7	NC	GND	HA_P2	HA_N3	LA_P2	LA_N0	HA_P4	HA_N5	GND	DP_M2C_N0	GND	DP_M2C_N2	GND	NC
8	GND	NC	HA_N2	GND	LA_N2	GND	HA_N4	GND	LA_P1	GND	DP_M2C_P8	GND	NC	GND
9	GND	NC	GND	HA_P7	GND	LA_P3	GND	HA_P9	LA_N1	GND	DP_M2C_N8	GND	NC	GND
10	NC	GND	HA_P6	HA_N7	LA_P4	LA_N3	HA_P8	HA_N9	GND	LA_P6	GND	DP_M2C_P3	GND	DP_M2C_P10
11	NC	GND	HA_N6	GND	LA_N4	GND	HA_N8	GND	LA_P5	LA_N6	GND	DP_M2C_N3	GND	DP_M2C_N10
12	GND	NC	GND	HA_P11	GND	LA_P8	GND	HA_P13	LA_N5	GND	DP_M2C_P7	GND	DP_M2C_P11	GND
13	GND	NC	HA_P10	HA_N11	LA_P7	LA_N8	HA_P12	HA_N13	GND	GND	DP_M2C_N7	GND	DP_M2C_N11	GND
14	NC	GND	HA_N10	GND	LA_N7	GND	HA_N12	GND	LA_P9	LA_P10	GND	DP_M2C_P4	GND	DP12_M2C_P
15	NC	GND	GND	HA_P14	GND	LA_P12	GND	HA_P16	LA_N9	LA_N10	GND	DP_M2C_N4	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA_P17	HA_N14	LA_P11	LA_N12	HA_P15	HA_N16	GND	GND	DP_M2C_P6	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA_N17	GND	LA_N11	GND	HA_N15	GND	LA_P13	GND	DP_M2C_N6	GND	DP13_M2C_N	GND
18	DP_C2M_P14	GND	GND	HA_P18	GND	LA_P16	GND	HA_P20	LA_N13	LA_P14	GND	DP_M2C_P5	GND	DP14_M2C_P
19	DP_C2M_N14	GND	HA_P21	HA_N18	LA_P15	LA_N16	HA_P19	HA_N20	GND	LA_N14	GND	DP_M2C_N5	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA_N21	GND	LA_N15	GND	HA_N19	GND	LA_P17	GND	GBTCLK_M2C_P1	GND	NC	GND
21	GND	REFCLK_C2M_N	GND	HA_P22	GND	LA_P20	GND	HB_P3	LA_N17	GND	GBTCLK_M2C_N1	GND	NC	GND
22	DP_C2M_P15	GND	HA_P23	HA_N22	LA_P19	LA_N20	HB_P2	HB_N3	GND	LA_P18	GND	DP_C2M_P1	GND	DP15_M2C_P
23	DP_C2M_N15	GND	HA_N23	GND	LA_N19	GND	HB_N2	GND	LA_P23	LA_N18	GND	DP_C2M_N1	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB_P1	GND	LA_P22	GND	HB_P5	LA_N23	GND	DP_C2M_P9	GND	DP_C2M_P10	GND
25	GND	REFCLK_M2C_N	HB_P0	HB_N1	LA_P21	LA_N22	HB_P4	HB_N5	GND	GND	DP_C2M_N9	GND	DP_C2M_N10	GND
26	NC	GND	HB_N0	GND	LA_N21	GND	HB_N4	GND	LA_P26	LA_P27	GND	DP_C2M_P2	GND	DP_C2M_P11
27	NC	GND	GND	HB_P7	GND	LA_P25	GND	HB_P9	LA_N26	LA_N27	GND	DP_C2M_N2	GND	DP_C2M_N11
28	GND	SYNC_M2C_P	HB_P6	HB_N7	LA_P24	LA_N25	HB_P8	HB_N9	GND	GND	DP_C2M_P8	GND	NC	GND
29	GND	SYNC_M2C_N	HB_N6	GND	LA_N24	GND	HB_N8	GND	JTAG_TCK	GND	DP_C2M_N8	GND	NC	GND
30	NC	GND	GND	HB_P11	GND	LA_P29	GND	HB_P13	JTAG_TDI	SCL	GND	DP_C2M_P3	GND	NC
31	NC	GND	HB_P10	HB_N11	LA_P28	LA_N29	HB_P12	HB_N13	JTAG_TDO	SDA	GND	DP_C2M_N3	GND	NC
32	GND	GND	HB_N10	GND	LA_N28	GND	HB_N12	GND	VCC3P3	GND	DP_C2M_P7	GND	NC	GND
33	GND	GND	GND	HB_P15	GND	LA_P31	GND	HB_P19	JTAG_TMS	GND	DP_C2M_N7	GND	NC	GND
34	NC	GND	HB_P14	HB_N15	LA_P30	LA_N31	HB_P16	HB_N19	JTAG_TRST	NC	GND	DP_C2M_P4	GND	NC
35	NC	GND	HB_N14	GND	LA_N30	GND	HB_N16	GND	NC	VCC12	GND	DP_C2M_N4	GND	NC
36	GND	12P0V	GND	HB_P18	GND	LA_P33	GND	HB_P21	VCC3P3	GND	DP_C2M_P6	GND	NC	GND
37	GND	12P0V	HB_P17	HB_N18	LA_P32	LA_N33	HB_P20	HB_N21	GND	VCC12	DP_C2M_N6	GND	NC	GND
38	NC	GND	HB_N17	GND	LA_N32	GND	HB_N20	GND	VCC3P3	GND	GND	DP_C2M_P5	GND	NC
39	NC	GND	GND	NC	GND	VCC10_FMC	GND	VCC10_FMC	GND	VCC3P3	GND	DP_C2M_N5	GND	NC
40	GND	12P0V	NC	GND	VCC10_FMC	GND	VCC10_FMC	GND	VCC3P3	GND	RES0	GND	3P3V	GND

Figure 2-18 FMC+ pin out table

Table 2-22 FMC+ Connector Pin Assignments, Signal Names and Functions

Signal Name	FPGA Pin Number	Description	I/O Standard
FMCP_CLK2_BIDIR_p	PIN_CF49	FMCP data bus	1.2 V
FMCP_CLK2_BIDIR_n	PIN_CH49	FMCP data bus	1.2 V
FMCP_CLK3_BIDIR_p	PIN_BW49	FMCP data bus	1.2 V
FMCP_CLK3_BIDIR_n	PIN_CA49	FMCP data bus	1.2 V
FMCP_CLK_M2C_p[0]	PIN_CH38	Clock from	True Differential Signaling

		mezzanine module to carrier card positive 0	
FMCP_CLK_M2C_n[0]	PIN_CF38	Clock from mezzanine module to carrier card negative 0	True Differential Signaling
FMCP_CLK_M2C_p[1]	PIN_BP92	Clock from mezzanine module to carrier card positive 1	True Differential Signaling
FMCP_CLK_M2C_n[1]	PIN_BM92	Clock from mezzanine module to carrier card negative 1	True Differential Signaling
FMCP_HA_p[0]	PIN_BM69	FMCP HA bank data p0	1.2 V/1.3 *(1)
FMCP_HA_p[1]	PIN_BM71	FMCP HA bank data p1	1.2 V/1.3
FMCP_HA_p[2]	PIN_BH62	FMCP HA bank data p2	1.2 V/1.3
FMCP_HA_p[3]	PIN_BR69	FMCP HA bank data p3	1.2 V/1.3
FMCP_HA_p[4]	PIN_BW69	FMCP HA bank data p4	1.2 V/1.3
FMCP_HA_p[5]	PIN_BU59	FMCP HA bank data p5	1.2 V/1.3
FMCP_HA_p[6]	PIN_BH69	FMCP HA bank data p6	1.2 V/1.3
FMCP_HA_p[7]	PIN_CH69	FMCP HA bank data p7	1.2 V/1.3
FMCP_HA_p[8]	PIN_CF59	FMCP HA bank data p8	1.2 V/1.3

FMCP_HA_p[9]	PIN_BW59	FMCP HA bank data p9	1.2 V/1.3
FMCP_HA_p[10]	PIN_CA62	FMCP HA bank data p10	1.2 V/1.3
FMCP_HA_p[11]	PIN_BM59	FMCP HA bank data p11	1.2 V/1.3
FMCP_HA_p[12]	PIN_BM62	FMCP HA bank data p12	1.2 V/1.3
FMCP_HA_p[13]	PIN_CF62	FMCP HA bank data p13	1.2 V/1.3
FMCP_HA_p[14]	PIN_CC71	FMCP HA bank data p14	1.2 V/1.3
FMCP_HA_p[15]	PIN_CF71	FMCP HA bank data p15	1.2 V/1.3
FMCP_HA_p[16]	PIN_BU62	FMCP HA bank data p16	1.2 V/1.3
FMCP_HA_p[17]	PIN_BF75	FMCP HA bank data p17	1.2 V/1.3
FMCP_HA_p[18]	PIN_BE83	FMCP HA bank data p18	1.2 V/1.3
FMCP_HA_p[19]	PIN_BE79	FMCP HA bank data p19	1.2 V/1.3
FMCP_HA_p[20]	PIN_BR71	FMCP HA bank data p20	1.2 V/1.3
FMCP_HA_p[21]	PIN_BF93	FMCP HA bank data p21	1.2 V/1.3
FMCP_HA_p[22]	PIN_BF86	FMCP HA bank data p22	1.2 V/1.3
FMCP_HA_p[23]	PIN_BE96	FMCP HA bank data p23	1.2 V/1.3
FMCP_HA_n[0]	PIN_BK69	FMCP HA bank data n0	1.2 V/1.3

FMCP_HA_n[1]	PIN_BP71	FMCP HA bank data n1	1.2 V/1.3
FMCP_HA_n[2]	PIN_BH59	FMCP HA bank data n2	1.2 V/1.3
FMCP_HA_n[3]	PIN_BU69	FMCP HA bank data n3	1.2 V/1.3
FMCP_HA_n[4]	PIN_CA69	FMCP HA bank data n4	1.2 V/1.3
FMCP_HA_n[5]	PIN_BR59	FMCP HA bank data n5	1.2 V/1.3
FMCP_HA_n[6]	PIN_BH71	FMCP HA bank data n6	1.2 V/1.3
FMCP_HA_n[7]	PIN_CF69	FMCP HA bank data n7	1.2 V/1.3
FMCP_HA_n[8]	PIN_CH59	FMCP HA bank data n8	1.2 V/1.3
FMCP_HA_n[9]	PIN_CA59	FMCP HA bank data n9	1.2 V/1.3
FMCP_HA_n[10]	PIN_CC62	FMCP HA bank data n10	1.2 V/1.3
FMCP_HA_n[11]	PIN_BK59	FMCP HA bank data n11	1.2 V/1.3
FMCP_HA_n[12]	PIN_BP62	FMCP HA bank data n12	1.2 V/1.3
FMCP_HA_n[13]	PIN_CH62	FMCP HA bank data n13	1.2 V/1.3
FMCP_HA_n[14]	PIN_CA71	FMCP HA bank data n14	1.2 V/1.3
FMCP_HA_n[15]	PIN_CH71	FMCP HA bank data n15	1.2 V/1.3
FMCP_HA_n[16]	PIN_BR62	FMCP HA bank data n16	1.2 V/1.3

FMCP_HA_n[17]	PIN_BF72	FMCP HA bank data n17	1.2 V/1.3
FMCP_HA_n[18]	PIN_BF83	FMCP HA bank data n18	1.2 V/1.3
FMCP_HA_n[19]	PIN_BE75	FMCP HA bank data n19	1.2 V/1.3
FMCP_HA_n[20]	PIN_BU71	FMCP HA bank data n20	1.2 V/1.3
FMCP_HA_n[21]	PIN_BF90	FMCP HA bank data n21	1.2 V/1.3
FMCP_HA_n[22]	PIN_BE86	FMCP HA bank data n22	1.2 V/1.3
FMCP_HA_n[23]	PIN_BE93	FMCP HA bank data n23	1.2 V/1.3
FMCP_HB_p[0]	PIN_BR81	FMCP HB bank data p0	1.2 V/1.3
FMCP_HB_p[1]	PIN_BW78	FMCP HB bank data p1	1.2 V/1.3
FMCP_HB_p[2]	PIN_CL91	FMCP HB bank data p2	1.2 V/1.3
FMCP_HB_p[3]	PIN_BM81	FMCP HB bank data p3	1.2 V/1.3
FMCP_HB_p[4]	PIN_BK89	FMCP HB bank data p4	1.2 V/1.3
FMCP_HB_p[5]	PIN_CF81	FMCP HB bank data p5	1.2 V/1.3
FMCP_HB_p[6]	PIN_BR92	FMCP HB bank data p6	1.2 V/1.3
FMCP_HB_p[7]	PIN_BH89	FMCP HB bank data p7	1.2 V/1.3
FMCP_HB_p[8]	PIN_CH89	FMCP HB bank data p8	1.2 V/1.3

FMCP_HB_p[9]	PIN_CK97	FMCP HB bank data p9	1.2 V/1.3
FMCP_HB_p[10]	PIN_CL88	FMCP HB bank data p10	1.2 V/1.3
FMCP_HB_p[11]	PIN_BR89	FMCP HB bank data p11	1.2 V/1.3
FMCP_HB_p[12]	PIN_CH78	FMCP HB bank data p12	1.2 V/1.3
FMCP_HB_p[13]	PIN_BR78	FMCP HB bank data p13	1.2 V/1.3
FMCP_HB_p[14]	PIN_CK76	FMCP HB bank data p14	1.2 V/1.3
FMCP_HB_p[15]	PIN_CK85	FMCP HB bank data p15	1.2 V/1.3
FMCP_HB_p[16]	PIN_CA81	FMCP HB bank data p16	1.2 V/1.3
FMCP_HB_p[17]	PIN_BM78	FMCP HB bank data p17	1.2 V/1.3
FMCP_HB_p[18]	PIN_BH81	FMCP HB bank data p18	1.2 V/1.3
FMCP_HB_p[19]	PIN_CK80	FMCP HB bank data p19	1.2 V/1.3
FMCP_HB_p[20]	PIN_CC92	FMCP HB bank data p20	1.2 V/1.3
FMCP_HB_p[21]	PIN_CF92	FMCP HB bank data p21	1.2 V/1.3
FMCP_HB_n[0]	PIN_BU81	FMCP HB bank data n0	1.2 V/1.3
FMCP_HB_n[1]	PIN_CA78	FMCP HB bank data n1	1.2 V/1.3
FMCP_HB_n[2]	PIN_CK94	FMCP HB bank data n2	1.2 V/1.3

FMCP_HB_n[3]	PIN_BP81	FMCP HB bank data n3	1.2 V/1.3
FMCP_HB_n[4]	PIN_BM89	FMCP HB bank data n4	1.2 V/1.3
FMCP_HB_n[5]	PIN_CH81	FMCP HB bank data n5	1.2 V/1.3
FMCP_HB_n[6]	PIN_BU92	FMCP HB bank data n6	1.2 V/1.3
FMCP_HB_n[7]	PIN_BH92	FMCP HB bank data n7	1.2 V/1.3
FMCP_HB_n[8]	PIN_CF89	FMCP HB bank data n8	1.2 V/1.3
FMCP_HB_n[9]	PIN_CL97	FMCP HB bank data n9	1.2 V/1.3
FMCP_HB_n[10]	PIN_CK88	FMCP HB bank data n10	1.2 V/1.3
FMCP_HB_n[11]	PIN_BU89	FMCP HB bank data n11	1.2 V/1.3
FMCP_HB_n[12]	PIN_CF78	FMCP HB bank data n12	1.2 V/1.3
FMCP_HB_n[13]	PIN_BU78	FMCP HB bank data n13	1.2 V/1.3
FMCP_HB_n[14]	PIN_CL76	FMCP HB bank data n14	1.2 V/1.3
FMCP_HB_n[15]	PIN_CL85	FMCP HB bank data n15	1.2 V/1.3
FMCP_HB_n[16]	PIN_CC81	FMCP HB bank data n16	1.2 V/1.3
FMCP_HB_n[17]	PIN_BK78	FMCP HB bank data n17	1.2 V/1.3
FMCP_HB_n[18]	PIN_BH78	FMCP HB bank data n18	1.2 V/1.3

FMCP_HB_n[19]	PIN_CL82	FMCP HB bank data n19	1.2 V/1.3
FMCP_HB_n[20]	PIN_CA92	FMCP HB bank data n20	1.2 V/1.3
FMCP_HB_n[21]	PIN_CH92	FMCP HB bank data n21	1.2 V/1.3
FMCP_LA_p[0]	PIN_BK38	FMCP LA bank data p0	1.2 V
FMCP_LA_p[1]	PIN_BE61	FMCP LA bank data p1	1.2 V
FMCP_LA_p[2]	PIN_BF57	FMCP LA bank data p2	1.2 V
FMCP_LA_p[3]	PIN_CK8	FMCP LA bank data p3	1.2 V
FMCP_LA_p[4]	PIN_BF50	FMCP LA bank data p4	1.2 V
FMCP_LA_p[5]	PIN_CK48	FMCP LA bank data p5	1.2 V
FMCP_LA_p[6]	PIN_CK11	FMCP LA bank data p6	1.2 V
FMCP_LA_p[7]	PIN_BE64	FMCP LA bank data p7	1.2 V
FMCP_LA_p[8]	PIN_BE46	FMCP LA bank data p8	1.2 V
FMCP_LA_p[9]	PIN_CF19	FMCP LA bank data p9	1.2 V
FMCP_LA_p[10]	PIN_CF22	FMCP LA bank data p10	1.2 V
FMCP_LA_p[11]	PIN_BM52	FMCP LA bank data p11	1.2 V
FMCP_LA_p[12]	PIN_BP41	FMCP LA bank data p12	1.2 V

FMCP_LA_p[13]	PIN_CL42	FMCP LA bank data p13	1.2 V
FMCP_LA_p[14]	PIN_BH38	FMCP LA bank data p14	1.2 V
FMCP_LA_p[15]	PIN_BH49	FMCP LA bank data p15	1.2 V
FMCP_LA_p[16]	PIN_BK49	FMCP LA bank data p16	1.2 V
FMCP_LA_p[17]	PIN_BR49	FMCP LA bank data p17	1.2 V
FMCP_LA_p[18]	PIN_CK30	FMCP LA bank data p18	1.2 V
FMCP_LA_p[19]	PIN_CK66	FMCP LA bank data p19	1.2 V
FMCP_LA_p[20]	PIN_CK63	FMCP LA bank data p20	1.2 V
FMCP_LA_p[21]	PIN_CK33	FMCP LA bank data p21	1.2 V
FMCP_LA_p[22]	PIN_CA38	FMCP LA bank data p22	1.2 V
FMCP_LA_p[23]	PIN_BR38	FMCP LA bank data p23	1.2 V
FMCP_LA_p[24]	PIN_CC41	FMCP LA bank data p24	1.2 V
FMCP_LA_p[25]	PIN_CH41	FMCP LA bank data p25	1.2 V
FMCP_LA_p[26]	PIN_CK39	FMCP LA bank data p26	1.2 V
FMCP_LA_p[27]	PIN_CK35	FMCP LA bank data p27	1.2 V
FMCP_LA_p[28]	PIN_CC52	FMCP LA bank data p28	1.2 V

FMCP_LA_p[29]	PIN_CF52	FMCP LA bank data p29	1.2 V
FMCP_LA_p[30]	PIN_CL56	FMCP LA bank data p30	1.2 V
FMCP_LA_p[31]	PIN_CL51	FMCP LA bank data p31	1.2 V
FMCP_LA_p[32]	PIN_CK73	FMCP LA bank data p32	1.2 V
FMCP_LA_p[33]	PIN_CK56	FMCP LA bank data p33	1.2 V
FMCP_LA_n[0]	PIN_BM38	FMCP LA bank data n0	1.2 V
FMCP_LA_n[1]	PIN_BE57	FMCP LA bank data n1	1.2 V
FMCP_LA_n[2]	PIN_BF53	FMCP LA bank data n2	1.2 V
FMCP_LA_n[3]	PIN_CL6	FMCP LA bank data n3	1.2 V
FMCP_LA_n[4]	PIN_BE50	FMCP LA bank data n4	1.2 V
FMCP_LA_n[5]	PIN_CL45	FMCP LA bank data n5	1.2 V
FMCP_LA_n[6]	PIN_CL8	FMCP LA bank data n6	1.2 V
FMCP_LA_n[7]	PIN_BF64	FMCP LA bank data n7	1.2 V
FMCP_LA_n[8]	PIN_BF46	FMCP LA bank data n8	1.2 V
FMCP_LA_n[9]	PIN_CC19	FMCP LA bank data n9	1.2 V
FMCP_LA_n[10]	PIN_CH22	FMCP LA bank data n10	1.2 V

FMCP_LA_n[11]	PIN_BP52	FMCP LA bank data n11	1.2 V
FMCP_LA_n[12]	PIN_BM41	FMCP LA bank data n12	1.2 V
FMCP_LA_n[13]	PIN_CK45	FMCP LA bank data n13	1.2 V
FMCP_LA_n[14]	PIN_BH41	FMCP LA bank data n14	1.2 V
FMCP_LA_n[15]	PIN_BH52	FMCP LA bank data n15	1.2 V
FMCP_LA_n[16]	PIN_BM49	FMCP LA bank data n16	1.2 V
FMCP_LA_n[17]	PIN_BU49	FMCP LA bank data n17	1.2 V
FMCP_LA_n[18]	PIN_CL26	FMCP LA bank data n18	1.2 V
FMCP_LA_n[19]	PIN_CL70	FMCP LA bank data n19	1.2 V
FMCP_LA_n[20]	PIN_CL66	FMCP LA bank data n20	1.2 V
FMCP_LA_n[21]	PIN_CL30	FMCP LA bank data n21	1.2 V
FMCP_LA_n[22]	PIN_BW38	FMCP LA bank data n22	1.2 V
FMCP_LA_n[23]	PIN_BU38	FMCP LA bank data n23	1.2 V
FMCP_LA_n[24]	PIN_CA41	FMCP LA bank data n24	1.2 V
FMCP_LA_n[25]	PIN_CF41	FMCP LA bank data n25	1.2 V
FMCP_LA_n[26]	PIN_CL39	FMCP LA bank data n26	1.2 V

FMCP_LA_n[27]	PIN_CL35	FMCP LA bank data n27	1.2 V
FMCP_LA_n[28]	PIN_CA52	FMCP LA bank data n28	1.2 V
FMCP_LA_n[29]	PIN_CH52	FMCP LA bank data n29	1.2 V
FMCP_LA_n[30]	PIN_CL60	FMCP LA bank data n30	1.2 V
FMCP_LA_n[31]	PIN_CK54	FMCP LA bank data n31	1.2 V
FMCP_LA_n[32]	PIN_CL73	FMCP LA bank data n32	1.2 V
FMCP_LA_n[33]	PIN_CL54	FMCP LA bank data n33	1.2 V
FMCP_GBTCLK_M2C_p[0]	PIN_AP16	LVDS input from the installed FMCP card to dedicated reference clock input pin	HCSL
FMCP_GBTCLK_M2C_p[1]	PIN_AV16	LVDS input from the installed FMCP card to dedicated reference clock input pin	HCSL
FMCP_GBTCLK_M2C_p[2]	PIN_BB16	LVDS input from the installed FMCP card to dedicated reference clock input pin	HCSL
FMCP_DP_C2M_p[0]	PIN_AU7	Transmit pair p0 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[1]	PIN_AR7	Transmit pair p1 of	High Speed Differential

		the FPGA transceiver	I/O
FMCP_DP_C2M_p[2]	PIN_AN7	Transmit pair p2 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[3]	PIN_AL7	Transmit pair p3 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[4]	PIN_BE7	Transmit pair p4 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[5]	PIN_BC7	Transmit pair p5 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[6]	PIN_BA7	Transmit pair p6 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[7]	PIN_AW7	Transmit pair p7 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[8]	PIN_BY7	Transmit pair p8 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[9]	PIN_BT7	Transmit pair p9 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[10]	PIN_BL7	Transmit pair p10 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[11]	PIN_BG7	Transmit pair p11 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[0]	PIN_AV1	Receiver pair p0 of	High Speed Differential

		the FPGA transceiver	I/O
FMCP_DP_M2C_p[1]	PIN_AT1	Receiver pair p1 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[2]	PIN_AP1	Receiver pair p2 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[3]	PIN_AM1	Receiver pair p3 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[4]	PIN_BF1	Receiver pair p4 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[5]	PIN_BD1	Receiver pair p5 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[6]	PIN_BB1	Receiver pair p6 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[7]	PIN_AY1	Receiver pair p7 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[8]	PIN_CB1	Receiver pair p8 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[9]	PIN_BV1	Receiver pair p9 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[10]	PIN_BN1	Receiver pair p10 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[11]	PIN_BJ1	Receiver pair p11	High Speed Differential

		of the FPGA transceiver	I/O
FMCP_REFCLK_C2M_p	PIN_BR41	Reference clock from carrier card mezzanine module to positive	DIFFERENTIAL 1.2-V SSTL
FMCP_REFCLK_M2C_p	PIN_CC22	Reference clock from mezzanine module to carrier card positive	True Differential Signaling
FMCP_SCL	PIN_BH118	Management serial clock line	3.3 V
FMCP_SDA	PIN_BK112	Management serial data line	3.3 V
FMCP_RES0	PIN_BF32	Reserved	3.3 V
FMCP_SYNC_C2M_p	PIN_CL14	Synchronize signal from carrier card to mezzanine module positive	DIFFERENTIAL 1.2-V SSTL
FMCP_SYNC_M2C_p	PIN_BW89	Synchronize signal from mezzanine module to carrier card positive	1.2V TRUE DIFFERENTIAL SIGNALING

- *(1): Select by JP1, see section 2.2 : FMC+ HAB VCCIO Select Header .

2.9 USB to UART

One of the USB Type-C connector on Atum A5 board (J6) is connected to three functions: USB blaster II interface, USB to UART for HPS and system MAX10. As shown in Figure **Figure 2-19**, the USB type C connector is connected to a 3-port USB HUB. One of the USB ports is connected to the USB blaster II MAX10 to provide **USB blaster** funcion. The other USB port is connected to the **dual port USB to UART** chip. This chip will provide two USB to UART ports to the board. The first UART bus is connected to

the **HPS UART** controller allows HPS to communicate with the host through UART. This bus will also pass through the USB blaster II MAX10 for 3.3v/1.8v level translator. Another UART interface will be connected to the **System MAX10**. This bus allows users to monitor the status of the board from the host through the UART interface.

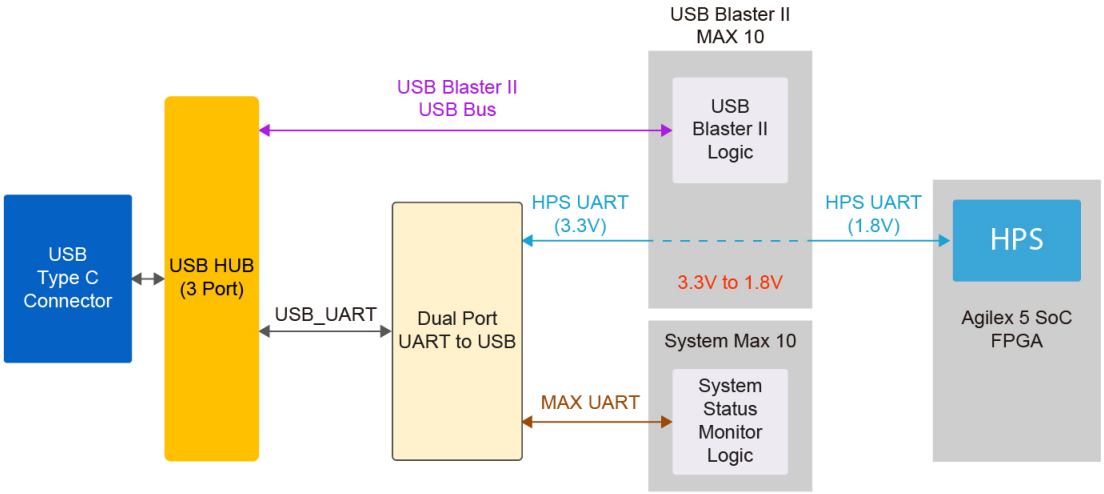


Figure 2-19 Three UART interface on the Atum A5 board

■ USB to UART for HPS Fabric

The board provides a UART interface for users to communicate and transfer data with HPS through the host. This interface is mainly implemented via a dual UART to USB (CP2105). For detailed chip information, please refer to \Datasheets\UART_TO_USB\ of the system CD. It can convert commands and data from the host via USB protocol to the UART interface and send it to HPS. **Figure 2-20** shows the connections between the FPGA(HPS), system MAX10, CP2105 chip, and the USB type-c connector.

Table 2-23 lists the pin assignment of UART interface connected to the HPS.

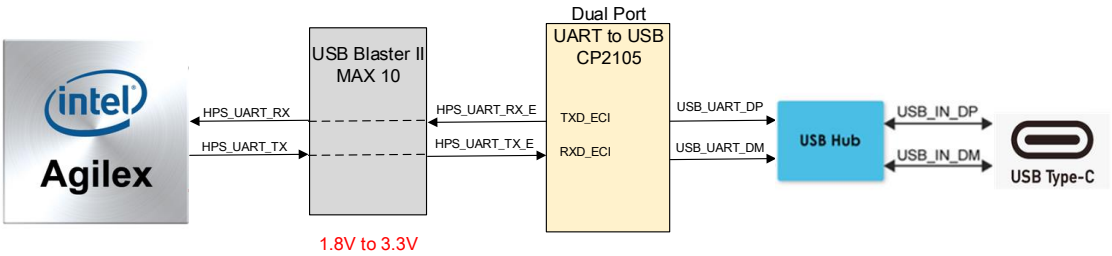


Figure 2-20 Connections between the HPS of Atum A5 and FT232R Chip

Table 2-23 Pin Assignment of HPS UART Interface

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_UART_RX	PIN_AK115	HPS UART Receiver	1.8V
HPS_UART_TX	PIN_W134	HPS UART Transmitter	1.8V

■ USB to UART for System MAX10

The last USB to UART interface is connected with the System MAX10. It allows users to monitor the status of the board from the host through the UART interface. As shown in **Figure 2-21**, the Atum A5 board provides several sensors to monitor the status of the board, such as FPGA temperature, board power monitor, and fan speed status. These interfaces are connected to the System MAX10 FPGA on the board. The board management logic (Dashboard) in the system MAX10 FPGA will monitor these status and perform corresponding control according to the status. For example, when the temperature of the FPGA increases, the system will automatically increase the fan speed to reduce the temperature. When the temperature of the FPGA continues to exceed the working range (such as a fan failure condition), the FPGA power will be cut to protect the board.

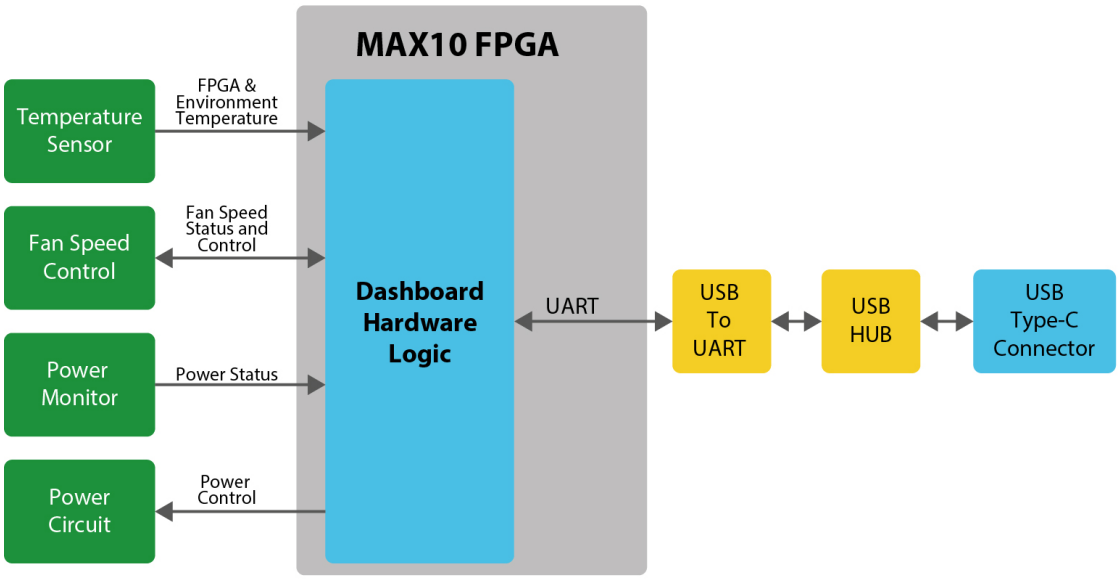


Figure 2-21 Block diagram of the system status interface

2.10 DDR4 SDRAM

The development board supports two independent banks of DDR4 SDRAM (**DDR4A**, and **DDR4B**). Each DDR4 bank can support 32-bit 4GB DDR4-2400 (no ECC). The I/O bank where DDR4A is located can implement Intel Agilex 5 FPGA EMIF IP with the Hard Processor Subsystem (HPS). If no HPS EMIF is used in a system, the DDR4A bank can be used for the EMIF of the FPGA. The DDR4A and DDR4B bank can run at the fastest clock frequency of 1200MHz clock. **Figure 2-22** shows the connections between the DDR4 SDRAM bank and Agilex 5 FPGA.

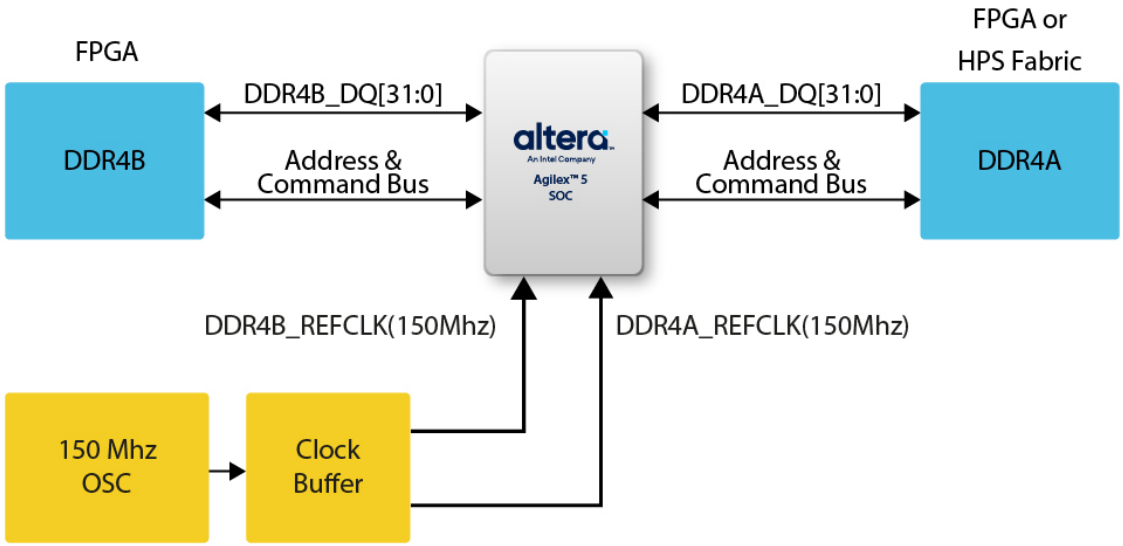


Figure 2-22 Connection between the DDR4 and Agilex 5 FPGA

The pin assignments for DDR4 SDRAM Bank A and Bank B are listed in **Table 2-24** and **Table 2-25** respectively.

Table 2-24 DDR4A Bank Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
DDR4A_DQ0	Data [0]	1.2-V POD	PIN_B128
DDR4A_DQ1	Data [1]	1.2-V POD	PIN_A116
DDR4A_DQ2	Data [2]	1.2-V POD	PIN_B130
DDR4A_DQ3	Data [3]	1.2-V POD	PIN_B116
DDR4A_DQ4	Data [4]	1.2-V POD	PIN_A130
DDR4A_DQ5	Data [5]	1.2-V POD	PIN_B113

DDR4A_DQ6	Data [6]	1.2-V POD	PIN_A128
DDR4A_DQ7	Data [7]	1.2-V POD	PIN_A113
DDR4A_DQ8	Data [8]	1.2-V POD	PIN_AG100
DDR4A_DQ9	Data [9]	1.2-V POD	PIN_Y98 -
DDR4A_DQ10	Data [10]	1.2-V POD	PIN_AC100
DDR4A_DQ11	Data [11]	1.2-V POD	PIN_AG104
DDR4A_DQ12	Data [12]	1.2-V POD	PIN_AC96
DDR4A_DQ13	Data [13]	1.2-V POD	PIN_Y95
DDR4A_DQ14	Data [14]	1.2-V POD	PIN_Y87
DDR4A_DQ15	Data [15]	1.2-V POD	PIN_Y84
DDR4A_DQ16	Data [16]	1.2-V POD	PIN_V98
DDR4A_DQ17	Data [17]	1.2-V POD	PIN_T98
DDR4A_DQ18	Data [18]	1.2-V POD	PIN_P95
DDR4A_DQ19	Data [19]	1.2-V POD	PIN_T95
DDR4A_DQ20	Data [20]	1.2-V POD	PIN_K84
DDR4A_DQ21	Data [21]	1.2-V POD	PIN_M84
DDR4A_DQ22	Data [22]	1.2-V POD	PIN_T84
DDR4A_DQ23	Data [23]	1.2-V POD	PIN_P84
DDR4A_DQ24	Data [24]	1.2-V POD	PIN_H98
DDR4A_DQ25	Data [25]	1.2-V POD	PIN_M98 -
DDR4A_DQ26	Data [26]	1.2-V POD	PIN_K87 -
DDR4A_DQ27	Data [27]	1.2-V POD	PIN_K98
DDR4A_DQ28	Data [28]	1.2-V POD	PIN_F98 -
DDR4A_DQ29	Data [29]	1.2-V POD	PIN_F84 -
DDR4A_DQ30	Data [30]	1.2-V POD	PIN_M87 -
DDR4A_DQ31	Data [31]	1.2-V POD	PIN_D84
DDR4A_DQS0	Data Strobe p[0]	DIFFERENTIAL 1.2-V POD	PIN_B122
DDR4A_DQS1	Data Strobe p[1]	DIFFERENTIAL 1.2-V POD	PIN_AG90
DDR4A_DQS2	Data Strobe p[2]	DIFFERENTIAL 1.2-V POD	PIN_K95
DDR4A_DQS3	Data Strobe p[3]	DIFFERENTIAL 1.2-V POD	PIN_F95
DDR4A_DQS_n0	Data Strobe n[0]	DIFFERENTIAL 1.2-	PIN_A125

		V POD	
DDR4A_DQS_n1	Data Strobe n[1]	DIFFERENTIAL 1.2-V POD	PIN_AG93
DDR4A_DQS_n2	Data Strobe n[2]	DIFFERENTIAL 1.2-V POD	PIN_M95
DDR4A_DQS_n3	Data Strobe n[3]	DIFFERENTIAL 1.2-V POD	PIN_D95
DDR4A_DBI_n0	Data Bus Inversion [0]	1.2-V POD	PIN_B119
DDR4A_DBI_n1	Data Bus Inversion [1]	1.2-V POD	PIN_AC90
DDR4A_DBI_n2	Data Bus Inversion [2]	1.2-V POD	PIN_V87
DDR4A_DBI_n3	Data Bus Inversion [3]	1.2-V POD	PIN_H87
DDR4A_A0	Address [0]	SSTL-12	PIN_T114
DDR4A_A1	Address [1]	SSTL-12	PIN_P114
DDR4A_A2	Address [2]	SSTL-12	PIN_V117
DDR4A_A3	Address [3]	SSTL-12	PIN_T117
DDR4A_A4	Address [4]	SSTL-12	PIN_M114
DDR4A_A5	Address [5]	SSTL-12	PIN_K114
DDR4A_A6	Address [6]	SSTL-12	PIN_V108
DDR4A_A7	Address [7]	SSTL-12	PIN_T108
DDR4A_A8	Address [8]	SSTL-12	PIN_T105
DDR4A_A9	Address [9]	SSTL-12	PIN_P105
DDR4A_A10	Address [10]	SSTL-12	PIN_M105
DDR4A_A11	Address [11]	SSTL-12	PIN_K105
DDR4A_A12	Address [12]	SSTL-12	PIN_AG111
DDR4A_A13	Address [13]	SSTL-12	PIN_Y114
DDR4A_A14	Address [14]/ WE_n	SSTL-12	PIN_AB114
DDR4A_A15	Address [15]/ CAS_n	SSTL-12	PIN_AK107
DDR4A_A16	Address [16]/ RAS_n	SSTL-12	PIN_AK104

DDR4A_BA0	Bank Select [0]	SSTL-12	PIN_AB108
DDR4A_BA1	Bank Select [1]	SSTL-12	PIN_Y105
DDR4A_BG0	Bank Group Select [0]	SSTL-12	PIN_AB105
DDR4A_BG1	Bank Group Select [1]	SSTL-12	PIN_F117
DDR4A_CK	Clock p	DIFFERENTIAL 1.2-V SSTL	PIN_H108
DDR4A_CK_n	Clock n	DIFFERENTIAL 1.2-V SSTL	PIN_F108
DDR4A_CKE	Clock Enable pin	SSTL-12	PIN_F105
DDR4A_CS_n	Chip Select	SSTL-12	PIN_K117
DDR4A_RESET_n	Reset	1.2 V	PIN_H117
DDR4A_ODT	On Die Termination	SSTL-12	PIN_F114
DDR4A_PAR	Command and Address Parity Input	SSTL-12	PIN_K108
DDR4A_ALERT_n	Register ALERT_n output	1.2 V	PIN_Y108
DDR4A_ACT_n	Activation Command Input	SSTL-12	PIN_M117
DDR4A_RZQ	External precision resistor	1.2 V	PIN_AK111
DDR4A_REFCLK_p	DDR4 B port Reference Clock p	LVDS	PIN_AB117

Table 2-25 DDR4B Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
DDR4B_DQ0	Data [0]	1.2-V POD	PIN_A82
DDR4B_DQ1	Data [1]	1.2-V POD	PIN_B70
DDR4B_DQ2	Data [2]	1.2-V POD	PIN_A85
DDR4B_DQ3	Data [3]	1.2-V POD	PIN_A70

DDR4B_DQ4	Data [4]	1.2-V POD	PIN_B82
DDR4B_DQ5	Data [5]	1.2-V POD	PIN_B66
DDR4B_DQ6	Data [6]	1.2-V POD	PIN_B85
DDR4B_DQ7	Data [7]	1.2-V POD	PIN_A66
DDR4B_DQ8	Data [8]	1.2-V POD	PIN_Y58
DDR4B_DQ9	Data [9]	1.2-V POD	PIN_AG64
DDR4B_DQ10	Data [10]	1.2-V POD	PIN_Y47
DDR4B_DQ11	Data [11]	1.2-V POD	PIN_Y44
DDR4B_DQ12	Data [12]	1.2-V POD	PIN_AC61
DDR4B_DQ13	Data [13]	1.2-V POD	PIN_AC64
DDR4B_DQ14	Data [14]	1.2-V POD	PIN_AG61
DDR4B_DQ15	Data [15]	1.2-V POD	PIN_Y55
DDR4B_DQ16	Data [16]	1.2-V POD	PIN_P55
DDR4B_DQ17	Data [17]	1.2-V POD	PIN_T55
DDR4B_DQ18	Data [18]	1.2-V POD	PIN_V58
DDR4B_DQ19	Data [19]	1.2-V POD	PIN_T58
DDR4B_DQ20	Data [20]	1.2-V POD	PIN_P44
DDR4B_DQ21	Data [21]	1.2-V POD	PIN_T44
DDR4B_DQ22	Data [22]	1.2-V POD	PIN_K44
DDR4B_DQ23	Data [23]	1.2-V POD	PIN_M44
DDR4B_DQ24	Data [24]	1.2-V POD	PIN_H47
DDR4B_DQ25	Data [25]	1.2-V POD	PIN_D44
DDR4B_DQ26	Data [26]	1.2-V POD	PIN_H58
DDR4B_DQ27	Data [27]	1.2-V POD	PIN_F47
DDR4B_DQ28	Data [28]	1.2-V POD	PIN_M58
DDR4B_DQ29	Data [29]	1.2-V POD	PIN_F44
DDR4B_DQ30	Data [30]	1.2-V POD	PIN_F58
DDR4B_DQ31	Data [31]	1.2-V POD	PIN_K58
DDR4B_DQS0	Data Strobe p[0]	DIFFERENTIAL 1.2-V POD	PIN_A80
DDR4B_DQS1	Data Strobe p[1]	DIFFERENTIAL 1.2-V POD	PIN_AG57
DDR4B_DQS2	Data Strobe p[2]	DIFFERENTIAL 1.2-V POD	PIN_K55
DDR4B_DQS3	Data Strobe p[3]	DIFFERENTIAL 1.2-V	PIN_F55

		POD	
DDR4B_DQS_n0	Data Strobe n[0]	DIFFERENTIAL 1.2-V POD	PIN_B76
DDR4B_DQS_n1	Data Strobe n[1]	DIFFERENTIAL 1.2-V POD	PIN_AG53
DDR4B_DQS_n2	Data Strobe n[2]	DIFFERENTIAL 1.2-V POD	PIN_M55
DDR4B_DQS_n3	Data Strobe n[3]	DIFFERENTIAL 1.2-V POD	PIN_D55
DDR4B_DBI_n0	Data Bus Inversion [0]	1.2-V POD	PIN_B73
DDR4B_DBI_n1	Data Bus Inversion [1]	1.2-V POD	PIN_AC53
DDR4B_DBI_n2	Data Bus Inversion [2]	1.2-V POD	PIN_V47
DDR4B_DBI_n3	Data Bus Inversion [3]	1.2-V POD	PIN_M47
DDR4B_A0	Address [0]	SSTL-12	PIN_P74
DDR4B_A1	Address [1]	SSTL-12	PIN_T74
DDR4B_A2	Address [2]	SSTL-12	PIN_V77
DDR4B_A3	Address [3]	SSTL-12	PIN_T77
DDR4B_A4	Address [4]	SSTL-12	PIN_M74
DDR4B_A5	Address [5]	SSTL-12	PIN_K74
DDR4B_A6	Address [6]	SSTL-12	PIN_V67
DDR4B_A7	Address [7]	SSTL-12	PIN_T67
DDR4B_A8	Address [8]	SSTL-12	PIN_M65
DDR4B_A9	Address [9]	SSTL-12	PIN_K65
DDR4B_A10	Address [10]	SSTL-12	PIN_T65
DDR4B_A11	Address [11]	SSTL-12	PIN_P65
DDR4B_A12	Address [12]	SSTL-12	PIN_AG79
DDR4B_A13	Address [13]	SSTL-12	PIN_AG72
DDR4B_A14	Address [14]/ WE_n	SSTL-12	PIN_AG75
DDR4B_A15	Address [15]/ CAS_n	SSTL-12	PIN_AG83

DDR4B_A16	Address [16]/ RAS_n	SSTL-12	PIN_AC83
DDR4B_BA0	Bank Select [0]	SSTL-12	PIN_Y74
DDR4B_BA1	Bank Select [1]	SSTL-12	PIN_Y67
DDR4B_BG0	Bank Group Select [0]	SSTL-12	PIN_Y65
DDR4B_BG1	Bank Group Select [1]	SSTL-12	PIN_K77
DDR4B_CK	Clock p	DIFFERENTIAL 1.2-V SSTL	PIN_H67
DDR4B_CK_n	Clock n	DIFFERENTIAL 1.2-V SSTL	PIN_F67
DDR4B_CKE	Clock Enable pin	SSTL-12	PIN_M67
DDR4B_CS_n	Chip Select	SSTL-12	PIN_F77
DDR4B_RESET_n	Reset	1.2 V	PIN_M77
DDR4B_ODT	On Die Termination	SSTL-12	PIN_D74
DDR4B_PAR	Command and Address Parity Input	SSTL-12	PIN_D65
DDR4B_ALERT_n	Register ALERT_n output	1.2 V	PIN_Y77
DDR4B_ACT_n	Activation Command Input	SSTL-12	PIN_H77
DDR4B_RZQ	External precision resistor	1.2 V	PIN_AC79
DDR4B_REFCLK_p	DDR4 B port Reference Clock p	LVDS	PIN_AC68

2.11 USB

The board provides two usb interface to Agilex 5 SoC FPGA. The first is USB 3.1 intrface implemented through FPGA GTS transceiver. The second interface is USB 2.0 OTG interface implemented through SMSC USB3320 (UTMI+ Low Pin Interface (ULPI) for HPS fabric. Both buses are connected to the external device through USB type-c connector. **Figure 2-23** shows the connections of USB interface and FPGA.

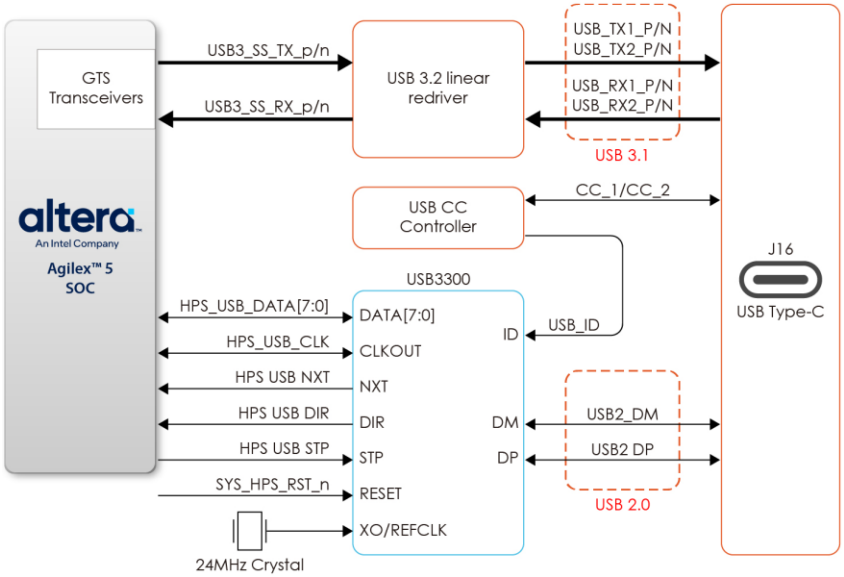


Figure 2-23 Connections between the Atum A5 and USB interface

■ USB 3.1 interface for HPS

This board implements USB3.1 interface through FPGA's GTS transceiver (HPS to FPGA) ,redriver IC and USB type-c connector. Table 2-26 lists the pin assignment of USB3.1 interface connected to the FPGA

Table 2-26 Pin Assignment of USB 3.1 interface

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_USB3_REFCLK_100M_p	PIN_AP120	USB 3.1 interface reference clock	CML
HPS_USB3_SS_TX_p	PIN_AN129	Differential positive output for USB port	HIGH SPEED DIFFERENTIAL I/O
HPS_USB3_SS_TX_n	PIN_AN126	Differential negative output for USB port	
HPS_USB3_SS_RX_p	PIN_AM135	Differential positive input for USB port	
HPS_USB3_SS_RX_n	PIN_AM133	Differential negative input for USB port	
HPS_USB_VBUS_FLT_n	PIN_B56	Low when VCONN over-current fault is detected.	1.2 V
HPS_USB_VBUS_DET	PIN_B60	VBUS detection	1.2 V
HPS_USB_VBUS_CTRL	PIN_A63	To control whether if the VBUS power of Type-C connector J16 should output.	1.2 V
HPS_USB_ID	PIN_A60	Asserted low when the CC pins detect device attachment when port is a source(DFP),ordual-role(DRP)actingassource(DFP).	1.2 V

■ USB 2.0 interface for HPS

The board also provides USB interfaces using the SMSC USB3320 controller. A Microchip USB3320 device is used to interface to a single Type AB Micro-USB connector. This device supports UTMI+ Low Pin Interface (ULPI) to communicate to USB 2.0 controller in HPS. As defined by OTG mode, the PHY can operate in Host or Device modes.Table 2-27 lists the pin assignment of USB2.0 interface connected to the FPGA

Table 2-27 Pin Assignment of USB 2.0 interface

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_USB_CLK	PIN_P132	60MHz Reference Clock Output	1.8V
HPS_USB_DATA[0]	PIN_AD135	HPS USB_DATA[0]	1.8V
HPS_USB_DATA[1]	PIN_M132	HPS USB_DATA[1]	1.8V
HPS_USB_DATA[2]	PIN_K132	HPS USB_DATA[2]	1.8V
HPS_USB_DATA[3]	PIN_AG129	HPS USB_DATA[3]	1.8V
HPS_USB_DATA[4]	PIN_J134	HPS USB_DATA[4]	1.8V
HPS_USB_DATA[5]	PIN_AG120	HPS USB_DATA[5]	1.8V
HPS_USB_DATA[6]	PIN_G134	HPS USB_DATA[6]	1.8V
HPS_USB_DATA[7]	PIN_G135	HPS USB_DATA[7]	1.8V
HPS_USB_DIR	PIN_J135	Direction of the Data Bus	1.8V
HPS_USB_NXT	PIN_AD134	Throttle the Data	1.8V
HPS_USB_STP	PIN_L135	Stop Data Stream on the Bus	1.8V

2.12 Gigabit Ethernet

This board provides two Ethernet ports for users. The first is a Gigabit Ethernet port connected to the Micrel KSZ9031RN PHY and provided to HPS Fabric. The other is a 2.5G Ethernet port connected to the FPGA through the Marvell 88E1512 PHY. Below Here is the detailed information about these two ports.

■ Gigabit Ethernet Port for HPS

The board supports Gigabit Ethernet transfer by an external Micrel KSZ9031RN PHY chip and HPS Ethernet MAC function. The KSZ9031RN chip with integrated 10/100/1000 Mbps Gigabit Ethernet transceiver also supports RGMII MAC interface.

Figure 2-24 shows the connections between the HPS, Gigabit Ethernet PHY, and RJ-45 connector.

For more information about the KSZ9031RN PHY chip and its datasheet, as well as the application notes, which are available on the manufacturer's website.

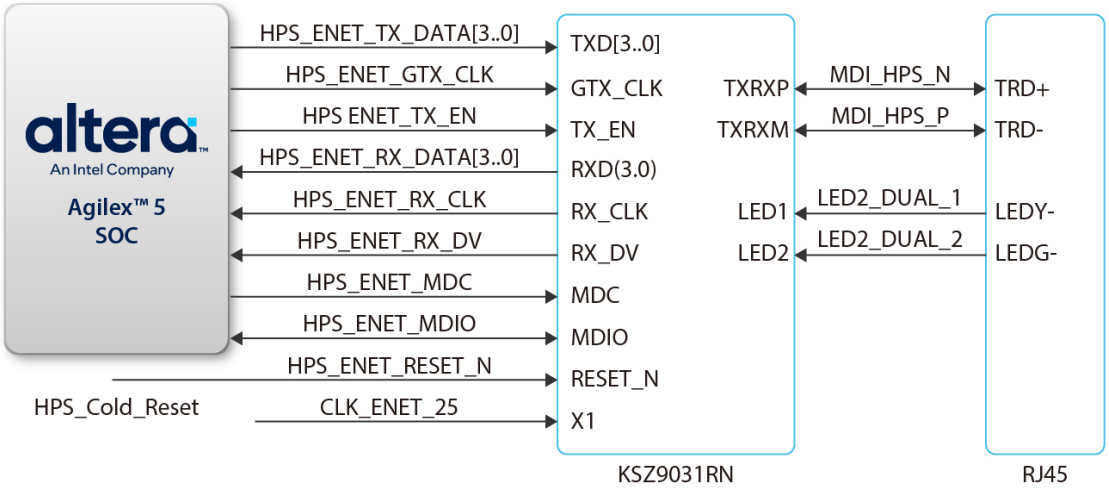


Figure 2-24 Connections between the HPS of Atum A5 and Ethernet PHY

There are two LEDs, a green LED (LEDG) and a yellow LED (LEDY), which represent the status of the Ethernet PHY (KSZ9031RN). The LED control signals are connected to the LEDs on the RJ45 connector. The state and the definition of LEDG and LEDY are listed in **Table 2-28**. For instance, the connection from board to Gigabit Ethernet is established once the LEDG lights on.

Table 2-28 State and Definition of LED Mode Pins

LED (State)		LED (Definition)		Link /Activity
LEDG	LEDY	LEDG	LEDY	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000 Link / No Activity
Toggle	H	Blinking	OFF	1000 Link / Activity (RX, TX)
H	L	OFF	ON	100 Link / No Activity
H	Toggle	OFF	Blinking	100 Link / Activity (RX, TX)
L	L	ON	ON	10 Link/ No Activity
Toggle	Toggle	Blinking	Blinking	Link / Activity (RX, TX)

Table 2-29 Pin Assignment of Gigabit Ethernet PHY

Signal Name	FPGA Pin No	Description	I/O Standard
HPS_ENET_TX_CTL	PIN_K127	GMII and MII transmit enable	1.8V
HPS_ENET_TX_DATA[0]	PIN_K124	MII transmit data[0]	1.8V
HPS_ENET_TX_DATA[1]	PIN_Y127	MII transmit data[1]	1.8V
HPS_ENET_TX_DATA[2]	PIN_F127	MII transmit data[2]	1.8V
HPS_ENET_TX_DATA[3]	PIN_Y124	MII transmit data[3]	1.8V
HPS_ENET_RX_CTL	PIN_AB127	GMII and MII receive data valid	1.8V
HPS_ENET_RX_DATA[0]	PIN_H127	GMII and MII receive data[0]	1.8V
HPS_ENET_RX_DATA[1]	PIN_AB124	GMII and MII receive data[1]	1.8V
HPS_ENET_RX_DATA[2]	PIN_F124	GMII and MII receive data[2]	1.8V
HPS_ENET_RX_DATA[3]	PIN_D124	GMII and MII receive data[3]	1.8V
HPS_ENET_RX_CLK	PIN_M124	GMII and MII receive clock	1.8V
HPS_ENET_MDIO	PIN_R134	Management Data	1.8V
HPS_ENET_MDC	PIN_AG115	Management Data Clock Reference	1.8V
HPS_ENET_TX_CLK	PIN_M127	GMII Transmit Clock	1.8V

■ 2.5 G Ethernet Port for FPGA

The board supports 10M/100M/1G/2.5G Ethernet interface by an external Marvell 88E2110 PHY. Users can implement an Ethernet MAC in the FPGA to implement network transmission. On this board, the 88E2110 PHY works in SGMII mdode by default. At the same time, the user can set the PHY address through SW26. For details, please see section 2.2 Ethernet PHY_ADR Setting Switch. Figure 2-25 shows the connections between the FPGA, 88E2110 PHY, and RJ-45 connector.

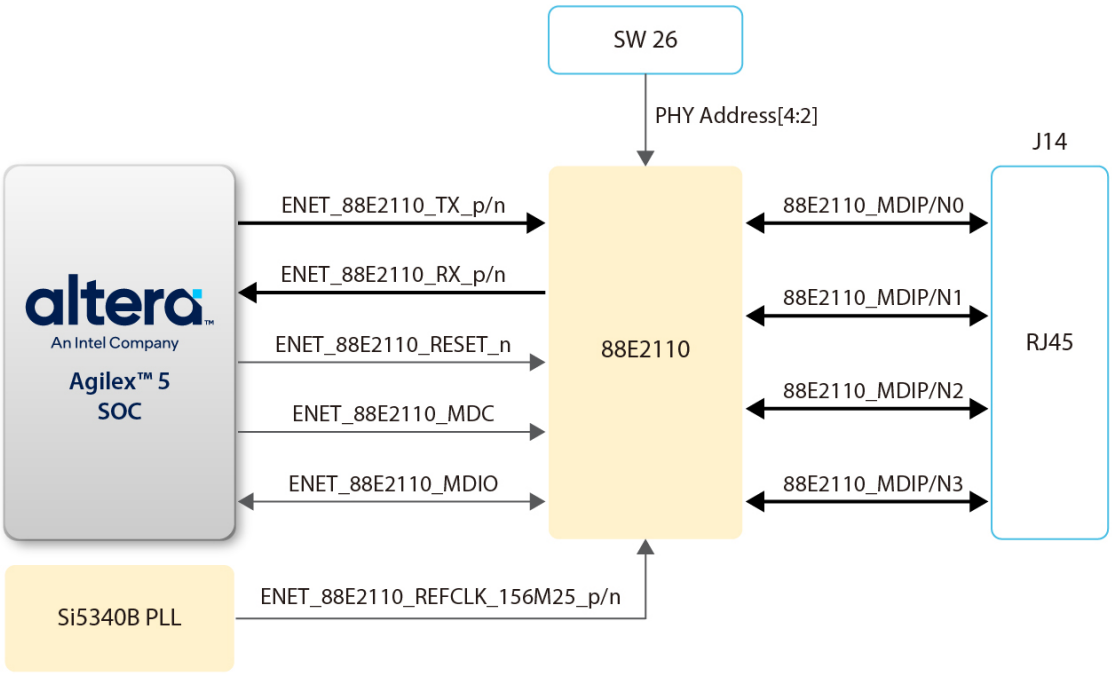


Figure 2-25 Connections between the FPGA and 88E2110 PHY

Table 2-30 Pin Assignment of 88E1512 PHY

Signal Name	FPGA Pin No	Description	I/O Standard
ENET_88E2110_TX_p	PIN_AL129	SGMII transmit data	HIGH SPEED DIFFERENTIAL I/O
ENET_88E2110_TX_n	PIN_AL126	SGMII transmit data	HIGH SPEED DIFFERENTIAL I/O
ENET_88E2110_RX_p	PIN_AK135	SGMII receive data	HIGH SPEED DIFFERENTIAL I/O
ENET_88E2110_RX_n	PIN_AK133	SGMII receive data	HIGH SPEED DIFFERENTIAL I/O
ENET_88E2110_REFCLK_125M_p	PIN_AT120	88E1512 reference clock	CML
ENET_88E2110_INT_n	PIN_A20	Interrupt output pin	3.3V
ENET_88E2110_MDC	PIN_B14	Management data clock reference	3.3V
ENET_88E2110_MDIO	PIN_A14	Management data	3.3V
ENET_88E2110_RESET_n	PIN_B11	88E1512 reset pin	1.8V

2.13 2x6 GPIO Header

The Atum A5 board provides two 2x6 pin GPIO headers (HPS and FPGA for each) to expand the I/O of Agilex SoC FPGA (See Figure 2-26). Each header has numbers of the digital FPGA I/O user pins connected to the Agilex SoC FPGA, two 3.3V power pins and two ground pins.

Note: The appearance of these two headers is same as the Terasic TMD header. However, but due to the different I/O voltage level or pin distribution, they do not support TMD interface daughter cards. The detailed I/O mapping will be introduced below.

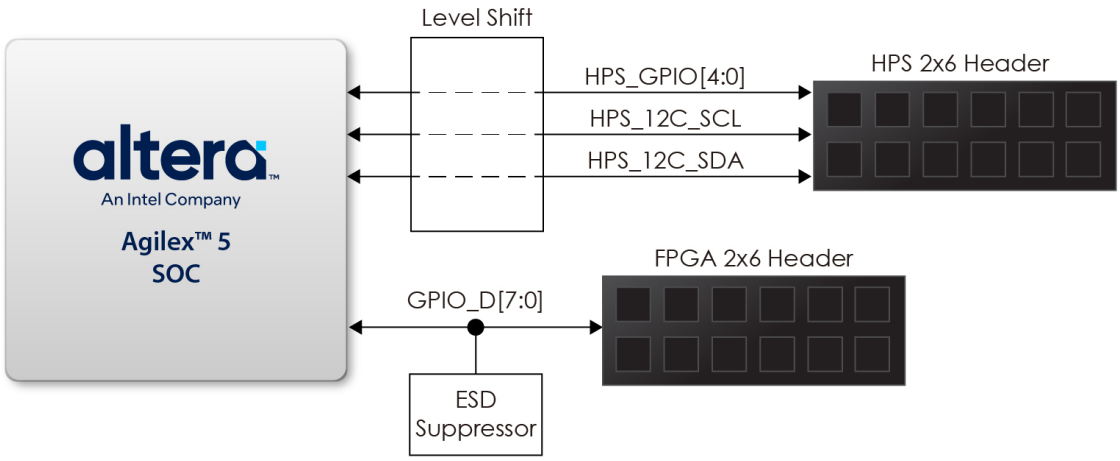


Figure 2-26 Connection between the 2x6 headers and FPGA

■ HPS 2x6 GPIO Header

The HPS 2x6 GPIO header expands 5 GPIO and 1 pair I2C interface of the HPS fabric for users. Users can control these I/Os though the HPS for their application. These HPS I/Os will be converted the voltage level from 1.8v to 3.3V by level translator circuit on the board so that users can connect more interfaces.

Table 2-31 Pin Assignment of USB OTG PHY

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_GPIO[0]	PIN_T132	HPS GPIO0	3.3V(*1)
HPS_GPIO[1]	PIN_AK120	HPS GPIO1	3.3V(*1)
HPS_GPIO[2]	PIN_N134	HPS GPIO2	3.3V(*1)
HPS_GPIO[3]	PIN_N135	HPS GPIO3	3.3V(*1)

HPS_GPIO[4]	PIN_U135	HPS GPIO4	3.3V(*1)
HPS_I2C_SCL	PIN_AL120	HPS I2C Clock	3.3V(*1)
HPS_I2C_SDA	PIN_U134	HPS I2C Data	3.3V(*1)

(*1) Due to the voltage level convert from 1.8v to 3.3V.

■ FPGA 2x6 GPIO Header

The FPGA 2x6 GPIO header expands 8 digital GPIO user pins connected to the Agilex SoC FPGA, two 3.3V power pins and two ground pins. There are two Transient Voltage Suppressor diode arrays used to implement ESD protection for 8 GPIO user pins.

There are two ESD suppressor used to implement ESD protection for 8 GPIO user pins.

Signal Name	FPGA Pin No.	Description	I/O Standard
TMD_D[0]	PIN_F18	FPGA 2x6 header GPIO0	3.3V
TMD_D[1]	PIN_F15	FPGA 2x6 header GPIO1	3.3V
TMD_D[2]	PIN_F27	FPGA 2x6 header GPIO2	3.3V
TMD_D[3]	PIN_F24	FPGA 2x6 header GPIO3	3.3V
TMD_D[4]	PIN_H27	FPGA 2x6 header GPIO4	3.3V
TMD_D[5]	PIN_D24	FPGA 2x6 header GPIO5	3.3V
TMD_D[6]	PIN_H18	FPGA 2x6 header GPIO6	3.3V
TMD_D[7]	PIN_D15	FPGA 2x6 header GPIO7	3.3V

2.14 QSFP+ Port

The development board has one QSFP+ connector that use one transceiver channel each from the Agilex SoC FPGA device. The QSFP+ module receives the serial data from the Agilex SoC FPGA, and transform them to optical signals. A Low-Jitter programmable clock generator (Si5391B) will provide flexible clock for serial transceivers of the FPGA. **Figure 2-27** shows the connections between the QSFP+ and Agilex SoC FPGA.

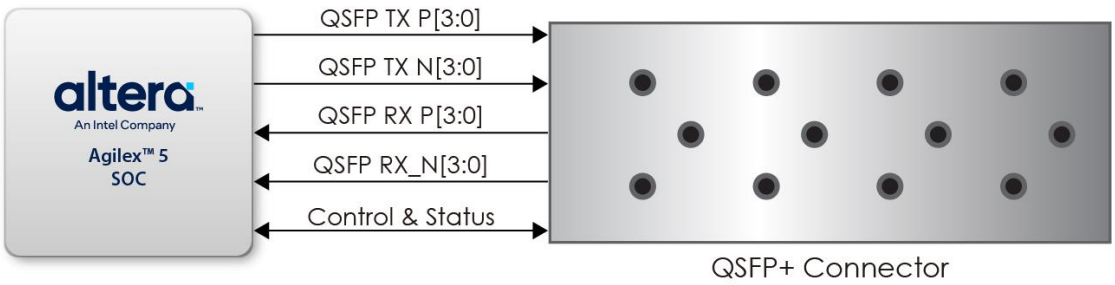


Figure 2-27 Connection between the QSFP+ and FPGA

Table 2-32 lists the QSFP+ pin assignments and signal names relative to the Agilex SoC FPGA.

Table 2-32 QSFP+ Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
QSFP_TX_p[0]	Transmitter data of channel 0	HIGH SPEED DIFFERENTIAL I/O	PIN_BE129
QSFP_TX_p[1]	Transmitter data of channel 1	HIGH SPEED DIFFERENTIAL I/O	PIN_BC129
QSFP_TX_p[2]	Transmitter data of channel 2	HIGH SPEED DIFFERENTIAL I/O	PIN_BA129
QSFP_TX_p[3]	Transmitter data of channel 3	HIGH SPEED DIFFERENTIAL I/O	PIN_AW129
QSFP_TX_n[0]	Transmitter data of channel 0	HIGH SPEED DIFFERENTIAL I/O	PIN_BE126
QSFP_TX_n[1]	Transmitter data of channel 1	HIGH SPEED DIFFERENTIAL I/O	PIN_BC126
QSFP_TX_n[2]	Transmitter data of channel 2	HIGH SPEED DIFFERENTIAL I/O	PIN_BA126

QSFP_TX_n[3]	Transmitter data of channel 3	HIGH SPEED DIFFERENTIAL I/O	PIN_AW126
QSFP_RX_p[0]	Receiver data of channel 0	HIGH SPEED DIFFERENTIAL I/O	PIN_BD135
QSFP_RX_p[1]	Receiver data of channel 1	HIGH SPEED DIFFERENTIAL I/O	PIN_BB135
QSFP_RX_p[2]	Receiver data of channel 2	HIGH SPEED DIFFERENTIAL I/O	PIN_AY135
QSFP_RX_p[3]	Receiver data of channel 3	HIGH SPEED DIFFERENTIAL I/O	PIN_AV135
QSFP_RX_n[0]	Receiver data of channel 0	HIGH SPEED DIFFERENTIAL I/O	PIN_BD133
QSFP_RX_n[1]	Receiver data of channel 1	HIGH SPEED DIFFERENTIAL I/O	PIN_BB133
QSFP_RX_n[2]	Receiver data of channel 2	HIGH SPEED DIFFERENTIAL I/O	PIN_AY133
QSFP_RX_n[3]	Receiver data of channel 3	HIGH SPEED DIFFERENTIAL I/O	PIN_AV133
CIPRI_REFCLK_p	CIPRI clock	CML	PIN_AY120
QSFP_REFCLK_p	QSFP+ port reference clock	CML	PIN_AV120
QSFP_MOD_SEL_n	Module Select	3.3V	PIN_B26
QSFP_RST_n	Module Reset	3.3V	PIN_B30
QSFP_SCL	2-wire serial interface clock	3.3V	PIN_A30
QSFP_SDA	2-wire serial interface data	3.3V	PIN_A35
QSFP_LP_MODE	Low Power Mode	3.3V	PIN_A33
QSFP_INTERRUPT_n	Interrupt	3.3V	PIN_A39
QSFP_MOD_PRS_n	Module Present	3.3V	PIN_B35

2.15 HDMI Output Port

The development board provides High Performance HDMI Transmitter via the Analog Devices ADV7513 which incorporates HDMI v1.4 features, including 3D video support, and 165 MHz supports all video formats up to 1080p and UXGA. The ADV7513 is controlled via a serial I2C bus interface, which is connected to pins on the Cyclone V SoC FPGA. A schematic diagram of the audio circuitry is shown in Figure 3 27. Detailed information on using the ADV7513 HDMI TX is available on the manufacturer's website, or under the Datasheets\HDMI folder on the Kit System CD.

Table 3 18 lists the HDMI Interface pin assignments and signal names relative to the FPGA.

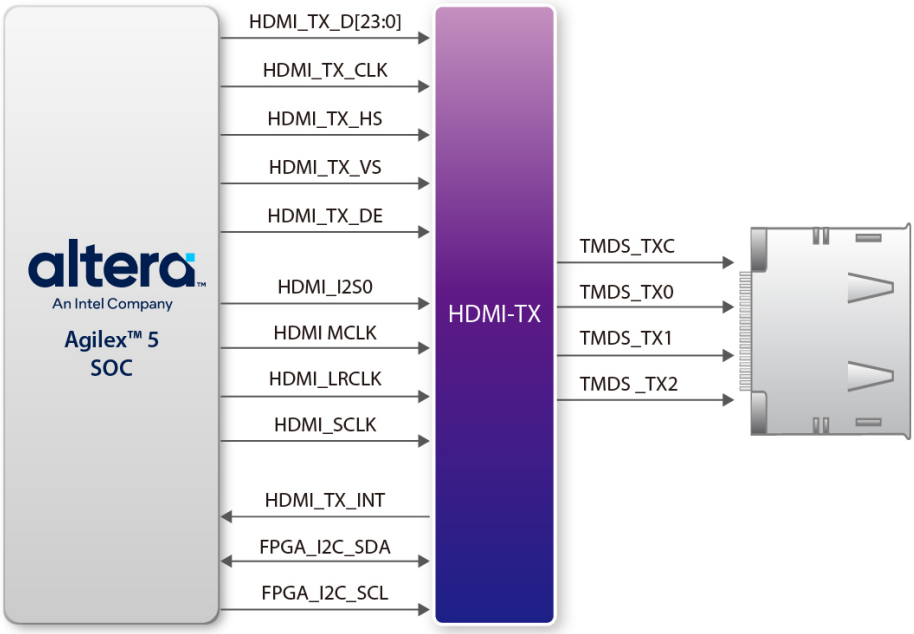


Figure 2-28 The HDMI output interface on the board

Table 2-33 HDMI Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
HDMI_TX_D0	Video Data bus	HSSI DIFFERENTIAL I/O	PIN_CD134
HDMI_TX_D1	Video Data bus	HSSI DIFFERENTIAL I/O	PIN_CD135

HDMI_TX_D2	Video Data bus	HSSI DIFFERENTIAL I/O	PIN_CG134
HDMI_TX_D3	Video Data bus	HSSI DIFFERENTIAL I/O	PIN_CG135
HDMI_TX_D4	Video Data bus	HSSI DIFFERENTIAL I/O	PIN_CH132
HDMI_TX_D5	Video Data bus	HSSI DIFFERENTIAL I/O	PIN_CF132
HDMI_TX_D6	Video Data bus	HSSI DIFFERENTIAL I/O	PIN_CF128
HDMI_TX_D7	Video Data bus	HSSI DIFFERENTIAL I/O	PIN_CK134
HDMI_TX_D8	Video Data bus	3.3V	PIN_CL125
HDMI_TX_D9	Video Data bus	3.3V	PIN_CF121
HDMI_TX_D10	Video Data bus	3.3V	PIN_CF118
HDMI_TX_D11	Video Data bus	3.3V	PIN_BU118
HDMI_TX_D12	Video Data bus	3.3V	PIN_BR118
HDMI_TX_D13	Video Data bus	3.3V	PIN_CA118
HDMI_TX_D14	Video Data bus	3.3V	PIN_BW118
HDMI_TX_D15	Video Data bus	3.3V	PIN_CL128
HDMI_TX_D16	Video Data bus	3.3V	PIN_CL130
HDMI_TX_D17	Video Data bus	3.3V	PIN_CK125
HDMI_TX_D18	Video Data bus	3.3V	PIN_CK128
HDMI_TX_D19	Video Data bus	3.3V	PIN_BF111
HDMI_TX_D20	Video Data bus	3.3V	PIN_BH109
HDMI_TX_D21	Video Data bus	3.3V	PIN_BE115
HDMI_TX_D22	Video Data bus	3.3V	PIN_BF115
HDMI_TX_D23	Video Data bus	3.3V	PIN_BU109
HDMI_TX_CLK	Video Clock	1.2V	PIN_BU52
HDMI_TX_DE	Data Enable Signal for Digital Video.	3.3V	PIN_BK109
HDMI_TX_HS	Horizontal Synchronization	3.3V	PIN_BR109
HDMI_TX_VS	Vertical Synchronization	3.3V	PIN_BE107
HDMI_TX_INT	Interrupt Signal	3.3V	PIN_BE111
HDMI_I2S	I2S Channel 0 Audio Data Input	3.3V	PIN_BK118
HDMI_MCLK	Audio Reference Clock Input	3.3V	PIN_BM118
HDMI_LRCLK	Audio Left/Right Channel Signal Input	3.3V	PIN_BP112
HDMI_SCLK	I2S Audio Clock Input	3.3V	PIN_BM112
FPGA_I2C_SCL	FPGA I2C Clock	3.3V	PIN_BR112

FPGA_I2C_SDA	FPGA I2C Data	3.3V	PIN_BM109

2.16 MIPI Connector

The Agilex 5 devices offer native mobile industry processor interface (MIPI) D-PHY. This support complies to MIPI D-PHY version 2.5, and allows transmission or reception of data with MIPI D-PHY interfaces. It provides the PHY-protocol interface (PPI) to connect with camera serial interface (CSI) and display serial interface (DSI) applications.

The board also provides two 22pin FPC connectors (1 lane clock and 2 lane data for each), allowing users to connect MIPI interface cameras and display devices through FPC cable (see Figure 2-29). Users can use this connector and camera cable to connect to camera devices such as Raspberry Pi camera module to form a camera input application. In addition, it can also be connected with the display device such asd Raspberry Pi MIPI Displayer module to implement a display application.

see Figure 2-30 shows the connections between the FPGA and 22-pin MIPI connector. Table 3 25 shows the pin assignment of 22-pin MIPI connector.

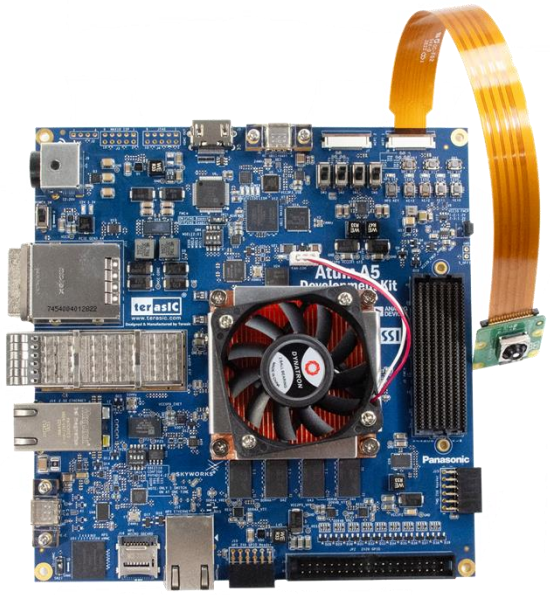


Figure 2-29 MIPI camera module connects to the board via cable

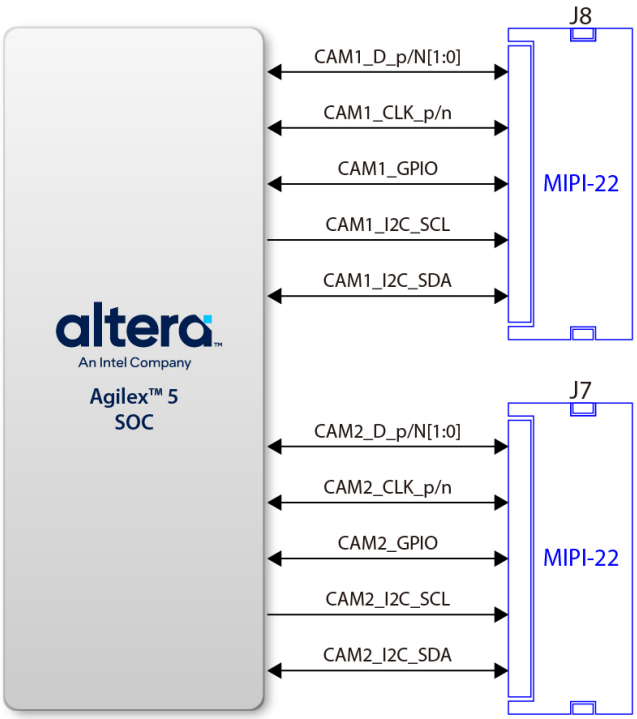


Figure 2-30 Connection between the MIPI connector and FPGA

Table 2-34 MIPI Connector 1 Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
CAM1_CLK_p	MIPI Clock positive	DPHY	PIN_CK17
CAM1_CLK_n	MIPI Clock negative	DPHY	PIN_CL17
CAM1_D_p[0]	MIPI Data 0 positive	DPHY	PIN_CL23
CAM1_D_p[1]	MIPI Data 1 positive	DPHY	PIN_CL20
CAM1_D_n[0]	MIPI Data 0 negative	DPHY	PIN_CK26
CAM1_D_n[1]	MIPI Data 1 negative	DPHY	PIN_CK20
CAM1_I2C_SCL	I2C clock	3.3V	PIN_J2
CAM1_I2C_SDA	I2C data	3.3V	PIN_G2
CAM1_GPIO	GPIO signal	3.3V	PIN_K4
CAM_RZQ0	External reference ball for output drive calibration	1.2V	PIN_BR52

Table 2-35 MIPI Connector 2 Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number

CAM2_CLK_p	MIPI Clock positive	DPHY	PIN_CF28
CAM2_CLK_n	MIPI Clock negative	DPHY	PIN_CC28
CAM2_D_p[0]	MIPI Data 0 positive	DPHY	PIN_CH31
CAM2_D_p[1]	MIPI Data 1 positive	DPHY	PIN_CA31
CAM2_D_n[0]	MIPI Data 0 negative	DPHY	PIN_CF31
CAM2_D_n[1]	MIPI Data 1 negative	DPHY	PIN_CC31
CAM2_I2C_SCL	I2C clock	3.3V	PIN_A8
CAM2_I2C_SDA	I2C data	3.3V	PIN_G1
CAM2_GPIO	GPIO signal	3.3V	PIN_J1

2.17 PCI Express

As shown in Figure 2-31, the board features one PCIe Express downstream interfaces (x4 lane) which are designed to interface with a PC motherboard x4 slot via PCIe cable and PCIe adapter card. Utilizing built-in transceivers on a Agilex SoC device, it is able to provide a fully integrated PCI Express-compliant solution for multi-lane (x4) applications. With the PCI Express hard IP block incorporated in the Agilex SoC device, it will allow users to implement simple and fast protocols, as well as saving logic resources for logic applications.

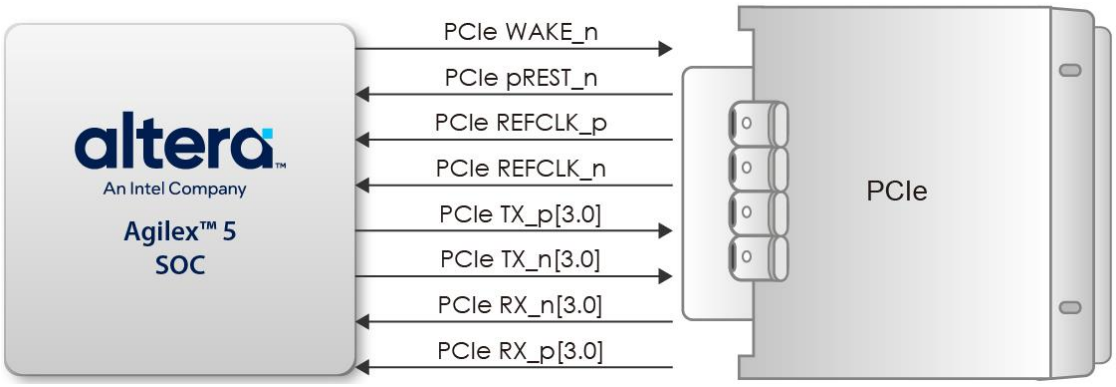


Figure 2-31 PCI Express Pin Connection

The PCI Express interface supports complete PCI Express Gen1 at 2.5Gbps/lane, Gen2 at 5.0Gbps/lane, and Gen3 at 8.0Gbps/lane protocol stack solution compliant to PCI Express base specification 3.0 that includes PHY-MAC, Data Link, and transaction layer circuitry embedded in PCI Express hard IP blocks.

To use PCIe interface, two external associated devices will be needed to establish a link with PC. First, a PCIe half-height add-in host card with a PCIe x4 cable connector called PCA3 (PCIe Cabling Adapter Gen3 Card and See Figure 2-32) will be used to plug into the PCIe slot on a mother board. Then, a PCIe x4 cable (See Figure 2-33) will be used to connect board and PCIe add-in card as shown in Figure 2-34, the longest length is up to 3 meters. These two associated devices are not included in the kit. To purchase the PCA3 card as well as the external cable, please refer to Terasic website pca3.terasic.com and PCIe_Cable.

Figure 2-32 PCIe Cabling Adaptor(PCA) Gen 3 card

Figure 2-33 PCIe External Cable

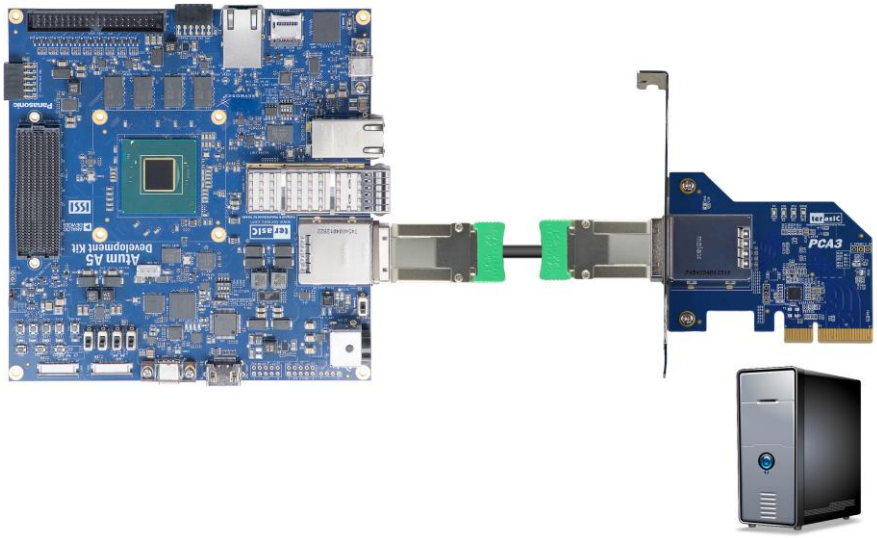


Figure 2-34 PCIe Link Setup between Atum A5 and PC

Table 2-36 Pin Assignment of PCIe connector

Signal Name	FPGA Pin No	Description	I/O Standard
PCIE_TX_p[0]	PIN_BY129	PCIe Transmitter data p0	HIGH SPEED DIFFERENTIAL I/O"
PCIE_TX_p[1]	PIN_BT129	PCIe Transmitter data p1	HIGH SPEED DIFFERENTIAL I/O"
PCIE_TX_p[2]	PIN_BL129	PCIe Transmitter data p2	HIGH SPEED DIFFERENTIAL I/O"
PCIE_TX_p[3]	PIN_BG129	PCIe Transmitter data p3	HIGH SPEED DIFFERENTIAL I/O"
PCIE_TX_n[0]	PIN_BY126	PCIe Transmitter data n0	HIGH SPEED DIFFERENTIAL I/O"
PCIE_TX_n[1]	PIN_BT126	PCIe Transmitter data n1	HIGH SPEED DIFFERENTIAL I/O"
PCIE_TX_n[2]	PIN_BL126	PCIe Transmitter data n2	HIGH SPEED DIFFERENTIAL I/O"
PCIE_TX_n[3]	PIN_BG126	PCIe Transmitter data n3	HIGH SPEED DIFFERENTIAL I/O"
PCIE_RX_p[0]	PIN_BV135	PCIe Receiver data p0	HIGH SPEED DIFFERENTIAL I/O"
PCIE_RX_p[1]	PIN_BN135	PCIe Receiver data p1	HIGH SPEED DIFFERENTIAL I/O"
PCIE_RX_p[2]	PIN_BJ135	PCIe Receiver data p2	HIGH SPEED DIFFERENTIAL I/O"
PCIE_RX_p[3]	PIN_BF135	PCIe Receiver data p3	HIGH SPEED DIFFERENTIAL I/O"
PCIE_RX_n[0]	PIN_BV133	PCIe Receiver data n0	HIGH SPEED DIFFERENTIAL I/O"
PCIE_RX_n[1]	PIN_BN133	PCIe Receiver data n1	HIGH SPEED DIFFERENTIAL I/O"
PCIE_RX_n[2]	PIN_BJ133	PCIe Receiver data n2	HIGH SPEED DIFFERENTIAL I/O"
PCIE_RX_n[3]	PIN_BF133	PCIe Receiver data n3	HIGH SPEED DIFFERENTIAL I/O"
PCIE_OB_REFCLK_p	PIN_BC111	PCIe on-borad reference clock	CML
PCIE_REFCLK_p	PIN_BB120	Motherboard reference clock	CML
PCIE_PERST_n	PIN_BF107	Reset	3.3V
PCIE_WAKE_n	PIN_D34	Wake signal	3.3V

Chapter 3

Dashboard GUI

The Atum A5 Dashboard GUI is a board management system. This system is connected from the Host to the system max on the Atum A5 board through the UART interface, and reads various status on the board. The reported status includes FPGA/Board temperature, fan speed, FPGA core power and 12V input power. **Figure 3-1** shows the block diagram of the Atum A5 Dashboard.

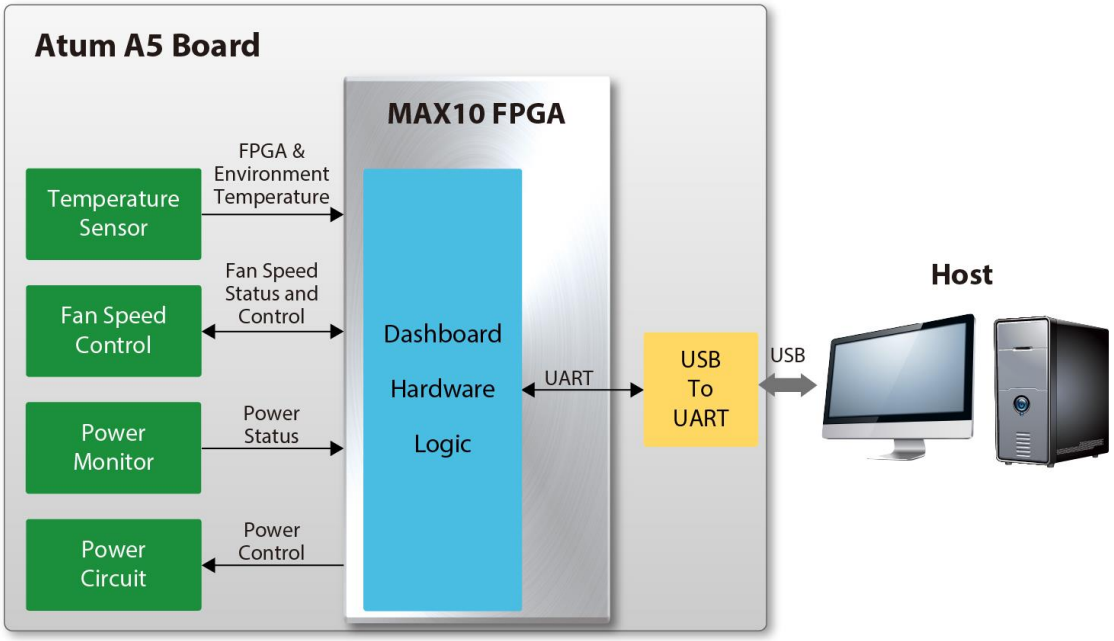


Figure 3-1 Block Diagram of the Dashboard GUI

3.1 Setup for the Dashboard GUI

To use the dashboard system, users need to install the USB to UART driver on the host first, so that user can establish a connection with the Atum A5 board. This section will describe how to install USB to UART driver on the windows OS host.

■ Connection Setting

1. Connect the USB type-c connector(U6) of the board to the host PC USB port through USB type-c cable.

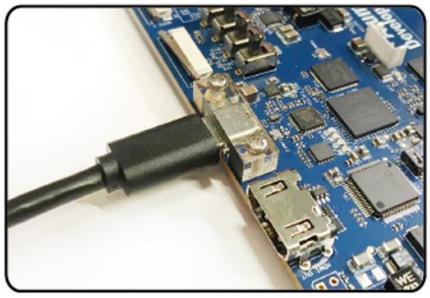


Figure 3-2 Connect USB type-c cable to the board

2. Connect power to the Atum A5 board.

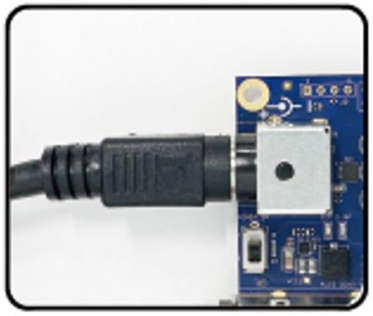


Figure 3-3 Connect power to the board

3. Power on the Atum A5 board.

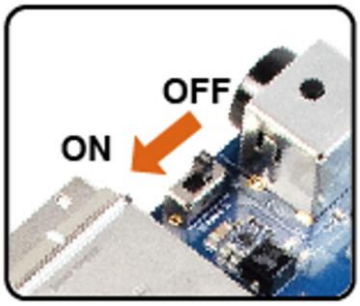


Figure 3-4 Power on the board

■ Install Driver

Please refer to the document "The CP2105 (USB to UART) Driver Installation

Instructions" to install the driver.

After the driver installation of CP2105 is completed, two USB to UART ports can be seen in the "Device Manager" window in the Windows system of the user's computer. As shown in Figure **Figure 3-5**, the Enhanced COM port is connected to the HPS fabric, and the Standard COM port is connected to the System MAX10. Note that the COM number (for example: COM16 and COM17) seen by each user should be different, because the hardware system of each user's computer is different

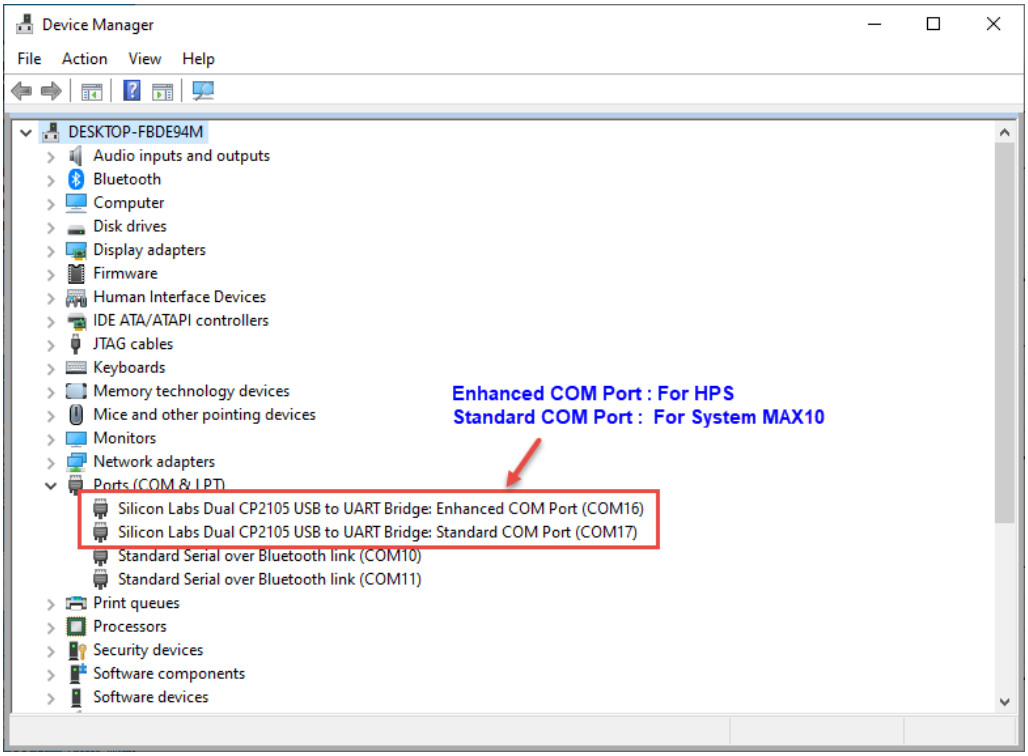


Figure 3-5 he CP2105 in the Device Manager

3.2 Run Dashboard GUI

■ Dashboard GUI software location

Users can find it from the path: Tool\dashboard_gui\Dashboard.exe in the Atum A5 system CD and copy it to the host PC.

Execute the Dashboard.exe, a window will show as **Figure 3-6**. It will describe the detail functions as below.

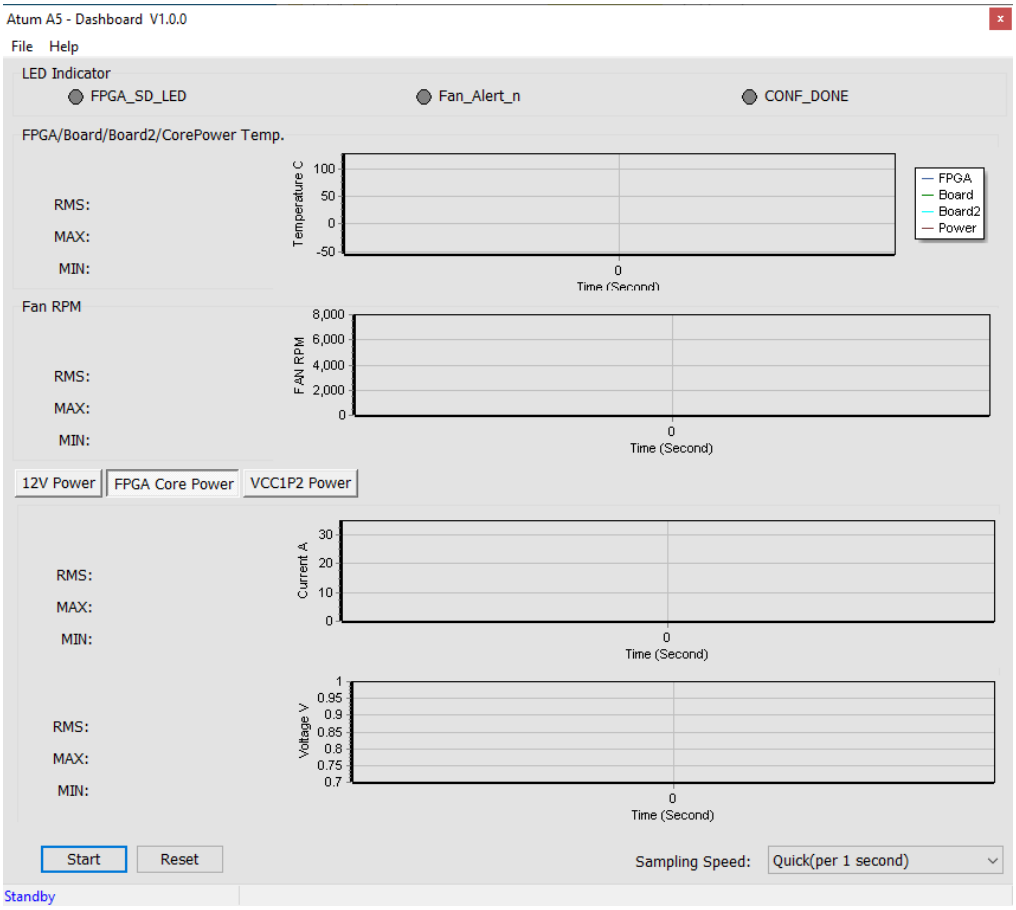


Figure 3-6 Dashboard GUI

■ Dashboard GUI function introduction

- **Start/Stop**: As shown in **Figure 3-7**, there is a **Start** button at the bottom-left of the GUI window. Click it to run the program (**Start** will change to **Stop**), it will show the Atum A5 board status. Users can press **Stop** button to stop the status data transmission and display.
- **Reset Button**: Press this button to clear the historical data shown in GUI, and record the data again.

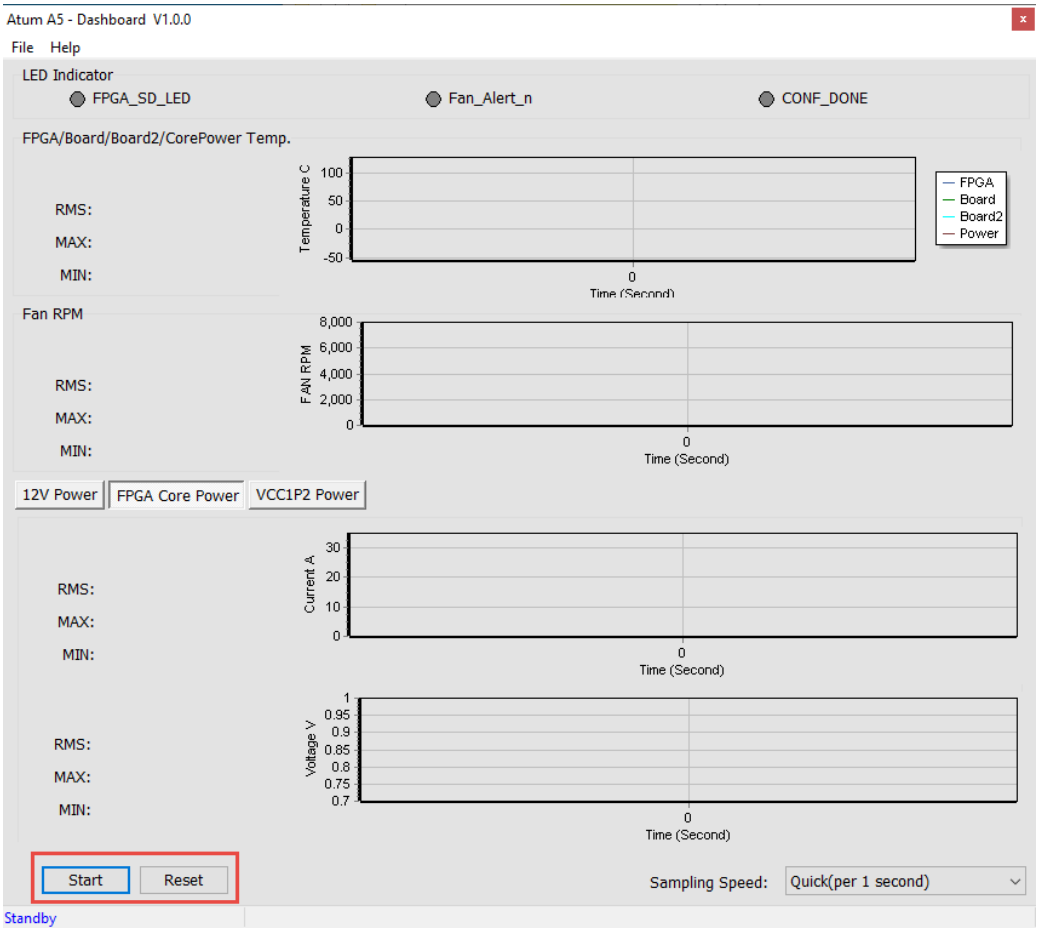


Figure 3-7 Start and Reset button

- **LED Indicator**:
  - **CONF_DONE** :As shown in **Figure 3-8**, once you press the "**Start**" button, it will show the status LED number on the Atum A5 board. Note that "**CONF_DONE**" stands for FPGA configure done status. There is no LED on Atum A5 board to display FPGA configure status. When this status is shown in green on the GUI, it means that FPGA configuration has been completed.
  - **Fan_Altert_n**: Illuminates when the fan is abnormal, such as when the fan speed is different from expected.
  - **FPGA_SD_LED:** When this status is shown in green on the GUI, it means that the FPGA temperature or the board temperature exceeds 95 degrees. All the power of the FPGA will be cut off.

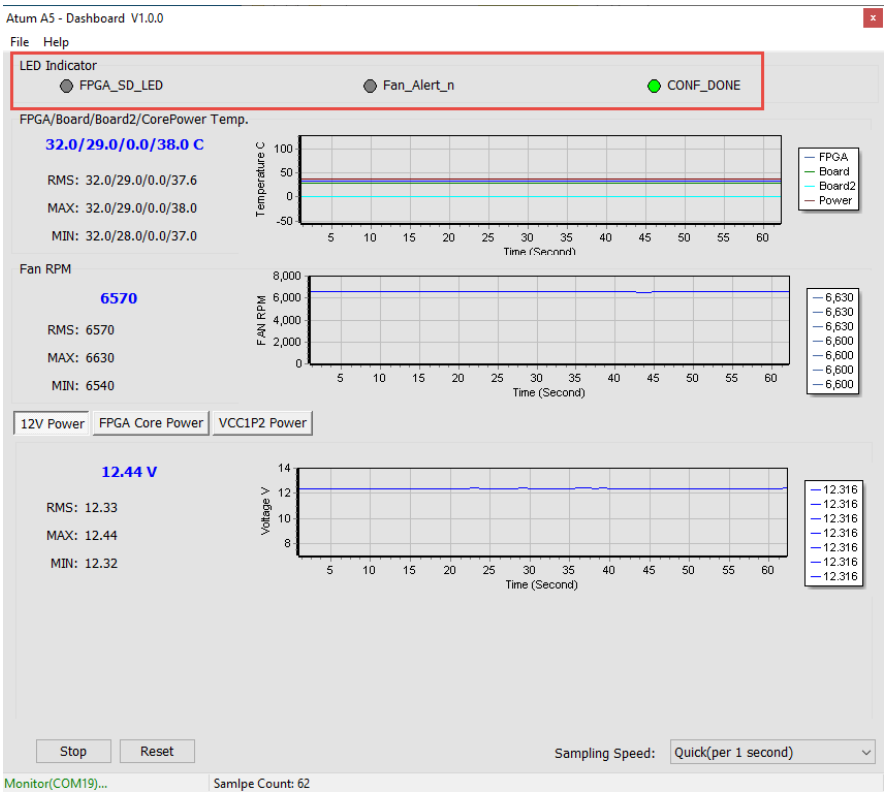


Figure 3-8 FPGA Status section

- **FPGA/Board/Board2/CorePower Temp.**: The Dashboard GUI will real-time show the fan speed, Atum A5 board ambient and FPGA temperature. Users can know the board temperature in time. The information will be refreshed per 1 second, and displays through diagram and number, as shown in **Figure 3-9**. **Figure 3-10** shows the location of the two temperature sensors of **Board** and **Board2** on the GUI.

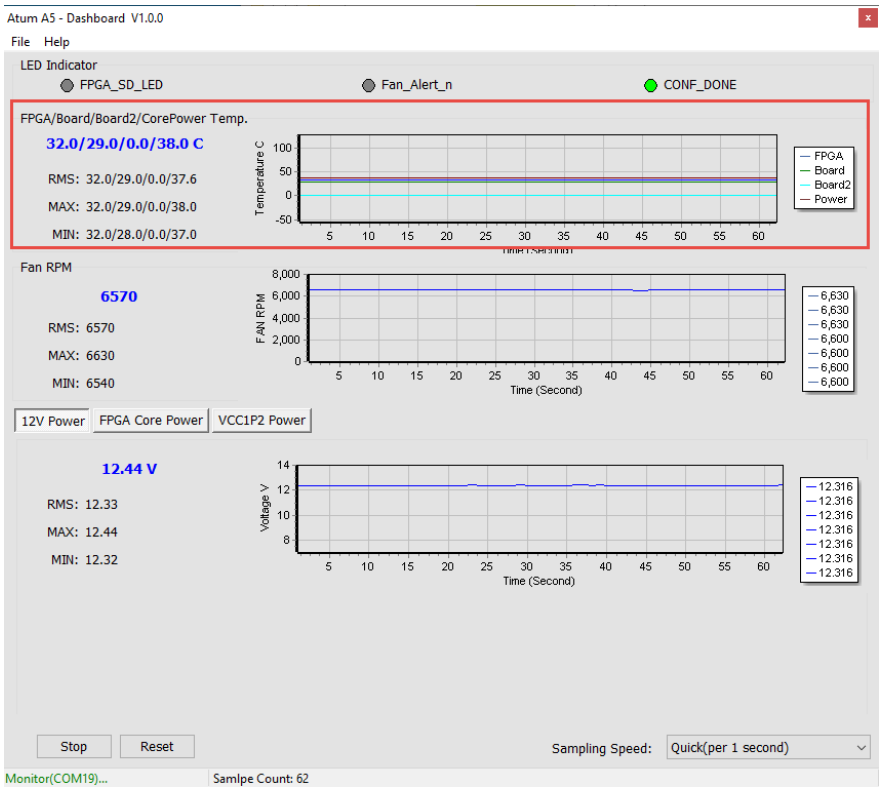


Figure 3-9 Temperature section

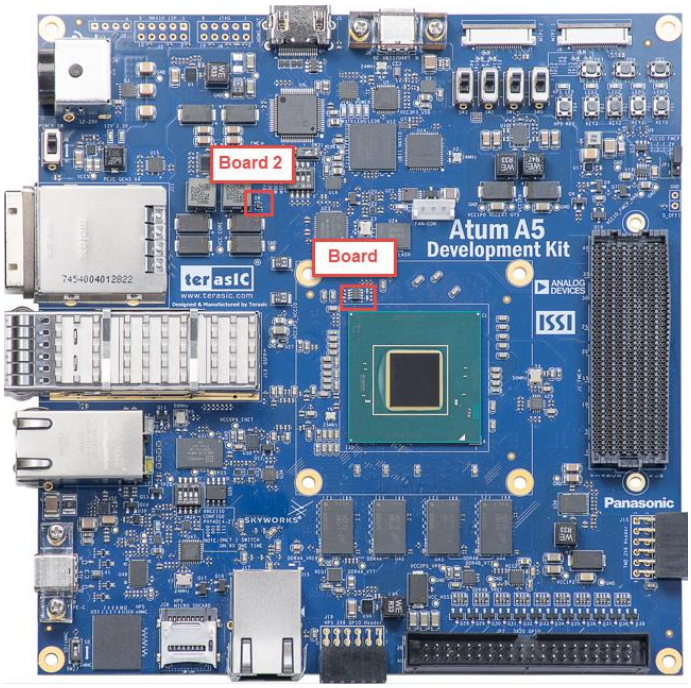


Figure 3-10 Location of the board's ambient temperature

- **Fan RPM**: It displays the real-time speed of the fan on the Atum A5 board, as shown in **Figure 3-11**.

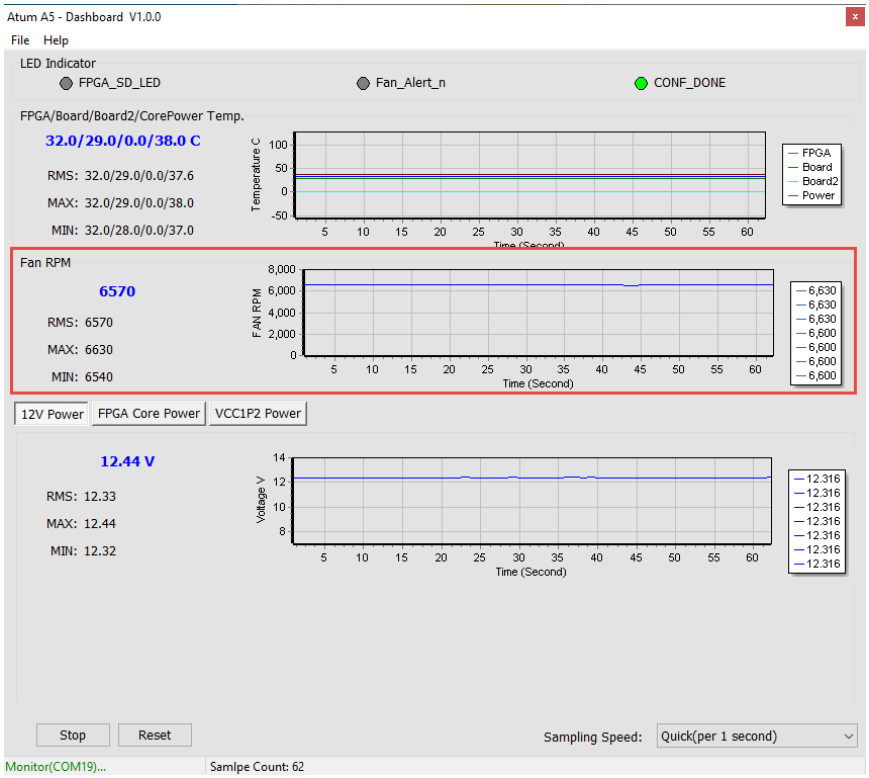


Figure 3-11 FAN RPM section

- **12V/ FPGA Core/ VCC1P2 Power monitor**: It displays the real-time 12V /FPGA / VCC1P2 Power voltage and consumption current on the Atum A5 board, as shown in **Figure 3-12**.

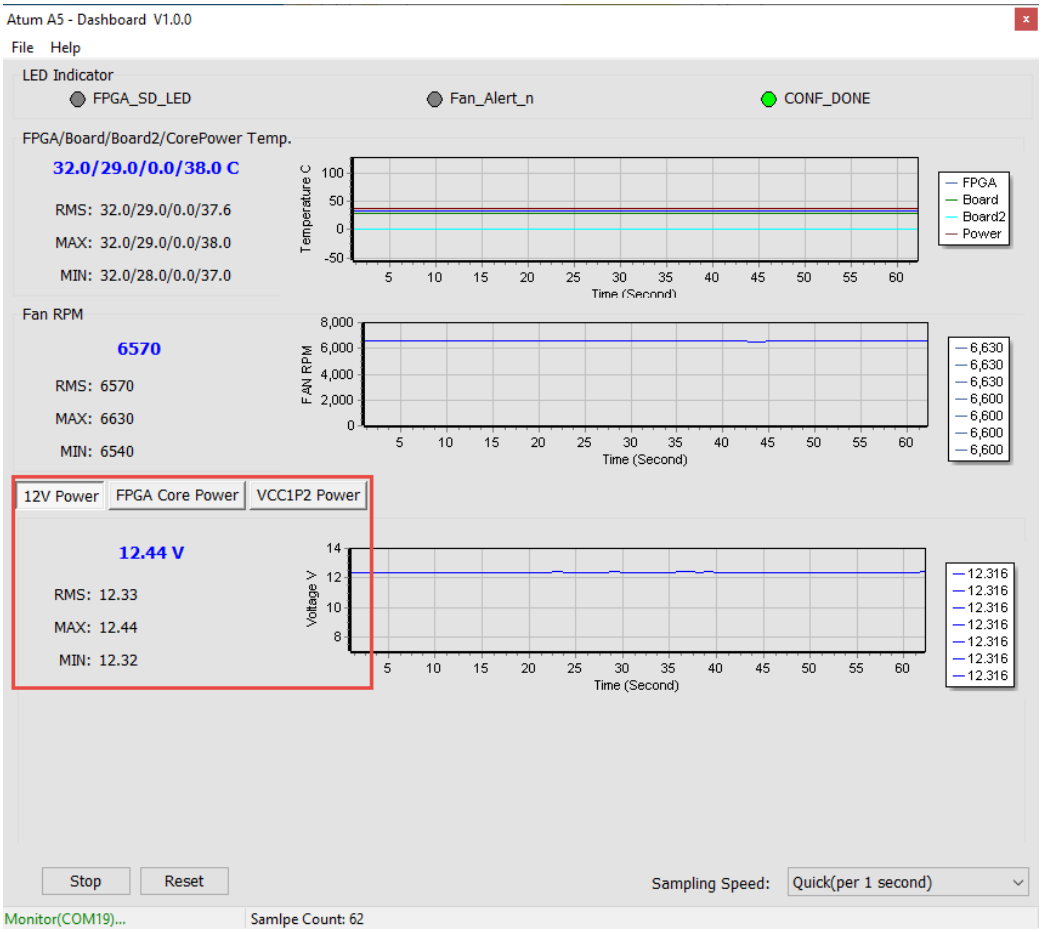


Figure 3-12 Power Monitor Section

- **Sampling Speed**: It can change interval time that the Dashboard GUI sample the board status. Users can adjust it to 1s/10s/1min/Full Speed (0.1s) to sample the board status, as shown in **Figure 3-13** and **Figure 3-14**.

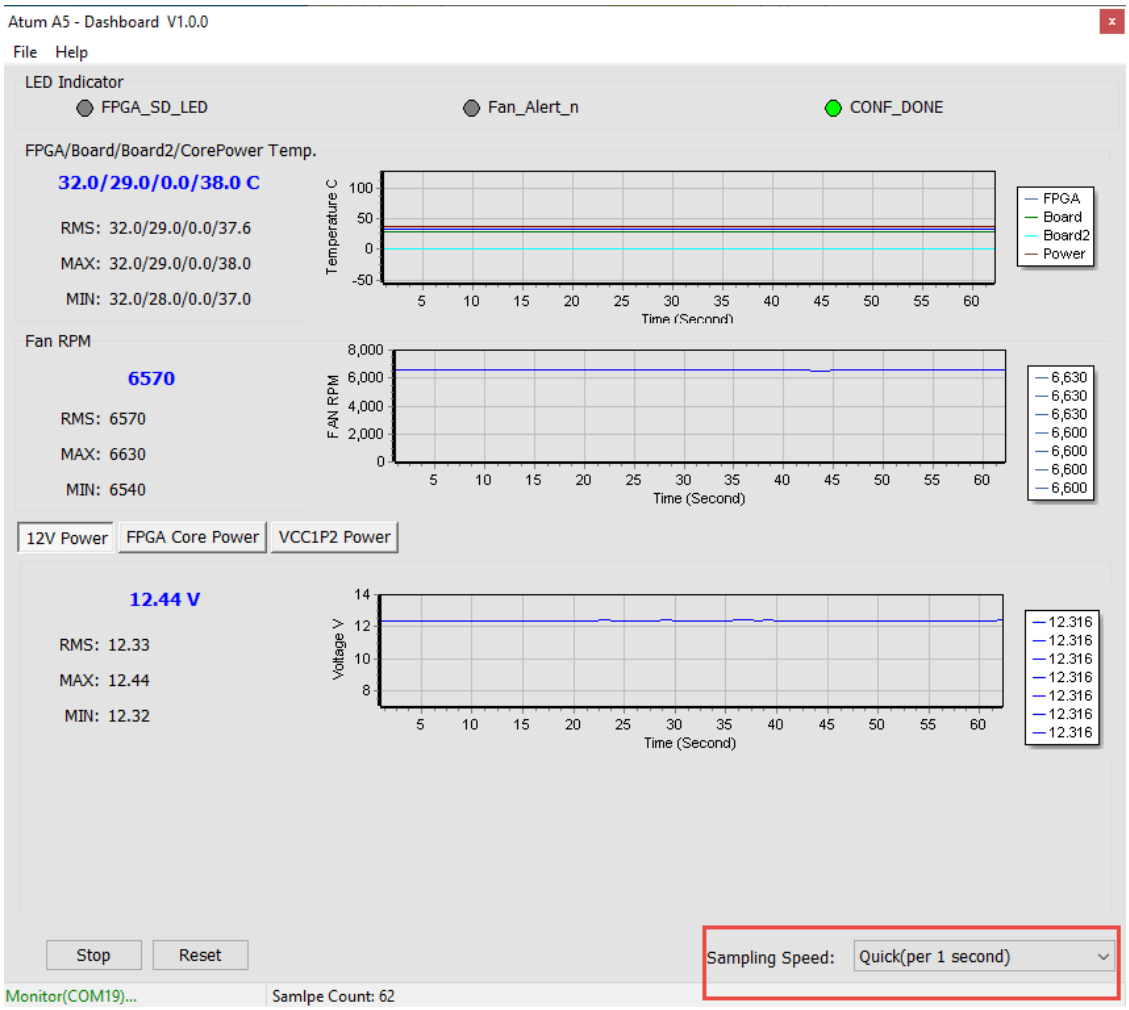


Figure 3-13 Sampling Speed section

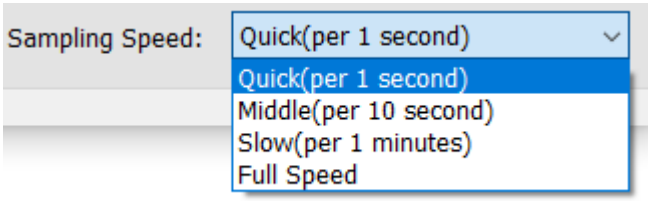


Figure 3-14 Options of Sampling Speed

- **File Manu**:

  The user can click “File” menu at the top left of the GUI (See **Figure 3-15**) and some options such as board information and status export will appear. Note that to active these functions, you will need to stop obtaining the board status (i.e. Don’t Press “**Start**” button) in the GUI. Detailed introductions of these functions are described in below.

Figure 3-15 File menu

- **Auto shutdown status** : This option will report whether the board entered "**Auto shutdown status**" because the FPGA temperature is too high or the fan speed is abnormal.

- **Board Information**: There is a **File** page on the upper left of the Dashboard GUI program window, click the **Board Information** to get the current software version and the Atum A5 board version, as shown in **Figure 3-16**. Note, user needs to stop the system monitor (press the "**Stop**" button on the Dashboard GUI), then you can run the Board Information.

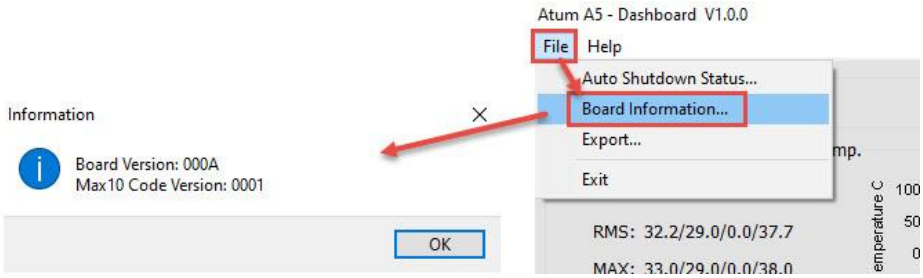


Figure 3-16 Board Information

- **Log File**: On the upper left of the Dashboard GUI program window, click the Export in the File page to save the board temperature, fan speed and voltage data in .csv format document, as shown in **Figure 3-17** and **Figure 3-18**.

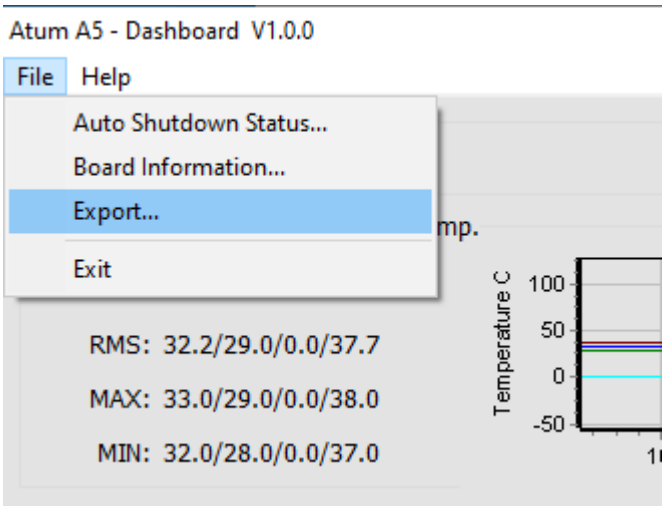


Figure 3-17 Export the log file

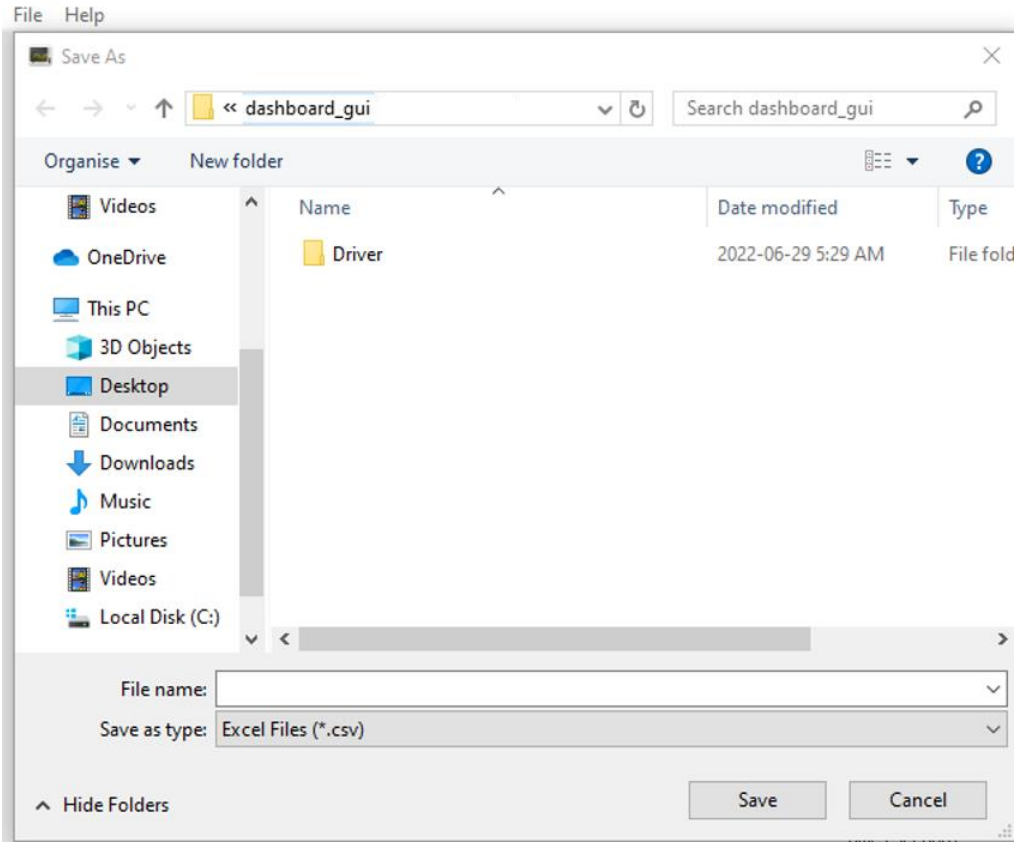


Figure 3-18 Export the log file in .csv format

Chapter 4

Install Driver for the Board

4.1 Install the USB Blaster II Driver

The Atum A5 board equipped with an USB-Blaster II circuit, it interfaces a USB port on a host computer to an Agilex SoC FPGA on the board. The USB-Blaster II circuit sends configuration data from the PC via the JTAG interface to the FPGA. To use USB-Blaster II circuit, user need to install the driver on your operation system.

When user install the Quartus Prime software on your host, In the last step of the installation, the installer will ask whether to install the USB Blaster driver. If you click "yes", the driver should be installed automatically in your operation system (Windows). If you skip this step, you can also find the driver from the Quartus installation path after the Quartus installation is complete. The driver path is in *<Qaurtus Install Path>\<version>\quartus\drivers\usb-blaster-ii* .

For linux users, please refer to this link to install : https://rocketboards.org/foswiki/Documentation/UsingUSBBlasterUnderLinux

4.2 Install USB to UART Driver

Please refer to the document "The CP2105 (USB to UART) Driver Installation Instructions" to install the driver.

Chapter 5

Additional Information

5.1 Getting Help

Here are the addresses where you can get help if you encounter problems:

■ Terasic Technologies

No.80, Fenggong Rd., Hukou Township, Hsinchu County 303035. Taiwan
Email: support@terasic.com
Web: www.terasic.com
Atum A5 Web: agilex-som.terasic.com

■ Revision History

Date	Version	Changes
2024.07	Version B First publication	
2025.01	V1.0	Fix some textual errors.