Himax

WiseEye™

DATA SHEET

(DOC No. HX6538-A-DS)

HX6538-A

WE2 AI Processor

Preliminary version 01 July 2023

Himax Technology, Inc.
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Revision History

Version	Date	Description of changes
01	2023/07/06	New setup.

List of Figures

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1. General Description

The HX6538-A is an extreme-low power, high performance microcontroller designed for battery powered Endpoint AI applications.

The HX6538-A embedded powerful dual ARM Cortex-M55 processors with Helium vector and floating-point extensions and an ARM Ethos-U55 microNPU core to accelerate convolution operation of neural network model. There are internal 2.5MB ultra-low-leakage SRAMs for system and program usage. With the benefit of Ethos-U55 microNPU and Helium vectored extended Cortex-M55 architecture, the HX6538-A provides maximum computing capability with the lowest power consumption and latency.

Besides traditional interrupt-based trigger wakeup mechanism from power-down or sleep mode, the HX6538-A provides a new multi-layer power management scheme to wakeup image sensor periodically for battery-powered applications. The multi-layer power management is controlled by hardware PMU state machine that support various trigger events for power state transition. The Cortex-M55 and Ethos-U55 cores are placed in 2nd power layer to save power consumption. Normally, Cortex-M55 and Ethos-U55 cores are in power shut-off state until 1st layer detection completed. There are hardware image accelerators in 1st layer to provide pre-processing of imaging tasks and provide a wake-up trigger when event is detected. Besides multi-layer power management, the HX6538-A also provides internal 0.8/0.9V Dynamic Voltage Frequency Scaling **(DVFS)** scheme to reduce dynamic power consumption. Both design schemes optimize power consumption and maintain required response time and accuracy in Endpoint AI applications.

Security is another key consideration for Internet of Things **(IoT)** or other embedded applications. In combing with hardware CryptoCell-312 crypto and Physical Unclonable Function **(PUF)** engines, the HX6538-A provides a complete system-level security solution including secure boot, secure OTA firmware update, and secure meta data output with minimum processing latency. A Physical Unclonable Function **(PUF)** hardware offers a unique identification **(UID)** or a hardware root of trust **(RoT)** for the establishment of a trusted foundation, from which all security operations need. PUF engine also provide high-quality TRNG number for crypto engine and security application usage. The HX6538-A also supports TrustZone security and TF-M software stack for application usage.

The HX6538-A provides rich peripheral interfaces for application need, including image MIPI CSI-2 transmitter and receiver, DVP and SDI interfaces, audio I^{2}S, PDM, interfaces, and peripheral interfaces of UART, I^{2}C, I^{3}C, SPI, GPIO, PWM, SD, SDIO and ADC.

2. Features

- ARM Cortex-M55 processor **(Big, high-performance core, version r1p1)**
  - Frequency up to 400MHz
  - Half/Single precision Floating Point Unit **(FPU)**
  - Helium vector processing extension for machine-learning
  - TrustZone security extension
  - 16KB of instruction cache, 16KB of data cache
  - 256KB of ITCM memory, 256KB of DTCM memory
  - Serial Wire Debug **(SWD)** with 8 breakpoints and 4 watch points
- ARM Cortex-M55 processor **(Little, high-efficiency core, version r1p1)**
  - Frequency up to 150MHz
  - Half/Single precision Floating Point Unit **(FPU)**
  - Helium vector processing extension for machine-learning
  - TrustZone security extension
  - 16KB of instruction cache, 16KB of data cache
  - Serial Wire Debug **(SWD)** with 8 breakpoints and 4 watch points
- ARM Ethos-U55 microNPU **(version r2p0)**
  - Frequency up to 400MHz
  - 64MACs/cycle
  - Support a variety of CNNs and RNNs network
  - Support weight compression
- Internal system memory
  - Configurable system memory, up to 2432KB
  - 64KB boot ROM
- External Flash
  - Support external 1 to 16MB QSPI Flash, up to 100MHz
  - Support Execute-In-Place **(XIP)** direct read mode
- Hardware accelerators
  - Motion detection
  - 2x2 sub-sampler and filter
  - 5x5 de-mosaic and filter
  - Image crop, sub-sampling, and binning
  - JPEG codec
  - Hardware-based voice active detector **(HWVAD)**
- Security
  - PUF based hardware Root-of-Trust **(RoT)**, and unique device ID
  - PUF based True Random Number Generator **(TRNG)**
  - CryptoCell-312 crypto engine
  - TrustZone security
  - Secure debug with certificated authentication
  - Secure boot, secure OTA, secure meta data output
- Image sensor interfaces
  - 2-lane MIPI CSI-2 RX, up to 1.8Gbps on each lane
  - 2-lane MIPI CSI-2 TX for image pass-through only, up to 1.8Gbps on each lane
  - Up to 1x DVP interface, 1/4/8-bit mode, up to 72MHz
  - Up to 1x SDI interface, 1-bit mode shared with DVP interface, up to 72MHz
- Audio interfaces
  - Up to 8-channel PDM RX
  - Up to 2-channel PDM TX for audio pass-through only
  - Up to 1x I^2S master or slave

- Peripheral interfaces
  - Up to 1x SPI master, up to 50MHz
  - Up to 1x SPI slave, up to 40MHz
  - Up to 2x I^2C master, up to 1MHz
  - Up to 2x I^2C slave, up to 1MHz
  - Up to 2x I^3C slave, support SDR and HDR-DDR, up to 12.5MHz
  - Up to 3x UARTs, 1 UART supports RS232/RS485 and IrDA
  - Up to 3x PWMs
  - Up to 37x GPIOs
- Memory card interface
  - Up to 1x SD and SDIO host, support DS mode, up to 25MHz
- ADC interface
  - Up to 4-channel
- Power management
  - Low power modes – active, sleep, power-down and deep-power-down
  - Hardware Power Management Unit **(PMU)**
  - Ultra-low leakage SRAMs with retention
  - Core 0.8/0.9V, up to 400MHz, Dynamic Voltage Frequency Scaling **(DVFS)**
  - On-chip high efficiency DC-DC for 0.8/0.9V core voltage generation
- Debug mode
  - Up to 1x Serial Wire Debug interface **(SWD)** with SRSTN
- Clock, reset and supply management
  - 1.8V supply for analog/mixed-signal blocks and SIF domain GPIOs
  - 1.8V or 3.3V supply for PIF and AON domain GPIOs
  - 24MHz crystal oscillator
  - 32.768KHz crystal oscillator
  - Internal 1/24/48/96MHz factory-trimmed RC oscillator
  - Internal 1/32.768KHz factory-trimmed RC oscillator
- Packages
  - LQFP128: 16.0mm x 16.0mm
  - WLCSP65: 2.3mm x 5.6mm
  - QFN88: 8.0mm x 12.0mm

3. Block Diagram

Figure 3.1 shows the functional modules in the HX6538-A.

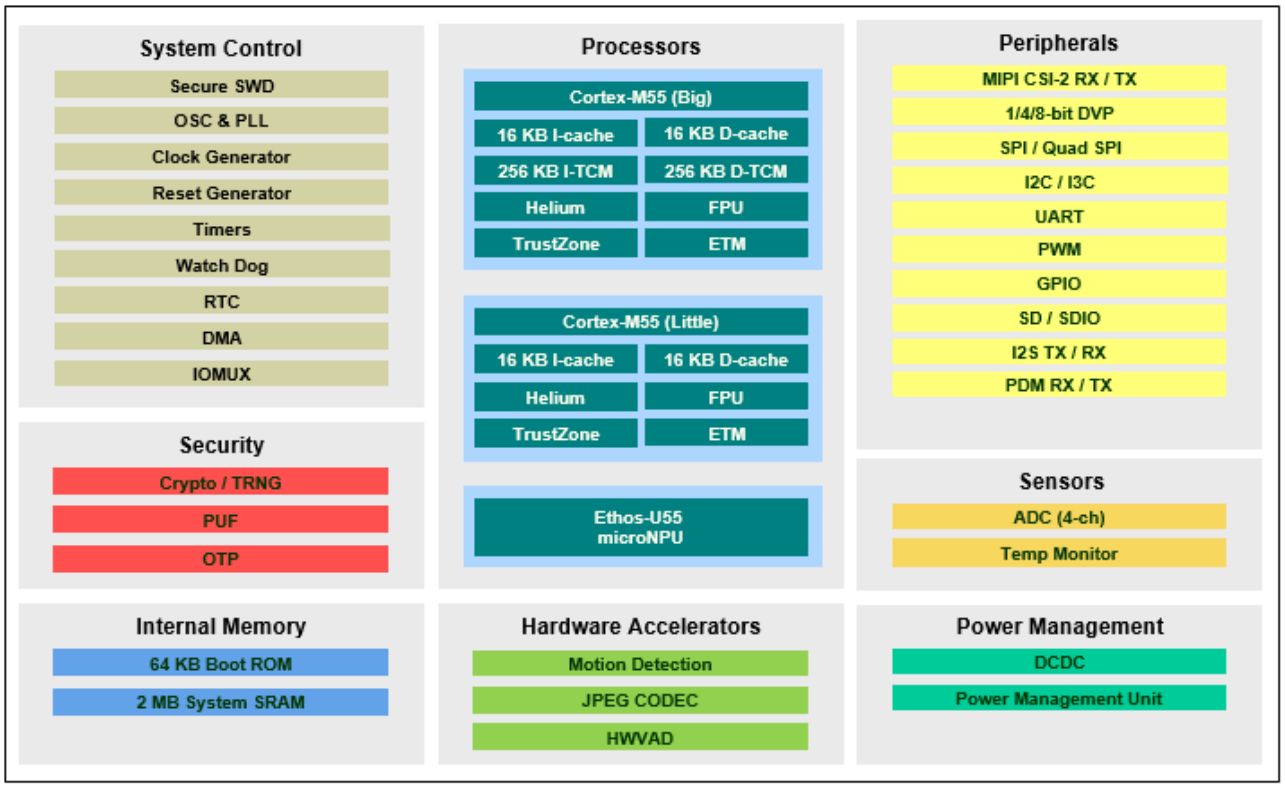


Figure 3.1: HX6538-A block diagram

4. Pin Assignment

4.1. LQFP128

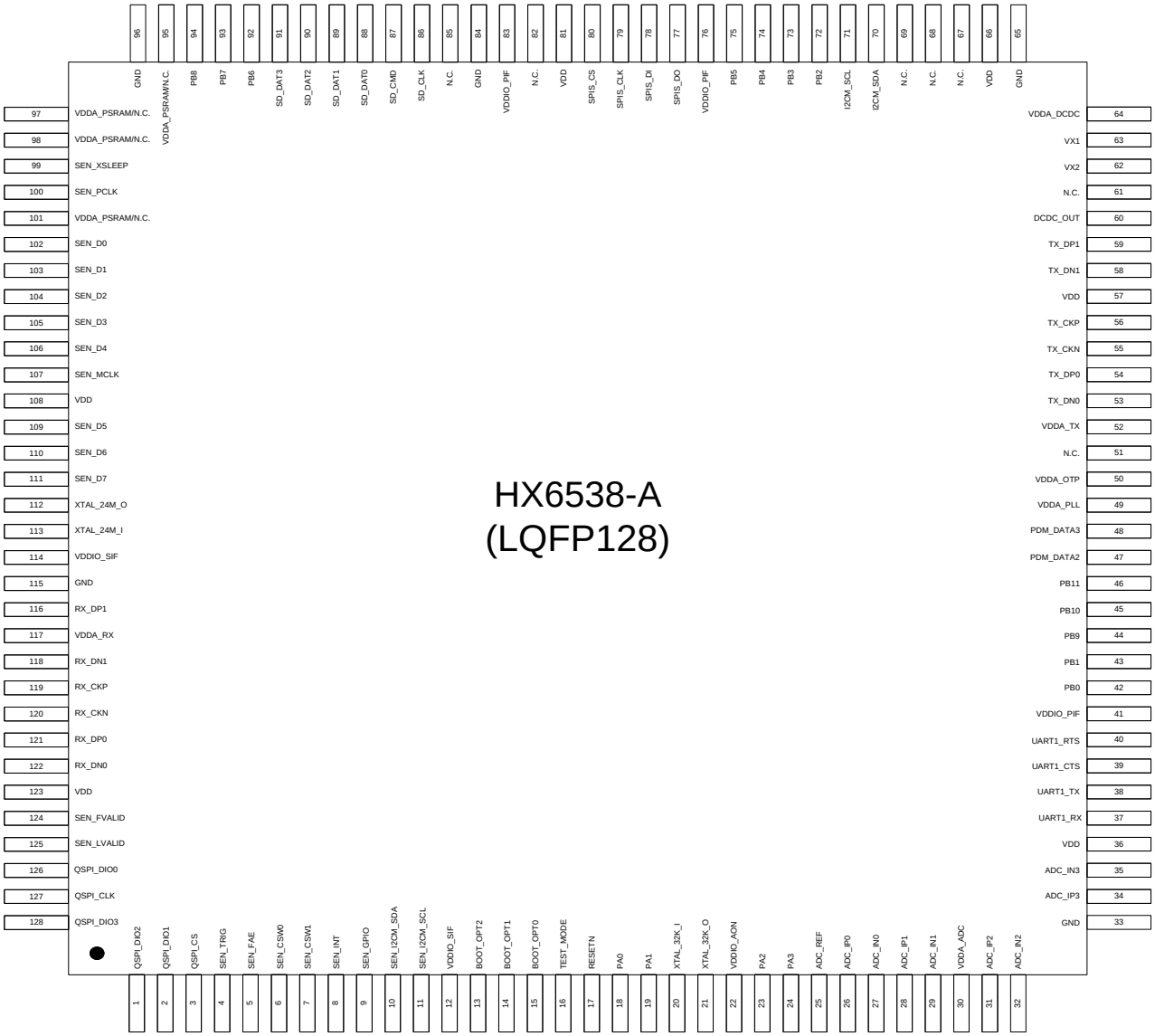


Figure 4.1: LQFP128 pin assignment (top view)

Pin Types: **A**=Analog, **I**=Input, **O**=Output, **P**=Power, **G**=Ground, **FS**=Fail-Safe
Reset States: **PH**=Pull High, **PL**=Pull Low
Pin Domains: **SIF**=1.8V only, **PIF**=1.8V or 3.3V, **AON**=1.8V or 3.3V **(always-on)**

Pin name	Pin no.	Type	Reset	Domain	Description
QSPI_DIO2	1	I/O, FS	O	SIF	QSPI data 2 for Flash.
QSPI_DIO1	2	I/O, FS	I, PL	SIF	QSPI data 1 for Flash.
QSPI_CS	3	O, FS	O	SIF	QSPI chip select for Flash.
SEN_TRIG	4	O, FS	O	SIF	Sensor trigger.
SEN_FAE	5	O, FS	O	SIF	Sensor frame auto exposure.
SEN_CSW0	6	O, FS	O	SIF	Sensor content switch0.
SEN_CSW1	7	O, FS	O	SIF	Sensor content switch1.
SEN_INT	8	I, FS	I; PL	SIF	Sensor interrupt.
SEN_GPIO	9	I/O, FS	O	SIF	Power down and reset control for image sensor.
SEN_I2CM_SDA	10	I/O, FS	I	SIF	I^2C master data for image sensor.
SEN_I2CM_SCL	11	I/O, FS	I	SIF	I^2C master clock for image sensor.
VDDIO_SIF	12,114	P	-	1.8V	I/O supply **(Image sensor GPIOs, SIF)**.
BOOT_OPT2	13	I	I; PL	AON	Boot option selection pin2.
BOOT_OPT1	14	I	I; PL	AON	Boot option selection pin1.
BOOT_OPT0	15	I	I; PL	AON	Boot option selection pin0.
TEST_MODE	16	I	I; PL	AON	Test mode.
RESETN	17	I, FS	I; PH	AON	Reset pin.
PA0 PA1	18 19	I/O, FS	I; PL	AON	General-purpose IO, group A.
XTAL_32K_I	20	I	I	AON	Crystal 32K.768Hz input.
XTAL_32K_O	21	O	O	AON	Crystal 32K.768Hz output.
VDDIO_AON	22	P	-	1.8/3.3V	I/O supply **(AON GPIOs)**.
PA2 PA3	23 24	I/O, FS	I; PH	AON	General-purpose IO, group A.
ADC_REF	25	AI	-	-	ADC reference voltage input.
ADC_IP0	26	AI	-	-	ADC input Ch0_P.
ADC_IN0	27	AI	-	-	ADC input Ch0_N.
ADC_IP1	28	AI	-	-	ADC input Ch1_P.
ADC_IN1	29	AI	-	-	ADC input Ch1_N.
VDDA_ADC	30	P	-	1.8/3.3V	Power supply **(ADC)**.
ADC_IP2	31	AI	-	-	ADC input Ch2_P.
ADC_IN2	32	AI	-	-	ADC input Ch2_N.
ADC_IP3	34	AI	-	-	ADC input Ch3_P.
GND	33,65 84,96 115	G	-	Ground	Ground.
ADC_IN3	35	AI	-	-	ADC input Ch3_N.
VDD	36,57 66,81 108,123	P	-	0.8/0.9V	Power supply from DC-DC output.
UART1_RX	37	I, FS	I; PL	PIF	UART1 RX pin.
UART1_TX	38	I/O, FS	I; PL	PIF	UART1 TX pin.
UART1_CTS	39	I, FS	I; PL	PIF	UART1 clear to send.
UART1_RTS	40	I/O, FS	I; PL	PIF	UART1 require to send.
VDDIO_PIF	41,76,83	P	-	1.8/3.3V	I/O supply **(peripheral GPIOs, PIF)**.
PB0 PB1 PB2 PB3	42 43 72 73	I/O, FS	I; PL	PIF	General-purpose IO, group B.

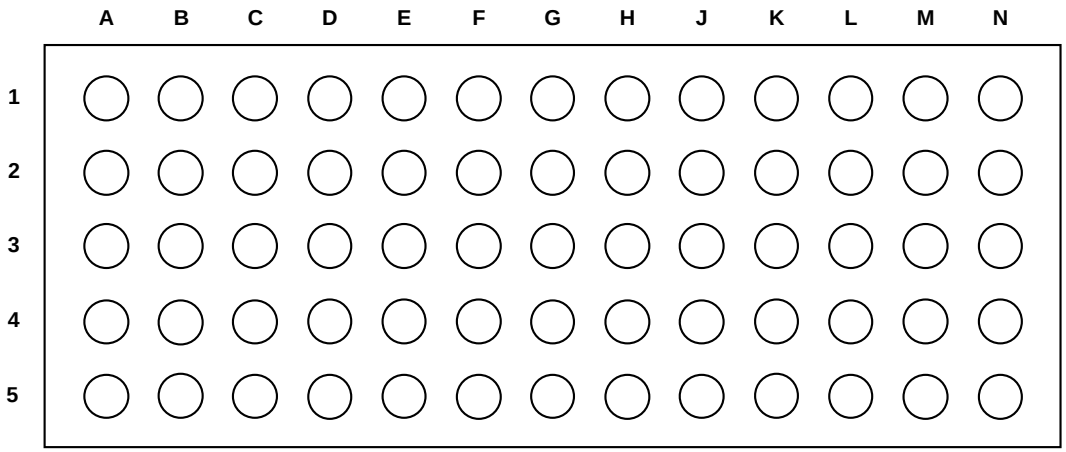
Pin name	Pin no.	Type	Reset	Domain	Description
PB4 PB5 PB6 PB7 PB8 PB9 PB10 PB11	74 75 92 93 94 44 45 46				
PDM_DATA2	47	I/O, FS	I; PL	PIF	PDM input data channel 2.
PDM_DATA3	48	I/O, FS	I; PL	PIF	PDM input data channel 3.
VDDA_PLL	49	P	-	1.8V	Power supply **(PLL)**.
VDDA_OTP	50	P	-	1.8V	Power supply **(OTP)**.
N.C.	51,61 67,68 69,82 85	-	-	-	No connection pin. It should be floating.
VDDA_TX	52	P	-	1.8V	Power supply **(MIPI TX)**.
TX_DN0	53	AO	-	-	MIPI TX data lane 0 negative output.
TX_DP0	54	AO	-	-	MIPI TX data lane 0 positive output.
TX_CKN	55	AO	-	-	MIPI TX clock negative output.
TX_CKP	56	AO	-	-	MIPI TX clock positive output.
TX_DN1	58	AO	-	-	MIPI TX data lane 1 negative output.
TX_DP1	59	AO	-	-	MIPI TX data lane 1 positive output.
DCDC_OUT	60	PO	-	-	DC-DC output **(0.8/0.9V)**.
VX2	62	AIO	-	-	Inductor termination for DC-DC. Connect to external inductor output side.
VX1	63	AIO	-	-	Inductor termination for DC-DC. Connect to external inductor input side.
VDDA_DCDC	64	P	-	1.8/3.3V	Power supply **(DC-DC)**.
I2CM_SDA	70	I/O, FS	I; PH	PIF	I^2C master data.
I2CM_SCL	71	I/O, FS	I; PH	PIF	I^2C master clock.
SPIS_DO	77	I/O, FS	I; PL	PIF	SPI slave data output.
SPIS_DI	78	I, FS	I; PL	PIF	SPI slave data input.
SPIS_CLK	79	I, FS	I; PL	PIF	SPI slave clock.
SPIS_CS	80	I, FS	I; PL	PIF	SPI slave chip select.
SD_CLK	86	I/O, FS	I; PL	PIF	SD/SDIO clock.
SD_CMD	87	I/O, FS	I; PL	PIF	SD/SDIO command.
SD_DAT0	88	I/O, FS	I; PL	PIF	SD/SDIO data 0.
SD_DAT1	89	I/O, FS	I; PL	PIF	SD/SDIO data 1.
SD_DAT2	90	I/O, FS	I; PL	PIF	SD/SDIO data 2.
SD_DAT3	91	I/O, FS	I; PL	PIF	SD/SDIO data 3.
N.C.	95,97 98,101	-	-	-	No connection pin. It should be floating.
SEN_XSLEEP	99	O, FS	O	SIF	Sensor XSLEEP.
SEN_PCLK	100	I, FS	I	SIF	Sensor PCLK.
SEN_D0	102	I, FS	I	SIF	Sensor data Bit0.
SEN_D1	103	I, FS	I	SIF	Sensor data Bit1.
SEN_D2	104	I, FS	I	SIF	Sensor data Bit2.
SEN_D3	105	I, FS	I	SIF	Sensor data Bit3.
SEN_D4	106	I, FS	I	SIF	Sensor data Bit4.
SEN_MCLK	107	O, FS	O	SIF	Sensor MCLK.
SEN_D5	109	I, FS	I	SIF	Sensor data Bit5.
SEN_D6	110	I, FS	I	SIF	Sensor data Bit6.
SEN_D7	111	I, FS	I	SIF	Sensor data Bit7.
XTAL_24M_O	112	O	O	SIF	Crystal 24MHz output.
XTAL_24M_I	113	I	I	SIF	Crystal 24MHz input.
RX_DP1	116	AI	-	-	MIPI RX data lane 1 positive input.
VDDA_RX	117	P	-	1.8V	Power supply **(MIPI RX)**.

Pin name	Pin no.	Type	Reset	Domain	Description
RX_DN1	118	AI	-	-	MIPI RX data lane 1 negative input.
RX_CKP	119	AI	-	-	MIPI RX clock positive input.
RX_CKN	120	AI	-	-	MIPI RX clock negative input.
RX_DP0	121	AI	-	-	MIPI RX data lane 0 positive input.
RX_DN0	122	AI	-	-	MIPI RX data lane 0 negative input.
SEN_FVALID	124	I, FS	I	SIF	Sensor frame valid.
SEN_LVALID	125	I, FS	I	SIF	Sensor line valid.
QSPI_DIO0	126	I/O, FS	O	SIF	QSPI data 0 for Flash.
QSPI_CLK	127	O, FS	O	SIF	QSPI clock for Flash.
QSPI_DIO3	128	I/O, FS	O	SIF	QSPI data 3 for Flash.

Table 4.1: LQFP128 pin assignment

4.2. WLCSP65

	A	B	C	D	E	F	G	H	J	K	L	M	N	
1	QSPI_DIO2	QSPI_DIO0	RX_DP0	RX_DN1	RX_DP1	XTAL_24M_O	SEN_D1	SEN_D0	SEN_PCLK	SEN_XSLEEP	PB8	PB7	PB6	1
2	SEN_INT	QSPI_CS	QSPI_CLK	RX_DN0	RX_CKN	RX_CKP	XTAL_24M_I	SEN_MCLK	SEN_D3	SEN_D2	VDDIO_SIF	GND	VDDIO_PIF	2
3	SEN_I2CM_SCL	SEN_I2CM_SDA	SEN_GPIO	QSPI_DIO1	QSPI_DIO3	VDDIO_SIF	VDDA_RX	GND	PB11	TX_CKP	GND	PB3	PB5	3
4	PA2	PA3	PA1	PA0	TEST_MODE	BOOT_OPT	GND	TX_DN0	TX_CKN	TX_DP1	DCDC_OUT	GND	PB4	4
5	PB0	PB1	GND	VDDIO_AON	RESETN	PB9	PB10	VDDA_TX	TX_DP0	TX_DN1	VX1	VDDA_DCDC	PB2	5
	A	B	C	D	E	F	G	H	J	K	L	M	N	



Bottom View

Figure 4.2: WLCSP65 ball map

Pin Types: **A**=Analog, **I**=Input, **O**=Output, **P**=Power, **G**=Ground, **FS**=Fail-Safe
Reset States: **PH**=Pull High, **PL**=Pull Low
Pin Domains: **SIF**=1.8V only, **PIF**=1.8V or 3.3V, **AON**=1.8V or 3.3V **(always-on)**

Pin name	Pin no.	Type	Reset	Domain	Description
RX_DP1	E1	AI	-	-	MIPI RX data lane 1 positive input.
RX_DN1	D1	AI	-	-	MIPI RX data lane 1 negative input.
RX_DP0	C1	AI	-	-	MIPI RX data lane 0 positive input.
RX_DN0	D2	AI	-	-	MIPI RX data lane 0 negative input.
RX_CKP	F2	AI	-	-	MIPI RX clock positive input.
RX_CKN	E2	AI	-	-	MIPI RX clock negative input.
TX_DP1	K4	AO	-	-	MIPI TX data lane 1 positive output.
TX_DN1	K5	AO	-	-	MIPI TX data lane 1 negative output.
TX_DP0	J5	AO	-	-	MIPI TX data lane 0 positive output.
TX_DN0	H4	AO	-	-	MIPI TX data lane 0 negative output.
TX_CKP	K3	AO	-	-	MIPI TX clock positive output.
TX_CKN	J4	AO	-	-	MIPI TX clock negative output.
SEN_MCLK	H2	O, FS	O	SIF	Master clock output for image sensor.
SEN_PCLK	J1	I, FS	I	SIF	Pixel clock input from image sensor.
SEN_D0	H1	I, FS	I	SIF	Sensor data Bit0.
SEN_D1	G1	I, FS	I	SIF	Sensor data Bit1.
SEN_D2	K2	I, FS	I	SIF	Sensor data Bit2.
SEN_D3	J2	I, FS	I	SIF	Sensor data Bit3.
SEN_XSLEEP	K1	O, FS	O	SIF	Sensor XSLEEP.
SEN_INT	A2	I, FS	I; PL	SIF	Sensor interrupt.
SEN_GPIO	C3	I/O, FS	I	SIF	Power down and reset control for image sensor.
SEN_I2CM_SDA	B3	I/O, FS	I	SIF	I^2C master data for image sensor.
SEN_I2CM_SCL	A3	I/O, FS	I	SIF	I^2C master clock for image sensor.
PA0 PA1	D4 C4	I/O, FS	I; PL	AON	General-purpose IO, group A.
PA2 PA3	A4 B4	I/O, FS	I; PH	AON	General-purpose IO, group A.
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7 PB8 PB9 PB10 PB11	A5 B5 N5 M3 N4 N3 N1 M1 L1 F5 G5 J3	I/O, FS	I; PL	PIF	General-purpose IO, group B.
XTAL_24M_O	F1	O	O	SIF	Crystal 24MHz output.
XTAL_24M_I	G2	I	I	SIF	Crystal 24MHz input.
BOOT_OPT	F4	I	I; PL	AON	Boot option selection pin.
TEST_MODE	E4	I	I; PL	AON	Test mode.
RESETN	E5	I, FS	I; PH	AON	Reset pin.
QSPI_CLK	C2	O, FS	O	SIF	QSPI clock for Flash.
QSPI_CS	B2	O, FS	O	SIF	QSPI chip select for Flash.
QSPI_DIO0	B1	I/O, FS	O	SIF	QSPI data 0 for Flash.
QSPI_DIO1	D3	I/O, FS	I, PL	SIF	QSPI data 1 for Flash.
QSPI_DIO2	A1	I/O, FS	O	SIF	QSPI data 2 for Flash.
QSPI_DIO3	E3	I/O, FS	O	SIF	QSPI data 3 for Flash.
VDDIO_SIF	F3, L2	P	-	1.8V	I/O supply **(Image sensor GPIOs, SIF)**.

Pin name	Pin no.	Type	Reset	Domain	Description
VDDIO_PIF	N2	P	-	1.8/3.3V	I/O supply **(Peripheral GPIOs, PIF)**.
VDDIO_AON	D5	P	-	1.8/3.3V	I/O supply **(AON GPIOs)**.
VDDA_DCDC	M5	P	-	1.8/3.3V	Power supply **(DC-DC)**.
VDDA_TX	H5	P	-	1.8V	Power supply **(MIPI TX, OTP and PLL)**.
VDDA_RX	G3	P	-	1.8V	Power supply **(MIPI RX)**.
VX1	L5	AIO	-	-	Inductor termination for DC-DC. Connect to external inductor input side.
DCDC_OUT	L4	PO	-	-	DC-DC output **(0.8/0.9V)**. Connect to external inductor output side.
GND	C5, G4 H3, L3 M2, M4	G	-	Ground	Ground.

Table 4.2: WLCSP65 pin assignment

4.3. QFN88

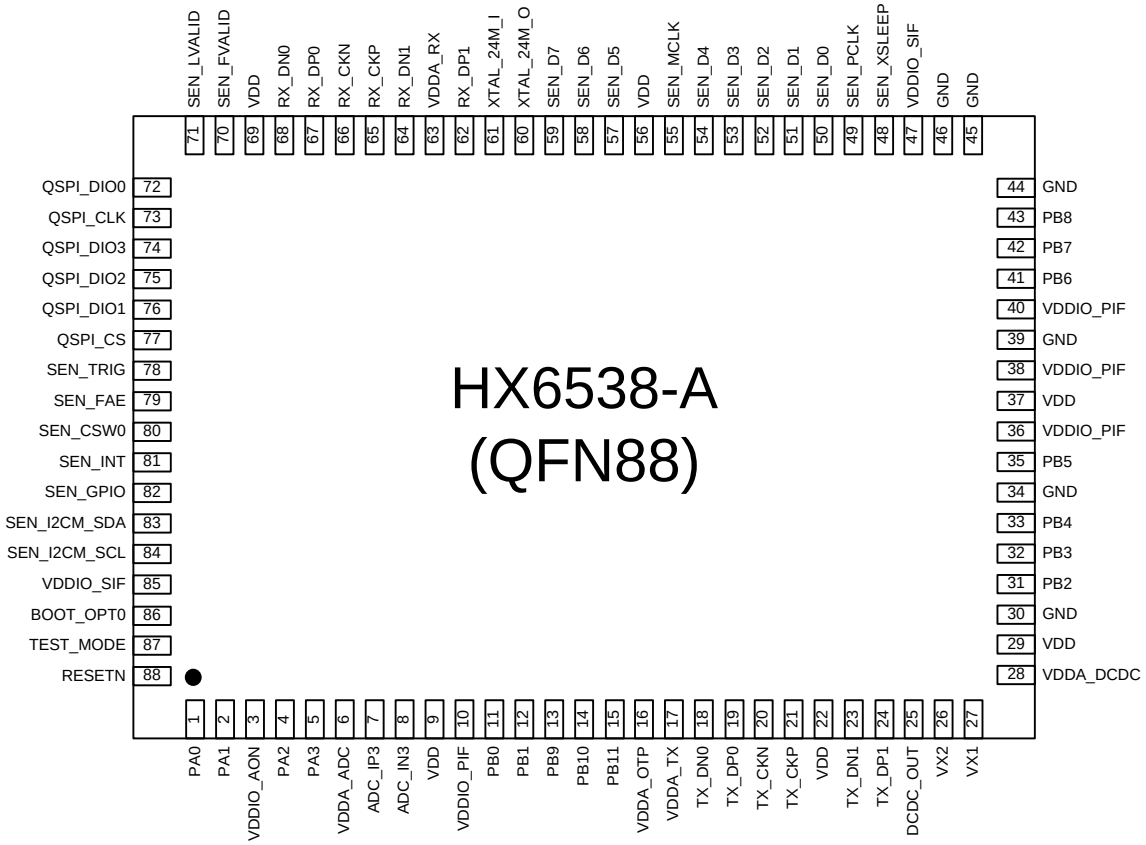


Figure 4.3: QFN88 pin assignment (top view)

Pin Types: **A**=Analog, **I**=Input, **O**=Output, **P**=Power, **G**=Ground, **FS**=Fail-Safe
Reset States: **PH**=Pull High, **PL**=Pull Low
Pin Domains: **SIF**=1.8V only, **PIF**=1.8V or 3.3V, **AON**=1.8V or 3.3V **(always-on)**

Pin name	Pin no.	Type	Reset	Domain	Description
PA0 PA1	1 2	I/O, FS	I; PL	AON	General-purpose IO, group A.
VDDIO_AON	3	P	-	1.8/3.3V	I/O supply **(AON GPIOs)**.
PA2 PA3	4 5	I/O, FS	I; PH	AON	General-purpose IO, group A.
VDDA_ADC	6	P	-	1.8/3.3V	Power supply **(ADC)**.
ADC_IP3	7	AI	-	-	ADC input Ch3_P.
ADC_IN3	8	AI	-	-	ADC input Ch3_N.
VDD	9,22 29,37 56,69	P	-	0.8/0.9V	Power supply from DC-DC output.
VDDIO_PIF	10,36 38,40	P	-	1.8/3.3V	I/O supply **(peripheral GPIOs, PIF)**.
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7 PB8 PB9 PB10 PB11	11 12 31 32 33 35 41 42 43 13 14 15	I/O, FS	I; PL	PIF	General-purpose IO, group B.
VDDA_OTP	16	P	-	1.8V	Power supply **(OTP and PLL)**.
VDDA_TX	17	P	-	1.8V	Power supply **(MIPI TX)**.
TX_DN0	18	AO	-	-	MIPI TX data lane 0 negative output.
TX_DP0	19	AO	-	-	MIPI TX data lane 0 positive output.
TX_CKN	20	AO	-	-	MIPI TX clock negative output.
TX_CKP	21	AO	-	-	MIPI TX clock positive output.
TX_DN1	23	AO	-	-	MIPI TX data lane 1 negative output.
TX_DP1	24	AO	-	-	MIPI TX data lane 1 positive output.
DCDC_OUT	25	PO	-	-	DC-DC output **(0.8/0.9V)**.
VX2	26	AIO	-	-	Inductor termination for DC-DC. Connect to external inductor output side.
VX1	27	AIO	-	-	Inductor termination for DC-DC. Connect to external inductor input side.
VDDA_DCDC	28	P	-	1.8/3.3V	Power supply **(DC-DC)**.
GND	30,34 39,44 45,46	G	-	Ground	Ground.
VDDIO_SIF	47,85	P	-	1.8V	I/O supply **(Image sensor GPIOs, SIF)**.
SEN_XSLEEP	48	O, FS	O	SIF	Sensor XSLEEP.
SEN_PCLK	49	I, FS	I	SIF	Sensor PCLK.
SEN_D0	50	I, FS	I	SIF	Sensor data Bit0.
SEN_D1	51	I, FS	I	SIF	Sensor data Bit1.
SEN_D2	52	I, FS	I	SIF	Sensor data Bit2.
SEN_D3	53	I, FS	I	SIF	Sensor data Bit3.
SEN_D4	54	I, FS	I	SIF	Sensor data Bit4.
SEN_MCLK	55	O, FS	O	SIF	Sensor MCLK.
SEN_D5	57	I, FS	I	SIF	Sensor data Bit5.
SEN_D6	58	I, FS	I	SIF	Sensor data Bit6.

Pin name	Pin no.	Type	Reset	Domain	Description
SEN_D7	59	I, FS	I	SIF	Sensor data Bit7.
XTAL_24M_O	60	O	O	SIF	Crystal 24MHz output.
XTAL_24M_I	61	I	I	SIF	Crystal 24MHz input.
RX_DP1	62	AI	-	-	MIPI RX data lane 1 positive input.
VDDA_RX	63	P	-	1.8V	Power supply **(MIPI RX)**.
RX_DN1	64	AI	-	-	MIPI RX data lane 1 negative input.
RX_CKP	65	AI	-	-	MIPI RX clock positive input.
RX_CKN	66	AI	-	-	MIPI RX clock negative input.
RX_DP0	67	AI	-	-	MIPI RX data lane 0 positive input.
RX_DN0	68	AI	-	-	MIPI RX data lane 0 negative input.
SEN_FVALID	70	I, FS	I	SIF	Sensor frame valid.
SEN_LVALID	71	I, FS	I	SIF	Sensor line valid.
QSPI_DIO0	72	I/O, FS	O	SIF	QSPI data 0 for Flash.
QSPI_CLK	73	O, FS	O	SIF	QSPI clock for Flash.
QSPI_DIO3	74	I/O, FS	O	SIF	QSPI data 3 for Flash.
QSPI_DIO2	75	I/O, FS	O	SIF	QSPI data 2 for Flash.
QSPI_DIO1	76	I/O, FS	I, PL	SIF	QSPI data 1 for Flash.
QSPI_CS	77	O, FS	O	SIF	QSPI chip select for Flash.
SEN_TRIG	78	O, FS	O	SIF	Sensor trigger.
SEN_FAE	79	O, FS	O	SIF	Sensor frame auto exposure.
SEN_CSW0	80	O, FS	O	SIF	Sensor content switch0.
SEN_INT	81	I, FS	I; PL	SIF	Sensor interrupt.
SEN_GPIO	82	I/O, FS	I	SIF	Power down and reset control for image sensor.
SEN_I2CM_SDA	83	I/O, FS	I	SIF	I^2C master data for image sensor.
SEN_I2CM_SCL	84	I/O, FS	I	SIF	I^2C master clock for image sensor.
BOOT_OPT	86	I	I; PL	AON	Boot option selection pin.
TEST_MODE	87	I	I; PL	AON	Test mode.
RESETN	88	I, FS	I; PH	AON	Reset pin.

Table 4.3: QFN88 pin assignment

5. Electrical Characteristics

5.1. Absolute maximum ratings(1)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Supply voltage	VDDA_ADC VDDA_PLL VDDA_OTP VDDA_TX VDDA_RX VDDIO_SIF	-0.5	-	2.07	V
	VDD	-0.5	-	1.03	V
	VDDIO_PIF VDDIO_AON VDDA_DCDC	-0.5	-	3.63	V
CMOS/TTL input voltage	V_{IN}	-0.5	-	VDDIO	V
CMOS/TTL output voltage	V_{OUT}	-0.5	-	VDDIO	V
Storage temperature	T_{STG}	-40	-	125	°C
ESD Human body model(3)	V_{ESD_HBM}	-	-	2000	V
ESD Machine model(4)	V_{ESD_MM}	-	-	100	V
Latch-up current(5)	I_{LU}	-	-	100	mA

Note: (1) Device will probably be damaged permanently in case that the stresses are over the absolute maximum ratings listed above.
(3) HBM condition: T_A=25°C, Standard EIA /JEDEC JESD22-A114.
(4) MM condition: T_A=25°C, Standard EIA /JEDEC JESD22-A115.
(5) Latch-up condition: T_A=25°C, Standard JEDEC STANDARD NO.78 March 1997.

5.2. Recommended operating conditions

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Supply voltage	VDDA_ADC VDDA_PLL VDDA_OTP VDDA_TX VDDA_RX VDDIO_SIF	-	1.7	1.8	1.9	V
	VDD	M55.Big core at 400MHz U55 core at 400MHz M55.Little core at 150MHz	0.85	0.9	0.95	V
		M55.Big core at 150MHz U55 core at 150MHz M55.Little core at 75MHz	0.75	0.8	0.95	V
	VDDIO_PIF VDDIO_AON VDDA_DCDC(2)	-	1.7	1.8(3)	1.9	V
		-	3.1	3.3(3)	3.5	V
Operating temperature	T_A	-	-40	25	85	°C
Junction temperature	T_J	-	-40	-	105	°C

Note:

(2) VDDA_DCDC supply voltage must be the same with VDDIO_AON.

(3) According to the host controller's I/O voltage.

5.3. DC electrical characteristics

5.3.1. I/O Pins

(3.3V mode I/O parameters for AON/PIF domain GPIOs)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
High level input voltage	V_{IH}	-	2.0	-	VDDIO	V
Low level input voltage	V_{IL}	-	GND	-	0.8	V
High level output voltage	V_{OH}	I_{OH}=-2mA	2.4	-	VDDIO	V
Low level output voltage	V_{OL}	I_{OL}=2mA	GND	-	0.4	V

Table 5.1: 3.3V mode I/O DC parameters

(1.8V mode I/O parameters for AON/PIF/SIF domain GPIOs)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
High level input voltage	V_{IH}	-	0.7 x VDDIO	-	VDDIO	V
Low level input voltage	V_{IL}	-	GND	-	0.3 x VDDIO	V
High level output voltage	V_{OH}	I_{OH}=-2mA	0.8 x VDDIO	-	VDDIO	V
Low level output voltage	V_{OL}	I_{OL}=2mA	GND	-	0.2 x VDDIO	V

Table 5.2: 1.8V mode I/O DC parameters

5.3.2. MIPI transmitter

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
High speed transmit static common mode voltage(1)	V_{CMTX}	-	150	200	250	mV
V_{CMTX} mismatch when output is differential-1 or differential-0(2)	$\lvert\Delta V_{CMTX}\rvert_{(1,0)}$	-	-	-	5	mV
High speed transmit differential voltage(1)	$\lvert V_{OD}\rvert$	-	140	200	270	mV
V_{OD} mismatch when output is differential-1 or differential-0(2)	$\lvert\Delta V_{OD}\rvert$	-	-	-	14	mV
High speed output high voltage(1)	V_{OHHS}	-	-	-	360	mV
Single ended output impedance	Z_{OS}	-	40	50	62.5	Ω
Single ended output impedance mismatch	ΔZ_{OS}	-	-	-	10	%

Note: (1) Value when driving into load impedance anywhere in the Z_{ID} range.
(2) It is recommended the implementer minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ in order to minimize radiation and optimize signal integrity.

Table 5.3: MIPI HS-TX DC parameters

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Thevenin output high level	V_{OH}	-	1.1	1.2	1.3	V
Thevenin output low level	V_{OL}	-	-50	-	50	mV
Output impedance of low power transmitter(1)	Z_{OLP}	-	110	-	-	Ω

Note: (1) Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the T_{RLP}/T_{FLP} specification is met.

Table 5.4: MIPI LP-TX DC parameters

5.3.3. MIPI receiver

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Common-mode voltage HS receive mode(1)(2)	$V_{CMRX(DC)}$	-	70	-	330	mV
Differential input high threshold	V_{IDTH}	-	-	-	70	mV
Differential input low threshold	V_{IDTL}		-70	-	-	mV
Single-ended input high voltage(1)	V_{IHHS}	-	-	-	460	mV
Single-ended input low voltage(1)	V_{ILHS}	-	-40	-	-	mV
Single-ended threshold for HS termination enable	$V_{TERM-EN}$	-	-	-	450	mV
Differential input impedance	Z_{ID}	-	80	100	125	Ω

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance, and variations below 450MHz.

Table 5.5: MIPI HS-RX DC parameters

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Logic 1 input voltage	V_{IH}	-	800	-	-	mV
Logic 0 input voltage, not in ULP state	V_{IL}	-	-	-	550	mV
Logic 0 input voltage, ULP state	$V_{IL-ULPS}$	-	-	-	300	mV
Input hysteresis	V_{HYST}	-	25	-	-	mV

Table 5.6: MIPI LP-RX DC parameters

5.4. AC electrical characteristics

5.4.1. I²C interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9/0.8V	-	-	1	MHz
Data input setup time	t_{SU}	VDD=0.9/0.8V	50	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	5	-	-	ns

Table 5.7: I²C AC parameters

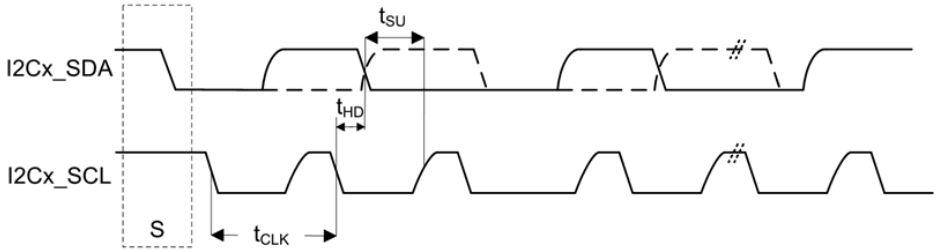


Figure 5.1: I²C bus timing

5.4.2. I³C interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9V	-	-	12.5	MHz
		VDD=0.8V	-	-	10	MHz
Data input setup time	t_{SU}	VDD=0.9/0.8V	6	-	-	ns
Data input hold time	t_{HD}	VDD=0.9V	3	-	-	ns
		VDD=0.8V	5	-	-	ns

Table 5.8: I³C AC parameters

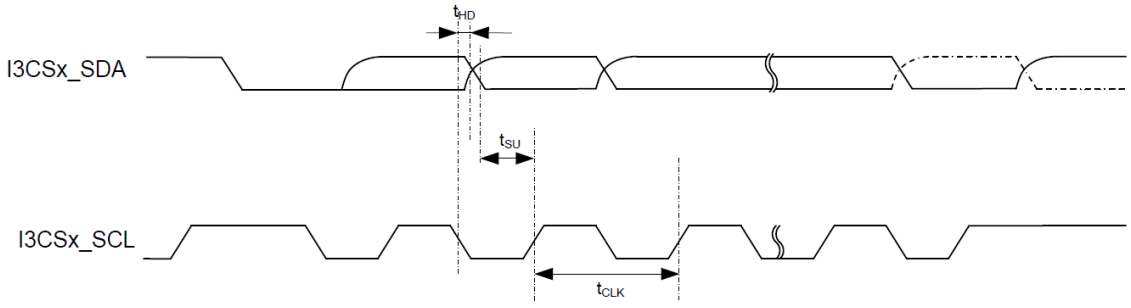


Figure 5.2: I³C bus timing

5.4.3. SPI interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9V	-	-	50	MHz
		VDD=0.8V	-	-	25	MHz
Data input setup time	t_{SU}	VDD=0.9/0.8V	4	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	0	-	-	ns
Data output valid time	t_{DV}	VDD=0.9/0.8V	-2(1)	-	8	ns

Note: (1) A negative time indicates the actual output data edge is earlier than clock appearing at pin.

Table 5.9: SPI master AC parameters

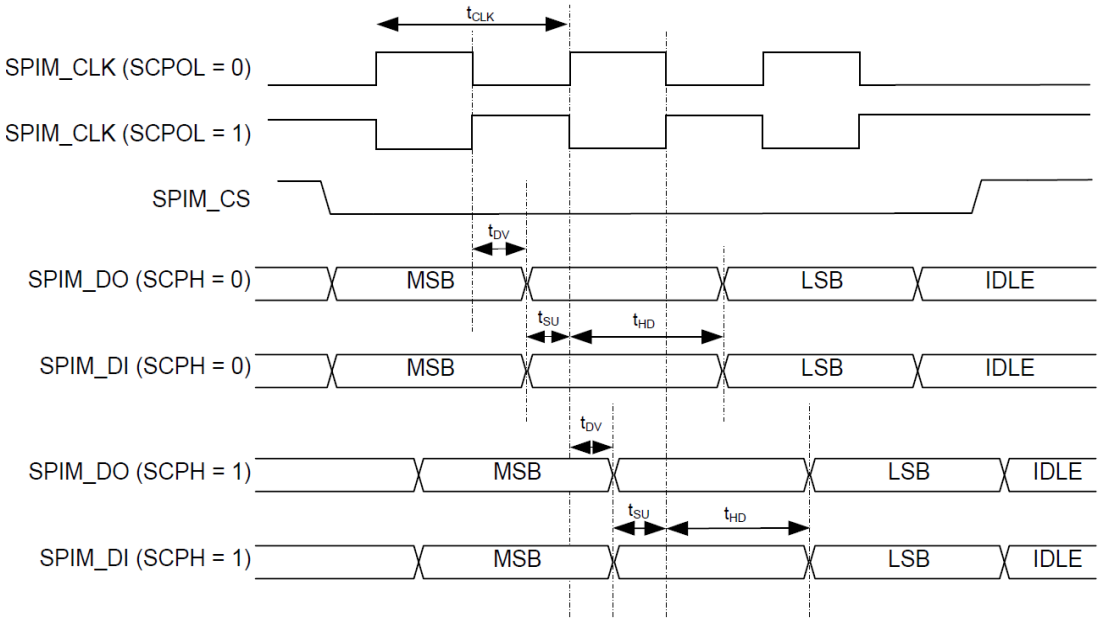


Figure 5.3: SPI master timing

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period(1)	t_{CLK}	VDD=0.9V	-	-	40	MHz
		VDD=0.8V	-	-	15	MHz
Data input setup time(1)	t_{SU}	VDD=0.9/0.8V	0	-	-	ns
Data input hold time(1)	t_{HD}	VDD=0.9V	10	-	-	ns
		VDD=0.8V	27	-	-	ns
Data output valid time(1)	t_{DV}	VDD=0.9V	10	-	22	ns
		VDD=0.8V	12	-	24	ns

Note: (1) SPIS_CLK, SPIS_DI, SPIS_DO signals are sampled by internal ssi_clk clock. The maximum clock period is one-tenth of ssi_clk frequency. The timing spec is based on ssi_clk frequency is 400MHz at 0.9V, and 150MHz at 0.8V.

Table 5.10: SPI slave AC parameters

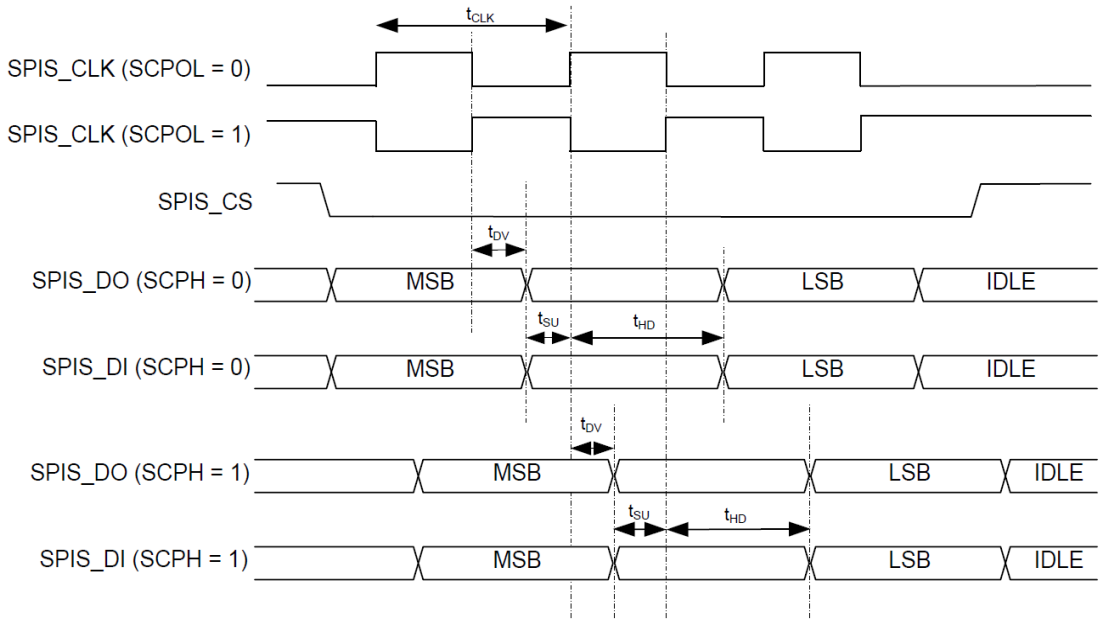


Figure 5.4: SPI slave timing

5.4.4. I²S interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9/0.8V	-	-	3.125	MHz
Clock HIGH	t_{WH}	VDD=0.9/0.8V	160	-	-	ns
Clock LOW	t_{WL}	VDD=0.9/0.8V	160	-	-	ns
Data input setup time	t_{SU}	VDD=0.9/0.8V	30	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	10	-	-	ns
Data output valid time	t_{DV}	VDD=0.9/0.8V	-	-	30	ns

Table 5.11: I²S master AC parameters

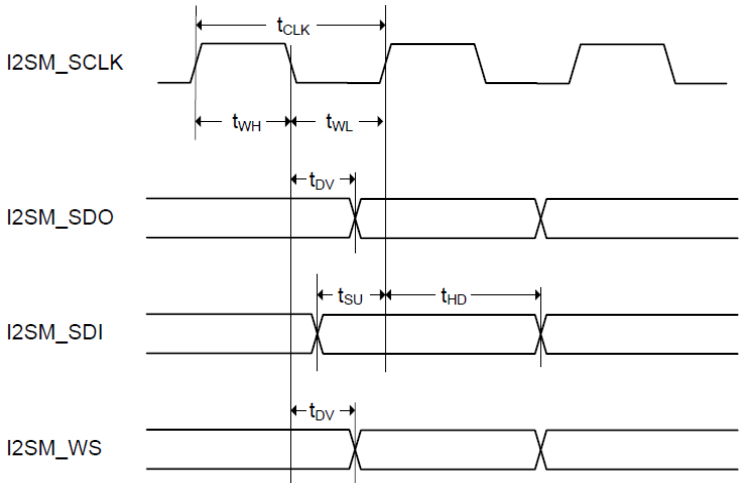


Figure 5.5: I²S master timing

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9/0.8V	-	-	3.125	MHz
Clock HIGH	t_{WH}	VDD=0.9/0.8V	160	-	-	ns
Clock LOW	t_{WL}	VDD=0.9/0.8V	160	-	-	ns
Data input setup time	t_{SU}	VDD=0.9/0.8V	30	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	0	-	-	ns
Data output valid time	t_{DV}	VDD=0.9/0.8V	-	-	30	ns

Table 5.12: I²S slave AC parameters

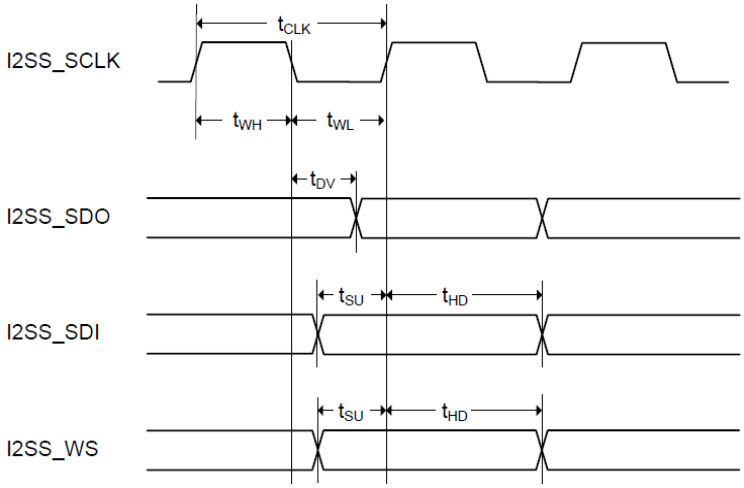


Figure 5.6: I²S slave timing

5.4.5. PDM interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9/0.8V	-	-	3.25	MHz
Data input setup time	t_{SU}	VDD=0.9/0.8V	30	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	5	-	-	ns

Table 5.13: PDM RX AC parameters

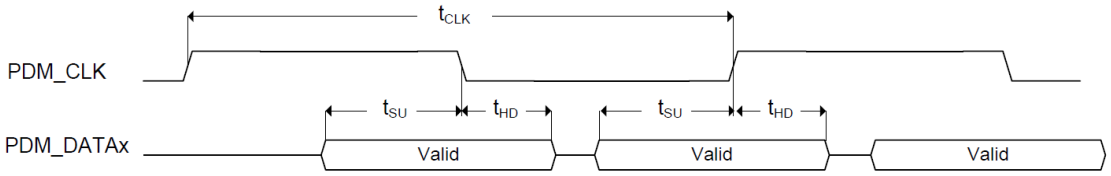


Figure 5.7: PDM RX timing

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9/0.8V	-	-	3.25	MHz
Clock path delay	t_{CLK_D}	VDD=0.9/0.8V	-	-	15	ns
Data path delay(1)	t_{DATA_D}	VDD=0.9/0.8V	-	-	15	ns

Note: (1) Only PDM_DATA0 input supports PDM pass-through mode.

Table 5.14: PDM pass-through AC parameters

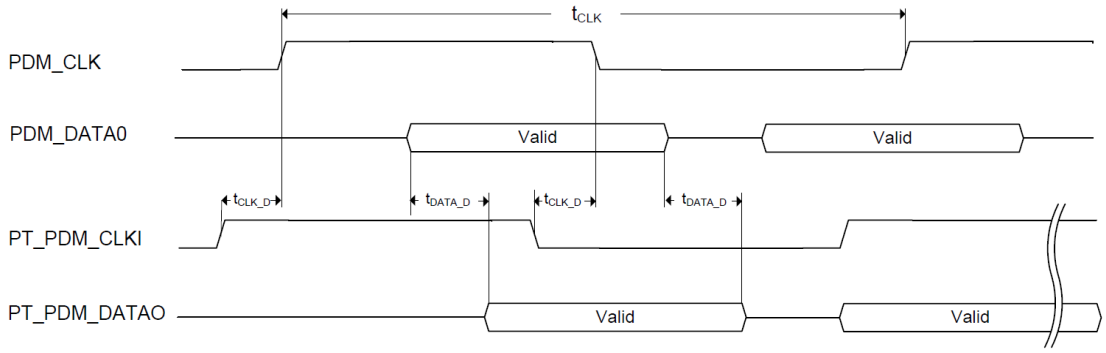


Figure 5.8: PDM pass-through timing

5.4.6. SD and SDIO host interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9V	-	-	25	MHz
		VDD=0.8V	-	-	12.5	MHz
Data input setup time	t_{SU}	VDD=0.9V	10	-	-	ns
		VDD=0.8V	13	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	3	-	-	ns
Data output valid time	t_{DV}	VDD=0.9V	-	-	14	ns
		VDD=0.8V	-	-	34	ns
Data output hold time	t_{OH}	VDD=0.9/0.8V	2	-	-	ns

Table 5.15: SD and SDIO host AC parameters

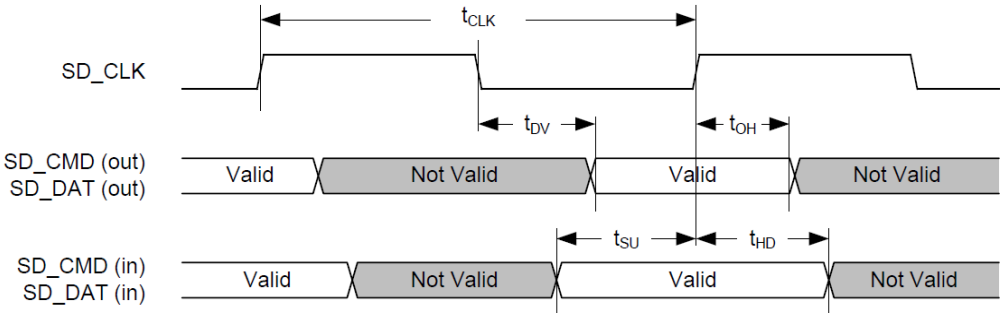


Figure 5.9: SD and SDIO host timing

5.4.7. DVP and SDI interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9V	-	-	72	MHz
		VDD=0.8V	-	-	40	MHz
Data input setup time	t_{SU}	VDD=0.9V	5	-	-	ns
		VDD=0.8V	11	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	6	-	-	ns

Table 5.16: DVP AC parameters

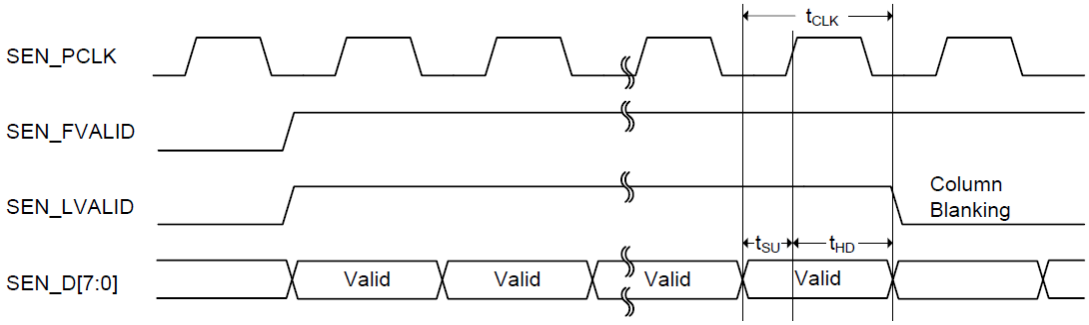


Figure 5.10: DVP interface timing

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9/0.8V	-	-	72	MHz
Data input setup time	t_{SU}	VDD=0.9/0.8V	3	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	6	-	-	ns

Table 5.17: SDI AC parameters

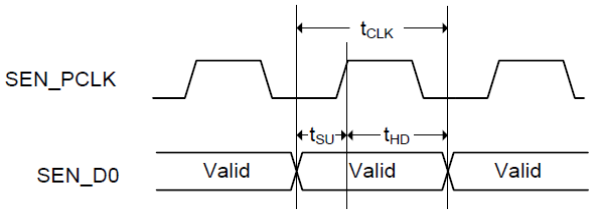


Figure 5.11: SDI interface timing

5.4.8. QSPI Flash interface(1)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9V	-	-	100	MHz
		VDD=0.8V	-	-	50	MHz
Data input setup time	t_{SU}	VDD=0.9/0.8V	-1(2)	-	-	ns
Data input hold time	t_{HD}	VDD=0.9V	6	-	-	ns
		VDD=0.8V	11	-	-	ns
Data output valid time	t_{DV}	VDD=0.9V	-	-	3	ns
		VDD=0.8V	-	-	15	ns
Data output hold time	t_{OH}	VDD=0.9/0.8V	-2(3)	-	-	ns

Note: (1) The timing values above are based on default software settings for QSPI sampling registers.
(2) A negative time indicates the actual capture edge inside the device is later than clock appearing at pin.
(3) A negative time indicates the actual output data edge is earlier than clock appearing at pin.

Table 5.18: QSPI Flash AC parameters

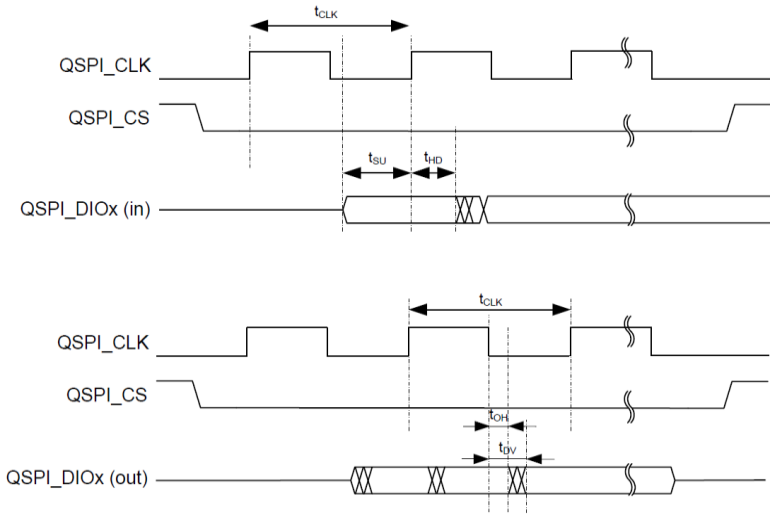


Figure 5.12: QSPI Flash interface timing

5.4.9. SWD debug interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock period	t_{CLK}	VDD=0.9/0.8V	-	-	15	MHz
Data input setup time	t_{SU}	VDD=0.9/0.8V	30	-	-	ns
Data input hold time	t_{HD}	VDD=0.9/0.8V	15	-	-	ns
Data output valid time	t_{DV}	VDD=0.9/0.8V	-	-	45	ns

Table 5.19: SWD debug AC parameters

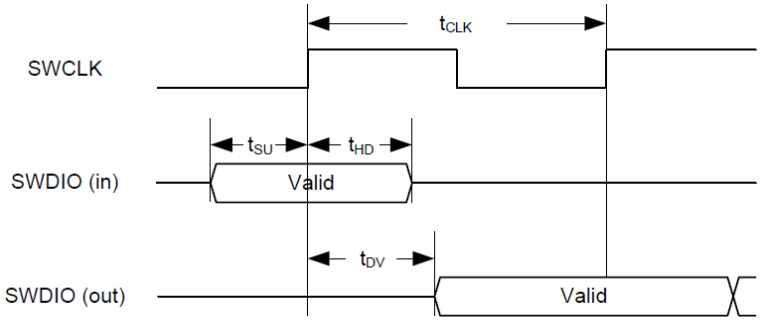


Figure 5.13: SWD debug interface timing

5.4.10. MIPI transmitter interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Common-level variations	$\Delta V_{CMTX(HF)}$	above 450MHz	-	-	15	mV_{RMS}
Common-level variations	$\Delta V_{CMTX(LF)}$	50-450MHz	-	-	25	mV_{PEAK}
Rise time and fall time	t_R and t_F	20% to 80%	-	-	0.3(1)(2)	UI
			-	-	0.35(1)(3)	UI
			-	-	0.4(4)	UI
			100(5)	-	-	ps

Note: (1) UI is equal to 1/(2*fh). See Ch. 8.3 of MIPI D-PHY specification for the definition of fh.
(2) Applicable when operating at HS bit rates ≤ 1Gbps **(UI ≥ 1ns)**.
(3) Applicable when operating at HS bit rates > 1Gbps **(UI < 1ns)**.
(4) Application for all HS Bit rate when supporting > 1.5Gbps.
(5) Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1Gbps **(UI ≥ 1ns)**, should not use values below 150ps.

Table 5.20: MIPI HS-TX AC parameters

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Rise time and fall time(1)	T_{RLP} /T_{FLP}	15% to 85%	-	-	25	ns
Rise time and fall time(1)(2)(3)	T_{REOT}	30% to 85%	-	-	35	ns
Pulse width of the LP exclusive-OR clock(4)	$T_{LP-PULSE-TX}$	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40	-	-	ns
		All other pulses	20	-	-	ns
Period of the LP exclusive-OR clock	$T_{LP-PER-TX}$	-	90	-	-	ns
Slew Rate(1)(5)(6)(7)(8)(9)	$\delta V/\delta t_{SR}$	C_{LOAD}=0 pF	30	-	500	mV/ns
		C_{LOAD}=5 pF	30	-	300	mV/ns
		C_{LOAD}=20 pF	30	-	250	mV/ns
		C_{LOAD}=70 pF	30	-	150	mV/ns
Load capacitance(1)	C_{LOAD}	20% to 80%	0	-	70	pF

Note: (1) C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
(2) The rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.
(3) With an additional load capacitance CCM between 0 and 60pF on the termination center tap at RX side of the lane.
(4) This parameter value can be lower than T_{LPX} due to differences in rise vs. fall signal slopes and trip levels and mismatches between DP and DN LP transmitters. Any LP exclusive-OR pulse observed during HS EoT **(transition from HS level to LP-11)** is glitch behavior.
(5) Measured as average across any 50mV segment of the output signal transition.
(6) This value represents a corner point in a piecewise linear curve.
(7) When the output voltage is in the range specified by VPIN **(absmax)**.
(8) When the output voltage is between 400mV and 930mV.
(9) When the output voltage is between 400mV and 700mV.

Table 5.21: MIPI LP-TX AC parameters

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Common-mode interference(1)	$\Delta V_{CMRX(HF)}$	above 450MHz	-	-	100	mV
Common-mode interference(2)(3)	$\Delta V_{CMRX(LF)}$	50-450MHz	-50	-	50	mV
Common-mode termination(4)	CCM	-	-	-	60	pF

Note: (1) $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.
(2) Excluding 'static' ground shift of 50mV.
(3) Voltage difference compared to the DC average common-mode potential.
(4) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 5.22: MIPI HS-RX AC parameters

5.4.11. MIPI receiver interface

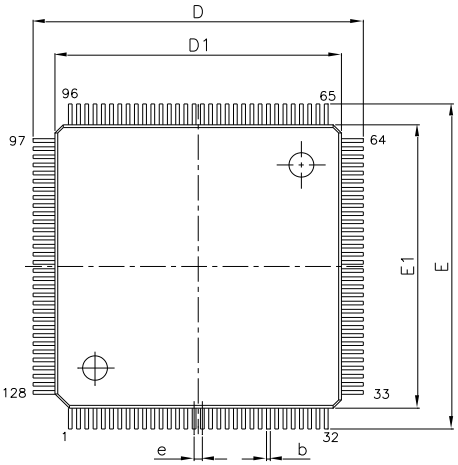
Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Input pulse rejection(1)(2)(3)	e_{SPIKE}	-	-	-	300	V.ps
Minimum pulse width response(4)	T_{MIN-RX}	-	20	-	-	ns
Peak Interference amplitude	V_{INT}	-	-	-	200	mV
Interference frequency	f_{INT}	-	450	-	-	MHz

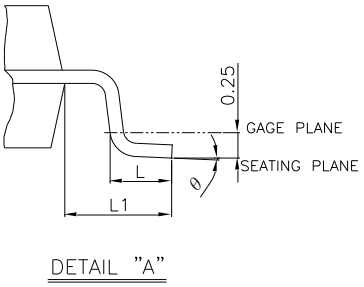
Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state.
(2) An impulse less than this will not change the receiver state.
(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
(4) An input pulse greater than this shall toggle the output.

Table 5.23: MIPI LP-RX AC parameters

6. Package Outline Dimension

6.1. LQFP128

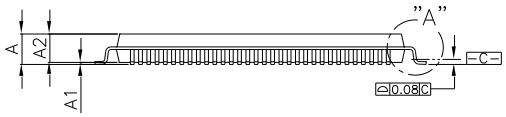




DETAIL "A"

Symbol	Min	Nom	Max
A	–	–	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
D	15.85	16.00	16.15
D1	13.90	14.00	14.10
E	15.85	16.00	16.15
E1	13.90	14.00	14.10
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

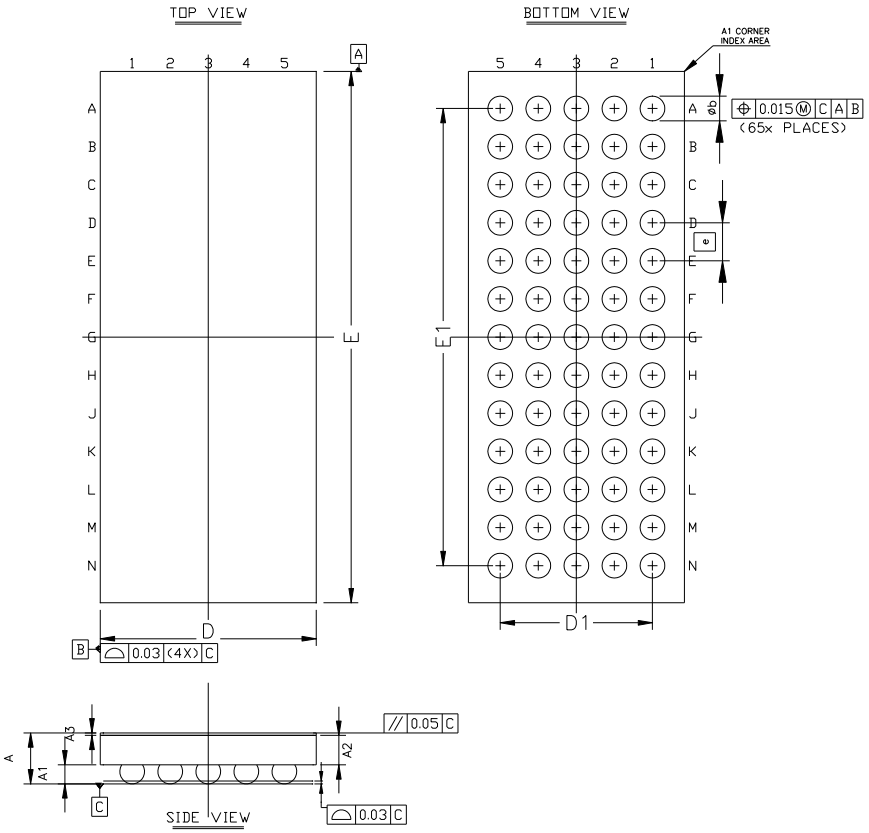
UNIT: MM



NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
   D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS
   INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE
   TO THE LOWEST POINT OF THE PACKAGE BODY.
6. REFERENCE DOCUMENT : JEDEC MS-026.

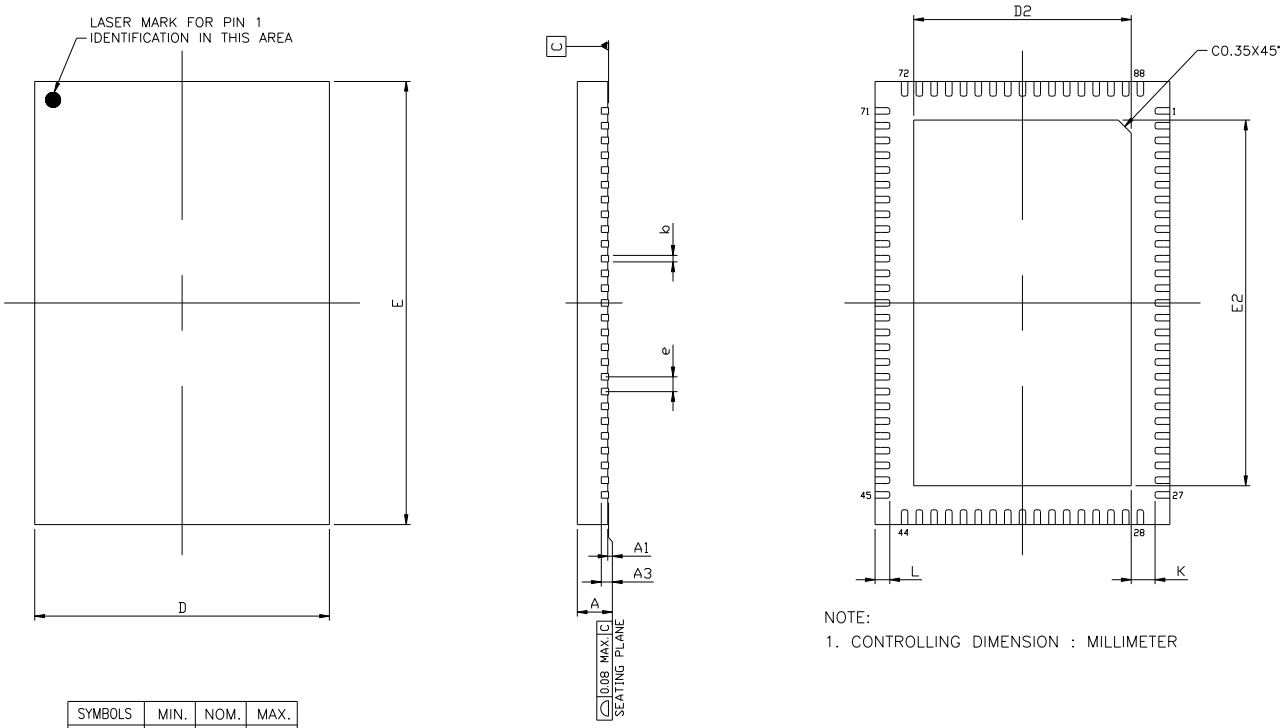
6.2. WLCSP65



SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	0.505	0.535	0.565
A1	0.18	0.2	0.22
A2	0.29	0.31	0.33
A3	0.025 BSC		
øb	0.24	0.26	0.28
D	2.240	2.273	2.306
D1	1.6 BSC		
E	5.551	5.584	5.617
E1	4.8 BSC		
e	0.4 BSC		

UNIT: MM

6.3. QFN88



NOTE:
1. CONTROLLING DIMENSION : MILLIMETER

SYMBOLS	MIN.	NOM.	MAX.
A	0.70	—	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
D	7.90	8.00	8.10
E	11.90	12.00	12.10
b	0.15	0.20	0.25
e	0.40 BSC		
L	0.30	0.40	0.50
K	0.20	—	—

Exposed pad size				
L/F	D2		E2	
	MIN.	MAX.	MIN.	MAX.
①	5.60	6.20	9.60	10.20

7. Ordering Information

Part no.	Package	Application	Description
HX6538-A04TLDG	LQFP128	AIoT, surveillance	WE2 AI processor
HX6538-A01TWA	WLCSP65	AIoT, Laptop, wearable	WE2 AI processor
HX6538-A06TDFG	QFN88	AIoT, surveillance	WE2 AI processor