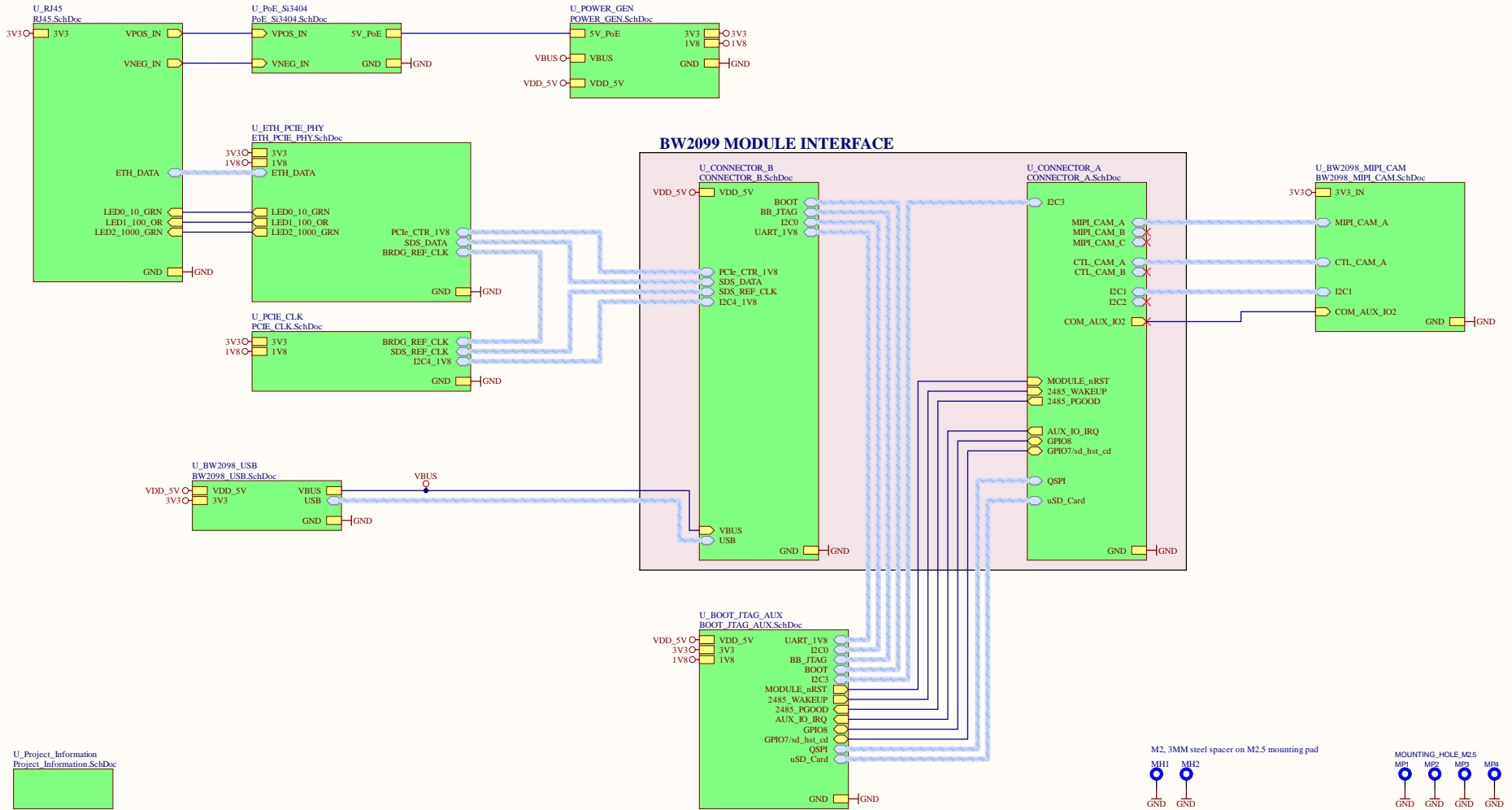


Project: BW2098POE
Current Revision: R4M1E3

BW2098POE Revision History:

Date	Revision	Reason for Change	Changes Implemented
3/4/2020	Initial Release -> R0M0E0		
5/29/2020	R0M0E0 --> R1M1E1	<ul style="list-style-type: none"> 1) Pull up the EN pin on the 3.3V regulator 2) R1 should be depopulated (PU for MA2485 WAKEUP line) 3) Add ESD protection diodes to the Ethernet lines 4) LEDs labels for "nRST" and "5V" are switched. 5) Polygon 3V3_L01_P425 is underneath GND polygon on Layer 1 and didn't pour correctly (still electrically connected by traces). 6) J5/J8 are a bit too close for both cable housings 7) RGB camera connector tab hard to get to as it's under the BW2099 8) Label the boot switches 9) King Top doesn't like the L1 inductor. Says it's too fragile and hard to handle. Try to find alternate. 	<ul style="list-style-type: none"> 1) 3.3V regulator EN pin pulled high to 5V 2) Depopulated R1 on Production variant 3) Added pads for ESD protection diodes on ethernet diff pairs 4) Swapped "nRST" and "5V" labels on overlay and added netnames to LEDs in schematic to help prevent this in the future. 5) Removed polygon and thickened traces 6) Increased connector spacing by 50mils to allow clearance 7) Moved connector 2mm right to make it a bit easier to grab the latch. Still not great, but better. 8) Added overlay labeling for each BOOT[4:0] and GPIO58 9) Moved the L1 inductor to L1 on layout so it wasn't so exposed to impacts. Did not change PN or schematic.
7/23/2020	R1M1E1 --> R2M1E2	<ul style="list-style-type: none"> 1) C35 preventing bridge from functioning properly. 2) Labeling of "GPIO6" is incorrect. Should be "GPIO8" 	<ul style="list-style-type: none"> 1) Removed C35 from PCB and BOM. 2) Changed references of GPIO6 to GPIO8. No physical change to PCB.
08/05/2022	R2M1E2 --> R3M1E3	<ul style="list-style-type: none"> 1) Move to universal camera FPC connector 2) No need for RST supervisor 3) Diodes for R145 no longer available? 4) Power jack not needed, USB power is OK 	<ul style="list-style-type: none"> 1) Changed connector to F32R-1A7H1-11026 and changed pinout 2) Removed RST supervisor 3) Replaced normal diodes with ideal diodes CD-HD01 4) Removed power jack and added USB power. Also removed input power selection jumper and replaced it with an OR gate ideal diodes.
08/31/2022	R3M1E3 -> R4M1E3	Camera connector was sticking out of PCB.	Moved connector back slightly so it doesn't protrude from the board.

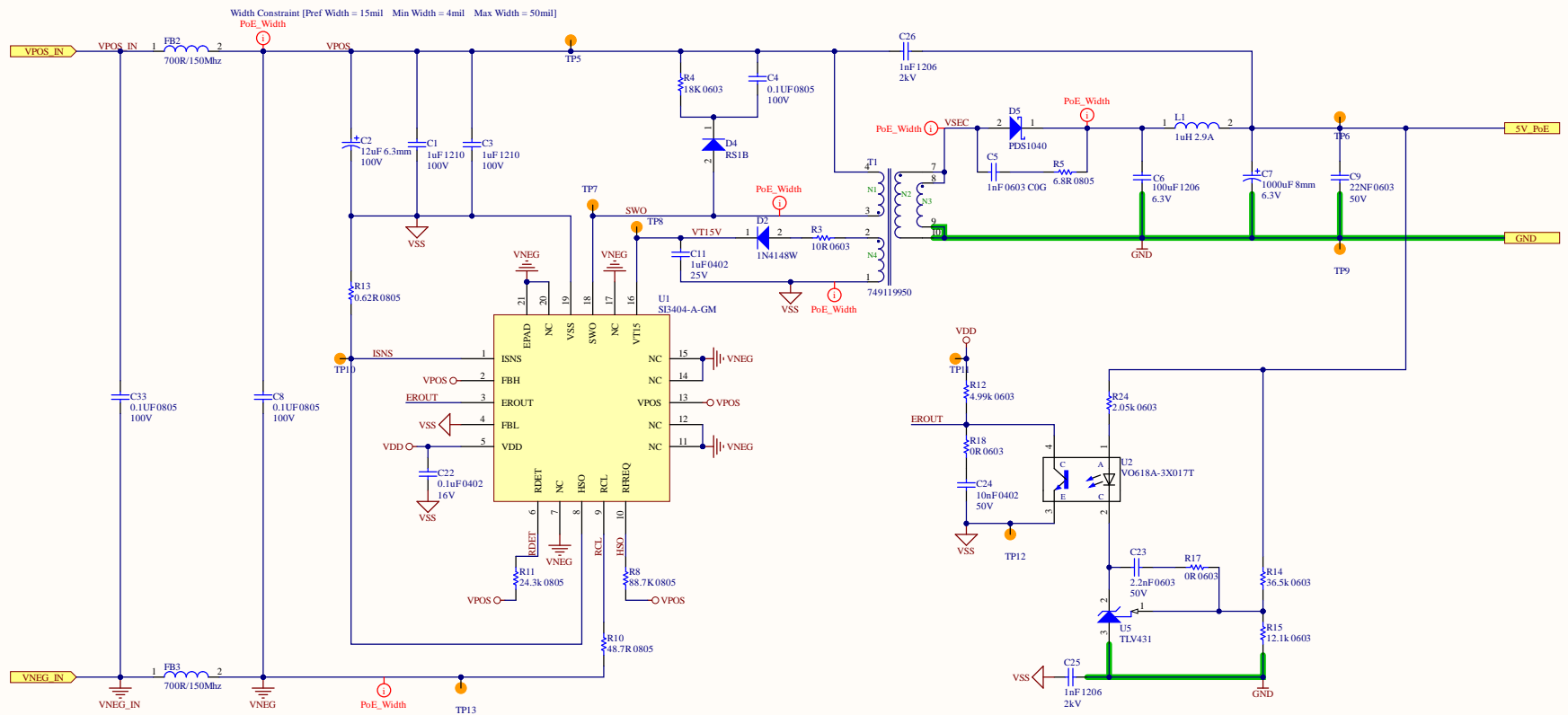
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Size: Tabloid	Number: D2098000	Revision: R4M1E3			
Date: 22/05/2024	Time: 18:23:35	Sheet 1 of 12	United States		
Drawn by: Brian Weinstein					



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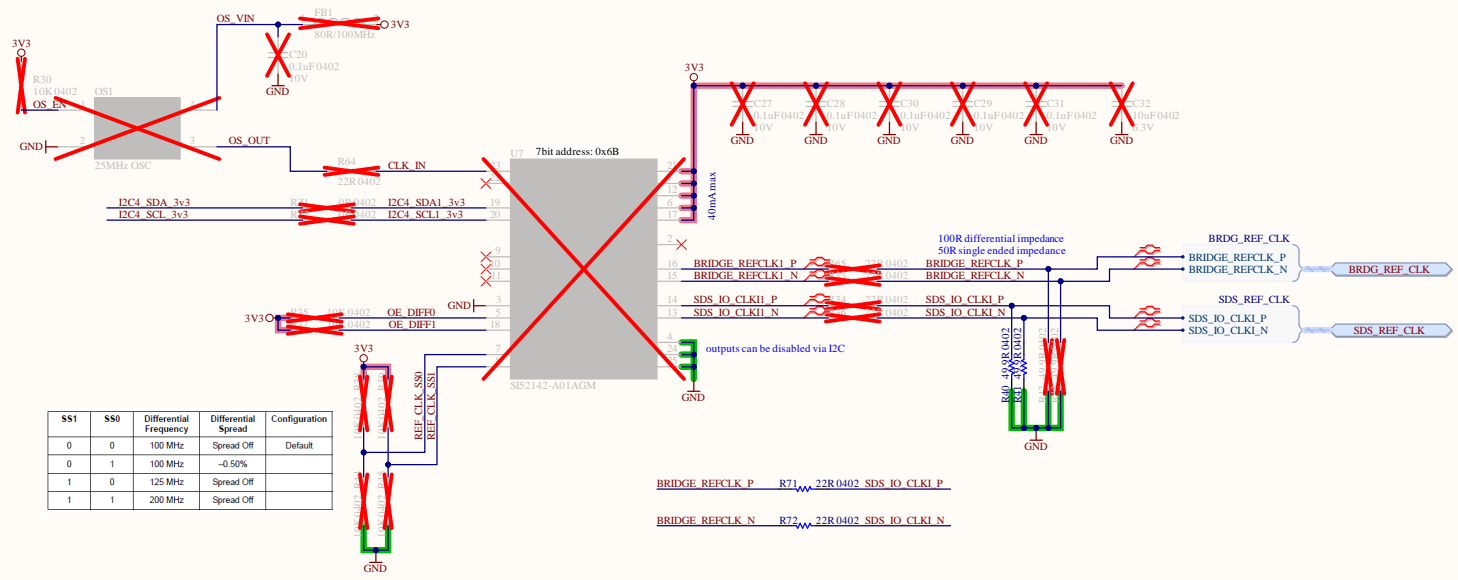
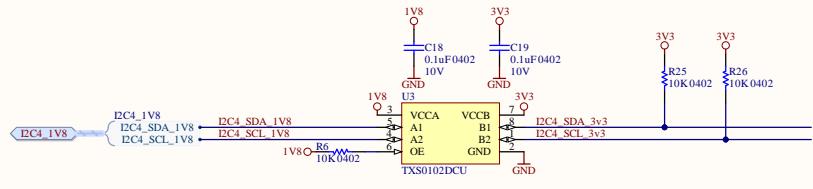
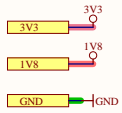
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Drawn by: Brian Weinstein					



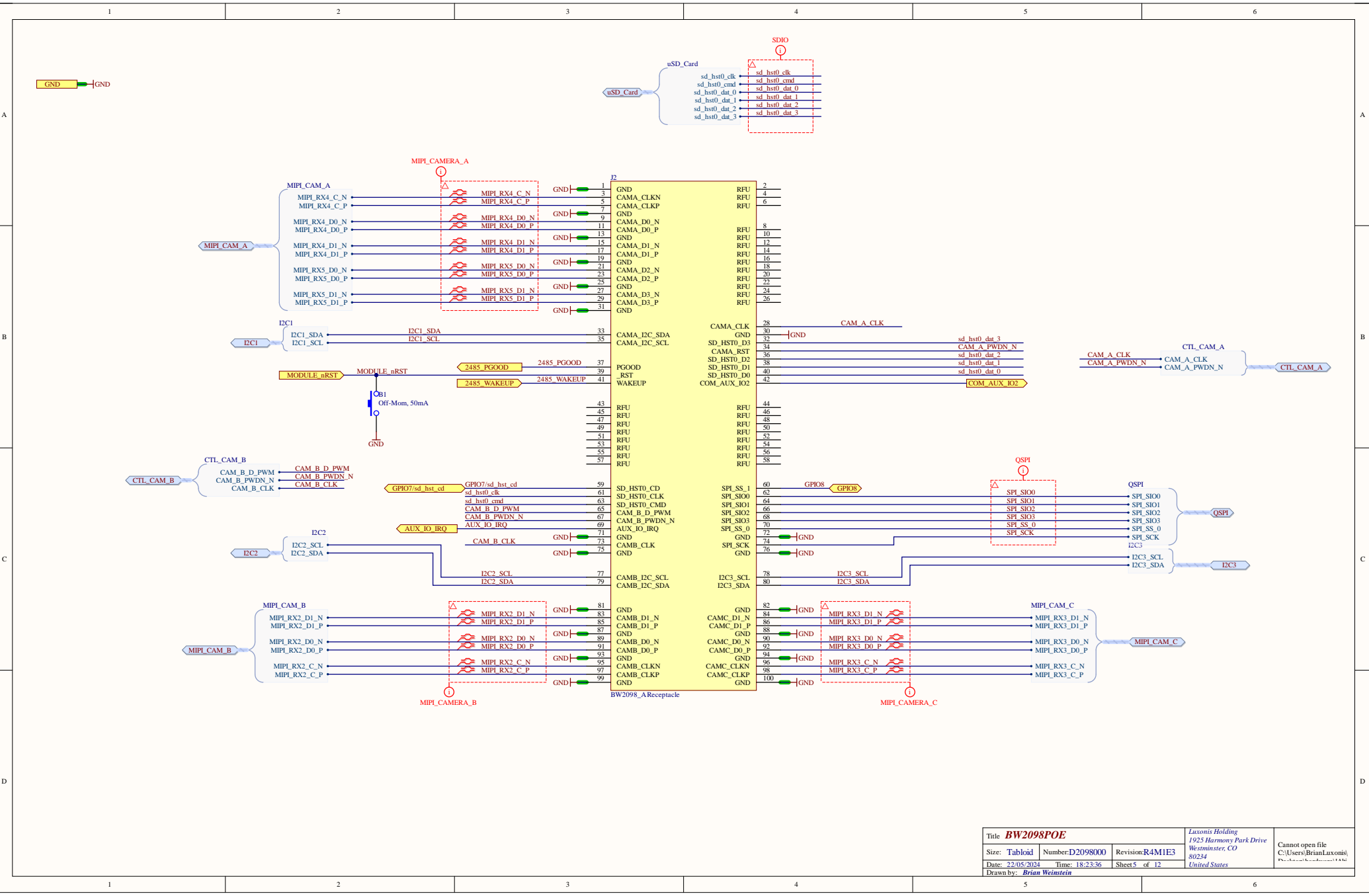
VNEG is a thermal plane as well as ESD and EMI. Use thermal vias to at least 1 inch square plane on backside.

Schematic based on the reference design for the SI3404 PoE.

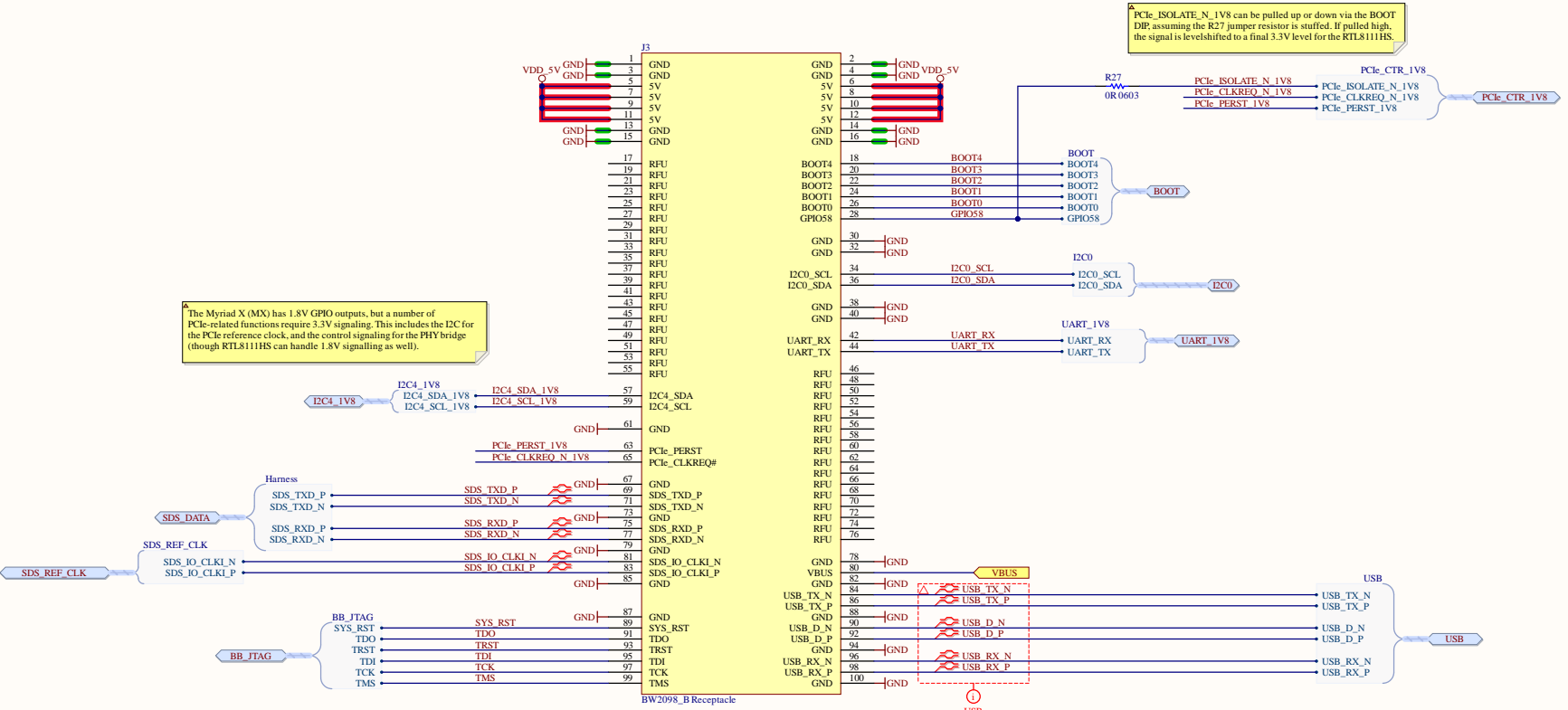
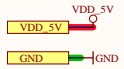
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Drawn by: <i>Brian Weinstein</i>				



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Drawn by: Brian Weinstein				



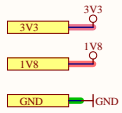
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Size: Tabloid	Number: D2098000	Revision: R4M1E3			
Date: 22/05/2024	Time: 18:23:36	Sheet 5 of 12			
Drawn by: <i>Brian Weinstein</i>					



The Myriad X (MX) has 1.8V GPIO outputs, but a number of PCIe-related functions require 3.3V signaling. This includes the I2C for the PCIe reference clock, and the control signaling for the PHY bridge (though RTL8111HS can handle 1.8V signaling as well).

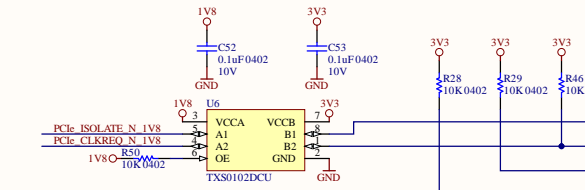
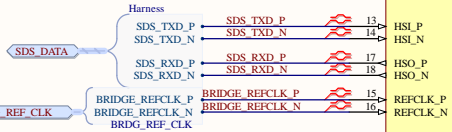
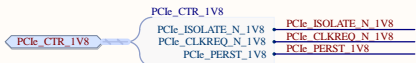
PCIe_ISOLATE_N_1V8 can be pulled up or down via the BOOT DIP, assuming the R27 jumper resistor is stuffed. If pulled high, the signal is levelshifted to a final 3.3V level for the RTL8111HS.

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Date: 22/05/2024	Time: 18:23:36	Sheet 6 of 12			
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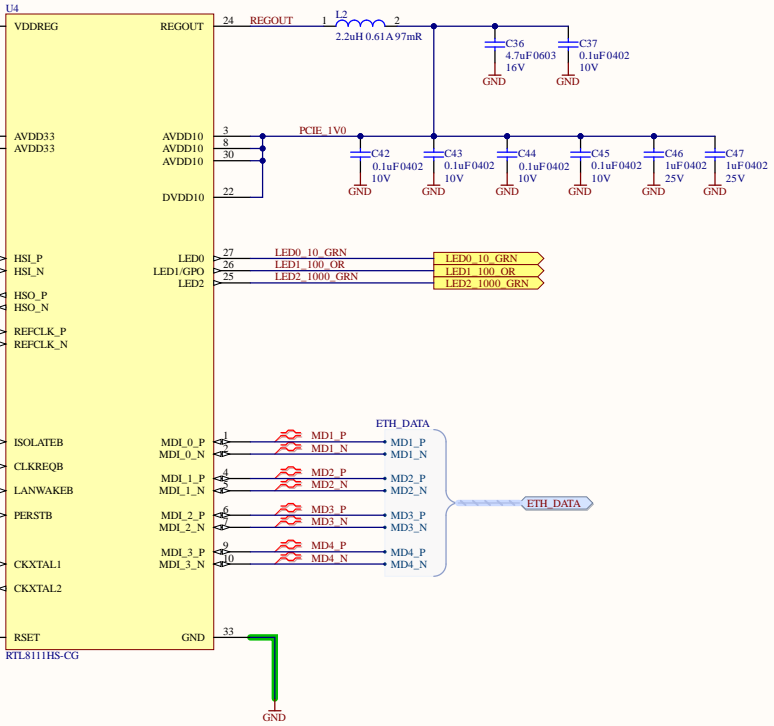
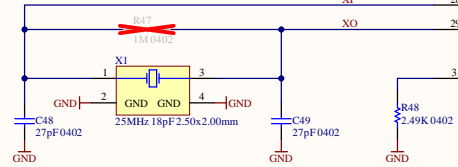


Power Sequence Requirements:
 - 3.3V POR ramp must be: 1ms < t < 100ms
 - All power inputs must be held >50ms at 0V between

Switching Regulator Layout:
 - VDDREG >40mils
 - REGOUT >60mils
 - Place caps and inductor as close as possible to the RTL8111HS
 - Place Lx and bulk C on the same layer as RTL8111HS
 - No additional inductance or FBs
 - Ceramic X5R caps or better

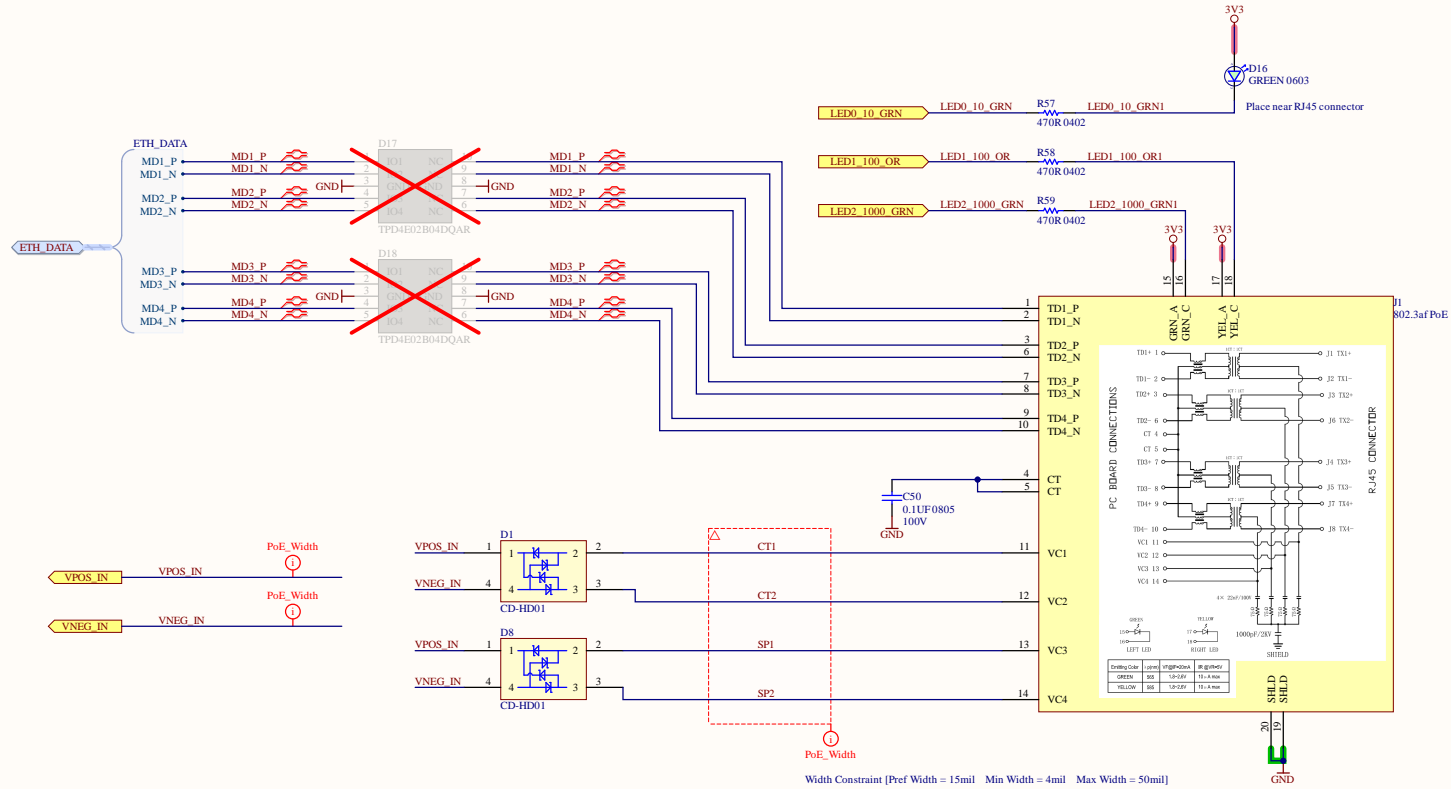


Drive PERST High to Enable PERST#
 PERST# signal is used to indicate when the power supply is within its specified voltage tolerance and is stable.
 Fundamental Reset for the PCIe Card



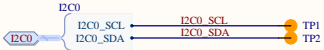
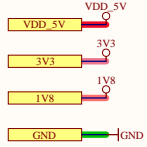
Schematic based on the reference design from the MV0247 PoE AOB reference design, with checking against the Realtek RTL8111HS reference design, layout guide, and datasheet.

Title BW2098POE			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States		Cannot open file C:\Users\Brian.Luxonis\...
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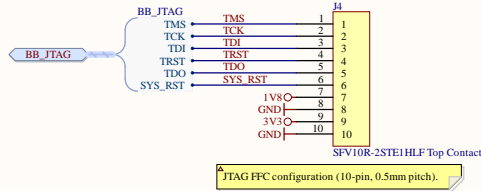


Width Constraint [Pref Width = 15mil Min Width = 4mil Max Width = 50mil]

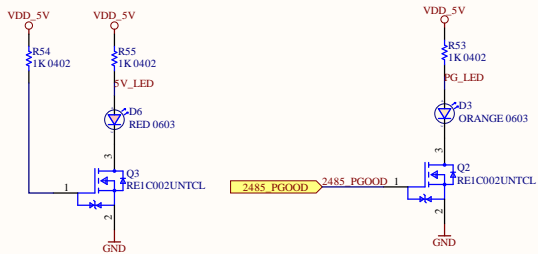
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Size: Tabloid	Number: D2098000	Revision: R4M1E3			
Date: 22/05/2024	Time: 18:23:36	Sheet 8 of 12			
Drawn by: <i>Brian Weinstein</i>					



LED INDICATORS



LED INDICATORS



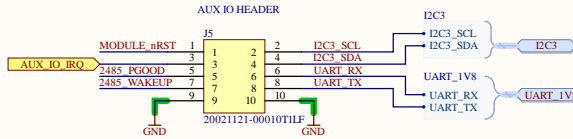
Mark "5V" on PCB

Mark "2485_PGOOD" on PCB

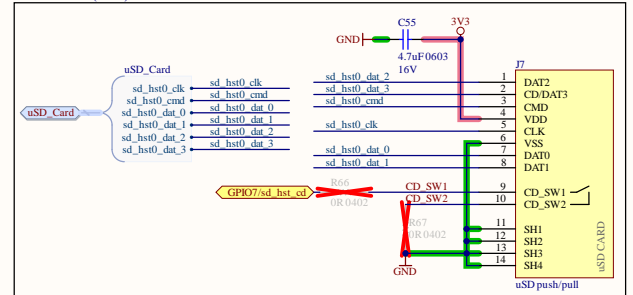
Mark "nRST" on PCB

2485_PGOOD and MODULE_nRST both have pull ups to 1.8V on 1099 module. 2485_PGOOD is held low by open-drain output on 1099 PMIC until power is good. MODULE_nRST rises with 1.8V at POR, but can be held low by user button or 1099 JTAG.

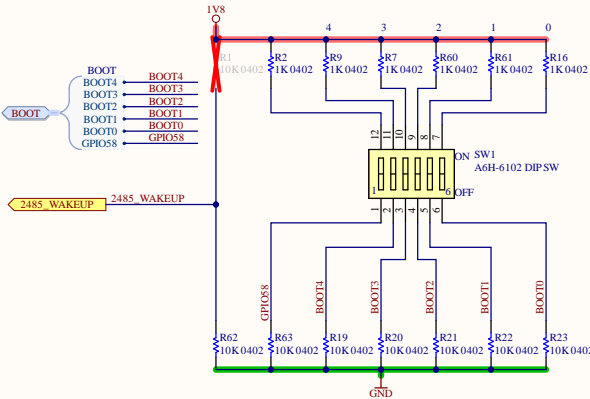
AUX IO HEADER



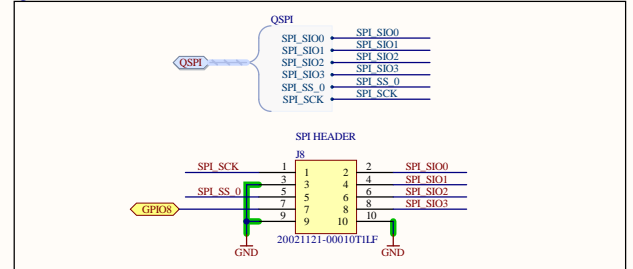
3.3V GPIO (uSD)



BOOT MODES



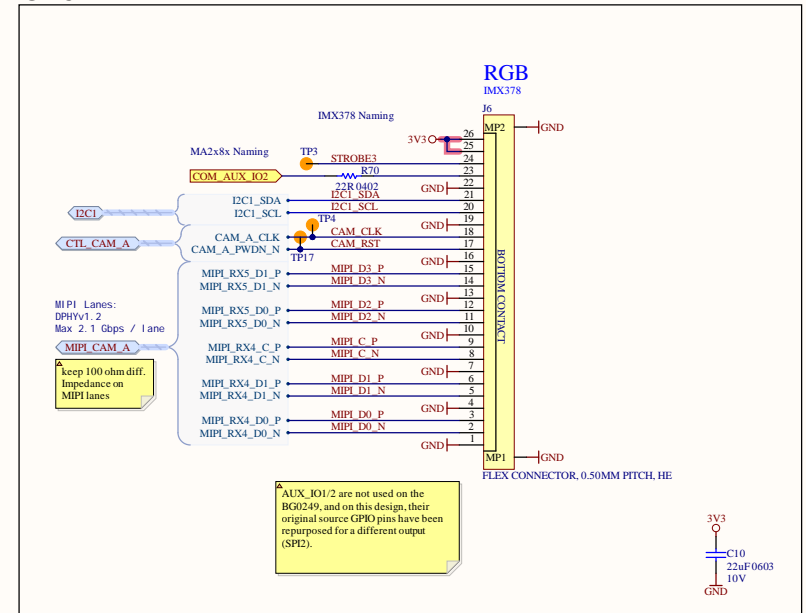
QUAD SPI



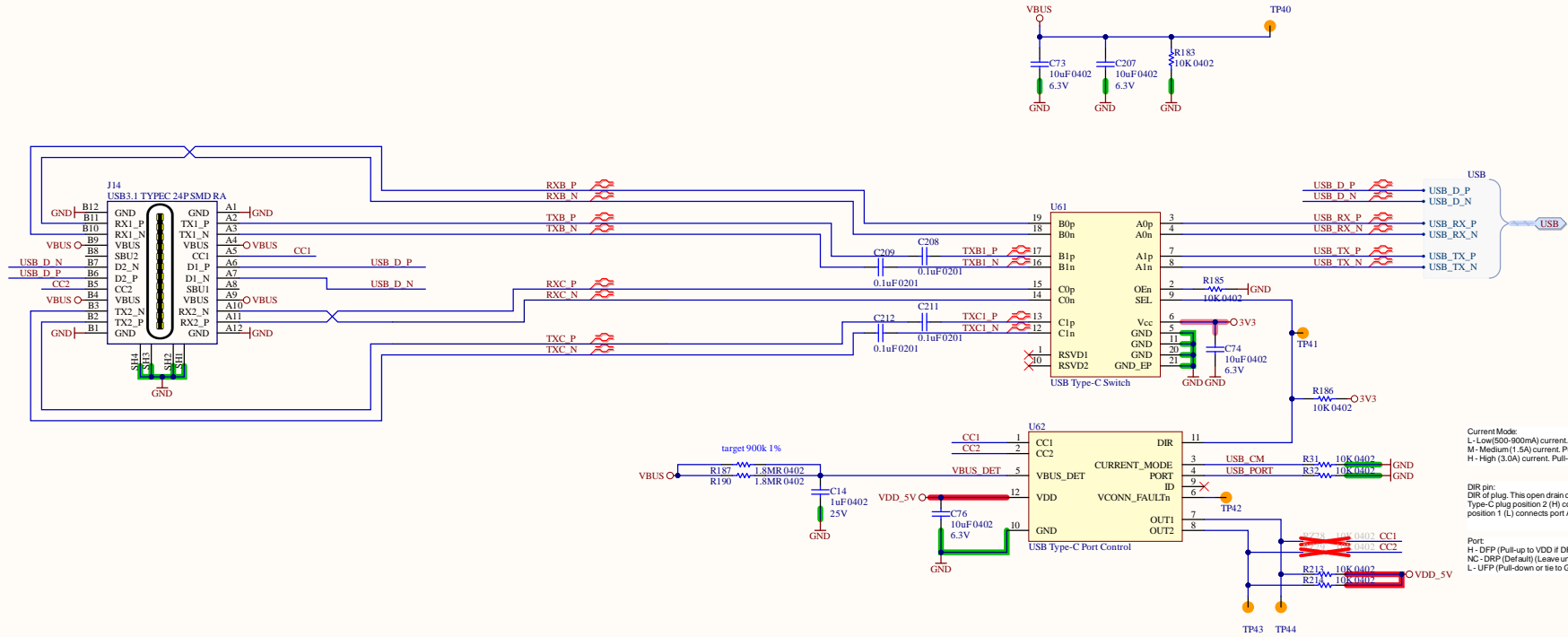
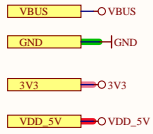
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Size: Tabloid	Number:D2098000	Revision:R4M1E3		
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RGB CAMERA



Title BW2098POE			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80244 United States	Cannot open file C:\Users\Brian.Luxonis\...
Size: Tabloid	Number: D2098000	Revision: R4M1E3		
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Drawn by: Brian Weinstein				

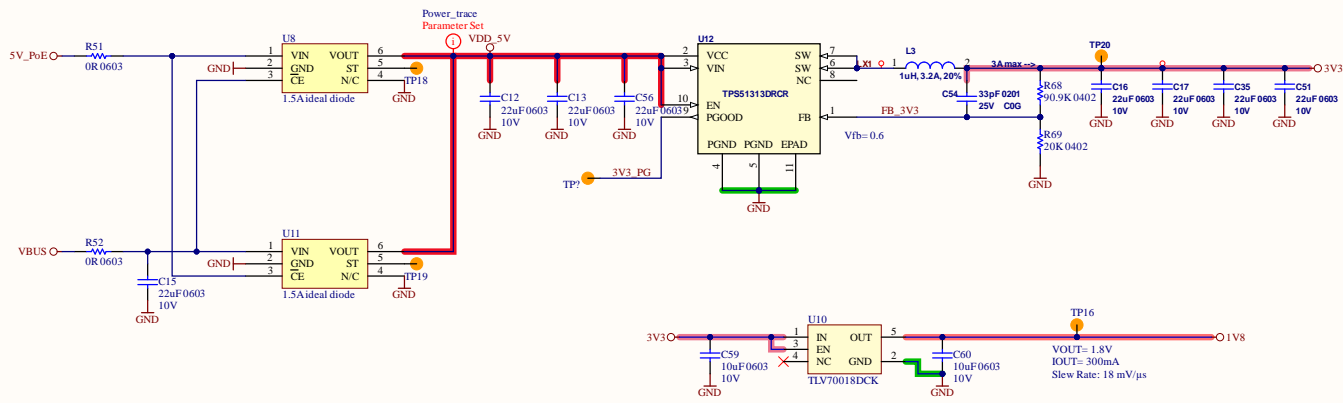
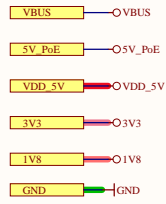


Current Mode:
 L- Low(500-900mA) current. (Default) Pull-down to GND or leave unconnected.
 M- Medium (1.5A) current. Pull-up to VDD with 500-kΩ resistor.
 H- High (3.0A) current. Pull-up to VDD with 10-kΩ resistor.

DIR pin:
 DIR of plug. This open drain output indicates the detected plug orientation:
 Type-C plug position 2 (H) connects Port A to Port C on U61. Type-C plug
 position 1 (L) connects port A to Port B on U61.

Port:
 H- DFP (Pull-up to VDD if DFP mode is desired)
 NC- DRP (Default) Leave unconnected if DRP mode is desired)
 L- UFP (Pull-down or tie to GND if UFP mode is desired)

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Size: Tabloid	Number: D2098000	Revision: R4M1E3		
Date: 22/05/2024	Time: 18:23:36	Sheet 11 of 12		
Drawn by: Brian Weinstein				



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Size: Tabloid	Number: D2098000	Revision: R4M1E3			
Date: 22/05/2024	Time: 18:23:36	Sheet: 12 of 12			
Drawn by: <i>Brian Weinstein</i>					