PAG7646J1: QVGA Global Shutter Image Sensor Module

General Description

The PAG7646J1 is an FPC (Flexible Printed Circuit) sensor module comprised of a monochrome QVGA global shutter image sensor and lens set. It is designed to fulfill the increasing gesture control demand for computer vision or fast-moving object applications.

PAG7646J1 has 180 frame-per-second (fps) image capture capability at full 320x240 resolution and outputs data through a 4-bit parallel interface. The sensor has built-in Auto Exposure and Auto Gain Control function.

With programmable WOI, frame rate, and flip function, it provides flexibility in various applications. The LED control signal output can control the timing of the external LED to sync with the exposure time, which is essential for the NIR applications.

Key Features

- Frame rate up to 180fps (@320x240)
- Lens FOV: 78.3° (Horizontal) ; 62.9°(Vertical)
- Ultra-low power consumption
- Enhanced sensor Quantum Efficiency (QE) in Near IR region
- Hardware Auto Exposure and Gain Control
- Lens shading correction (LSC)
- 4-bit Parallel interface
- Data format: Full 8-bit RAW
- I^2C with speed up to 1 MHz (Fast Mode Plus)
- Supports I^2C multi-slave ID by I/O strapping
- Programmable WOI (Window of Interest)

Applications

- Gesture recognition
- Surveillance system

Key Parameters

Parameter	Value
Array Size	320 x 240
Pixel Size	3.0 x 3.0 μm^2
Shutter Type	Electronic global shutter
Max. Frame Rate	180 fps
FOV (Horizontal)	78°
Signal to Noise Ratio (SNR)	36 dB
Dynamic Range	59 dB
Sensitivity	6500 mV/[($\mu W/cm^2$)x Sec.] @ 940nm
Supply Voltage	VDDMA: 3.3V VDDIO: 1.8V / 3.3V
Power Consumption	50.9 mW @ 180 fps (typ.) 5.45 mW @ 15 fps (typ.) 0.69 mW @ 1 fps (typ.)
Operating Temperature	-20 to +70 °C
Stable image	0 to +50 °C
Package Type	Chip Scale Package (CSP)
Package Dimension (L x W x H)	3090 x 2650 x 760 μm^3

Ordering Information

Part Number	Description	Module Type	Contact Type	MOQ
PAG7646J1	QVGA Global Shutter Image Sensor Module	FPC	19-pin Golden Finger	650 units

RoHS compliant

For any additional inquiries, please contact us at https://www.pixart.com

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1.0 Introduction

1.1 Overview

The PAG7646J1 is an FPC (Flexible Printed Circuit) sensor module comprised of a monochrome QVGA global shutter image sensor and lens set. The sensor has 180 frame-per-second (fps) image capture capability at full 320x240 resolution and outputs data through a 4-bit parallel interface.

PAG7646J1 has built-in auto Exposure and the auto Gain-Control function that can auto-calibrate based on the environment brightness. The module has the flexibility to configure WOI (the scheme is predefined WOI Region) for partial array sensing and the pixel-average scheme for the power saving purpose.

Note: Throughout this document, the PAG7646LT is referred to as the “module”.

Figure 1. FPC Module Appearance

1.2 Terminology

Term	Description
ISP	Image Signal Processor
I^2C	Inter-Integrated Circuit
Min.	Minimum
Typ.	Typical
Max.	Maximum
CIS	CMOS Image Sensor
WOI	Window of Interest

1.3 FPC Golden Finger Pin Assignment and Signal Description

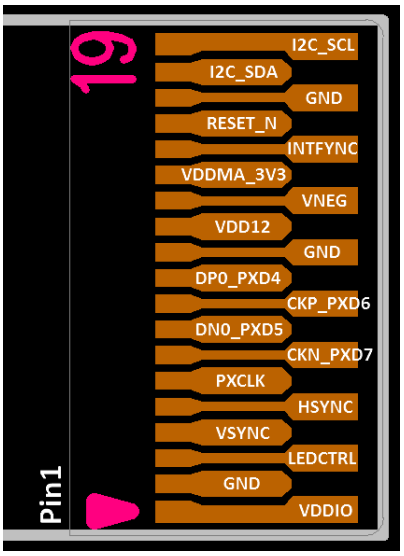

Figure 2. FPC Pin Assignment (Bottom View)

Table 1. Signal Description

Function	Pin No.	Signal Name	Type	Description
Power Supplies	12	VDD12	Power	Internal regulator +1.2V terminal pad. Strictly for Voltage Stabilizing Capacitor Connection.
	14	VDDMA_3V3	Power	Main power supply of +3.3V.
	1	VDDIO	Power	I/O power supply
	2,11,17	GND	Ground	Reference Ground
	13	VNEG	Power	Built-in negative Voltage Charge Pump.
Functional I/O	16	RESET_N	Input	Reset pin (Active low)
	3	LEDCTRL	I/O	External LED timing control pin. The timing is synchronized to exposure signal
	15	INTFYNC	I/O	Multi-sensor sync signal output pin.
I^2C Interface	19	I2C_SCL	Input	I^2C communication clock
	18	I2C_SDA	I/O	I^2C communication data
Parallel Data Interface	10	DP0_PXD4	Output	Parallel Data (bit [4]) Output
	8	DN0_PXD5	Output	Parallel Data (bit [5]) Output
	9	CKP_PXD6	Output	Parallel Data (bit [6]) Output
	7	CKN_PXD7	Output	Parallel Data (bit [7]) Output
	5	HSYNC	Output	Line signal of parallel interface
	4	VSYNC	Output	Frame signal of parallel interface
	6	PXCLK	Output	Pixel clock of parallel interface

2.0 Operation Specification

2.1 Absolute Maximum Rating

Table 2. Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-30	70	°C	
Main Voltage Supply	VDDMA	-0.3	3.6	V	
I/O Voltage Supply	VDDIO	-0.3	3.6	V	VDDIO=3.3V
		-0.3	2.1	V	VDDIO=1.8V
I/O Pin Voltage	V_{IO}	-0.3	VDDIO + 0.3	V	
I/O Pin Current	I_{IO}	-	16	mA	
Relative Humidity	RH	0	85	%	Non-condensing, Non-biased

Notes:

1. At ambient temperature = 25°C.
2. If the module operated beyond the maximum rating values, it may cause device damage.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.

2.2 Recommended Operating Condition

Table 3. Recommended Operating Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Ambient Temperature	T_A	-20	25	50	°C	
Main Voltage Supply	VDDMA	3.14	3.3	3.47	V	Include ripples
Core Voltage Supply	VDD12	1.14	1.2	1.26	V	Include ripples
I/O Voltage Supply	VDDIO	3.14	3.3	3.47	V	Include ripples For 3.3V I/O interface
		1.71	1.8	1.89	V	Include ripples For 1.8V I/O interface
Digital I/O Driving Ability	I_{DDIODR}	4	-	16	mA	At VDDIO = 3.3V
		3	-	12	mA	At VDDIO = 1.8V
System clock frequency	f_{sysclk}	50	56.5	63	MHz	Square wave Duty cycle = 45% to 55%

Note: PixArt does not guarantee the performance if the operating temperature is beyond the specified limit.

2.3 DC Electrical Characteristic

Table 4. DC Electrical Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
DC Supply Current	I_{DD33_QVGA}	-	11	16	mA	At QVGA image size, exposure time = 5.5ms, 180fps
Suspend Current	I_{DD33_SUS}	-	-	100	µA	Suspend current of VDDMA
	I_{DD18_SUS}	-	-	10		Suspend current of VDDIO
I/O Input High Voltage	V_{IH}	0.8 x VDDIO	-	VDDIO + 0.3	V	
I/O Input Low Voltage	V_{IL}	-0.3	-	0.2 x VDDIO	V	
I/O Output High Voltage	V_{OH}	0.8 x VDDIO	-	VDDIO	V	
I/O Output Low Voltage	V_{OL}	0	-	0.2 x VDDIO	V	

Notes: All the parameters are tested under operating conditions: VDDMA = 3.3V, VDDIO = 1.8V, T_A = 25°C

2.4 AC Electrical Characteristic

Table 5. AC Electrical Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
System Clock Rise Time	t_R	-	-	1	ns	@ C_{load} = 0.5pF & Voltage Level = 10% to 90% & f_{pxclk} = 56.5MHz.
System Clock Fall Time	t_F	-	-	1	ns	@ C_{load} = 0.5pF & Voltage Level = 90% to 10% & f_{pxclk} = 56.5MHz.
VDDMA Rise Time	t_{R_MA}	-	-	5	ms	0 to minimum VDDMA
VDDIO Rise Time	t_{R_IO}	-	-	5	ms	0 to minimum VDDIO

Note: All the parameters are tested under operating conditions: VDDMA = 3.3V, VDDIO = 1.8V, T_A = 25°C

2.5 Chip Array Specification

Table 6. Array Specification

Parameter	Symbol	Value	Unit	Note
Horizontal Image Array Count	-	320	pixel	
Vertical Image Array Count	-	240	pixel	
Pixel Size	-	3 x 3	μm^2	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Signal to Noise Ratio	-	36			dB	
Dynamic Range	-	59			dB	
Sensitivity	-	6500			mV/[(µW/cm^2)x Sec.]	@940nm

3.0 Mechanical Specification

3.1 Package Mechanical Dimension

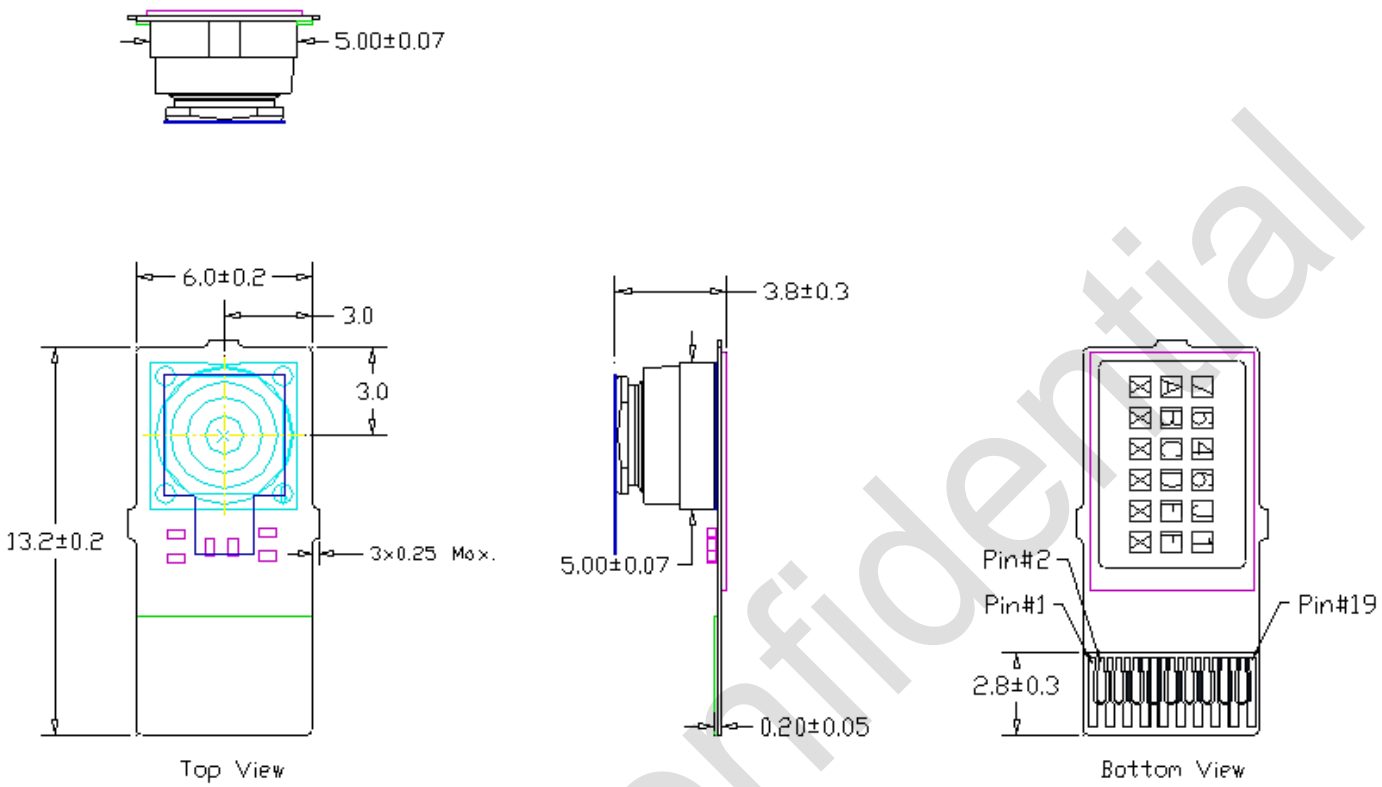

Figure 3. Package Outline Diagram (Unit in mm)

3.2 Golden Finger Design

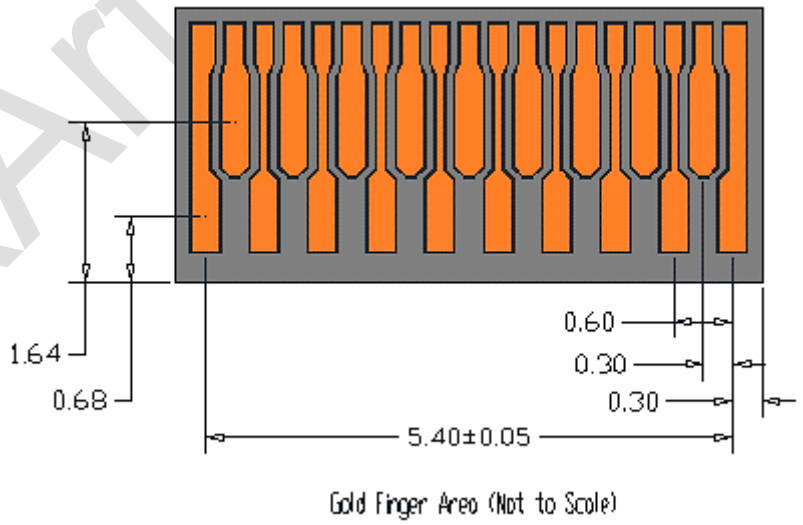

Figure 4. Golden Finger Design (Bottom View; Unit in mm)

4.0 Design Reference

4.1 Module Schematic

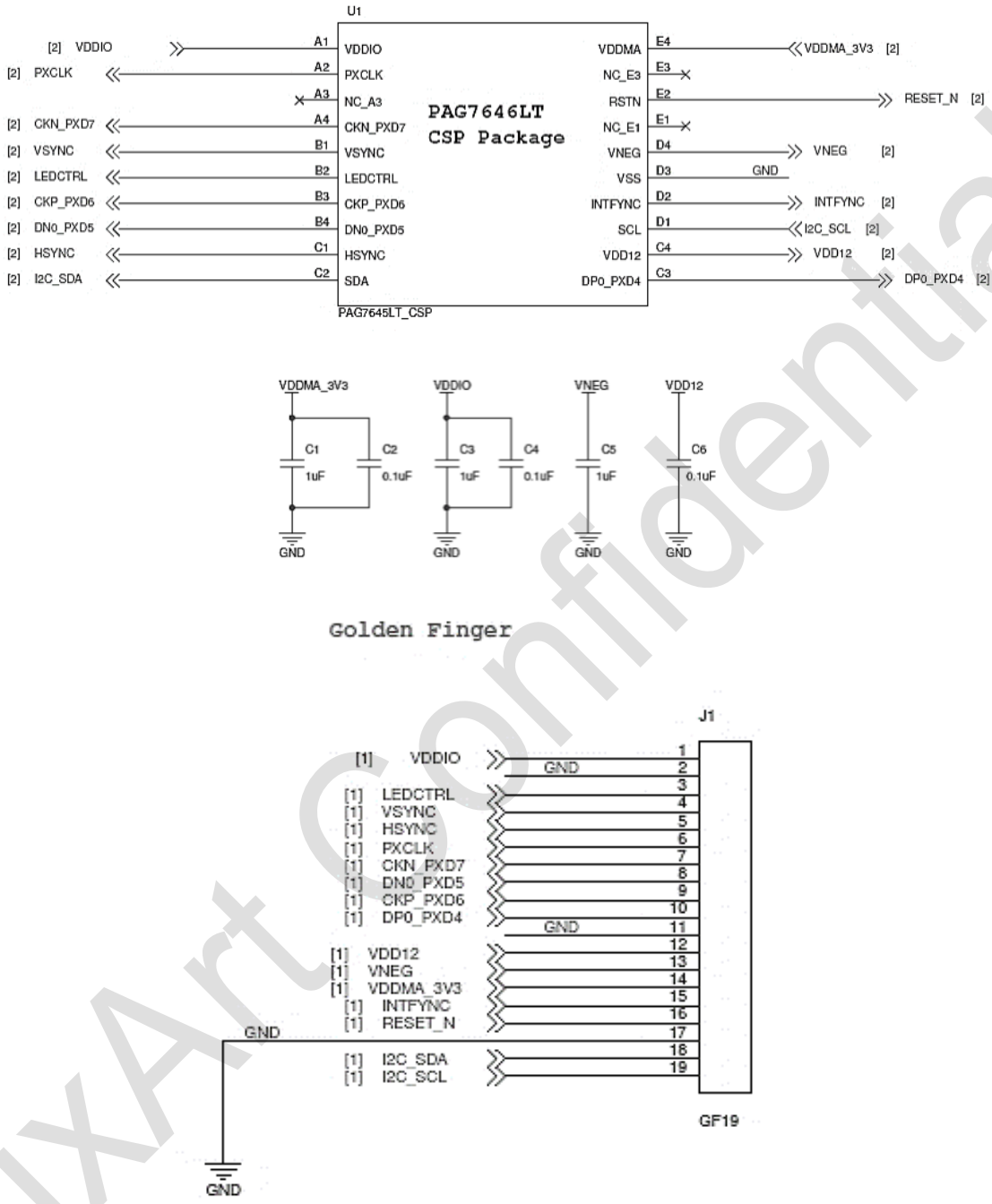

Figure 5. Reference Design Schematic

4.2 Assembly Guide

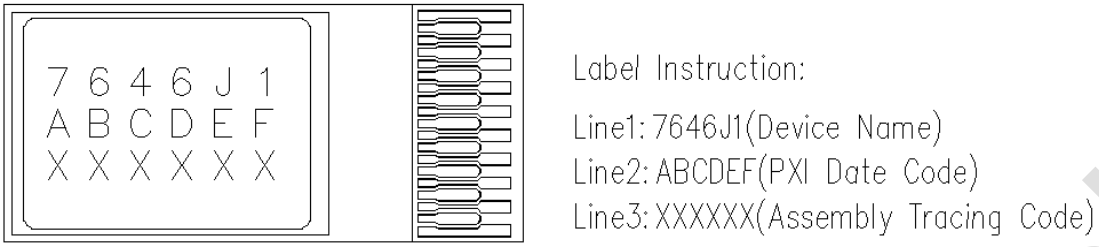

Figure 6. Module Label Marking Instruction (Bottom View)

4.2.1 Packing Information

- Module orientation is toward the chamfer of chip tray

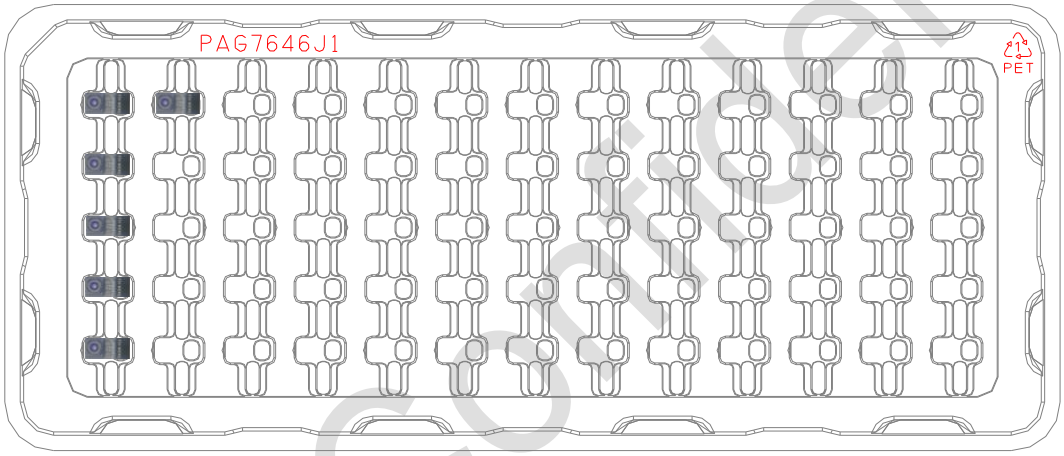

Figure 7. Module Orientation

- Stack 10 trays(1 tray+10 trays+1 tray) with two cover trays in a bunch

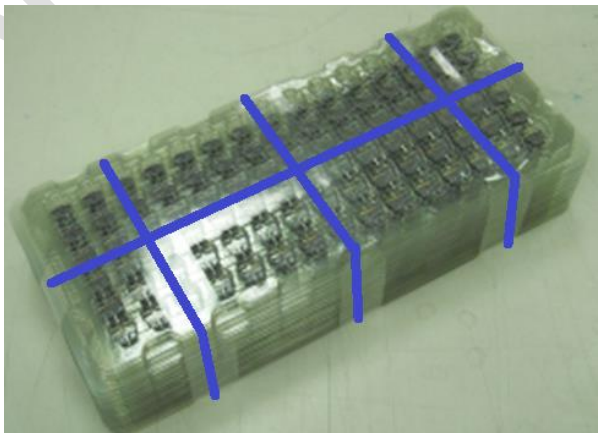

Figure 8. One Bunch

- Pack one bunch of trays into one moisture proof bag.

Figure 9. Bunch & Moisture Proof Bag

- Pack one bag into an inner packing box Pack.

Figure 10. Bag & Inner Packing Box

- Pack six inner packing box into one outer packing box
- The maximum capacity of one outer packing box using PET tray of PAG7646J1

Description	Value
One outer packing box	3900 units
Remark	(65ea per tray) x (10 tray per inner box) x (6 inner box per outer box)

5.0 Power Management

5.1 Power Sequence

- Power-on sequence with external RSTN control
  - VDDIO and VDDMA power on at same time or follow the sequence as shown in Figure 11.
  - RSTN must always asserted when the Power on in progress. After VDDMA power on and stabilized, wait for at least 1 ms before RSTN de-assert.
  - Wait for at least 5ms after RSTN release prior writing the initial command.

- Power-off sequence with external RSTN control
  - VDDMA, VDDIO power off and RSTN asserted at same time or follow the sequence as shown in Figure 11.
  - Power off interval time before next power on must be at least 1ms.

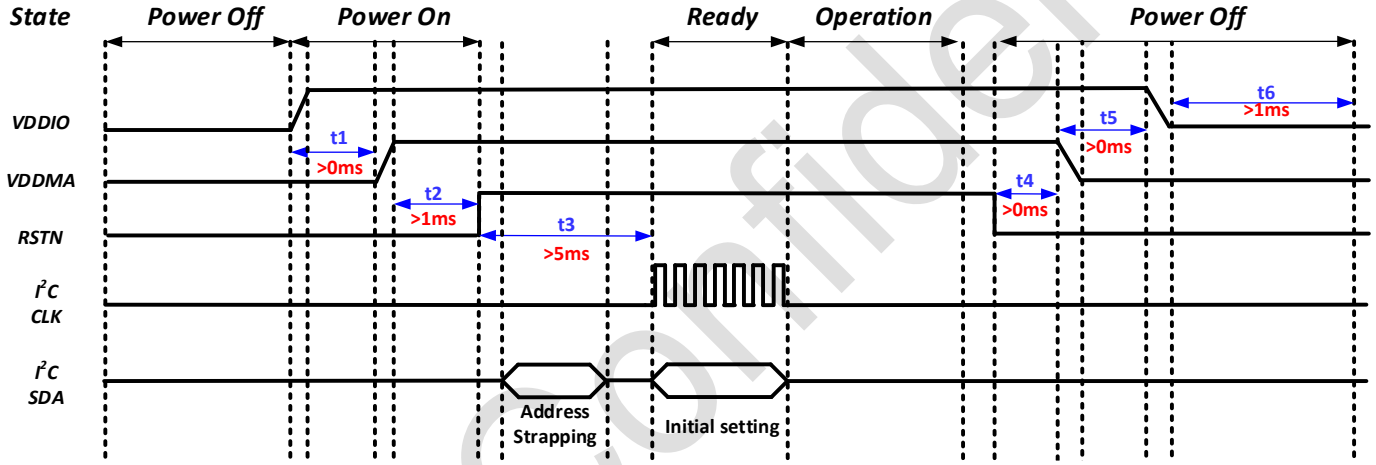

Figure 11. Power On/off Timing Diagram with External Reset Control

- Power-on sequence without RSTN control (RSTN connects a pull-up resistor to VDDIO).
  - VDDIO and VDDMA power on at same time or follow the sequence as shown in Figure 12.
  - Wait for at least 6ms after power ready prior writing the initial command.

- Power-Off Sequence without RSTN control
  - VDDMA and VDDIO power off at same time or follow the sequence as shown in Figure 12.
  - Power off interval time before next power on must be at least 1ms.

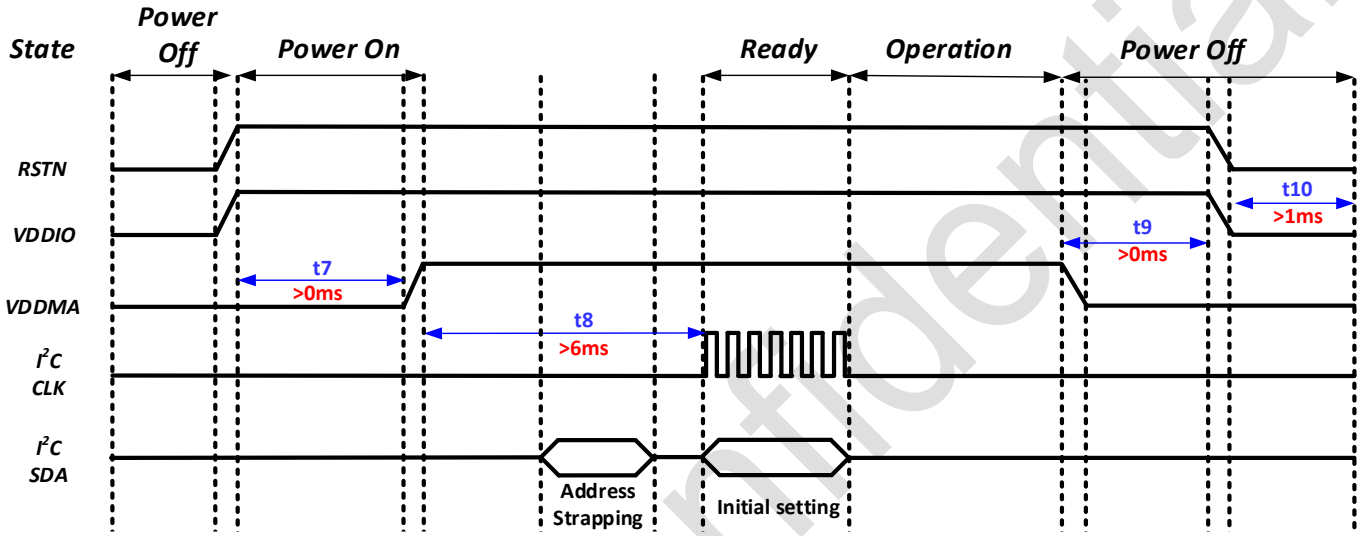

Figure 12. Power On/off Timing Diagram without Reset Control

Table 7. Power On/Off Sequence Timing Constraint

Constraint	Label	Min.	Max.	Unit
VDDIO rising – VDDMA rising	t1	0	-	ms
VDDMA rising – RSTN rising	t2	1	-	ms
RSTN rising – I²C command	t3	5	-	ms
RSTN falling – VDDMA falling	t4	0	-	ms
VDDMA falling – VDDIO falling	t5	0	-	ms
Power off interval time before next power on	t6	1	-	ms
VDDIO steady to VDDMA rising	t7	0	-	ms
Power ready to I²C command	t8	6	-	ms
VDDMA falling to VDDIO falling	t9	0	-	ms
Power off interval time before next power on	t10	1	-	ms

5.2 Power State

5.2.1 State Description

Table 8. State Description

State	Description
OFF	No power supply, all the voltage rails and clocks are gated.
Suspend	The module hardware complete the power on process. The module enters this state when I^2C interface is ready for the host communication upon initialization complete. The module is available to receive command from the host. The module enters this state as needed for power saving purpose while all the parameter setting still intact.
Operation	The module enters continuous state upon receive the host's command. This is the state where the module executes and deliver the required data according to host command. The module requires to initialize when first entry to this state.
Trigger	The module enters this state upon receiving command for single frame capturing and output image data.

5.2.2 State Diagram

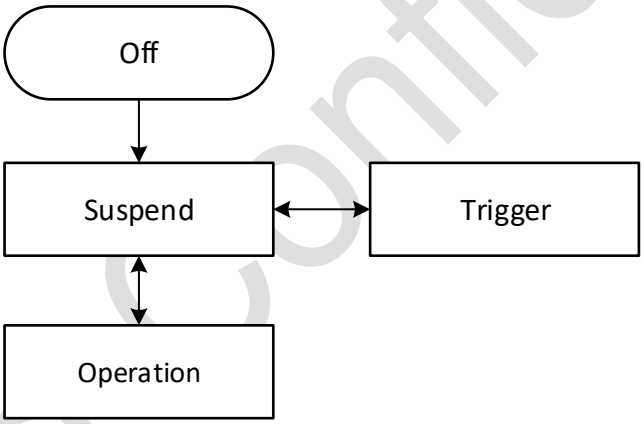

Figure 13. Power State Diagram

5.3 Reset

The module needs to re-initialize due to all previous registers will be cleared after each reset.

5.3.1 Power on Reset

During power-on, the module does not need an external reset as there is an internal circuitry that performs power-on reset function for the module.

5.3.2 Pin Reset

The module can be reset by pulling RSTN pin. When RSTN pin is pulled low, the module will be reset.

5.3.3 Reset Timing Specification

Table 9. RSTN Timing Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Reset hold time	-	100	-	-	µs	-
Wake up time - Reset pin release to Ready State	-	6	-	-	ms	Refer to section 5.1
Power up reset VDDMA voltage	-	-	1.5	-	V	-
Pin Reset Voltage	-	0.2 x VDDIO	-	-	V	-

Note: At ambient temperature = 25°C.

Revision History

Revision Number	Date	Description
0.8	30 Jan 2023	Initial release