IT8951E
IT8951TE
IT8951VG
IT8951E-64
IT8951VG-64

EPD Timing Controller

Preliminary Specification V0.2.4.3

(For D Version)

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Please note that the IT8951 V0.2.4.3 is applicable to the D version.

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Revision History

The contents below indicate the change between this version and the previous version only. The revision history shown in the previous version will not remain in the following table.

Section	Revision	Page No.
-	● Part IT8951VG in VFBGA 128 added ● eMMC support added ● Tables below in Pin Description section modified → Pin Description of Supplies Signals → Difference between IT8951E/IT8951TE/ IT8951E-64/IT8951VG/IT8951VG-64	-

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1. Features

- **Built-in SDRAM**
  - Built-in 32Mb mobile SDRAM (IT8951E/ IT8951TE/IT8951VG)
  - Built-in 64Mb mobile SDRAM (IT8951E-64/IT8951VG-64)

- **Source / Gate Driver Interface**
  - Supports up to 2048x2048 resolution
  - Supports 16/32-level grayscale mode
  - Supports 8/16-bit source driver data bus
  - Supports 2/4-bit coding of source driver
  - Supports various types of source and gate drivers
  - Supports panel border
  - Supports AC/DC EPD panel
  - Supports variable frame rate

- **Image Processing Engine**
  - Supports Dither4, Dither5 output function.
  - Supports 0/90/180/270-degree rotation, mirror, flip

- **Display Engine**
  - Supports partial-region display
  - Supports 8 programmable LUTs for different applications
  - Each LUT has programmable frame count which can be up to 256 frames.
  - Built-in serial flash controller for waveform read
  - Supports Alpha Blending effect
  - Supports Fill Rectangle function

- **Several Host Interface**
  - Intel 80 compatible asynchronous interface (16 bits)
  - Motorola 68 compatible asynchronous interface (16 bits)
  - SPI slave interface
  - I2C slave interface
  - All registers accessible by host interface
  - All memory contents accessible by host interface
  - Supports 0/90/180/270-degree rotation when loading image
  - Supports ARGB8888/ RGB888/RGB565 image input

- **16C750 Compatible UART**
  - 1 channel UART

- **I2C Interface**
  - Supports Multi-Master I2C/SMBus
  - 100Kbit/s Standard mode or 400Kbit/s Fast mode
  - SMBus compatible

- **USB 2.0 Device**
  - 1-port USB 2.0 Device
  - Compatible with USB Specification version 2.0

- **SD/MMC Host Interface (IT8951VG/IT8951VG-64)**
  - SD standard host spec(ver2.0) compatible
  - Dedicated DMA access support
  - Compatible with SD memory card protocol
  - version 2.1
  - Compatible with HS-MMC/eMMC protocol version 4.2
  - Compatible with SDIO card protocol version 1.0

- **Built-in Thermal Sensor**
  - Built-in temperature sensor supporting external thermal diode 3904/3906
  - Supports external temperature sensor with I2C interface

- **Power Saving Mode**
  - Active mode
  - Standby mode
  - Sleep mode

- **System**
  - Built-in programmable PLL
  - 1 interrupt output pin to host to indicate any exception from display engine
  - 1 interrupt input pin from power IC to indicate any abnormal status
  - Core voltage 1.8V
  - I/O voltage 3.3V
  - Package LQFP 128-pin (IT8951E/IT8951E-64)
  - Package TQFP 128-pin (IT8951TE)
  - Package VFBGA 128-pin (IT8951VG/IT8951VG-64)

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2. General Description

The IT8951 is a high performance and low cost timing controller supporting both AC and DC VCOM EPDs. It provides functions including boot up auto display, alpha blending and picture-in-picture to reduce the overhead of CPU. In addition, it also supports the flexible resolution of EPD up to 2048 x2048 and with 32Mb/64Mb mobile SDRAM inside.

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2.1 Register Map

Figure 2-1 shows the hardware peripheral register address map. All of the hardware I/O are located between 0x08000000 to 0x0800FFFF.

Figure 2-1. Peripheral Regiter Mapping

	Offset	
Reserved		
USB	0x4E00	*double word
I2C	0x4C00	double word
Reserved		
Reserved		
Image Process	0x4600	double word
Reserved		
Reserved		
JPG	0x4000	double word
Reserved		
Reserved		
Reserved		
Reserved		
GPIO	0x1E00	double word
HS UART	0x1C00	Byte
Reserved		
Reserved		
Reserved		
INTC	0x1400	double word
Reserved		
Display Control	0x1000	double word
SPI	0x0E00	double word
Reserved		
Reserved		
Thermal Sensor	0x0800	double word
SD Card	0x0600	double word
Reserved		
Memory Converter	0x0200	double word
System	0x0000	double word

Note: The USB controller can be accessed by the internal CPU only.

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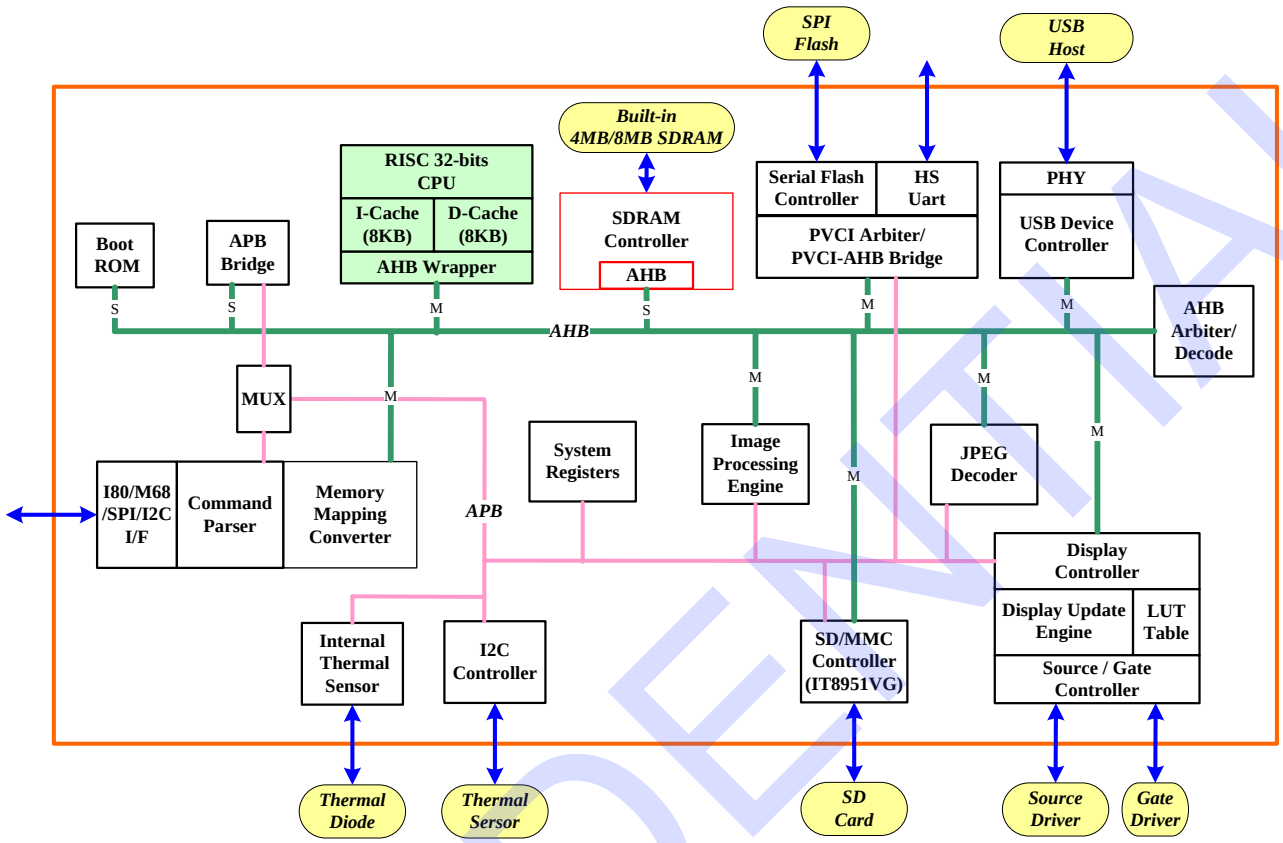
3. Block Diagram



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4. Pin Configuration

Figure 4-1. Pin Configuration of IT8951E/IT8951E-64 (LQFP-128)

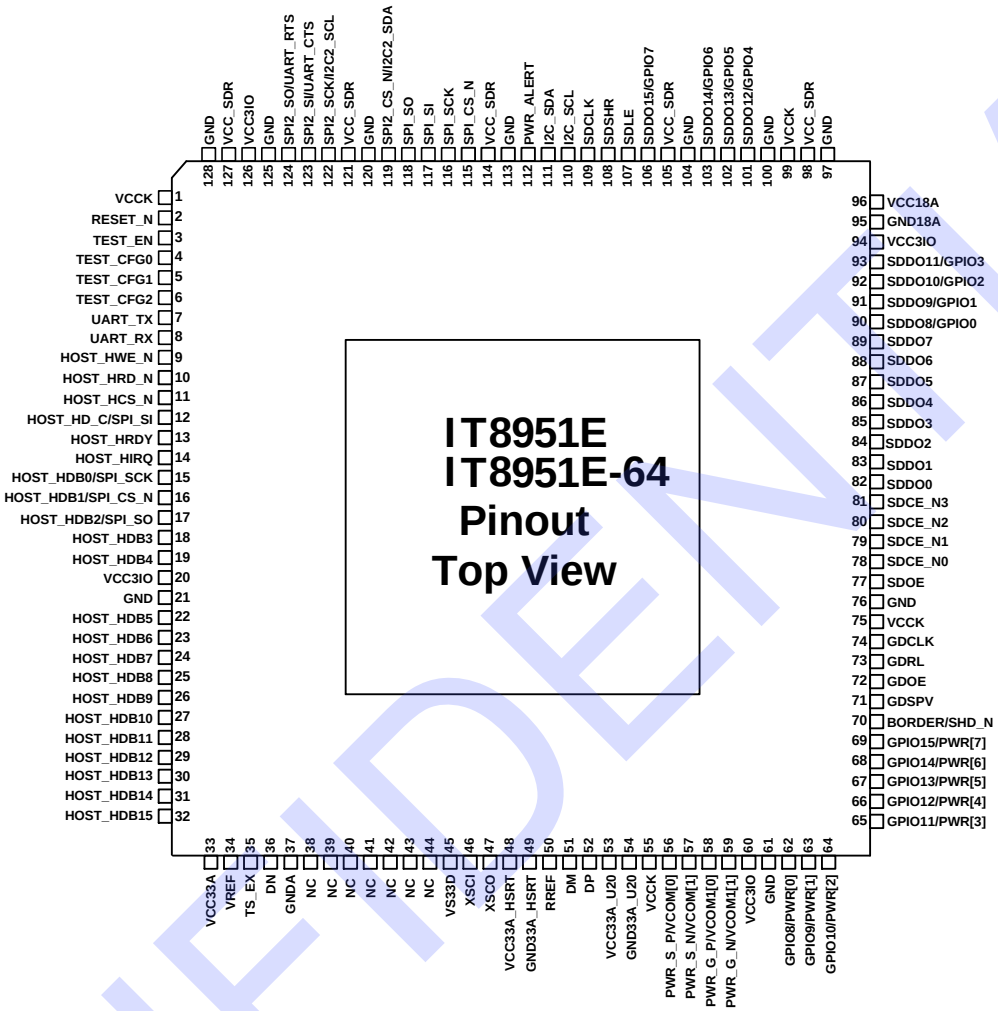

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Figure 4-2. Pin Configuration of IT8951TE (TQFP-128)

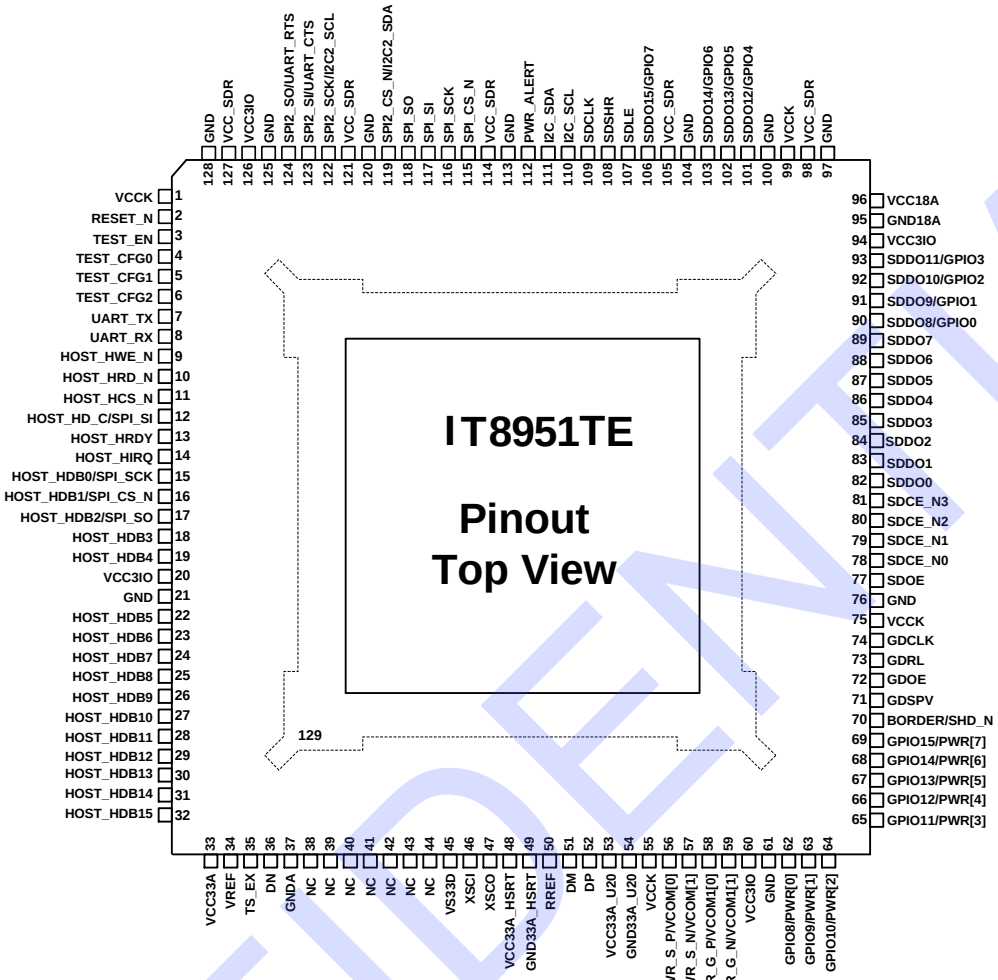

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Figure 4-3. Pin Configuration of IT8951VG/IT8951VG-64 (VFBGA-128)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	SPI_SI	SPI_SCK	SD_DATA1	SD_DATA3	I2C_SDA	SPI_CS_N	PWR_ALERT	SDDO15/GPIO7	SDLE	SDDO14/GPIO6	SDDO13/GPIO5	SDDO5	SDDO9/GPIO1	SDDO8/GPIO0	SDDO11/GPIO3	VCC18A	A
B	SPI2_CS_N/I2C2_SDA	SPI_SO	SD_DATA2	SD_CD_N	VCC_SDR	SDCLK	SDSHR	I2C_SCL	SDDO12/GPIO4	SDDO7	SDDO4	SDDO3	SDDO6	SDDO1	SDCE_N3	SDDO10/GPIO2	B
C	SD_WP	SD_CLK		GND	VCC3IO							SDDO2	GND		SDCE_N2	GND18A	C
D	SD_CMD	SD_DATA0	VCCK											SDDO0	SDCE_N1	SDCE_N0	D
E	GND	GND	VCC_SDR											VCCK	SDOE	VCC_SDR	E
F	SPI2_SI/UART_CTS	SD_PWR_N													GND	VCC_SDR	F
G	SPI2_SCK/I2C2_SCL	SPI2_SO/UART_RTS													VCC_SDR	XSCI	G
H	TEST_CFG1	RESET_N													XSCO	VCC33A_HSRT	H
J	TEST_CFG2	TEST_EN													NC	GND33A_HSRT	J
K	HOST_HDB2/SPI_SO	TEST_CFG0													VCC33A_U20	GND33A_U20	K
L	HOST_HDB4	HOST_HDB1/SPI_CS													PWR_S_P/VCOM[0]	PWR_G_P/VCOM1[0]	L
M	HOST_HDB5	HOST_HDB3	UART_TX											VCCK	GDOE	GDCLK	M
N	HOST_HDB7	HOST_HDB6	VCC3IO											GDSPV	BORDER/SHD_N	GDRL	N
P	HOST_HDB8	HOST_HDB9		HOST_HD_C/SPI_SI	HOST_HDB0/SPI_SCK							GPIO15/PWR[7]	VCC3IO		GPIO13/PWR[5]	GPIO12/PWR[4]	P
R	HOST_HDB10	HOST_HDB12	UART_RX	HOST_HRDY	HOST_HDB14	HOST_HRD_N	HOST_HWE_N	VCCK	TS_EX	GND	DM	DP	PWR_S_N/VCOM[1]	GPIO14/PWR[6]	GPIO8/PWR[0]	GPIO11/PWR[3]	R
T	GND	HOST_HDB11	HOST_HDB13	HOST_HIRQ	HOST_HCS_N	HOST_HDB15	VCC33A	VREF	VSSA	DN	RREF	GND	PWR_G_N/VCOM1[1]	GND	GPIO9/PWR[1]	GPIO10/PWR[2]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

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Table 4-1. Pins Listed in Numeric Order(IT8951E/IT8951E-64/IT8951TE)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCCK	33	VCC33A	65	GPIO11/PWR[3]	97	GND
2	RESET_N	34	VREF	66	GPIO12/PWR[4]	98	VCC_SDR
3	TEST_EN	35	TS_EX	67	GPIO13/PWR[5]	99	VCCK
4	TEST_CFG0	36	DN	68	GPIO14/PWR[6]	100	GND
5	TEST_CFG1	37	GNDA	69	GPIO15/PWR[7]	101	SDDO12/GPIO4
6	TEST_CFG2	38	NC	70	BORDER/SHD_N	102	SDDO13/GPIO5
7	UART_TX	39	NC	71	GDSPV	103	SDDO14/GPIO6
8	UART_RX	40	NC	72	GDOE	104	GND
9	HOST_HWE_N	41	NC	73	GDRL	105	VCC_SDR
10	HOST_HRD_N	42	NC	74	GDCLK	106	SDDO15/GPIO7
11	HOST_HCS_N	43	NC	75	VCCK	107	SDLE
12	HOST_HD_C/ SPI_SI	44	NC	76	GND	108	SDSHR
13	HOST_HRDY	45	VS33D	77	SDOE	109	SDCLK
14	HOST_HIRQ	46	XSCI	78	SDCE_N0	110	I2C_SCL
15	HOST_HDB0/ SPI_SCK	47	XSCO	79	SDCE_N1	111	I2C_SDA
16	HOST_HDB1/ SPI_CS_N	48	VCC33A_HRST	80	SDCE_N2	112	PWR_ALERT
17	HOST_HDB2/ SPI_SO	49	GND33A_HSRT	81	SDCE_N3	113	GND
18	HOST_HDB3	50	RREF	82	SDDO0	114	VCC_SDR
19	HOST_HDB4	51	DM	83	SDDO1	115	SPI_CS_N
20	VCC3IO	52	DP	84	SDDO2	116	SPI_SCK
21	GND	53	VCC33A_U20	85	SDDO3	117	SPI_SI
22	HOST_HDB5	54	GND33A_U20	86	SDDO4	118	SPI_SO
23	HOST_HDB6	55	VCCK	87	SDDO5	119	SPI2_CS_N / I2C2_SDA
24	HOST_HDB7	56	PWR_S_P/ VCOM[0]	88	SDDO6	120	GND
25	HOST_HDB8	57	PWR_S_N/ VCOM[1]	89	SDDO7	121	VCC_SDR
26	HOST_HDB9	58	PWR_G_P/ VCOM1[0]	90	SDDO8/GPIO0	122	SPI2_SCK / I2C2_SCL
27	HOST_HDB10	59	PWR_G_N/ VCOM1[1]	91	SDDO9/GPIO1	123	SPI2_SI / UART_CTS
28	HOST_HDB11	60	VCC3IO	92	SDDO10/GPIO2	124	SPI2_SO / UART_RTS
29	HOST_HDB12	61	GND	93	SDDO11/GPIO3	125	GND
30	HOST_HDB13	62	GPIO8/PWR[0]	94	VCC3IO	126	VCC3IO
31	HOST_HDB14	63	GPIO9/PWR[1]	95	GND18A	127	VCC_SDR

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Table 4-2. Pins Listed in Numeric Order (IT8951VG/IT8951VG-64)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	SPI_SI	C1	SD_WP	J1	TEST_CFG2	R1	HOST_HDB10
A2	SPI_SCK	C2	SD_CLK	J2	TEST_EN	R2	HOST_HDB12
A3	SD_DATA1	C4	GND	J15	NC	R3	UART_RX
A4	SD_DATA3	C5	VCC3IO	J16	GND33A_HSRT	R4	HOST_HRDY
A5	I2C_SDA	C12	SDDO2	K1	HOST_HDB2/SPI_SO	R5	HOST_HDB14
A6	SPI_CS_N	C13	GND	K2	TEST_CFG0	R6	HOST_HRD_N
A7	PWR_ALERT	C15	SDCE_N2	K15	VCC33A_U20	R7	HOST_HWE_N
A8	SDDO15/GPIO7	C16	GND18A	K16	GND33A_U20	R8	VCCK
A9	SDLE	D1	SD_CMD	L1	HOST_HDB4	R9	TS_EX
A10	SDDO14/GPIO6	D2	SD_DATA0	L2	HOST_HDB1/SPI_CS	R10	GND
A11	SDDO13/GPIO5	D3	VCK	L15	PWR_S_P/VCOM[0]	R11	DM
A12	SDDO5	D14	SDDO0	L16	PWR_G_P/VCOM1[0]	R12	DP
A13	SDDO9/GPIO1	D15	SDCE_N1	M1	HOST_HDB5	R13	PWR_S_N/VCOM[1]
A14	SDDO8/GPIO0	D16	SDCE_N0	M2	HOST_HDB3	R14	GPIO14/PWR[6]
A15	SDDO11/GPIO3	E1	GND	M3	UART_TX	R15	GPIO8/PWR[0]
A16	VCC18A	E2	GND	M14	VCCK	R16	GPIO11/PWR[3]
B1	SPI2_CS_N	E3	VCC_SDR	M15	GDOE	T1	GND
B2	SPI_SO	E14	VCCK	M16	GDCLK	T2	HOST_HDB11
B3	SD_DATA2	E15	SDOE	N1	HOST_HDB7	T3	HOST_HDB13
B4	SD_CD_N	E16	VCC_SDR	N2	HOST_HDB6	T4	HOST_HIRQ
B5	VCC_SDR	F1	SPI2_SI/UART_CTS	N3	VCC3IO	T5	HOST_HCS_N
B6	SDCLK	F2	SD_PWR_N	N14	GDSPV	T6	HOST_HDB15
B7	SDSHR	F15	GND	N15	BORDER/SHD_N	T7	VCC33A
B8	I2C_SCL	F16	VCC_SDR	N16	GDRL	T8	VREF
B9	SDDO12/GPIO4	G1	SPI2_SCK	P1	HOST_HDB8	T9	GNDA
B10	SDDO7	G2	SPI2_SO/UART_RTS	P2	HOST_HDB9	T10	DN
B11	SDDO4	G15	VCC_SDR	P4	HOST_HD_C/SPI_SI	T11	RREF
B12	SDDO3	G16	XSCI	P5	HOST_HDB0/SPI_SCK	T12	GND
B13	SDDO6	H1	TEST_CFG1	P12	GPIO15/PWR[7]	T13	PWR_G_N/VCOM1[1]
B14	SDDO1	H2	RESET_N	P13	VCC3IO	T14	GND
B15	SDCE_N3	H15	XSCO	P15	GPIO13/PWR[5]	T15	GPIO9/PWR[1]
B16	SDDO10/GPIO2	H16	VCC33A_HSRT	P16	GPIO12/PWR[4]	T16	GPIO10/PWR[2]

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5. Pin Description

Table 5-1. Pin Description of Supplies Signals

IT8951E/TE/ E-64 Pin(s) No.	IT8951VG/ VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
20, 60, 94, 126	C5,N3,P13	VCC3IO	PWR	-	***I/O Power Supply***
1, 55, 75, 99,	E14,M14,R8	VCCK	PWR	-	***1.8V Digital Core Power***
21, 61, 76, 97, 100, 104, 113, 120, 125, 128	C4,C13,E1, E2,F15,R10,T1,T12,T14	GND	GND	-	***Digital Ground***
33	T7	VCC33A	PWR	-	***3.3V Analog Power***
37	T9	GNDA	GND	-	***Analog Ground***
53	K15	VCC33A_U20	PWR	-	***3.3V Power Supply for OTG PHY***
48	H16	VCC33A_HSRT	PWR	-	***3.3V Power Supply for OTG PHY***
54	K16	GND33A_U20	GND	-	***Ground for OTG PHY***
49	J16	GND33A_HSRT	GND	-	***Ground for OTG PHY***
95	C16	GND18A	GND	-	***Ground for PLL***
96	A16	VCC18A	PWR	-	***1.8V Power Supply for PLL***
45	-	VS33D	GND	-	***Analog Ground***
98, 105, 114, 121, 127	B5,E3,E16, F16,G15	VCC_SDR	PWR	-	***1.8V SDRAM Core/Pad Power Supply***
38, 39, 40, 41, 42, 43,44	J15	NC	-	-	***No Connect***
129	-	GND	GND	-	***Exposed Pad. Must connect to ground. (IT8951TE)***

Table 5-2. Pin Description of Host Interface Signals

IT8951E/TE/E-64 Pin(s) No.	IT8951VG/ VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
12	P4	HOST_HD_C	DI	VCC3IO	***Host I/F Command/Data Select*** This input pin is to select command (Low)/data (High).
11	T5	HOST_HCS_N	DI	VCC3IO	***Host I/F Chip Select*** This input pin is to select chip.
15, 16, 17, 18, 19, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32	T6,R5,T3, R2,T2,R1, P2,P1,N1, N2,M1,L1, M2,K1,L2, P5	HOST_HDB[15:0]	DIO16	VCC3IO	***Host I/F Data*** These input/output pins are for host i/F data.
10	R6	HOST_HRD_N	DI	VCC3IO	***Host I/F Read Enable*** This input pin is to enable host I/F read.
9	R7	HOST_HWE_N	DI	VCC3IO	***Host I/F Write Enable Pin*** This input pin is to enable host I/F write.
13	R4	HOST_HRDY	DO16	VCC3IO	***Host I/F Ready*** This output pin is for host I/F ready.
14	T4	HOST_HIRQ	DO16	VCC3IO	***Host I/F Interrupt*** This output pin is for Host I/F interrupt.
119	B1	SPI2_CS_N	DIO16	VCC3IO	***SPI Host I/F Chip Select / I2C Host I/F Data*** This input pin is to select chip in SPI Host I/F. This input/output pin is for I2C Host I/F data.
122	G1	SPI2_SCK	DIO16	VCC3IO	***SPI Host I/F Clock*** This input pin is clock input in SPI Host I/F.
123	F1	SPI2_SI	DI	VCC3IO	***SPI Host I/F Data Input*** This input pin is data input in SPI Host I/F.
124	G2	SPI2_SO	DO16	VCC3IO	***SPI Host I/F Data Output***

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IT8951E/TE/E-64 Pin(s) No.	IT8951VG/VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
					This output pin is data output in SPI Host I/F.
119	B1	I2C2_SDA	DIO16	VCC3IO	***I2C Host I/F Data*** This input/output pin is for I2C Host I/F data.
122	G1	I2C2_SCL	DIO16	VCC3IO	***I2C Host I/F Clock*** This input/output pin is for I2C Host I/F clock.

Table 5-3. Pin Description of System Control Signals

IT8951E/TE/E-64 Pin(s) No.	IT8951VG/VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
2	H2	RESET_N	DI	VCC3IO	***System Reset*** This input pin is to reset the system. (Active Low)
3	J2	TEST_EN	DI	VCC3IO	***Test Mode Enable*** This input pin is to enable the test mode. For normal use, please connect a pull-down resister to this pin.
4, 5, 6	J1, H1, K2	TEST_CFG[2:0]	DI	VCC3IO	***Test Mode Configuration*** These input pins are to configure the test mode and host I/F mode.
7	M3	UART_TX	DO16	VCC3IO	***UART TX*** This is an output UART TX pin.
8	R3	UART_RX	DI	VCC3IO	***UART RX*** This is an input pin UART RX pin.
123	F1	UART_CTS	DI	VCC3IO	***UART Flow Control CTS*** This is an input UART CTS pin.
124	G2	UART_RTS	DO16	VCC3IO	***UART Flow Control RTS*** This is an output UART RTS t pin.
46	G16	XSCI	AIO	VCC33A_HSRT	***Crystal Oscillator Input*** This is an input crystal oscillator pin. It is recommended to connect a 12Mhz crystal to this pin.
47	H15	XSCO	AIO	VCC33A_HSRT	***Crystal Oscillator Output*** This is an output crystal oscillator pin. It is recommended to connect a 12Mhz crystal to this pin.

Table 5-4. Pin Description of SPI Master for Serial Flash

IT8951E/TE/E-64 Pin(s) No.	IT8951VG/VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
115 (Reg SFMSR[3] =0) / 16 (Reg SFMSR[3] = 1)	A6	SPI_CS_N	DO16	VCC3IO	***SPI Slave Chip Select*** This output pin is to select the SPI slave chip.
116 (Reg SFMSR[3] = 0) / 15 (Reg SFMSR[3] = 1)	A2	SPI_SCK	DO16	VCC3IO	***SPI Clock*** This output pin is for SPI clock.
117 (Reg SFMSR[3] = 0) / 12 (Reg SFMSR[3] = 1)	A1	SPI_SI	DI	VCC3IO	***SPI Data Input*** This pin is for SPI data input.

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IT8951E/TE/E-64 Pin(s) No.	IT8951VG/VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
118 (Reg SFMSR[3] = 0) / 17 (Reg SFMSR[3] = 1)	B2	SPI_SO	DO16	VCC3IO	***SPI Data Output*** This pin is for SPI data output.

Table 5-5. Pin Description of I2C Master/Slave

IT8951E/TE/E-64 Pin(s) No.	IT8951VG/VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
110	B8	I2C_SCL	DO16	VCC3IO	***I2C Clock*** This output pin is for I2C clock.
111	A5	I2C_SDA	DIO16	VCC3IO	***I2C Data*** This input/output pin is for I2C data.

Table 5-6. Pin Description of Source Driver Signals

IT8951E/TE/E-64 Pin(s) No.	IT8951VG/VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
109	B6	SDCLK	DO16	VCC3IO	***Source Driver Clock*** This output pin is for source driver clock.
81, 80, 79, 78	B15,15, D15, D16	SDCE_N[3:0]	DO16	VCC3IO	***Source Driver Chip Select*** These output pins are to select the source driver chip.
107	A9	SDLE	DO16	VCC3IO	***Source Driver Latch Enable*** This output pin is to enable the source driver latch.
77	E15	SDOE	DO16	VCC3IO	***Source Driver Output Enable*** This output pin is to enable the source driver output.
108	B7	SDSHR	DO16	VCC3IO	***Source Driver Shift Right Enable*** This output pin is to enable the source driver shift right.
106, 103, 102, 101, 93, 92, 91, 90, 89, 88, 87, 86, 85, 84, 83, 82	A8, A10, A11, B9, A15, B16, A13, A14, B10, B13, A12, B11, B12, C12, B14, D14	SDDO[15:0]	DO16	VCC3IO	***Source Driver Data Output*** These output pins are for source driver data output.

Table 5-7. Pin Description of Gate Driver Signals

IT8951E/TE/E-64 Pin(s) No.	IT8951VG/VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
74	M16	GDCLK	DO16	VCC3IO	***Gate Driver Clock*** This output pin is for gate driver clock.
72	M15	GDOE	DO16	VCC3IO	***Gate Driver Output Enable*** This output pin is to enable gate driver output.
73	N16	GDRL	DO16	VCC3IO	***Gate Driver Right/Left Select*** This output pin is to select gate driver right/left.
71	N14	GDSPV	DO16	VCC3IO	***Gate Driver Start Pulse*** This output pin is for the source driver start pulse.

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Table 5-8. Pin Description of Power Switch Signals

IT8951E/TE/E-64 Pin(s) No.	IT8951VG/VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
56	L15	PWR_S_P	DO16	VCC3IO	***Source Driver Positive Power Control*** This output pin is to control the source driver positive power.
57	R13	PWR_S_N	DO16	VCC3IO	***Source Driver Negative Power Control*** This output pin is to control the source driver negative power.
58	L16	PWR_G_P	DO16	VCC3IO	***Gate Driver Positive Power Control*** This output pin is to control the gate driver positive power.
59	T13	PWR_G_N	DO16	VCC3IO	***Gate Driver Negative Power Control*** This output pin is to control the gate driver negative power.
112	A7	PWR_ALERT	DI	VCC3IO	***Alert From Power IC*** This input pin is the error alert input from power IC.
70	N15	BORDER	DO16	VCC3IO	***Display Border Power Control*** This output pin is to control the display border power.

Table 5-9. Pin Description of GPIO Signals

IT8951E/TE/E-64 Pin(s) No.	IT8951VG/VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
69, 68, 67, 66, 65, 64, 63, 62, 106, 103, 102, 101, 93, 92, 91, 90	P12, R14, P15, P16, R16, T16, T15, R15, A8, A10, A11, B9, A15, B16, A13, A14	GPIO[15:0]	DO16	VCC3IO	***Dedicated GPIO Control*** These output pins are for GPIO control.

Table 5-10. Pin Description of USB PHY Signals

IT8951E/TE/E-64 Pin(s) No.	IT8951VG/VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
52	R12	DP	AIO	VCC33A_HSRT	***USB PHY Data*** USB2.0 data in positive pin terminal
51	R11	DM	AIO	VCC33A_HSRT	***USB PHY Data*** USB2.0 data in negative pin terminal
50	T11	RREF	AIO	VCC33A_HSRT	***Reference Control*** Connect external reference resistor(12kΩ +- 1%) to ground

Table 5-11. Pin Description of AC Mode Signals

IT8951E/TE/E-64 Pin(s) No.	IT8951VG/VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
56	L15	VCOM[0]	DO16	VCC3IO	***Panel 0 VCOMIN[0] Control*** This output pin is to control the VCOMIN[0] for AC mode panel.
57	R13	VCOM[1]	DO16	VCC3IO	***Panel 0 VCOMIN[1] Control*** This output pin is to control the VCOMIN[1] for AC mode panel.
58	L16	VCOM1[0]	DO16	VCC3IO	***Panel 1 VCOMIN[0] Control*** This output pin is to control the VCOMIN[0] for AC mode panel.

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IT8951E/TE/E-64 Pin(s) No.	IT8951VG/VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
59	T13	VCOM1[1]	DO16	VCC3IO	***Panel 1 VCOMIN[1] Control*** This output pin is to control the VCOMIN[1] for AC mode panel.
70	N15	SHD_N	DO16	VCC3IO	***Shutdown Control*** This output pin is to control the shutdown c of AC mode panel.
69, 68, 67, 66, 65, 64, 63, 62	P12, R14, P15, P16, R16, T16, T15, R15,	PWR[7:0]	DO16	VCC3IO	***Power Board Control*** These output pins are to control the power board of AC mode panel.

Table 5-12. Pin Description of Built-in Thermal Sensor

IT8951E/TE/E-64 Pin(s) No.	IT8951VG/VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
34	T8	VREF	AIO	VCC33A	***Thermal Sensor Reference Voltage*** This pin is for the reference voltage.
35	R9	TS_EX	AIO	VCC33A	***External Diode Positive*** This pin is used to be connected to the anode of external diode.
36	T10	DN	AIO	VCC33A	***External Diode Negative*** This pin is used to be connected to the cathode of external diode.

Table 5-13. Pin Description of SD Controller Signals (IT8951VG/IT8951VG-64)

IT8951E/TE/E-64 Pin(s) No.	IT8951VG/VG-64 Pin(s) No.	Symbol	Attribute	Power	Description
-	C2	SD_CLK	DO16	VCC3IO	***SD Card Clock*** This output pin is for the SD Card clock.
-	D1	SD_CMD	DIO	VCC3IO	***SD Card Command*** This output pin is for the SD Card command.
-	C1	SD_WP	DI	VCC3IO	***SD Card Write Protect*** This input pin is for the SD Card write protect.
-	B4	SD_CD_N	DI	VCC3IO	***SD Card detect*** This input pin is for the SD Card detect.
-	F2	SD_PWR_N	DO16	VCC3IO	***SD Card Power Controller*** This output pin is for the SD Card power controller.
-	A4, B3, A3, D2	SD_DATA_0~ SD_DATA_3	DIO	VCC3IO	***SD Card Data*** These output pins are for the SD Card data.

Table 5-14. Difference between IT8951E/IT8951TE/ IT8951E-64/IT8951VG/IT8951VG-64

Description	IT8951E-64	IT8951E	IT8951TE	IT8951VG	IT8951VG-64
Embedded DRAM Size	64Mb	32Mb	32Mb	32Mb	64Mb
Package Type	LQFP	LQFP	TQFP	VFBGA	VFBGA
Body Outline	14mm x 14mm x 1.6mm	14mm x 14mm x 1.6mm	14mm x 14mm x 1.2mm	10mm x 10mm x 1mm	10.5mm x 10.5mm x 1mm
No Connect (NC) Pins	38, 39, 40, 41, 42, 43,44	38, 39, 40, 41, 42, 43,44	38, 39, 40, 41, 42, 43,44	J15	J15
Exposed Pad	N/A	N/A	129	N/A	N/A
SD card Host Controller Pins	N/A	N/A	N/A	C2, D1, C1, B4, F2, A4, B3, A3, D2	C2, D1, C1, B4, F2, A4, B3, A3, D2
Analog Ground Pin – VS33D	45	45	45	N/A	N/A

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Table 5-15. Pin Attributes of Different Host Interface

TEST_CFG [2:0]	3'b000 I80CPCR[16]=0	3'b000 I80CPCR[16]=1	3'b001	3'b110	3'b111
Host Interface	Intel 80	Motorola 68	SPI	I2C (Slave ID: 7'h46)	I2C (Slave ID: 7'h35)
Pin Attribute					
HOST_HWE_N	I80, input	I80, input	N/F, output	N/F, output	N/F, output
HOST_HRD_N	I80, input	I80, input	N/F, output	N/F, output	N/F, output
HOST_HCS_N	I80, input	I80, input	N/F, output	N/F, output	N/F, output
HOST_HD_C*	I80, input	I80, input	N/F, output	N/F, output	N/F, output
HOST_HRDY	I80, output	I80, output	N/F, input	N/F, input	N/F, input
HOST_HIRQ	I80, output	I80, output	N/F, input	N/F, input	N/F, input
HOST_HDB[15:0]*	I80, bi-dir	I80, bi-dir	N/F, input	N/F, input	N/F, input
SPI2_SO/ UART_RTS	N/F, output	N/F, output	SPI, output	UART, output	UART, output
SPI2_SI/ UART_CTS	N/F, input	N/F, input	SPI, input	UART, input	UART, input
SPI2_SCK/ I2C2_SCL	N/F, input	N/F, input	SPI, input	I2C, O/D	I2C, O/D
SPI2_CS_N/ I2C2_SDC	N/F, input	N/F, input	SPI, input	I2C, O/D	I2C, O/D

N/F = No Function
O/D = Open Drain
* SFMSR[3] is set to 0

Table 5-16. Interface Signal Mapping for Intel 80 and Motorola 68

Pin Name	Intel 80	Motorola 68
HOST_HWE_N	HWR_L	R/W
HOST_HRD_N	HRD_L	E
HOST_HCS_N	HCS_L	HCS_L
HOST_HD_C	HD/C	HD/C
HOST_HRDY	HRDY	HRDY
HOST_HDB[16:0]	HDB[15:0]	HDB[15:0]

Note: Please refer to section 9.1 for the detailed signal timing for Intel 80 and Motorola 68.

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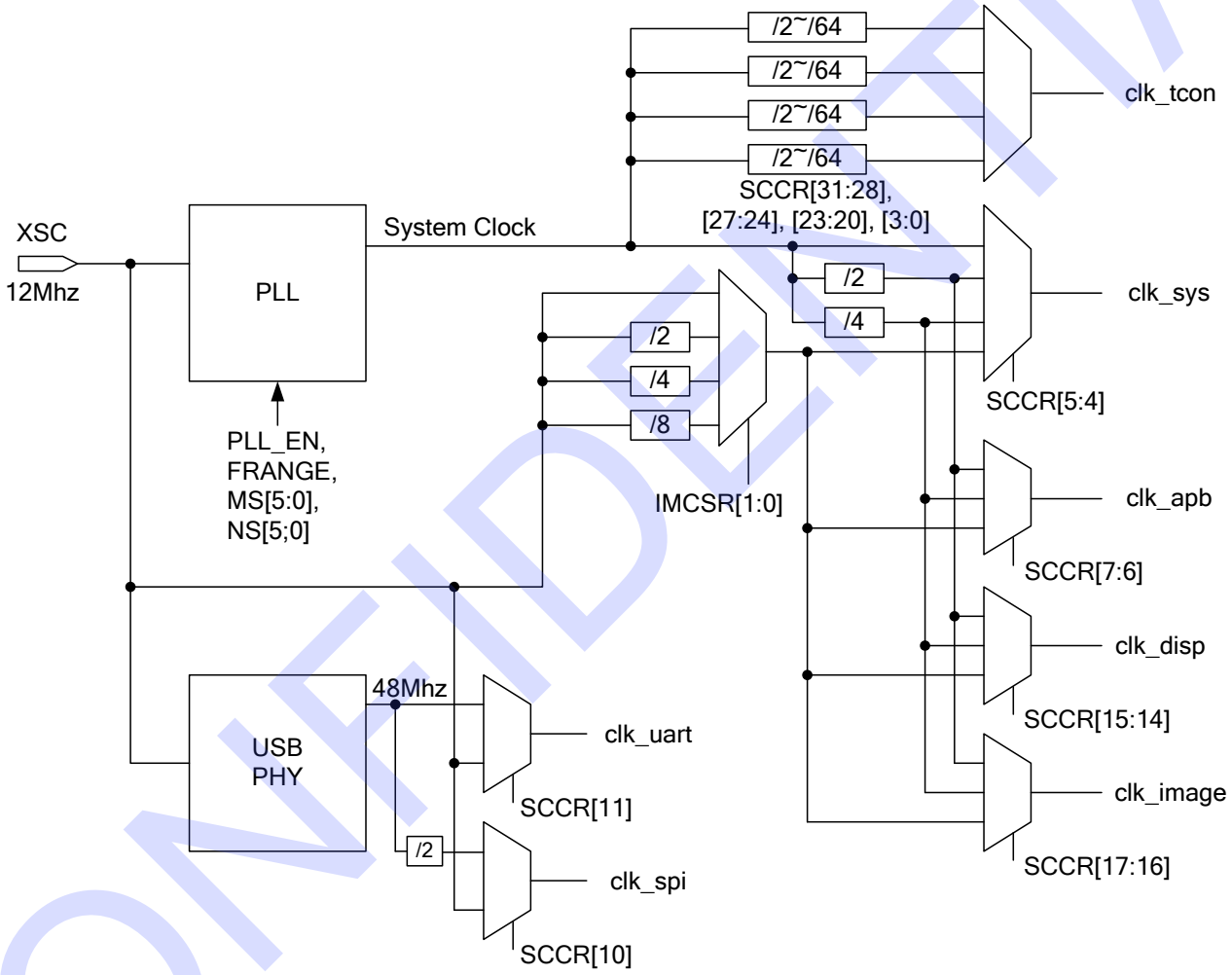
6. System Configuration

6.1 Clock Management

The clock tree of IT8951 is shown in Figure 6-1. clk_sys is the main clock of the system including SDRAM, system bus, etc. Its frequency is decided by the main PLL with programmable MS & NS factor. clk_apb is the hardware register clock. clk_tcon is the source driver clock and can be dynamically switched between 4 tables. All other clocks are also programmable depending on their respective functions.

Figure 6-1. System Clock Tree Diagram



6.2 Power Management

IT8951 has 3 power modes, active, standby, and sleep mode and the correlation among them are shown in Figure 6-2 & Table 6-2 below.

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Figure 6-2. Power Mode State Diagram

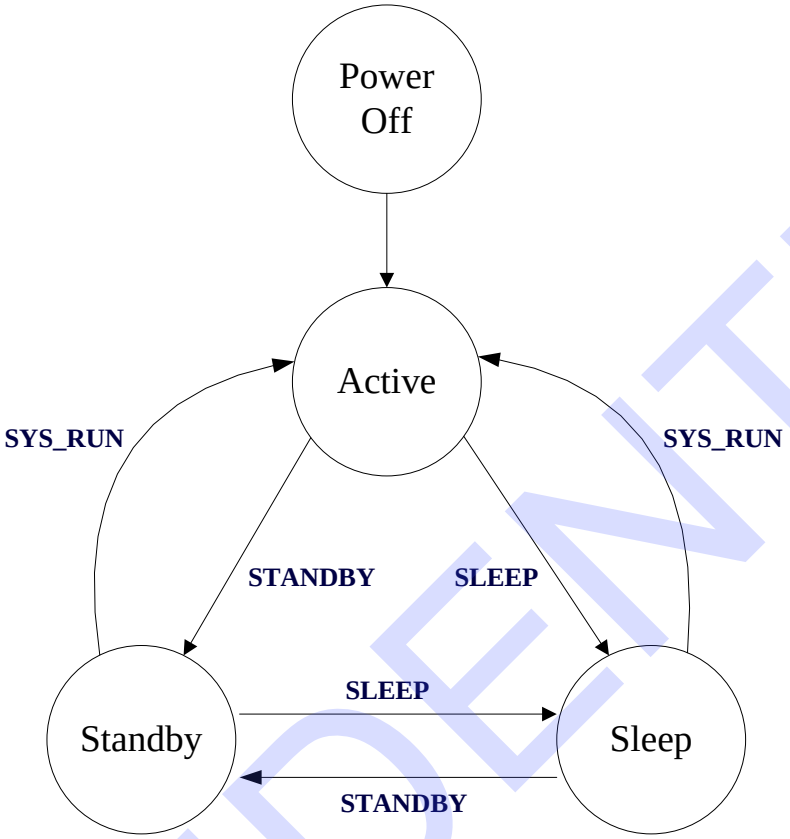

Table 6-1. Power State Summary

Power Mode	IT8951 Controller State	PLL State	Panel Power State	OSC State	SDRAM State
ACTIVE	All clock active	Active	Active	Active	Normal Operation
STANDBY	All clocks gated off (Asynchronous Wakeup)	Active	Active	Active	Self Refresh
SLEEP	PLL off (Asynchronous Wakeup)	Power-Down	Power-Down	Power-Down	Self Refresh

6.3 Vcom and GPO Control Setting

IT8951 supports four IO pins' functional selection. When IT8951 is connected to the AC-panel, the four IO pins act as the VCOM voltage selection. Its output value is controlled by hardware engine according to the AC VCOM Table Register ACVTR0~ACVTR15（0x11C4~0x11E0, 0x122C~0x1248. When IT8951 is connected to the DC-panel, the four IO pins act as the GPO function. Its output value is directly controlled by register （0x0008~0x000C）. Normally, it could be used as a switch of the Source/Gate power circuit. The detailed diagram of these IO pins' functional selection is shown in Figure 6-3.

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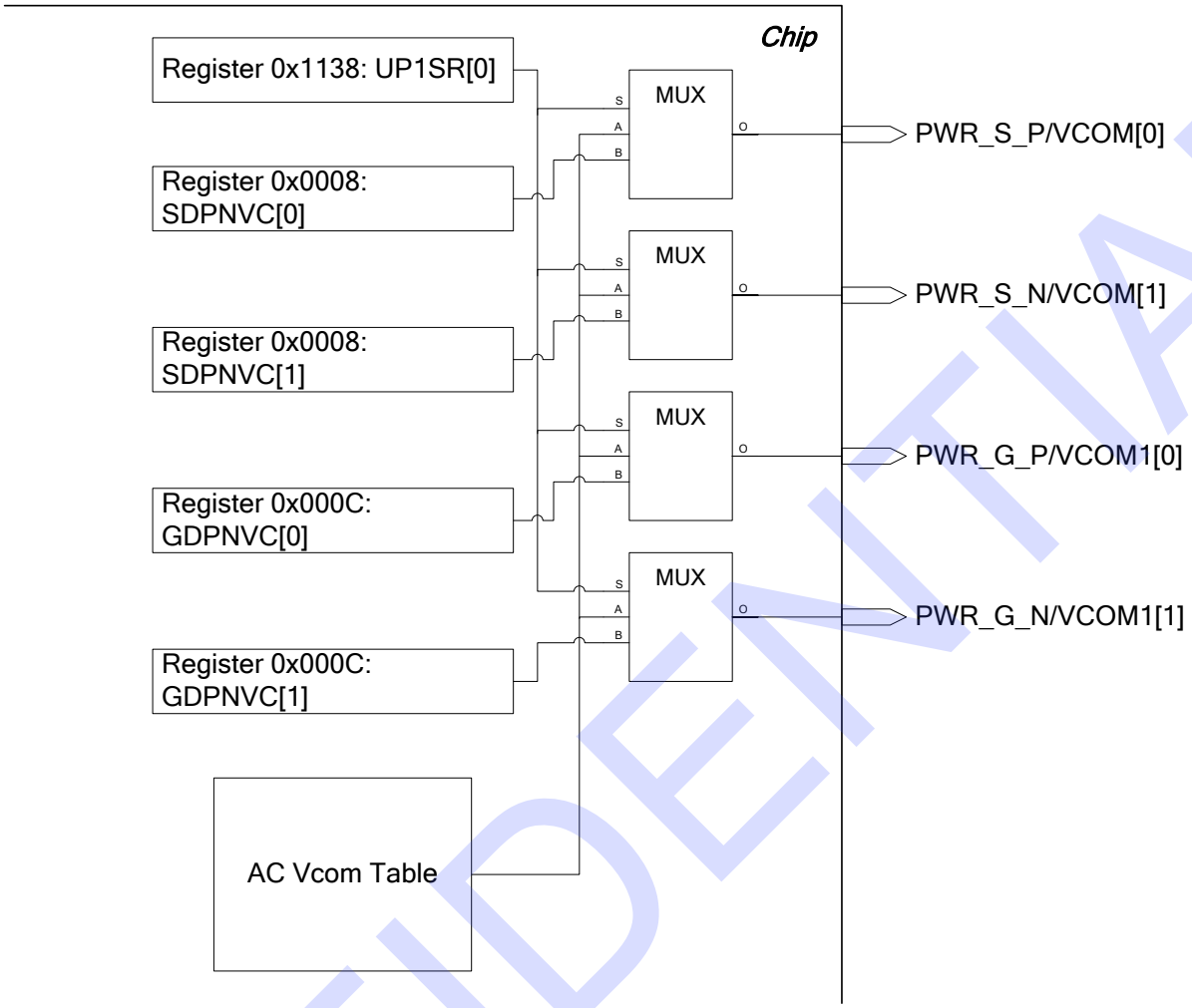
Figure 6-3. IO-pins Functional Selection Diagram



When UP1SR[0] is set high, the mode is AC Vcom and the IO pin is determined by hardware engine.
When UP1SR[0] is set low, the mode is DC Vcom and the IO-pin is determined by register.

6.4 Power On Sequence

Figure 6-4 and Table 6-2 show the power on sequence of IT8951. The core power 1.8V should be stable first then the IO power and analog power 3.3V be ready afterwards and finally the chip reset is de-asserted last.

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Figure 6-4. Power On Sequence Diagram

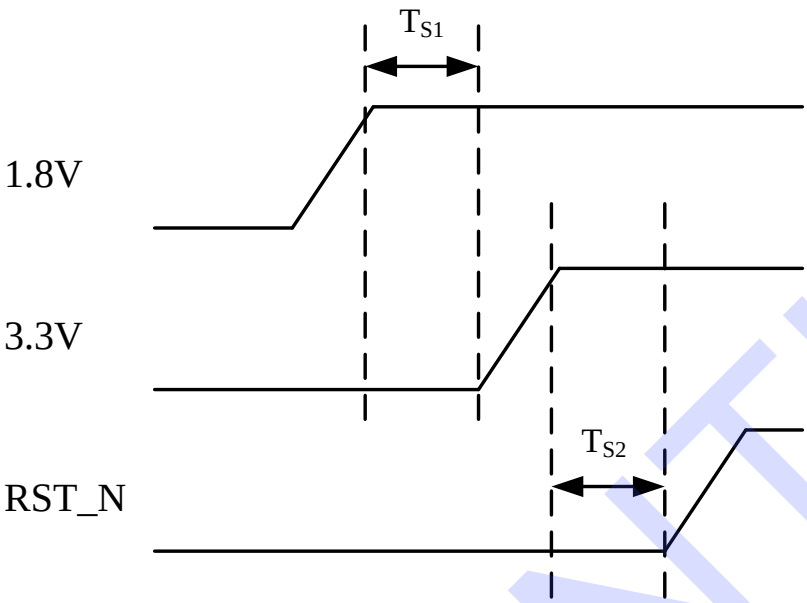

Table 6-2. Power On Stable Time

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{S1}	1.8V stable time	0	-	-	us
T_{S2}	3.3V stable time	10	-	-	us

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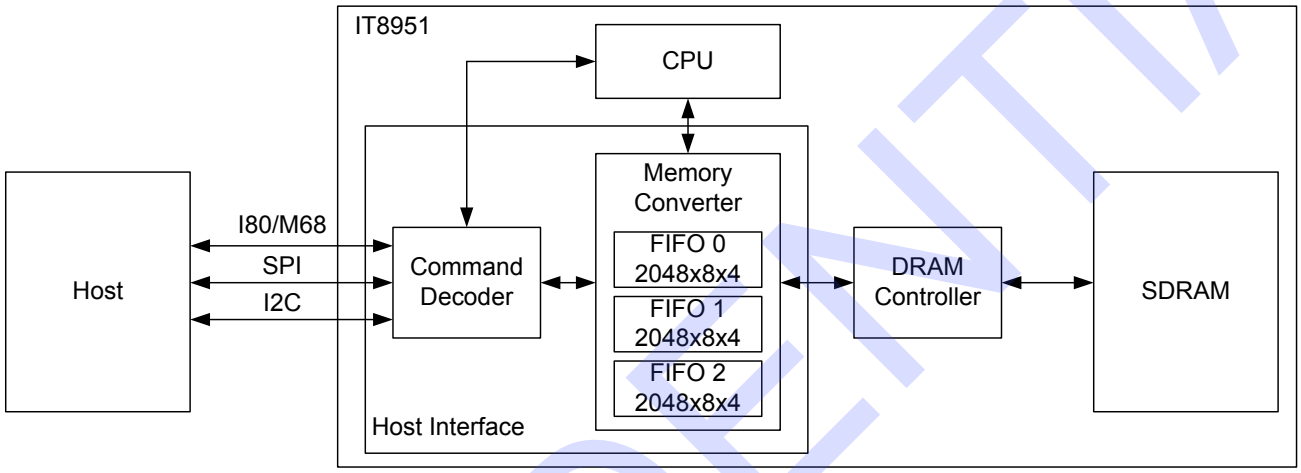
7. Host Interface

7.1 Overview

IT8951 supports various interfaces to connect to the host like Intel 80 (i.e. I80), Motorola 68 (i.e. M68), 4-wire SPI, 2-wire I2C and USB. For the detailed description of USB, please refer to IT8951 datasheet v0.3 or above.

The host interface module handles the other interfaces described above except USB. It includes two sub-modules: command decoder and memory converter. The command decoder sub-module is used to transfer I80/M68/SPI/I2C to the internal bus. The memory converter sub-module handles the data R/W between host side and IT8951 timing controller. The block diagram of the host interface is shown in Figure 7-1.

Figure 7-1. Host Interface Block Diagram



7.2 Features

- Compatible with Intel 80/ Motorola 68 Interface (16 bits data bus)
- Compatible with 4-wire SPI Interface (Mode 0 and 3)
- Compatible with 2-wire I2C Interface
- Supports RGB to Y function
- Enabled to extend command list through firmware
- Receives image data from host interface and sends data to SDRAM
- 24K FIFO (8K x 3)
- Supports burst read/write data from/to SDRAM through host interface
- Supports image rotating function (degree 0, 90, 180, 270)
- Supports different length of pixel (2 bits, 3 bits, 4 bits, 8 bits)
- Supports packed pixel transfer
- Supports any starting position of an image
- Supports rotation DMA function

7.3 Host Interface Selecetion

TEST_CFG[2:0] pins are used for the selection of different host interfaces, which are listed in Table 7-1. The detailed pin attributes of different host interface are shown in Table 5-15.

Table 7-1. Host Interface Selection

TEST_CFG [2:0]	I80CPCR [16]	Host Interface	Used Pins			
			HOST_*	SPI2_*	I2C2_*	UART_RTS UART_CTS
3'b000	1'b0 (default)	Intel 80	Yes	No	No	No
3'b000	1'b1	Motorola 68	Yes	No	No	No
3'b001	Don't care	SPI	No	Yes	No	No

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3'b110	Don't care	I2C (Slave ID : 7'h46)	No	No	Yes	Yes
3'b111	Don't care	I2C (Slave ID : 7'h35)	No	No	Yes	Yes
Others	Don't care	Reserved	-	-	-	-

7.4 Command Operation

7.4.1 Intel 80 / Motorola 68 Command & Parameter/Data Cycle

The I80 host command cycle is shown in Figure 7-2 and Figure 7-3, and the M68 host command cycle is shown in Figure 7-4 and Figure 7-5. HCS_L pin is used to determine this packet is a command or a parameter/data. All supported commands are listed in Table 7-4.

Figure 7-2. I80 Parameter/Data Write Cycle

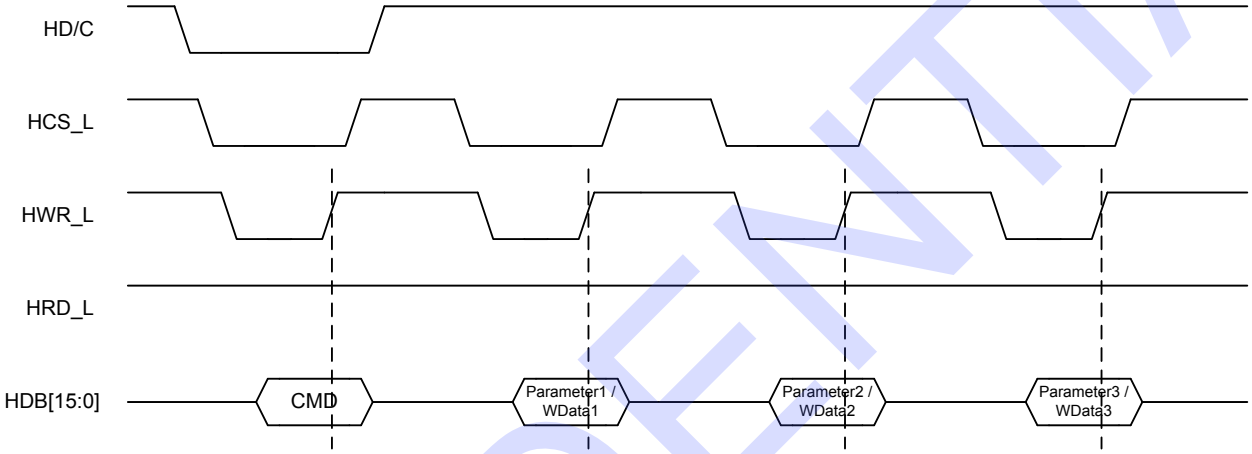

Figure 7-3. I80 Data Read Cycle

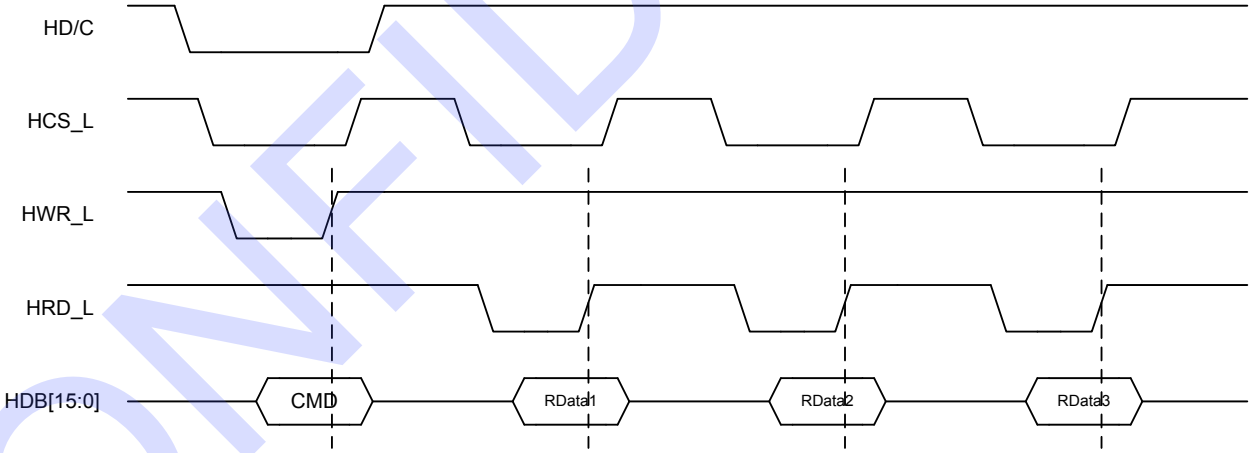

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Figure 7-4. M68 Parameter/Data Write Cycle

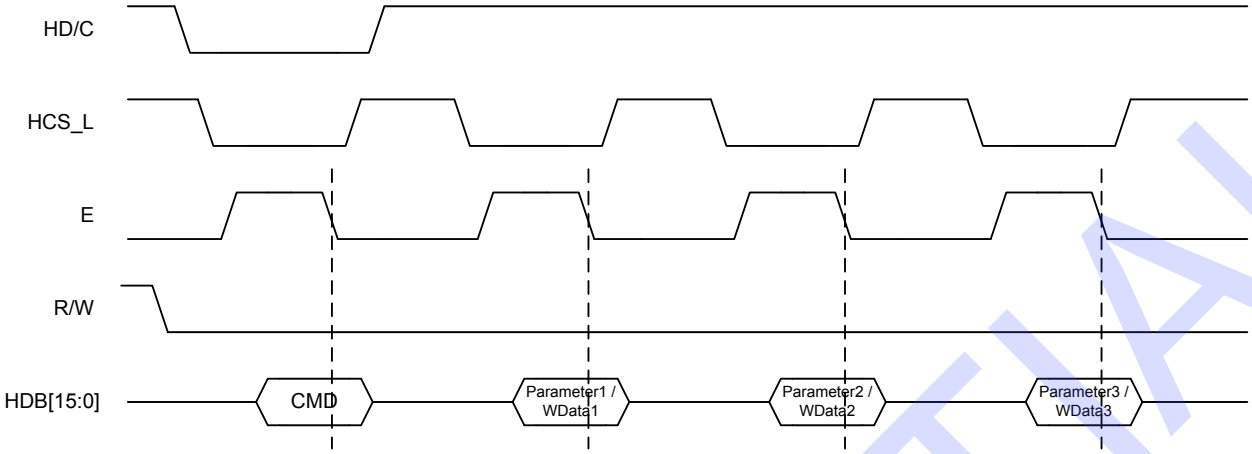
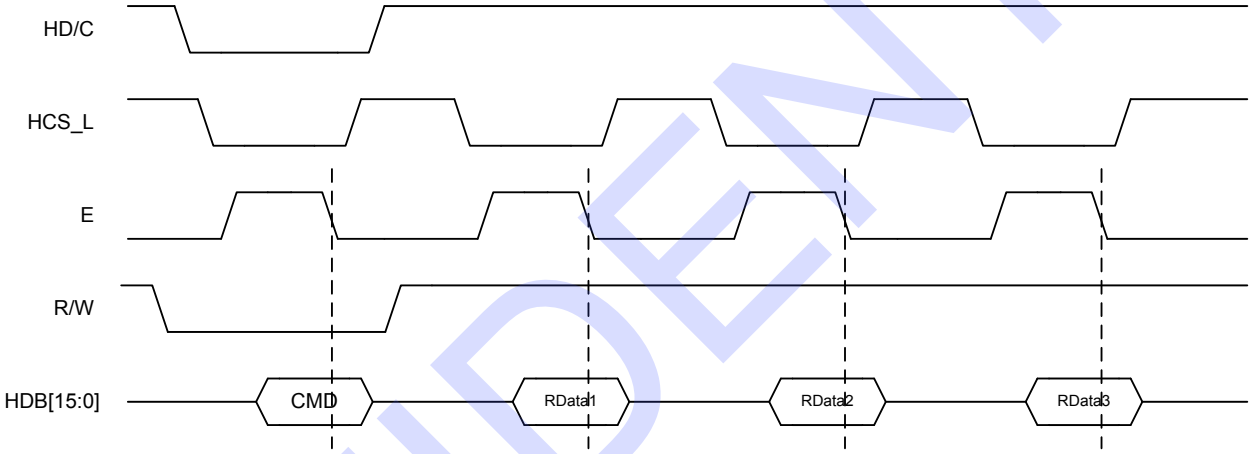


Figure 7-5. M68 Data Read Cycle



7.4.2 SPI Command & Parameter/Data Cycle

The SPI has no signal like the HCS_N pin to tell from command cycle or data cycle, so every packet must contain a preamble word prior to the command/data field. The preamble words are list in Table 7-2.

Table 7-2. Preamble Word of SPI

Packet Type	Preamble Word
Command	0x6000
Write Data	0x0000
Read Data	0x1000

The SPI read/write cycle is show in Figure 7-6, Figure 7-7, and Figure 7-8. All messages are sent by MSB first order. For convenience, SPI clock – SPI2_CLK pin is not shown in the following figures.

Figure 7-6. SPI Command Cycle

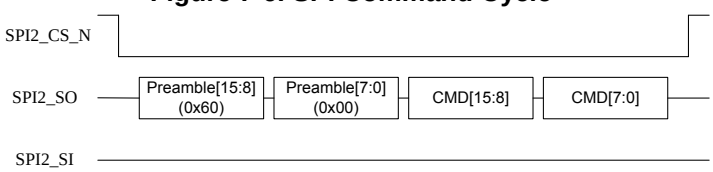


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Figure 7-7. SPI Parameter/Data Write Cycle

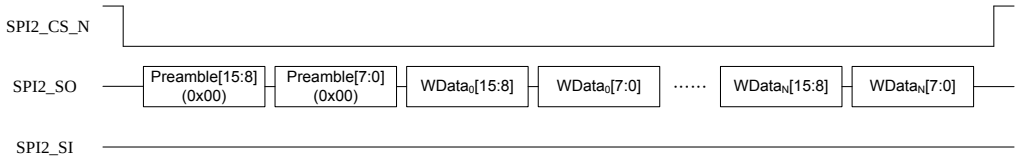
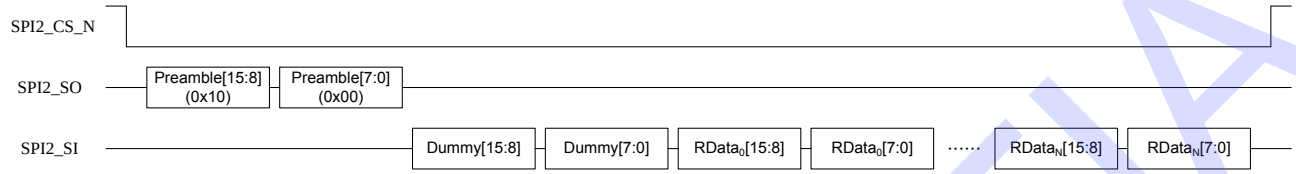
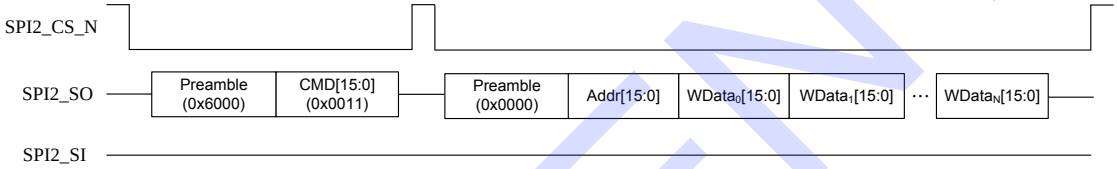


Figure 7-8. SPI Parameter/Data Read Cycle



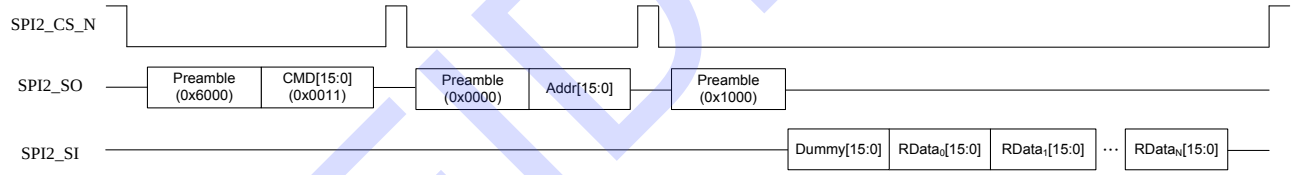
Then the host can send any commands using the above 3 types of packets. The following example illustrates the REG_WR command.

Figure 7-9. SPI REG_WR Cycle



The following example illustrates the REG_RD command.

Figure 7-10. SPI REG_RD Cycle



7.4.3 I2C Command & Parameter/Data Cycle

The I2C has no signal like the HCS_N pin to tell from command cycle or data cycle, so every packet also needs a preamble byte prior to the command/data field. The preamble bytes are list in Table 7-3.

Table 7-3. Preamble Byte of I2C

Packet Type	Preamble Byte
Command	0x00
Write Data	0x80
Read Data	0x80

The I2C read/write cycle is show in Figure 7-11, Figure 7-12, and Figure 7-13. All messages are sent by LSB first order.

Figure 7-11. I2C Command Cycle

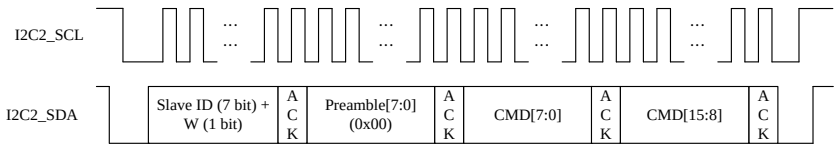


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Figure 7-12. I2C Parameter/Data Write Cycle

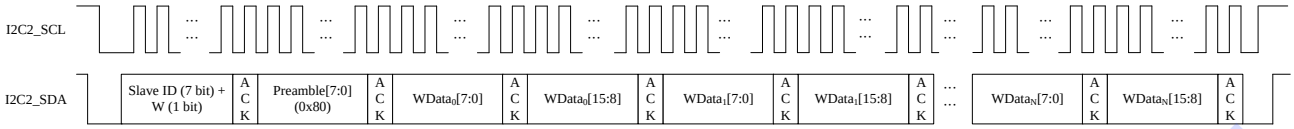
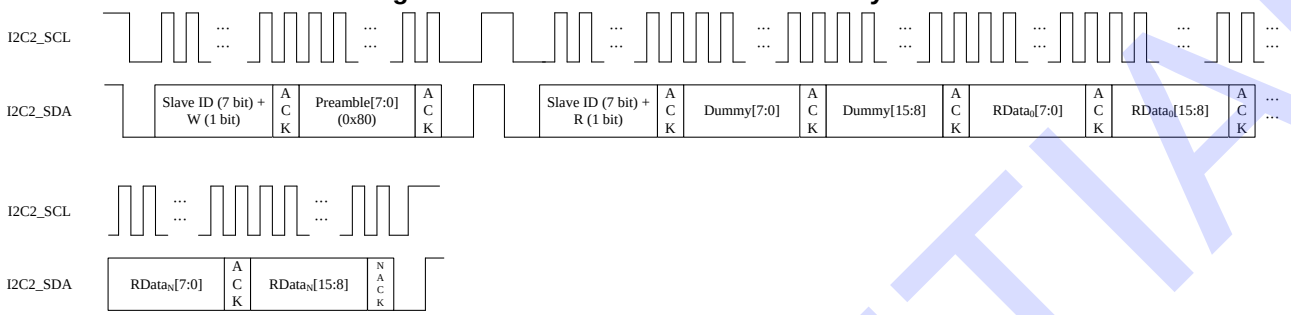
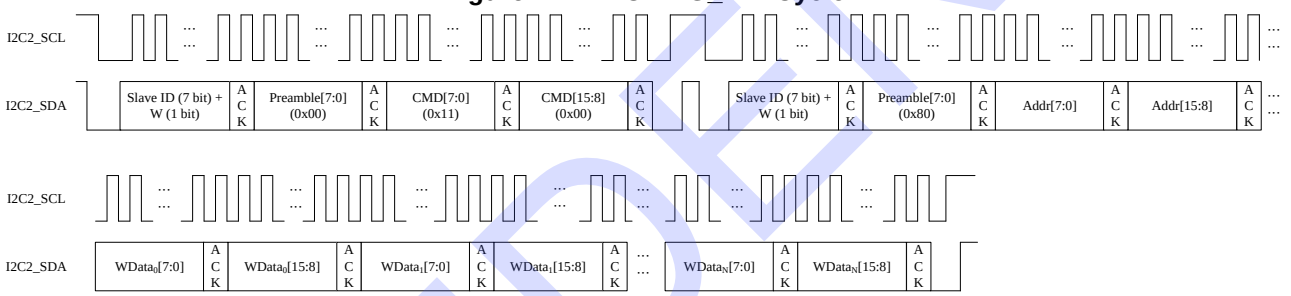


Figure 7-13. I2C Parameter/Data Read Cycle



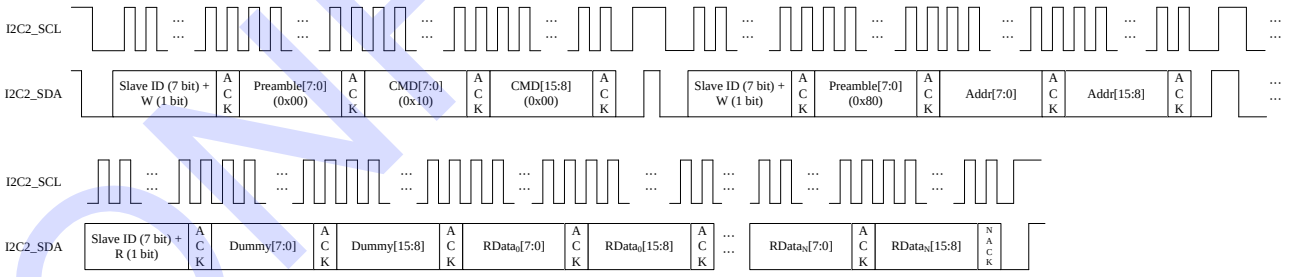
Then host can send any commands using the above 3 types of packets. The following example illustrates the REG_WR command.

Figure 7-14. I2C REG_WR Cycle



The following example illustrates the REG_RD command.

Figure 7-15. I2C REG_RD Cycle



7.4.4 Command Lists

Here are the command lists.

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Table 7-4. Host Interface Command Lists

Command List	Code	Parameter					Data	Description
SYS_RUN	0x0001							System running Command (enable all clocks, and go to active state)
STANDBY	0x0002							Standby Command (gate off clocks, and go to standby state)
SLEEP	0x0003							Sleep Command (disable all clocks, and go to sleep state)
REG_RD	0x0010	Addr[15:0]					rdata[15:0]	Read Register Command
REG_WR	0x0011	Addr[15:0]					wdata[15:0]	Write Register Command
MEM_BST_RD_T(*)	0x0012	Addr[15:0]	Addr[25:16]	Cnt[15:0]	Cnt[25:16]			Memory Burst Read Trigger Command (This command will trigger internal FIFO to read data from memory.)
MEM_BST_RD_S	0x0013						rdata[15:0]*cnt	Memory Burst Read Start Command (This is only a data read command. It will read data from internal FIFO. So, this command should be issued after MEM_BST_RD_T command)
MEM_BST_WR (*)(**)	0x0014	Addr[15:0]	Addr[25:16]	Cnt[15:0]	Cnt[25:16]		wdata[15:0]*cnt	Memory Burst Write Command
MEM_BST_END	0x0015							End Memory Burst Cycle
LD_IMG(*)	0x0020	ARG[15:0]					wdata[15:0]*n	Load Full Image Command (AEG[15:0] see Register 0x200) (Write Data Number equals to full display size)
LD_IMG_AREA(*)	0x0021	ARG[15:0]	start_x[10:0]	start_y[10:0]	width[11:0]	height[11:0]	wdata[15:0]*n	Load Partial Image Command (AEG[15:0] see Register 0x200) (Write Data Number equals to partial display size according to width and height)

* For these commands, the parameters are unnecessary when bit 0 of I80CPCR is false.
** The rotation angle of MCSR[1:0] must be 2'b00.

7.5 Data Transfer

7.5.1 Data Transfer Format

IT8951 supports 2bpp, 3bpp, 4bpp, and 8bpp pixel data formats. The ways they are packed are shown in the following figures.

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Figure 7-16. Different Format of Pixel Length

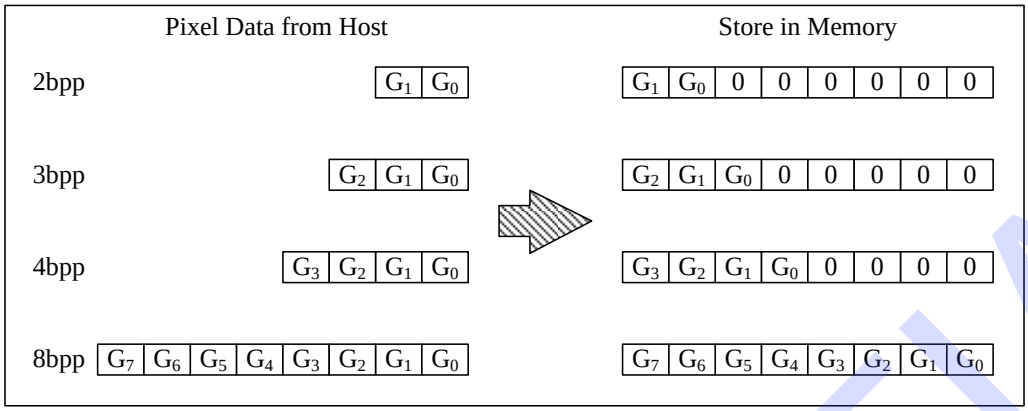
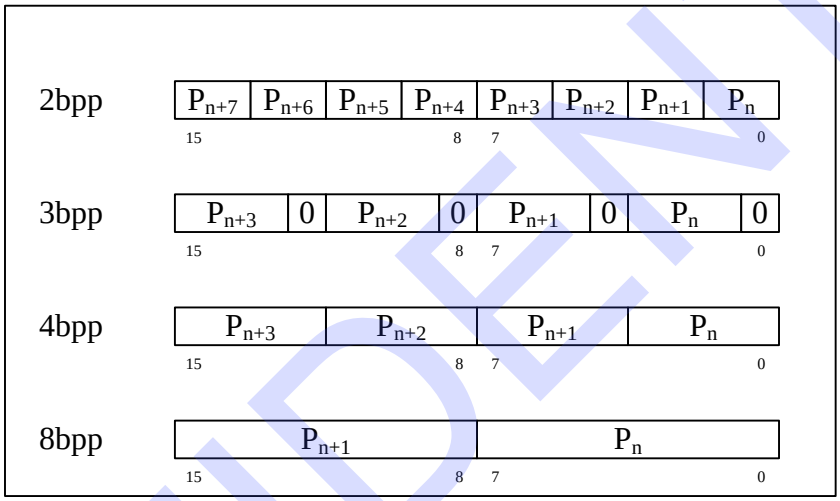


Figure 7-17. Packed Pixel Data Transfer



For color image inputs, IT8951 supports 3 color formats: ARGB8888, RGB888 and RGB565. R, G, B components are transferred to gray level image by multiplying the programmable factor. The data packet timing is shown in Figure 7-18.

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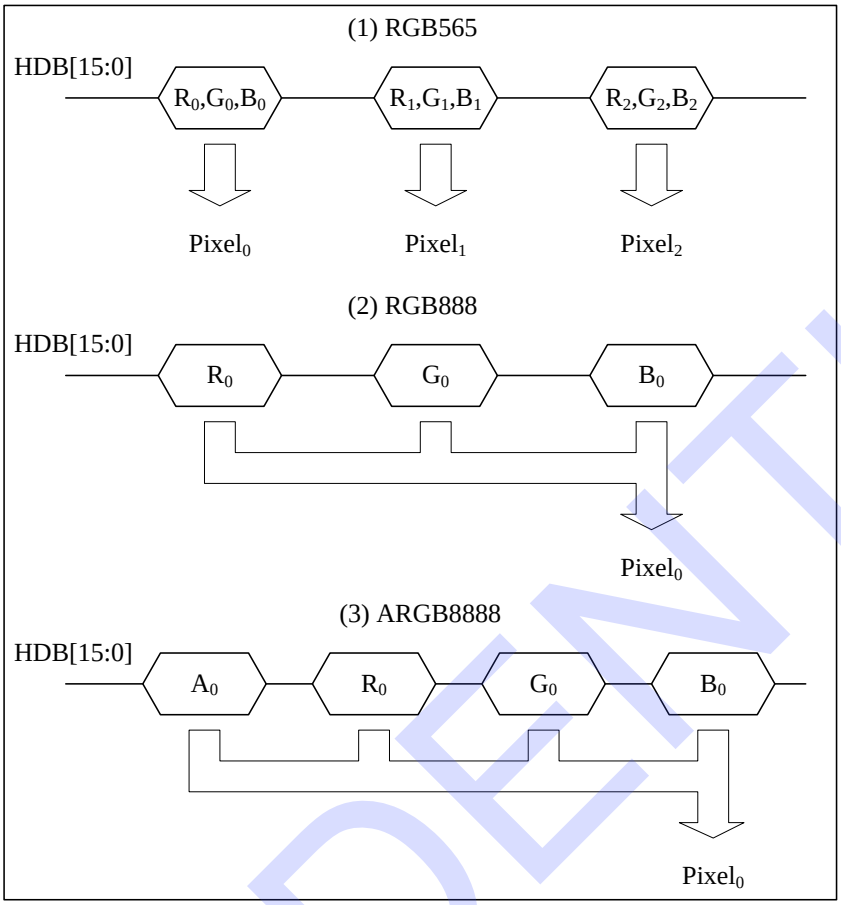
Figure 7-18. Color Data Packet Timing



7.5.2 Image Rotation

IT8951 supports 0/90/180/270-degree rotation by the hardware when transferring the image. The relationship of each rotation angle is shown in the following figures.

Figure 7-19. Relationship of 90-degree Rotation

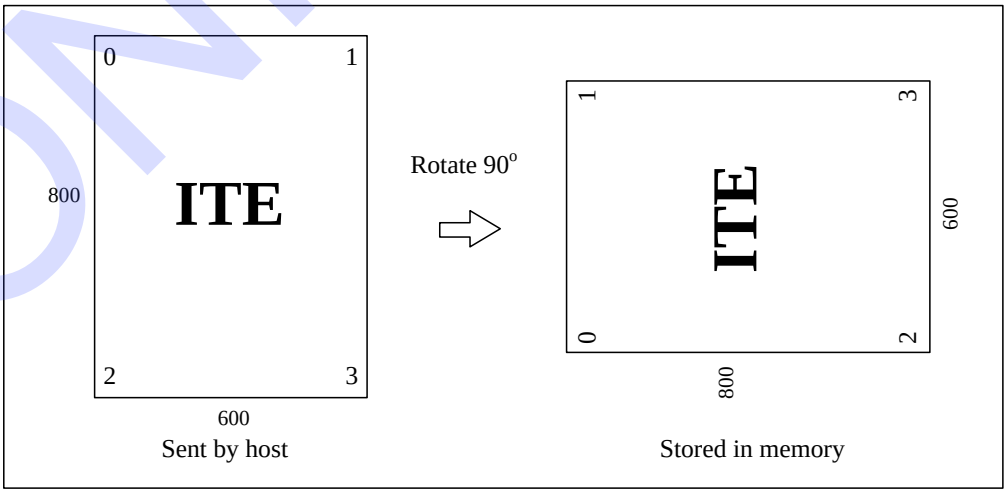


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Figure 7-20. Relationship of 180-degree Rotation

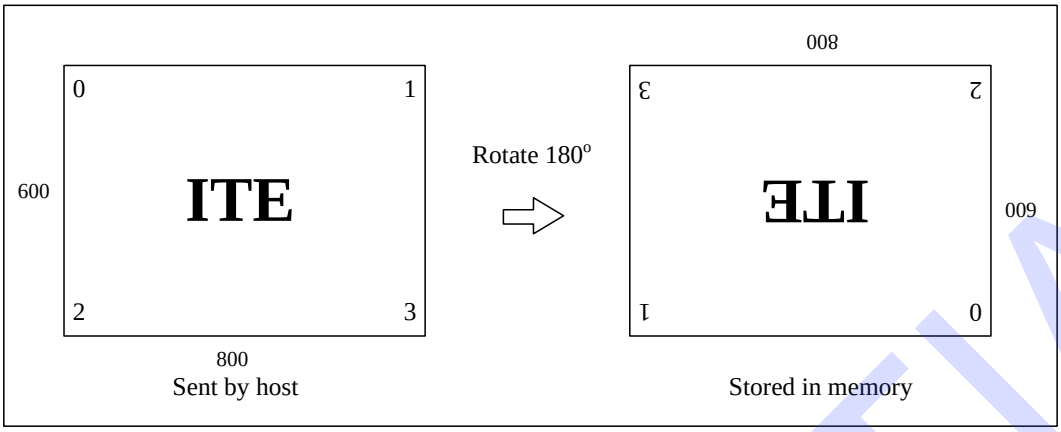
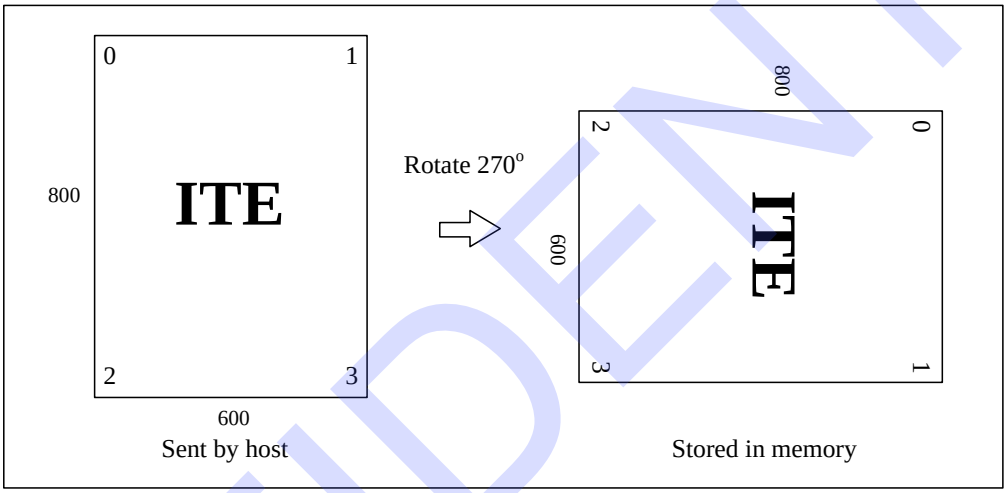


Figure 7-21. Relationship of 270-degree Rotation



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8. DC Characteristics

Operation Conditions

VCC3IO ..... 3.3V±0.15V
VCC33A..... 3.3V±0.15V
VCC33A_U20..... 3.3V±0.15V
VCC33A_HSRT..... 3.3V±0.15V
VCC18A..... 1.8V±0.09V
VCCK..... 1.8V±0.09V
VCC_SDR ..... 1.8V±0.09V
Operation Temperature (Ta) ..... 0°C to +70°C

Absolute Maximum Ratings*

Applied Voltage ..... -0.3V to 3.6V
Input Voltage (Vi)..... -0.3V to VCC3IO+0.3V
Output Voltage (Vo)..... -0.3V to VCC3IO+0.3V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 300mW

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DO16 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -16 mA	2.4			V
DIO16 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 8 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -8 mA	2.4			V
V_{IL}	Low Input Voltage				VCC3IO *0.3	V
V_{IH}	High Input Voltage		VCC3IO *0.7			V
I_{IL}	Low Input Leakage	V_{IN} = 0		10		μA
I_{IH}	High Input Leakage	V_{IN} = VCC3IO			-10	μA
I_{OZ}	Tri-state Leakage				20	μA

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9. AC Characteristics

9.1 Host Interface Timing

Figure 9-1. Read Timing for Intel 80 Interface

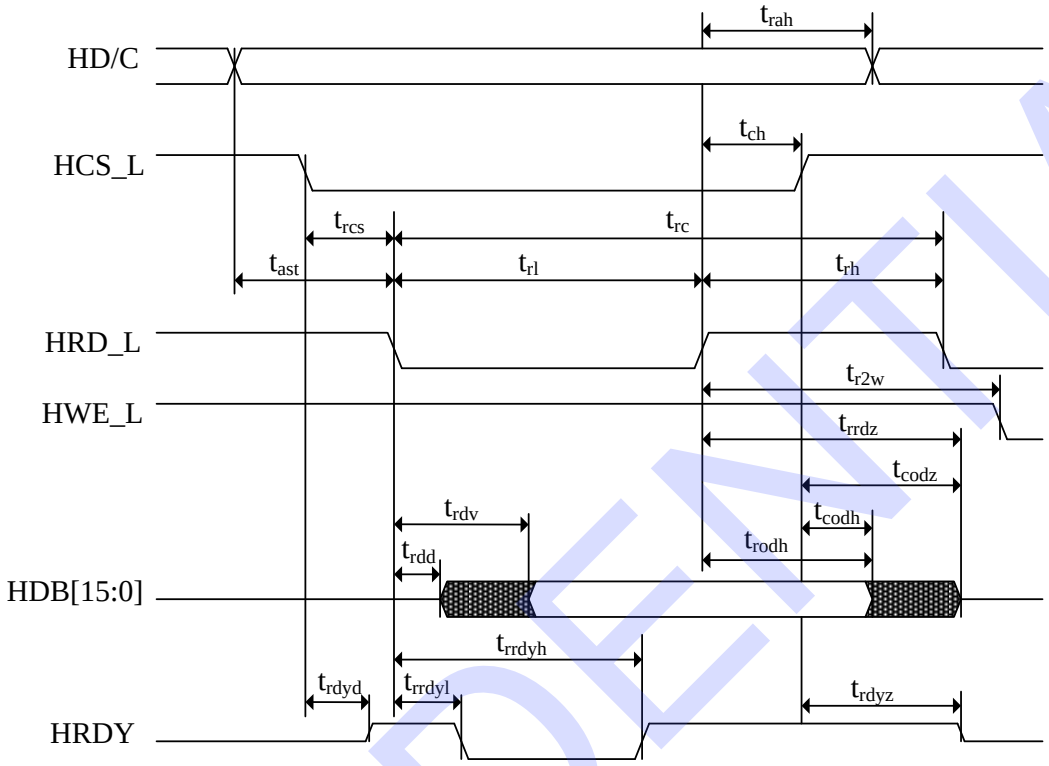

Figure 9-2. Write Timing for Intel 80 Interface

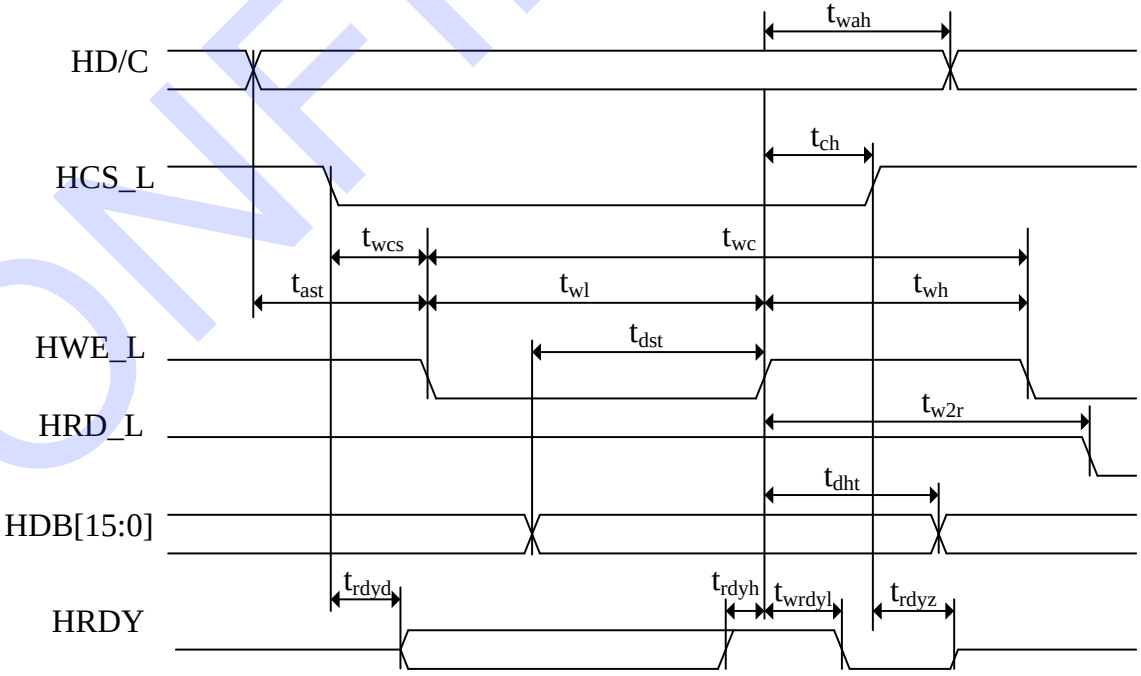

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Table 9-1. AC Characteristic for Intel 80

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
HD/C	t_{ast}	Address setup time (write)	0		ns	
		Address setup time (read)	5		ns	
	t_{wah}	Address hold time (write)	5		ns	
	t_{rah}	Address hold time (read)	0		ns	
HCS_L	t_{wcs}	Chip Select setup time to HWE_L falling edge	0		ns	
	t_{rcs}	Chip Select setup time to HRD_L falling edge	5		ns	
	t_{ch}	Chip Select hold time (write)	5		ns	
		Chip Select hold time (read)	10		ns	
HWE_L	t_{wl}	Pulse low duration	5		ns	
	t_{wh}	Pulse high duration	5		ns	
	t_{wc}	Write cycle for Register	8		Ts	
		Write cycle for Memory	12		Ts	
	t_{w2r}	HWE_L rising edge to HRD_L falling edge	6		Ts	
HRD_L	t_{r2w}	HRD_L rising edge to HWE_L falling edge	0		ns	
	t_{rc}	Read cycle for Registers	9		Ts	
		Read cycle for Memory	5		Ts	
	t_{rl}	Pulse low duration (for Registers)	8T + 10		Ts	
		Pulse low duration (for Memory)	4T + 10		Ts	
	t_{rh}	Pulse high duration	5		ns	
HDB[15:0]	t_{dst}	Write data setup time	7		ns	
	t_{dht}	Write data hold time	6		ns	
	t_{rodz}	Read data hold time from HRD_L rising edge	10		ns	
	t_{rrdz}	HRD_L rising edge to HDB[15:0] Hi-Z		11	ns	
	t_{codh}	Read data hold time from HCS_L rising edge		0	ns	
	t_{crdz}	HCS_L rising edge to HDB[15:0] Hi-Z		0	ns	
	t_{rdv}	HRD_L falling edge to HDB[15:0] valid for Registers		8T + 10	ns	
		HRD_L falling edge to HDB[15:0] valid for Memory (if t_{rc} not met)		4T+10	ns	
	t_{rdd}	HRD_L falling edge to HDB[15:0] driven		0	ns	
HRDY	t_{rdyd}	HCS_L falling edge to HRDY driven		0	ns	
	t_{rdyz}	HCS_L rising edge to HRDY Hi-Z		0	ns	
	t_{wrdyl}	HWE_L rising edge to HRDY low		2	Ts	
	t_{rrdyl}	HRD_L falling edge to HRDY low		2	Ts	
	t_{rrdyh}	HRD_L falling edge to HRDY high		8T + 11	Ts	
	t_{rdyh}	HRDY high to HWE_L rising edge	5		ns	

1. Ts = system clock period

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Figure 9-3. Read Timing for Motorola 68 Interface (E as Data latch Signal)

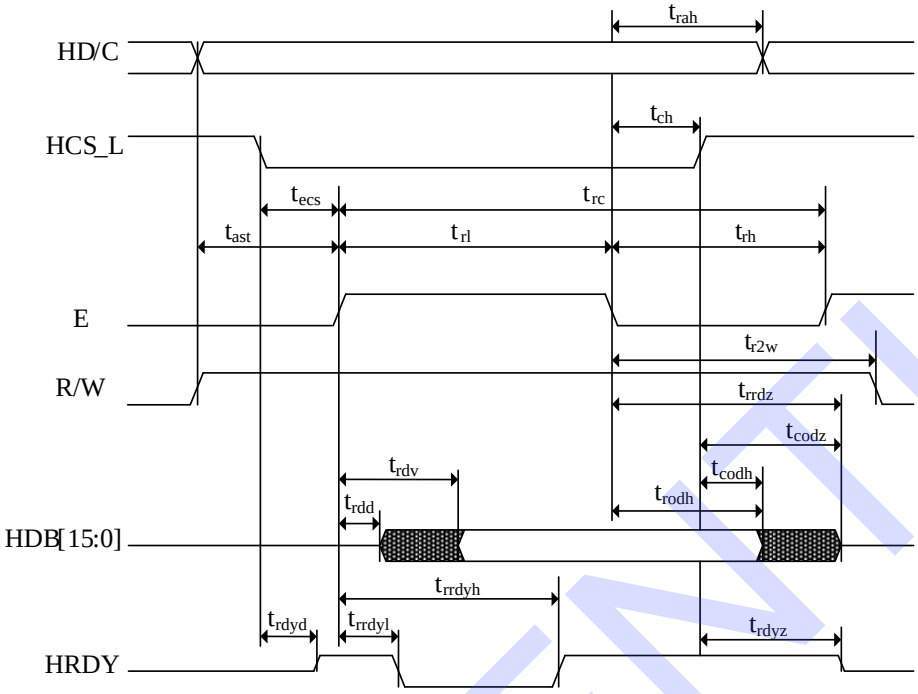

Figure 9-4. Read Timing for Motorola 68 Interface (HCS_L as Data latch Signal)

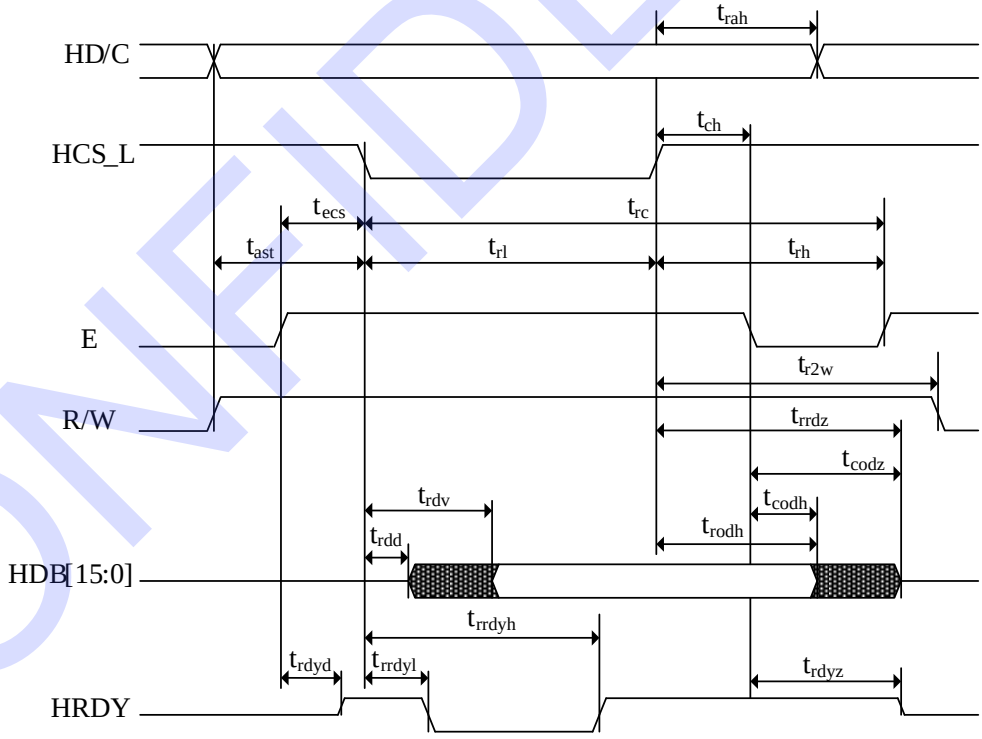

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Figure 9-5. Write Timing for Motorola 68 Interface (E as Data latch Signal)

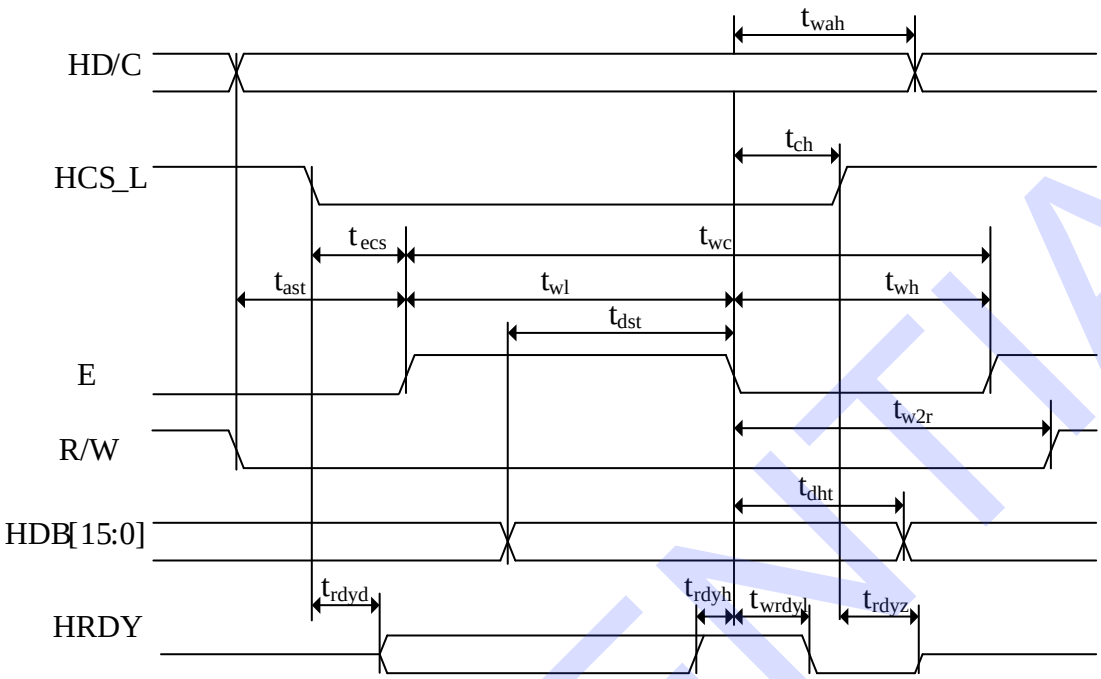

Figure 9-6. Write Timing for Motorola 68 Interface (HCS_L as Data latch Signal)

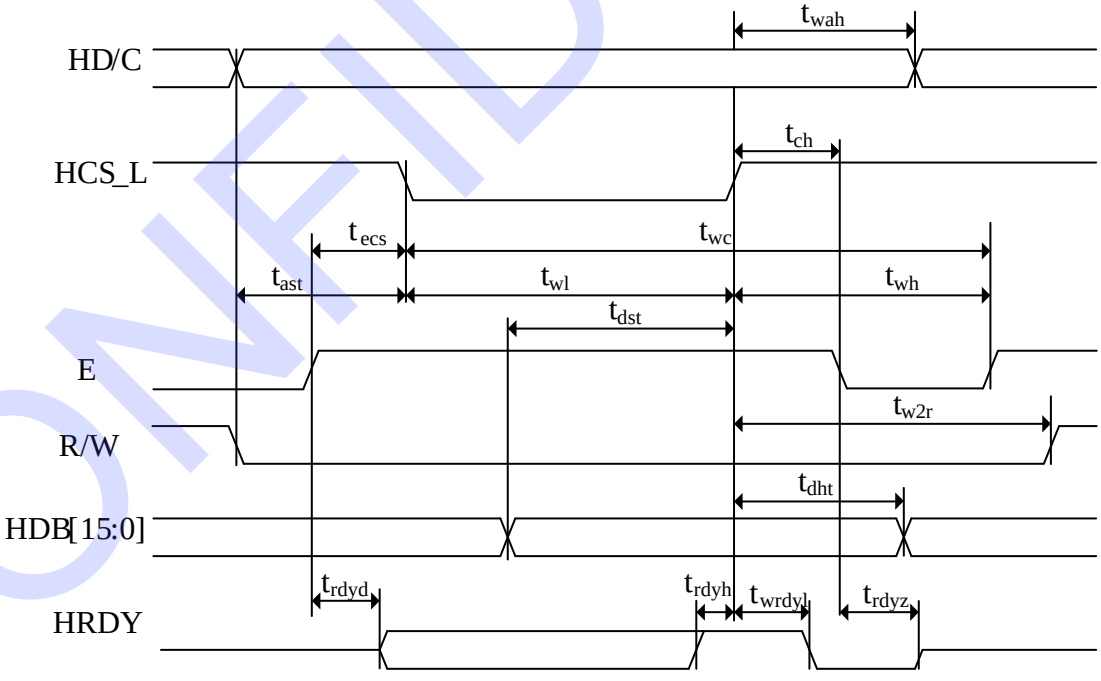

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Table 9-2. AC CharacteristicS for Motorola 68

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
HD/C	t_{ast}	Address setup time write)	5		ns	
		Address setup time (read)	5		ns	
	t_{wah}	Address hold time (write)	5		ns	
	t_{rah}	Address hold time (read)	0		ns	
HCS_L	t_{ecs}	Chip Select setup time to E falling edge E setup time to HCS_L falling edge	5		ns	
	t_{ch}	Chip Select/Enable hold time	10		ns	
E	t_{wl}	Pulse low duration (write)	5		ns	
	t_{wh}	Pulse high duration (write)	5		ns	
	t_{wc}	Write cycle for Register	8		Ts	
		Write cycle for Memory	12		Ts	
	t_{w2r}	HCS_L falling/E rising edge to R/W rising edge	6		Ts	
	t_{r2w}	HCS_L falling/E rising edge to R/W falling edge	0		ns	
	t_{rc}	Read cycle for Registers	9		Ts	
		Read cycle for Memory	5		Ts	
	t_{rl}	Pulse low duration (for Registers read)	8T + 10		Ts	
		Pulse low duration (for Memory read)	4T + 10		Ts	
	t_{rh}	Pulse high duration	5		ns	
HDB[15:0]	t_{dst}	Write data setup time	7		ns	
	t_{dht}	Write data hold time	6		ns	
	t_{rodz}	Read data hold time from HRD_L rising edge	10		ns	
	t_{rrdz}	HRD_L rising edge to HDB[15:0] Hi-Z		11	ns	
	t_{codh}	Read data hold time from HCS_L rising edge		0	ns	
	t_{crdz}	HCS_L rising edge to HDB[15:0] Hi-Z		0	ns	
	t_{rdv}	HRD_L falling edge to HDB[15:0] valid for Registers		8T + 10	ns	
		HRD_L falling edge to HDB[15:0] valid for Memory (if t_{rc} not met)		4T+10	ns	
	t_{rdd}	HRD_L falling edge to HDB[15:0] driven		0	ns	
HRDY	t_{rdyd}	HCS_L falling edge to HRDY driven		0	ns	
	t_{rdyz}	HCS_L rising edge to HRDY Hi-Z		0	ns	
	t_{wrdyl}	HWE_L rising edge to HRDY low		2	Ts	
	t_{rrdyl}	HRD_L falling edge to HRDY low		2	Ts	
	t_{rrdyh}	HRD_L falling edge to HRDY high		8T + 11	Ts	
	t_{rdyh}	HRDY high to HCS_L falling/E rising edge edge	5		ns	

1. Ts = system clock period

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9.2 I²C Master and Slave Timing

Figure 9-7. Definition of Timing for I²C Interface

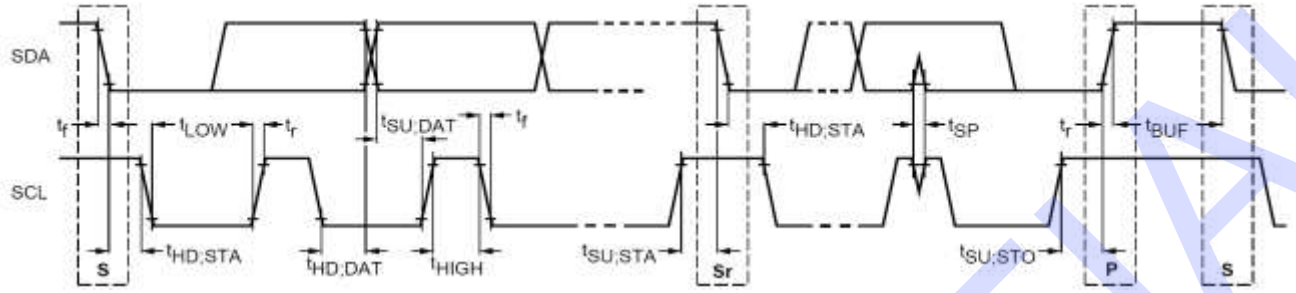

Table 9-3. I²C AC Characteristics

Symbol	Parameter	Min.	Max.	Unit
f_{SCL}	SCL clock frequency	1	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6	-	us
t_{LOW}	LOW period of the SCL clock	1.3	-	us
t_{HIGH}	HIGH period of the SCL clock	0.6	-	us
$t_{SU;STA}$	Set-up time for a repeated START condition	0.6	-	us
$t_{HD;DAT}$	Data hold time	0	0.9	us
$t_{SU;DAT}$	Data set-up time	100	-	ns
t_r	Rise time of both SDA and SCL signals	$20+0.1C_b$	300	ns
t_f	Fall time of both SDA and SCL signals	$20+0.1C_b$	300	ns
$t_{SU;STO}$	Set-up time for STOP condition	0.6	-	us
t_{BUF}	Bus free time between a STOP and START condition	1.3	-	us
C_b	Capacitive load for each bus line	-	400	pF
V_{nL}	Noise margin at the LOW level for each connected device (including hysteresis)	$0.1V_{DD}$	-	V
V_{nH}	Noise margin at the HIGH level for each connected device (including hysteresis)	$0.2V_{DD}$	-	V
$t_{timeout}$	Cumulative SCL low timeout limit	3	5	ms

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9.3 SPI Slave Timing

Figure 9-8. Definition of Timing for SPI Interface

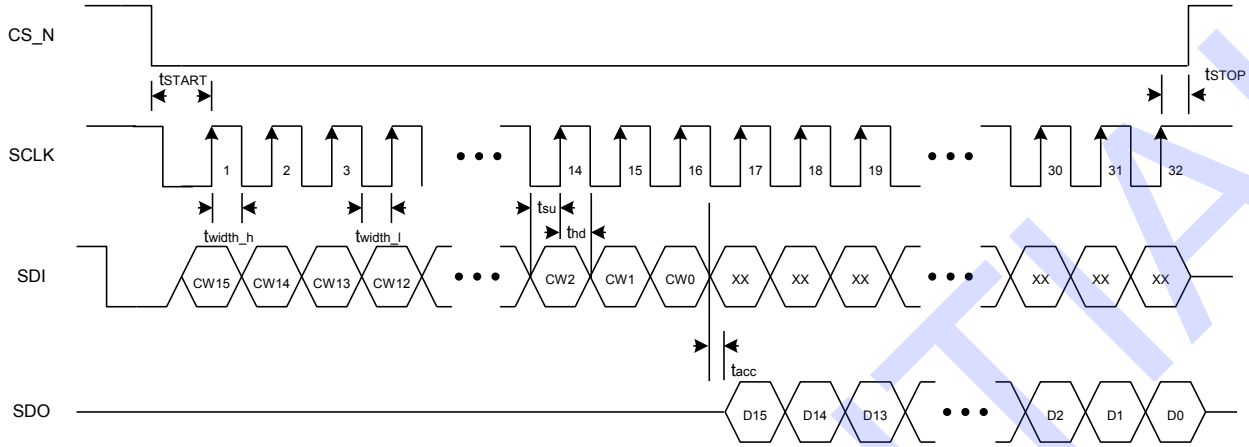

Table 9-4. SPI AC Characteristics

Symbol	Parameter	Min.	Max.	Unit
f_{SCLK}	SCKL clock frequency	0	24	MHz
t_{START}	CS_N falling to SCLK rising edge	10	-	ns
t_{STOP}	SCLK rising to CS_N rising edge	10	-	ns
t_{width_h}	SCLK high pulse width	20	-	ns
t_{width_l}	SCLK low pulse width	20	-	ns
t_{SU}	SDI to SCLK Setup time	10	-	ns
t_{HD}	SDI to SCLK hold time	10	-	ns
t_{acc}	SDO access time after SCLK falling edge	-	20	ns

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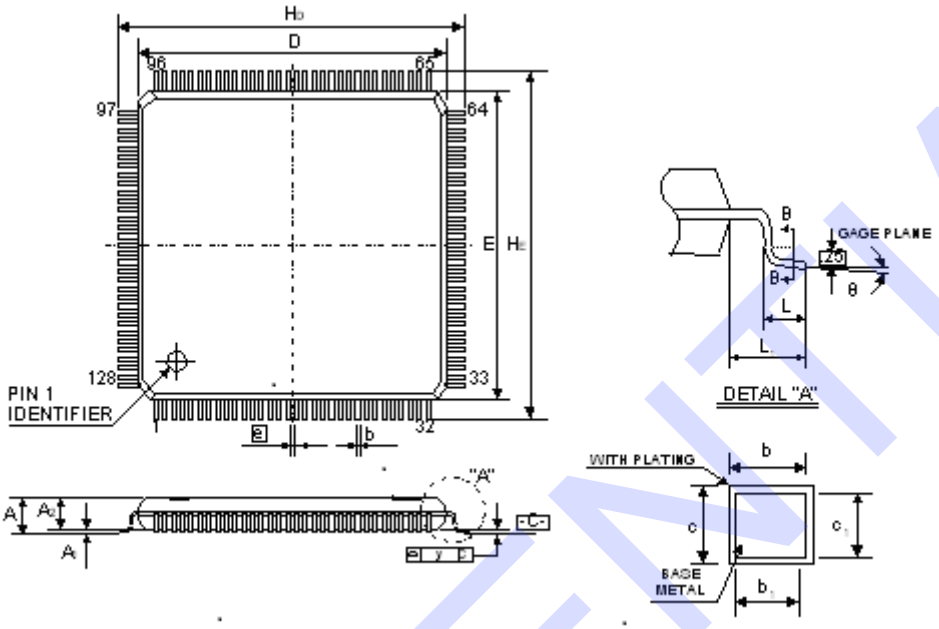
10. Package Information

LQFP 128(14*14) Outline Dimensions (For IT8951E/IT8951E-64) unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.063	-	-	1.60
A1	0.002	-	-	0.05	-	-
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.005	0.007	0.009	0.13	0.18	0.23
c	0.004	-	0.008	0.09	-	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.547	0.551	0.555	13.90	14.00	14.10
e	0.016 BSC			0.40 BSC		
H_D	0.624	0.630	0.636	15.85	16.00	16.15
H_E	0.624	0.630	0.636	15.85	16.00	16.15
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	0.039 REF			1.00 REF		
y	-	-	0.004	-	-	0.10
θ	0°	3.5°	7°	0°	3.5°	7°

Notes:
1. Dimensions D and E do not include mold protrusion.
2. Dimensions b does not include dambar protrusion.
3. Total in excess of the b dimension at maximum material condition.
4. Dambar cannot be located on the lower radius of the foot.
5. Controlling dimensions: Millimeter
6. Reference document: JEDEC MS-026

DI-LQFP128(14*14)v4

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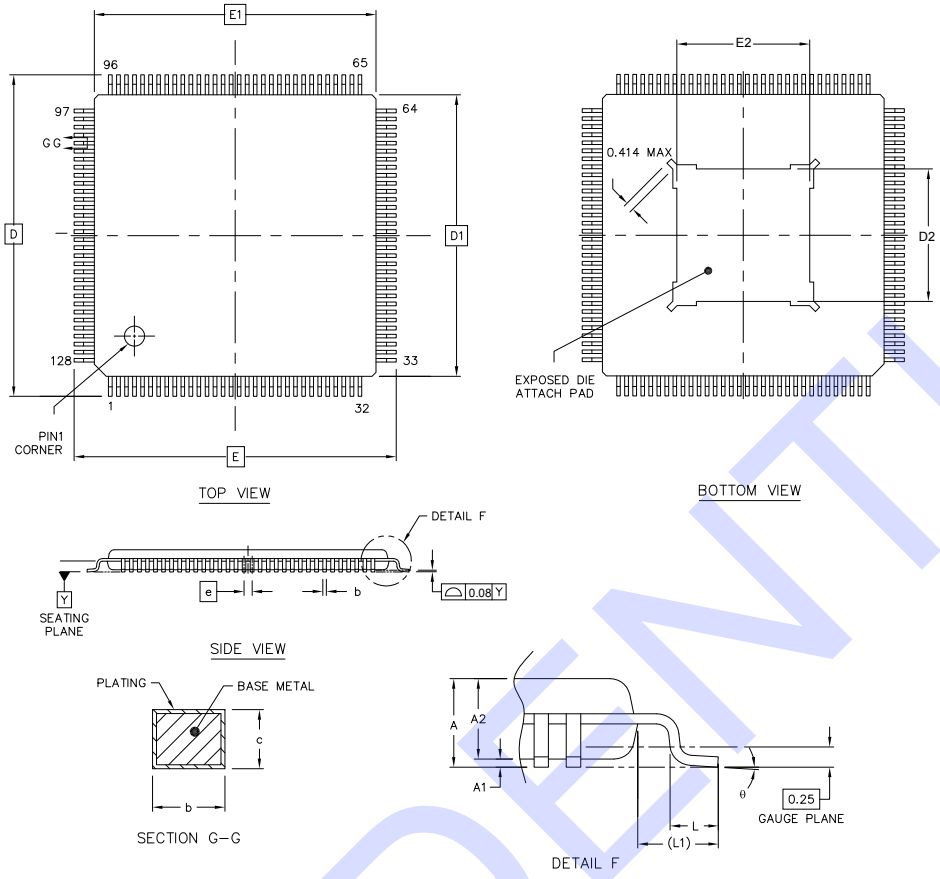
TQFP 128L Outline Dimensions (For IT8951TE) unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.047	-	-	1.20
A1	0.002	-	0.006	0.05	-	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.005	0.007	0.009	0.13	0.18	0.23
c	0.004	-	0.008	0.09	-	0.20
D / E	0.630 BSC			16.00 BSC		
D1 / E1	0.551 BSC			14.00 BSC		
D2 / E2	0.256	0.260	0.264	6.5	6.6	6.7
e	0.016 BSC			0.40 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	0.039 REF			1.00 REF		
θ	0^o	3.5^o	7^o	0^o	3.5^o	7^o

Notes:

1. Dimensions D1 and E1 do not include mold protrusion. But mold mismatch is included.
2. Dimensions b does not include dambar protrusion.
3. Controlling dimension: Millimeter

DI-E(260*260MIL)-TQFP128(14*14)v0

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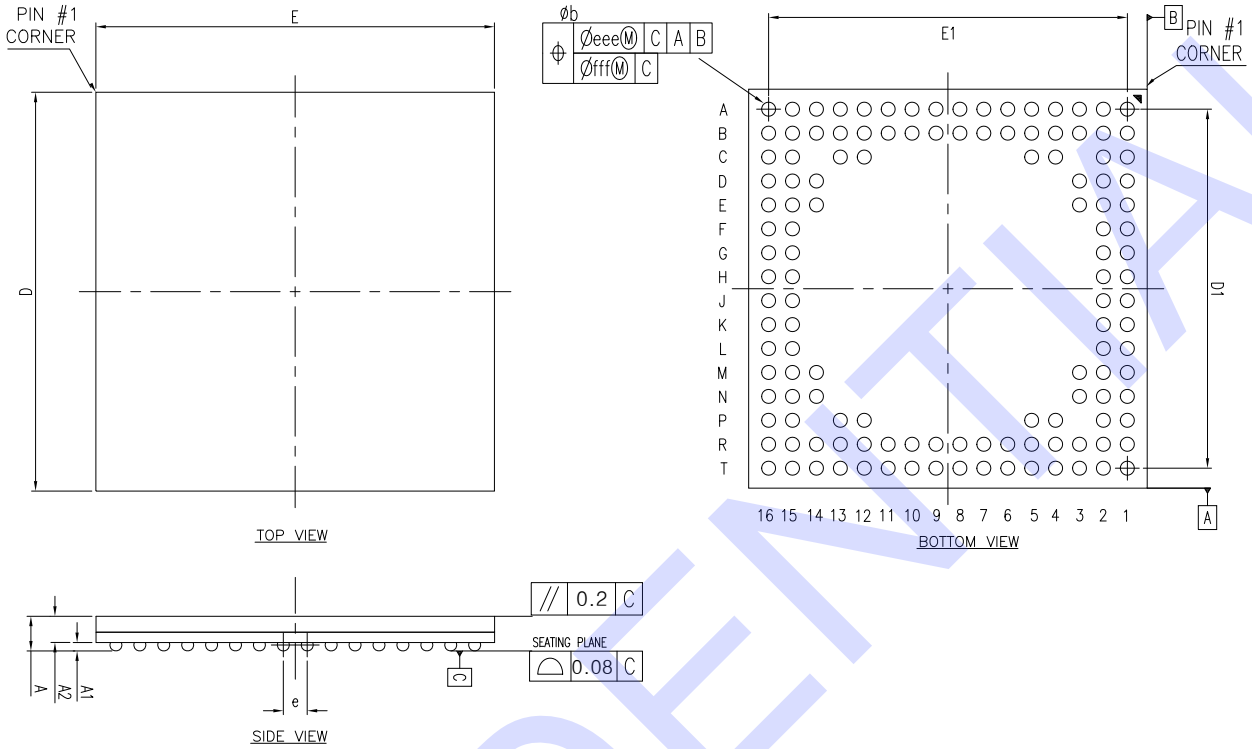
VFBGA 128(10*10) Outline Dimensions (For IT8951VG) unit: inches/mm

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	0.039	---	---	0.99
A1	0.006	0.008	0.010	0.16	0.21	0.26
A2	0.023	0.026	0.029	0.59	0.66	0.73
D / E	0.390	0.394	0.398	9.90	10.00	10.10
D1 / E1	0.354 BSC			9.0 BSC		
e	0.024 BSC			0.6 BSC		
b	0.010	0.012	0.014	0.25	0.30	0.35
eee	0.006			0.15		
fff	0.003			0.08		
MD/ME	16/16			16/16		

Notes:
1. Controlling dimensions: Millimeter
2. Reference document: JEDEC MO-195

DI-VFBGA128(10*10)v1

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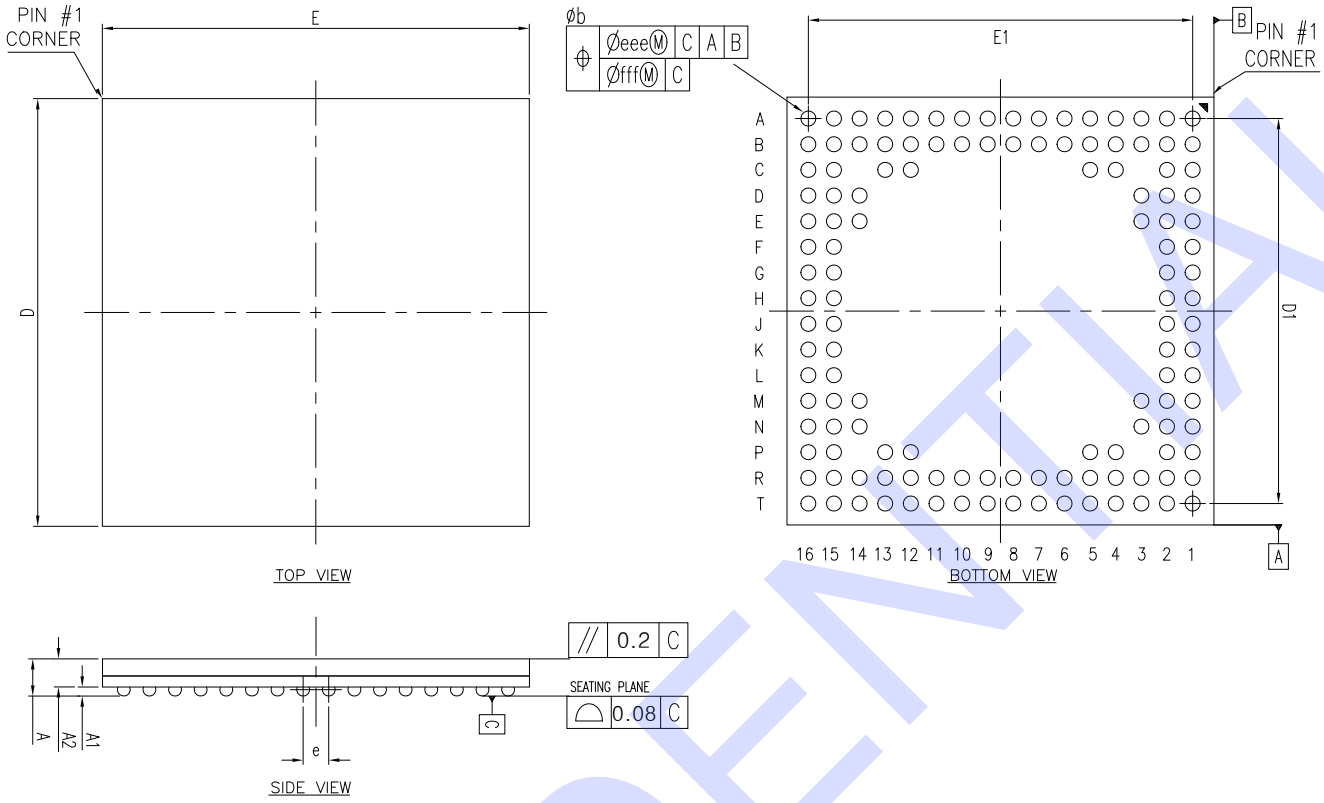
VFBGA 128(10.5*10.5) Outline Dimensions (IT8951VG-64)

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	0.039	---	---	0.99
A1	0.006	0.008	0.010	0.16	0.21	0.26
A2	0.023	0.026	0.029	0.59	0.66	0.73
D / E	0.409	0.413	0.417	10.40	10.50	10.60
D1 / E1	0.354 BSC			9.0 BSC		
e	0.024 BSC			0.6 BSC		
b	0.010	0.012	0.014	0.25	0.30	0.35
eee	0.006			0.15		
fff	0.002			0.05		
MD/ME	16/16			16/16		

Notes:
1. Controlling dimensions: Millimeter
2. Reference document: JEDEC MO-195

DI-VFBGA128(10.5*10.5)v0

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11. Ordering Information

Part No.	Package	DRAM
IT8951E/DX	LQFP 128L	32Mb
IT8951TE/DX	TQFP 128L	32Mb
IT8951VG/DX	VFBGA 128	32Mb
IT8951E-64/DX	LQFP 128L	64Mb
IT8951VG-64/DX	VFBGA 128	64Mb

All green components provided are in compliance with RoHS, and Halogen-Free.

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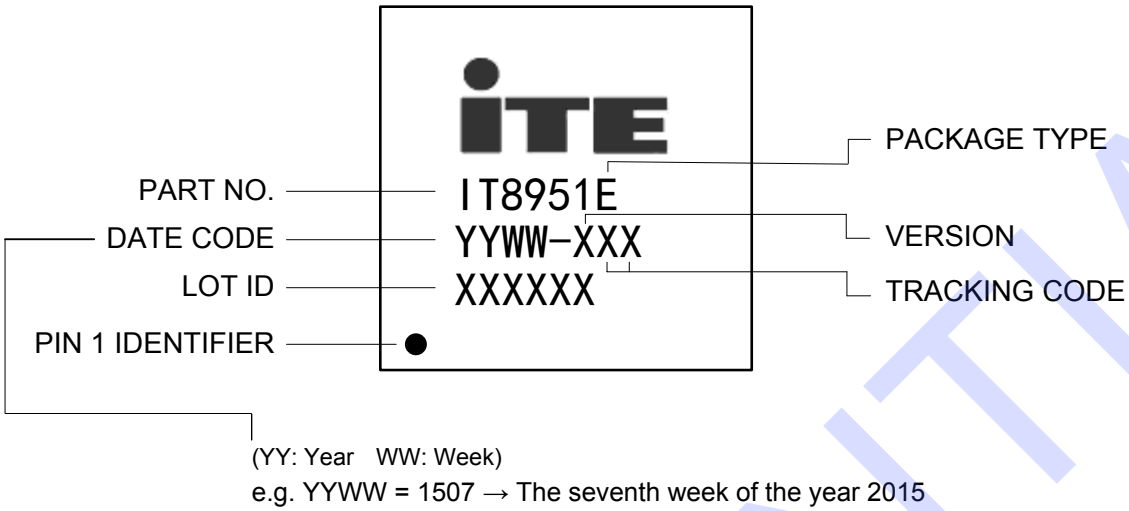
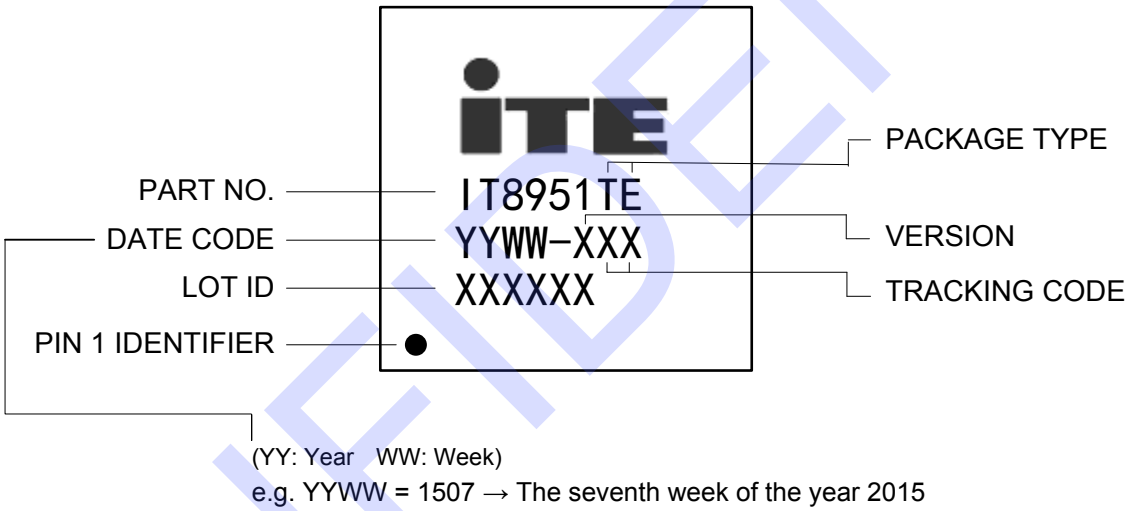
12. Top Marking Information

IT8951E



(YY: Year WW: Week)
e.g. YYWW = 1507 → The seventh week of the year 2015

IT8951TE



(YY: Year WW: Week)
e.g. YYWW = 1507 → The seventh week of the year 2015

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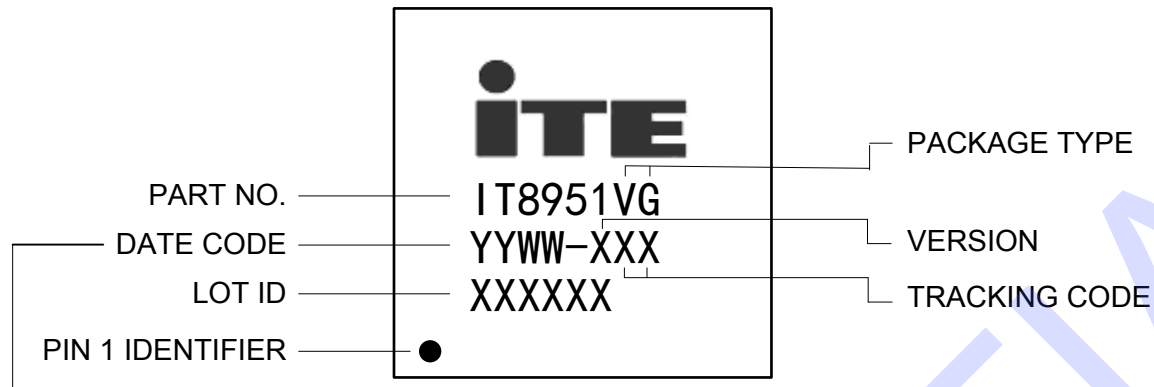
IT8951VG

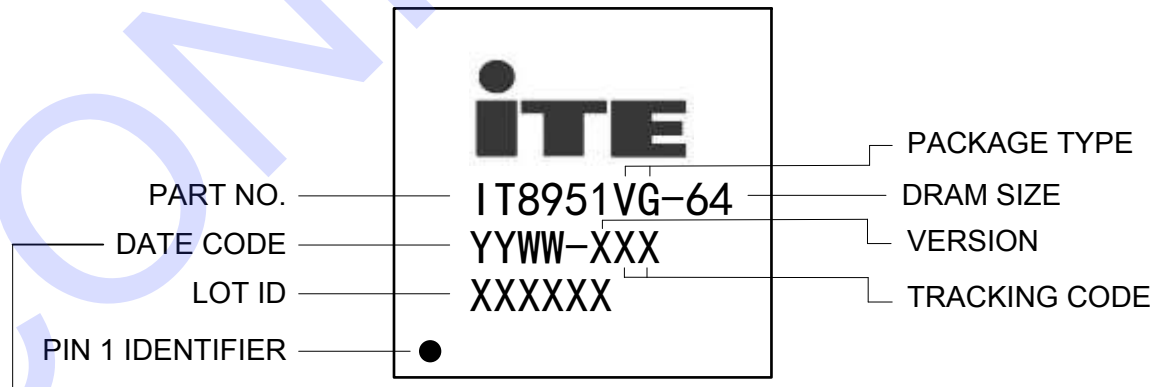


(YY: Year WW: Week)
e.g. YYWW = 1507 → The seventh week of the year 2015

IT8951E-64

(YY: Year WW: Week)
e.g. YYWW = 1507 → The seventh week of the year 2015

IT8951VG-64



(YY: Year WW: Week)
e.g. YYWW = 1507 → The seventh week of the year 2015

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ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2013)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc.

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Otherwise specified in the order agreed by Seller, delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.
(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.
(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.
(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.
(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.
(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.
(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and by its conditions Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.
(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.
(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.
(c) Buyer will not return any goods without first obtaining a customer return order number.
(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.

(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.
(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.

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