

Title: <b>BLOCK DIAGRAM</b>	Revision: <b>V4.2.1</b>
Size: <b>A4</b>	Project: <b>Nereid.PrjPcb</b>
Date: <b>11/14/2017</b>	Time: <b>10:30:24 AM</b>
File: <b>Nereid.SchDoc</b>	Sheet <b>1</b> of <b>10</b>

**Numato Systems Pvt.Ltd**



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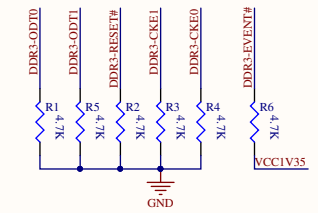
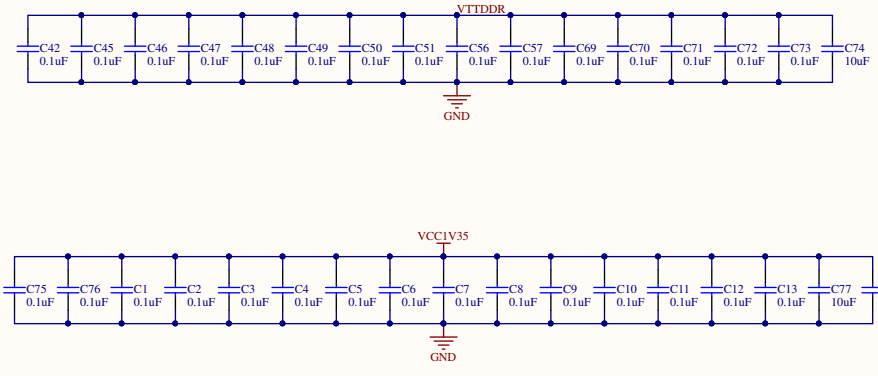
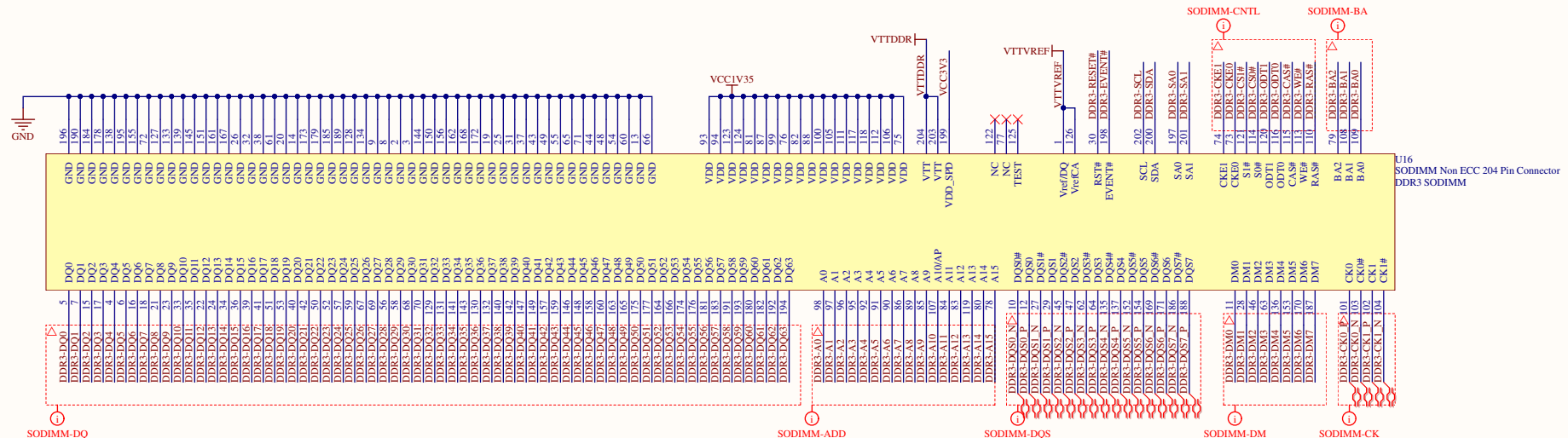
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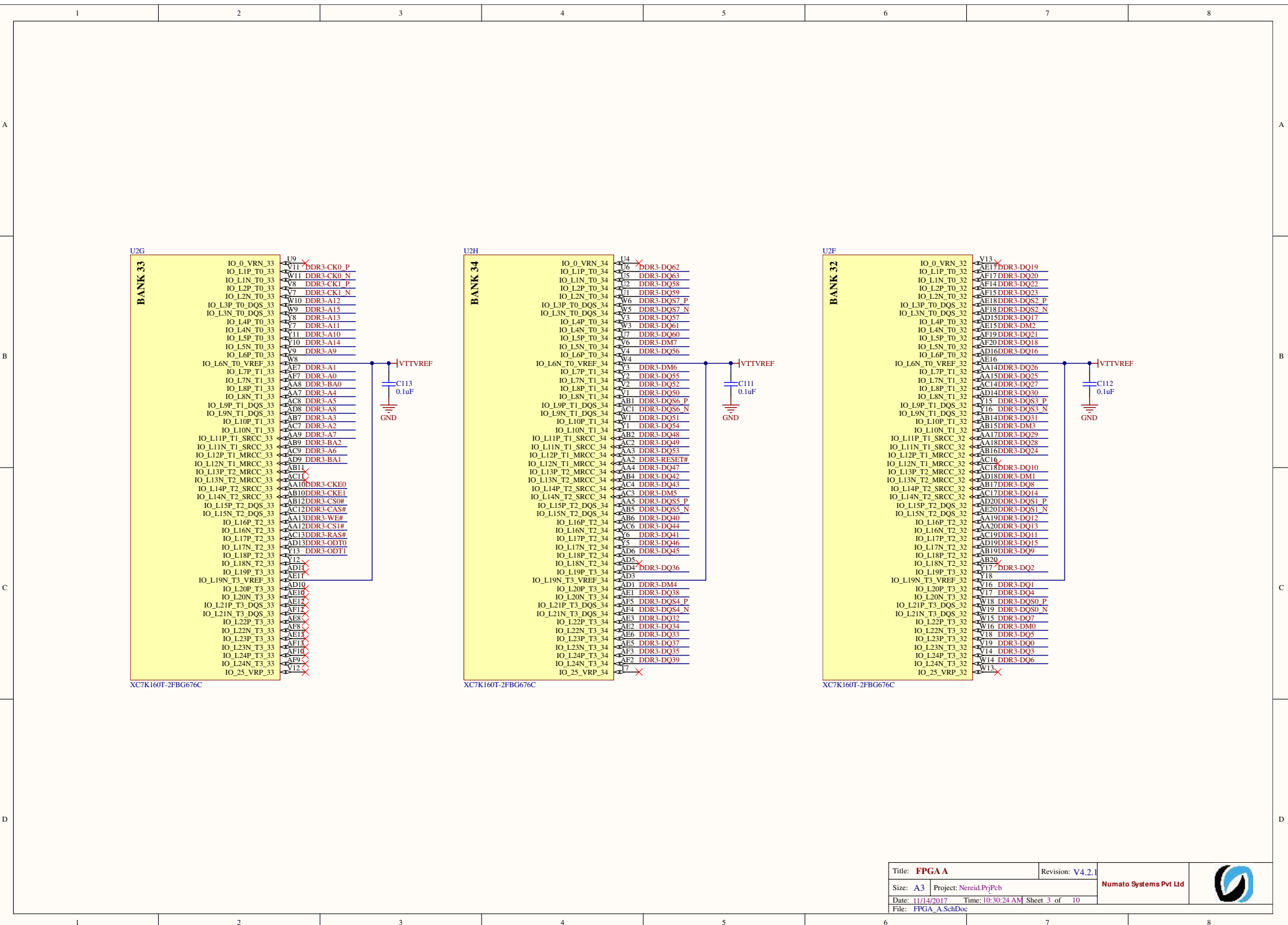
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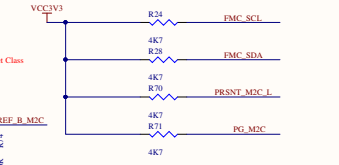
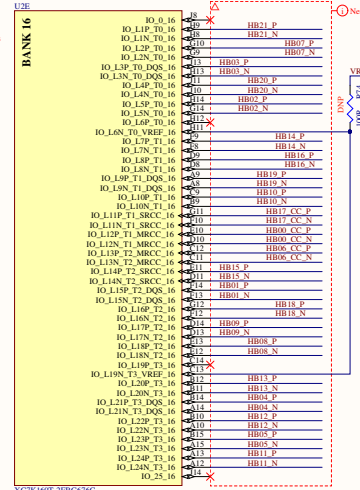
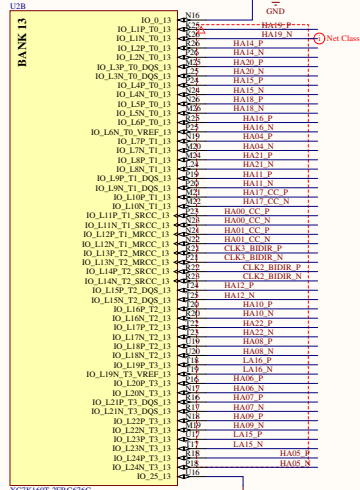
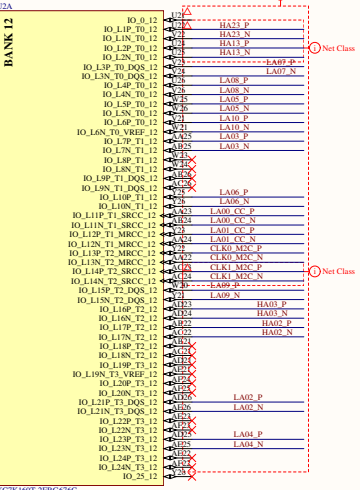
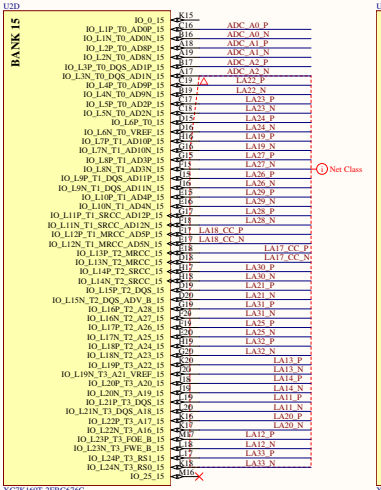
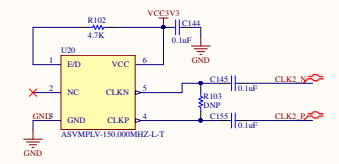
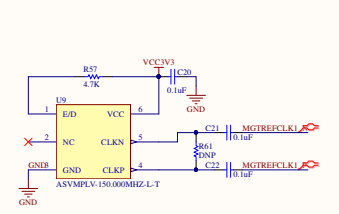
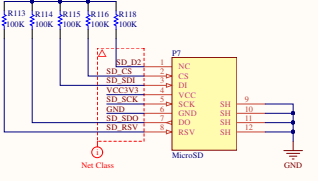
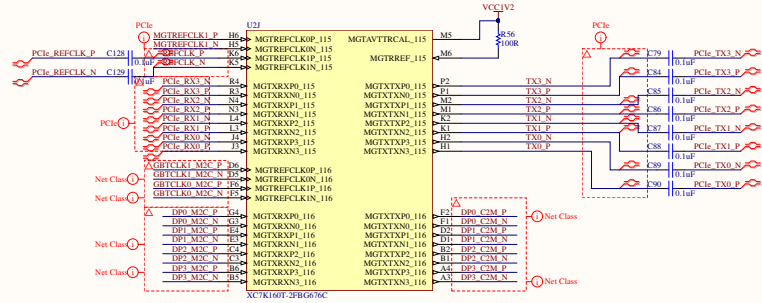
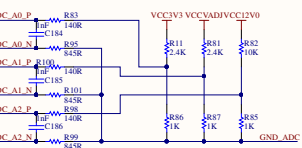
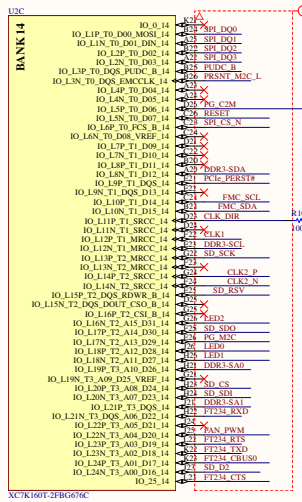
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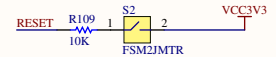
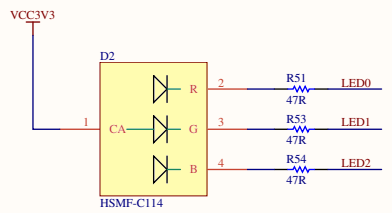
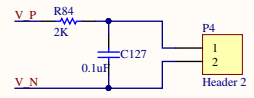
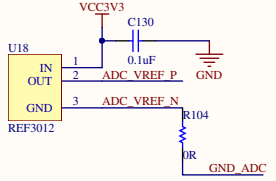
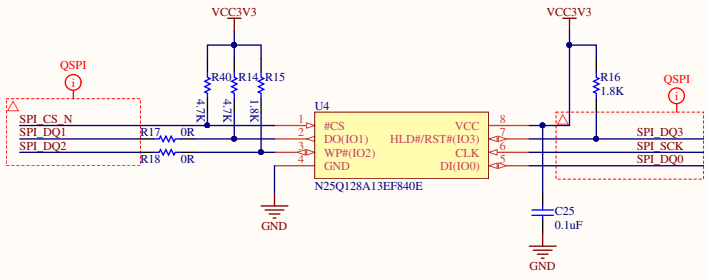
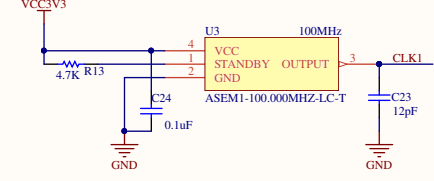
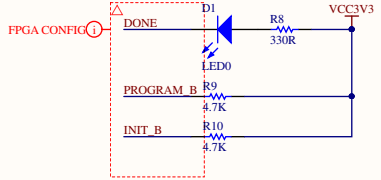
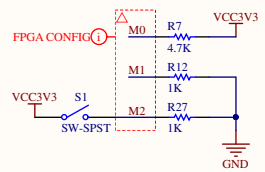
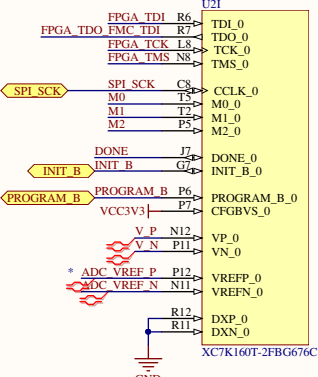
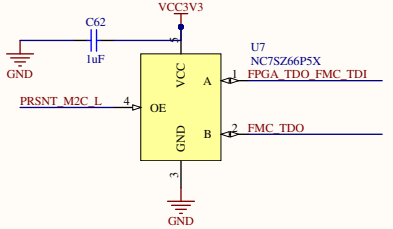
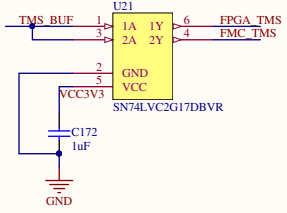
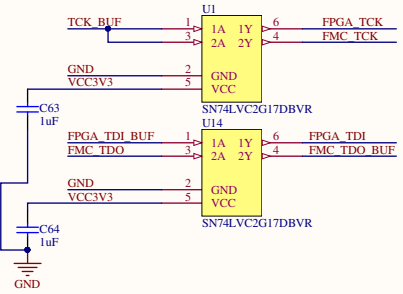
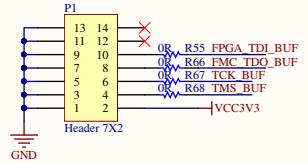
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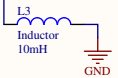
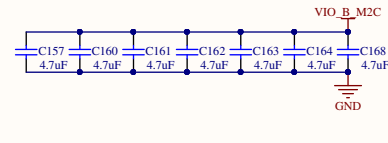
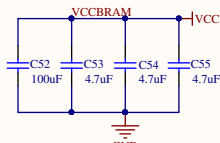
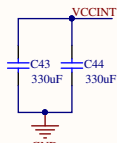
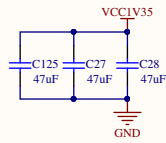
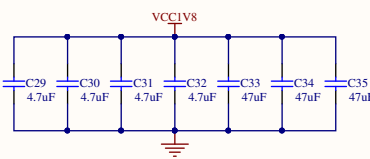
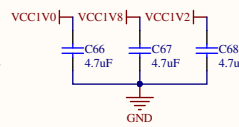
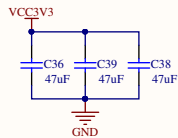
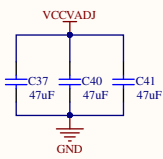
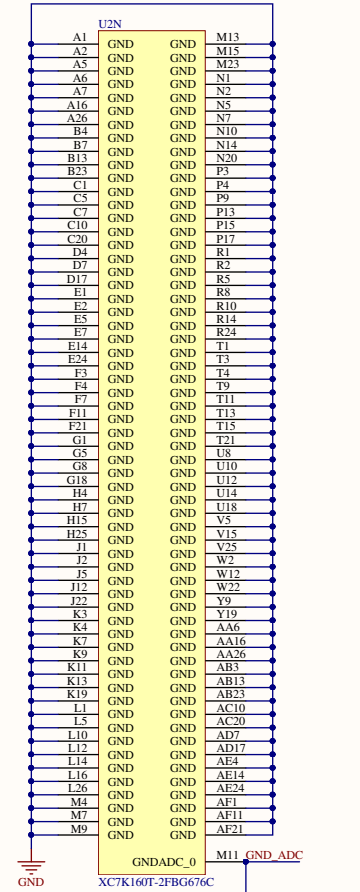
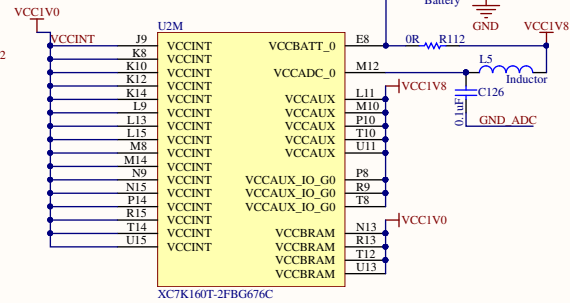
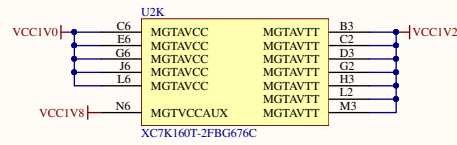
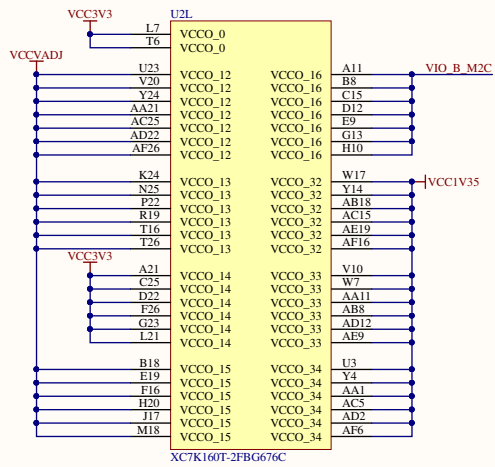
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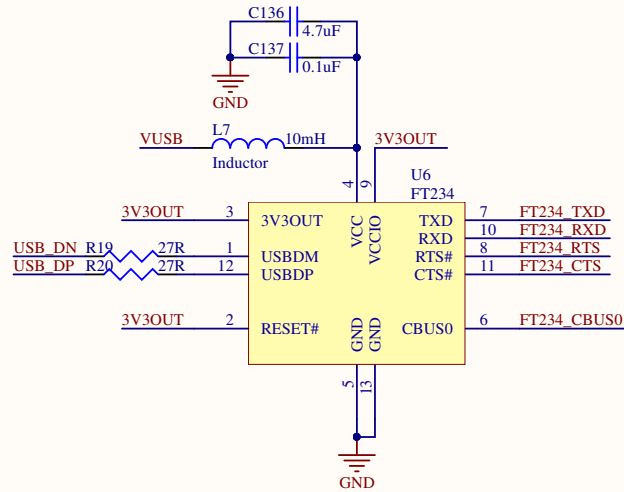
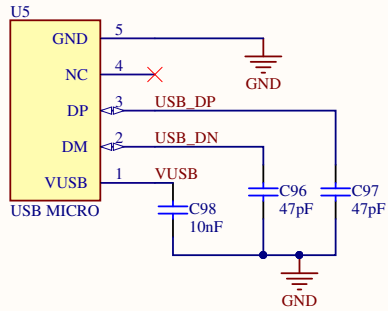
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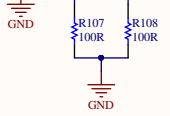
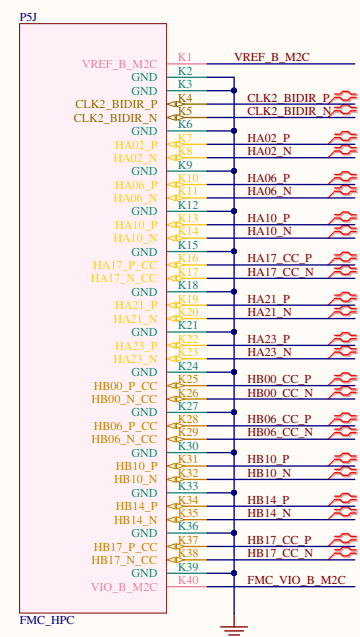
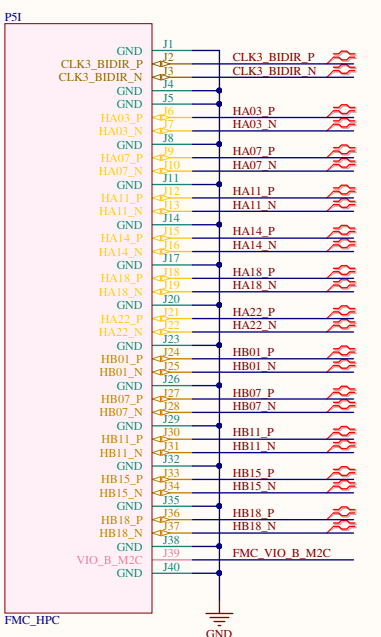
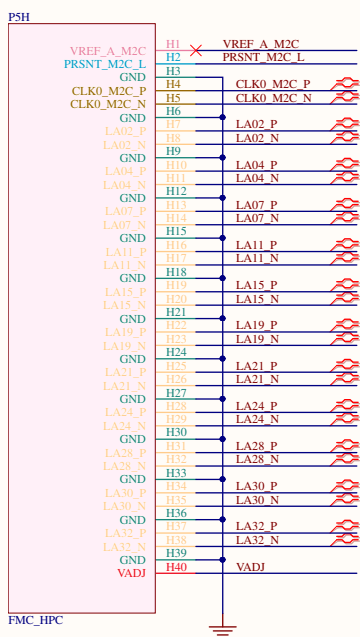
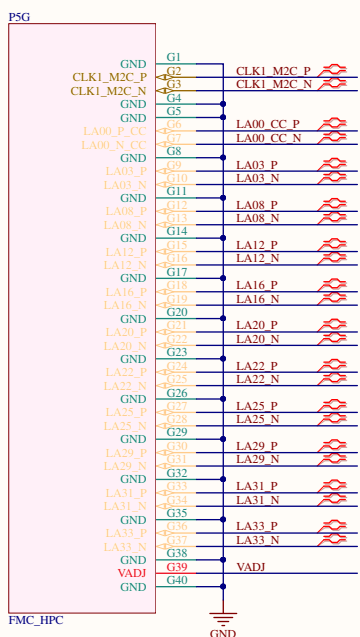
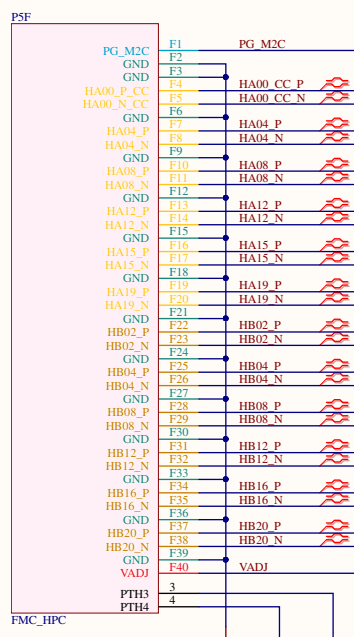
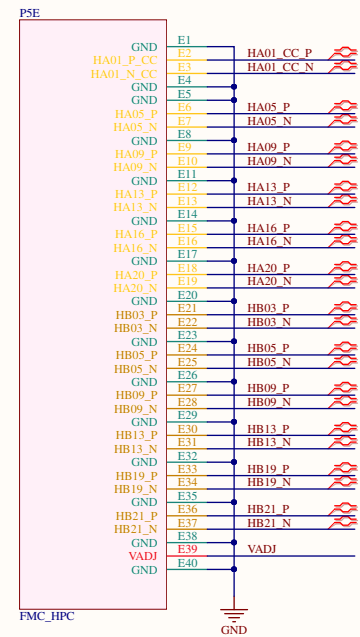
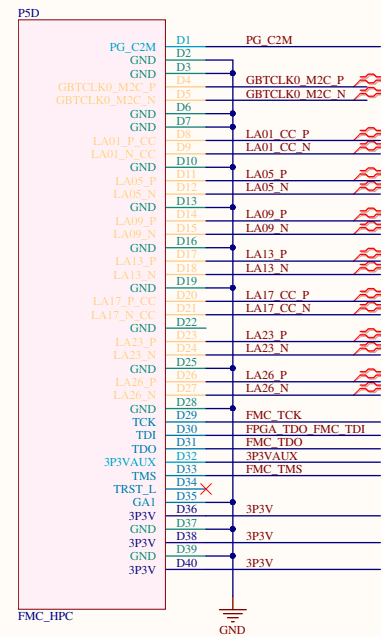
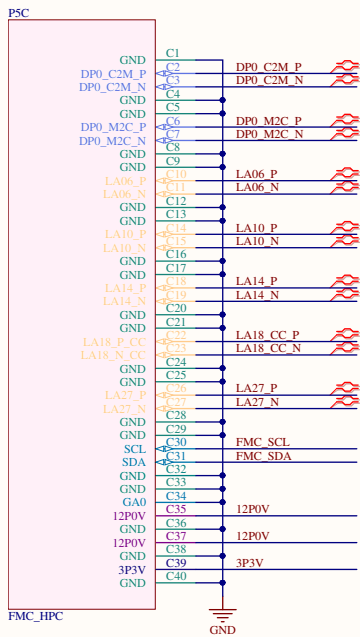
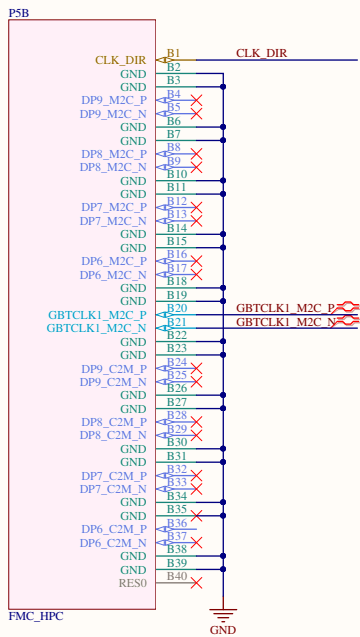
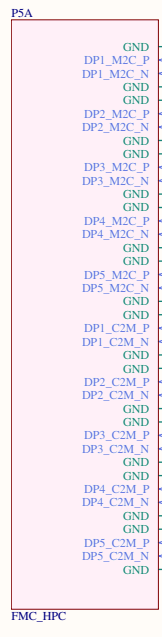


\*The VRefP and VRefN lines should be treated in a similar way to the analog inputs themselves. The two lines should be routed as close as possible to one another. They should be shielded vertically and horizontally by a low-impedance quiet ground or quiet supply, such as GNDADC or VCCADC.

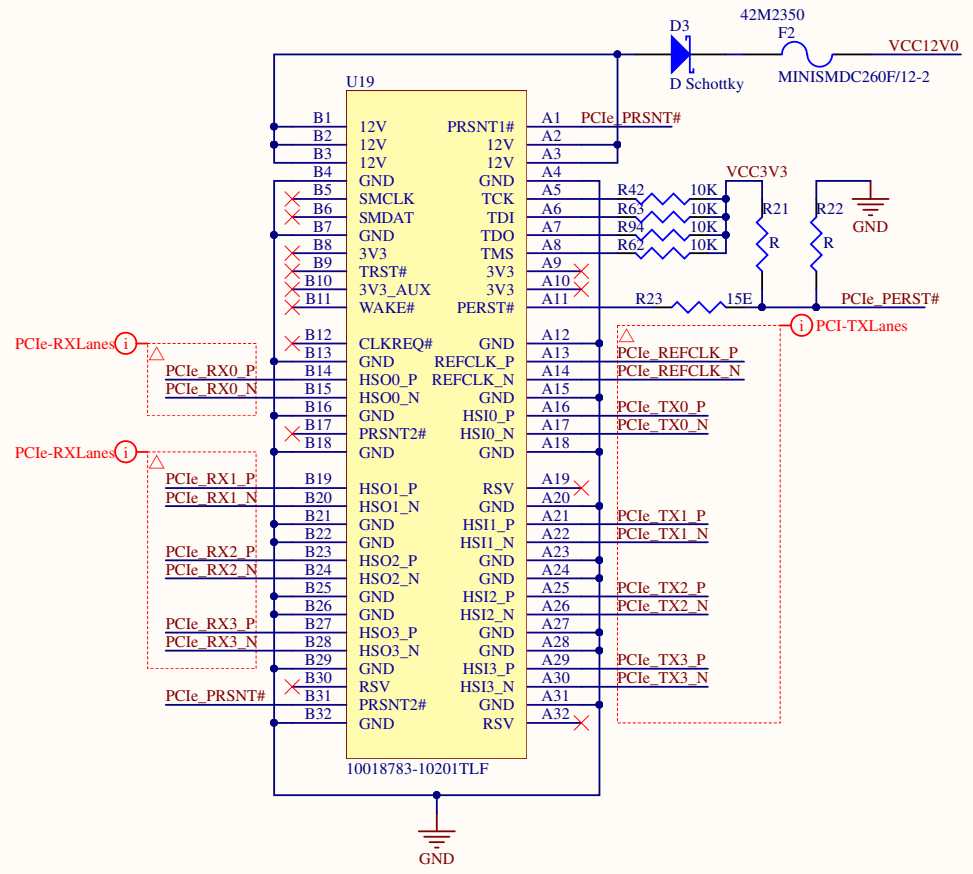





Title: <b>FT234XD</b>		Revision: <b>V4.2.1</b>	
Size: <b>A4</b>	Project: <b>Nereid.PrjPcb</b>		
Date: <b>11/14/2017</b> Time: <b>10:30:25 AM</b> Sheet <b>7</b> of <b>10</b>			
File: <b>FT234XD.SchDoc</b>			







Title: <b>PCIe</b>		Revision: <b>V4.2.1</b>	 <b>Numato Systems Pvt Ltd</b>
Size: <b>A4</b>	Project: <b>Nereid.PrjPcb</b>		
Date: <b>11/14/2017</b>	Time: <b>10:30:26 AM</b> Sheet <b>9</b> of <b>10</b>		
File: <b>PCIe.SchDoc</b>			

