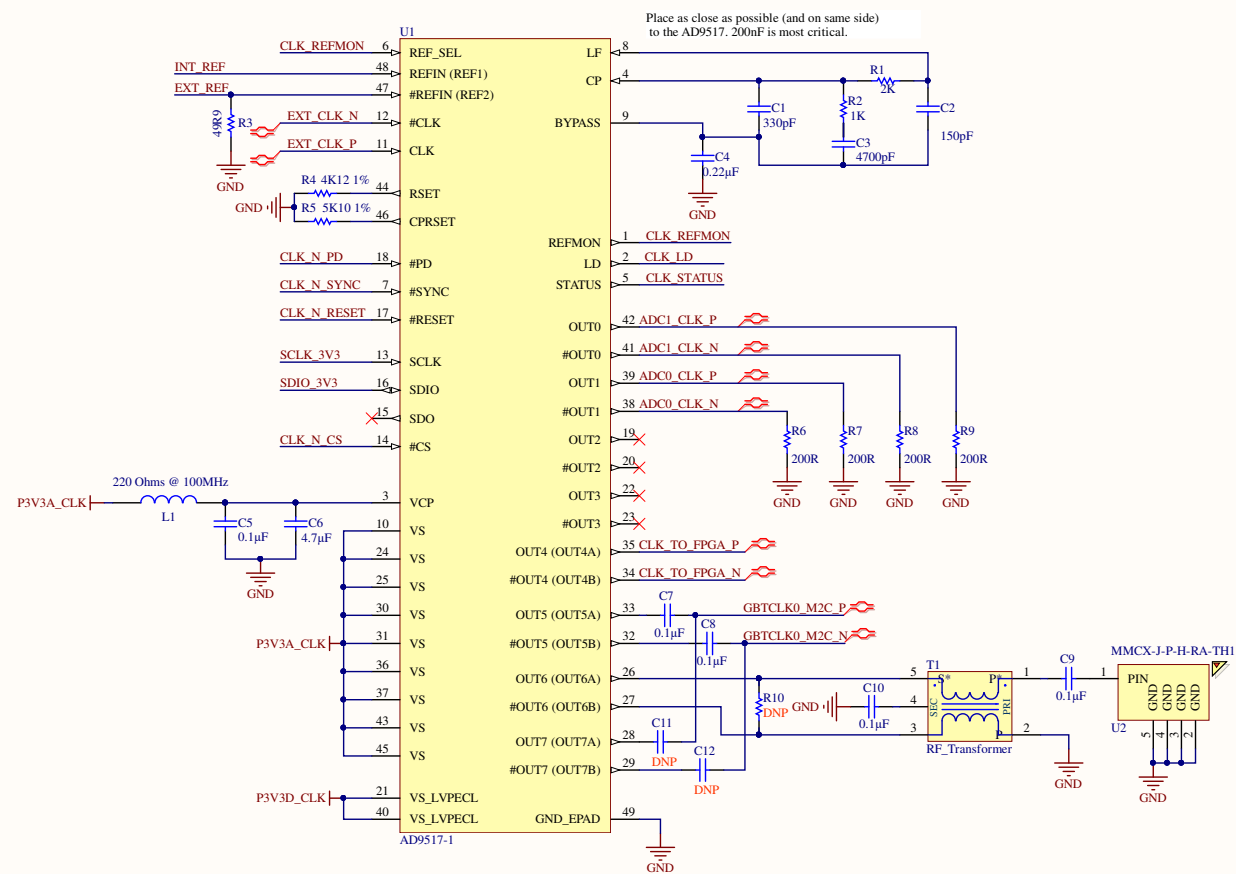
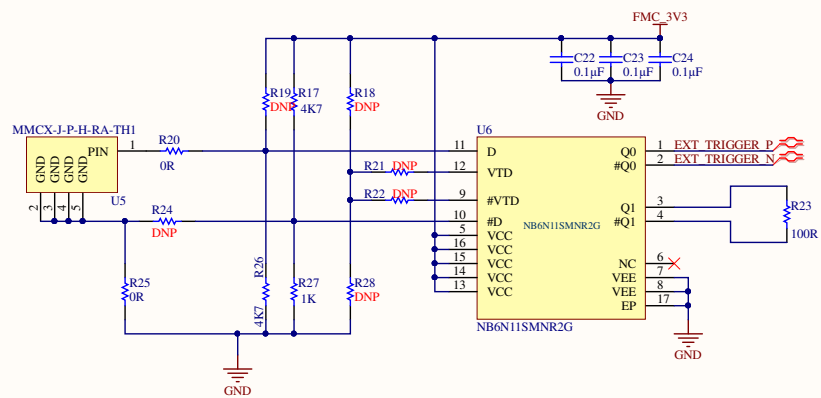
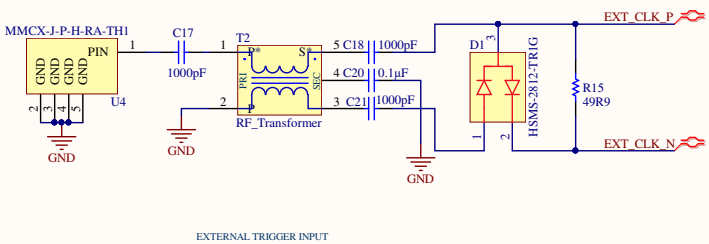
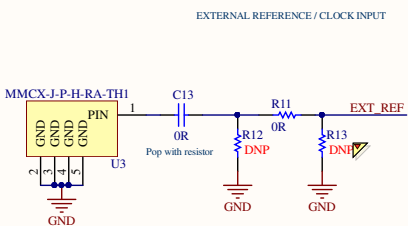
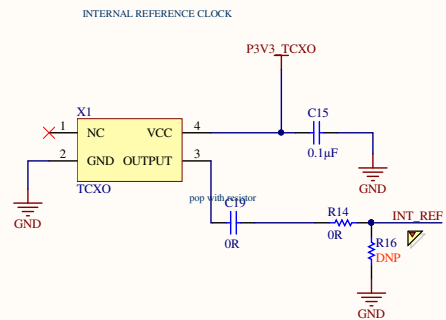
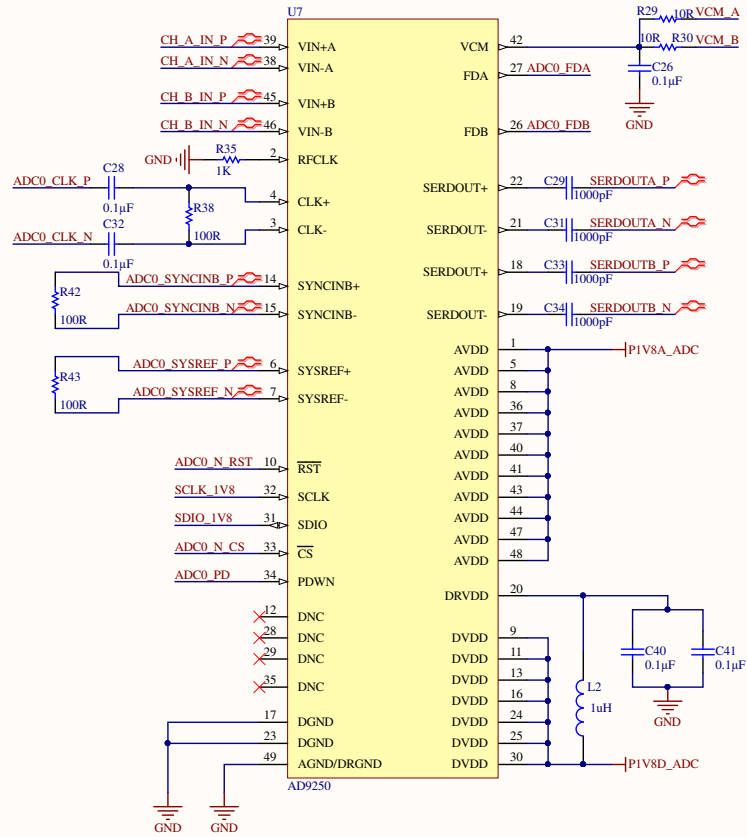
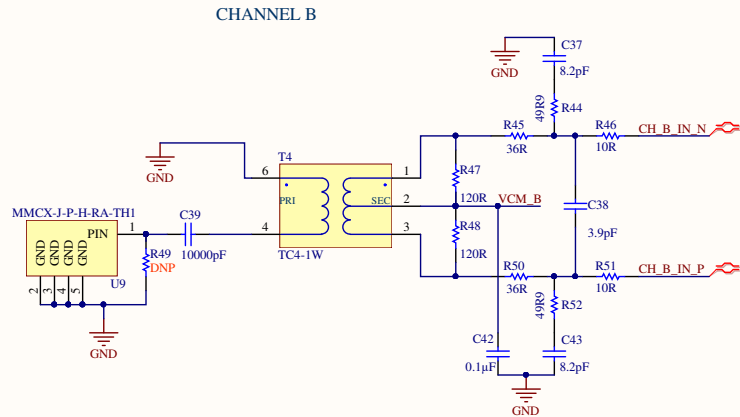
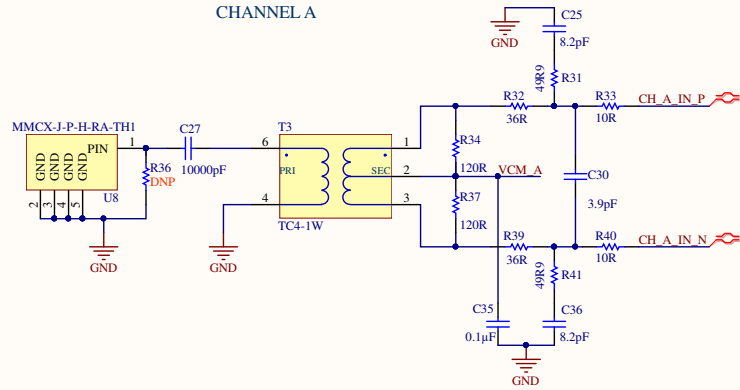


Phase Locked Loop and Clock distribution

Place as close as possible (and on same side) to the AD9517. 200nF is most critical.

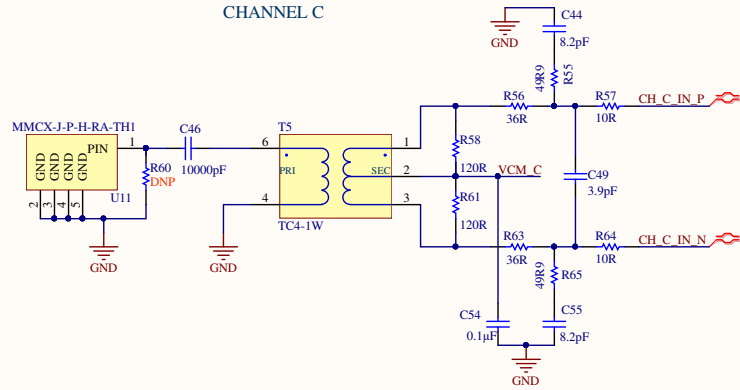


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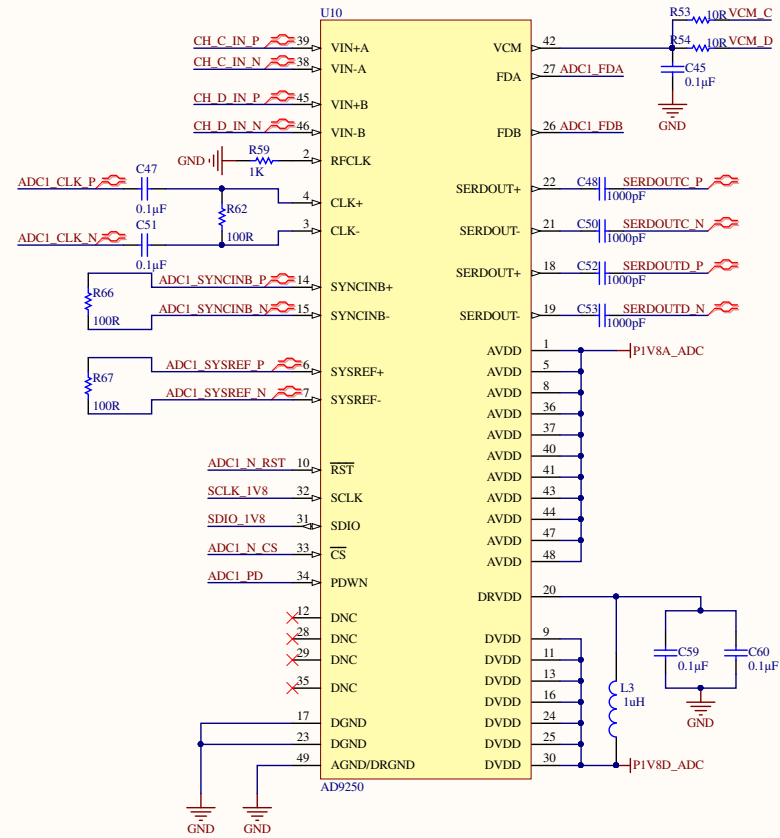
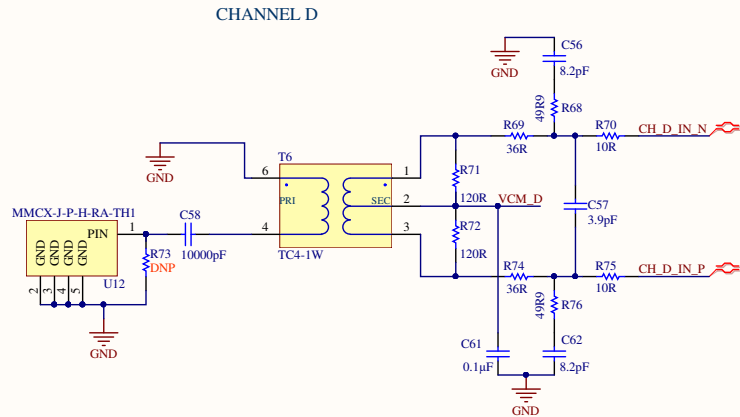


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CHANNEL C



CHANNEL D



DECOUPLING CAPACITORS

