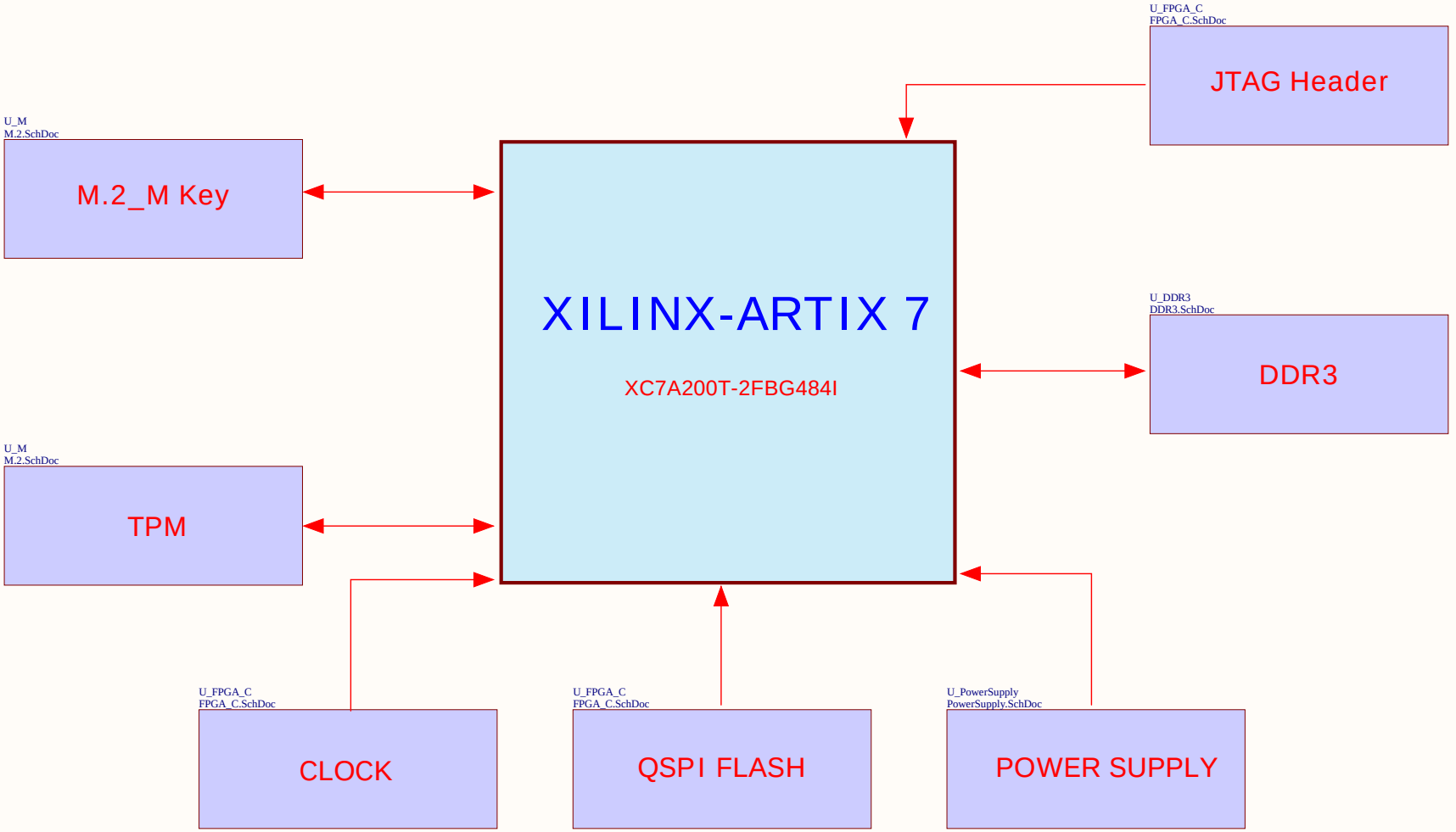
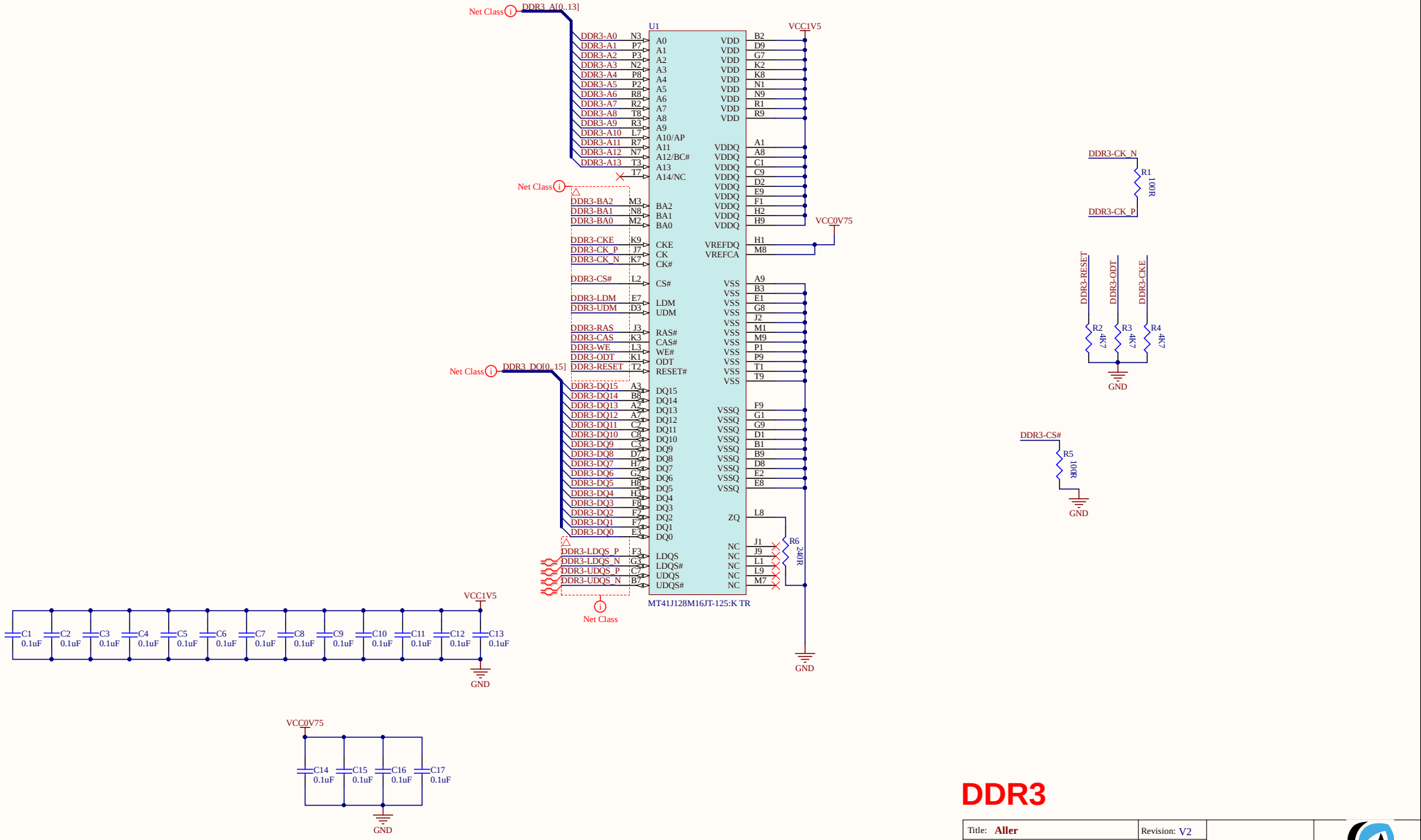


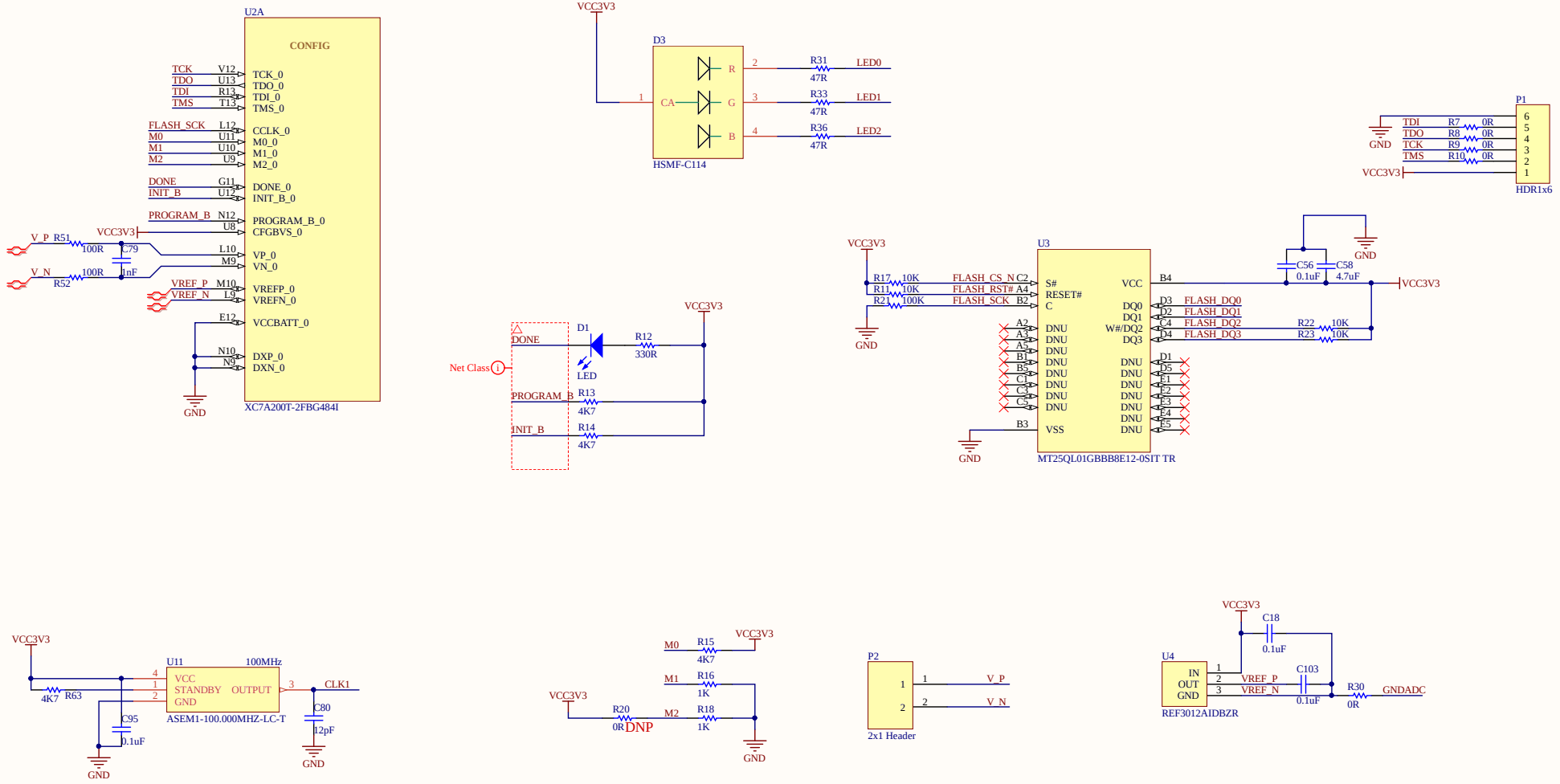
Block Diagram

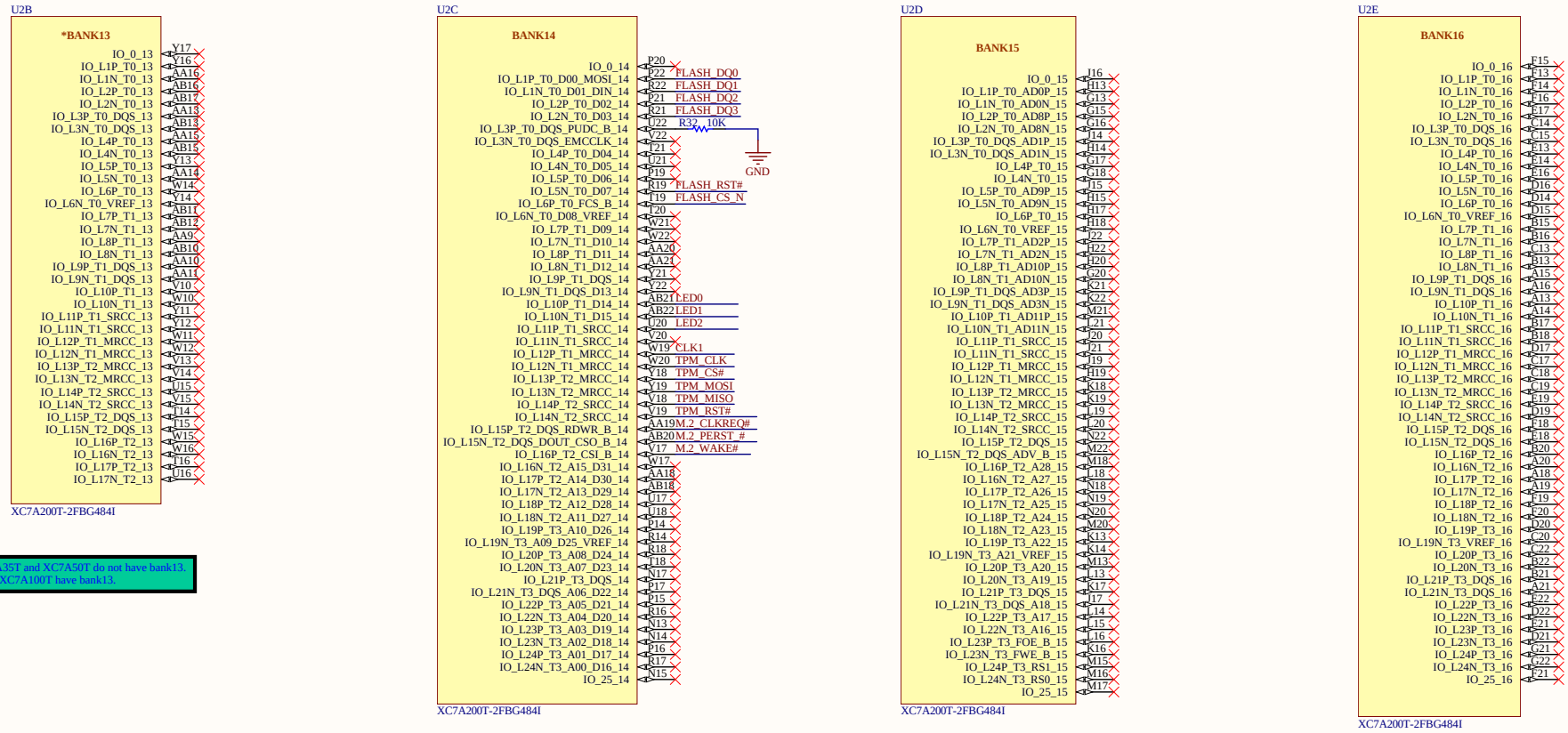
Title: Aller		Revision: V2	Numato Systems Pvt Ltd
Size: A3	Project: Aller.PrjPcb		
Date: 15-05-2019	Time: 15:34:33	Sheet 1 of 8	
File: BlockDiagram.SchDoc			



DDR3

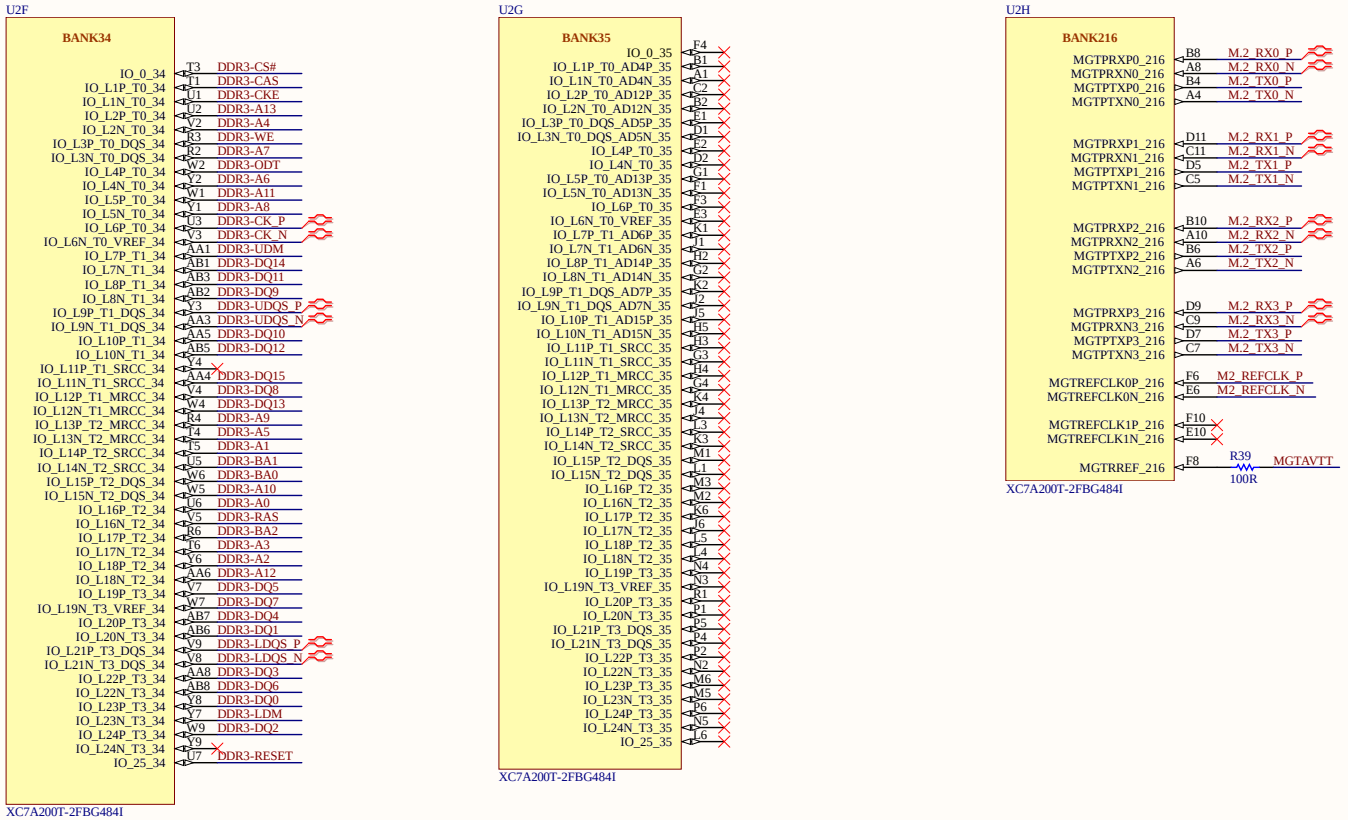
Title: **Aller**		Revision: V2	Numato Systems Pvt Ltd
Size: A3	Project: Aller.PrjPcb		
Date: 15-05-2019	Time: 15:34:33	Sheet 2 of 9	
File: DDR3.SchDoc			


U2A
CONFIG
TCK V12 TCK_0
TDO U13 TDO_0
TDI R13 TDI_0
TMS T13 TMS_0
FLASH_SCK L12 CCLK_0
M0 U11 M0_0
M1 U10 M1_0
M2 U9 M2_0
DONE G11 DONE_0
INIT_B U12 INIT_B_0
PROGRAM_B N12 PROGRAM_B_0
U8 CFGBVS_0
V_P R51 100R
V_N R52 100R
C79 1nF
VCC3V3
L10 VP_0
M9 VN_0
VREF_P M10 VREFP_0
VREF_N L9 VREFN_0
E12 VCCBATT_0
N10 DXP_0
N9 DXN_0
GND
XC7A200T-2FBG484I
VCC3V3
D3
R
G
B
CA
1
2
3
4
R31 47R LED0
R33 47R LED1
R36 47R LED2
HSMF-C114
P1
GND
TDI R7 0R
TDO R8 0R
TCK R9 0R
TMS R10 0R
VCC3V3
6
5
4
3
2
1
HDR1x6
VCC3V3
D1
DONE
Net Class 1
LED
R12 330R
PROGRAM_B R13 4K7
INIT_B R14 4K7
VCC3V3
U3
R17 10K FLASH_CS_N C2
R11 10K FLASH_RST# A4
R21 100K FLASH_SCK B2
S#
RESET#
C
VCC
B4
DQ0 D3 FLASH_DQ0
DQ1 D2 FLASH_DQ1
W#/DQ2 C4 FLASH_DQ2
DQ3 D4 FLASH_DQ3
C56 0.1uF
C58 4.7uF
R22 10K
R23 10K
VCC3V3
GND
DNU
VSS
B3
MT25QL01GBBB8E12-0SIT TR
VCC3V3
U11
100MHz
VCC
STANDBY
GND
OUTPUT
CLK1
4K7 R63
C95 0.1uF
C80 12pF
ASEM1-100.000MHZ-LC-T
GND
M0 R15 4K7
M1 R16 1K
M2 R18 1K
VCC3V3
R20 0R DNP
GND
P2
V_P
V_N
2x1 Header
VCC3V3
U4
IN
OUT
GND
C18 0.1uF
C103 0.1uF
VREF_P
VREF_N
R30 0R
GNDADC
REF3012AIDBZR
FPGA Configuration
Title: Aller
Revision: V2
Size: A3
Project: Aller.PrjPcb
Date: 15-05-2019
Time: 15:34:33
Sheet 3 of 9
File: FPGA_C.SchDoc
Numato Systems Pvt Ltd



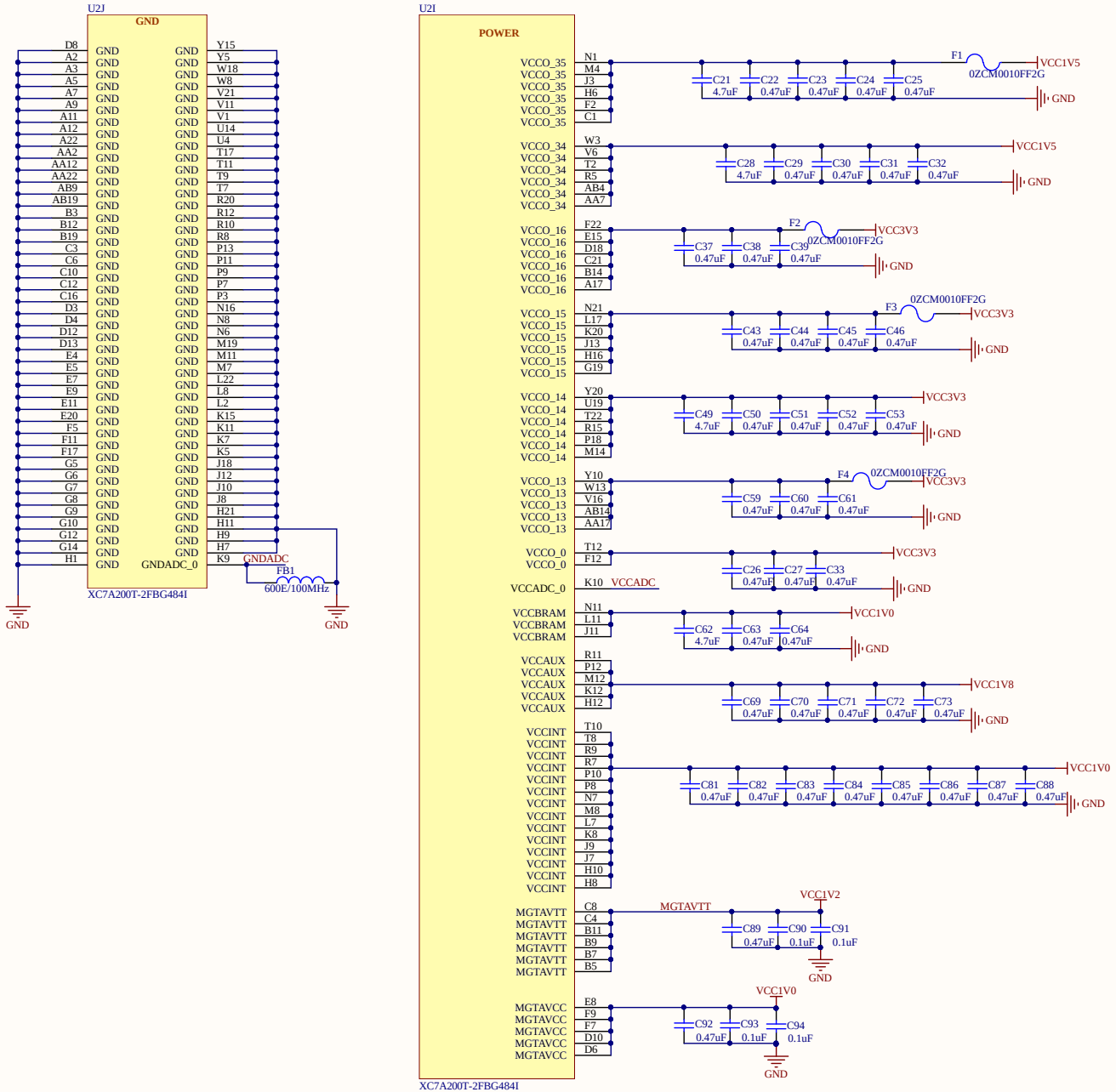
FLASH AND TPM BANKS

Title: Aller		Revision: V2	Numato Systems Pvt Ltd
Size: A3	Project: Aller.PrjPcb		
Date: 15-05-2019	Time: 15:34:34	Sheet 4 of 9	
File: FPGA_B.SchDoc			



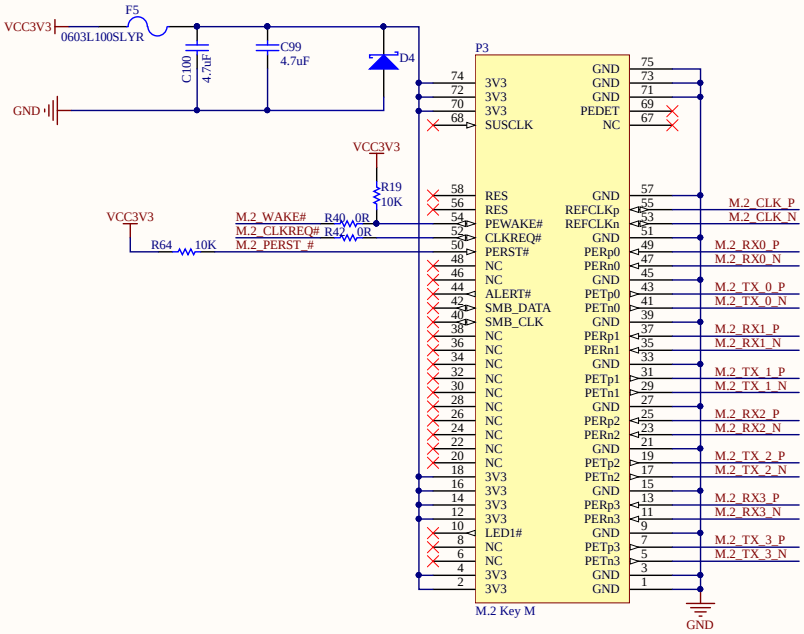
FPGA DDR3 and M.2 Banks

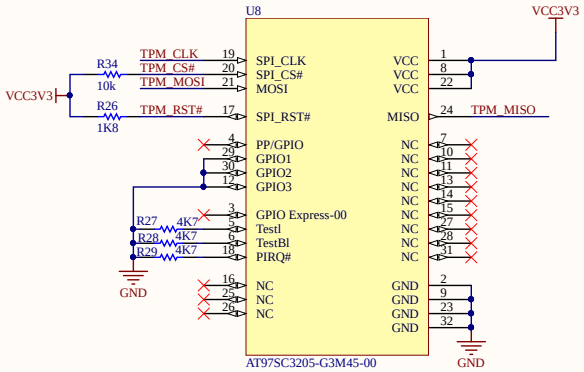
Title: Aller		Revision: V2	Numato Systems Pvt Ltd
Size: A3	Project: Aller.PrjPcb		
Date: 15-05-2019	Time: 15:34:34	Sheet 5 of 9	
File: FPGA_A.SchDoc			

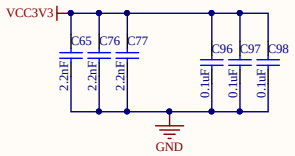


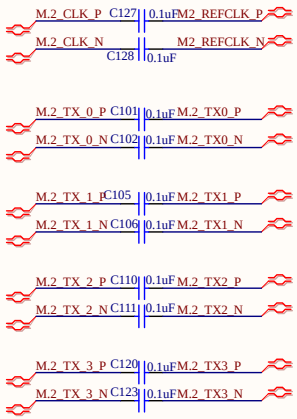
FPGA POWER

Title: Aller		Revision: V2	Numato Systems Pvt Ltd
Size: A3	Project: Aller.PrjPcb		
Date: 15-05-2019	Time: 15:34:34	Sheet 6 of 9	
File: FPGA_D.SchDoc			





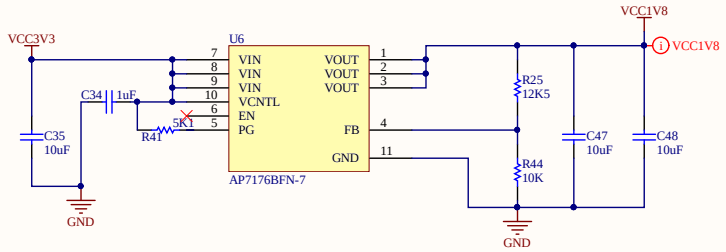




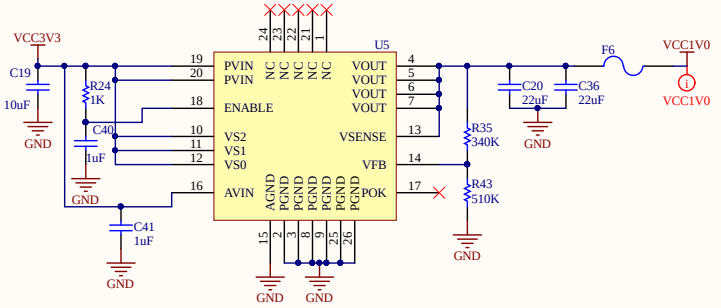
M.2 and TPM

Title: Aller		Revision: V2	Numato Systems Pvt Ltd
Size: A3	Project: Aller.PrjPcb		
Date: 15-05-2019	Time: 15:34:34	Sheet 8 of 9	
File: M.2.SchDoc			

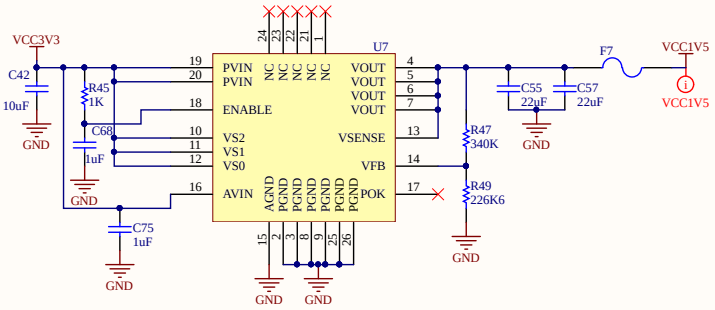
3V3 TO 1V8



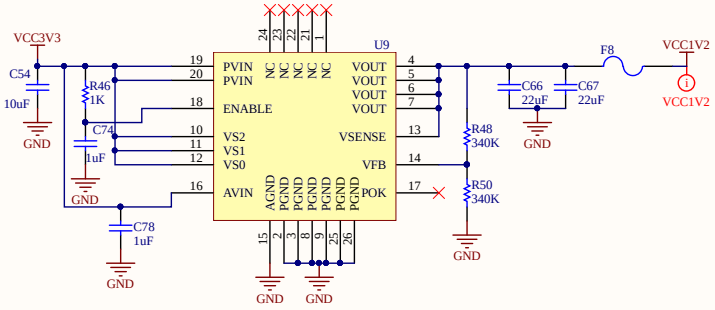
3V3 TO 1V0

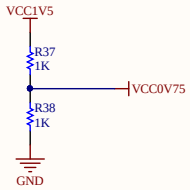


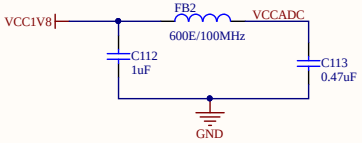
3V3 TO 1V5



3V3 TO 1V2







POWER SUPPLY

Title: Aller		Revision: V2	Numato Systems Pvt Ltd
Size: A3	Project: Aller.PrjPcb		
Date: 15-05-2019	Time: 15:34:34	Sheet 9 of 9	
File: PowerSupply.SchDoc			